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ADDITIONAL EXPERIMENTAL RESULTS RELEVANT TO TDMA-SYSTEM SYNCHRONIZATION

The Ohio State University
ElectroScience Laboratory

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13. ABSTRACT

In this report, experimental results are given which augment the technological basis established previously for designing and instrumenting time division multiple access (TDMA) satellite communications systems, in which two coupled sampled-data delay lock loops are used to perform the timing functions. Emphasis is placed on presenting information needed to design TDMA system synchronizers when only coarse estimates of signal parameters and the instantaneous system geometry are available a prior. Methods described in preceding reports for controlling loop gains automatically and for minimizing the effect of relative satellite/terminal motion on system timing errors are demonstrated to be both feasible and effective; the results given are related to analytical results documented previously. Techniques for acquiring the correct system timing relationships are also considered.

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FOREWORD

This report, OSURF 2738-8, was prepared by the ElectroScience Laboratory, Department of Electrical Engineering, The Ohio State University Research Foundation, Columbus, Ohio. Research was conducted under contract F30602-69-C-0112, Job Order Number 45190000, for Rome Air Development Center, Griffiss Air Force Base, New York. Mr. Thomas F. Treadway (CORR) was the RADC Program Monitor for this research.

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ADDITIONAL EXPERIMENTAL RESULTS RELEVANT TO TDMA-SYSTEM SYNCHRONIZATION

I. INTRODUCTION

Methods for instrumenting time division multiple access (TDMA) satellite communications systems have been investigated extensively at The Ohio State University ElectroScience Laboratory since 1965. As a result of this work, a basis for designing practical and effective TDMA systems has been established which includes both analytical and experimental results. System concepts, synchronization techniques, and associated design information were documented previously[1]-[8]. The purposes of the present report are to describe a second-generation experimental synchronizer instrumented to provide additional experimental data which augment the results reported previously.

In the new synchronizer, two coupled sampled-data delay lock loops (SDDLLs) are employed to provide the required receive and transmit timing information as in the original equipment. One loop -- the clock loop -- tracks the arrival time of a pulsed-envelope network clock signal (NCS); the second loop -- the ranging loop -- controls the transmit time base so that the transmitted pulses arrive at the satellite in the assigned time intervals (slots). Design changes were incorporated into the second-generation synchronizer to permit the usefulness of several concept refinements and alternative instrumentation approaches to be determined. The time base correction subsystems now contain digital circuits only rather than a combination of analog and digital circuits, and a capability is provided for introducing the clock loop corrections into the ranging loop in an inverted sense on an open-loop basis. The open-loop correction or "cross-strapping" operation reduces the amount by which the synchronization error accumulates

between ranging loop (transmit time base) correction instants due to relative motion between the terminal and the satellite[2],[5]. Also, the automatic gain control (AGC) technique described in reference [1] has been incorporated into the new synchronizer. A more complete description of circuit modifications is given in Section II; the additional experimental results obtained are presented in Section III.

In addition to determining the in-lock performance of the synchronizer, methods for acquiring lock in both the clock and ranging loops have been investigated. For the clock loop to acquire properly, the network clock signal must be separable from the ranging, linking, and data carrying (pulsed) signals which are also present on the down-link. An estimate of the terminal to satellite range at the time of acquisition must either be available or provided by a separate subsystem to avoid an excessively long ranging-loop acquisition time and to minimize interference caused by the transmitted waveform before proper timing has been established. Methods for acquiring lock are described in Section IV. The results are summarized and conclusions drawn in Section V.

II. DESCRIPTION OF THE EXPERIMENTAL SYNCHRONIZER

A block diagram of the experimental synchronizer is shown in Fig. 1. Subassemblies which would have to be added to the synchronizer to instrument an operational TDMA modem are indicated by blocks drawn with dashed lines. The clock tracking loop synchronizes the time base of a continuous, locally-generated clock with the time base of a pulsed-envelope network clock signal (NCS) received on the down-link. A pseudo-noise (PN) code is used to biphase modulate the NCS during its on time. The code has a length M equal to 2^n-1 where n is the number of shift register stages used to instrument the code generator, and the duration of each code symbol (chip), Δ, equals the inverse of the rate at which the code generator is clocked: f_c^{-1}. The duration of each pulse

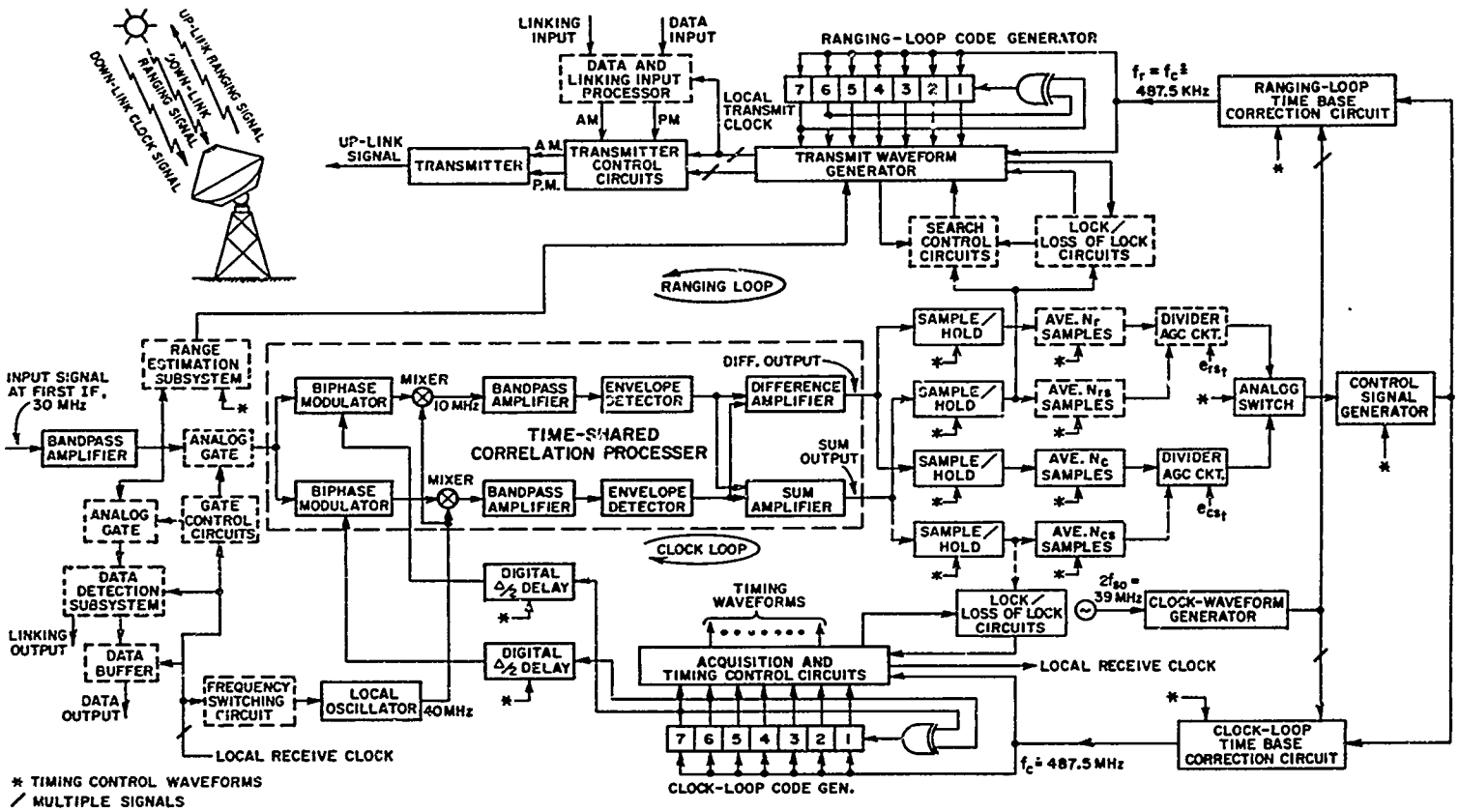

Fig. 1. Block diagram of the experimental synchronizer. Subassemblies which would have to be added to the synchronizer to instrument an operational TDMA modem are indicated by blocks drawn with dashed lines.

in the NCS equals the period of the code, $M\Delta$, and the envelope of the NCS has a period equal to $KM\Delta$ where K is a positive integer greater than one. The values assigned to several waveform and circuit parameters in the experimental work are given in Table I.

TABLE I
PARAMETERS OF THE EXPERIMENTAL SYNCHRONIZER

Parameter	Notation	Value
Shift register length	n	7
Number of chips per code period	$M = 2^n-1$	127
System oscillator frequency	f_{so}	19.5 MHz
Counter modulus	N_d	40
Nominal clocking frequency	$f_c = f_{so}/N_d$	487.5 KHz
Chip width	$\Delta = f_c^{-1}$	$\doteq$ 2.05 μs
Maximum quantization error	$\varepsilon_{qmax} = \Delta/N_d$	51 ns
Code period	$M\Delta$	261 μs
Number of code periods per frame	K	40
Frame length	$T_f = KM\Delta$	10.43 ms
Bandwidth of loop correlator filters	B_{if}	5 KHz (3 dB)
		14 KHz (60 dB)
Pre-mixer bandwidth	B_{RF}	6 MHz (3 dB)
Center frequency of pre-mixer signal	$f_r = \omega_r/2\pi$	30 MHz
Center frequency of post-mixer signal	$f_1 = \omega_1/2\pi$	10 MHz

A code having the same structure and essentially the same symbol duration as the code used to modulate the NCS is generated locally in the clock tracking loop. An estimate of the timing error between the time bases of the locally-generated code (clock) and the NCS is obtained by using intermediate frequency (IF) correlation processing circuits.* Two bandpass correlators were instrumented by 1) biphase

*The processing technique is similar to one investigated by Gill[9] in his study of conventional delay-lock loops.

switching the amplified input signal with two local codes displaced in time by Δ seconds, 2) mixing the phase-switched signals with a CW 40 MHz local oscillator (LO) signal, and 3) bandpass filtering and amplifying the components of the mixer outputs having spectra centered on 10 MHz. The filter bandwidths are approximately equal to $1.37/M\Delta$ Hz (see Table I). In the correlation processor instrumented previously, the time-displaced local codes were used to biphase modulate a CW LO signal and the input signal was mixed with the two phase modulated LO signals. The two processor configurations are functionally equivalent. An increased circuit gain and an improvement in dynamic range resulted on biphase switching the input signal rather than the LO signal due to the characteristics of the active biphase switches employed.

The bandpass amplifier outputs are processed by "linear" envelope detectors. Detectors having a dynamic range greater than 40 dB were instrumented using the technique illustrated in Fig. 2. Full-wave rectification is provided by switching the sign of the input signal in synchronism with the signal zero crossings. The hard limiter essentially senses the zero crossings and the sign inversions are performed by the phase switch (synchronous detector). Low pass filters are used to eliminate components of the phase switch outputs having spectra centered on integer multiples of 10 MHz. A difference output is generated by subtracting the envelope detector outputs (see Fig. 1). Since the input-signal is pulsed, the difference output is a train of video pulses plus noise rather than a continuous signal plus noise as in a conventional delay lock loop. These pulses are sampled at appropriate instants in time, t_s, to provide a difference output $e_c(t_s,\varepsilon_c)$ where ε_c represents the amount by which the receive clock is in error. The mean value of the sampled error voltage, $E\{e_c(t_s,\varepsilon_c)\}$, is proportional to ε_c (the clock loop timing error) when $|\varepsilon_c|$ is less than $\Delta/2$.*

*Square-law envelope detectors can also be employed in the correlation processor to provide a linear error characteristic for $|\varepsilon_c|<\Delta/2$. However, their use in TDMA modems is not recommended.

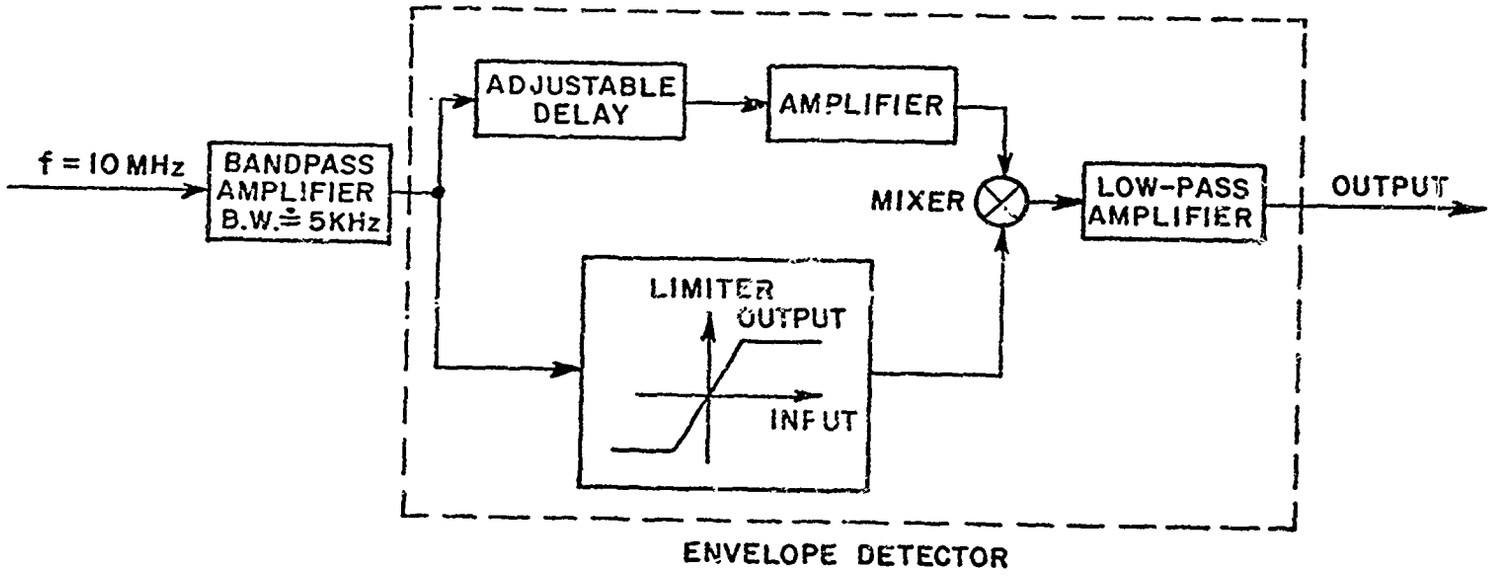

Fig. 2. A simplified block diagram of the envelope detectors in the time-shared correlation processor.

The mean value of the sampled error voltage is also proportional to signal amplitude when "linear" envelope detectors are employed in the correlation processor. A forward acting automatic gain control (FAAGC) circuit is used to prevent signal amplitude fluctuations from having a significant effect on clock loop gain. A block diagram of the FAAGC circuit and sampled error voltage versus timing error characteristics appropriate for describing its operation are shown in Fig. 3. As

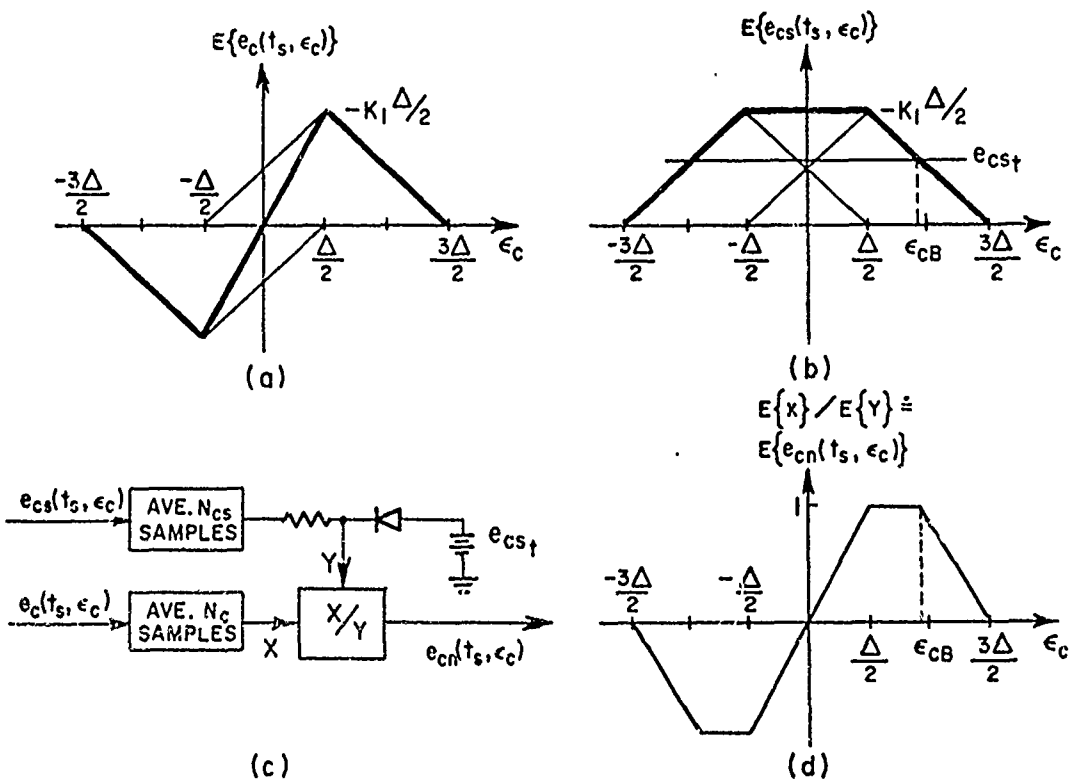

Fig. 3. Sampled voltage versus timing offset characteristics when FAAGC is employed.

indicated in this figure, an estimate of the signal amplitude is obtained by sampling the sum of the envelope detector outputs. The mean value of this sampled sum, $E\{e_{cs}(t_s,\varepsilon_c)\}$, is proportional to the signal amplitude and independent of ε_c when $|\varepsilon_c|<\Delta/2$. In one of several selectable modes of operation, error voltage $e_c(t_s,\varepsilon_c)$ is divided by sampled sum voltage $e_{cs}(t_s,\varepsilon_c)$ when the latter voltage exceeds a threshold level, e_{cs_t}; otherwise, $e_c(t_s,\varepsilon_c)$ is divided by e_{cs_t}. For this mode, the number of error voltage and sum voltage samples "averaged" -- parameters N_c and N_{cs}, respectively (see Fig. 1) -- equal one. In the experimental synchronizer, an analog module is used to perform the division. The divider is accurate to within ±2% over a 30 dB range of signal level variation. Means are provided for adjusting threshold voltage e_{cs_t} and the FAAGC circuit can be disabled if desired. In a second mode of operation, four consequtive error voltage samples are averaged (N_c=4) using an integrate/hold/reset module, and the average error voltage is divided by the most recent sample of the sum signal (N_{cs}=1) to obtain each processed error voltage sample. The option of averaging both the difference (error) and sum signals over four consecutive samples (N_c=N_{cs}=4) and dividing the average error signal by the average sum signal to obtain a processed error voltage sample is also provided. Each processed error voltage sample is applied to the control signal generator's input during an appropriate time interval by the analog multiplexer. One discrete correction is made to the time base of the receive clock for each clock pulse processed when N_c equals one, or for each set of four consequtive clock pulses processed when N_c equals four. A description of the control signal generator and the time base correction circuit will be given following a brief description of the ranging loop.

The ranging loop controls the time base of the transmit clock (see Fig. 1) and operates essentially the same as the clock loop. It is assumed that each user terminal is assigned one time slot in each frame of the TDMA signaling format for the exclusive purpose of maintaining proper transmitter timing, i.e., for range tracking purposes.

To simplify the discussion, it is also assumed that the duration of the ranging slots equals $M\Delta$ -- the width of the network clock pulses -- and that all other slots span an integer number of intervals $M\Delta$ seconds long. Now, the pulses processed by the ranging loop at a terminal -- the ranging pulses -- originate at that terminal. They are generated in synchronism with the continuous transmit clock and are also biphase modulated by a PN code. Each ranging pulse is received on the down-link one round-trip propagation time after its transmission. The difference between its arrival time and its assigned time of arrival in the time base of the NCS is designated as the ranging-loop error, ε_r. This error cannot be estimated directly at the receiver since exact knowledge of the NCS's time base is not available and the clock and ranging pulses occupy different time slots. However, the error in ranging pulse arrival time relative to the locked receive clock, $\varepsilon_{r/c}$, can be estimated. Of course, this indirect approach to error estimation results in a transfer of timing error in the clock loop to the ranging loop. A second correlation processor could be employed to provide an estimate of $\varepsilon_{r/c}$, or the correlation processor can be time shared between the clock and ranging loops if the clock and ranging pulses have the same duration; the processor is time shared in the experimental synchronizer. As in the clock loop, the error voltage samples, $e_{r/c}(t_s,\varepsilon_{r/c})$, can be averaged and normalized -- or, alternatively, normalized and averaged -- and the processed error voltage samples then applied to the analog multiplexer. Error sample processing was not employed in the ranging loop of the experimental synchronizer since the effects of averaging and controlling the gain automatically in the ranging loop can be predicted by extrapolating the results obtained from the clock loop experiments.

For the range tracking loop to be stable, the transmit time base must not be corrected following the transmission of a ranging pulse (or set of pulses if the error samples are averaged in the

ranging loop) until after that pulse (or set of pulses) has been processed at the receiver. Consequently, the minimum allowable spacing between ranging pulses is slightly greater than the maximum round-trip delay time. In the experimental synchronizer, the envelope of the ranging pulses processed has a period equal to twenty-eight times the period of the NCS's envelope: 28 KMΔ or 0.292 sec. That is, twenty-eight subframes of length KMΔ are contained in each frame of the signaling format.

During acquisition of lock in the clock loop, the NCS must be distinguishable from all other pulsed signals occupying the TDMA format if the acquisition circuitry is to operate properly. Two approaches to providing the separability required were described previously[1]. In the experimental synchronizer, the codes used to modulate the network clock and ranging pulses have the same structure. For this case, the carrier frequencies of the NCS and the ranging signals must differ if the clock pulses are to be uniquely identifiable. Consequently, if the correlation processor is to be time shared, the frequency of the LO signal generated within an operational synchronizer must be switched between two values. Since switching LO signals does not present any fundamental problems, and since the experiments could be conducted with the carrier frequencies of the NCS and ranging signal being essentially equal, the circuits required to switch LO signals were not incorporated in the experimental synchronizer. The need for LO switching can be eliminated while retaining the desirable features of time sharing the correlation processor by using different codes having equal periods to generate the network clock and ranging signals. Of course, a second code generator must be instrumented for this case and code multiplexing circuits provided, or the configuration of the feedback circuit in the code generator must be selected from two alternative configurations in a cyclic sequence. More complete descriptions of alternative circuit configurations and discussions of their advantages and limitations are contained in reference [1].

Block diagrams of the control signal generator and the time base correction circuits are shown in Fig. 4. These circuits are collectively called the time base control subsystem. They generate waveforms for clocking the clock and ranging loop code generators and correct the time bases of these waveforms (clocks) by amounts (nominally) proportional to the appropriate time-multiplexed filtered error voltage samples. All timing corrections are initiated by a low to high state transition of the convert command. The states of the sample identification (SI) and cross strap (CS) control signals determine the time base (or time bases when clock to ranging loop cross strapping is employed) to be corrected. A detailed discussion of the control signal generator will be deferred until after the technique used to correct the time bases has been described.

As can be seen from Fig. 4, the clock and ranging loop time base correction circuits and the basic notation used to represent the devices and waveforms in these circuits are identical. Subscripts c and r are used to designate devices and waveforms in the clock and ranging loops, respectively. For brevity, these subscripts will not be utilized in the remainder of this paragraph since the discussion applies to both time base correction circuits. Now, clocking waveform C is generated by performing appropriate logical operations on waveforms c_2, q_1, and q_2 (see Fig. 4). The period of C equals $4\cdot(2f_{so})^{-1}$ -- 102.4 nsec. in the experimental synchronizer -- irrespective of the states assumed by control signals q_a and q_b. Thus, a control cycle having a duration of $4\cdot(2f_{so})^{-1}$ seconds can be defined and circuit operation described by considering how the states of q_a and q_b affect the shape of waveform C in each control cycle. Waveforms appropriate to the discussion are given in Fig. 5. Between time base corrections, q_a and q_b are in the high and low states, respectively (q_aq_b equals 10), and waveform C contains two pulses per control cycle spaced uniformly by f_{so}^{-1} seconds. When q_aq_b equals 01, waveform c contains

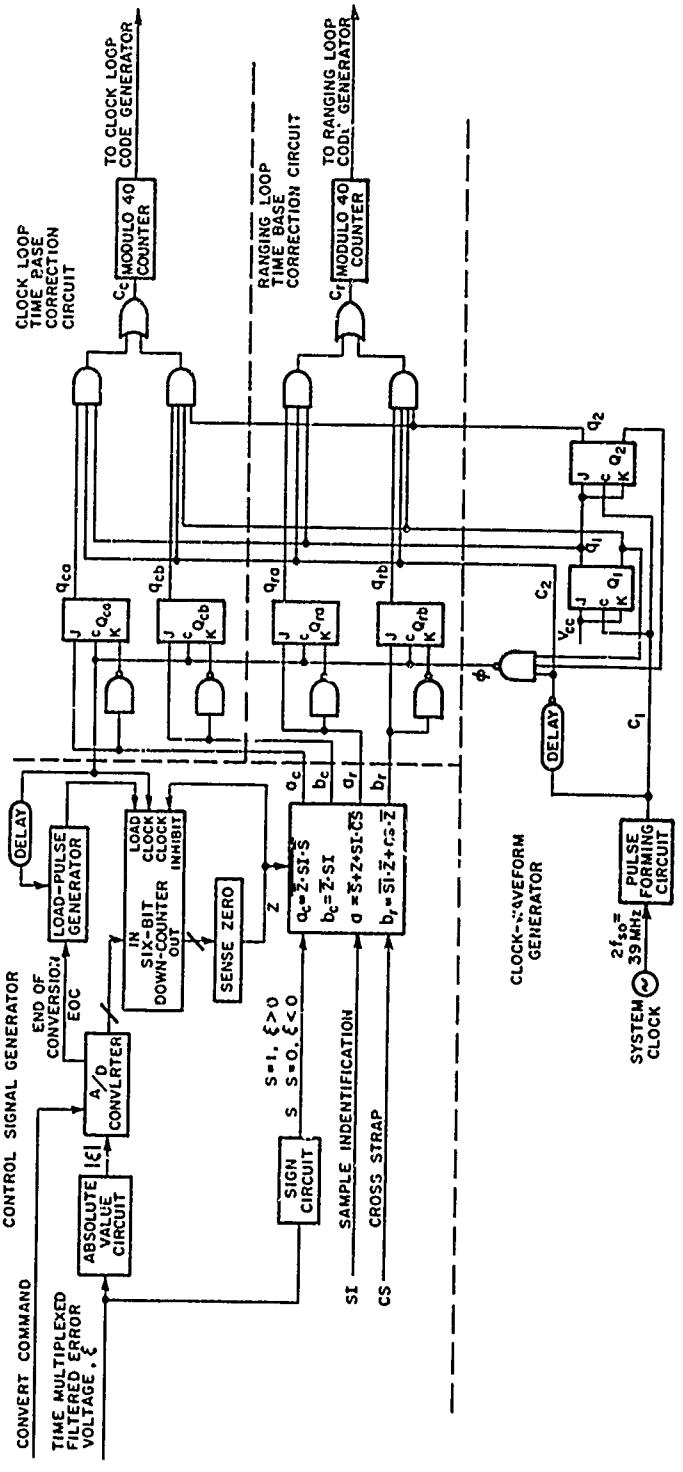

Fig. 4. Block diagram of the time base control subsystem.

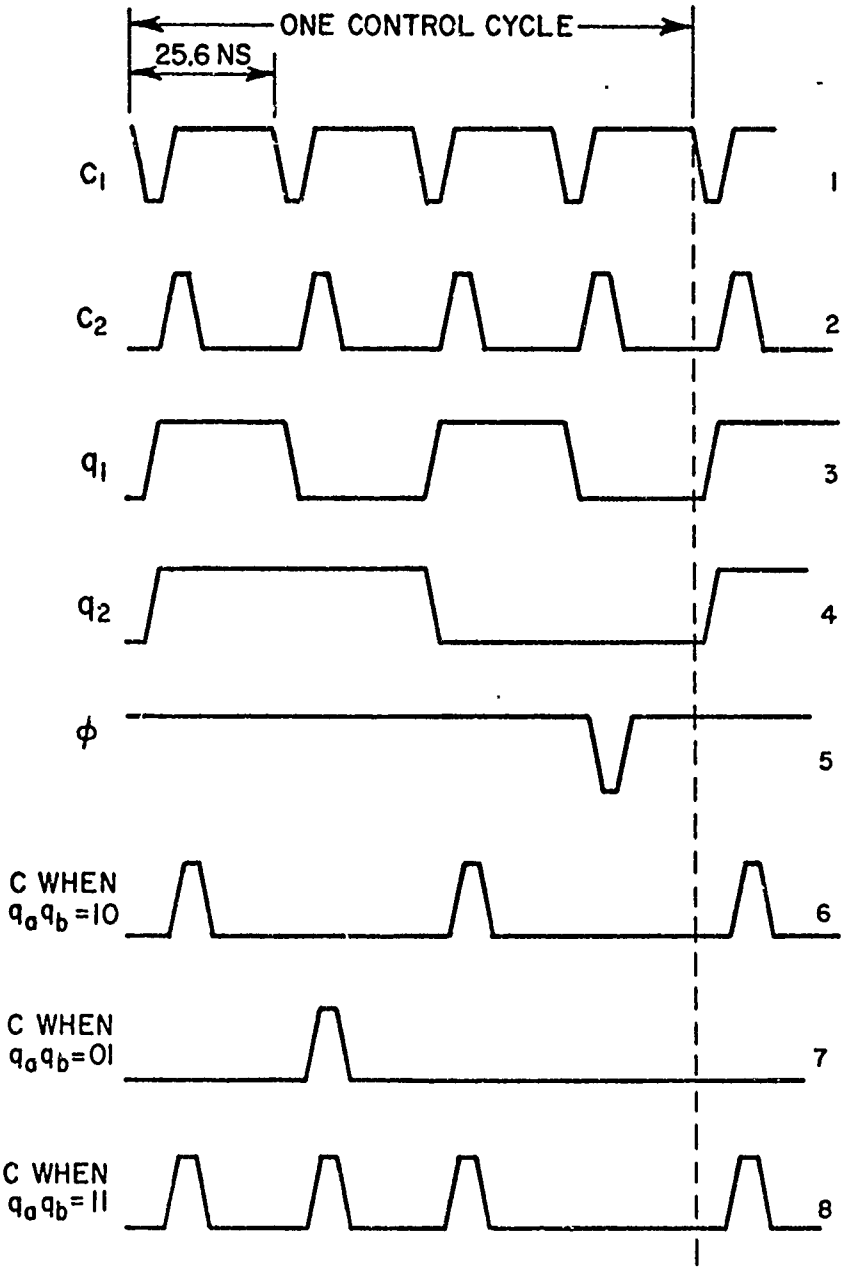

Fig. 5. Waveforms in the time base control subsystem.

only one pulse per control cycle. As a result, the time base of the code generator clocking signal is retarded by f_{so}^{-1} seconds -- 51.2 nsec in the experiment -- per control cycle as long as $q_a q_b$ equals 01. When $q_a q_b$ equals 11, waveform C contains three pulses per control cycle and the time base is advanced by f_{so}^{-1} seconds multiplied by the number of control cycles over which $q_a q_b$ equals 11. The time required to advance or retard the time base by $n \cdot f_{so}^{-1}$ sec where n is a positive integer equals $2n \cdot f_{so}^{-1}$.

Immediately prior to a control cycle, signals a and b are clocked into flip flops Q_a and Q_b, respectively, by the pulse in waveform ϕ which precedes the cycle. Thus, the states of $q_a q_b$ and a b are the same immediately after the flip flops are loaded. The two sets of a and b signals assume states determined by control signals SI, CS, S, and Z (see Fig. 4). Zero-sense signal Z is high when the six-bit down counter contains all zeros and both $a_c b_c$ and $a_r b_r$ assume the state 10, i.e., time base corrections are inhibited when Z is high. Each time $Z+\phi$ is low (where + designates the logical OR operation), at least one time base is incremented by f_{so}^{-1} seconds. Since the down counter is clocked by waveform ϕ, a timing correction having a magnitude $n\ f_{so}^{-1}$ will follow loading of the counter by the binary equivalent of n. Now, as previously stated, a time base correction is initiated by a low-state to high-state transition of the convert command at the analog to digital (A/D) converter's control input. When conversion is initiated, the absolute value of the filtered error voltage sample present at the input to the control signal generator is digitized by the A/D converter. After the conversion is completed, the end of conversion (EOC) signal changes state and the binary word at the converter's output is loaded as the initial count in the down-counter at an appropriate instant (see Fig. 4). This arrangement forces the magnitude of the time base correction(s) to be (nominally) proportional to the magnitude of the processed error voltage sample.

The sign of each processed error voltage sample is sensed to generate a sign signal, S; the state of S is high when the error voltage is positive and is low otherwise. Cross strap signal CS is high when open-loop ranging loop corrections are to be made which have the same magnitude as the clock loop corrections but a reversed sense; otherwise, CS is low. Lastly, sample identification signal SI is high when the error sample has been obtained by processing the NCS and is low when a ranging pulse has been processed to obtain the sample. The desired states of $a_c b_c$ and $a_r b_r$ for the various states of CS, SI, S, and Z are listed in Table II. Note that the receive clock is

TABLE II
CONTROL WAVEFORM STATES

Function	Z	SI	CS	S	$a_c b_c$	$a_r b_r$
Inhibit timing corrections	1	--	--	-	10	10
Advance receive clock only	0	1	0	1	11	10
Delay receive clock only	0	1	0	0	01	10
Advance receive clock and delay transmit clock	0	1	1	1	11	01
Delay receive clock and advance transmit clock	0	1	1	0	01	11
Advance transmit clock only	0	0	--	0	10	11
Delay transmit clock only	0	0	--	1	10	01

advanced when the error voltage sample is positive, i.e., when S equals 1; otherwise, the clock loop would be unstable. In contrast, a positive ranging loop error voltage sample causes the transmit time base to be retarded. This inversion of the correction sense is required because the time bases of the codes at the two local-code inputs to the correlation processor are corrected following processing of the NCS, whereas the time base of the signal input to the processor is corrected (after an interval of time greater than the round-trip propagation delay has elapsed) and the local code time bases held

fixed following ranging pulse processing. The logical operations performed on CS, SI, S, and Z to generate the required $a_c b_c$ and $a_r b_r$ states are described mathematically in Fig. 4.

Schottky-clamped TTL circuits were employed to instrument most of the time base control subsystem. The selection of this logic family was dictated by the rate at which the circuits used to generate and process waveforms c_1, c_2, q_1, and q_2 must operate. In addition, the circuit delays must be sufficiently small so that the a and b waveforms assume the desired states within approximately 80 nsec following loading of the down counter. The allowable delay time can be increased to permit the use of slower-speed logic circuits in the control signal generator by clocking the down-counter at a rate $f_{so}/(2k)$ where k is a positive integer greater than one, i.e., by reducing the clocking rate by a factor k. Correspondingly, the circuits used to generate q_a and q_b from a and b would have to be changed; otherwise, the number of pulses effectively added to or deleted from waveform C would be k times larger than the desired number.

As evident from the sampled error voltage versus timing error characteristic shown in Fig. 3, the timing error in the clock loop must be less than $3\Delta/2$ seconds before the clock loop will respond to reduce the error to a small value. The search and acquisition circuits instrumented previously were employed in the second-generation synchronizer.* These circuits are described in references [2] and [5]. To acquire lock, the receive (clock loop) time base is incremented in $\Delta/2$ second steps each $KM\Delta$ seconds. The envelope detected output of a third IF correlator is compared with a threshold voltage at appropriate instants to determine when the timing error is sufficiently

*The original timing control circuits (see Fig. 1) were also incorporated into the new unit.

small for the loop to respond properly. In subsequent designs, it is recommended that the sampled sum output of the correlation processor be used to generate a lock/loss-of-lock signal as indicated in Fig. 1. Using this approach, the time base can be indexed in Δ second steps and a third IF correlator is not needed. Experimental observations regarding clock loop acquisition are discussed in Section IV; more complete discussions of alternative acquisition algorithms are contained in reference [1].

Acquisition of proper transmitter timing must be accomplished after the clock loop is locked. In most applications, ranging loop acquisition will proceed in two steps. First, a coarse estimate of the round trip delay time is obtained using a separate subsystem. This estimate is used to set the transmit clock. The residual error can then be reduced to a small value by incrementing the time base in Δ second steps. Circuits constructed to determine the feasibility of using frequency-swept signals to obtain a coarse estimate of the round trip delay time are described in Section IV.

III. CLOSED-LOOP TIMING ERROR DATA

A. Introduction

Bench tests were conducted to determine the effects of wide-band Gaussian noise, carrier frequency offset, and a constant rate of change in the delay experienced by the received network clock signal on the tracking accuracy of the experimental synchronizer. The basic objectives of the tests were 1) to verify proper operation of the control loops when the FAAGC and clock to ranging loop cross strapping subsystems are disabled, 2) to determine how the performance of the FAAGC circuit is affected by error in the signal amplitude estimate caused by noise, and 3) to establish the applicability of the

two-loop model employed previously[2],[5] in analyzing the effect of clock to ranging loop cross strapping on synchronizer performance. Results obtained from the bench tests are presented and compared with available theoretical results in this section. The tests were conducted in essentially the same manner as the previous tests and the same peripheral test instruments were employed. Since these aspects of the work have already been documented[2],[5], they will be considered only briefly in the present report.

B. Clock Loop Performance

It has been shown analytically[2],[5] that the standard deviation of the clock loop timing error due to noise divided by the chip length is given approximately by

$$(1) \qquad \frac{\sigma_{\varepsilon c}}{\Delta} \doteq 0.55 \left(\frac{A_c}{2-A_c}\right)^{1/2} \left(N_c \cdot \frac{E_c}{N_{co}}\right)^{-1/2}$$

where

$A_c \sim$ the gain of the clock tracking loop, $0<A_c<2$,
$N_c \sim$ the number of error voltage samples averaged to obtain a filtered error voltage sample,
$E_c \sim$ the energy in each pulse of the network clock signal at the synchronizer's input, and
$N_{co} \sim$ the single-sided power spectral density of the (Gaussian) input noise voltage during intervals occupied by the network clock pulses.

This result was derived subject to the assumptions that 1) the magnitude of the timing error seldom exceeds $\Delta/2$ seconds, 2) the bandpass filters in the correlation processor have ideal rectangular passbands of width $1.37/M\Delta$ Hertz, 3) the quantization error introduced by the

time base control circuit is negligibly small, and 4) FAAGC is not incorporated in the loop, i.e., the loop gain was assumed to be constant.

Plots of Eq. (1) for N_c equal to one and four and A_c equal to one are shown in Fig. 6 along with experimental data points obtained while operating the synchronizer with the FAAGC circuit disabled. In the experiment, the loop gain was first set equal to two by adjusting the signal level to the smallest value which resulted in an oscillatory loop response. The signal amplitude was then reduced by one-half to establish a loop gain of one. The pulse energy to noise density ratio, E_c/N_{co}, was varied by changing the level of the noise summed with the signal at the synchronizer's input. A time interval meter was used to measure the timing error at appropriate instants. One thousand timing-error samples were processed by a digital instrumentation computer operating on-line to obtain each data point. The computer was programed to provide a histogram of the error samples and to calculate their mean value in addition to calculating the standard deviation.

The effect of quantizing the time base corrections on the timing jitter is evident from the experimental results shown in Fig. 6: a lower bound is imposed on $\sigma_{\varepsilon c}/\Delta$ which is approximately equal to one-half the maximum quantization error divided by Δ, i.e., $(\sigma_{\varepsilon c}/\Delta)_{min} \doteq \frac{1}{2}\left(\frac{\Delta}{40}\right)/\Delta = 0.0125$. This bound is approximately 0.7 times the corresponding bound observed in previous experiments. The reduction in timing jitter due to quantization error is attributed to improvements in the time base correction circuit design. A compensated theoretical result can be obtained by adding the ideal theoretical result and the measured rms quantization error divided by Δ in an rms (square root of the sum of squares) sense. The compensated analytical result and the experimental data points are in close agreement for

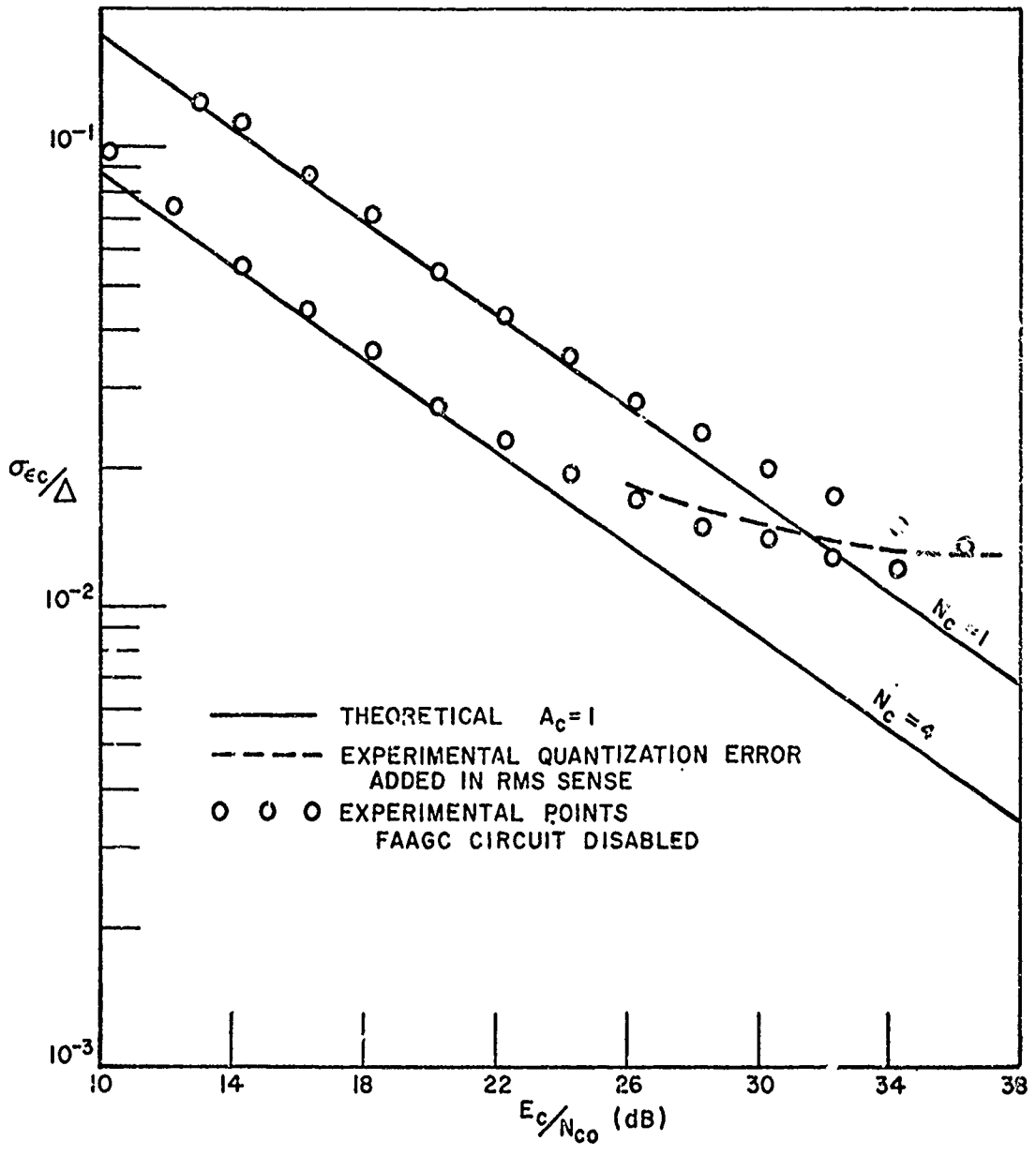

Fig. 6. Normalized clock loop timing jitter versus pulse energy to noise density ratio for two values of N_c and unity loop gain when the FAAGC circuit is disabled and E_c/N_{co} is varied by changing the noise level.

values of E_c/N_{co} greater than 12 dB. For E_c/N_{co} less than 12 dB, a better agreement between analytical and experimental results can be obtained by calculating $\sigma_{\varepsilon c}/\Delta$ using an expression given in references [2] and [5] which includes a first-order correction to Eq. (1).

Several experiments were conducted to determine the effectiveness of the FAAGC technique. In these tests, the loop gain was set equal to one with the noise removed from the synchronizer's input. Of course, when noise was applied to the input, the loop gain became a random process since noise caused the sum output of the correlation processor to fluctuate. It can be shown that the loop gain has an average value larger than its value when noise is removed from the input by an amount which depends on the pulse energy to noise density ratio. However, the increase in average value is small when E_c/N_{co} exceeds 10 dB. In subsequent discussions, the loop gain will be described as equaling one to simplify the presentation.

In one series of tests, the threshold level in the FAAGC circuit, e_{cs_t}, was set at a value much smaller than the nominal sum output of the correlation processor when the lowest-level clock signal was applied at the synchronizer's input. The results obtained from these tests are shown in Figs. 7 and 8. To provide a basis for comparison, theoretical results obtained using Eq. (1) are also shown in the figures. The data shown in Fig. 7 were obtained with the number of sum voltage samples averaged in the FAAGC circuit, N_{cs}, set equal to one; the pulse energy to noise density ratio was changed by varying the signal amplitude while holding the input noise power constant. For completeness, data was also obtained which show the effect of changing E_c/N_{co} by varying the noise power while holding the signal amplitude constant. These latter results are shown in Fig. 8. Comparing Fig. 7 with Fig. 6 shows that enabling the FAAGC circuit has a negligible effect on $\sigma_{\varepsilon c}/\Delta$ throughout the range over

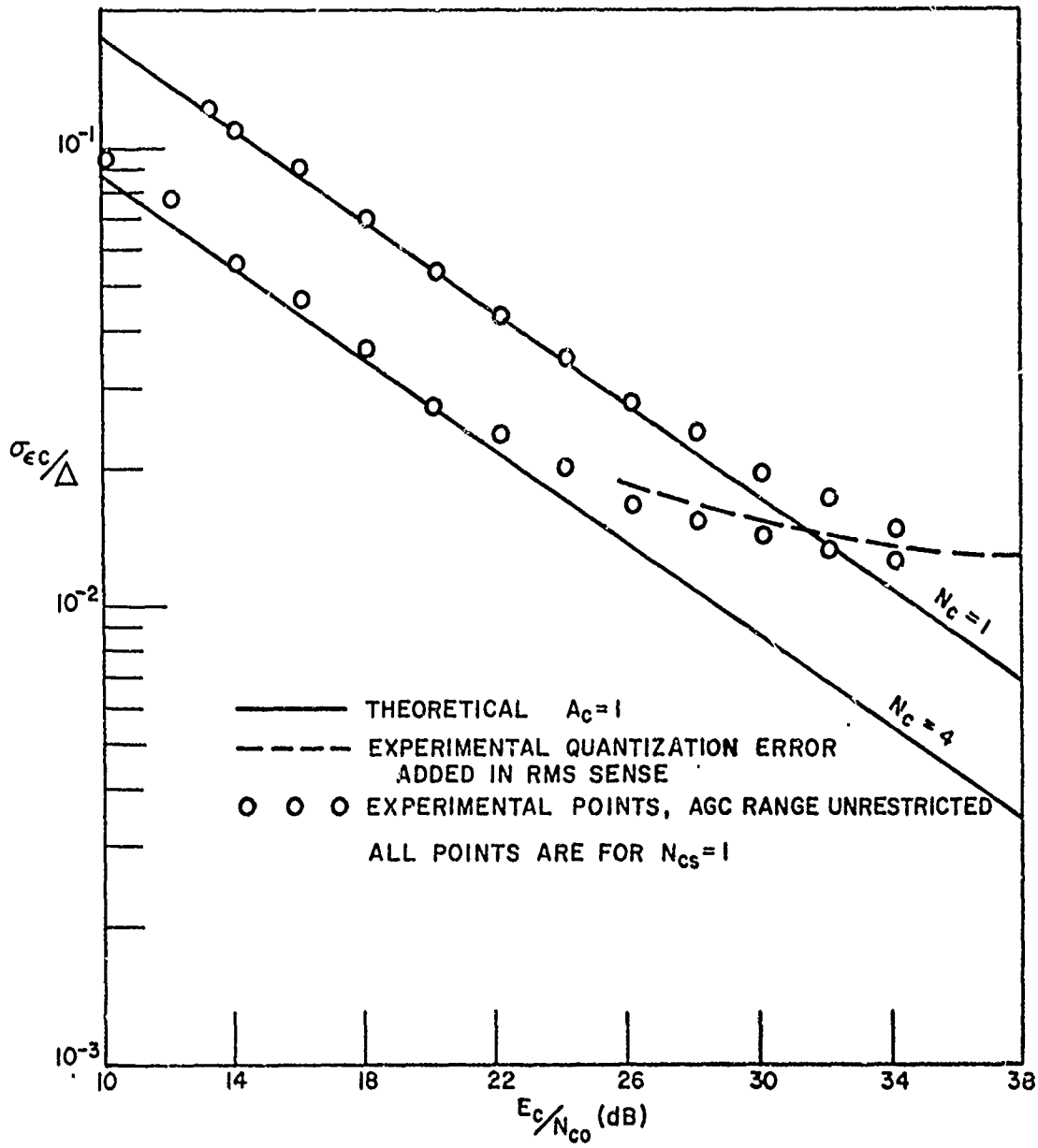

Fig. 7. Normalized clock loop timing jitter versus pulse energy to noise density ratio for a loop gain of one when the FAAGC circuit is enabled and E_c/N_{co} is varied by changing the signal level; $N_{cs}=1$.

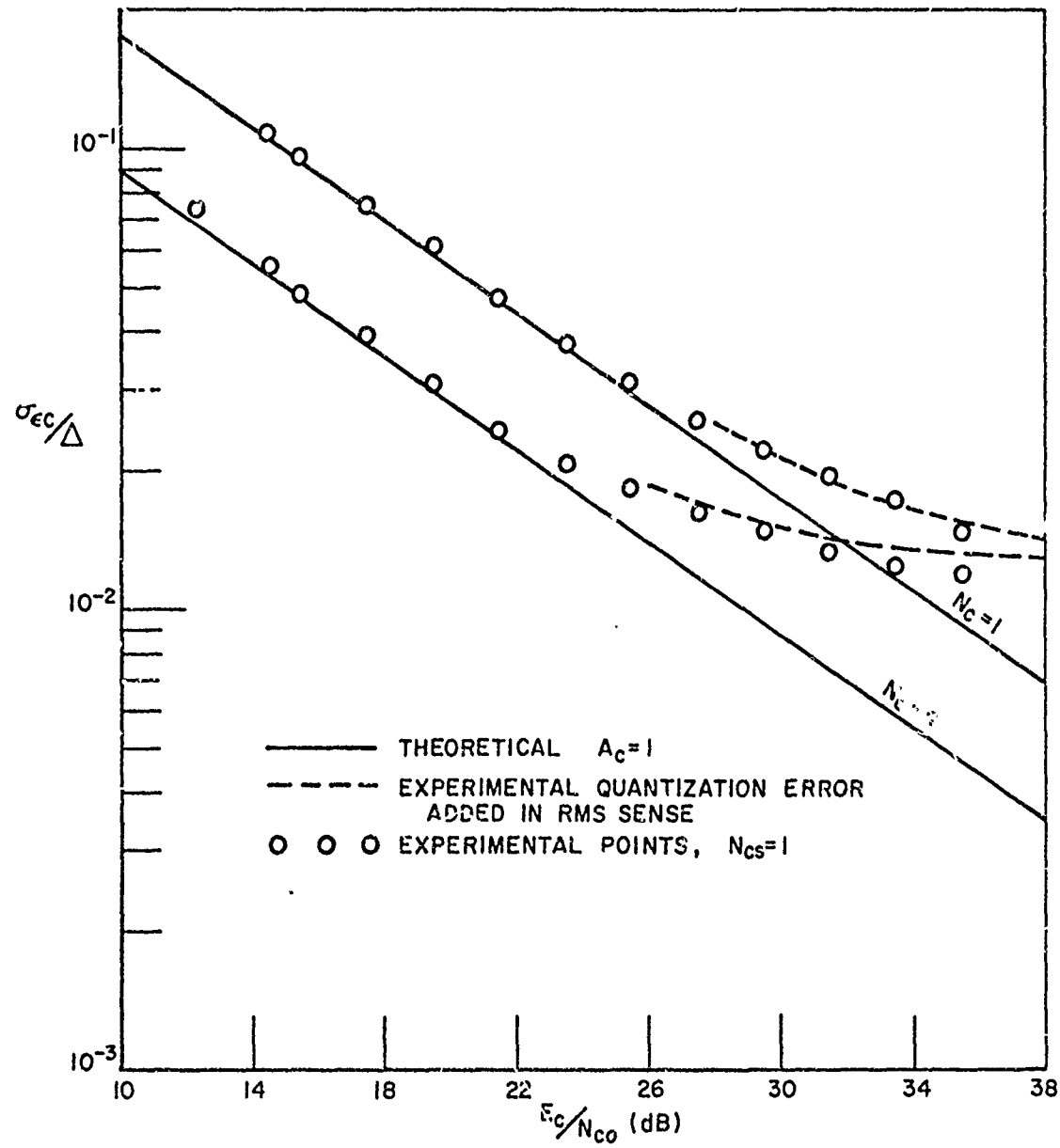

Fig. 8. Normalized clock loop timing jitter versus pulse energy to noise density ratio for a loop gain of one when the FAAGC circuit is enabled and E_c/N_{co} is varied by changing the noise level; $N_{cs}=1$.

which E_c/N_{co} was varied. The results in Fig. 7 show that the effective loop gain is apparently held constant at one as the signal amplitude is varied over a 24 dB range. For the results to be conclusive, it must also be shown that enabling the FAAGC circuit does not alter the response of the loop to deterministic changes in the network clock signal's delay. This latter aspect of loop performance will be discussed in a subsequent paragraph.

The standard deviation of the loop gain variations can be reduced by averaging the sum voltage samples. Results obtained with N_{cs} set equal to four are shown in Fig. 9; the value of E_c/N_{co} was changed by varying the signal level. As anticipated from the results presented in the preceding paragraph, averaging the sum samples does not reduce $\sigma_{\varepsilon c}/A$. However, averaging does reduce the probability that a large loop gain error or consecutive loop gain errors will cause a loss of lock. This factor should be considered when E_c/N_{co} is less than approximately 12 dB.

Results showing the effect of setting threshold voltage e_{cs_t} at values which are typically larger than the sum output of the correlation processor when a low-level clock signal is applied at the synchronizer's input are given in Figs. 10 and 11. To facilitate discussion, a breakpoint signal amplitude is defined as the amplitude of the network clock signal which results in the mean value of the correlation processor's sampled sum output equaling the threshold voltage. The procedure used to set the threshold level and thus the breakpoint signal amplitude can best be described by example. In Fig. 10, the FAAGC breakpoint is indicated as occurring at E_c/N_{co} equal to 14 dB. Prior to setting the threshold level, a pulse energy to noise density ratio of 14 dB was established by appropriately adjusting the signal and noise levels. The noise was then removed from the synchronizer's input and the threshold voltage set equal

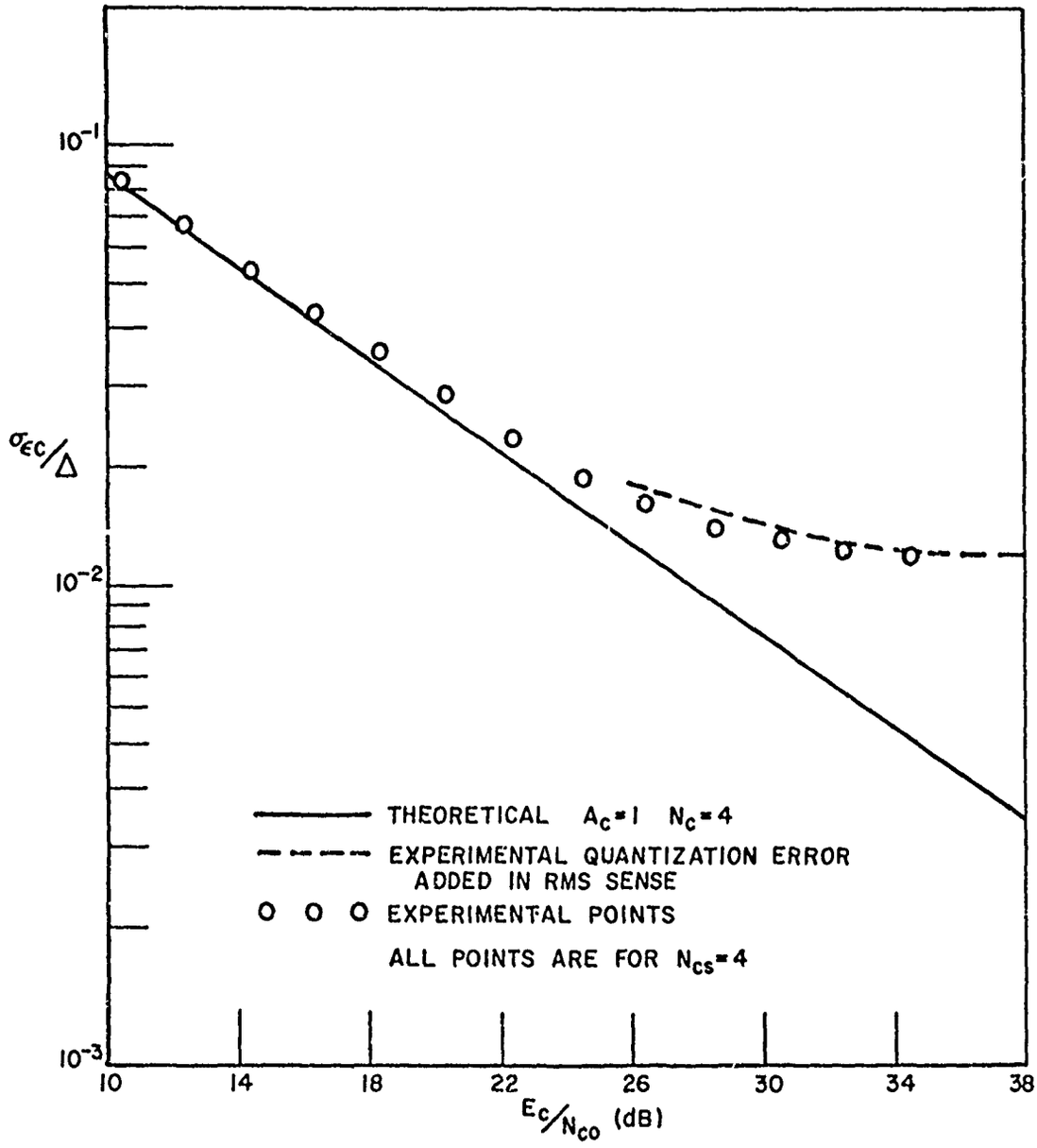

Fig. 9. Normalized clock loop timing jitter versus pulse energy to noise density ratio for a loop gain of one when the FAAGC circuit is enabled and E_c/N_{co} is varied by changing the signal level; $N_{cs}=N_c=4$.

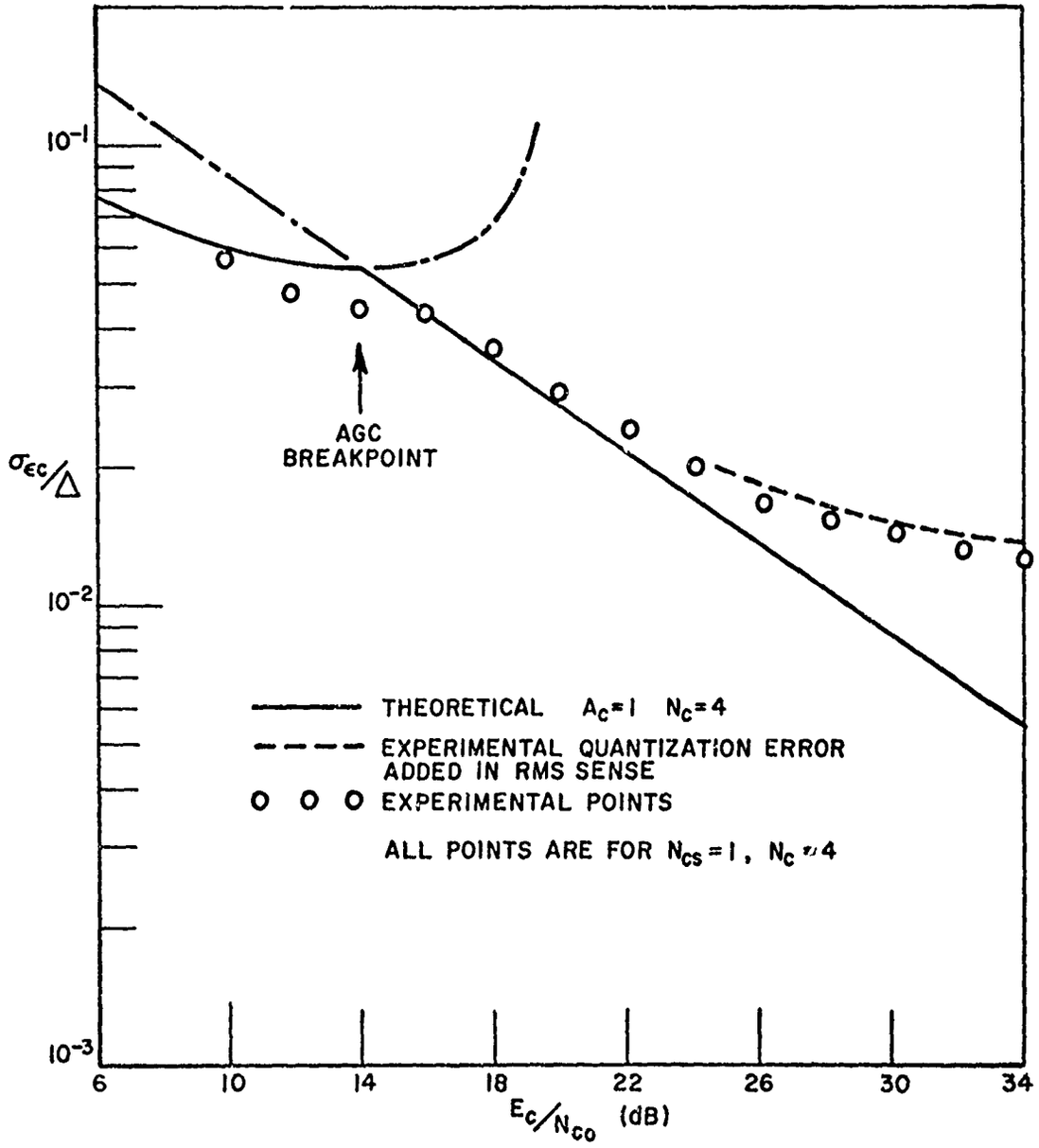

Fig. 10. Normalized clock loop timing jitter versus pulse energy to noise density ratio for N_{cs} equal to one and N_c equal to four when the breakpoint of the FAAGC circuit occurs at E_c/N_{co} equal to 14 dB and E_c/N_{co} is varied by changing the signal level.

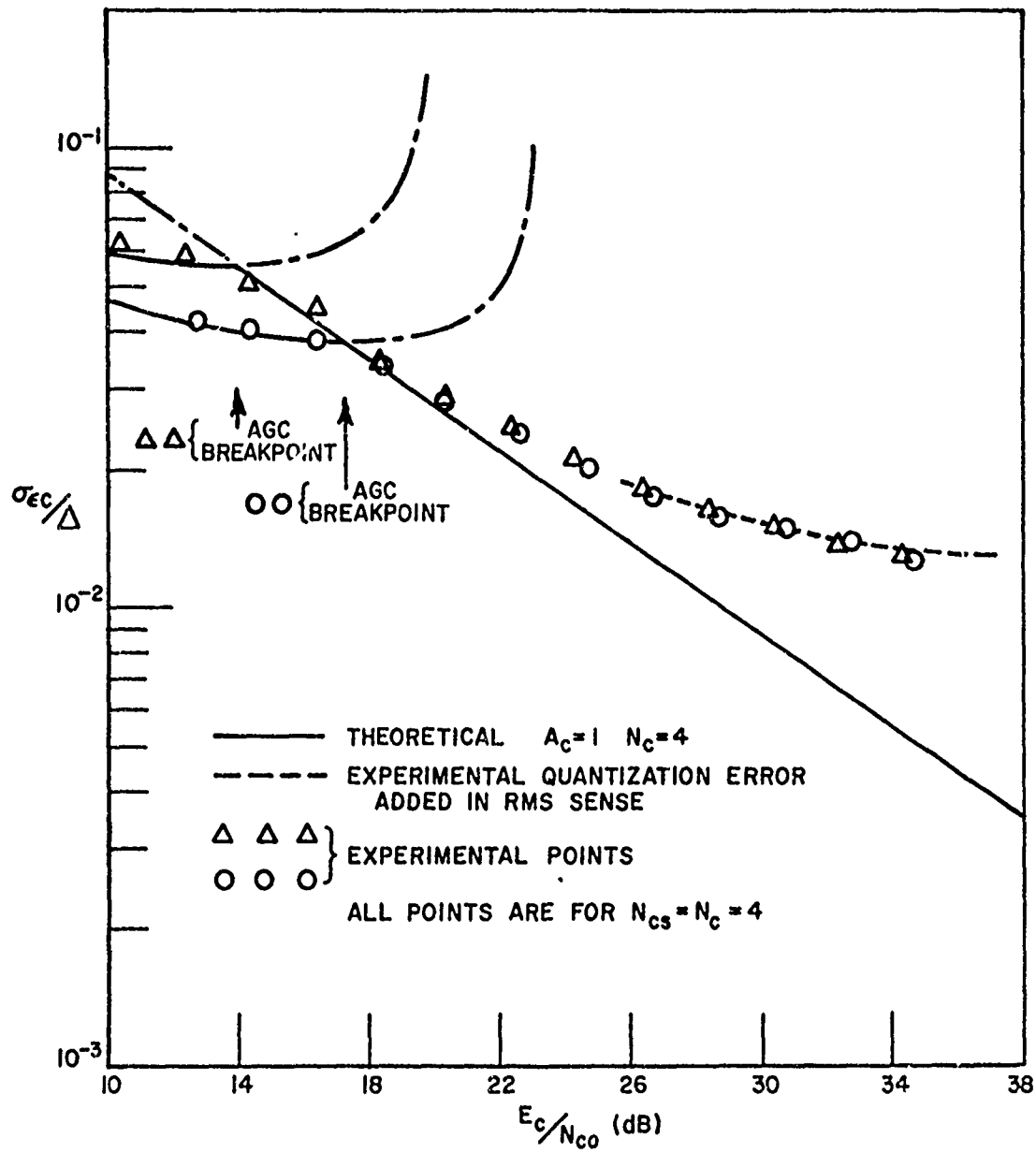

Fig. 11. Normalized clock loop timing jitter versus pulse energy to noise density ratio for two values of the FAAGC circuit breakpoint when E_c/N_{co} is varied by changing the signal level; $N_{cs}=N_c=4$.

to the (sampled) sum output of the correlation processor. On re-applying the noise at the synchronizer's input, an E_c/N_{co} breakpoint of 14 dB was established. A similar procedure was used to set the breakpoint at 17.3 dB prior to obtaining one of the sets of data shown in Fig. 11. The pulse energy to noise density ratio was varied in the experiments by changing the signal amplitude.

The results given in Fig. 10 were obtained with N_{cs} set equal to one. They indicate that the effective loop gain was less than one when E_c/N_{co} equaled 14 dB: the breakpoint value. This occurred because the gain control was enabled only when voltage e_{cs} exceeded e_{cs_t} (see Fig. 3) -- a condition which occurred fifty-percent of the time when E_c/N_{co} equaled 14 dB. When e_{cs} did exceed e_{cs_t}, the instantaneous gain was less than unity; values of e_{cs} smaller than e_{cs_t} resulted in a loop gain of one. Thus, the effective loop gain was less than one when E_c/N_{co} equaled 14 dB (or, more generally, the breakpoint value). When the signal amplitude exceeded the breakpoint signal amplitude by approximately two decibels or more, sum voltage e_{cs} exceeded the threshold most of the time and the effective loop gain equaled one. The threshold level was seldom exceeded when the signal amplitude was smaller than the breakpoint amplitude by three decibels or more. Over this range of operation, the loop gain was directly proportional to the signal amplitude.

The effect of averaging four consecutive sum voltage samples to obtain an estimate of the signal amplitude, i.e., of setting N_{cs} equal to four, is shown in Fig. 11. Comparing the behavior of $\sigma_{\varepsilon c}/\Delta$ in the vicinity of the breakpoints with the data shown in Fig. 10 shows that the change in signal level required to make the transition from no gain control to a controlled gain of unity was much smaller when N_{cs} equaled four. That is, the breakpoint was more clearly defined. This occurred because averaging reduced the standard deviation of the signal amplitude estimate.

In an operational system, the primary purpose for utilizing automatic gain control is to maintain the loop gain at or near a design value when the signal amplitude equals or exceeds the level required for acceptable performance of the data detection subsystem. During signal fades, maintaining the loop gain at a constant value may be less desirable than allowing the gain to drop. That is, rather than keeping the deterministic tracking error small by holding the loop gain constant at the expense of a large increase in $\sigma_{\varepsilon C}/\Delta$, an increase in deterministic tracking error and a less severe increase in $\sigma_{\varepsilon C}/\Delta$ may be preferred when the signal amplitude fades. As evident from Figs. 10 and 11, such a compromise can be realized by setting the threshold voltage at an appropriate value. Additionally, setting the threshold so that the breakpoint signal amplitude is slightly lower than the minimum amplitude required for reliable data detection restricts the range over which the instantaneous loop gain can fluctuate.

It can be concluded from the data given to this point that the timing jitter does not change significantly when the FAAGC circuit is enabled. Experiments were also conducted to determine how enabling the FAAGC circuit affects the response of the loop to a constant rate of change in the network clock signal's delay. The results to be described were obtained with both N_C and N_{CS} set equal to one and the pulse energy to noise density ratio set at a moderate value of 20.3 dB. These parameters resulted in $\sigma_{\varepsilon C}/\Delta$ being approximately equal to 0.052; the magnitude of the normalized timing error due to noise was usually less than $3\,\sigma_{\varepsilon C}/\Delta$ or 0.156. Thus, it was possible to increase the magnitude of the peak deterministic timing error, $|\bar{\varepsilon}_C|_{max}$, to approximately 0.344Δ before causing the loop to operate outside the linear tracking range a significant percentage of the time. A constant rate of change in the signal delay was simulated by offsetting the rate at which the code generator used to modulate

the input signal was clocked. The effective loop gain was determined from the computed mean of one thousand timing error samples at several delay rates. The gain was found to remain essentially constant at 1.02 as $|\bar{\varepsilon}_c|_{max}$ was varied from zero to 0.35Δ. Since experimental errors could well have caused a plus or minus two percent error in establishing the loop gain with noise removed from the synchronizer's input, a non-zero number cannot be assigned to the gain change caused by the FAAGC circuit at an acceptable level of confidence. However, it can be concluded that -- at worst -- the change in effective loop gain is small and can be neglected when E_c/N_{co} equals or exceeds 20.3 dB. Additional results obtained indicate that this conclusion also applies when E_c/N_{co} is less than 20 dB provided the magnitude of the total timing error is less than $\Delta/2$ most of the time.

In the experiment described in the preceding paragraph, the behavior of $\sigma_{\varepsilon c}/\Delta$ as a function of the peak deterministic timing error was also determined. As $|\bar{\varepsilon}_c|_{max}$ was increased from zero to 0.35Δ, $\sigma_{\varepsilon c}/\Delta$ increased by 0.011 from 0.052 to 0.063 or approximately twenty percent. The percentage increase was small until $|\bar{\varepsilon}_c|_{max}$ became large in comparison with $\sigma_{\varepsilon c}/\Delta$. At each delay rate, the increase in jitter was less than one-twentieth the corresponding value of $|\bar{\varepsilon}_c|_{max}$. The increase can normally be neglected in designing practical synchronizers.

As noted previously, the peripheral instrumentation computer employed in the tests also provided histograms of the timing error samples. Several of these histograms were employed to obtain estimates of the timing error's cumulative distribution function. The results of this work show that the timing error can be modeled as a Gaussian process except when the timing error due to noise is significantly smaller than the quantization error resulting from correcting the time base by discrete amounts.

In the experiments described to this point, the carrier frequency of the network clock signal was set equal to its design value. Data reported previously in references [2] and [5] show that a frequency offset causes the timing jitter to increase by an amount which depends on the bandshapes of the bandpass filters employed in the correlation processor. More precisely, the responses of the filters at the sampling instant to a pulsed signal as a function of carrier frequency determines the degradation in timing jitter caused by a frequency offset of Δf Hertz. The average pulse and cw responses of the filters employed in the experimental synchronizer* are shown in Fig. 12. These responses differ because the filter bandwidth is not large compared to the width of the pulsed signal's spectrum. Note that when the signal is pulsed, the effective shape factor of the filters is reduced because part of the signal's spectrum overlaps the passband when the frequency offset is significantly larger than the half bandwidth. Now, as the frequency offset is increased from zero, the reduction in the relative amplitude responses of the filters causes the effective pulse energy to noise density ratio to decrease. Moreover, if the loop gain is not controlled automatically and the amplitude of the input signal is held fixed, the slope of the error voltage characteristic, and thus the loop gain, decreases as $|\Delta f|$ is increased from zero. In contrast, the loop gain remains essentially constant when the FAAGC circuit is enabled since the deterministic components of both the sum and difference outputs of the correlation processor are reduced by the same factor when Δf is non-zero. Experimental results showing the factor by which $\sigma_{\varepsilon c}/\Delta$ increased as a function of Δf when the FAAGC circuit was both enabled and disabled are shown in Fig. 13. Corresponding quasi-theoretical results are also shown in the figure. These latter results were obtained by employing the measured relative amplitude response of the filters to a pulsed

*The bandshapes of the two filters were similar but not identical.

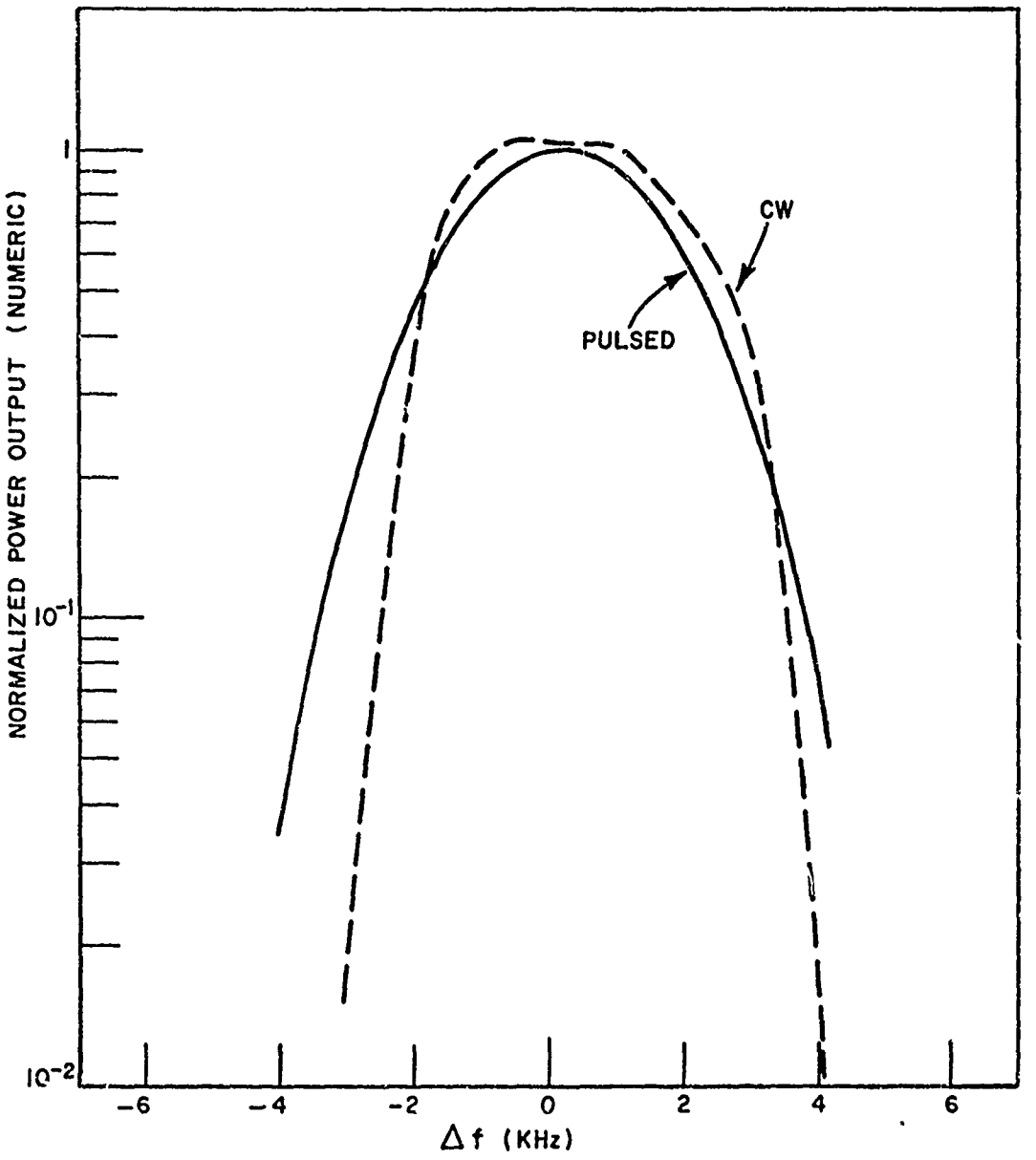

Fig. 12. Average amplitude responses of the bandpass filters in the correlation processor as a function of frequency offset for CW and pulsed envelope waveforms applied at the processor's input.

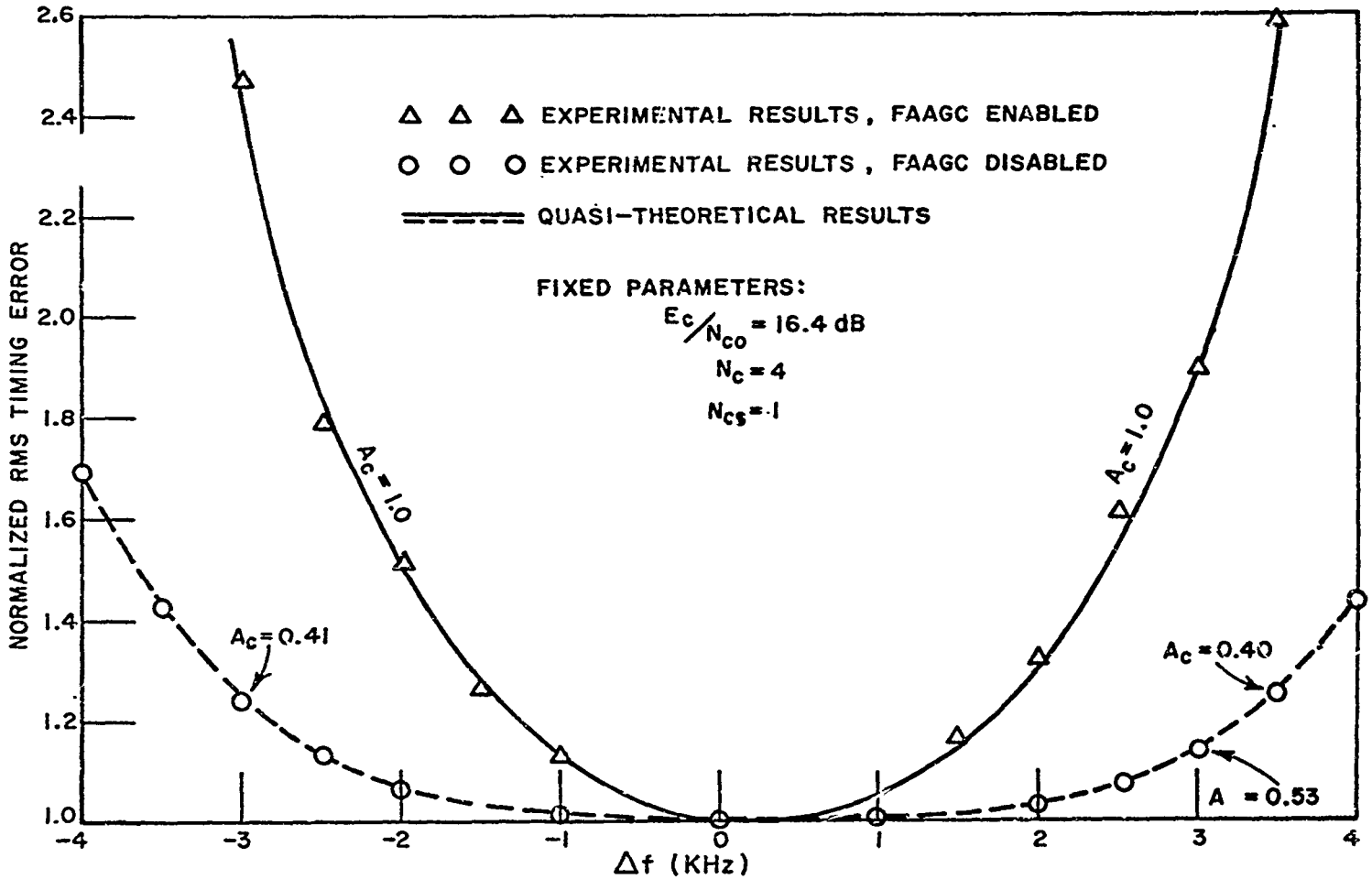

Fig. 13. Clock loop timing jitter normalized to its value when the frequency offset equals zero versus carrier frequency offset when the FAAGC circuit is either enabled or disabled; the loop gain was set equal to one with the frequency offset set equal to zero.

signal (see Fig. 12) in conjunction with Eq. (1). In performing the calculations, it was assumed that the loop gain was held fixed at one when the FAAGC circuit was enabled and that the loop gain was proportional to the relative amplitude response of the filters when the gain control circuit was disabled. The experimental and quasi-theoretical results are in sufficiently close agreement to justify the following conclusions: 1) the increase in timing jitter caused by a frequency offset can be predicted using Eq. (1) if the frequency response of the filters to a pulsed signal is known, 2) the FAAGC circuit does maintain the loop gain at essentially a constant value as the frequency offset is varied, and 3) precise frequency control is not required since the frequency must be offset by (nominally) 1 KHz -- approximately twenty percent of the filter bandwidth -- before the timing jitter increases ten percent.

In some applications, an automatic frequency control (AFC) circuit may be required to prevent doppler shift from causing an unacceptably large degradation in system performance. An AFC capability can easily be provided if the initial frequency offset is sufficiently small to permit locking of the clock loop: typically, on the order of one-half the correlation processor's bandwidth or smaller. For this case, an estimate of the frequency offset can be obtained after the clock loop is locked by 1) summing the outputs of the bandpass filters in the correlation processor, 2) (soft) limiting the sum signal, 3) applying the limited sum signal to a discriminator, 4) sampling the discriminator's response to the network clock pulse train at appropriate instants, and 5) filtering the samples to obtain an error voltage having a mean value proportional to the frequency offset. In turn, the (filtered) error voltage could be applied to a voltage controlled crystal oscillator and the oscillator's output signal used to synthesize the local oscillator signal applied to the correlation processor. An AFC loop of this type should have a bandwidth several

times smaller than the reciprocal of the clock-pulse spacing. Now, when the initial frequency offset is sufficiently large to prevent reliable locking of the clock loop, a two-dimensional frequency/time search is required to acquire lock if the sampled-data AFC technique is employed. This would not necessarily cause the acquisition time to become prohibitively large; however, additional circuitry would be required. To avoid the need for a two dimensional search, a continuous low-level beacon signal could be received from the satellite and appropriately processed to estimate the doppler shift.

C. Joint Performance of the Clock and Ranging Loops

The appropriate measure of overall synchronizer performance is the error between the time bases of the received ranging pulses and the network clock signal, ε_r. This error depends on both the clock and ranging loop responses since the two loops are coupled. Analytical results showing how the standard deviation of ε_r, $\sigma_{\varepsilon r}$, and the deterministic component of ε_r are related to signal and system parameters were reported previously in references [2] and [5]. Also, the correctness of the analytical result applicable when clock to ranging loop cross strapping is not employed was established by experimental testing. The basic objective of the two loop tests performed on the second-generation experimental synchronizer was to establish the feasibility of cross strapping and to determine the correctness of the model used to analyze the effect of cross strapping on timing error ε_r.

When cross strapping is not employed and the number of error samples "averaged" in the ranging loop equals one,* the standard deviation of ε_r divided by Δ is given approximately by

*More general results are contained in references [2] and [5].

$$(2) \qquad \frac{\sigma_{\varepsilon r}}{\Delta} \doteq 0.55 \left\{ \left(\frac{A_r}{2-A_r} \right) \left[\left(\frac{A_c}{2-A_c} \right) \frac{1}{N_c \cdot E_c / N_{co}} + \frac{1}{E_r / N_{ro}} \right] \right\}^{1/2}$$

where

$A_r \sim$ the gain of the ranging loop, $0<A_r<2$,
$E_r \sim$ the energy in each pulse of the ranging signal at the synchronizer's input, and
$N_{ro} \sim$ the single-sided power spectral density of the Gaussian input noise voltage during intervals occupied by the ranging pulses.

The remaining parameters in Eq. (2) were defined previously. On applying the clock loop corrections as open-loop corrections to the transmit time base in an inverted sense, timing error ε_r becomes nonstationary in the strict sense. However, the standard deviation of timing error samples having the same spacing as the ranging loop corrections is defined, i.e., ε_r is periodically stationary. The value of $\sigma_{\varepsilon r}/\Delta$ depends on the instants at which the samples are taken relative to the ranging loop correction instants. From results given in references [2] and [5], it can be shown that

$$(3) \qquad \frac{\sigma_{\varepsilon r}}{\Delta} \leq 0.55 \left\{ \left(\frac{A_r}{2-A_r} \right) \left[\left(\frac{A_c}{2-A_c} \right) \frac{1}{N_c \cdot E_c / N_{co}} + \frac{1}{E_r / N_{ro}} \right] + \frac{2[1+A_r|1-A_r|(1-A_c)]}{2-A_r} \left(\frac{A_c}{2-A_c} \right) \frac{1}{N_c \cdot E_c / N_{co}} \right\}^{1/2}$$

when $0<A_c \leq 1$. The bound given by the right hand side of this expression is closely approached by $\sigma_{\varepsilon r}/\Delta$ when A_r is approximately equal to one: the case of greatest practical interest. Comparing this latter result with Eq. (2) shows that cross strapping increases the timing jitter.

However, cross strapping substantially reduces the deterministic timing error caused by relative satellite/terminal motion; open-loop compensation of the transmitter timing is exact when the round-trip delay experiences a constant rate of change. Between closed-loop corrections in the ranging loop (when cross strapping is employed), the transmitter timing error accumulates at a nominal rate of $2\Delta f/f_c$ seconds per second where Δf represents the difference between the rate at which the network clock signal is modulated at the satellite and the rate at which the local code generater is clocked at the terminal, and f_c represents the nominal modulation rate. If a means for trimming the frequency of the local clock is available, the clock can be "set" by trimming the frequency until the average value of the closed-loop ranging corrections equals zero. The transmission of all pulses can be inhibited between messages if closed-loop corrections in the ranging loop are also inhibited and the frequency offset is sufficiently small. Of course, if messages are transmitted on an infrequent basis, an occasional up-date of the transmitter timing might be required to prevent the timing error from accumulating to the point where reacquisition of precise transmitter timing would require an excessive amount of time.

Note that both the energies and noise densities associated with the clock and ranging signals can be unequal if the signals incident on the satellite in the clock and ranging slots have different amplitudes. In applications where the satellite bandwidth is not large in comparison with the data rate, the noise density over the duration of a slot can be affected significantly by noise radiated from the satellite if the amplitude of the up-link signal occupying that slot is marginal. The remainder of the discussion will be restricted to the case where the energies and noise densities are equal:

$$E_c = E_r = E_o \tag{4}$$

and

$$N_{co} = N_{ro} = N_{oo}. \tag{5}$$

In deriving the expression for $\sigma_{\varepsilon r}/$ from which the bound given by Eq. (3) was obtained, it was assumed that the clock loop is corrected several times during the round trip delay experiences by the ranging pulses. This condition will normally exist in an operational TDMA system. Although a means for delaying the ranging pulses by a sufficient amount to make the assumption valid was not available in the experiment, it was possible to investigate the validity of the basic analytical approach and the two-loop model (see Fig. 19 of reference [2]) through bench testing.* First, the round trip delay was set equal to zero in the model and an expression for the normalized rms timing error derived using the analytical approach employed previously. Results obtained by bench testing were then compared with the modified analytical results ' and appropriate conclusions drawn.

It was shown analytically that timing error ε_r, remains only periodically stationary when the round trip delay is set equal to zero. When the timing error is sampled immediately following closed-loop corrections in the ranging loop (and at these instants only), enabling the cross strapping circuit does not change the calculated value of $\sigma_{\varepsilon r}/\Delta$ provided the ranging loop's gain equals either one or one-half. That is, Eq. (2) also applies when cross strapping is employed if 1) the round-trip delay equals zero, 2) the timing error samples are taken immediately after closed loop corrections in the ranging loop, and 3) loop gain A_r equals either one or one-half. All of these conditions were satisfied in the experiments. Measured values of $\sigma_{\varepsilon r}/\Delta$ obtained with the cross-strapping circuit both enabled and disabled are compared with curves calculated using Eq. (2) in Fig. 14. Compensated analytical results obtained by adding the theoretical results and the measured rms quantization error divided by Δ in an rms. sense are also shown. As anticipated from results reported previously, the analytical and experimental results are in close agreement when cross strapping is inhibited and when quantization error contributes

*Sufficient time was not available for performing experiments involving operational satellites.

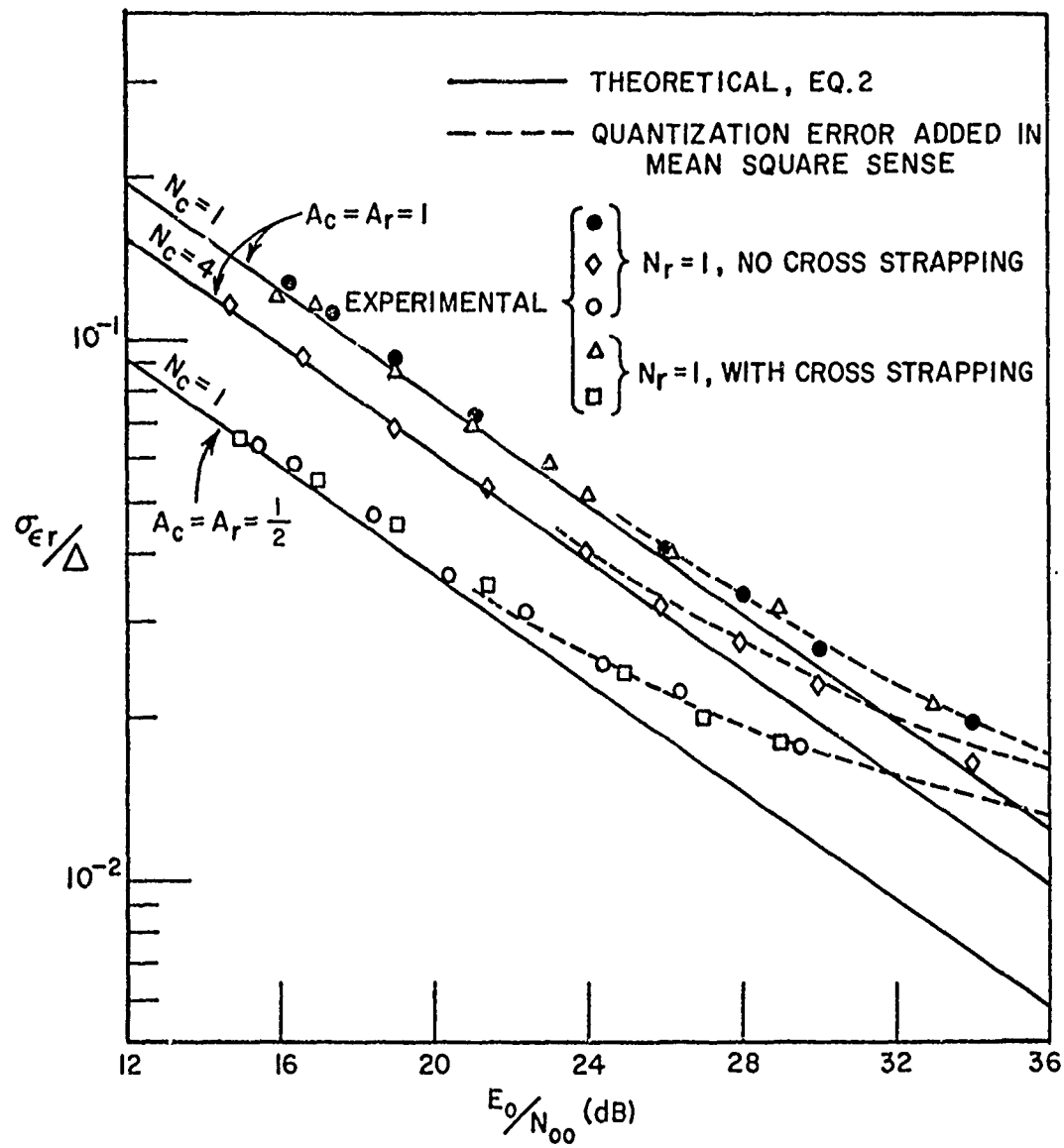

Fig. 14. Two-loop timing jitter versus pulse energy to noise density ratio when the cross strap is either enabled or disabled.

negligibly to the overall jitter. However the rms quantization error in the two-loop system was expected to be forty percent larger than in the clock loop rather than the measured increase of less than fifteen percent. Apparently, the reduction in the percentage increase was due to the design changes incorporated in the time base correction circuits;

the quantization errors are definitely dependent rather than independent in the second generation synchronizer. As predicted by the modified analysis, enabling the clock to ranging loop cross strap does not significantly affect the timing jitter (at the instants where the error samples were taken). Note that this conclusion applies even when the quantization time base corrections are the dominant source of jitter. However, it is anticipated that the cumulative quantization error would increase when the cross strapping circuit is enabled if the round trip delay were large relative to the spacing between clock loop corrections.

The response of the experimental synchronizer to a constant rate of change in signal delay was also investigated by bench testing. A constant network clock signal delay rate was simulated as described previously. As anticipated, the delay rate of the transmit time base resulting from the open-loop corrections was exactly equal to the negative of the clock signal's delay rate. It can be shown[2] that this response results in the compensation of errors due to relative satellite/terminal motion and a doubling of the timing error due to an offset in the system oscillator frequency.

IV. ACQUISITION CONSIDERATIONS

A. Introduction

As noted previously, the magnitude of the clock loop timing error, $|\varepsilon_c|$, must be less than $3\Delta/2$ seconds before the clock loop will respond to reduce $|\varepsilon_c|$ to a small value; similarly, the error in arrival time of the ranging pulses relative to the time base of the locked local clock, $\varepsilon_{r/c}$, must have a magnitude smaller than $3\Delta/2$ seconds for the ranging loop to respond properly. Thus, means for acquiring lock and identifying a loss of lock in both the clock and ranging loops must be provided. In this section, selected details of the acquisition problem will be addressed. A more general discussion of the factors which must be considered in designing acquisition subsystems is contained in reference[1].

B. Clock Loop Acquisition

One method which can be used to acquire lock in the clock loop is to increment the time base of the local receive clock in discrete steps until the timing error is reduced to a sufficiently small value. To instrument this approach, a means must be provided for stopping the open-loop search and enabling closed-loop corrections at the appropriate instant. The required stop-search decision can be based on a comparison between the sum output of the correlation processor at the clock loop sampling instants and a threshold voltage. As shown in Fig. 3, the deterministic component of the sum output is constant at its maximum value when the timing error has a magnitude less than $\Delta/2$ seconds, i.e., when the error is within the clock loop's linear tracking range. Thus, a Δ second search increment can be employed; the time base can be incremented only once for each clock pulse received. Two basic factors must be considered in designing an acquisition subsystem of this type. First, an estimate of the clock signal's amplitude is required before the threshold level can be appropriately set. In some applications, the clock signal's amplitude is known *a priori* to within the accuracy required for setting the threshold properly. However, an accurate estimate of the signal level may not be available at an airborne terminal. For this case, the required estimate can be obtained by searching through the total time uncertainty and using a peak follower circuit to store the peak value of the correlation processor's sum output during the search interval. The threshold level could then be set at a fraction of the peak voltage and the search continued. A lower limit could be imposed on the threshold level to prevent erratic operation when the signal amplitude is not adequate for proper operation of the loops.

The second basic consideration in designing a clock loop acquisition subsystem is the method employed to distinguish the clock pulses from other signals present on the down link during acquisition. As

noted previously, a unique carrier frequency and/or code can be assigned to the network clock signal to make it distinguishable from the data, ranging, and linking signals. Unfortunately, the effect these latter signals have on the sum output of the correlation processor at the sampling instants is, in general, difficult to predict. Moreover, general conclusions cannot be drawn from a specific set of experimental results since the undesired responses depend on code length(s), code structure(s), code starting point(s), frequency offset(s), filter characteristics, and the bit streams modulating the data and linking signals.* However, a specific set of experimental results does provide a point of reference. Several tests performed to determine the feasibility of using the same code to modulate clock and ranging pulses having different carrier frequencies are described in the following paragraph.

In one series of tests, a network clock signal having fixed parameters was applied at the synchronizer's input, a second signal having a variable carrier frequency was summed with the clock signal, and an oscilloscope was used to observe the sum output of the correlation processor as a function of time. The modulation impressed on the second signal was selectable from the following alternatives: 1) no amplitude or phase modulation, 2) on/off amplitude (pulse) modulation only, 3) biphase modulation only by a code having the same structure as the clock signal code, and 4) a combination of on/off amplitude and biphase modulation. This latter alternative permitted the simulation of ranging pulses having a different carrier frequency than the network clock signal. Except for a time displacement, the

*Of course, an acceptable response can be obtained by assigning a separate frequency band to clock signal transmission. However, this approach results in an inefficient use of the frequency spectrum.

amplitude modulation waveform was identical to the waveform used to pulse the network clock signal. The code employed in the synchronizer (see Fig. 1) and its starting point were selected on the basis of instrumentation simplicity rather than minimization of undesired responses. Seven ones are contained in the code generator shift register stages at the beginning of each signal pulse. To simplify testing, the clock loop was first locked to the network clock signal and the second signal then applied. A constant rate of slip between the time bases of the two signals was introduced by offsetting the modulation rate associated with the second signal. Most observations were made with the amplitudes of the two signals set at the same value.* For this case, it was found that the second signal had the least effect on the correlation processor's sum output when it was unmodulated. Pulsing the second signal resulted in the sum output having a peak value approximately equal to one-sixth the clock signal response under worst-case conditions, i.e., when the time base slip assumed the worst-case value and the frequency offset equaled zero. Of course, when both on/off amplitude and biphase modulation was impressed on the second signal and the frequency offset equaled zero, the peak responses to the two signals were equal under worst-case timing conditions. The maximum value of the response to the second signal did not decrease monotonically as the frequency offset was increased from zero. However, offsets greater than approximately 15 KHz (three times the noise bandwidth of the filters in the correlation processor) resulted in worst-case responses no greater than approximately one-fourth the peak clock signal response. This level of distinguishability would be adequate in systems where the error in the signal amplitude estimate is three decibels or less.

*In an operational system, the network clock signal's amplitude will usually be greater than or equal to the amplitudes of the other signals present on the down link.

The feasibility of biphase modulating the clock and ranging signals with different codes to make the clock signal distinguishable was also investigated experimentally. The code used to modulate the second signal was generated by performing an exclusive or operation on the outputs of stages four and seven and applying the result to the input of the first stage. When the second signal was pulsed, seven ones were contained in the shift register stages at the beginning of each pulse. With the carrier frequency offset set equal to zero, the peak value of the undesired response under worst-case timing conditions was approximately equal to one-fourth the peak clock signal response. The undesired response could undoubtedly be decreased by selecting the codes and their starting points so that the partial cross correlation function associated with the codes has a minimum peak value. Irrespective of whether or not a reduction can be achieved, the experimental results show that separate codes can be used to distinguish the clock signal from the ranging signals provided the uncertainty in the estimate of the clock signal's amplitude is no greater than a few decibels.

C. Ranging Loop Acquisition

Ranging loop acquisition is inhibited until after the clock loop has been enabled and an in-lock criterion satisfied. Acquisition of proper transmitter timing requires a coarse estimate of the round trip propagation delay which can be either available *a priori* or provided by a separate subsystem. This estimate must be sufficiently accurate to allow the transmission of the ranging pulses so that they "fall" within time slots assigned to the accessing terminal. To reduce the magnitude of the timing error to less than $3\Delta/2$ seconds, the transmit time base can be incremented by small amounts, e.g., in Δ second increments. As in the clock loop acquisition circuit, the sum output of the correlation processor sampled at appropriate instants can be compared to a threshold voltage to determine when

search should be stopped. However, since the intervals occupied by the ranging pulses when the transmitter is properly timed are known, there is no need for the ranging pulses to be distinguishable from the other signals present on the down link. Moreover, in most applications, the ranging pulses and the network clock signal have approximately the same amplitudes (during their respective on times) on the down link. For this case, the threshold level in the ranging loop acquisition circuit can be derived by filtering the samples of the correlation processor's sum output taken at the clock loop sampling instants and appropriately scaling the filtered signal. Thus, no basic difficulties are normally encountered after the ranging pulses have been timed to fall within slots assigned to the accessing terminal. Two techniques for timing the ranging pulses initially when a sufficiently accurate estimate of the round trip propagation delay is not available a priori were described and their limitations dicussed in reference [1]. A relatively detailed description of how one of these techniques can be instrumented is given in the following paragraph.

A low-level, frequency-swept (chirped) signal can be transmitted on the up-link, received on the down-link, and correlation processing employed at the receiver to determine when transmitter timing is nominally correct. The use of a sawtooth frequency modulation is recommended. For convenience of discussion, it will be assumed temporarily that a sawtooth waveform is generated in synchronism with the transmit time base and used to sweep the frequency of the transmitted (coarse ranging) signal. The sawtooth's period must be at least as large as the total uncertainty in the round-trip propagation delay. A reference signal is generated in the receiver by frequency modulating a sinusoid with a second sawtooth waveform having a time base determined by the locked receive clock. The two frequency modulation waveforms differ only in that their

time bases are displaced. Now, the time base of the transmitter is searched in discrete increments to remove the initial timing error. When proper timing is established, the frequency modulations present on the received coarse ranging signal and the reference signal generated in the receiver will be aligned in time; thus, the signal frequencies will differ by a constant. The value of this constant depends on the carrier frequencies of the two frequency-modulated sinusoids, and on the frequency translations and doppler shifts experienced by the coarse ranging signal on arriving at the input to the coarse-ranging correlation processor. In the processor, the received coarse ranging signal is multiplied by the reference signal, the difference frequency component of the product is bandpass filtered, the filter's output is detected, and the detected signal is compared with a threshold voltage to provide a means for identifying when the time bases are properly aligned.

Ideally, the filter's center frequency would be exactly equal to the constant difference which exists between the two signal frequencies when correct timing is established; in practice, the constant frequency difference is not known exactly due to error in the doppler-shift estimate and to uncertainties in system-oscillator frequencies. When the estimate of the received coarse ranging signal's carrier frequency is in error by Δf Hertz and the filter's center frequency equals the value appropriate when Δf equals zero, it can be shown that the filter response peaks when the transmit time base is in error by an amount

$$\varepsilon_t \doteq \frac{\Delta T}{\Delta F} \Delta f \tag{6}$$

where ΔT represents the period of the sawtooth frequency modulation waveforms and ΔF represents the peak to peak frequency deviation. If necessary to ensure reliable threshold crossings, the filter's bandwidth, B_f, can be made smaller than $2|\Delta f|$ to increase the ratio of the

signal power to the noise power at the filter's output. A tradeoff is involved in specifying B_f since the search time increases as B_f is decreased. The maximum allowable value of the transmit time base search increment is given approximately by

$$(7) \qquad \Delta\epsilon_{t_{max}} \approx \frac{\Delta T}{\Delta F} B_f \ .$$

The search increments should be spaced by $1.5\ B_f^{-1}$ seconds or more to allow adequate time for the filter to respond between increments. In many practical applications, a search increment spacing of $1.5\ B_f^{-1}$ seconds would be small compared to the round trip propagation delay and a transmit time base overshoot would result if that spacing were employed. Circuitry for removing the overshoot after a threshold crossing has occurred at the receiver can be incorporated in the coarse-ranging subsystem or the spacing between search increments can be increased to a value which exceeds the round trip propagation delay. If the latter alternative is selected, the coarse ranging signal can be pulsed, e.g., the pulse length can be set equal to ΔT and B_f can equal $1.5(\Delta T)^{-1}$. Pulsing the ranging signals transmitted by the network terminals allows them to be time division multiplexed on a relatively crude basis to minimize the problem of distinguishing between ranging signals transmitted simultaneously by two or more terminals.

The fundamental problem encountered in instrumenting a coarse-ranging subsystem using the approach described in the preceding two paragraphs is the generation of two frequency-swept signals which track in frequency when the time bases of the modulation waveforms are aligned. Frequency tracking error places a lower limit on the bandwidth of the filter in the coarse-ranging correlation processor. In some applications, matched voltage-controlled crystal oscillators (VCXOs) may be employed to generate the required signals. However,

this approach requires the maintenance of an accurate calibration and the use of relatively high-cost VCXOs. As an alternative, digital circuits can be used to generate a signal having a frequency which changes by discrete amounts at specific instants in time. The frequency steps can be smoothed out by applying the signal as the reference input to a phase lock loop (PLL) having an appropriate transient behavior, and taking the output from the loop's voltage controlled oscillator (VCO). The VCO need not be particularly stable nor is a linear relationship between frequency offset and the control voltage required since the VCO's output is locked to the reference input. The remainder of this section is devoted to a more detailed description of the hybrid frequency-sweeping technique and circuits instrumented to demonstrate its feasibility.

A square wave having a period which changes in discrete, equisize steps at uniformly spaced instants in time can easily be instrumented by employing a frequency divider (counter) having a modulus which changes by one at uniformly spaced instants to process a fixed-frequency clock signal. However, since the frequency of a signal is equal to the inverse of the signal's period, a constant average rate of change in a waveform's period with time does not result in a constant average rate of change in frequency. If the counter modulus is increased with time, frequency linearity can be improved by decreasing the spacing between the instants at which the modulus is changed as time increases. This can be accomplished as shown in Fig. 15. Counter A divides clock frequency f_c by a number a which is determined by word d contained in counter D. A modulo-two counter is used to generate a square wave signal from the output of counter A suitable for application to the reference input of the PLL. Dividers B and C determine the number of clock signal transitions required to change the state of counter D. Counter C has a constant modulus of c_0 and is used solely to reduce the rate at which counter D is

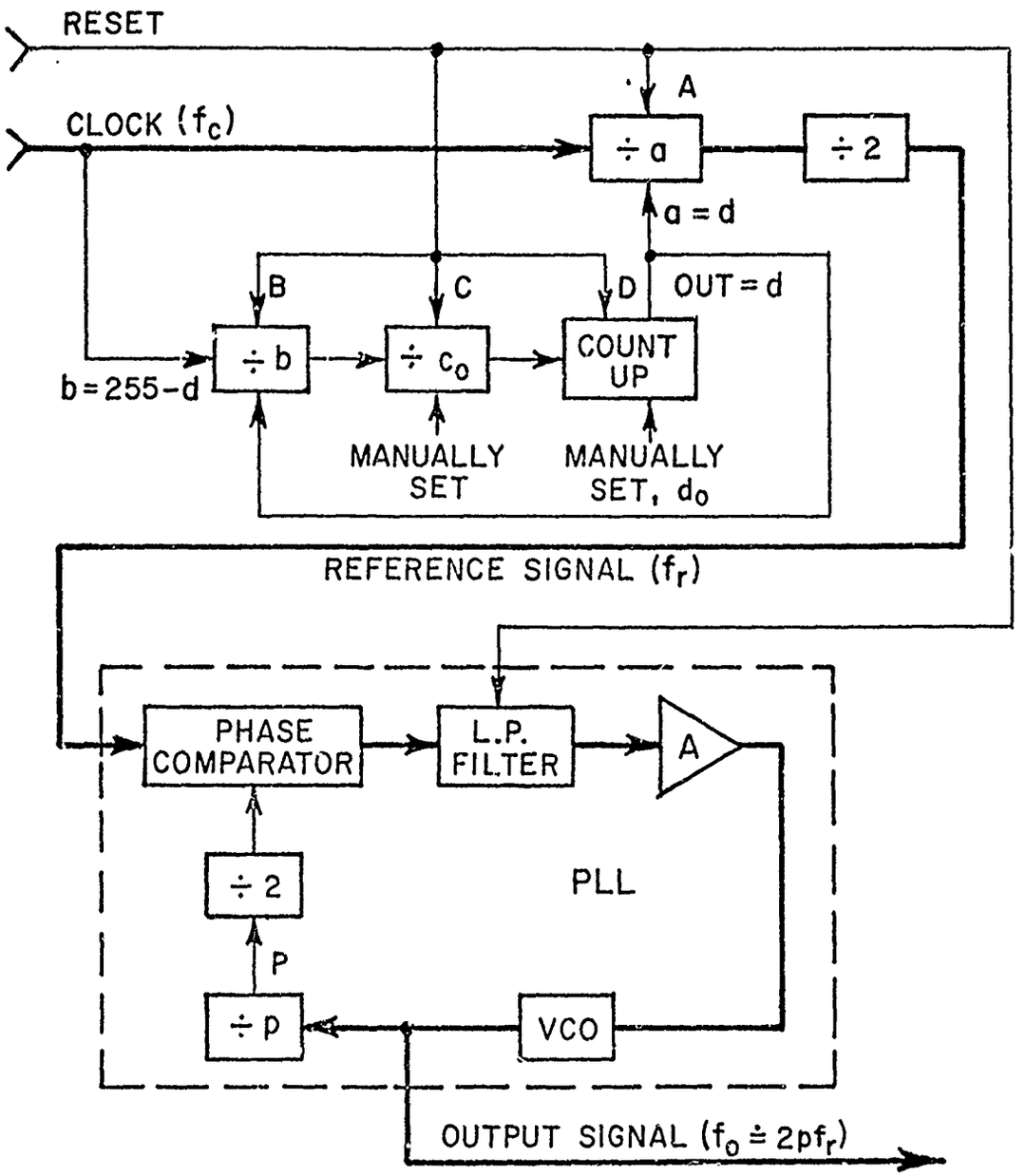

Fig. 15. Block diagram of the digital/analog frequency-sweeping circuit.

clocked, i.e., to expand the time scale. The modulus of counter B decreases by one each time counter D is incremented; thus, the rate at which counter D is clocked increases with time. A schematic diagram of circuits instrumented to demonstrate the feasibility of the frequency sweeping technique is shown in Fig. 16. Eight bit, presettable up/down counters were used to instrument counters (dividers) A, B, C, and D. To keep the package count at a minimum, it was necessary to set b, the modulus of counter B, equal to 255-d. In general, a different relationship between b and d could be established. The frequency of the output signal is nominally equal to 2p times the frequency of the reference signal since a modulo 2p counter is connected between the VCO's output and the phase detector input.

An expression for the instantaneous frequency of the reference signal in the experimental circuit, f_r, will now be derived. At time t equal to zero, a reset pulse is applied to the counters which forces the following initial conditions:

(8) $d(0+) = d_o$,

(9) $a(0+) = d_o$,

(10) $b(0+) = 255-d_o$, and

(11) $f_r(0+) = \frac{f_c}{2d_o}$.

The count contained in counter D increases by one at

(12) $t = t_1 = \Delta_1 = \frac{b_o c_o}{f_c} = \frac{(255-d_o)c_o}{f_c}$

and f_r decreases to

(13) $f_r(\Delta_1^+) = \frac{f_c}{2(d_o+1)}$.

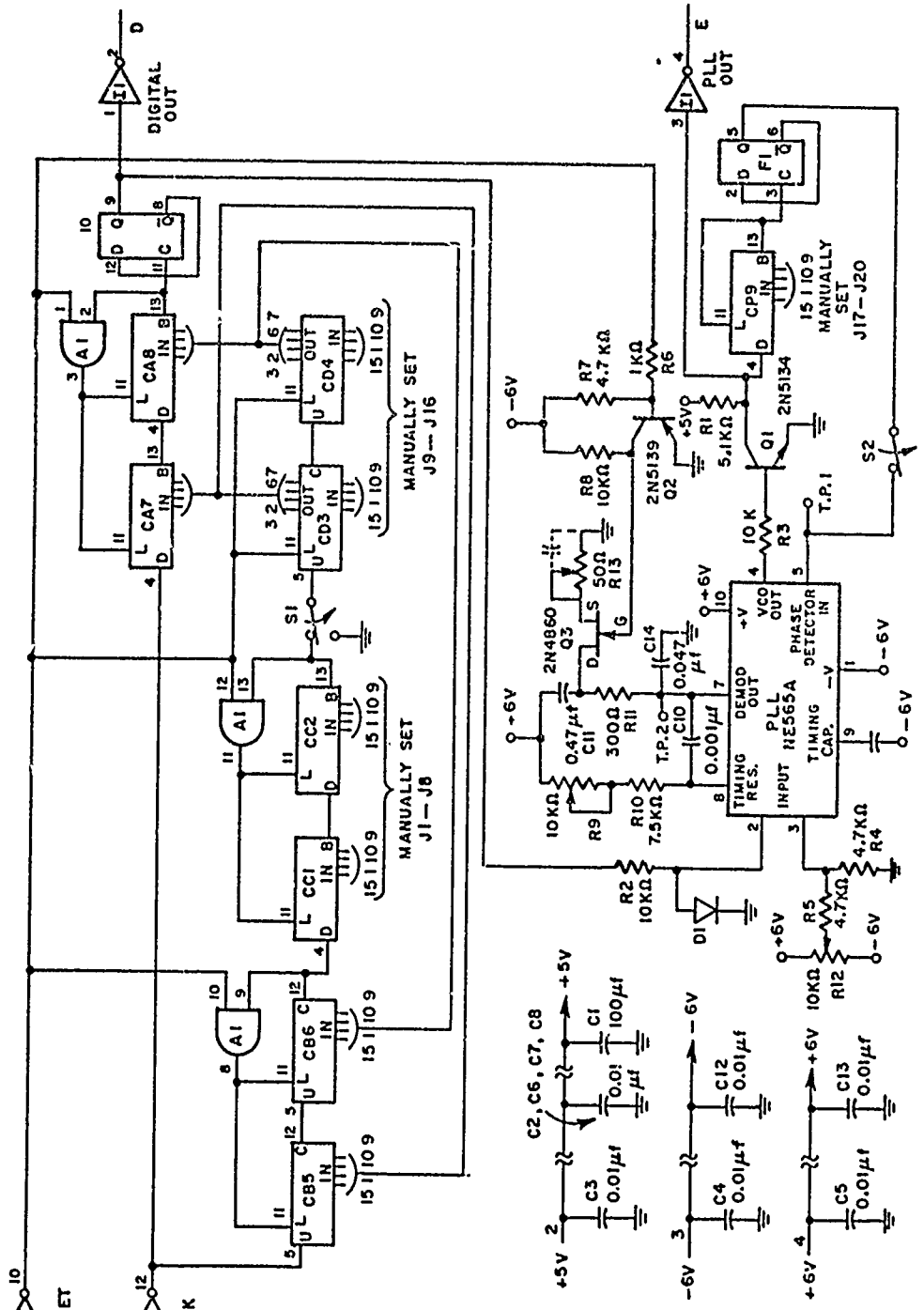

Fig. 16. Schematic diagram of the experimental digital/analog frequency-sweeping circuit.

After one additional period of the clocking waveform has elapsed, the new value of d is loaded into counter B. It can be shown that the Nth transition in the state of counter D occurs at

$$t = t_N = \Delta_1 + \sum_{n=2}^{N} \Delta_n \quad ; \quad N \geq 2 \tag{14}$$

where

$$\Delta_n = \frac{\{255-[d_o+n-1]\}\, c_o+1}{f_c} \quad . \tag{15}$$

The frequency of the reference signal for $t_{N-1} < t < t_N$ is given by

$$f_r(t) = \frac{f_c}{2(d_o+N-1)} \quad ; \quad t_{N-1} < t < t_N \quad . \tag{16}$$

Using Eqs. (14) and (15) to solve for N as a function of t_N and substituting the result in Eq. (16) gives

$$f_r(t) = \frac{f_c}{2\left\{\frac{1}{c_o} + 255.5 - \left[\left(d_o - \frac{1}{c_o} - 256.5\right)^2 - \frac{2}{c_o}(t_N f_c+1)+1\right]^{1/2}\right\}} ; \tag{17}$$

$$t_{N-1} < t < t_N \quad .$$

Clearly, f_r is not related linearily to t_N. As t_N increases from zero, $f_r(t_N^-)$ decreases at a decreasing rate until

$$t = t_i = \frac{c_o}{2f_c}\left[\left(d_o - \frac{1}{c_o} - 256.5\right)^2 - \frac{2}{c_o} + 1 - \frac{1}{9}\left(\frac{1}{c_o} + 255.5\right)^2\right]. \tag{18}$$

At this instant,

$$f_r(t_i) = f_{ri} = \frac{3f_c}{4\left(\frac{1}{c_o}+255.5\right)} \quad . \tag{19}$$

As t_N increases beyond t_i, $f_r(t_N^-)$ decreases at an increasing rate. For t in the vicinity of inflection point t_i, the equation for the frequency of the reference signal at t_N^- as a function of t_N can be closely approximated by a linear expression.

In the experimental circuits, frequency f_c equaled 19.5 MHz; parameters c_o and d_o equaled 51 and 147, respectively. For p equal to one, the frequency of the VCO signal is nominally equal to $2f_r$. A graph of $2f_r$ as a function of time is given in Fig. 17. The period

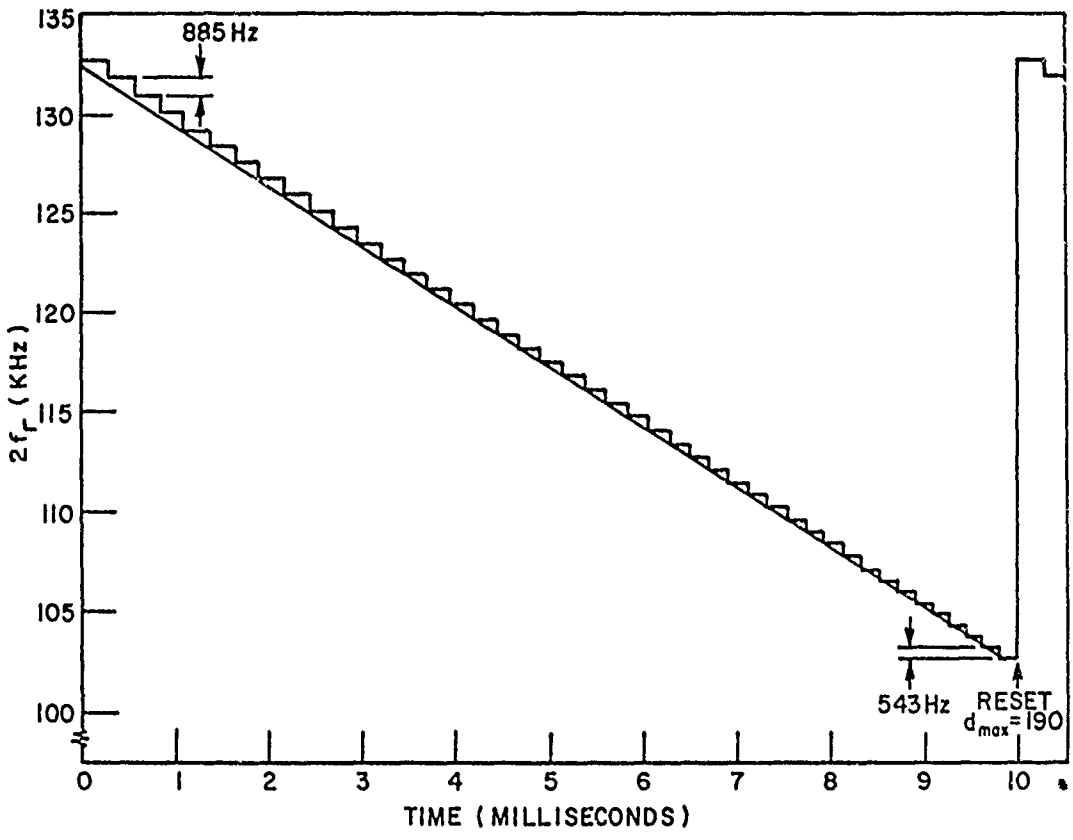

Fig. 17. Twice the frequency of the reference signal in the experimental frequency-sweeping circuit as a function of time.

of the effective modulation waveform is determined by the spacing of the reset pulses: approximately 10 msec in the experimental circuits.

Clearly, the clock signal can be used to generate two frequency-stepped reference signals which are identical except for a time base displacement. Now, if the PLLs used to smooth out the frequency steps in the reference signal are identical and their parameters are appropriately specified, the VCO signals will be identical except for a time base displacement and their frequencies will vary essentially linearily with time. Since the motivation for using a digital frequency synthesis technique is to avoid the need for matched VCOs, it must be shown that the PLL parameters need not be identical to achieve acceptable tracking of the frequency-swept output signals before use of the hybrid digital/analog synthesis technique can be recommended. To this end, two experimental circuits having a schematic diagram as shown in Fig. 16 were instrumented and appropriate experiments conducted. The NE 565A integrated circuit PLLs were selected at random and the tolerance of the peripheral resistors and capacitors equaled or exceeded ±5%. The circuits were reset by the same pulse train and the two VCO output signals were displayed on an oscilloscope to permit observation of the phase tracking accuracy. Except for a brief interval of time following each reset pulse, the signal phase angles varied almost identically with time. Unfortunately, a means for accurately measuring the instantaneous frequency was not available. Observations made of the control inputs to the VCOs (the demodulation outputs of the PLLs) indicated that the frequencies of the VCO signals varied relatively smoothly with time but in a somewhat exponential-like fashion between steps in the frequencies of the reference signals. Limitations on time and other resources prevented optimization of the loop filter and the construction of frequency conversion, modulation, and correlation processing circuits for evaluating technique effectiveness more thoroughly. However, there does not appear to be any basic obstacle to utilization of the hybrid frequency-sweeping technique in practical systems.

V. SUMMARY AND CONCLUSIONS

In this report, a second-generation TDMA-system synchronizer has been described and experimental results obtained by bench testing have been given which characterize the synchronizer's performance. Emphasis was placed on presenting information needed to design synchronizers employing coupled sampled-data delay-lock loops when only coarse estimates of signal parameters and the instantaneous system geometry are available a priori. It was shown that the effective gain of the control loops can be held at a design value when the signal amplitude is unknown and/or the estimate of the signal carrier frequency is in error by using a forward-acting automatic gain control (FAAGC) circuit. The noise component of the signal amplitude in the FAAGC circuit was shown to have a minimal influence on timing jitter, i.e., analytical results applicable when the loop gain is constant can be used to design synchronizers incorporating FAAGC circuits. To the extent practical by bench testing, the feasibility of cross-strapping clock-loop corrections into the ranging loop in an inverted sense to compensate for the effects of relative satellite/terminal motion on timing error was demonstrated. Techniques employed previously to model the cross-strapped loops and to calculate the effects of cross strapping on timing error were shown to be sound.

Methods for acquiring lock in the clock and ranging loops when the signal amplitude and initial round-trip propagation delay are not accurately known were considered. It was concluded that the clock signal can be adequately distinguished from other signals occupying the TDMA format during clock loop acquisition if reasonable care is exercised in design. A technique for utilizing a frequency-swept, low-level signal to obtain the coarse estimate of the round-trip propagation delay required to time the pulsed transmissions initially was described. To simplify the problem of making the coarse ranging signals transmitted by the aggregate of terminals distinguishable, they

could be pulsed and time division multiplexed on a relatively crude basis. Experiments performed to date indicate that this technique is feasible and that a coarse-ranging subsystem can be instrumented at a reasonable cost by employing hybrid (digital/analog) frequency-synthesis circuits.

REFERENCES

1. Huff, R.J., "TDMA Space Communications Systems: Concepts and Practical Techniques," Report 2738-4, November 1971, Electro-Science Laboratory, Department of Electrical Engineering, The Ohio State University; prepared under Contract No. F30602-69-C-0112 for Rome Air Development Center, Griffiss AFB, N. Y.

2. Huff, R.J., Reinhard, K.L., and Upp, D.C., "The Synchronization of Time Division Multiple Access Systems -- An Analytical and Experimental Study," Report 2358-9, 31 January 1969, Electro-Science Laboratory, Electrical Engineering Department, The Ohio State University Research Foundation; prepared under Contract F30602-67-C-0119 for Rome Air Development Center, Griffiss Air Force Base, New York. (AD 689 223)

3. Huff, R.J., "The Imperfectly-Timed Demodulation of Differential Phase Shift Keyed Signals," Report 2738-1, June 1969, Electro-Science Laboratory, Electrical Engineering Department, The Ohio State University Research Foundation; prepared under Contract F30602-69-C-0112 for Rome Air Development Center, Griffiss Air Force Base, New York. (AD 695 504)

4. Huff. R.J. and Reinhard, K.L., "A Sampled-Data Delay-Lock Loop for Synchronizing TDMA Space Communications Systems," presented at EASCON 1968, Washington, D.C., September 9-11, 1968.

5. Huff, R.J., "An Investigation of Time Division Multiple Access Space Communications Systems," Ph.D. Dissertation, The Ohio State University, Columbus, August 1969.

6. Huff, R.J. and Reinhard, K.L., "A Delay-Lock Loop for Tracking Pulsed-Envelope Signals," IEEE Trans. Aerospace and Electronic Systems, Vol. AES-7, May 1971, pp. 478-485.

7. Reinhard, K.L., "Analysis of a Pseudo-Random Network Timing System for Time-Division Multiple Access Communications," Report 2358-2, 2 June 1967, ElectroScience Laboratory, Department of Electrical Engineering, The Ohio State University Research Foundation; prepared under Contract F30602-67-C-0119 for Rome Air Development Center, Griffiss Air Force Base, New York. (AD 820 800L)

8. Wallace, K.A., "The Tracking Performance of Sampled-Data Delay-Lock Loops with Pulsed Envelope Input Signals," Report 2358-7, 26 June 1968, ElectroScience Laboratory, Electrical Engineering Department, The Ohio State University Research Foundation; prepared under Contract F30602-67-C-0119 for Rome Air Development Center, Griffiss Air Force Base, New York. (AD 821 657)

9. Gill, W.J., "A Comparison of Binary Delay-Lock Tracking Loop Implementations," IEEE Trans. Aerospace and Electronic Systems, Vol. AES-2, July 1966, pp. 415-424.