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Los Alamos Scientific Laboratory Acoustic Locator System

Vol. V
Telemetry Display System (TDS) Maintenance Manual

by

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CONTENTS

LOS ALAMOS SCIENTIFIC LABORATORY ACOUSTIC LOCATOR SYSTEM,

TELEMETRY DISPLAY SYSTEM (TDS) MAINTENANCE MANUAL

CHAPTER 1. INTRODUCTION

1-1 Scope

This manual provides instructions for long-term maintenance of the **Telemetry Display System (TDS)** that is a part of the **Los Alamos Scientific Laboratory Acoustic Locator System.** The system detects the muzzle blast from weapons such as mortars and artillery and computes the precise coordinates of that blast.

The Telemetry Display System is a portable, battery-operated unit used at a central location to display signals transmitted from distant **Azimuth Processors (APs)** by radio or field wire. The TDS contains four readout modules, each capable of accepting signals from eight APs (for a total of 32 signals) and displaying them in sequence on NIXIE-tube visual readouts.

The Azimuth Processor is a portable, battery-operated unit on which the azimuth may be either read locally on a NIXIE-tube visual readout or be transmitted to a TDS by field wire or radio. Signal transmission by high-frequency radio is used over difficult terrain, over distances exceeding about 2 miles, or when field wires are inconvenient.

1-2 Organization of Material

1-2.1 Routine Procedures. Chapters 2, 3, and 4 describe the TDS; contain routine maintenance, setup, and checking procedures; and give instructions for the repair of malfunctions by means of board (card) replacement. These procedures require only careful reading of the text and a trial-and-error approach to locate most ordinary troubles. Laboratory instruments are usually not required for repairs; a multimeter (indicating volts, V, and ohms, Ω) generally suffices.

1-2.2 Special Procedures. Chapters 5, 6, 7, and 8 are, in general, useful only to an electronics expert. No one else should attempt any of the procedures described in these chapters. A multimeter (20,000 Ω/V) and a high-quality oscilloscope are the only laboratory instruments required, but the multimeter must be accurate and must be calibrated by a standards laboratory.

Chapter 5 outlines the theory of operation of all circuits except Board 6, which is covered in LA-4444-TM, Vol. III. Chapter 5 assumes a knowledge of basic electronics and familiarity with the operation of linear amplifiers, multivibrators, single shots, Schmidt trigger circuits, RS and master-slave flip-flops, shift registers, power supply regulators of a switching or linear variety, and dc-to-dc converters. No attempt is made to describe these circuits in detail.

Chapter 6 gives systematic procedures for locating defects on individual boards and, like Chapter 5, assumes detailed knowledge of electronics.

Chapter 7 contains circuit diagrams of individual boards and photographs of the boards with parts labeled according to the circuit diagrams. These are to be used in conjunction with Chapters 5 and 6.

Chapter 8 contains the module wiring diagrams specifying interconnections among the printed board sockets, front panel, and module connectors, and lists the intermodule wiring on special Interconnection Board 37.

1-3 Abbreviations

The following abbreviations are used throughout this manual.

ac	- Alternating current.
AGC	- Automatic gain control.
AP	- Azimuth processor.
A-h	- Ampere-hour.
BCD	- Binary coded decimal.
Board	- Printed circuit card containing wiring and electronic parts. See Chapter 7 for diagrams of the various boards.
Bus	- Any line (wire) carrying signals between more than two points, usually among many points. The term "party-line bus" refers to the TDS output cables, which are connected to the Display System Data Connectors, and to the fact that more than one input may drive the cables and more

than one remote device may be connected to them.

dc - Direct current.

ID - Channel identification (assigned at the azimuth processor). See also Module ID.

LASL-ACL - Los Alamos Scientific Laboratory Acoustic Coordinate Locator system. This abbreviation refers to the system components, from azimuth processors being used to locate sounds to the complete computer system, or any combination of intermediate complexity.

Long Line - The twisted-pair field-wire connection between an azimuth processor and the TDS that carries transmitted data.

Module ID - A two-bit identification number for an individual module that is wired into the module connector, and is sensed in the printer (if attached).

msec - One thousandth of a second.

Parallel Data - Data that are all present simultaneously, one wire or connection being used for each bit of data in a multibit data word.

PSC - Power supply connector.

PSM - Power supply module.

rf - Radio frequency.

RSC - External read (remote reset) push-button connector.

Serial Data - Data transmitted (either by wire or radio one data bit at a time until the whole sequence of data bits (data word) is transmitted. Only one wire or radio channel is required to transmit serial data.

TCG - Test code generator module (labeled Portable Test Azimuth Generator).

TDM - Telemetry display module.

TDS - Telemetry display system (contains 4 TDMs. 1 TTM, 1 PSM, 1 TCG, and 1 Battery).

TDM-1 - Telemetry display module No. 1.

TDS-1 - Telemetry display system connector No. 1.

Terminating Shoe - A connector-mounted termination network that provides a termination for the party-line bus (see p. 56). The party-line bus will not operate without the shoe.

TTM - Time tag module.

V - Volt.

μsec - One millionth of a second.

Ω - Ohm.

CHAPTER 2. GENERAL DESCRIPTION OF TELEMETRY DISPLAY SYSTEM

2-1 Definition

The **Telemetry Display System (TDS)** is a mobile unit capable of receiving up to 32 telemetered or long-line signals and of displaying them visually on four sets of NIXIE tubes. Time tagging and channel identification are also displayed on four corresponding sets of tubes. These data can be transferred directly to a computer or printer system. Figures 2.1 and 2.2, respectively, show the front and rear of the TDS with covers removed.

2-2 Major Components

The telemetry display system consists of the following components.

2-2.1 Cabinet. The waterproof cabinet, 21 in. deep with a 12- by 19-in. opening for the interior panel, has removable covers. The front cover must be removed prior to operation to expose the interior panel.

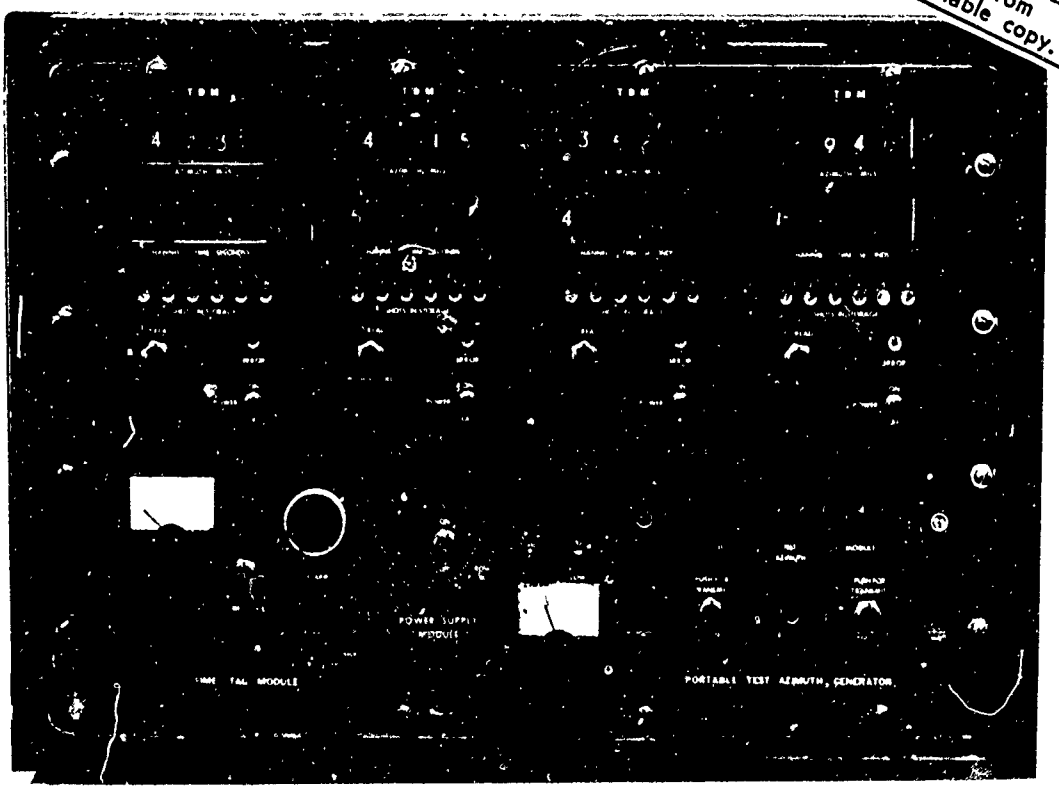


Fig. 2.1. Telemetry Display System (TDS), front view.

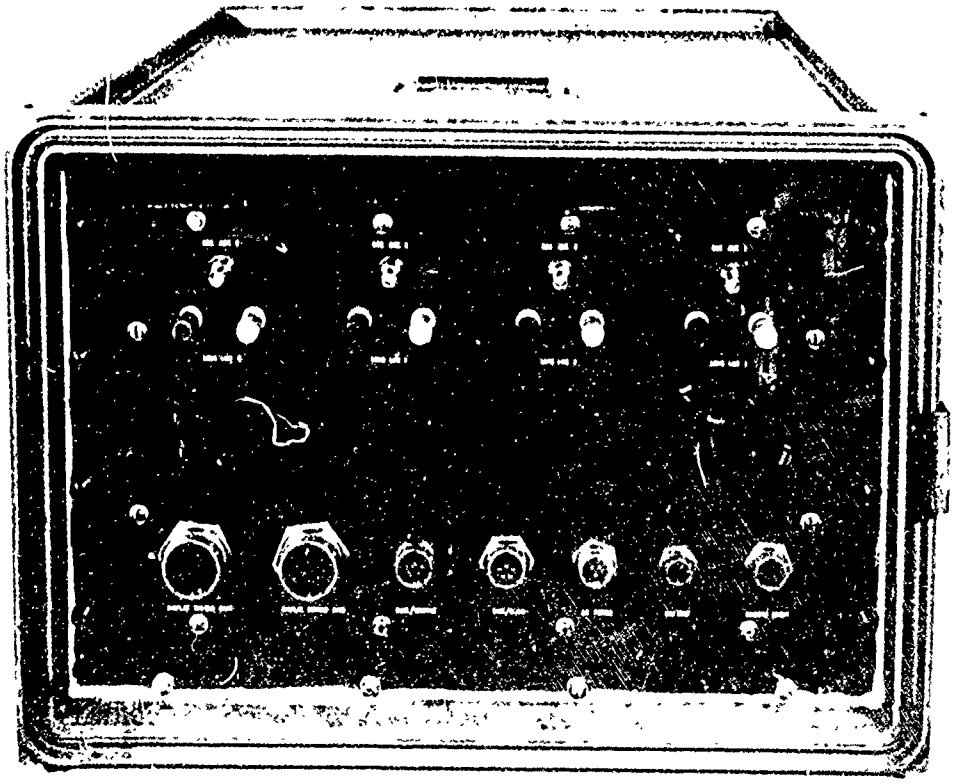


Fig. 2.2. Telemetry Display System (TDS), rear view.

2-2.2 Interior Panel. The interior panel, 12 by 19 in., has cutouts for mounting the seven individual modules and has waterproofing gaskets between the panel and the modules.

2-2.3 Telemetry Display Module. Four TDMs are provided, each of which contains complete circuitry for receiving up to eight telemetered or long-line signals, as well as provisions for six-shot storage in the visual display mode and one-shot storage (only) in the automatic mode, time-tagging and ID circuits, drivers for a party-line bus that can be connected to a computer or printer, NIXIE display tubes, and miscellaneous controls and indicators. The TDMs are numbered 1 through 4, left to right. When the TDS output is connected to the printer, the TDMs have Module ID numbers of 0 through 3 in printout. Figures 2.3 and 2.4 are, respectively, top and bottom views of the TDM.

2-2.4 Time Tag Module. The TTM contains a tuning-fork clock oscillator and dividers and generates the time-tag information that is fed to each of the four TDMs. A bus driver feeds the time-tag information to a printer, an audible alarm warns of shots received in the visual display mode, a push button permits time presetting or resetting, and a signal-strength meter selector switch permits noting the received-signal strengths in each of the four receivers in the TDMs. Figure 2.5 shows the TTM.

2-2.5 Test Code Generator Module. The TCG module, labeled Portable Test Azimuth Generator on its front panel for clarity but historically called TCG, contains the test code generator and switches for generating either single or repetitive serial codes identical to those produced by the APs. The TCG is removed from the cabinet for independent use in the field, with only the addition of a battery and case, to check out transmitters and receivers. The field cabinet is described in LA-4444-TM, Vol. II. Figure 2.6 shows the TCG module.

2-2.6 Power Supply Module. The PSM may be used either as a battery charger or as a system power supply. The system may alternatively be operated from the battery alone. Figure 2.7 shows the PSM.

2-2.7 Wiring Harness. The wiring harness, including Board 37 (a cable-interconnection printed-circuit card), ties the various cables together. The wiring harness has the following connectors.

A. Five 55-pin connectors, four for the TDM and one for the TTM.

B. Two 55-pin rear-panel connectors.

C. One 12-pin PSM connector.

D. Two 5-pin master-slave time clock synchronizing connectors.

E. One 10-pin external reset connector.

F. One 8-pin TCG module connector.

G. One 3-pin 115-V ac connector.

H. One 6-pin battery connector.

I. Four pairs of long-line binding posts.

Figure 2.8 shows the connector panel.

2-2.8 Terminating Shoe. Two terminating shoes terminate the party-line bus system. These shoes, which consist of 300-Ω resistors tied to a 3-V power supply, function as pull-up resistors for the party-line bus. A terminating shoe is shown in Fig. 2.9.

2-2.9 Operating Cables. The following cables are provided.

A. One 55-pin data cable for connecting the output of a system to a printer or computer.

B. One time-slave cable for slaving the time clocks in two or more systems.

C. A remote reset cable and box with four push-button switches for remote readout and reset of the individual TDMs.

D. Two 115-V ac power cables (one spare).

E. Two battery cables (one spare).

Figure 2.9 shows the cables and the terminating shoe.

2-2.10 Battery. The nominal 12-V, 30-A-h nickel-cadmium battery is contained in a metal box along with the temperature-compensated regulator circuit. Figure 2.10 shows the battery box with the lid removed.

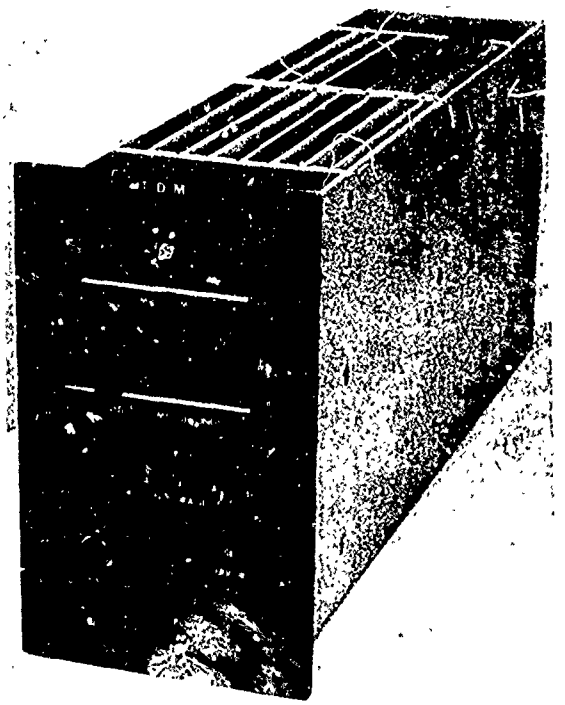


Fig. 2.3. Telemetry Display Module (TDM), top view.

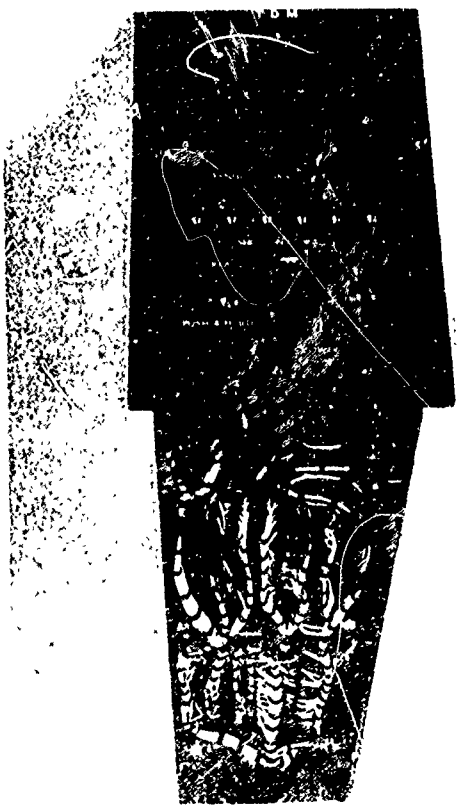


Fig. 2.4. Telemetry Display Module (TDM), bottom view.

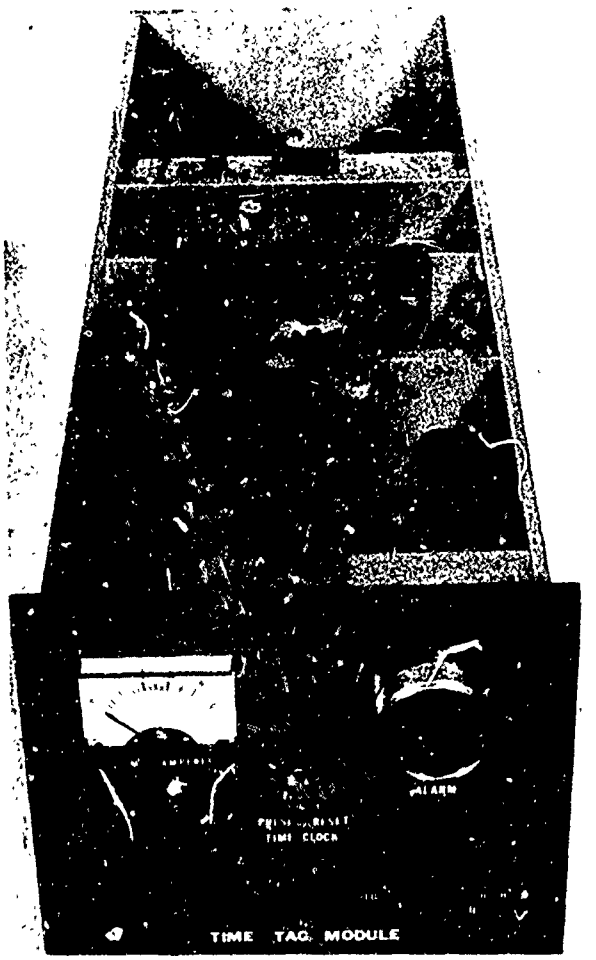


Fig. 2.5. Time Tag Module (TTM).

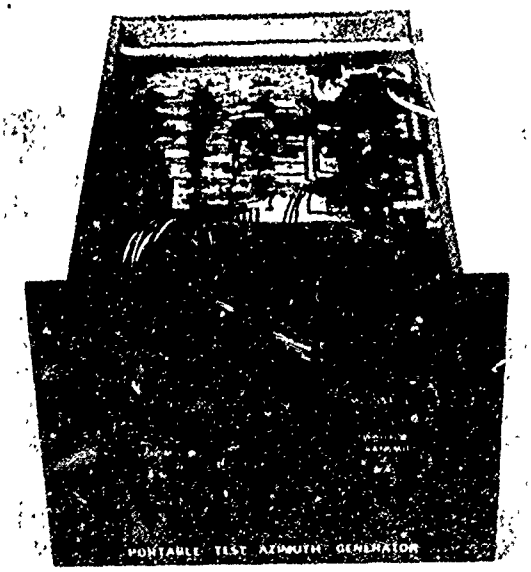


Fig. 2.6. Test Code Generator Module (TCG), labeled Portable Test Azimuth Generator.

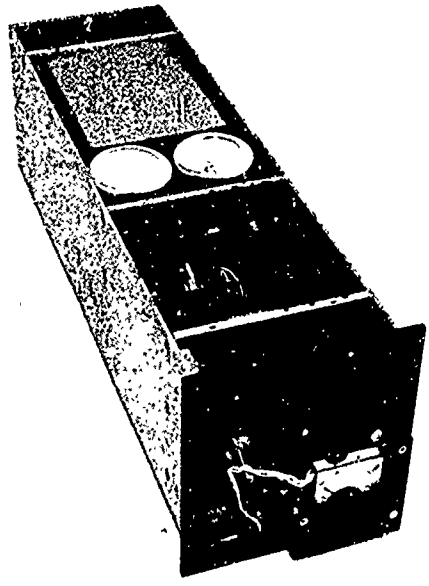


Fig. 2.7. Power Supply Module (PSM

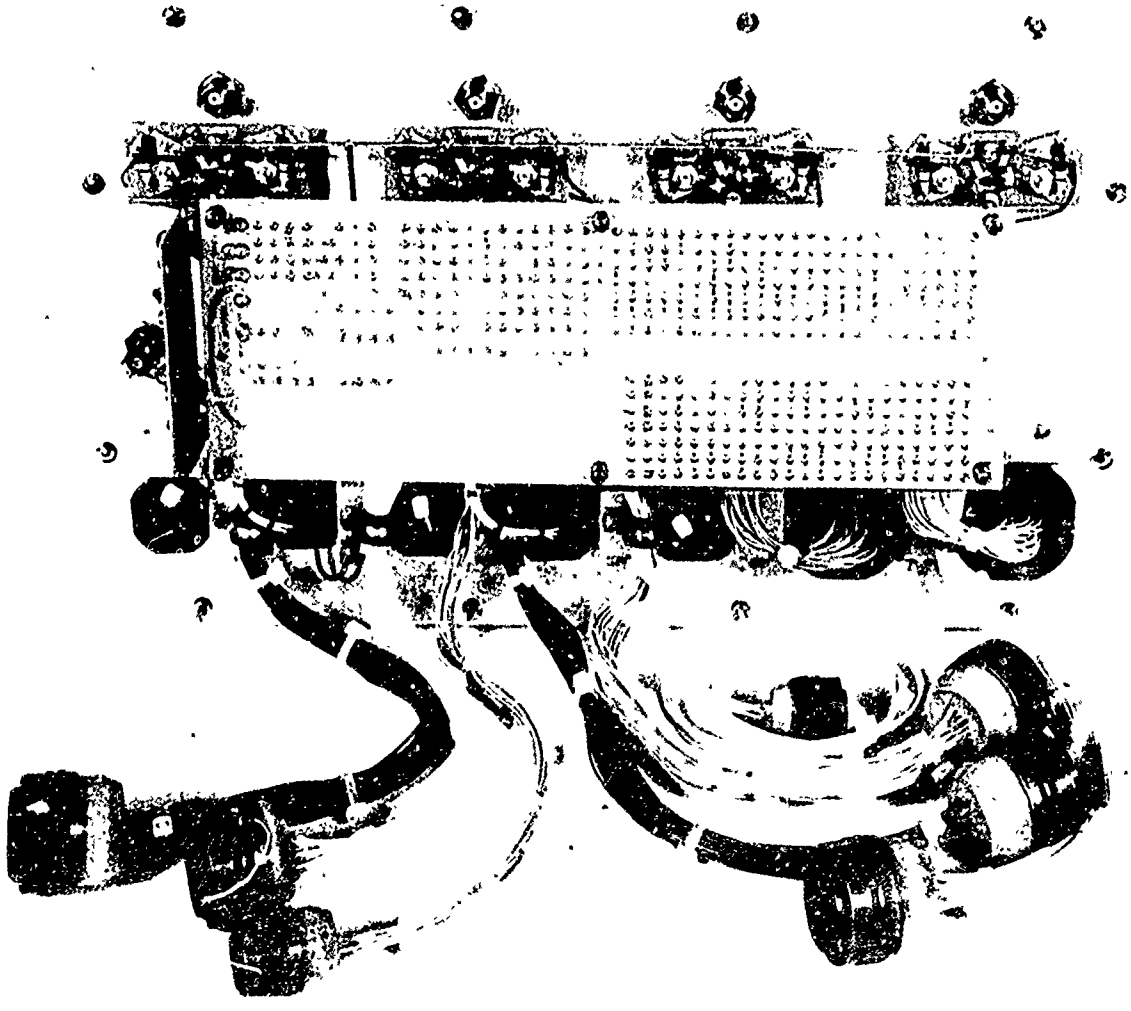


Fig. 2.8. TDS connector panel, interior view.

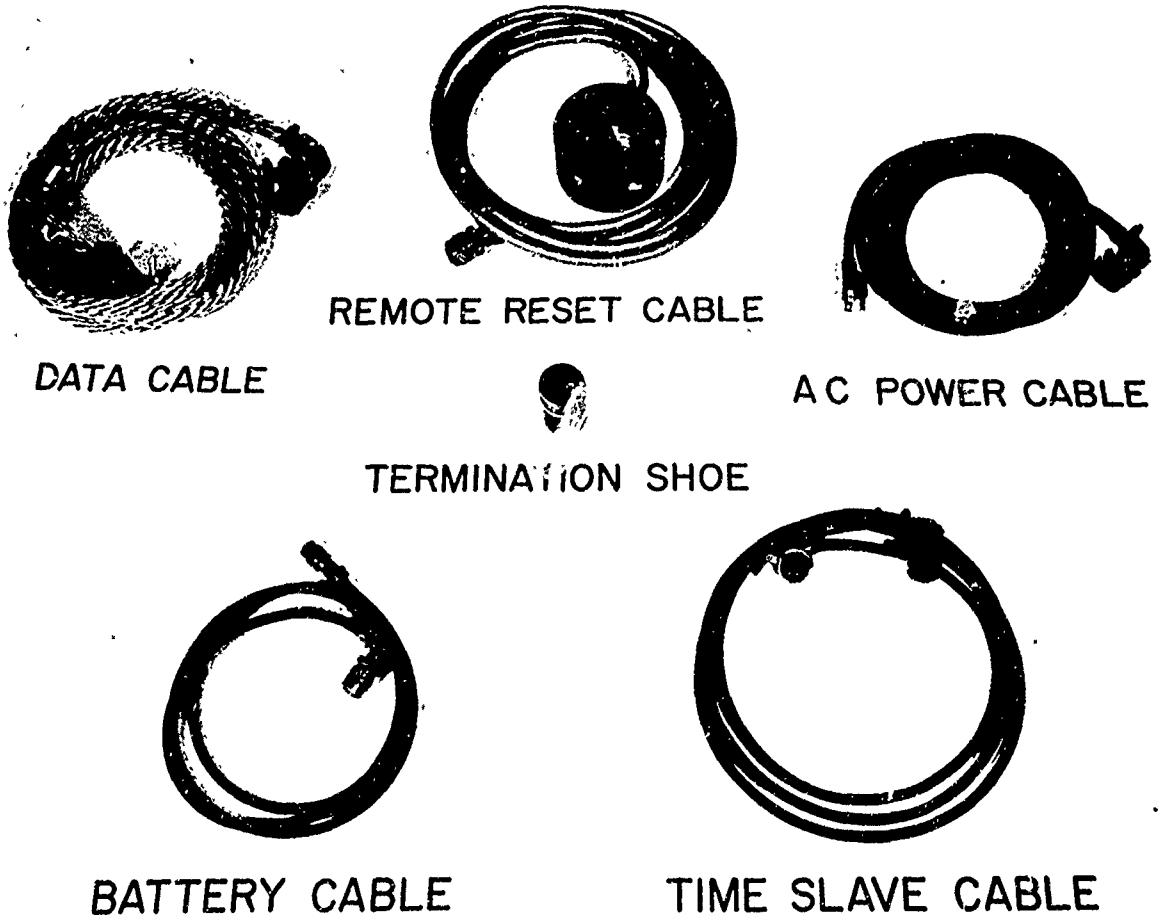


Fig. 2.9. Termination shoe and operating cables.

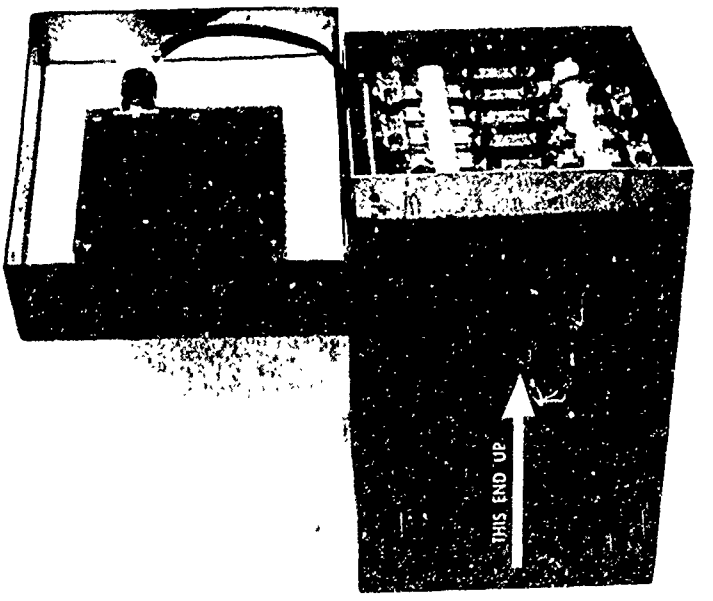


Fig. 2.10. Battery box.

CHAPTER 3. INITIAL SETUP AND ROUTINE MAINTENANCE PROCEDURES

3-1 Initial Setup

3-1.1 Unpacking. Unpack all equipment from its shipping crates and inspect for damage. If damage is absent or slight, proceed with the checkout. If damage is severe (deep dents in the case, broken or badly deformed metal extending into the various modules), repack and return the equipment.

3-1.2 Panel Inspection. Remove the front and rear panels from the main TDS package. Inspect the front panel for broken push button and power switches, fragments of NIXIE tubes within the windows, and dents or deformation. Test tightness of each of the seven panels by wiggling it back and forth. Inspect the rear panel for broken or damaged connectors or deformation. Also, check to see that all the rear-panel retaining screws are in place and are not broken.

3-1.3 Interior Damage Inspection. If the front panels are loose or if the case has been dented or slightly damaged, remove the rear connector panel by loosening the cam-lock screws. Inspect the wiring for broken ends; inspect the large interior connection panel (Board 37), the lightning arresters, and the under-overvoltage protection card for damage. If any module is loose, tighten the large knurled screw on the back of the module until the panel is firmly against the rubber gasket on the front of the TDS. Do not use excessive force. After inspecting the interior, replace the rear panel carefully so as not to pinch any wires between it and the rubber gasket. Replace and tighten all cam-lock screws.

3-1.4 Battery Inspection. Remove the top of the battery box and inspect as follows:

A. Check for spilled and dried electrolyte around the top of the battery, particularly in the vent screw holes and over the top battery surface. Spilled and dried electrolyte has a white or grayish-white powdery appearance. Remove the dried electrolyte and fill the battery cells per Sec. 3-1.7 using the potassium hydroxide solution.

B. The battery is shipped with round-headed vent seal screws in the filler plugs to prevent electrolyte spillage during shipping. Remove and replace these screws with the square-top vent plugs provided with the battery to allow venting of the hydrogen and oxygen released during normal battery charging.

C. Check the battery connector, the wiring from it to the battery, and the wiring from the battery and battery connector to the temperature-compensated regulator connector; be sure that its connector is firmly seated in the temperature-compensated regulator package.

D. Check the battery box for dents and the battery case for breakage. Replace the battery box top.

3-1.5 Cable Inspection. Inspect all cables for damaged wires or bent connectors. Connect the ac power cable and the battery cable to the back panel of the TDS. Plug the power cable into the 115-V line outlet. Before turning on any power, make sure that all TDM power switches are off.

3-1.6 PSM Inspection. Turn on the PSM power switch. Observe (a) the pilot lamp for a red glow indicating power, and (b) the ammeter. With the battery connected, the ammeter should register 2 to 3 A, and this rate of charge should be maintained for a few (up to 15) hours.

3-1.7 Initial Electrolyte Check. After about two weeks of operation with power connected continuously to the PSM, check the electrolyte level of all battery cells. If there was no evidence of electrolyte spillage when the battery was inspected (Sec. 3-1.4), add enough distilled water to bring the level of the electrolyte to between 1/4 and 1/2 in. above the bottom of the wells visible when the battery plugs are removed. If electrolyte was spilled, fill the batteries as above with the potassium hydroxide electrolyte supplied with the TDS.

3-1.8 TDM Check. Perform this check after PSM inspection (Sec. 3-1.6) and after the battery has been on charge for about 30 min. Turn on the TDM-1 power switch and set the test code generator (Portable Test Azimuth Generator) module switch to Module 1. Refer to Table 3.1 and load the 10 test azimuths as indicated. After each step in the table, press the transmit-single button on the TCG once. Observe the shots lamps on the TDM module. After pressing the button, the No. 1 shots lamp should start blinking. Depress read button on the TDM and note the azimuth and channel ID. This should be the same as the value just read in. Also note the time-tag reading on the TDM. These numbers should change from one reading to another. Repeat this procedure for all steps in Table 3.1. Then repeat Steps 1 through 7 in the table but do not press the read button between steps. Be careful to push the transmit button only once per step. Each time the transmit-single button is pushed, the number of shots in storage should increase by one. After the sixth step, the No. 6 shots lamp should be lit and blinking and should continue to do so during the seventh transmission. Press the read button and verify

that the azimuth reading is the same as the test azimuth input in Step 1; repeat this verification for Steps 2 through 6 in the table. Push the button a seventh time and observe that no numbers are lit. The seventh step should not be read into the TDM. Turn off TDM-1 and repeat the above procedures for TDMs 2, 3, and 4.

3-1.9 Alarm Check. Turn on all TDM power switches and load each TDM with any azimuth. Note that the module selector switch on the TCG will have to be set separately for each TDM. Turn up the alarm volume on the TTM and check the alarm for operation. Clear all four TDMs by depressing the four read buttons; the alarm should stop.

3-1.10 Battery Power Check. Turn off the PSM and allow the battery only to run the system. Repeat the procedures given in Sec. 3-1.8 on TDM-1 only to check the battery supply.

3-1.11 Long-Line and Antenna Check. Connect the long lines or receiver antennas to the various TDMs to be used in field operations. Refer to LA-4444-TM, Vols. II and VII, for antenna orientation and installation, for long-line installation and various combinations allowed, for lightning arrester connections, and for ID settings. Send an assistant into the field to generate azimuths with the azimuth processor as described in LA-4444-TM, Vol. II, and check for correct operation. Note that each TDM can be connected to a long line only, a receiver only, or to both. Be sure not to duplicate channel ID numbers for any azimuth processors connecting into a given TDM.

3-1.12 Power Saving. Each TDM has power-saving circuits that turn off the power to most TDM circuits when no azimuth signal is loaded in the TDM. If the PSM or line voltage fails, keep all TDM modules cleared of azimuths (by reading out azimuths as soon as practical after they are received) to reduce battery drain. Turn off any unused TDMs during battery operation.

3-1.13 External Device Checks.

A. Another TDS. Check out another TDS by the procedure outlined above. Connect the time-slave cable. Only one time-slave cable should be connected between two TDSs. The cable connected to the time-master connector of a TDS will use the time clock in that TDS as the master time clock. The time clock in the other TDS will then be suppressed and slaved to the first time clock. To synchronize the two time clocks, push the time clock button on the TTM. To check the time clock synchronization, load data into a TDM on both TDSs simultaneously. The time tag on the two TDMs should agree to within ~ 1/2 sec.

B. Printer. Connect a data cable from the printer control chassis to either one of the display system data connectors and place a termination shoe on the other. If two TDSs are to be connected to the printer, connect a data cable from the second display system data connector on the TDS that is connected to the printer to either display system data connector on the other TDS and place a termination shoe on the remaining connector. Set the time on the printer control chassis and press the time clock button on the TTM to set the one-day time clock in the printer control chassis. Check the operation of the printer by depressing the transmit-single button on the TCG module and observe the azimuths read out on the printer. Proceed through all 10 steps in Table 3.1, and observe the values that are printed out. To check the module ID at the printer, repeat the steps for TDMs 1 through 4 on the TDS and observe the corresponding module ID on the printer. For further operations, refer to LA-4444-TM, Vol. IV.

TABLE 3.1. AZIMUTH LOADING

Step	TCG Setting: Channel ID	TCG Setting: Test Azimuth
1	0	0000
2	1	1110
3	2	2220
4	3	3330
5	4	4440
6	5	5555
7	6	6665
8	7	6775
9	7	6885
10	7	6996

C. Computer. Connect the display system data cables as indicated above in B. For further information refer to LA-4444-TM, Vol. VI.

3-2 Routine Maintenance

3-2.1 Routine Electrolyte Check. Check the battery electrolyte level each month as outlined in Sec. 3-1.7. *Never check the electrolyte level unless the battery is fully charged, because the electrolyte level drops as the battery discharges. If the battery is filled when discharged it will overflow when fully charged.*

3-2.2 Operation of Battery and PSM. After checking the battery electrolyte level, turn off the PSM, load one shot in each TDM, and wait for 30 min. Turn on the PSM, reset the TDM, and observe the current on the ammeter of the TTM. It should read 2 to 3 A for ~ 5 to 10 min.

3-2.3 TDM Operation. Check the TDM according to the steps outlined in Secs. 3-1.8 and 3-1.9.

3-2.4 Changing Batteries in Azimuth Processors. Whenever batteries are changed in the APs, generate a few azimuths and check the TDS to ensure that the azimuths are being received with the correct channel ID. If an AP long line or field wire is broken, check the error lights when the wire is reconnected to ensure that the light is not glowing continuously (indicating that the field wires are reversed), and check the AP by generating azimuths and reading them out on the TDS.

3-2.5 Time-Tag Operation. In Secs. 3-2.2, 3-2.3, and 3-2.4 above, check the time-tag numbers each time a piece of data is read out to see that these numbers change and appear to give the correct time when they are read out. To check that the time counter is counting correctly and in the proper sequence, load a test azimuth from the TCG every 1, 2, 5, or 10 sec to check the operation of the time-tag circuits.

3-2.6 Channel ID Code Check. Check occasionally during operation to see that all APs are sending data by observing that the AP channel ID code corresponding to that AP is received. If trouble is experienced with some stations, check the TDM according to Secs. 3-1.8 and 3-1.9. If no trouble is found, the difficulty is probably in the AP or in the transmitter-receiver combination. Refer to LA-4444-TM, Vols II and VII, for procedures to correct malfunctions of the transmitter-receiver data link or the AP.

3-2.7 Wires and Lines. Occasionally check all wires, connectors, lightning arresters, field lines, etc., for damage. Keep the area neat and clean. Be sure that the battery is always firmly placed and standing upright to prevent spillage of electrolyte. Do not expose the equipment unnecessarily to very hot or very cold temperatures; in particular, avoid placing olive drab-painted equipment in direct sunlight in a hot climate.

CHAPTER 4. MALFUNCTIONS AND REPAIR (BOARD REPLACEMENT)

4-1 Introduction

This section describes simple maintenance procedures not requiring detailed knowledge of the TDS electronic circuits. No testing of circuits on individual printed circuit boards (cards) is required. Board replacement is the primary repair procedure. *Handle boards carefully and do not drop or scrape boards against each other.*

First establish the presence or absence of system power (see Sec. 4-2).

If system power is present, attempt to load test azimuths with the TCG and note any malfunctions. If all TDMs exhibit an identical or similar malfunction, the trouble is probably either in the TCG (Sec. 4-4) or in the TTM (Sec. 4-3). If only one TDM is causing trouble, proceed to Sec. 4-5 and attempt to repair that module. If an azimuth cannot be satisfactorily loaded in any TDM, try to load remotely with an AP.

4-2 Main System Power Supply Module

4-2.1 Procedures Prior to Checking. Remove the rear connector panel from the PSM and the plastic cover from Board 37. Check the line voltage on Pins J and K of the PSM connector. For proper operation of the power supply, the line voltage must be greater than 75 V but less than 135 V.

4-2.2 Checking Procedures. If the ac line voltage is correct, follow the steps in Table 4.1 to isolate the trouble.

4-3 Time Tag Module

To check the TTM, follow the steps in Table 4.2.

4-4 Test Code Generator Module

To check the TCG, follow the steps in Table 4.3.

4-5 Telemetry Display Module

Troubles associated with various boards of the TDM can usually be corrected by replacing the board causing the malfunction.

4-5.1 Board 21. The following troubles may be caused by malfunctions in Board 21.

A. With the TDM power switch on and the power supply module working correctly, there is either no voltage, or a voltage less than 5 V, or a voltage greater than 5.5 V measured at Pin Y of Board 37 for the module being examined.

B. Some NIXIE tubes–particularly the channel ID

TABLE 4.1. POWER SUPPLY MODULE CHECK PROCEDURES

	Symptom		Check
A.	Power lamp does not light when the switch is turned on.	1.	Check fuse on front panel. Use the ohmmeter on the X1 scale if there is any doubt whether current is present. Disconnect power before checking the fuse.
		2.	Check voltage on power lamp. If voltage is present, replace lamp.
		3.	Check power switch to be sure it operates.
		4.	Examine for broken or burned-out wires.
B.	Power lamp lights, but power supply output is less than 11 V or is zero with the battery removed.	1.	Check the voltage across the large 6000-μF filter capacitors. Voltage must be between 20 and 50 V.
		2.	Check the current on the front-panel meter. If it is greater than 2 A, there is a short circuit or some circuits are drawing excessive current. If the meter indicates less than 2 A, replace Board 30-2.
		3.	Turn off all TDMs. If the output increases, the trouble is probably due to a defective module. Turn on the TDMs one at a time. Note if one behaves differently than the rest.
		4.	Replace Boards 30-1 and 30-2.
C.	Batt Low lamp glows continuously.	1.	Check battery voltage at Pins A and B of the PSC connector (Board 37). If this voltage is less than 11 V, the battery is discharged or defective.
		2.	If the voltage is greater than 11 V, replace Board 30-4.

TABLE 4.2. TIME TAG MODULE CHECK PROCEDURES

	Symptom		Check
A.	Time tag operates incorrectly and alarm does not sound.	1.	Check the 5-V power for the module on Pin Y on the TTM connector (Board 37). If voltage is zero or less than 5 V and the voltage on Pin W of the TTM connector is greater than 10 V, replace Board 30-3. If this does not solve the problem, Board 26 or Board 31 is defective, or there is a shorted or broken wire in the module.
B.	Alarm does not sound when it should, but time tag operates.	1.	Measure the voltage on Pin EE of the TTM connector. It should be at least 4 V for the alarm to function. If required voltage is present, replace Board 31. If trouble persists, the alarm or the wiring is faulty.
C.	Alarm sounds, but time tag does not.	1.	Check the voltage at Pins B, C, D, F, G, H, J, K, M, P, and Q on the TDM connectors. Pin Q carries the 0.1-sec time code, and Pin B carries the 40-sec time code. The voltage should oscillate between 0.1 and about 5 V. If these voltages are present, the time tag module is not at fault. If these voltages are not present, replace Board 26.

TABLE 4.3. TEST CODE GENERATOR MODULE CHECK PROCEDURE

Symptom	Check
A. **Transmit** lamp does not light when either the **single** or **repeat** button is pushed, or the lamp glows for less than 0.5 sec when the **single** button is pushed.	1. Replace Board 24. If trouble persists, the wiring is defective.
B. **Transmit** lamp lights, but test code does not load.	1. Replace Board 6. 2. Replace Board 24.

NIXIE–will not extinguish when the **read** button is depressed and released.

C. More than one number lights at one time on the ID NIXIE.

D. The azimuth NIXIES will not light when data are stored and the **read** button is depressed. (This malfunction could also be caused by Board 1A.)

E. Data load correctly and can be read out correctly, but the **shots** lamps will not flash.

F. With another module loaded and no data in the module being examined, all zeros light when the **read** button is depressed.

G. The receiver has no power (measure on **Pin 1** of Board 28).

H. The **read** button will not reset data. (Could also be caused by malfunctions in Boards 23, 31, or 29C.)

I. The **alarm** does not sound when a shot is stored (as indicated by **shots** lamps.

4-5.2 Board 20. The following troubles may be caused by malfunctions in Board 20.

A. Shots load erratically, usually accompanied by the **error** lamp flashing. (Could also be caused by noise on the field wire if connected, by malfunction of the receiver, by weak rf signal, or by radio interference.)

B. Shot will load in automatic mode, but not in manual mode; or after loading one shot in automatic mode, the remaining five shots will load normally when switching to manual mode if the original shot remains stored after switching to manual mode.

C. No shots will load. (Could also be caused by malfunctions in Boards 21, 23, 29C, and 31, or by the receiver.)

D. Instead of loading shots, the **error** lamp flashes every time loading is attempted, particularly when shots are fed in with the TCG. (Could also be caused by faulty receiver or by malfunctions in Board 21.)

4-5.3 Board 23. The following troubles may be caused by malfunctions in Board 23.

A. More than one **shots** lamp flashes at one time.

B. One **shots** lamp does not light even though the module loads and resets correctly. (Could also be a defective lamp.)

C. The module loads, but either will not reset or will reset only partially.

D. The data load correctly according to the lamps, but when the data are read out all zeros appear or numbers (usually 7 and 9) are superimposed on some of the NIXIE tubes. (Could also be caused by malfunctions in Boards 29A, 29B, 29C, 29D, 21, 1A, or 1B.)

E. The azimuth and ID data load correctly, but the time-tag loads either zeros only, or load numbers (usually 7 and 9) are superimposed on the time-tag NIXIES. (Could also be caused by malfunctions in Board 22.)

4-5.4 Board 29. The following troubles may be caused by malfunctions in Board 29.

A. Board 29A: Incorrect reading of some numbers in the azimuth thousands and hundreds positions. (Could also be caused by malfunctions in Board 1A or by a defective NIXIE tube.)

B. Board 29B: Incorrect reading of some numbers in the azimuth tens or units position, or they cause failure to read either ID 4, 5, 6, and 7 or ID 1, 2, 3, and 4 on the ID NIXIE. (Could also be caused by malfunctions in Boards 1A or 21, or by a defective NIXIE tube.)

C. Board 29C: Failure to load shots in storage, incorrect readout of the ID NIXIE, or incorrect readout of the time-tag tenths or units positions. (Could also be caused by malfunctions in Boards 1B, 21, or 22 or by a defective NIXIE tube.)

D. Board 29D: Failure to read the time-tag tens, units, or tenths positions. (Could also be caused by malfunctions in Boards 1B, or 22, or by a defective NIXIE tube.)

E. Boards 29A, B, C, or D: Faults as listed for Board 23 (Sec. 4-5.3.D).

4-5.5 Board 1. The following troubles may be caused by malfunctions in Board 1.

A. Board 1A: Any of the azimuth NIXIES fail to light.

B. Board 1A: Double numbers light on the azimuth NIXIES or any number (other than 7 in the thousands position) may be blank.

C. Board 1B: Trouble in time-tag NIXIES as listed for Board 1A above for the azimuth NIXIES.

4-5.6 Board 31. The following troubles may be caused by malfunctions in Board 31.

A. Time-tag NIXIE tubes light in automatic mode, or fail to light in manual mode. (Could also be caused by malfunctions in Board 1B.)

B. If six shots are stored and the operating mode is changed from manual to automatic, all shots are not cleared from storage. (Could also be caused by malfunctions in Board 23 or Board 21.)

C. The time-tag decimal point does not extinguish in automatic mode, or does not light in manual mode.

D. In automatic mode, the correct number is shown on the NIXIES, but an attached printer or computer does not indicate the correct number.

CHAPTER 5. PRINCIPLES OF TDS OPERATION

5-1 Information Transmitted

5-1.1 Serialization of Data. The data generated in the AP are in the form of parallel binary coded decimal (BCD) information. To transmit this information, the data must be serialized by Board 6 in the AP, which takes in the BCD azimuth and channel ID data and reads the data out serially. These serialized data are then transmitted (1) from a radio transmitter in the AP to a receiver in a TDS, or (2) directly over a long line or field wire to the TDS.

5-1.2 Transmission of Code. The information generated by the AP is in the form of an 18-bit serial code. The transmission of the code is preceded by a waiting period of ~ 11 to 12 msec. Following the waiting period, the code is transmitted:

A *"one"* is indicated by an 80-μsec pulse of 5-V magnitude. Both leading and trailing edges of the pulse have a linear ramp of ~ 5-μsec duration.

A *"zero"* is indicated by a 40-μsec pulse. This pulse also has a magnitude of 5 V, with a 5-μsec rise time on the leading edge and a 5-μsec fall time on the trailing edge.

The spacing, or period, of the pulses is 160 μsec. All pulses start from a base of 0 V dc. The 5-μsec linear ramps on the leading and trailing edges of the pulses prevent rapid transients from appearing at the transmitter or long line, and reduce the amount of current required to drive a long line. (Lines of 2 to 3 km may be driven by the AP.)

5-1.3 Order of Transmittal. The pulses representing ones and zeros are transmitted in the following order:

A. The first pulse transmitted is always a *"one"* and is called the *"initial one."* This pulse is included for convenience in decoding and storing the data in a TDS.

B. The second, third, and fourth pulses are the 4, 2, and 1, respectively, of the channel ID. This code identifies the AP that is generating data if two or more APs are on the same frequency or are connected together by the daisy-chain system (described in LA-4444-TM, Vol. II).

C. The fifth, sixth, and seventh pulses represent the 4, 2, and 1, respectively, of the azimuth thousands data.

D. The eighth, ninth, 10th, and 11th pulses are the 8, 4, 2, and 1, respectively, of the azimuth hundreds data.

E. The 12th, 13th, 14th, and 15th pulses are the 8, 4, 2, and 1, respectively, of the azimuth tens BCD data.

F. The 16th pulse represents the azimuth units data. A *"zero"* corresponds to a zero, and a *"one"* corresponds to a *"five"* in the last azimuth position.

G. The 17th and 18th pulses are the so-called parity bits. Parity is obtained by counting all the preceding ones in the transmitted code in a two-bit binary counter. These bits are attached to check parity or to check the *"one"*-count when the data are received to see whether the count agrees with that at the transmitting end.

5-1.4 Signal Characteristics. The voltage output from the AP is a constant 5-V signal until an azimuth and its accompanying ID are about to be transmitted. The 5-V signal then drops to zero with a 5-μsec ramp, which indicates the beginning of the waiting period. After the waiting period and the transmission of the 18th pulse in the code, the voltage from the AP returns to +5 V, with a 5-μsec rise time. The return to 5 V indicates to the transmitter that the code has been transmitted, and ~ 300 μsec after return to the 5-V steady level the transmitter will turn off. The waiting period of 11 to 12 msec allows time for the transmitter to turn on and come up to power; for the receiver AGC circuits to respond; and, in the event of a telemetry display module with no data stored, for the power turn-on circuits to turn the voltage on and for all reset circuits to complete their cycle.

5-2 General Description and Organization of Various Components

Individual board diagrams (Chapter 7) and connection diagrams for the various modules (Chapter 8) are required for understanding this chapter.

The TDS interconnections list (also in Chapter 8) specifies all module interconnections on Board 37, the large rear-panel board.

5-3 The Telemetry Display Module

5-3.1 Loading of Data. If the transmitted code is conveyed over field wires or long lines, it is fed directly to Board 20, which is the serial-to-parallel converter card in the TDM. If sent by the transmitter, the code is received and conveyed to the receiver in the TDM, which couples the output directly to Board 20. When no pulses are being transmitted, the receiver output is in the form of full-scale white noise, and these serial-to-parallel cards (Board 20) must be turned off so that the white-noise pulses will not be interpreted as data. The output of the input amplifier on Board 20 is coupled to Transistor 4, which is a noise switch. In the presence of noise, Transistor 4 conducts current and charges the 0.022-μF capacitor and, through Transistors 5 and 7, keeps the receiver output clamped to +5 V so that the Schmidt trigger, which consists of Transistors 8, 9, and 10, will not fire. When transmitter power comes on, indicating the beginning of a transmission period, the output of the receiver quiets down, the noise from the input amplifier ceases and the Transistor 4 turns off, allowing the noise switch (through Transistors 5 and 7) to turn off and the following data signal to be coupled from the input amplifier to the Schmidt trigger.

A long-line signal to Pin A32 of Board 20 causes Transistor 27 to clamp the receiver output to +5 V, thereby eliminating the receiver noise source and allowing the noise switch to turn on again. The output of the Schmidt trigger (Transistor 10 collector) is reconstructed data of the same form as the output data from the AP except that the rise and fall times of this signal are much shorter than 5 μsec. The reconstructed data appear at Pin B27 of Board 20.

Transistors 11, 12, and 13 form a 60-μsec single shot to distinguish between *"ones,"* which are 80-μsec long, and *"zeros,"* which are 40-μsec long. At the beginning of a pulse, i.e., at the positive edge of a reconstructed data pulse from Transistor 10, the 60-μsec single shot is fired. After 60 μsec, Transistor 14 generates a differentiated shift pulse of ~ 1- to 2-μsec duration. This pulse causes data to be shifted into the input of the 18-bit shift register. The data input to the shift register are the reconstructed data appearing on Pin B27. If the data bit is a *"one,"* then at 60 μsec the data will still be high at the input to the shift register (Integrated Circuits 1, 2, 3, 4, and 9) and a *"one"* will be shifted into the shift register. If the reconstructed data are *"zeros,"* they will be low at 60 μsec and will be shifted-in as a *"zero."*

Transistors 15, 16, and 26 cause a pulse to be generated every time a bit is a *"one"* for the 1st through 16th pulses in the transmitted data chain. These pulses appear on Pin A27 and are fed to the two-bit parity counter (Integrated Circuit 6).

Transistors 17, 18, and 19 form a single shot that generates a pulse of ~ 4- to 4½-msec duration. The single shot output is actively differentiated by Transistor 20 to form an end-of-data pulse at Pin A28. Transistors 17, 18, and 19 limit the time available to load a complete code into Board 20. If, for example, a false-noise pulse is generated, the shift register will be loaded with only one bit and locked unless the shift register is cleared after a waiting period. In addition, Transistors 17, 18, and 19 allow a waiting period of ~ 1 to 1½ msec so that the parity comparator (Integrated Circuits 5 and 7) can establish its output before the data are loaded into the rest of the TDM circuits.

If the parity as counted on Board 10 agrees with the parity as generated at the transmitting AP, the output of Integrated Circuit 7 will be high, indicating that the two parity counts compare. If, in addition, all 18 bits have been loaded, indicated by the initial *"one"* appearing at Pin 12 of Integrated Circuit 9, then the end-of-data pulse will generate a Load 1 on Pin A31, indicating that a correct signal has been loaded. The Load-1 pulse at Pin

A31 loads the data stored in the shift register. If the parity does not agree or if all 18 bits of the shift register are not loaded, then an error pulse generated through Pin 8 of Integrated Circuit 8 appears at Pin B30. In the event of an error, the Load-1 signal is not generated; instead, the error signal feeds back to Integrated Circuit 12 at Pin 14 to reset the shift register. By this means, erroneous signals are not loaded but are automatically reset and the data are ignored.

5-3.2 Storing of Data. If fewer than five shots are stored in the TDM, the Load-1 pulse to Pin 3 of Board 23 generates a reset-shift pulse at Pin 12 of Board 23 and connects the pulse back to Pin B24 of Board 20. Thus, the load pulse is coupled back to automatically reset Board 20. The timing of the reset single shot (Integrated Circuit 12, Output 3; Integrated Circuit 8, Output 5; and Transistors 24 and 25) is such that Board 20 will not be reset until ~6 μsec after the data are loaded on Board 20. If five shots are already stored in the TDM, the automatic reset on Board 23 is inhibited, preventing Board 20 from resetting so that Board 20 will not respond to any further input signals. The output labeled *"One Full"* on Board 20 through the 100-Ω resistor to the base of Resistor 10 will lock the output of the Schmidt trigger (collector of Transistor 10) in the low state and prevent any further loading until Board 20 has reset.

Data are stored in the TDM in Boards 20, 21, 22, 29A, 29B, 29C, 29D, 1A, and 1B. Storage sequencing is controlled by Board 23, which is the stacked storage-control board. Board 20 (the serial-to-parallel converter) and the **read** button generate the pulses that initiate storage and sequencing on Board 23. Each piece of data, i.e., the azimuth, its channel ID, and the accompanying time tag, is referred to as a data word. Each data word has three channel-ID bits, 12 azimuth bits, and 11 time-tag bits for a total of 26 bits. Word 1 is stored in Board 20 for the azimuth and ID, and in Board 22 for the time tag. Boards 29A, B, C, and D store Words 2, 3, 4, and 5. Word 6, i.e., the data that will be displayed when the **read** button is depressed, is stored in Boards 1A (azimuth), 1B (time tag), and 21 (channel ID).

Boards 29A, B, C, and D have 28 set-reset (RS) flip-flops each. There are seven strings of four flip-flops, each having the output of one flip-flop connected to the input of the succeeding flip-flop. If a bit is loaded into the first flip-flop by allowing the load input to go high momentarily, the bit is stored in that (first) flip-flop; if the next load line is allowed to go high, the bit will be transferred to the second flip-flop; and, similarly to the third or fourth flip-flop through the four stages. With proper operation of the load and reset lines, these flip-flops then can pass data from one stage to another. Four Boards 29 are capable of storing 28 bits in any word. Twenty-six bits are used for the channel ID, the time tag, and the azimuth, one bit is used for sequencing control, and one bit is not used. Boards 29 can, therefore, store four words, i.e., Words 2, 3, 4, and 5.

Assume now that no words are stored in the TDM. When a word is received and stored in Board 20, a Load-1 pulse will be generated when the end-of-data single-shot period ends. This Load-1 pulse, conveyed to Board 23, causes Words 1, 2, 3, 4, 5, and 6 to load the azimuth, the channel ID, and the time tag (the time tag is received from the time-tag module and is loaded at the time of the Load-1 pulse into Board 22). The Load-1 pulse will be coupled back through Integrated Circuits 8 and 9 on Board 23 to cause a reset at Pin B24 of Board 20. At the end of this reset pulse, a *"Reset One"* pulse is generated at Pin A29. Board 23 will respond to the Load-1 pulse by loading all six words into storage, but the Reset-1 pulse on Pin 5 of this Board will reset only five words. For the 10-μsec period between the beginning of the Load-1 pulse and the beginning of the Reset-1 pulse, all six words in storage are loaded with the same data. When the Reset-1 pulse occurs, only five words are reset so that the word received is now in Word 6 along with its time-tag and channel-ID information. If the **read** button is depressed, this word will be displayed.

It is assumed that Words 1, 2, 3, 4, 5, and 6 were all empty; therefore, the signals at Pins 31, 26, 22, 18, and 14 were low at the beginning of this process and the signal at Pin 9 was high. Circuit 5 on Board 23 is a Miller integrator. The control string of flip-flops on Boards 29 and the Word-6 flip-flop on Board 21 were loaded simultaneously from the *"One Full"* (Pin A12 of Board 20) line and contained all *"ones"* in all six words. Because Word 6 could not be reset, the control flip-flop for Word 6 is left (at the end of the first loading) with a *"one"* in the Word-6 control flip-flop and with a *"zero"* in all the others. When Circuit 5 (Board 23) is presented with a high input at Pin 31 on Board 23, the output of the 2N3904 transistor falls below the level of the integrated circuit gates at ~ 20 μsec. Therefore, during this process, none of the outputs of Circuit 5 drops below the *"zero"*-gate threshold of the integrated circuits during the interval between the Load-1 and the Reset-1 pulses. Consequently, none of these outputs were low before the Reset-1 pulse occurred. Because Word 6 could not be reset by the Reset-1 signal, its output will continue to fall after the Reset-1 pulse and will, therefore, block the Load Word-6 and the Reset Word-5 lines on Board 23 by means of Integrated Circuit 7, Pin 3, for the Load Word-6 pulse and by means of Integrated Circuit 5, Pin 5, for the Reset Word-5 pulse. If the **read** button is not depressed, one word will remain stored in Word 6 of the storage registers and all other words will remain reset.

When a second signal is loaded into Board 20, the Load-1 pulse will load this word into Words 1, 2, 3, 4, and 5, and the Reset-1 pulse will reset Words 1, 2, 3, and 4. In this manner, the second word will be stored in Word 5, and the second Miller integrator circuit (Circuit 5 on Board 23) will continue to fall and will cut off the loading of Word 5 and the resetting of Word 4. When the third word is loaded in Board 20, Words 1, 2, 3, and 4 are loaded, and Words 1, 2, and 3 are reset by the Reset-1

pulse. The fourth word will load Words 1, 2, and 3, and the Reset-1 pulse will reset Words 1 and 2. The fifth word will load Words 1 and 2 but will reset only Word 1.

At this point, the *"Word-2 Full"* control flip-flop (Pin 14 of Board 23) will cause the output of the corresponding Miller integrator to cut off the automatic reset to Board 20 (through Pin 12 of Integrated Circuit 8) and also the loading of Word 2 through the line to Pin 9 of Integrated Circuit 8. When the sixth word arrives, it will load Board 20, and the Load-1 pulse will be translated into a Load Word-1 at Pin 4 of Board 23 which will load the time-tag data into Board 22. The Reset-1 pulse will not occur at this time because the reset shift is cut off (Pin 12 of Board 23) and prevents Board 20 from resetting. If Board 20 does not reset, the Reset-1 pulse is not generated and Board 22 is not reset. At this point, any further loading of data is inhibited through the 100-kΩ resistor connected to the base of Transistor 10 on Board 20.

5-3.3 Display of Data. If the **read** button is now pushed, the data will be displayed on the NIXIE tubes. When the **read** button is released, a pulse is generated at Pin 28 of Board 23. This pulse is applied directly to Pin 13 of Integrated Circuit 7 and generates a Load Word-6 pulse to Boards 1A, 1B, and 21. A 47-pF capacitor couples this **read** button reset signal to Pin 9 of Integrated Circuit 7, generating simultaneously a Load Word-6 and a Reset Word-6 pulse to Word 6 of storage. The 47-pF capacitor and differentiating networks cause the Reset Word-6 pulse to vanish before the Load Word-6 does, resulting in the loading of Word 5 into Word 6. The **read** button reset signal is ~4 μsec long. This signal (through Circuit 3 of Board 23 which is a 20-μsec single-shot circuit) causes a delay of 20 μsec before the pulse output is applied to the load and resets gates for Word 5. Again, the reset pulse is shorter than the load pulse, and, therefore, Word 4 is loaded into Word 5.

This process continues through the remaining Circuits 3 with the result that Word 5 is loaded into Word 6, Word 4 into Word 5, Word 3 into Word 4, and Word 2 is loaded into Word 3. Through the action of the last Circuit 3 (feeding into the 220-pF capacitor in a differentiating network consisting of the capacitor, the 100-kΩ resistor, and five 1N4154 diodes), a 4-μsec pulse is coupled into Pin 9 of Integrated Circuit 9 and generates a reset shift to Board 20. This signal resets Board 20 through the action of the *"Reset Single Shot"* on Board 20. When Board 20 is reset, a Reset-1 pulse is generated which, through Pin 8 of Board 23, resets Board 22. The result of this action is the loading of all zeros into Boards 20 and 22, and the shifting of all words toward the right (towards the NIXIE-tube display boards) by one position.

If the **read** button is depressed again and then released, all words will be moved toward the right by one position, and Words 1 and 2 will be left with no data. This process can continue until all six words are cleared, which was the initial condition. During clearing of the words with the **read** button, words can be loaded into Board 20 to fill up the last empty position just as they did when all data were loaded initially.

The data pilot lamps that indicate shots in storage are operated by the circuits indicated in the square boxes numbered 1, 2, and 3 (on Board 23). These circuits are a two-transistor AND circuit. If, for example, Word 6 is full (Pin 31 of Board 23) and Word 5 is empty (Pin 26 of Board 23), Input 1 (of the two-transistor AND circuit) will be high; and, because Word 5 Full is low, the output of Circuit 5 (another integrator) will be high, causing Input 2 of the transistor AND circuit to be high. This will cause current to flow from the collector of the second transistor and will light the No. 1 **shots** lamp. The positive ends of all six **shots** lamps are tied to the data-lamp flasher on Board 21. The data-lamp flasher alternately pulls the plus side of the lamps up to ~3.5 V and then allows the plus side to return to ground. With the No. 1 **shots** lamp (minus side) connected to ground, this lamp will flash.

When Word 5 is full, Pin 26 of Board 23 will be high and the output of the Miller integrator will diminish until the No. 1 **shots** lamp is cut off. The No. 2 **shots** lamp will then light. This process continues until the No. 5 **shots** lamp is lit. When Word 1 is filled, resulting in *"Word 1 Empty"* going low (Pin 9 of Board 23), then the No. 5 **shots** lamp will be cut off and the No. 6 **shots** lamp will light through the two-transistor AND circuit driver.

Board 22, which stores Word 1 of the time-tag information, is required because there is no other way to store the time-tag information. Board 22 consists of 12 RS flip-flops with 12 input gates for setting the flip-flops. Only 11 of these 12 flip-flops are used because there are only 11 bits of time-tag information. Board 22 is controlled by Load Word-1 and Reset Word-1 outputs from Board 23.

5-3.4 Power Supply Circuits. Board 21 contains the main TDM power supply, a receiver power supply, a NIXIE-tube voltage regulator, a 5-V power switch, a **read** button circuit, the error-lamp driver, the data-lamp flasher, two general-purpose inverters, the Word-6 control flip-flop, and the Word-6 channel ID storage flip-flops and its NIXIE decoder.

The main power supply is a switching regulator and will take input voltages from 8 to 20 V which it reduces and regulates to 5.1 V for the system power. At 12-V input to the main regulator, the input current is about half the output current, resulting in high-efficiency conversion of power from 12 to 5 V. The 2N3741 switch transistor (Transistor 1), larger than necessary for normal operation, will withstand a short circuit on the 5.1-V regulated bus without destroying the transistor. The 2N1306 transistor (Transistor 2) is connected as a simple diode (the catch diode of the switching regulator). The Zener diode (1N3828A) protects the circuits powered by the regulator if the regulator fails and the voltage tends to go too high. This diode limits the voltage output of the

regulator to ~6 V if the main power supply fails. The 1-mH choke and the 33-pF capacitor form an inductance-capacitance filter for removing the small amount of residual ripple from the regulating action of the switching regulator.

Transistors 39, 40, and 41 form the receiver voltage regulator. Its output may be adjusted by changing the value of the resistor between Pin B30 and the base of Transistor 39; further small changes may be made by adjusting the trim resistor.

The NIXIE regulator operates like the receiver regulator except that a boost transistor (Transistor 38) and a larger-series pass transistor (2N3741) are used because of the higher current requirements. A 2-MΩ resistor (on Board 34, the NIXIE power supply, and the NIXIE tube board) connects to Pin A1 of Board 21 which is the 200-V sense line. The 5-V reference voltage is applied to the base of Transistor 7 through a 47-kΩ resistor. NIXIE power is turned on and off by applying or removing the 5-V reference voltage. The 0.022 μF shown in dotted lines on the NIXIE regulator stabilizes the power supply by preventing the input to the dc-to-dc converter from changing too rapidly.

Transistors 8 and 9 form a switch that applies voltage to the BCD-to-decimal decoders on Board 1. This voltage is also the reference voltage for the NIXIE regulator. Transistor 9 can be turned on and can, therefore, cause the decoder power and the NIXIE power to be applied by (a) depressing either the **read** button (on the front of the TDM), (b) by depressing the **remote reset** button (on the Remote Reset box), or (c) by applying voltage to Pin B4 (the external NIXIE turn-on). The voltage applied to Pin B4 on Board 21 when the TDM is put in automatic mode (described in Sec. 5-3.7 below) is 5 V; otherwise, the voltage on Pin B4 is zero. If the TDM **read** button or the **remote reset** button is depressed, one of the two reset flip-flops on Board 21 will apply voltage to Transistor 9 and the NIXIE tubes are lit. When the **read** or **remote reset** button is released, one of the reset flip-flops (through the 220-pF and two 100-kΩ resistive-capacitive differentiator networks) generates a pulse at Pin A9 of Board 21. This pulse resets the data in Word 6 and moves Word 5 up to Word 6 when the TDM is in the manual display mode.

The power switch on Board 21 consists of Transistors 3, 4, and 5. These transistors remove the 5-V power from most circuits in the TDM when no shots are being stored. They are controlled by the noise-switch on Board 20 that is fed into Pin B32 on Board 21, and by the *"Word-6 Full"* flip-flop, also on Board 21. The power switch is turned on by the noise switch when the receiver quiets or is clamped to +5 V because of the long-line signal being received. The noise-switch signal at Pin B32 causes Transistor 5 to turn on Transistor 4, which turns on Transistor 3 and applies 5 V to all circuits. When the Load-1 signal occurs, indicating that data have been loaded on Board 20, the Word-6 control (the flip-flop on Board 21 whose output is connected to Pin B22) is connected to Pin B33, causing Transistor 4 to remain on as long as any words are stored in the TDM. Note that Word-6 control will always be full if any shots are stored in the TDM.

5-3.5 Reset, Error Lamp, and Word-6 Control Circuits. The **read** or **remote reset** push-button reset signal (Pin A9 of Board 21) is connected to Board 31 (Pin A29). The output of Board 31 (Pin B30) is the reset signal that is allowed to pass through Board 31 in manual display mode but not in automatic display mode. The reset signal from Board 31 is applied to Pin 28 of Board 23, completing the push-button reset circuits. Pins B9 and B10 allow external (**remote reset**) reset signals to be applied to Board 21 (described in Sec. 5-2.2.7).

The error output from Board 20 (Pin B30 of Board 20) is wired to Pin A5 of Board 21. If an error signal is generated, the ~1-sec-long single shot formed by Transistors 14, 15, and 16 will fire and light the **error** lamp through Transistors 12 and 13.

The **error** lamp will also light if the long-line input is connected backwards; Pin A4 will then carry a negative voltage. This negative voltage coupled to the base of Transistor 10 will result in collector current on Transistor 11, subsequently turning on Transistor 13, and thus lighting the **error** lamp. In this case, the **error** lamp will not flash for 1 sec but will stay on continuously as long as the negative voltage is applied to Pin A4, indicating that the long-line signal is being applied backwards to the TDM and that the long lines must be reversed.

The **shots** lamp flasher is a multivibrator formed by Transistors 18 and 20. Transistors 21 and 19 are for other systems using Board 21. Pins B7 and B5 are not connected. Transistors 22 and 23 form a double emitter follower, coupling the output of one side of the multivibrator through Pin B6 of Board 21 to the plus side of the six **shots** lamps.

Because Boards 29A, B, C, and D do not contain Word-6 storage, it is necessary to provide an additional flip-flop on Board 21 (connected by Pins B29 and B22) for control of Word 6 to Board 23. The Word-6 storage for the channel ID and the Word-6 NIXIE decoder are also included on Board 21. This decoder consists of Transistors 26 through 37 and of associated resistors and diodes.

5-3.6 Data Transfer to External Devices. Pin A33 on Board 21 is connected to the mode control. In automatic mode, 5 V is applied to Pin A33 and the power is on continuously. During automatic operation, either a printer or a computer is connected to the TDS. Because these devices require large amounts of power, the power (about 1 W per TDM) consumed by keeping the NIXIE tubes on continuously is minor in comparison. Therefore, the NIXIE tubes are turned on continuously during automatic operation.

When a printer or a computer is used with the TDS, it is necessary to transfer the data arriving at Board 20

either to the printer or to the computer. The printer must also receive the time-tag information, which is transferred automatically from the TTM (covered in Sec. 5-4) to the computer.

The azimuth, the channel ID, and the module ID (generated locally in each module) are transferred to the printer or computer by party-line bus drivers on Board 31. To allow several modules to communicate to the computer simultaneously, it is necessary to use negative true logic. Any bus driver that has a Data 1 at the input will produce a low pulse, which (on a party-line bus) is interpreted as a 1. Thus, all the modules driving the printer or computer can be connected in parallel, with a common resistor to the plus voltage. In this case, the common load resistor is installed by means of a **terminating shoe**, which has 300-Ω resistors from each party-line bus terminal to a +3 V filtered reference. The **terminating shoe** system allows more than one TDS to be connected to a computer or printer.

Bus drivers operate as follows: Data input from Board 20 for the azimuth, channel ID, or a hard-wire input to the module for a module ID are connected to Pins B3 through B12, and Pins B17 through B26 (Board 31), respectively. The 2N930 transistors connected to these inputs serve as emitter followers to drive ~2 mA into the bases of the 2N3904 party-line bus drivers when the bus is strobed. The bus drivers are strobed by two 2N3300 transistors, each of which grounds the emitters to ten 2N3904's. There are 20 bus drivers on Board 31. The bases of the 2N3300 transistors are driven with a current of 40 to 50 mA to ensure good saturation and low emitter-to-collector voltage, and thus to produce as low as possible a signal for a Data 1. The bus strobe on Pin B2 of Board 31 is driven by the Load-1 signal ~4 μsec long. The extremely short duty cycle of the bus drivers makes it possible to supply 3 V to operate the bus drivers through a 1-kΩ resistor with a 330-μF capacitor to ground. This capacitor stores sufficient charge to allow no more than a few mV decay in the 3-V supply during the strobe pulse even though a rather large amount of current is involved in the strobing operation.

5-3.7 Mode Control Circuits. In addition to the bus-driver circuits, Board 31 also contains the mode-control circuits. Putting the TDM in automatic mode alters the system in the following ways:

A. Storage capacity is reduced from six words to one word (the last word transmitted to the TDM) by feeding the One-Empty signal from Board 20 into Pin B29 of Board 31. As soon as the shift register on Board 20 is full, which occurs ~1 to 1½ msec before the end of the data pulse (which generates the Load-1 pulse), One-Empty goes low, generating a differentiated pulse for Integrated Circuit 2 on Board 31. The positive output pulse at Pin 3 of Integrated Circuit 2 drives a 2N3904 transistor connected in an AND circuit with another 2N3904 that is turned on in the automatic mode (that is, when the voltage is high at the mode-control input and, therefore, high at the input of the base of the second 2N3904). This AND circuit produces a negative pulse at Pin A28 of Board 31, and this pulse is wired to Pin A24 of Board 23. A negative pulse at Pin A24 of Board 23 resets Words 2 through 6, thereby ensuring that all words except the first are zero when the end-of-data pulse is generated. When a Load-1 pulse occurs, the data are loaded into Word-6 and Board 20 is reset automatically, ensuring that no more than one word ever appears in the TDM at one time in the automatic mode.

B. Because the printer or computer will print out its own time tagging, it is not necessary to include time-tagging information in the NIXIE display. Therefore, the time-tag NIXIES are blanked by removing the decode power from Board 1B, which gets its power from Pin A27 of Board 31. The azimuth decode power is fed in at Pin B28 to ensure that in the manual display mode the time-decode power can be on only when the azimuth-decode power is also on.

C. Because the data presented by the NIXIE tubes are automatically updated, it is not necessary to use the reset push button. The reset signal, fed in at Pin A29 of Board 31, is inverted twice to appear at Pin B30 of Board 31. When the mode voltage is high, the input to Pin 12 of Integrated Circuit 2 will be low, thereby ensuring that the reset signal will be blocked from Pin B30 of Board 31, thus deactivating the push button.

D. The decimal point in the time-tag time readout is disconnected by means of Pin B32 of Board 31. When the mode voltage is high, the input to the 2N3440 transistor is low, thereby preventing any current from flowing through the decimal-point neon bulb.

E. The mode-control voltage is connected to Pin A33 of Board 21. When the mode voltage is high, that is, in automatic mode, the 5-V switched power at Pin A31 of Board 21 is always present. Because large amounts of power are available with the printer or computer, it is no longer necessary to conserve power and, therefore, unnecessary to switch the 5 V off.

F. The mode voltage is also applied to Pin B4 on Board 21. This ensures that both the NIXIE decode power and the reference for the NIXIE regulator supply are always present. The latter causes the NIXIE power supply to turn on, and the azimuth and ID NIXIES to remain continuously on, as long as the mode voltage is high.

G. If six words are already stored in the TDM and a switch is made to the automatic mode, Board 20 must be reset because failure to do so would lock up the system and prevent data from automatically entering in the automatic mode. The mode voltage is therefore applied to Pin

B11 on Board 21. The inverted output of the mode voltage at Pin A11 of Board 21 is connected to Pin B10 of Board 21, thereby ensuring that a reset (a low pulse) appears at Pin A9 of Board 21 when mode voltage is put in the automatic mode. A 47-pF capacitor between Pins A18 and A21 of Board 21 is connected between Pins A9 and A11 of Board 21 to speed up the action of Transistor 24 to ensure that the reset pulse at Pin A9 is rapid enough to trigger the single-shot circuits (Number 3 on Board 23). In this manner, an automatic reset is generated when switching to automatic mode that will clear one word in storage and thereby clear Board 20 to allow it to receive data signals. The signal at Pin A9 of Board 21 is low continuously as long as the system is in automatic mode. However, the mode-control voltage at Pin A32 on Board 21 will remove the reset signal as soon as the modified Schmidt circuit switches to a high output. This switching is delayed slightly after the low output at Pin A9 of Board 21 because of the 0.22-μF capacitor connected in the mode-control Schmidt trigger circuit. As soon as this Schmidt trigger output shifts to high, the reset signal is disconnected, the signal is removed from Pin B30 of Board 31, and no more reset signals may appear at Board 23 until operation is returned to the manual display mode.

5-3.8 Power Turn-On Circuits. To conserve power in the manual display mode, the 5-V power to Boards 1, 29, 22, and 23; to the logics section of Board 20; to the mode-control section of Board 31; and to most of Board 21 is cut off when no data are stored in the TDM. Automatic reset circuits on various boards ensure that all flip-flops and storage elements will be in their proper state when the 5-V power comes on.

Integrated Circuits 6 and 9 on Board 20 are reset through the action of a 0.47-μF capacitor connected to Transistor 24. This ensures that Integrated Circuit 9 contains zeros in both stages and, therefore, that the output of Integrated Circuit 10, Pin 14 (the shift-register mode-control voltage), is in the proper mode for an automatic reset. Integrated Circuit 11 is reset by the 0.47-μF capacitor connected to Pin 5. Integrated Circuit 11 controls the action of the initial reset circuit which consists of Transistors 21, 22, and 23 on Board 20. When Integrated Circuit 11 is in the low state, the first data signal that occurs upon receipt of a data train will cause a negative pulse to appear at Pin B28 of Board 20. This negative signal is fed to Pin 6 of Board 23 and causes a reset-shift signal at Pin 12 of Board 23, thereby causing Board 20 to reset before the first data bit is loaded into the shift register.

The reset and Integrated Circuits 6 and 9 on Board 20 also cause a Reset-One signal to appear at Pin A29 of Board 20, which by means of Board 23 causes a Reset Word One that will reset Board 22. Boards 29 and 1 are reset by the signal that appears at Pin A28 of Board 31, generated by means of the 0.47-μF capacitor and of two 4.7-kΩ resistors connected to the transistor connected to Pin 28. Board 23 will then reset all Boards 29 and Boards 1, as well as the ID storage and Word-6 control on Board 21.

The **remote reset** button flip-flop on Board 21 is also put in initial reset condition by means of a 0.47-μF capacitor and a 47-kΩ resistor connected to Pin 9 of Integrated Circuit 4.

In the above manner, all storage elements are put in their proper reset condition during the power turn-on transient and are, therefore, ready to receive a transmitted signal and display it correctly when it arrives. In addition, power may be applied to only the decode circuits of Boards 1A and 1B, and NIXIE power is turned on only when either the **read** or **remote reset** button is depressed in the manual data-display mode.

5-4 Time Tag Module

The TTM contains Board 26 (the visual display system time clock), Board 31 (used as a bus driver for the time-tag signal), and Board 30-3 (identical to the power-supply regulator shown in the dashed lines on Board 21).

The basic time reference of the system is a tuning-fork oscillator operating at 1200 Hz, with an accuracy of $\sim \pm$ 10 to 20 sec/day.

The 1200-Hz signal from the tuning-fork oscillator is reduced by Circuits 1, 2, 3, 4, and 5 on Board 26 to a 10-Hz signal. Integrated Circuits 5, 6, and 7 on Board 26 form a decade divider, and the four 2N3904 transistors connected to this decade divider produce BCD-coded outputs for the tenths-of-second time-tag signals. Similarly, Integrated Circuit 8, the first section of Circuit 9, and Integrated Circuit 10 form another decade divider that produces BCD-coded outputs for the seconds output, and a second section of Circuit 9 and Integrated Circuit 11 and the RS flip-flop formed from Circuit 12 produce the octal output for the tens time-tag signals.

The signals from Board 26 are fed directly to all TDMs where they form the input for Board 22, which is the Word-One Time Store board in a TDM. When data are loaded in Board 20 and the Load-1 pulse occurs, this time-tag information will be stored in Board 22.

The outputs of Board 26 also connect to 11 of the 20 bus drivers on Board 31. When a strobe pulse appears at Pin A of the module connectors (55-pin connectors) to indicate that data are being loaded in one of the modules, the Board 31 in the TTM is strobed, producing a bus-driver output to operate the printer which may be connected to one or more TDSs.

The mode-control voltage is connected to Pin A32 of Board 31 in the TTM. The alarm signal produced at Pin B31 of any of the TDMs is connected to Pin B28 of Board 31 in the TTM. Pin A27 of Board 31 is connected to the alarm and will, therefore, produce an audible signal when the switched 5 V is on in any of the TDMs in the visual display mode. In this manner, the alarm will automatically sound and continue to sound until all data are removed from all TDMs. In the automatic mode, however,

the audible alarm is unnecessary and the mode-control voltage at Pin A32 of Card 31 cuts off the voltage to Pin A27 of Card 31 to silence the alarm.

Board 30-3 produces a regulated voltage of 5 V to operate Boards 26 and 31 which are continuously turned on.

The TTM contains a meter to indicate the AGC voltages of the four receivers and, hence, the signal strengths to the receivers in the various TDMs. A selector switch allows selection of any receiver for display of its AGC voltage on the meter.

The **time clock** button connected to Board 26 will set this board to zero when the button is depressed. This will generate a reset-preset signal at Pin 20 of Board 26, which, if a printer is connected to the system, will preset the one-day time clock in the printer to whatever value is chosen on the preset thumb switches on the printer-control chassis. If it is desired to use two or more interconnected telemetry display systems, a time-slave cable may be used to make the connection. This time-slave cable at one of the systems will cause the clock signal at Pin 5 of Board 26 to be low, thereby slaving both clocks together. The driver connected to Pin 9 of Board 26 produces a 1200-Hz signal to slave another system to the original system. Through the action of the reset bus on Pin 30 of Board 26, all individual Boards 26 will slave together to reset to zero at the same time whenever any **time clock** button on a TTM is depressed, thereby synchronizing time-tag signals in various systems.

5-5 Test Code Generator Module

The TCG (labeled Portable Test Azimuth Generator on the front panel) generates codes to test the operation of the overall system by testing various TDMs.

This module can be removed and placed in a separate box (described in LA-4444-TM, Vol. II) to activate long lines in the field or to connect with a transmitter in the field to test the overall operation of the transmitter and receiver in the TDM.

The TCG contains two cards, Board 24 (a power-control board for Board 6) and Board 6 (a parallel-to-serial data converter generating azimuths identical to those transmitted from the azimuth processor).

Board 6 is the same as that used in the azimuth processors to generate long-line and transmitter codes. A test code is selected by means of the thumb switches on the front panel of the TCG. An additional switch section, with settings 1 through 4 only, will allow this test code to be fed to TDMs 1 through 4. When the TCG is connected in an external box for field operation, any setting of this switch will produce a test-code output.

Two push buttons on the front of the TCG module allow a single or a repetitive series of test codes to be generated. The single button connects to Pin 32 of Board 24. When the button is depressed, it turns on the power switch consisting of Transistors 1, 2, and 3; the power switch, after generation of a single test code, is turned off by means of Transistor 9. When the **repeat** button is depressed and held down, it will turn on the power switch regardless of reset pulses coming back from Transistor 9.

The regulator on Board 24, consisting of Transistor 4 and the LM105 integrated-circuit voltage regulator, generates 5 V when the power switch is on at Pin 27 of Board 24. When the 5-V power is on, the Schmidt trigger-type delayed timer (using Transistors 5 and 6) holds the base of Transistor 8 through Transistor 7 at ground potential and prevents the multivibrator, consisting of Transistors 8 and 9, from operating and thereby from sending start pulses to Board 6 (Pin 19). After a delay of ~ 0.7 sec, the 4.7-μF capacitor connected to the base of Transistor 5 charges sufficiently to turn off Transistor 6 and thereby allows Transistors 8 and 9 to operate as a multivibrator. Every cycle of the multivibrator causes a start pulse to appear in Pin 19.

The output from Pin 21 of Board 6 is in the form of a test code with very sharp rise and decay times and very little drive capability. This output is connected to Pin 14 of Board 24 that connects to a line driver whose output is connected to Pin 24 of Board 24. This line driver is capable of driving a pulse current of at least 100 mA into the long line.

Board 6 is part of the AP system and is described in LA-4444-TM, Vol. III. The thumb switches connected to the various inputs of Board 6 will determine the serial output code that appears at Pin 21 of Board 6. Board 6 resets itself when it finishes transmitting. It is, therefore, only necessary to generate a start pulse to generate a test code.

To conserve power, the line driver on Board 24 is not connected to +5 V when the power switch is turned off, thereby ensuring that no power is drained from the TCG while it is not operating. To allow Transistors 2N2905 and 2N2219 in the output stage of the line driver to have a code present when power is off, 5 V must be supplied to the emitter of the 2N2905 from current fed from the long lines to Pin 24 through the 1-MΩ resistor to the 180-μF capacitor connected to the emitter of the 2N2905.

When the test-code generator is connected to Pin A32 of Board 20, as it would be in a system, the voltage at Pin A32 is derived from the 5 V by way of the 47-kΩ resistor, with the 1N4154 diode and the 100-Ω resistor connected from Pin A32 to the 5-V switch. This resistance is sufficient to keep the output at Pin 24 of Board 24 at +5 V. When the test-code generator is connected to a transmitter, the 270-kΩ and 200-kΩ dividers in the transmitter Board 25 are sufficient to keep 5 V again at Pin 24 of Board 24. However, when the test-code generator is connected to a daisy-chain input, this input has a resistance of ~ 200 kΩ to ground. Because this voltage is absent, it is likely that an error pulse will be generated at the error light of the TDM every time a test code is generated with daisy-chain input. This is normal and does not indicate malfunction of the TDM.

5-6 Power Supply Module

5-6.1 General. The TDS main power supply system normally consists of the power supply module (PSM), a 30 A-h rechargeable nickel-cadmium battery, the overvoltage-reverse voltage circuit protector card (Board 37-3), and the temperature-compensated voltage regulator.

In normal operation, the power supply is connected to a 115-V ac line (50 to 400 Hz) and keeps the battery fully charged at ambient temperatures from −40 to 125°F.

If the line voltage drops below 75 V or increases to above 135 V, the PSM will fail to provide power to the system (but will not be damaged) and the battery will supply power to the system for a period of time that depends upon the current drain from the battery. If all TDMs are operated in the manual display mode and shots stored are read out promptly, the battery will supply power for one to three weeks.

When the line voltage is reestablished correctly, the PSM will recharge the battery to full charge.

If the battery is removed or fails, the PSM will supply power to the system as long as the ac line voltage is correct.

If the battery is accidently connected backwards or if the power supply fails by providing an output voltage above 20 V, the overvoltage-reverse voltage protector card will blow out the fuse connected to it to prevent damage to the TDMs, the TTM, and the TCGs.

The batt low lamp on the PSM will light when the battery charge drops to 25 to 50% of full charge and will remain on until the battery is either fully discharged or is recharged to ~ 50% of full charge.

A meter on the front panel of the PSM indicates the current being supplied by the PSM to the battery and to the rest of the system. If the battery is not fully charged, the meter will indicate 2 or 3 A continuously until the battery is fully charged. With the battery fully charged, the meter will indicate the current supplied to the TDS during normal operation.

5-6.2 Overall Wiring of PSM. Chapter 8 contains information on the overall wiring of the PSM, the battery, the temperature-compensated voltage regulator and ooost charger, and the overvoltage-reverse voltage protector.

5-6.3 Overvoltage Protection of PSM. The overvoltage cutoff card (Board 30-1) continuously monitors line voltage and turns off ac voltage to the power transformer (M8055) if line voltage increases above ~ 135 V. This card prevents damage to the PSM if it is connected to the wrong voltage or if a generator ac voltage regulator fails. Board 30-1 will withstand a continuous overvoltage up to 250 V ac.

Diodes D1, D2, D3, and D4 form a full-wave diode bridge in series with the transformer primary winding across the ac line. If the output of the bridge is shorted, power is applied to the transformer to turn on the PSM. If the bridge output is open, no power is applied to the transformer, the PSM is turned off, and a full-wave rectified dc voltage appears across Transistor Q1.

Transistors Q1, Q2, and Q3 and Resistors R1 and R2 form a dc transistor switch across the output of the bridge.

The line voltage (appearing between Pins 8 and 20 of Board 30-1) is half-wave rectified by Diodes D4 and D5 to a filtered voltage across C3. Transistors Q4 and Q5 are connected in a Schmidt trigger circuit that applies current to the base of Q3 to keep the switch on (diode bridge short-circuited) as long as the ac voltage is not too high. As the ac line voltage increases, the resistor divider R3 and R4 raises the base voltage of Q4 until the voltages at the bases of Q4 and Q5 are nearly equal; the current then abruptly shifts from Q4 to Q5, shutting off the transistor switch and turning off power to T1. Diode D10 is the voltage reference for the Schmidt trigger.

The three Zener Diodes D6, D7, and D8 protect the transistor switch against overvoltages (above 300 V) in the event of line transients due to lightning, switching transients, or voltages above 200 V rms.

The output of the power transformer (M8055) is rectified to a nominal 32 to 37 V dc at 115-V input and is filtered by the two 6000-μF capacitors. The output dc voltage will allow the 3-A switching regulator to operate correctly from input voltages of 70 to 150 V ac.

5-6.4 Three-Ampere Switching Regulator (Board 30-2). Because of the wide range of input ac voltage required of the PSM, the normal proportional type of dc regulator would require dissipation of excessive quantities of heat and is, therefore, not practical. Instead, a switching regulator is required.

Transistor Q1, Diode D3, Inductor L2, and filter Capacitors C5 and C6 are the basic switching and filtering elements of the power supply regulator. In addition, Capacitor C1 and Inductor L1 filter the switching transients generated on Board 30-2 from the unregulated power supply, and Inductor L3 and Capacitor C7 filter the switching transients at the output to prevent them from appearing at the load.

The LM105 regulator senses the output voltage (through Dividers R11, R12, R13, and C4) at Pin 6. A positive feedback signal necessary to cause the regenerative switching action is applied through R6 to Pin 5 of the LM105. The voltage at Pin 5 is an unsymmetrical square wave of ~ 50 to 100 mV amplitude with a frequency of 8 to 20 kHz. The voltage at Pin 6 is a triangular wave of the same amplitude and frequency. The output of the LM105 at Pin 2 drives, through Transistors Q3 and Q2, the power-switching transistor (Q1). Zener Diode D1 prevents the applied voltage to the LM105 from exceeding its rated maximum of 40 V.

The 5-W, 0.2-Ω resistor (R10), along with Transistors Q4 and Q5 and Zener Diodes D2 and D4, forms the current-limiting circuit. As more and more current is

drawn from the regulator circuit, the voltage drop across R10 becomes large enough to turn on Transistor Q5, which causes (through Q4) the voltage-sensing terminal (Pin 6) of LM105 to remain at its correct value while allowing the regulator output voltage to drop just far enough to maintain the output current at its maximum. Switching action is thus maintained (to prevent burning out Q1) while the output voltage drops. Diodes D2 and D4 are necessary to prevent latch-up and burning-out of LM105 if these voltages are not restricted to the correct values.

Resistor R14 and Capacitor C8 allow an external voltage to be fed back to the regulator from the temperature-compensating auxiliary regulator connected at the battery terminals. The external voltage allows the auxiliary regulator to control the output voltage of the main regulator to the exact value required to fully charge the battery throughout its temperature range. When the battery is removed, the main regulator assumes a constant output voltage set by Resistors R11, R12, and R13.

Resistor R10, in addition to acting as a current-limiting sense resistor, is also used as a shunt for the output current meter. The voltage across Resistor R10 is read on the front-panel meter (a 300-μA meter with a series resistor to calibrate it to 3A at full scale).

The output of the main regulator charges the battery and provides power for all other TDS circuits. Because all other TDS circuits have secondary regulators of either the proportional or switching variety, the output of the main regulator is not critical except for charging the battery. All TDS circuits will operate satisfactorily with an input voltage of 10 to 20 V dc.

5-6.5 Low Battery Voltage Indicator (Board 30-4). The low-voltage indicator card lights the batt low lamp on the PSM front panel when the battery voltage drops 1.5 V below full charge. Because the full-charge voltage of the battery has a temperature coefficient of about −15 mV/°F (or 1.5 V/100°F), the low-voltage indicator must also have the same temperature coefficient.

Transistors Q5 and Q6 are a Schmidt trigger circuit connected in the mode where the input voltage (base of Q5) is fixed and the applied B+ voltage varies. As the applied B+ voltage drops from 13 V (the full-charge voltage at 70°F) to 11.5 V, the current through Q6 at higher voltages shifts abruptly to Q5 (due to the position feedback action of the R2, R5, and R6 voltage divider) which turns off Transistor Q7, allowing Q8 to turn on and to light the pilot lamp. The applied voltage must decrease to 12 V (at 70°F) before the lamp will extinguish (due to the hysteresis of the Schmidt trigger).

The parts of the power-supply system external to the PSM are the battery, the overvoltage-reverse voltage protector, and the temperature compensated auxiliary regulator.

5-6.6 Overvoltage-Reverse Voltage Protection Circuit (Board 37-3). The overvoltage-reverse voltage protection circuit (Board 37-3) is not mounted in the PSM but is considered a part of the power supply system. This circuit prevents damage to the transistors and integrated circuits of all modules except the PSM should the regulated voltage rise above 20 V. Such a voltage rise would cause Zener Diode D2 to conduct and SCR1 to fire, drawing sufficient current to blow out Fuse F1 and thereby disconnecting the circuits. **Fuse F1** on the rear panel of the TDS must be replaced after the cause of the failure is determined.

If the battery is connected in reverse, Diode D1 will conduct and blow out Fuse F1. This action will not protect the PSM, which will be damaged and must be repaired after the battery reversal is corrected.

5-6.7 Battery. The battery mounted externally to the main TDS cabinet is a 30 A-h, 10-cell nickel-cadmium battery Model VNC-30 manufactured by the Eagle-Picher Industries, Inc. *Note that these batteries do not use the same electrolyte as standard lead-acid automotive batteries; addition of acid to these batteries will destroy them.*

The batteries are shipped with round-headed vent seal screws in the filler plugs. *These must be removed and replaced by the square-top vent plugs provided in the attached bag before charging.* Failure to do so may damage the batteries and endanger personnel.

Unlike lead-acid cells, the electrolyte level drops as the cells discharge. *Therefore, never add electrolyte to the batteries unless they have been on charge for at least two days.* If the electrolyte level in a fully charged battery has dropped due to normal charging, add distilled water only to bring the level up to ¼ to ½ in. above the bottom of the plastic well. If electrolyte has been lost because of spillage, add potassium hydroxide electrolyte to raise the level as needed.

Do not short-circuit the batteries by accidently dropping metallic objects across the metal connectors on top of the batteries as this can generate a fire and burn hazard.

The batteries are contained in a metal box with a side connector that mates with the TDS battery cable. The battery box also contains the temperature-compensated auxiliary regulator (an epoxy encapsulated circuit mounted on top of the battery). Ensure that the connector to this circuit is connected before the battery is put on charge because failure to do so will result in excessive charge rates and loss of electrolyte.

5-6.8 Temperature-Compensated Auxiliary Regulator Circuit (Board 27). The temperature-compensated auxiliary regulator circuit (Board 27) is mounted with the battery in the battery box. Nickel-cadmium batteries require close control of the charging voltage with a constant-potential method of charging. Accordingly, the temperature-compensated regulator is mounted on top of the battery to ensure accurate sensing of temperature and to regulate the voltage at the battery terminals rather than at the main regulator. Zener Diode D1 (LM103-2.4) and diode-connected Transistors Q5 through Q12 form the reference voltage source with the required temperature

coefficient of −15 mV/°F. The Nexus Q200 amplifier senses the error voltage, amplifies it, and applies it through R21 to the voltage-adjust terminal of the main regulator. The operational amplifier (Q200) is a low-current amplifier supplied with a regulated voltage generated by the regulator consisting of Transistors Q13, Q14, Q15, and of reference Diode D2 (LM103-5.6).

CHAPTER 6. BOARD REPAIR

6-1 General

For troubleshooting operations, it is advisable to put the system into automatic mode by connecting Pins W and Y to the TDS connector, or by connecting Pins W and Y on Board 37.

6-2 Board 20

Connect the TCG to the module being tested and use the repeat button to generate a continuous string of test codes. With an oscilloscope, examine the signal at Pin A32 of Board 20. In addition, be sure that receiver noise is present at Pin A33 of Board 20. If receiver noise is not present, Board 20 will not load correctly. If receiver noise is absent, track down the trouble to see whether a receiver or a regulator on Board 21 is defective.

Look at the output of Transistor 3 on Board 20 to see whether the differentiated test-code signals are present. If they are not, the trouble lies somewhere in the input amplifier.

6-2.1 Input Amplifier. Examine the output of Transistor 5 at Pin B31 to see whether the noise switch is allowing the signal to pass to the Schmidt trigger transistor (Number 8). If the noise switch is not operating correctly, determine the cause. If the noise switch is operating correctly, check at the collector of Transistor 8 to see whether the Schmidt trigger is switching. If the Schmidt trigger is switching correctly, examine the collector of Transistor 10. At this point, the reconstructed code should be identical to the test-code output except for the rise and fall time to the signal.

If there is no test code at the output of Transistor 10, look at the signal on Pin A12 of Board 20. A high signal will inhibit the output of the Schmidt trigger and prevent the test code from appearing. A high signal on Pin A12 indicates either that the shift register is loaded and does not receive reset pulses through Pin B24, or that there is a malfunction in the reset circuits on Board 20.

6-2.2 Reset Circuit. Examine Pin B24 for reset pulses that should occur at least once after turning the system power off, and then on again, and putting a single code into the TDM. If necessary, disconnect the end of the resistor connecting the base of Transistor 10 to Pin A12 to ground and examine the output of this stage. If there is an output from this transistor, examine the collector of Transistor 19 for the 4 to 4½ msec pulse that should appear there. Also examine the output of Transistor 13 to see if the 60-μsec single-shot pulses are present. During this process, it is advisable to trigger an oscilloscope externally with a probe (not a divide-by-ten probe) connected to the external horizontal synchronization input from Pin A32 of Board 20. If the rising edge of the initial *"one"*-pulse is to be synchronized, set the synchronizing controls on the oscilloscope to AC Slow, Plus Slope. If the falling edge at the beginning of the waiting period is to be examined, the oscilloscope can be set on AC Fast, Negative Slope.

6-2.3 End-of-Data and Shift Pulse. If the two single shots are working correctly, examine Pin A28 for the end-of-data pulse and Pin B25 for the very narrow shift pulse, or Pin A27 for the *"one"*-pulse. Trouble in Board 20 may be due to malfunctions of the shift registers (Integrated Circuits 1, 2, 3, 4, and 9), the parity counter (Integrated Circuit 6), or of the compare circuit (Integrated Circuits 5 and 7). Examine the output of Integrated Circuit 7, Pin 10, to see if its output is high just prior to the end-of-data pulse. Examine the output of Integrated Circuit 9, Pin 12, to ensure that its output is also loaded just prior to the end-of-data pulse. If the trouble is in the shift register, it may be necessary to disconnect Pins A3 and B3 (Board 20), and connect Pin B3 to ground temporarily to examine the operation of the shift register. This will cause continuous error pulses at Pin B30; it will not allow loading of the data through the Load-1 pulse at Pin A31, but it will allow checking the output of the various stages of the shift register for possible malfunctions. Be sure to reconnect Pins A3 and B3 at the end of this operation.

6-2.4 Error Pulse. If Board 20 is still not operating correctly, look at Pin B30 to see if an error pulse is being produced. If such a pulse is present, track down its cause through Integrated Circuits 8 and 12, 7, 5, 6, and 1 to localize the trouble on Board 20. If Board 20 loads only once and then locks up and no reset pulse appears at Pin B24 the first time a code is loaded after the module is turned off and back on again, the trouble is either in

Board 23, or the *"Two-Full"* signal connected to **Pin 14** of Board 23 is high when it should not be. In any event, track a Load-1 pulse (**Pin 3** of Board 23) through Integrated Circuits 8 and 9 to **Pin 12** to ensure that the reset pulse is appearing at Board 23. If this trouble is not easily located, it might be advisable to connect directly **Pins A31** and **B24** of Board 20 and to remove the other wires to isolate the trouble.

6-3 Board 21

If the trouble is in Board 21, examine **Pins A30** and **B1** to ensure that main system power is present at these pins.

6-3.1 Main 5-V Regulator. Next, examine **Pin A32** for the 5-V regulated output. If it is absent, determine whether the absence is due to a malfunction of the switching regulator or to a short circuit. If the trouble is not due to a short circuit, examine the collector of **Transistor 1** to see if the switching waveform appears. This switching waveform signal should vary from ~ 8 kHz at no load to 50 to 100 kHz under full load and should be an asymmetrical square wave. If this regulator is operating property, examine the 5-V switched output at **Pin A31** of Board 21. If this voltage is present, the power circuits are operating correctly. If not, determine whether the cause is due to a short circuit, to a blown-out Transistor 3 (2N2905), or to incorrect operation of Transistors 4 and 5, and check whether the 5-V mode-control signal is present at **Pin A33** of Board 21.

6-3.2 Reset Push Button Circuits. To examine the reset push button circuits, depress the **read** button on the TDM or the **remote reset** button repeatedly and look for reset pulses at **Pin A9** of Board 21 with an oscilloscope on internal synchronization. If reset pulses are absent, track the signal back to the point where the signal is correct to determine the cause of the failure.

6-3.3 NIXIE Regulator. To examine the NIXIE regulator on Board 21, first determine whether there is voltage at **Pin B4** to turn on Transistor 9. If 5 V is present on **Pin B3**, then Transistors 8 and 9 are working correctly. If not, determine the cause and repair it. Measure the NIXIE voltage on Board 34. It is correct if between 170 and 180 V, and no further attention need be paid to the NIXIE regulator. If the voltage is high, Transistor 38 (2N2095) on Board 21 is probably shorted. If this is not the case, track down the trouble. Examine the output of **Pin B6** on Board 21, the data-lamp flasher, to ensure that voltage is present.

6-3.4 Channel Identification. If the ID NIXIE does not indicate the correct value, check the signals at **Pins B24, B14,** and **B16** of Board 21 to ensure that they are correct. Then, check the **ID-1, ID-2,** and **ID-4** signals as shown in the Board 21 diagram (p. 31) to make sure they are correct. If they are correct, the trouble is with the NIXIE decoder. Determine which characters are not displayed and track down the cause.

6-4 Board 23

To check the operation of Board 23, put the TDM in automatic mode and examine the reset and load pulses appearing for each word. When the Load-1 pulse occurs, Words 2 through 6 should be loaded. Check with the oscilloscope to find the signals, synchronizing the oscilloscope on the external trigger from either Load-1 or on **Pin A** of the TDM connector, either at the TDM or at Board 37. About 10 μsec after the Load-1 pulse, the Reset-Word pulse should appear at Words 2 to 5. To examine the Reset Word-6 pulse from Board 23, synchronize the oscilloscope on **Pin A12** of Board 20 and examine the pulse that appears at **Pin 30** of Board 23 (the Reset Word-6 pulse) with the oscilloscope. Reset pulses will also appear at Words 2 through 5 at the same time. If all these pulses appear, then all the drivers for the reset and mode signals are probably operating correctly. To check the word-control circuits, synchronize the oscilloscope again on **Pin A** of the TDM connector. While continuously loading codes, look at the output of Circuits 5 on Board 23. The Word-6 control connected to **Pin 31** of Board 23 will decay linearly to zero, while the other four Miller integrator circuits will decay partway to zero on a ramp to a voltage of ~ 2 to 2½ V and then charge back to 5 V or, in some cases to 4 V, when the Reset-1 signal reappears. If the Miller integrators are all functioning normaily, it can be assumed that Board 23 is functioning correctly. The pilot-lamp circuits can be tracked down by seeing where the malfunction exists (usually a defective transistor, connection, or pilot lamp).

After checking in automatic mode, the telemetry display module should be put in manual mode and test codes should be loaded one at a time to ensure that the data are loading correctly and that the shots lamps display in correct order.

6-5 Board 22

To examine Board 22, recall that the Load-1 pulse will load Board 22 and Reset-1 will reset it so that the data should be present at the output of Board 22 for ~ 10 μsec. Put the TDM module in automatic mode, and depress the **repeat** button. Synchronize the oscilloscope externally on **Pin A** of the TDM connector on Board 37 and observe the output of Board 22. Consult the TDM Wiring Diagram (46Y23631-D 60) on p. 76 to determine which signal is connected to which output pin on Board 22.

The time-tag signals are changing slowly enough to be observed visually on the oscilloscope. For example,

one can determine that the 0.1-sec time-code signal appearing on **Pin A18** of Board 22 is correct by observing the trace to go up and down at ~ 10 cps on the oscilloscope. If no output signals are present on Board 22, the load or reset circuits obviously are not functioning correctly. If only some outputs are incorrect, then the trouble has been localized on Board 22.

6-6 Board 31

Board 31 consists of two sections, one containing 20 party-line bus drivers which drive external equipment (a printer or computer), and the other containing mode-control circuits. The bus drivers and the associated strobe circuit ordinarily will not affect the operation of the TDM. If there is trouble in the operation of the TDM because of Board 31, it is almost certainly located on the mode-control section of this board.

6-6.1 Mode Control Circuit. Measure the mode-control voltage at **Pin A32** of Board 31, in both automatic and manual modes. In automatic mode, the voltage should be 5 V, and in manual mode, zero. With the exception of the rise and fall times, this voltage should be duplicated at **Pins 9** and **10** of Integrated Circuit 2. Check to see whether this is true.

6-6.2 Decimal Point. If the decimal-point neon bulb is extinguished in automatic mode and lights properly in manual mode when the reset push button is depressed, the 2N3440 transistor connected to **Pin B32** of Board 31 is operating correctly. Pins A31, B31, and A30 are not used in the TDM and, therefore, can be ignored.

6-6.3 Read and Remote Reset Push Button Disconnect. To check the reset push-button disconnect between **Pins A29** and **B30** of Board 31, put the TDS in automatic mode and the TCG on continuous transmission, depress either the **read** or **remote reset** button, and check (with the oscilloscope on internal synchronization, negative slope) for the reset pulses on **Pin A29** when the reset push button is depressed repeatedly. Check again on **Pin B30**. If these pulses are present in manual mode and absent in automatic mode, this section is operating correctly.

6-6.4 Automatic Reset. To check the automatic reset of Board 23 at **Pin A28** of Board 31, put the TDS in automatic mode with the test generator on continuous transmission. Synchronize the oscilloscope on **Pin A12** of Board 20 (positive slope). Observe the output pulse of **Pin A28** of Board 31 to ensure that it is present in automatic mode and absent in manual mode. In addition to checking the reset at **Pin A28** when switching from manual to automatic mode, it should be possible to synchronize the oscilloscope internally and to switch the mode-control button between manual and automatic. Every time the switch is made, a pulse should appear at **Pin A28**.

6-6.5 Time-Decode Circuit. To check the time-decode power circuit, put the system on manual mode, depress the **time clock** button, and measure the voltage at **Pins B28** and **A27** of Board 31. If both **Pins B28** and **A27** are at 5 V, switch to automatic mode; the 5-V signal at **Pin A27** should vanish.

6-6.6 Bus Drivers. To check the bus drivers, connect a **termination shoe** to one of the TDS connectors. Remove the rear panel and with an oscilloscope synchronize on **Pin A** of the TDM connector (negative slope). Observe the pulses produced at **Pins A** through **Q**. (Note that some of these connections are grounded. Consult the TDM Wiring Diagram (46Y23631-D 60) on p. 76 to determine which signal is connected to which pin.) These pulses should be negative and have an amplitude of 3 to 4 V. The low point on the pulse should be less than 0.4 V, and the length should be ~ 5 μsec. Change the azimuth and ID settings of the TCG to observe the presence and absence of each pulse. On the time-tag pulses, the time will change automatically. No changes need be made in the TCG thumbswitch settings; simply observe when the time-tag pulse is present or absent.

6-6.7 Module Identification Code. To check the module ID bits, it may be necessary to switch module connectors because the module ID is established by the connector and is hardwired on Board 37. Therefore, the easiest way to check the module ID bits is to switch all four connectors to one module, one at a time.

6-7 Board 1

To check Board 1 (1A or 1B), put the TDS in automatic mode using the TCG in "continuous" mode by pressing the **repeat** button. Synchronize the oscilloscope on **Pin A** of the TDM connectors, or on **Pin A** of Board 37 (negative slope). At the beginning of the trace, all stored bits should be zero and should, within a fraction of a microsecond, come up to their final value where they will stay for almost the entire time (~ 30 msec between test codes). Using an oscilloscope, look for the stored data; for example, if it is desired to examine the azimuth 0 - 5, look at **Pin 14** on Integrated Circuit 3 of Board 1A. If these pulses are correct, the storage section of Board 1 is operating correctly. Check to see that the NIXIE tubes indicate the correct value.

If, in addition to the azimuth NIXIE tubes, it is desired to observe the time-tag NIXIES, connect temporarily **Pin A2** to **Pin A1** of Board 1B, and the time-tag values will be displayed continuously (with the TCG on "continuous"). If there is any further trouble on Board 1, it is due to the NIXIE decoding section of the board.

6-8 Board 29

To check Board 29, put the TDS in automatic mode

and the TCG on "continuous" as for checking Board 1. Check to ensure that the four reset and four load pulses are present before checking the board itself. On each string of four flip-flops, examine the input and the output of the first flip-flop, and the output of the second, the third, and the fourth flip-flop to locate the trouble.

6-9 Board 24

6-9.1 Power Control Circuits. To check the operation of Board 24, first measure the voltage of **Pin 31** of Board 24 to ensure that the battery is connected to the board. Depress the **repeat** button and measure the voltage at the collector of **Transistor 1**. It should be ~ 0.05 to 0.1 V less than that appearing on Pin 31. Pushing the **repeat** button should cause this voltage to appear regardless of the condition of the remainder of the card. With the repeat switch depressed, measure the voltage of **Pin 27** of Board 24. This should be 5 to 5.5 V. Next, depress the **single** button connected to **Pin 32** of Board 24 and observe the voltage at the base of **Transistor 7**. When the **single** switch is depressed, the voltage at the base of Transistor 7 should come up to ~ 0.6 V and remain there for ~ 0.7 sec. When this voltage vanishes, the multivibrator, consisting of Transistors 8 and 9, should start cycling. Depress the **repeat** switch connected to **Pin 33** and observe the waveform at **Pin 19**. This wave should be rectangular for ~ 85% of its duration of ~ 30 msec between pulses. The rise time should be quite slow, and the decay time quite rapid. If the circuit is not turning off after a single test code, examine the waveform at the base of Transistor 3 after the **repeat** button is depressed. This waveform should drop from an amplitude of ~ 0.6 V to a peak negative voltage of ~ −2 V. This waveform should turn the power switch off. If it does not, the trouble is in the power switch. If the waveform is not present, the trouble is in the coupling capacitor or resistor.

6-9.2 Line Driver. To check the line driver, push the **repeat** button connected to **Pin 33** and observe the waveform at **Pin 14**. The waveform at the collector of **Transistor 10** should be the inverse of that. The bases of **Transistors 11** and **12** should be at a potential of ~ 1.2 to 2.4 V and should not vary. The emitters of **Transistors 11** and **12** should vary 0.6 V above and below this potential. Check the waveforms at the collectors of **Transistors 11** and **12** to ensure that the output transistors are being driven, and finally check the output of **Pin 24** of the line driver. Rise and fall time of the signal at Pin 24 should be a linear ramp-up of ~ 5 μsec to 5 V and down from 5 V to zero.

6-10 Board 26

Board 26 is checked by following the signal through all stages of the frequency dividers. Measure the waveform at **Pin 3** of the tuning fork to ensure that it is a 1200-Hz square wave of ~ 3 V amplitude. Check the output of the transistor connected to the tuning-fork oscillator. With **Pins 5** and **6** of Board 26 at +5 V, the signal should appear at **Pin J1** on Board 26. Check for a 60-Hz wave at **Pin J5**. The voltage should remain low for 80% of the period and should rise to ~ 3.5 to 4 V for 20% of the total period. This waveform also can be checked at **Pin 7** of Board 26.

Check next for a 20-Hz signal at **Pin J7**. For the remainder of the signals check the 0.1-, 0.2-, 0.4-, 0.8-, 1-, 2-, 4-, 8-, 10-, 20-, and 40-sec output signals from the various pins of Board 26. If no dividers are operating correctly, check the reset line connected to **Pin 30** of Board 26 to ensure that this is high–a potential of +5 V. If the reset line is low, determine whether the reset bus or the reset push-button circuit is the cause of the trouble or whether the reset line is short-circuited to ground. Finally, depress the reset push button repeatedly while looking at **Pin 20** of Board 26 to determine whether the reset signal is present. This signal should be a negative pulse of ~ 10 to 15 μsec with an amplitude of 5V.

6-11 Board 34

If NIXIE voltage is absent, and checking according to Sec. 6-3.3 reveals no defect on Board 21, the battery current is either too high or too low when turning on the NIXIE regulator and there is base drive to **Transistor Q1** (2N3741) on Board 34, then the trouble is probably in Board 34. Check the +175-V bus for short circuit or low resistance to ground; check **Capacitors C1, C3,** and **C4** for short circuits; check **Diodes D1, D2, D3,** and **D4** for short circuits or open diodes; and check **Resistors R1, R2,** and **R3** for proper resistance. If all these checks indicate no trouble, check the transformer for continuity.

6-12 Board 6

See LA-4444-TM, Vol. III, for repair of Board 6.

CHAPTER 7. CIRCUIT DIAGRAMS OF INDIVIDUAL TDS BOARDS

Circuit diagrams of individual boards of the TDS used in conjunction with Chapters 5 and 6 are listed below.

Board Number	Title	Figure Number	Pages
Board 20	Serial-to-Parallel Code Converter	Fig. 7.1	28 to 31
Board 21	Power, ID Store and Decode, Reset, and Miscellaneous Circuits	Fig. 7.2	32 to 36
Board 22	Word-One Time Store	Fig. 7.3	37 to 38
Board 23	Stacked Storage Control	Fig. 7.4	39 to 40
Board 24	Test Code Power Control and Line Driver	Fig. 7.5	41 to 43
Board 26	One-Minute Time Clock	Fig. 7.6	44 to 46
Board 27	Temperature-Compensated Battery Charger Control	Fig. 7.7	47
Board 29	Stacked Storage	Fig. 7.8	48 to 49
Board 30	Main Power Supply Circuits	Fig. 7.9	50 to 53
Board 30-1	Overvoltage Protection Circuit		50, 51
Board 30-2	3-Ampere Switching Regulator		50, 52
Board 30-3	350-mA Switching Regulator		50, 53
Board 30-4	Low-Voltage Alarm		50, 53
Board 31	Party-Line Bus Drivers and Mode Control	Fig. 7.10	54 to 55
Board 34	NIXIE Display and Power Supply	Fig. 7.11	56 to 57
Board 36	Termination Shoe for Party-Line Bus	Fig. 7.12	58
Board 37	Interconnection Board	Fig. 7.13	59
Board 37-1	Lightning Arrester for Long Lines		60
Board 37-3	Reverse and Overvoltage Protection Circuit		61
–	TDS Interconnection Panel	Fig. 7.14	62 to 63
Board 1	NIXIE Store and Decode	Fig. 7.15	64 to 67
Board 6	Parallel-to-Serial Data Converter	Fig. 7.16	68 to 72

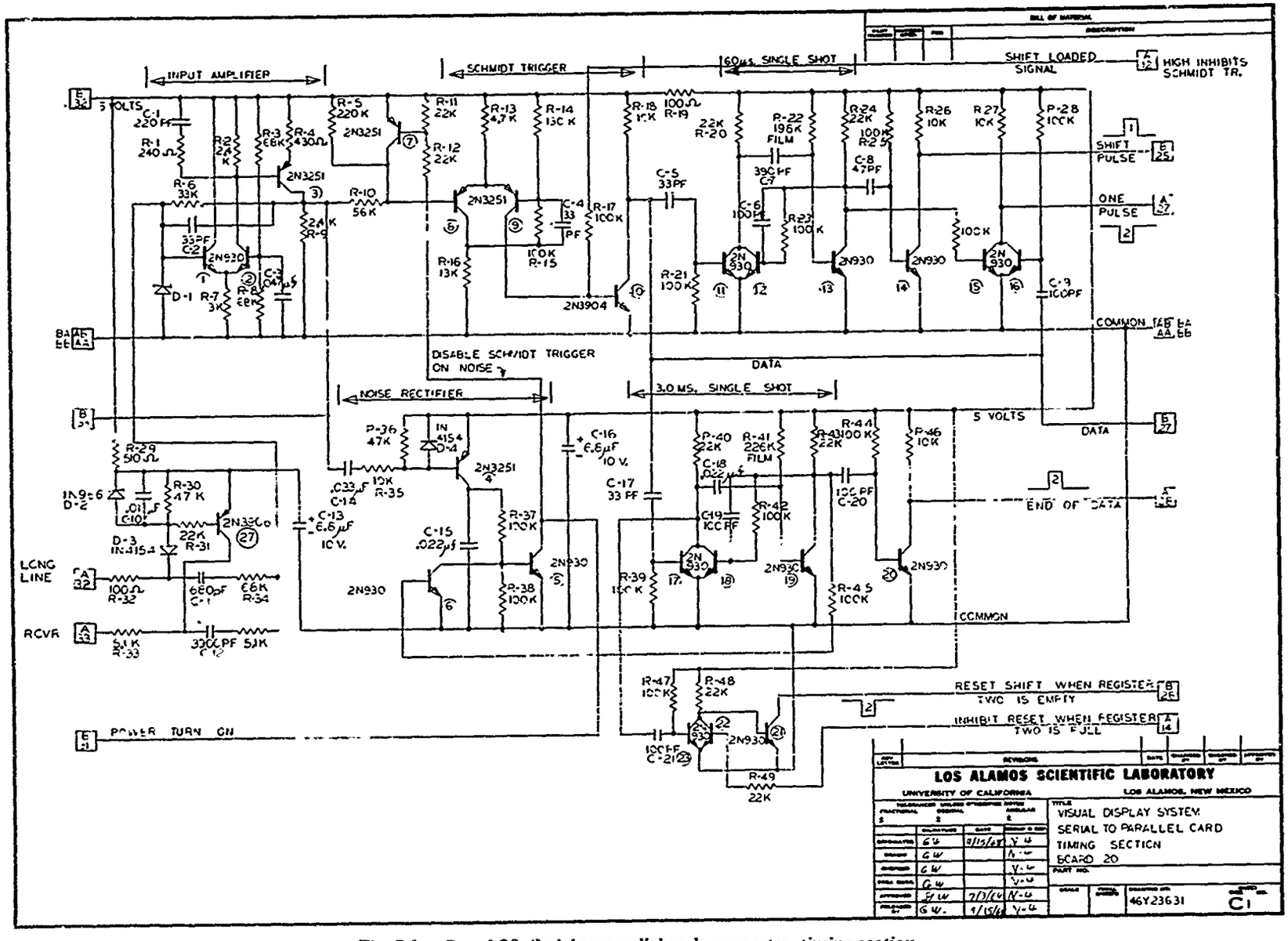


Fig. 7.1a. Board 20. Serial-to-parallel code converter, timing section.

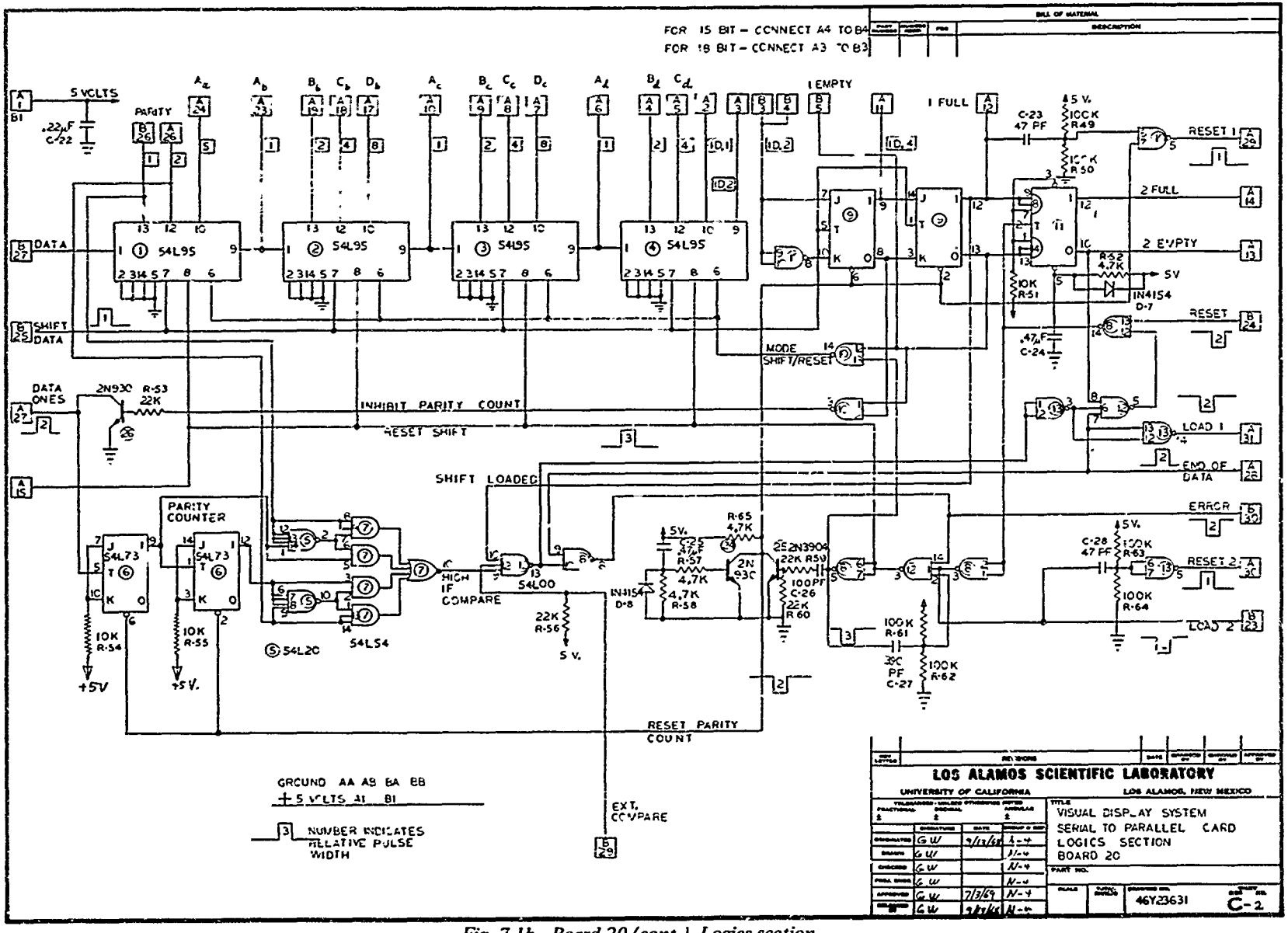


Fig. 7.1b. Board 20 (cont.). Logics section.

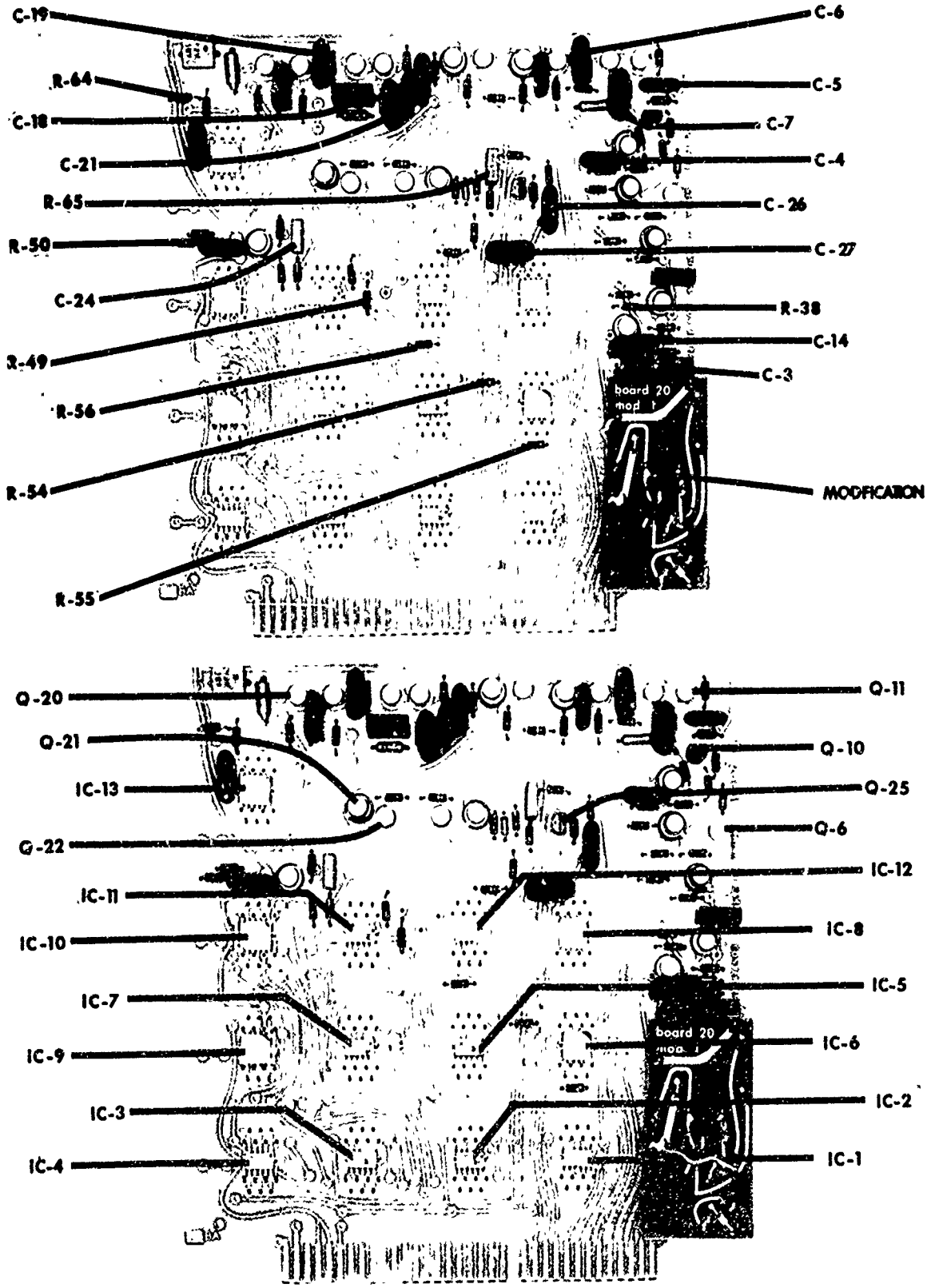


Fig. 7.1c. Board 20 (cont.).

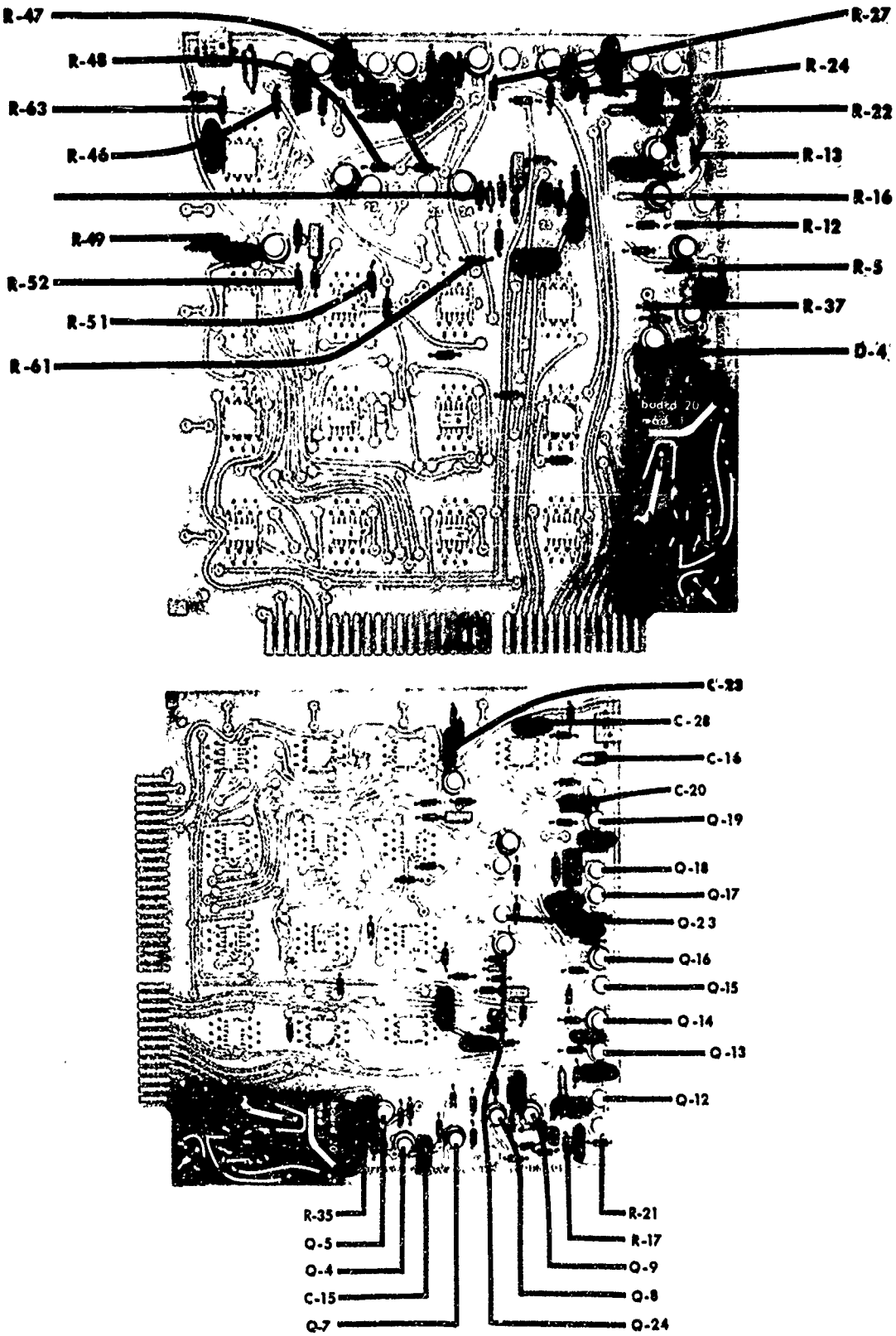


Fig. 7.1d. Bourd 20 (cont.).

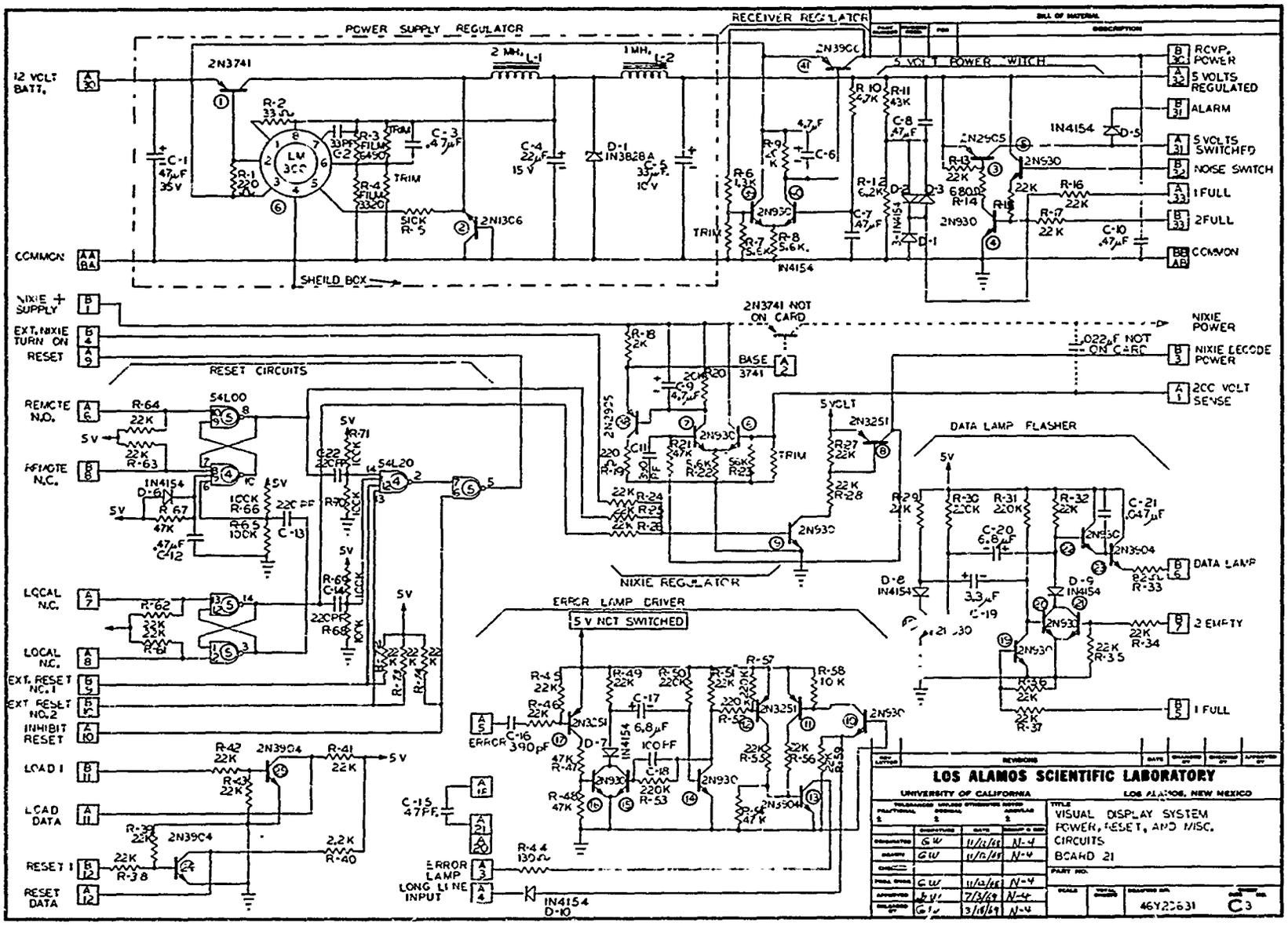


Fig. 7.2a. Board 21. Power, ID store and decode, reset, and miscellaneous circuits.

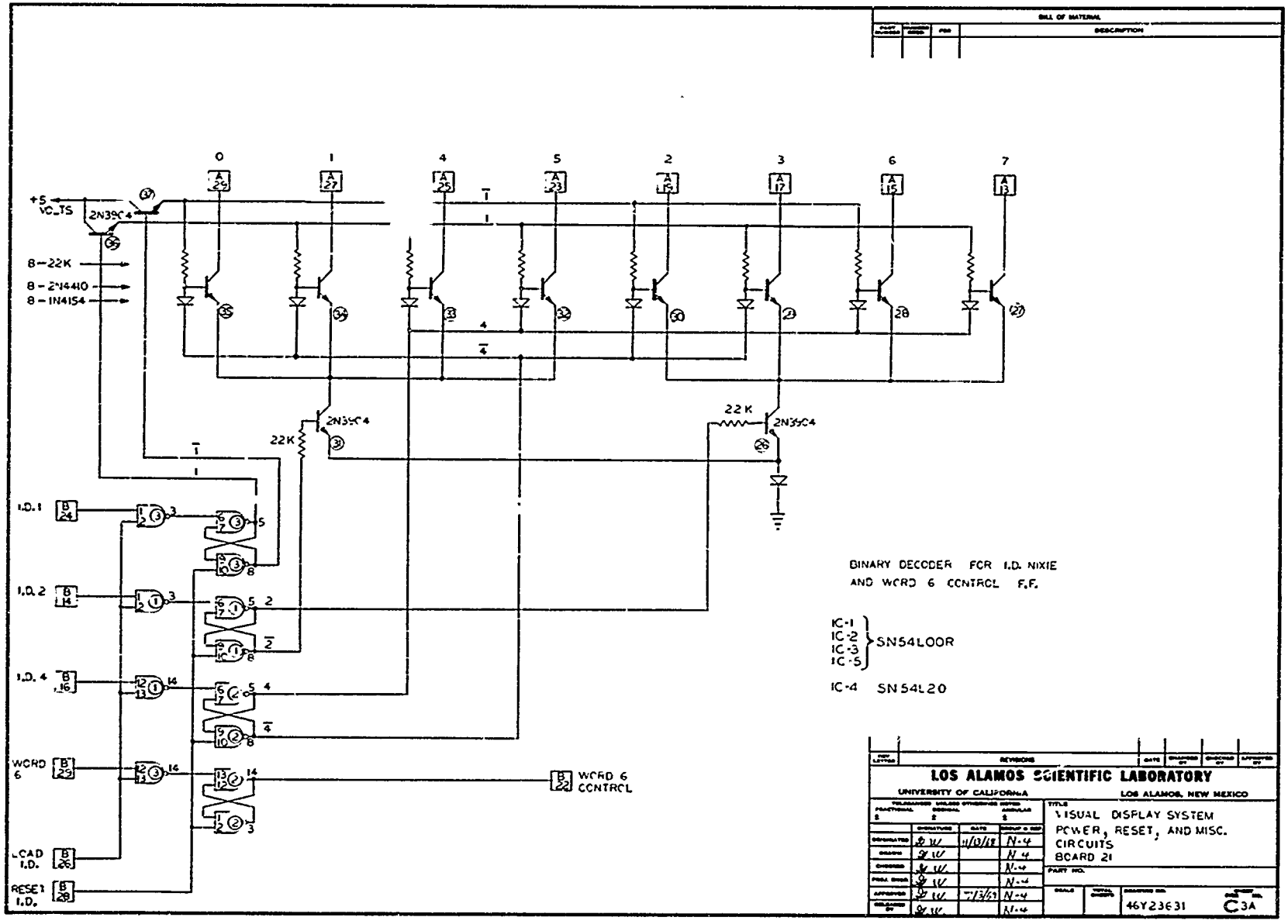


Fig. 7.2b. Board 21 (cont.).

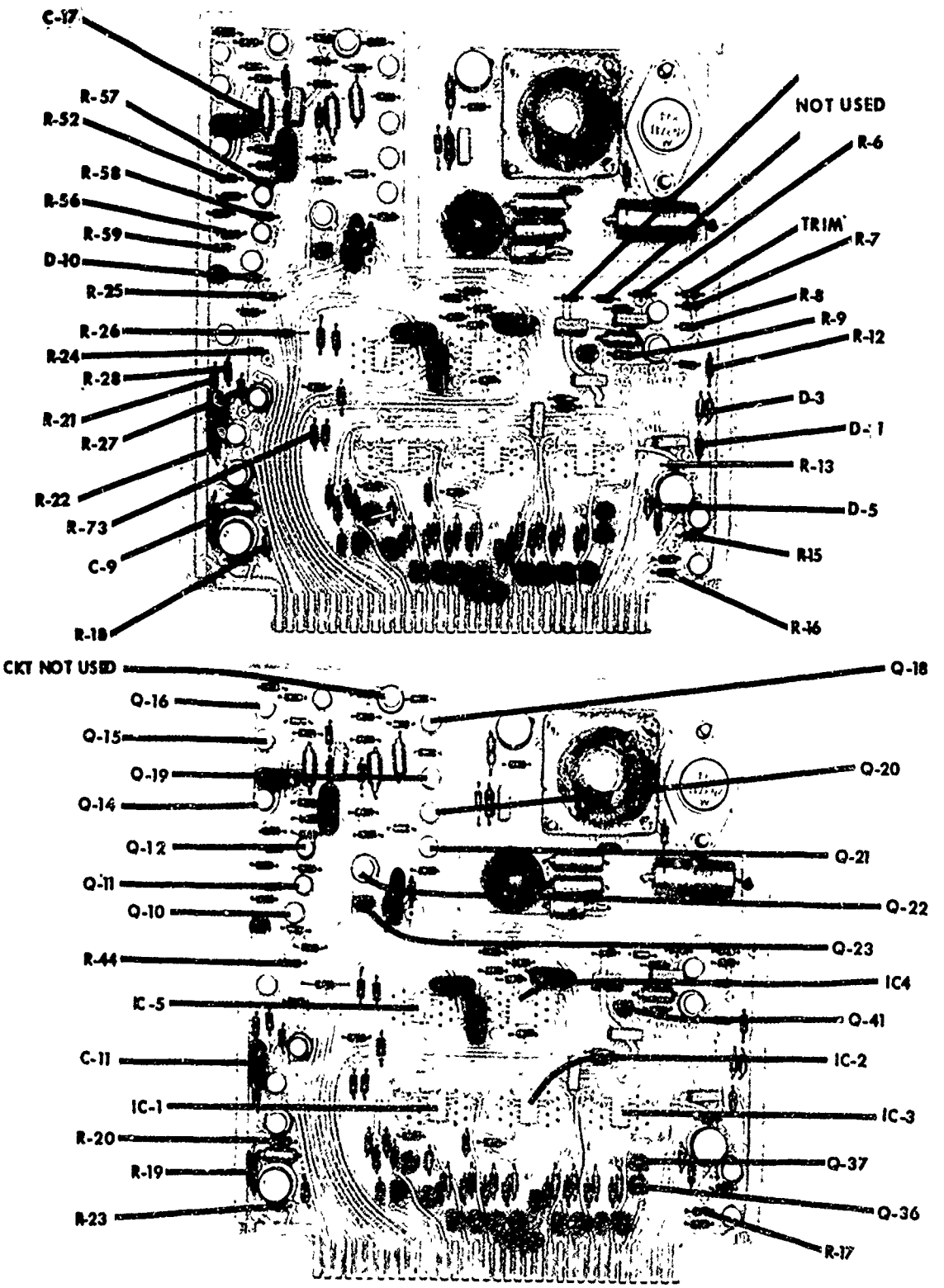


Fig. 7.2c. Board 21 (cont.).

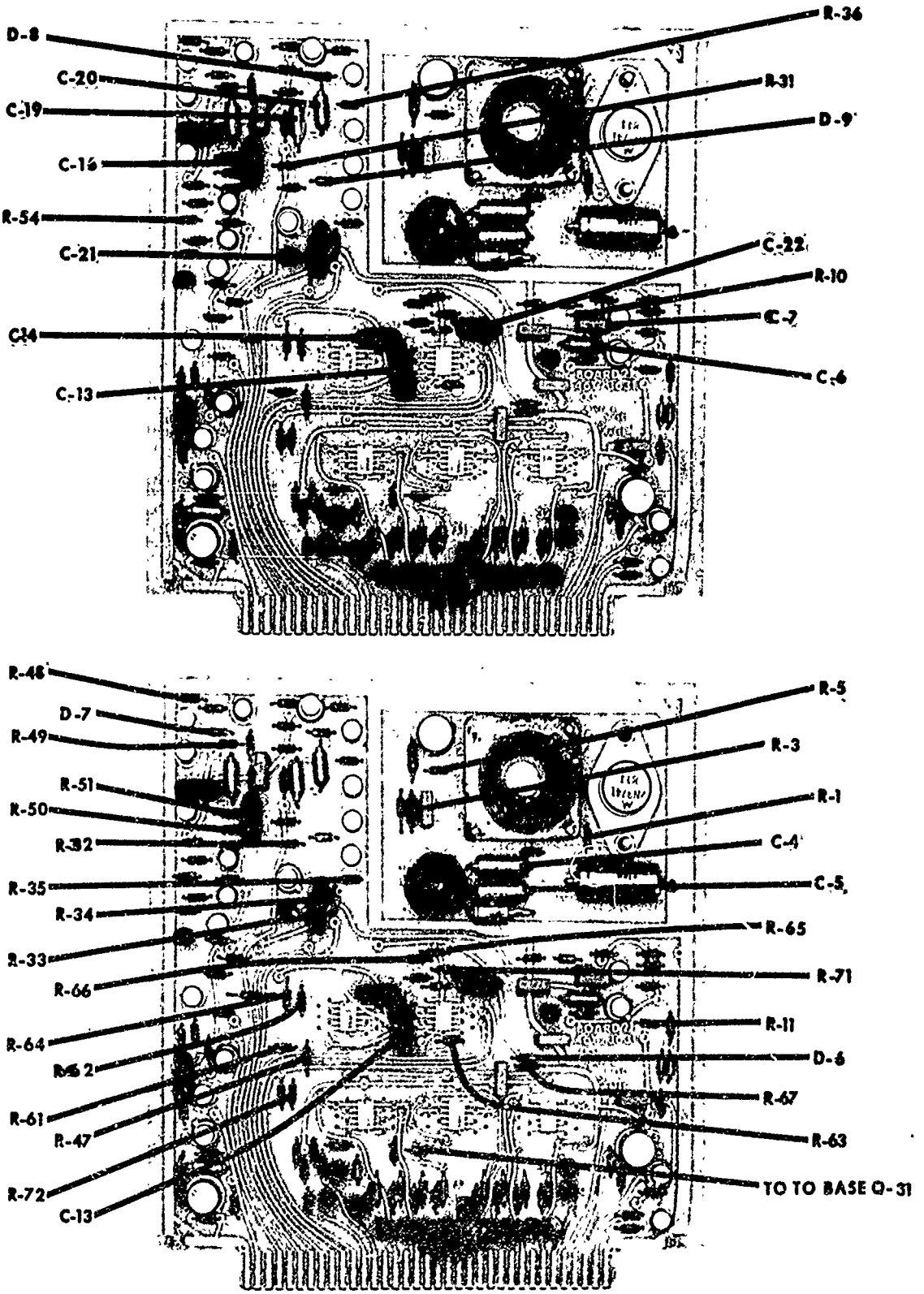


Fig. 7.2d. Board 21 (cont.)

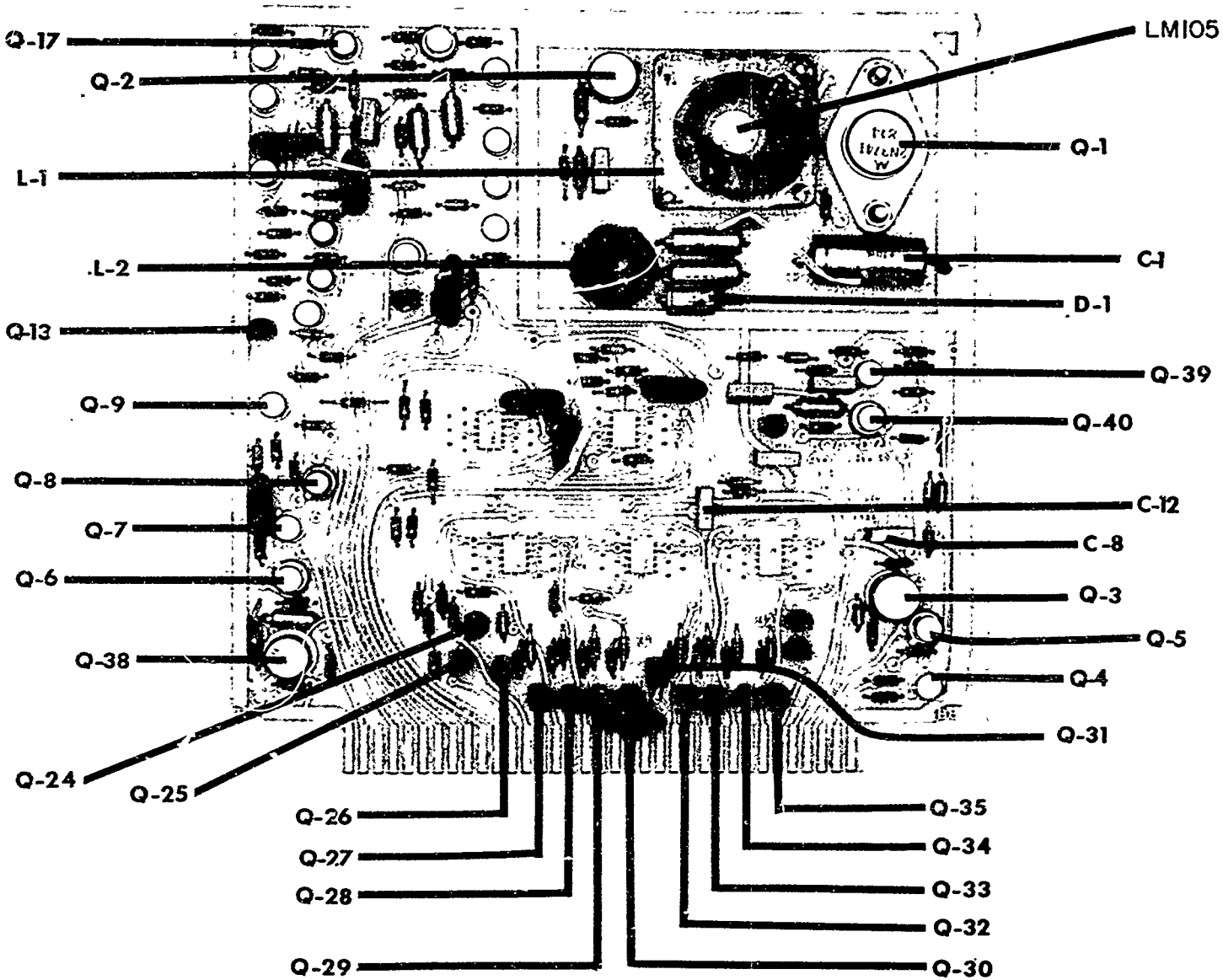


Fig. 7.2e. Board 21 (cont.).

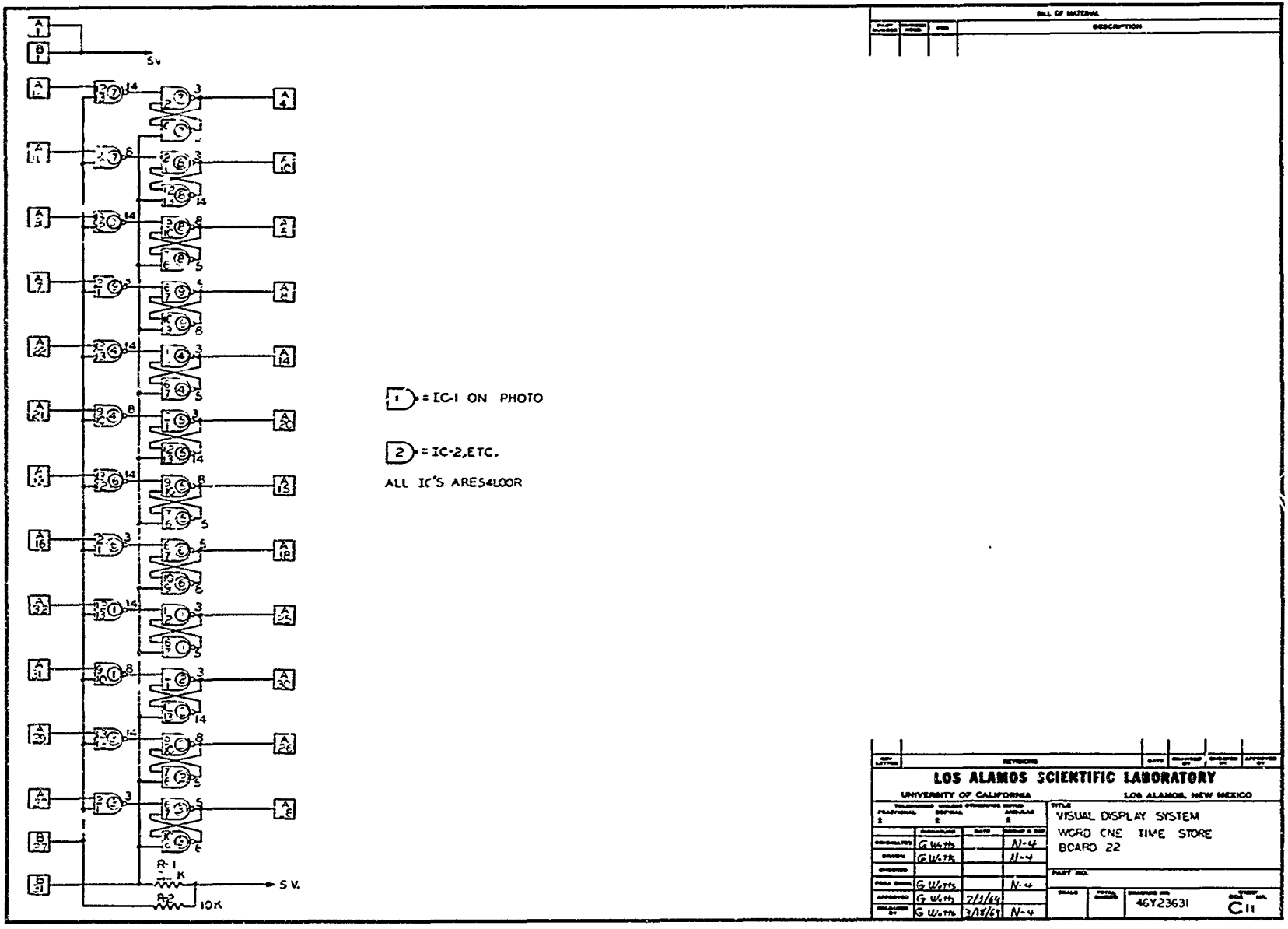


Fig. 7.3a. Board 22. Word-One time store.

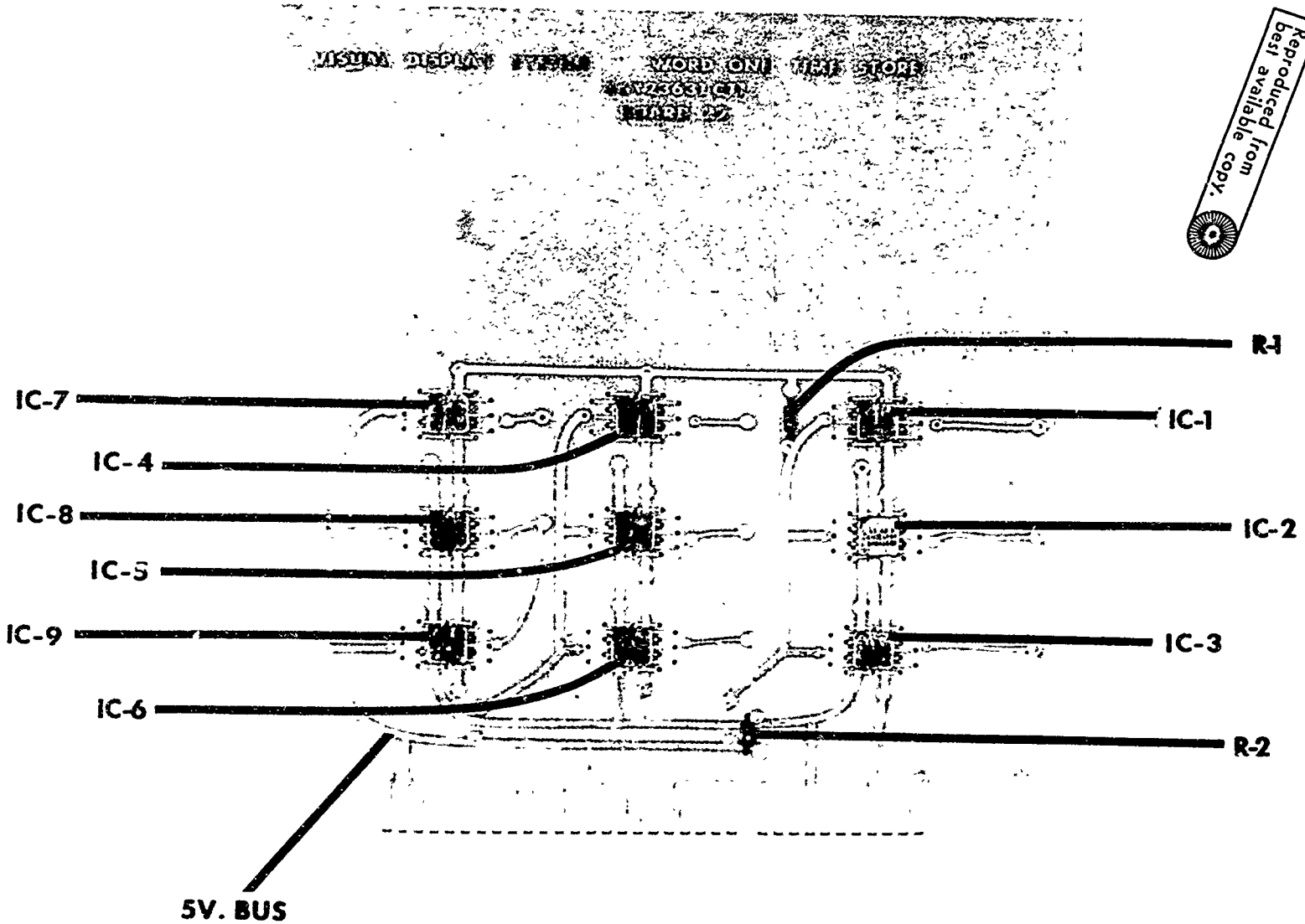


Fig. 7.3b. Board 22 (cont.).

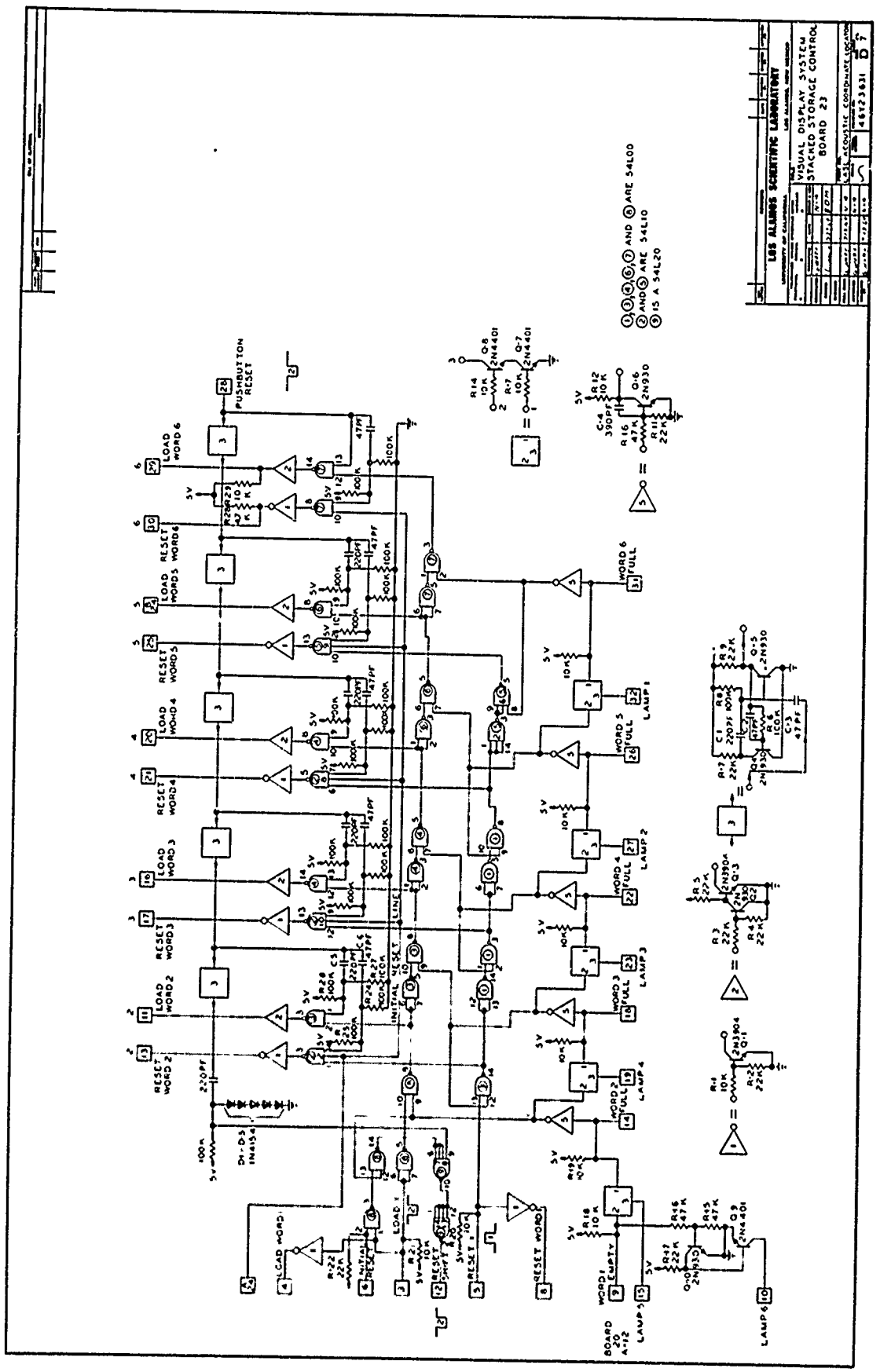


Fig. 7.4a. Board 23. Stacked storage control.

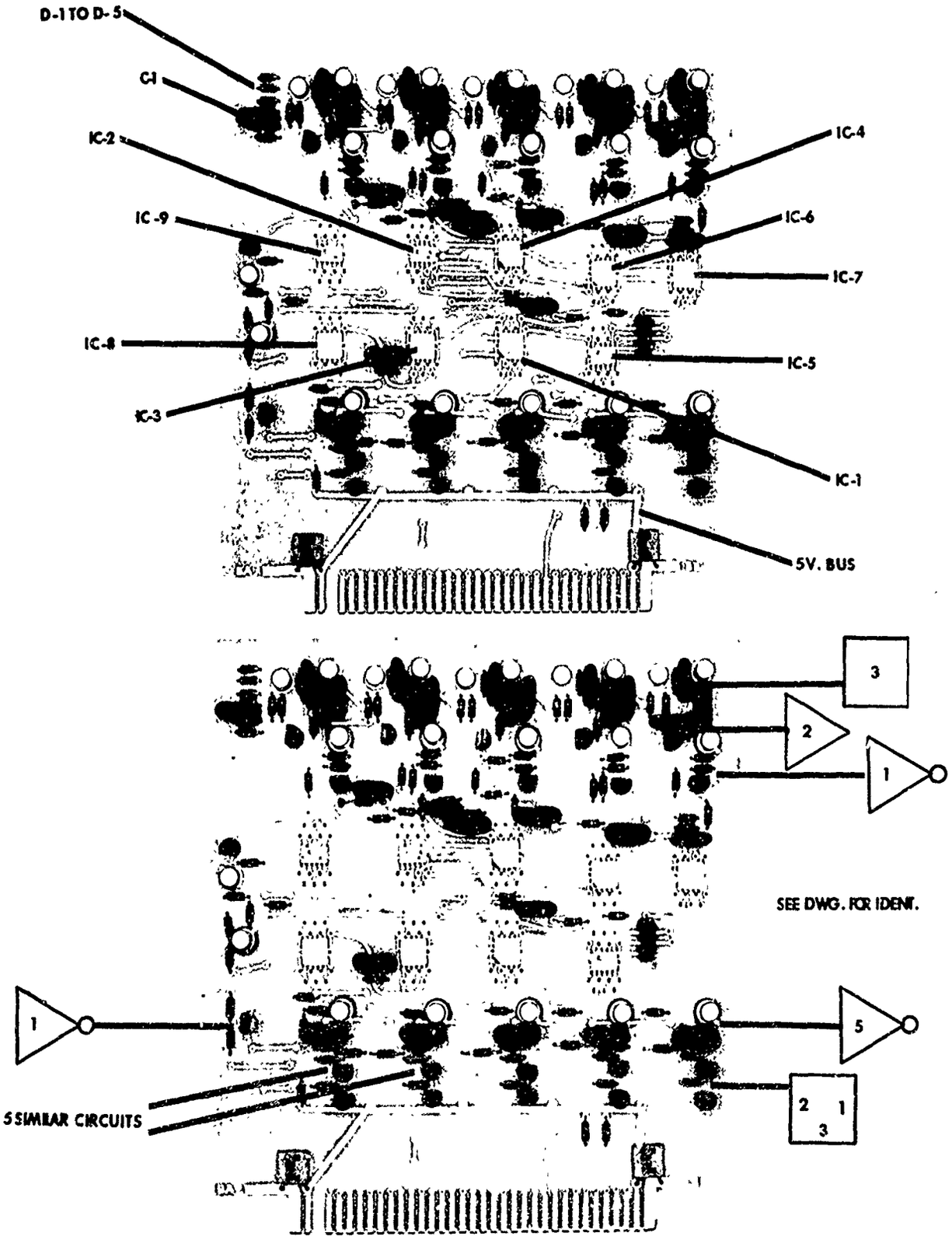


Fig. 7.4b. Board 23 (cont.).

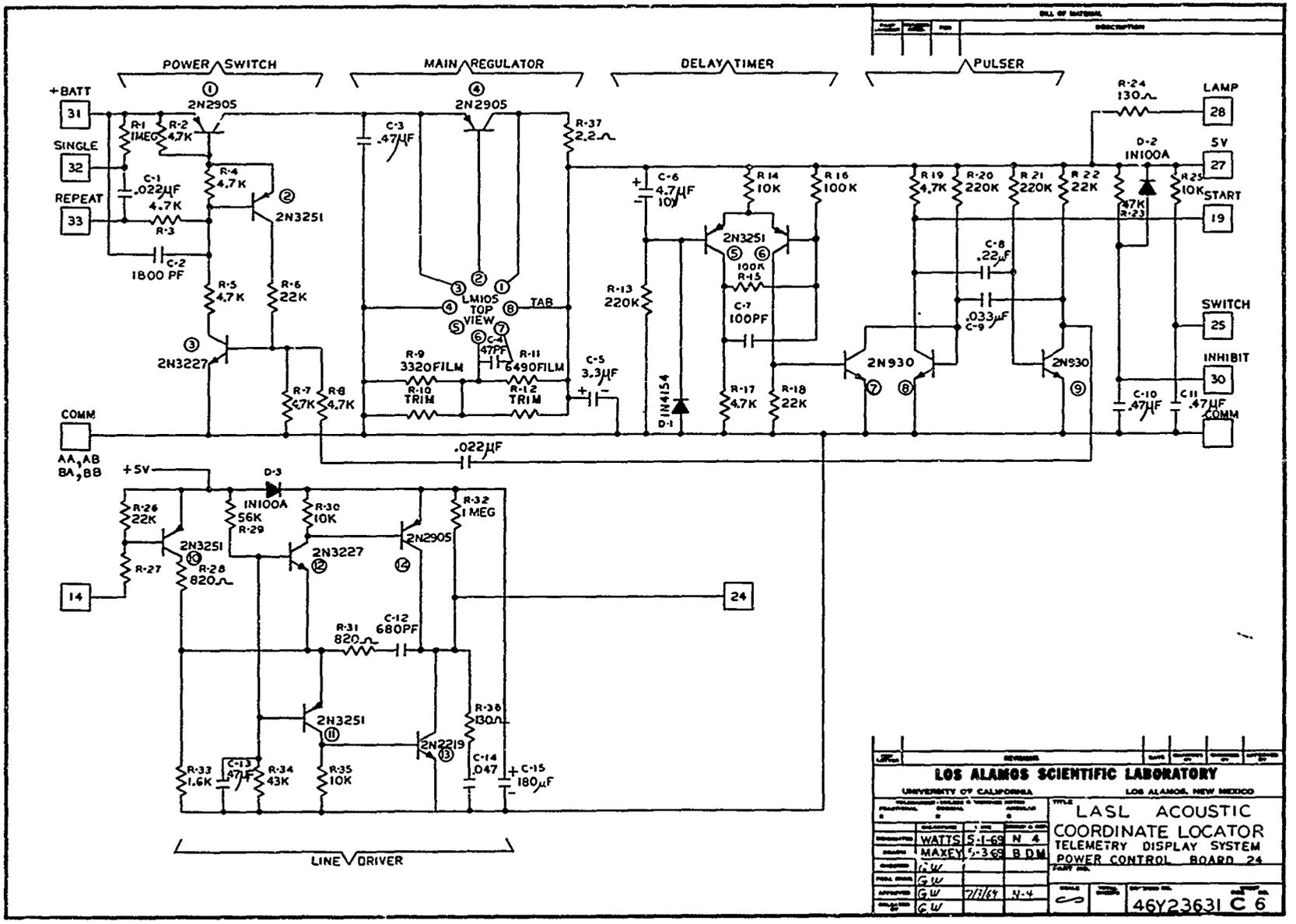
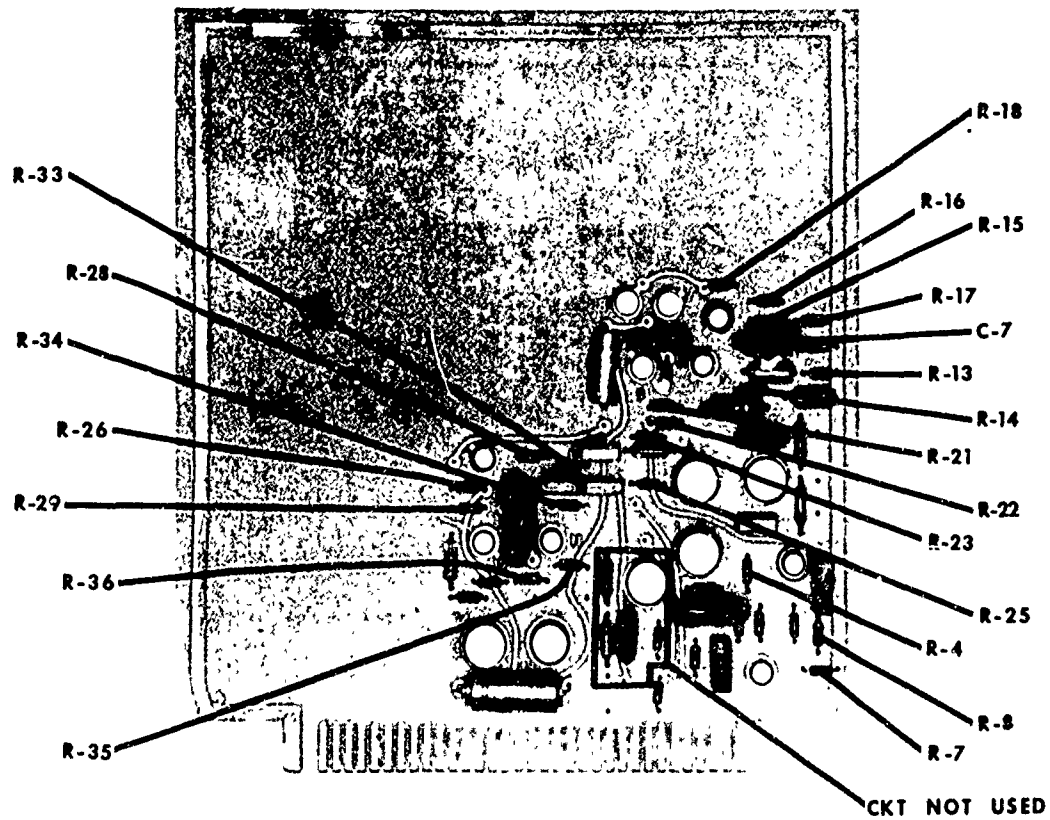


Fig. 7.5a. Board 24. Test code power control and line driver.



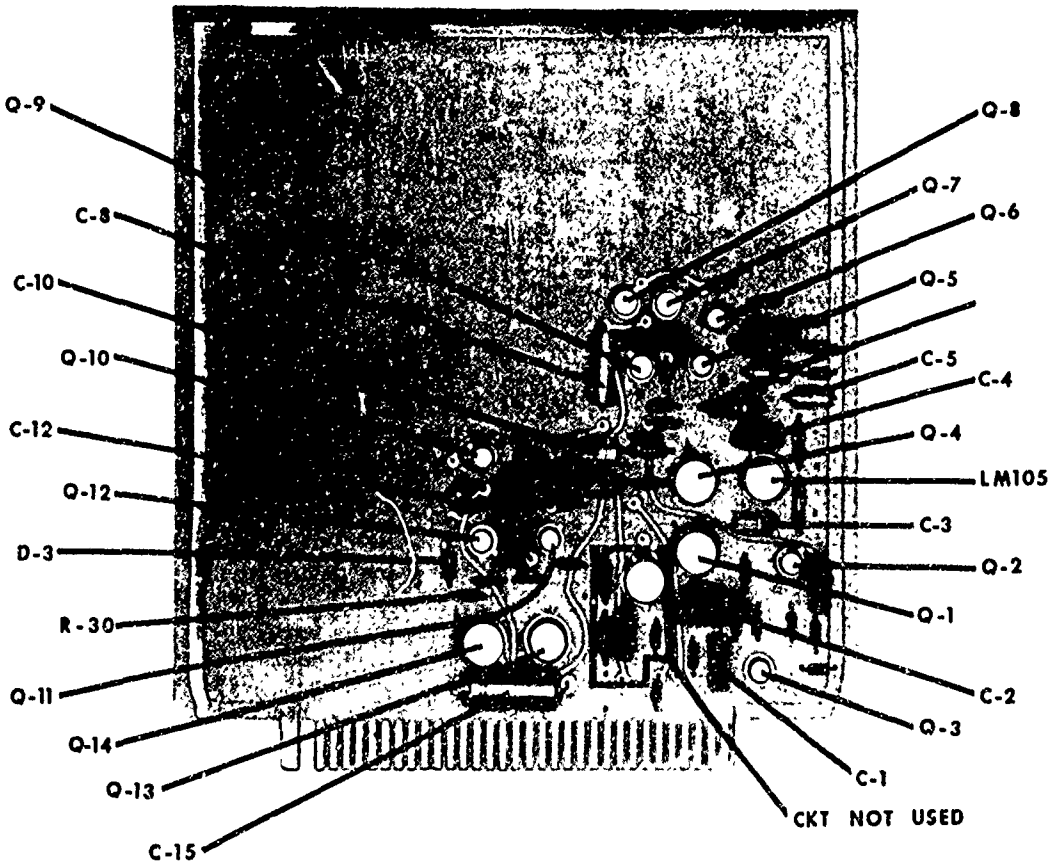


Fig. 7.5b. Board 24 (cont.).

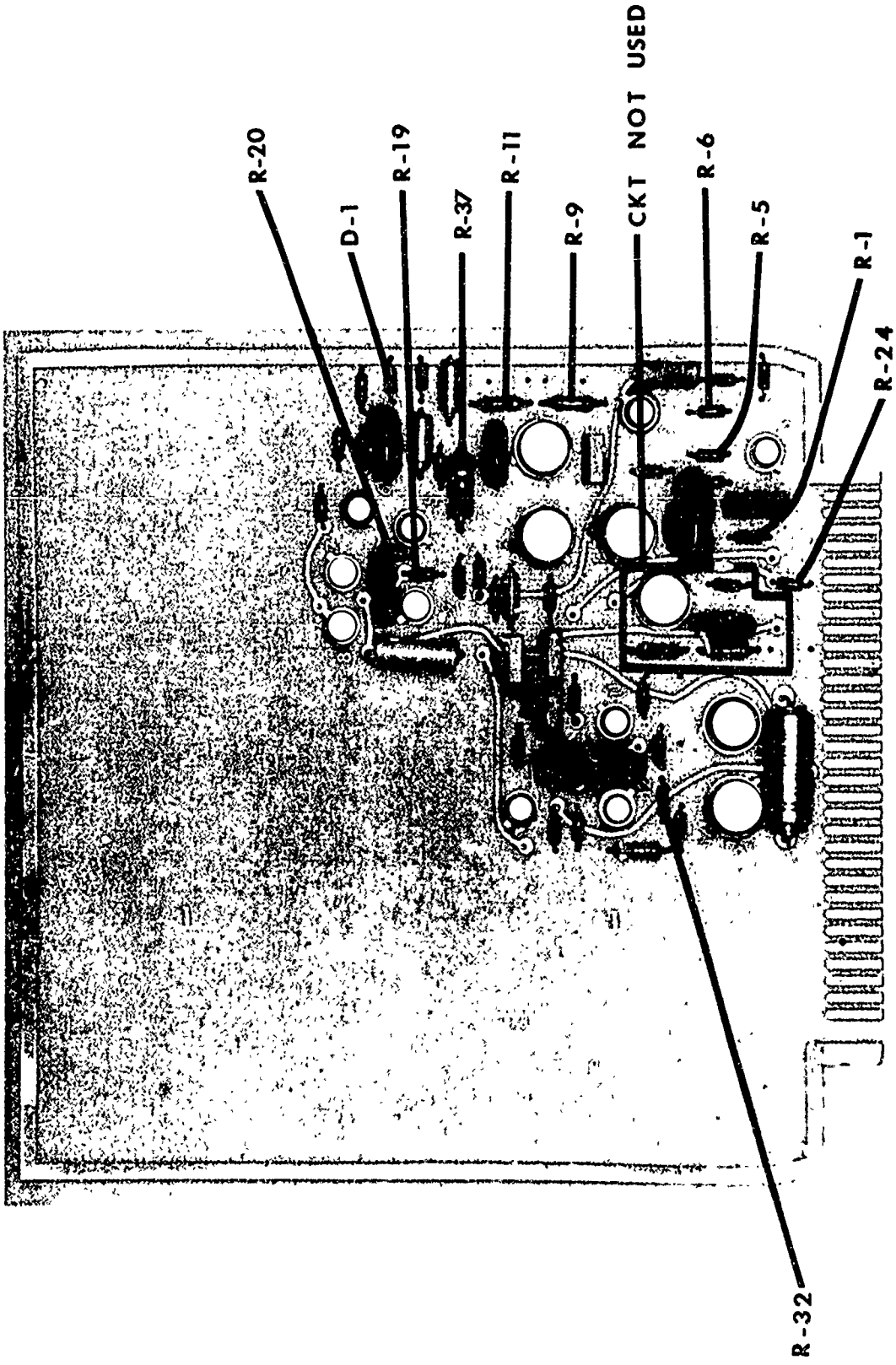


Fig. 7.5c. Board 24 (cont.).

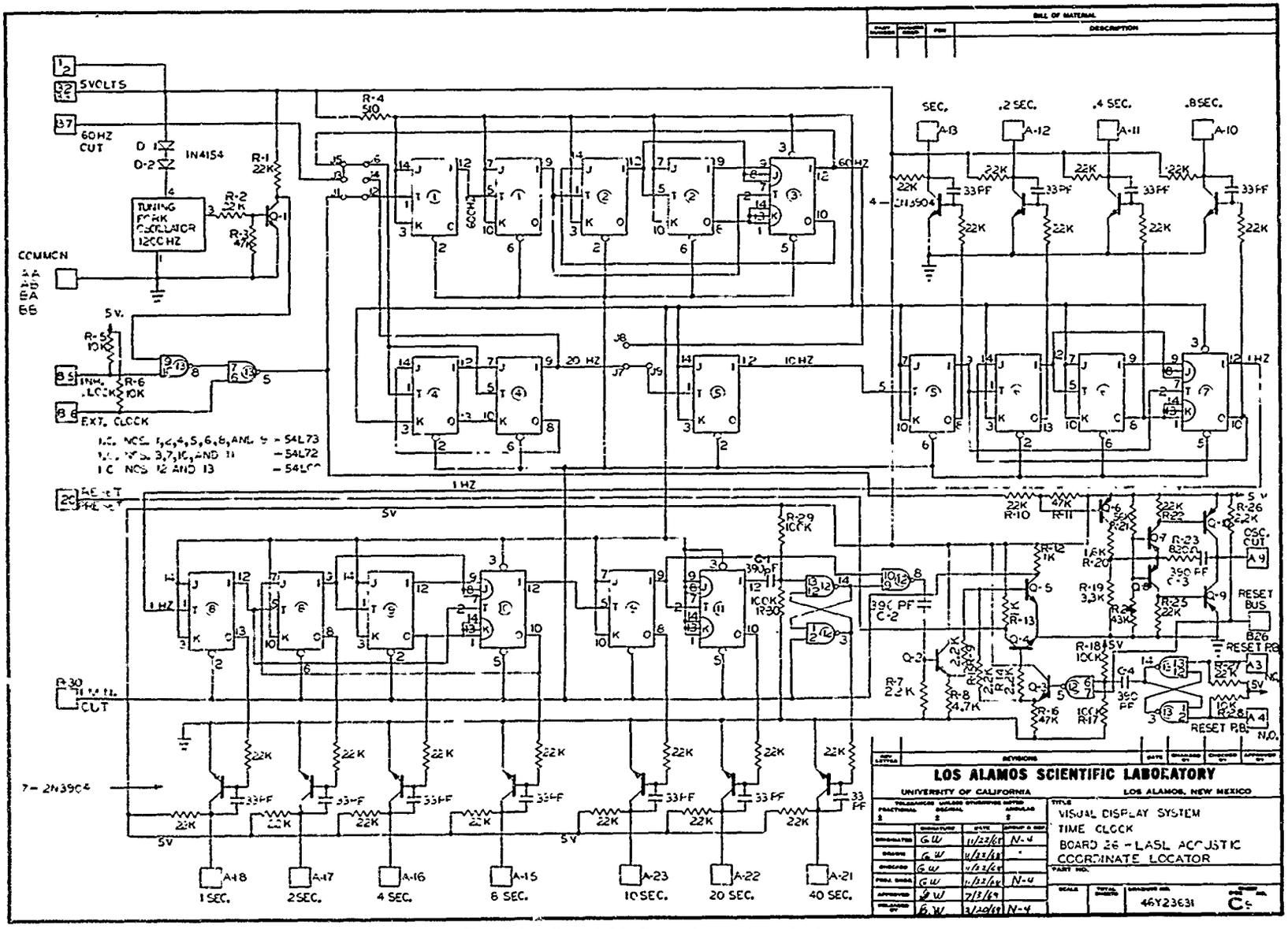


Fig. 7.6a. Board 26. One-minute time clock.

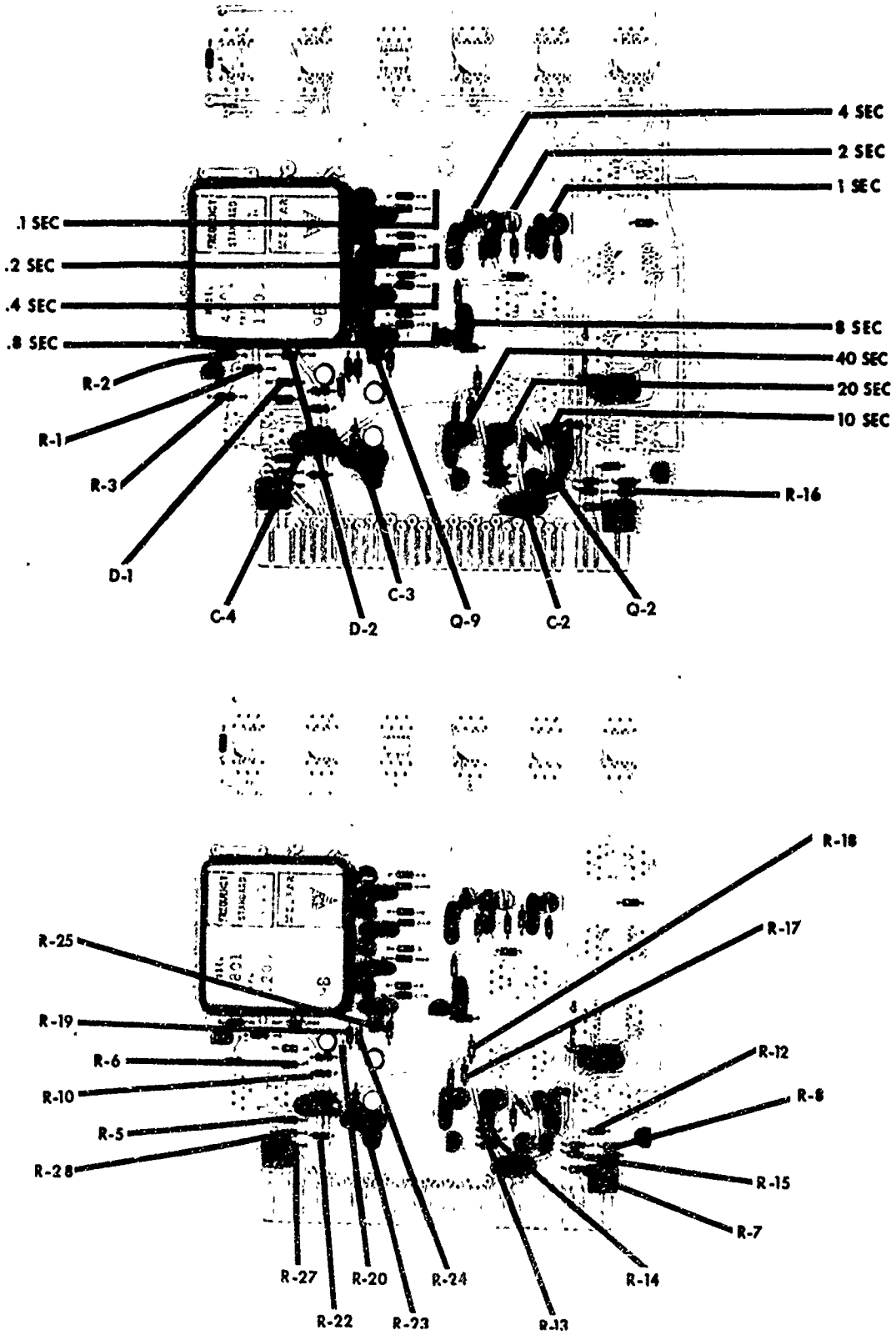


Fig. 7.6b. Board 26 (cont.).

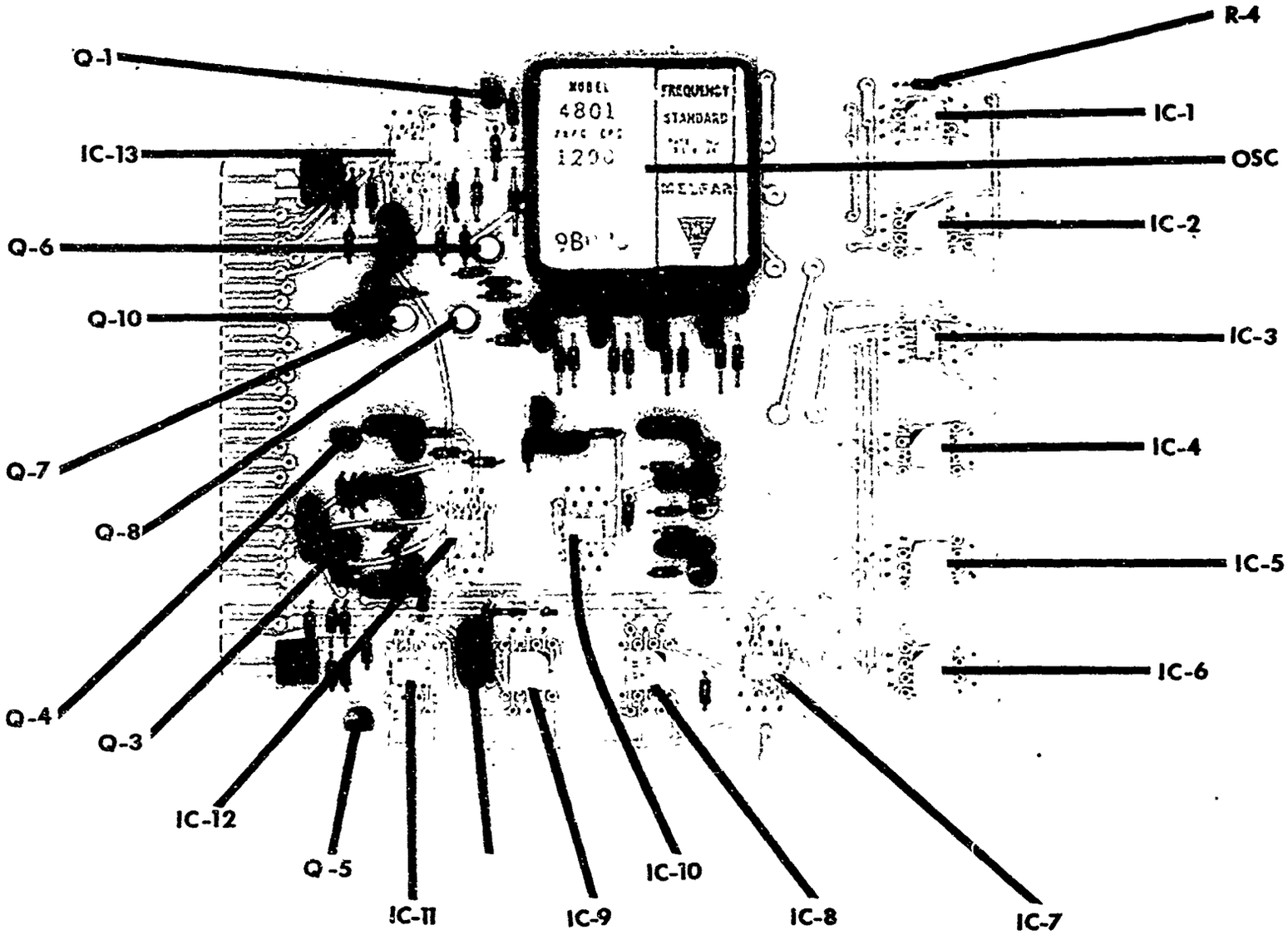


Fig. 7.6c. Board 26 (cont.).

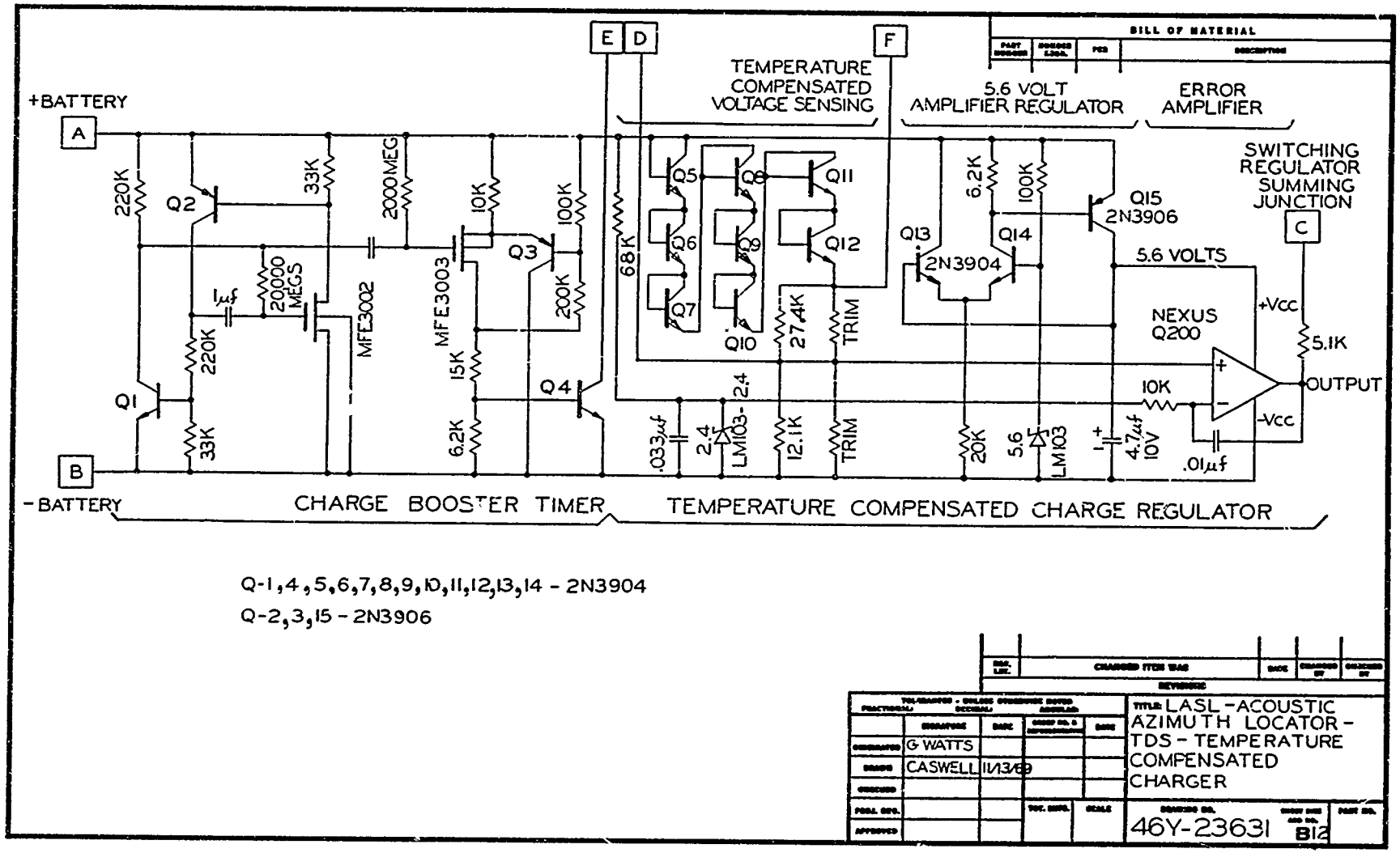


Fig. 7.7. Board 27. Temperature-compensated battery charger control.

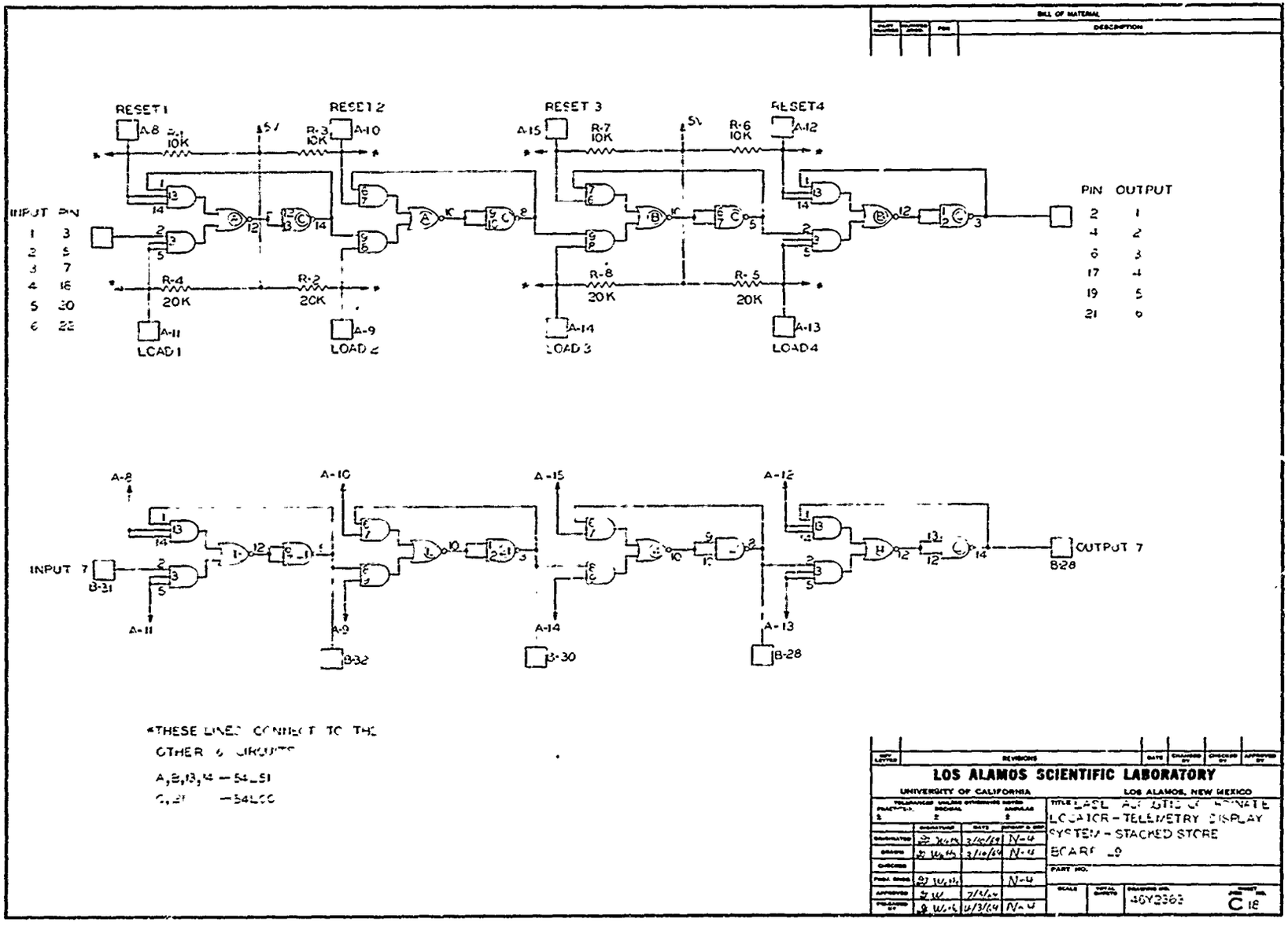


Fig. 7.8a. Board 29. Stacked storage.

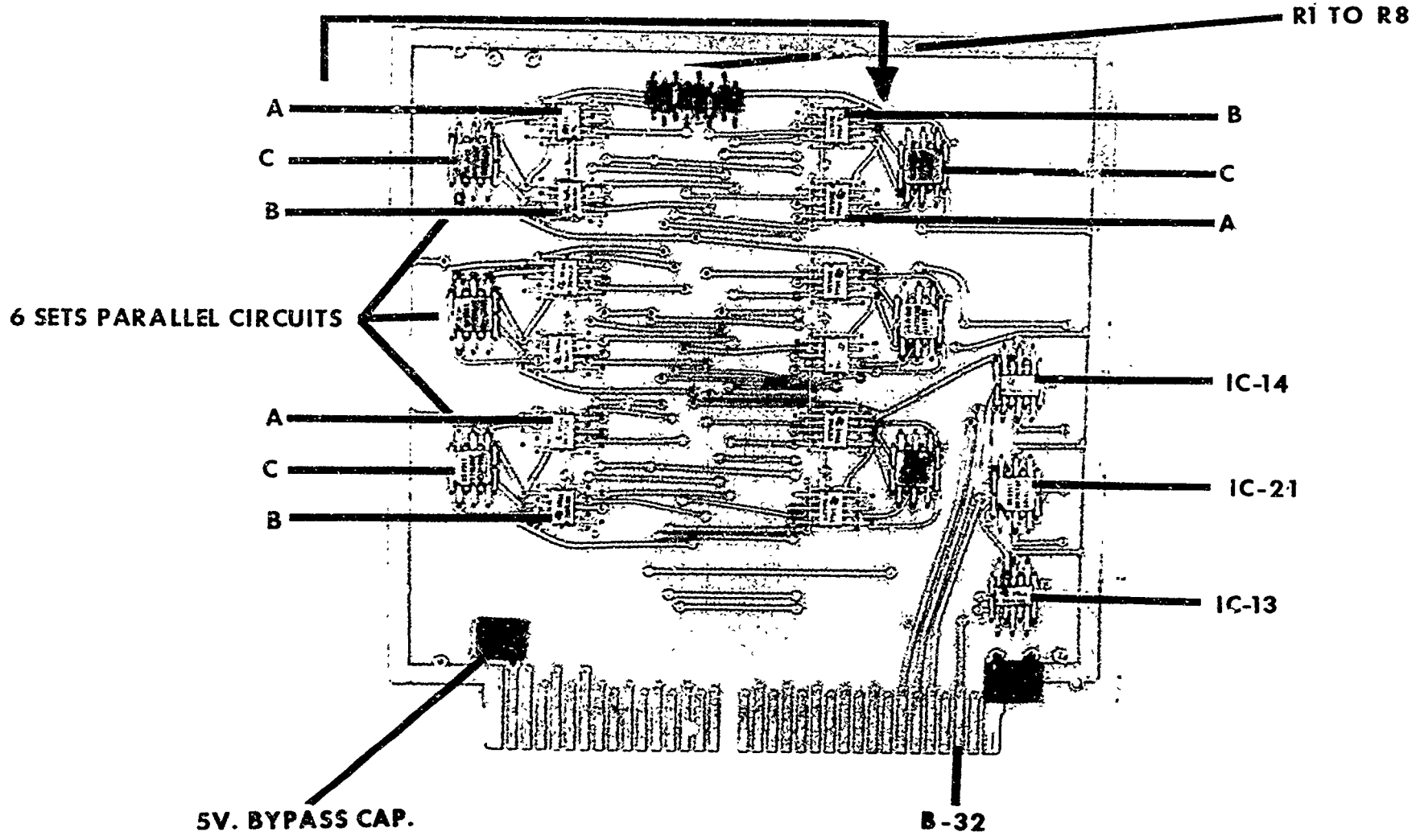


Fig. 7.8b. Board 29 (cont.).

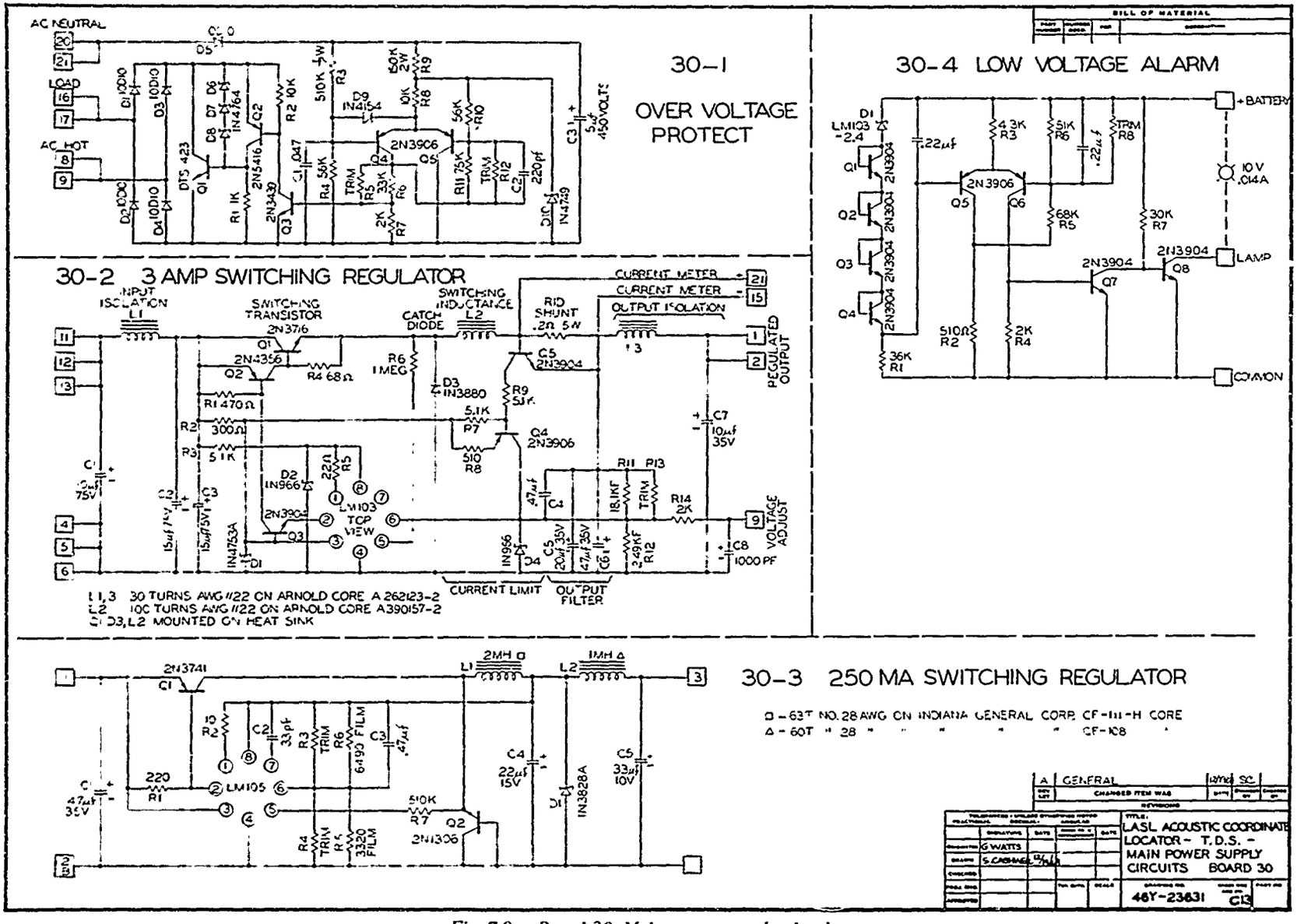


Fig. 7.9a. Board 30. Main power supply circuits.

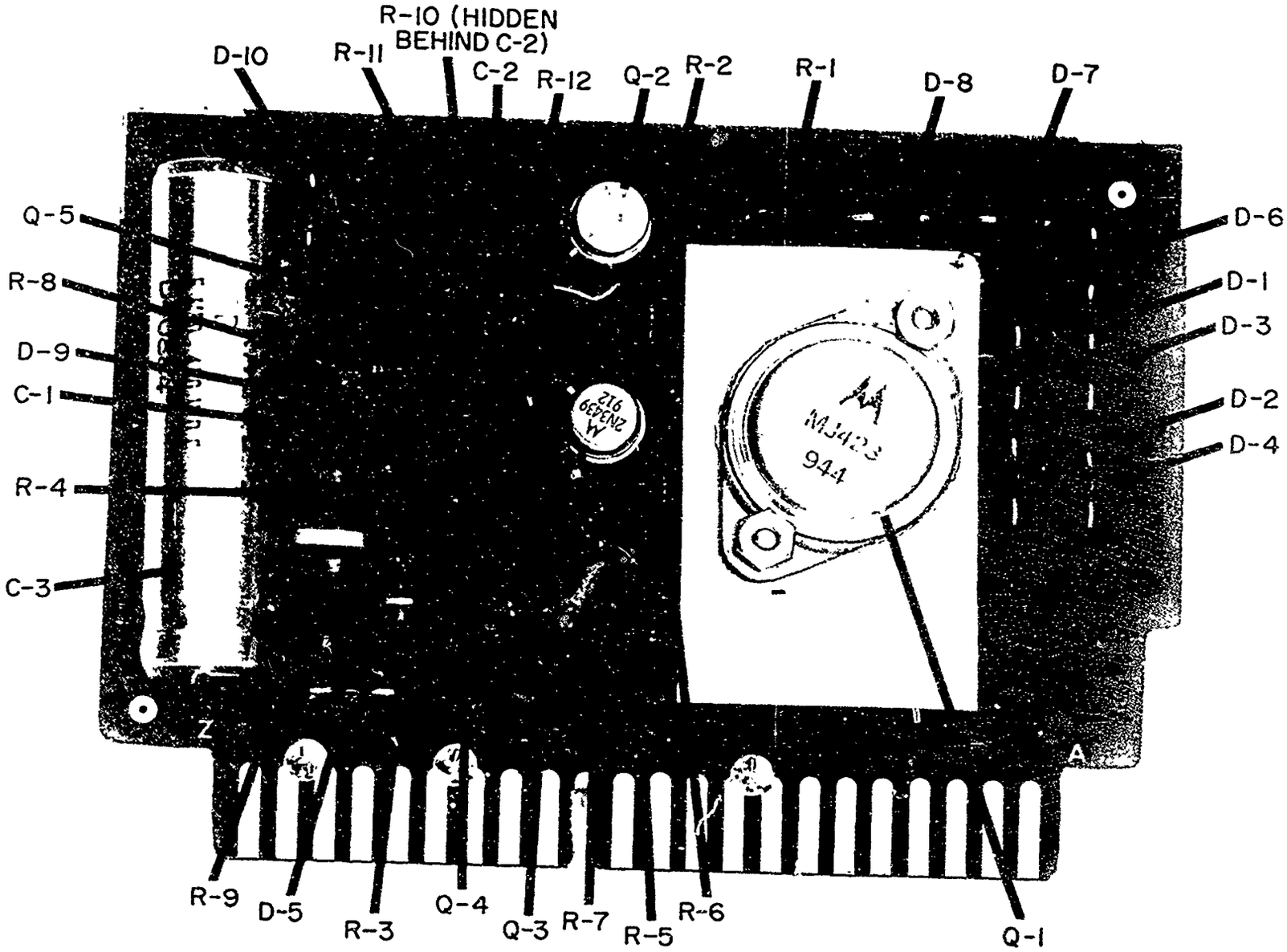


Fig. 7.9b. Board 30 (cont.). Board 30-1. Overvoltage protection circuit.

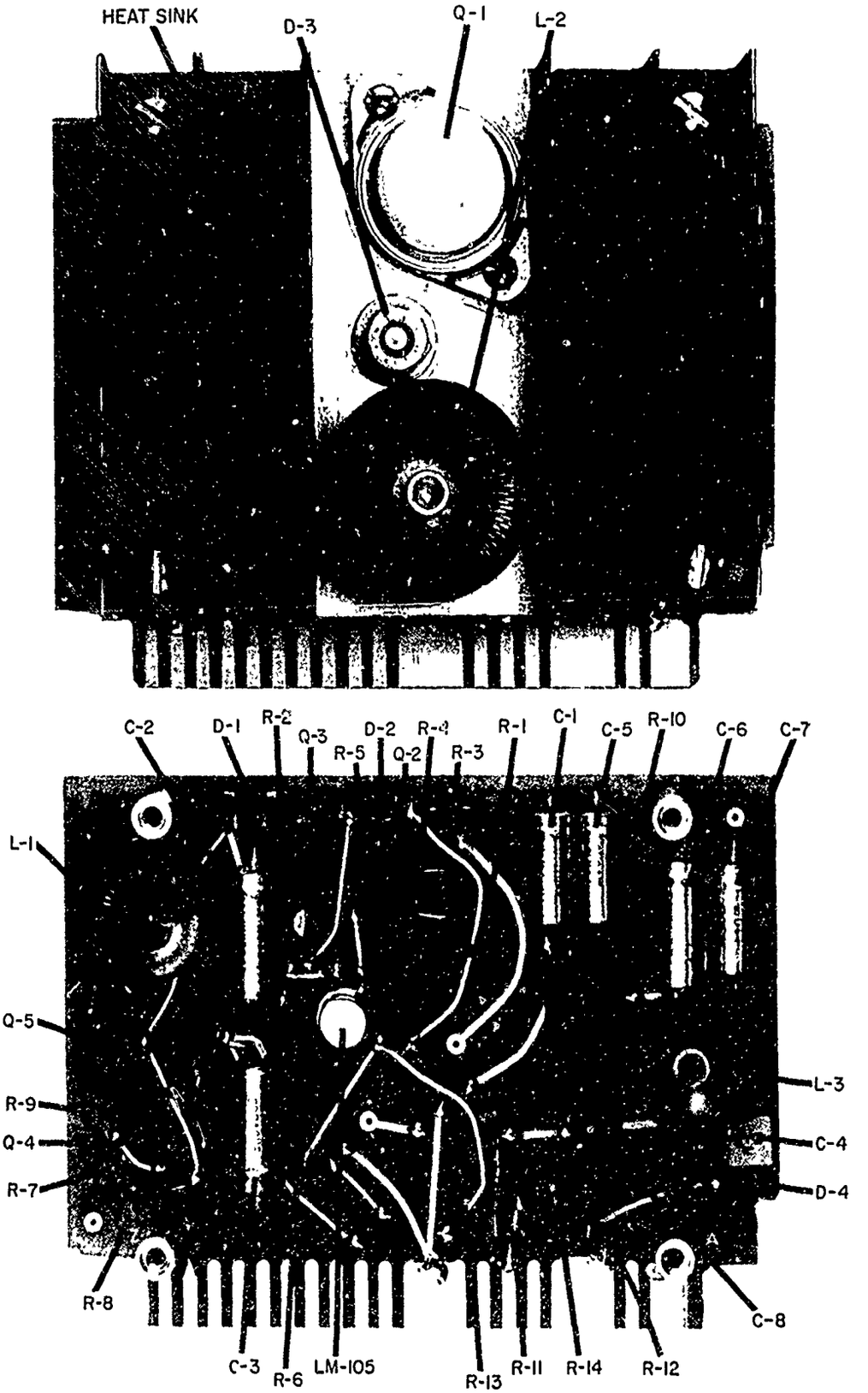


Fig. 7.9c. Board 30 (cont.). Board 30-2. 3-ampere switching regulator (bottom, heat sink removed).

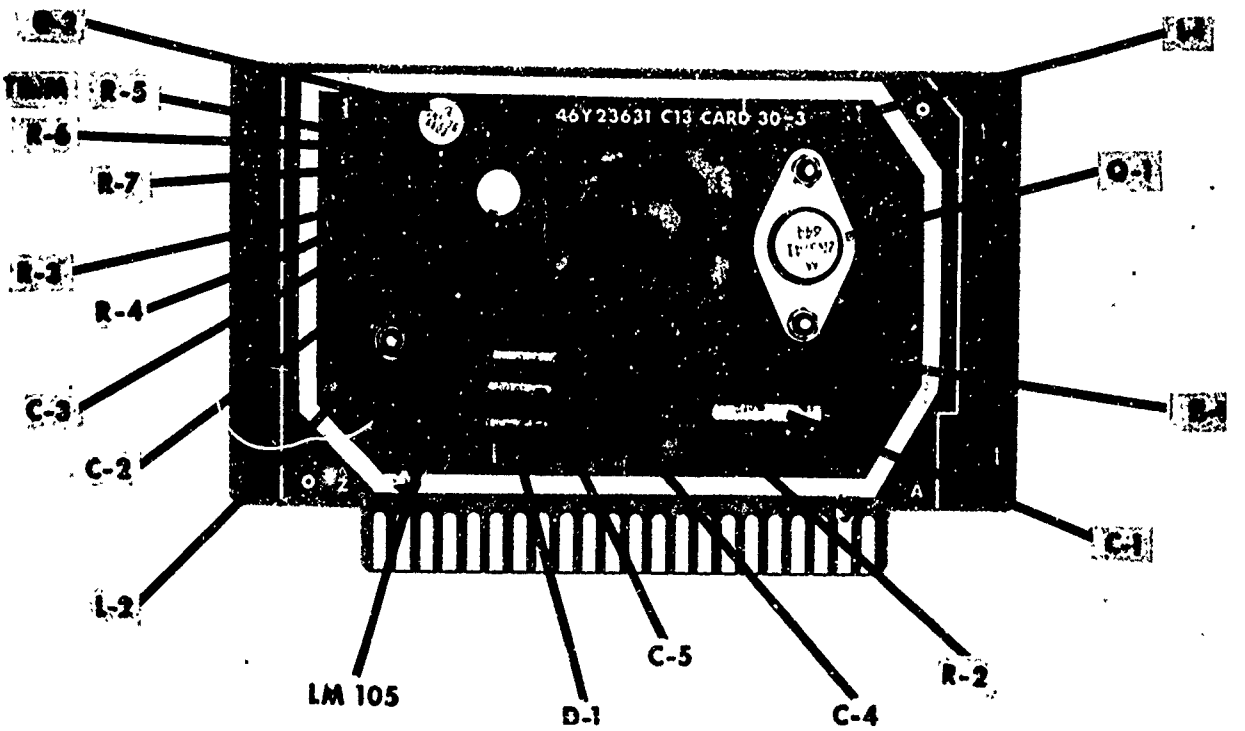


Fig. 7.9d. Board 30 (cont.). Board 30-3. 350-mA switching regulator.

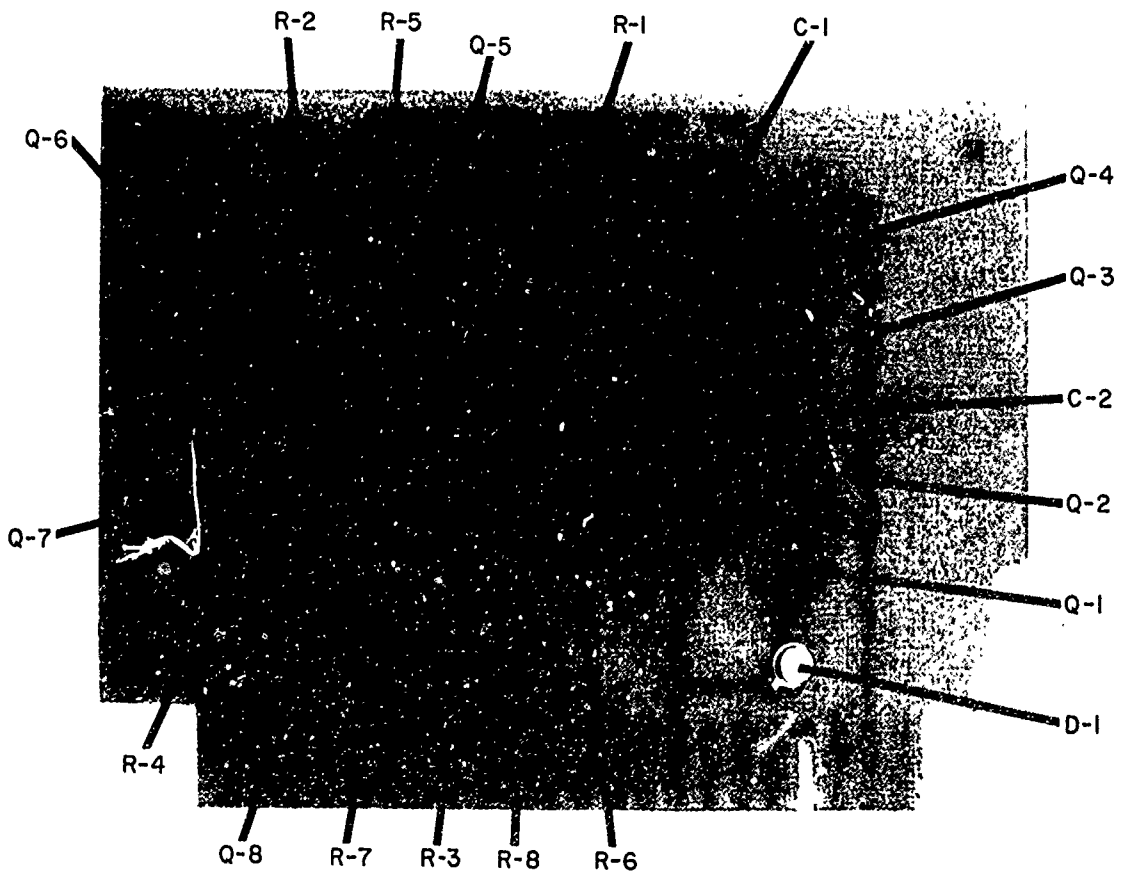


Fig. 7.9e. Board 30 (cont.). Board 30-4. Low-voltage alarm.

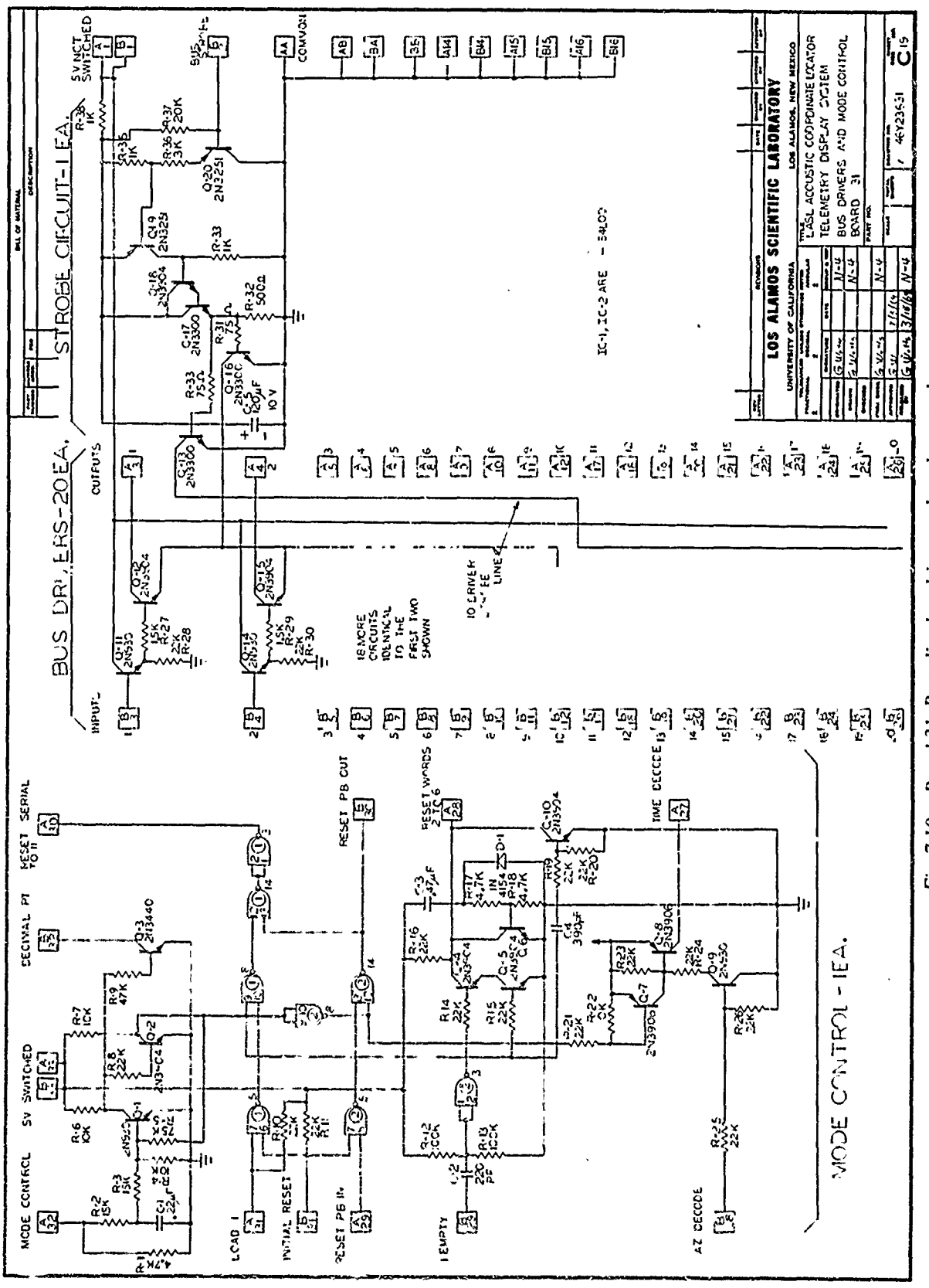


Fig. 7.10a. Board 31. Party-line bus drivers and mode control.

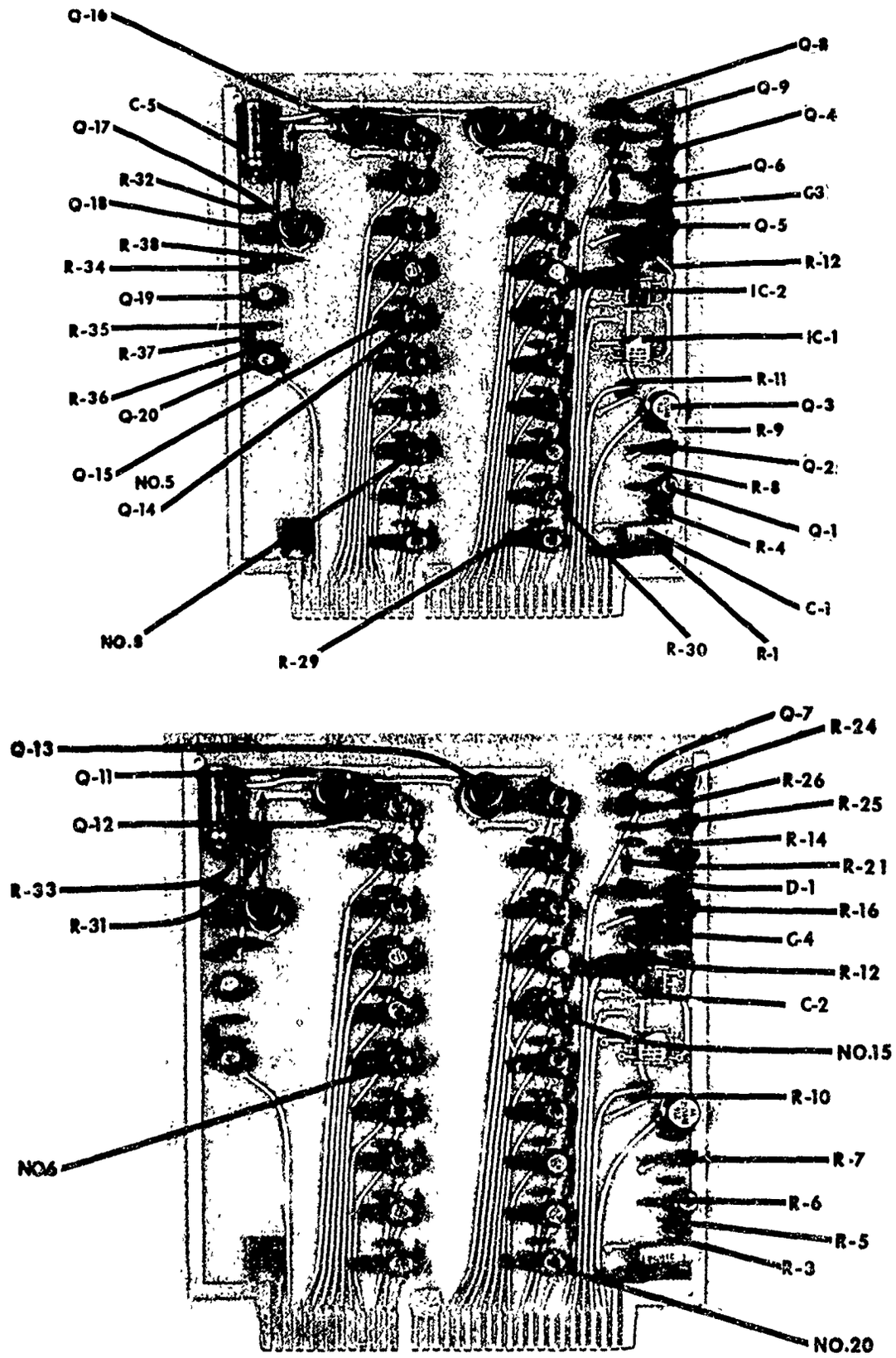


Fig. 7.10b. Board 31 (cont.).

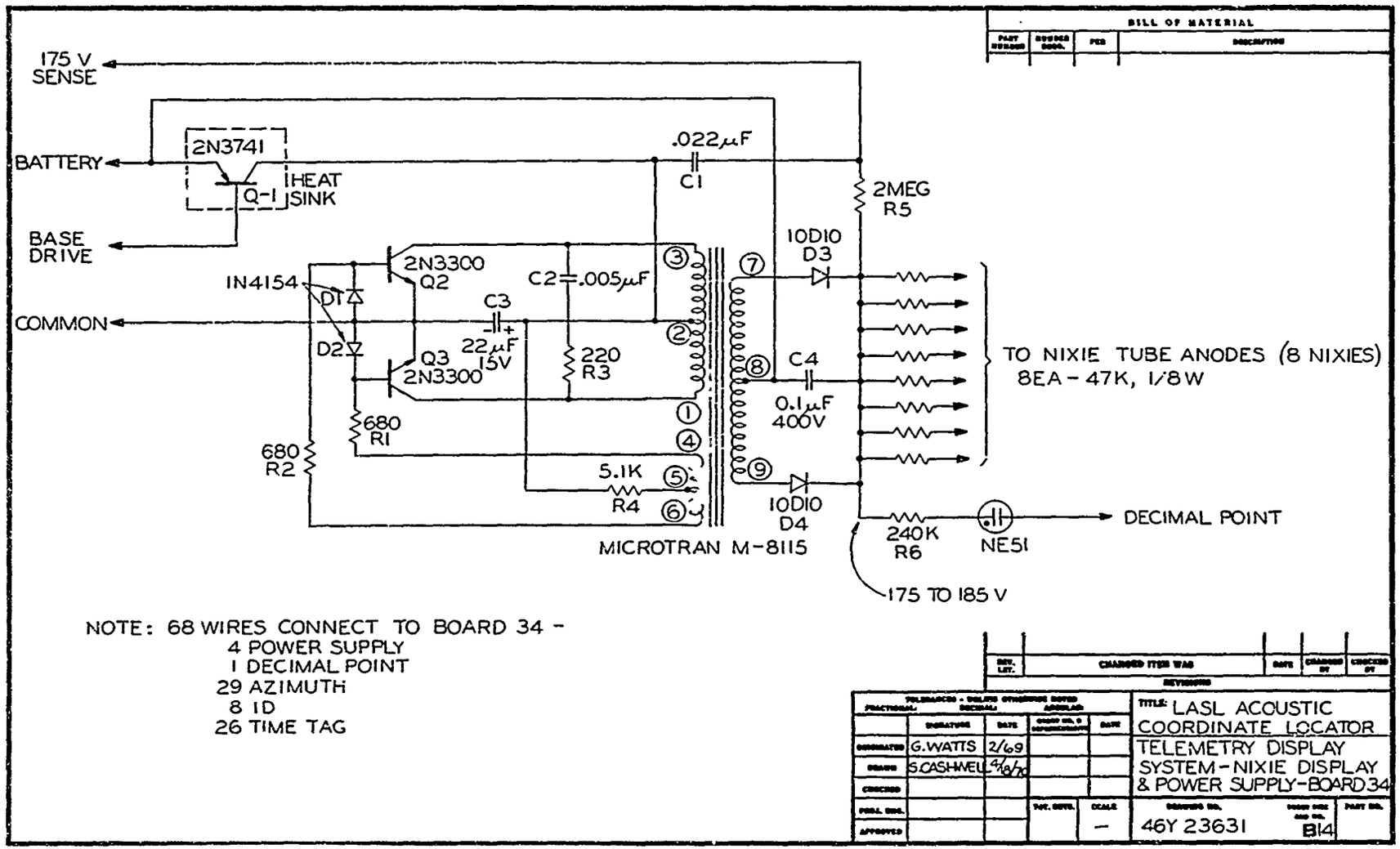


Fig. 7.11a. Board 34. NIXIE display and power supply.

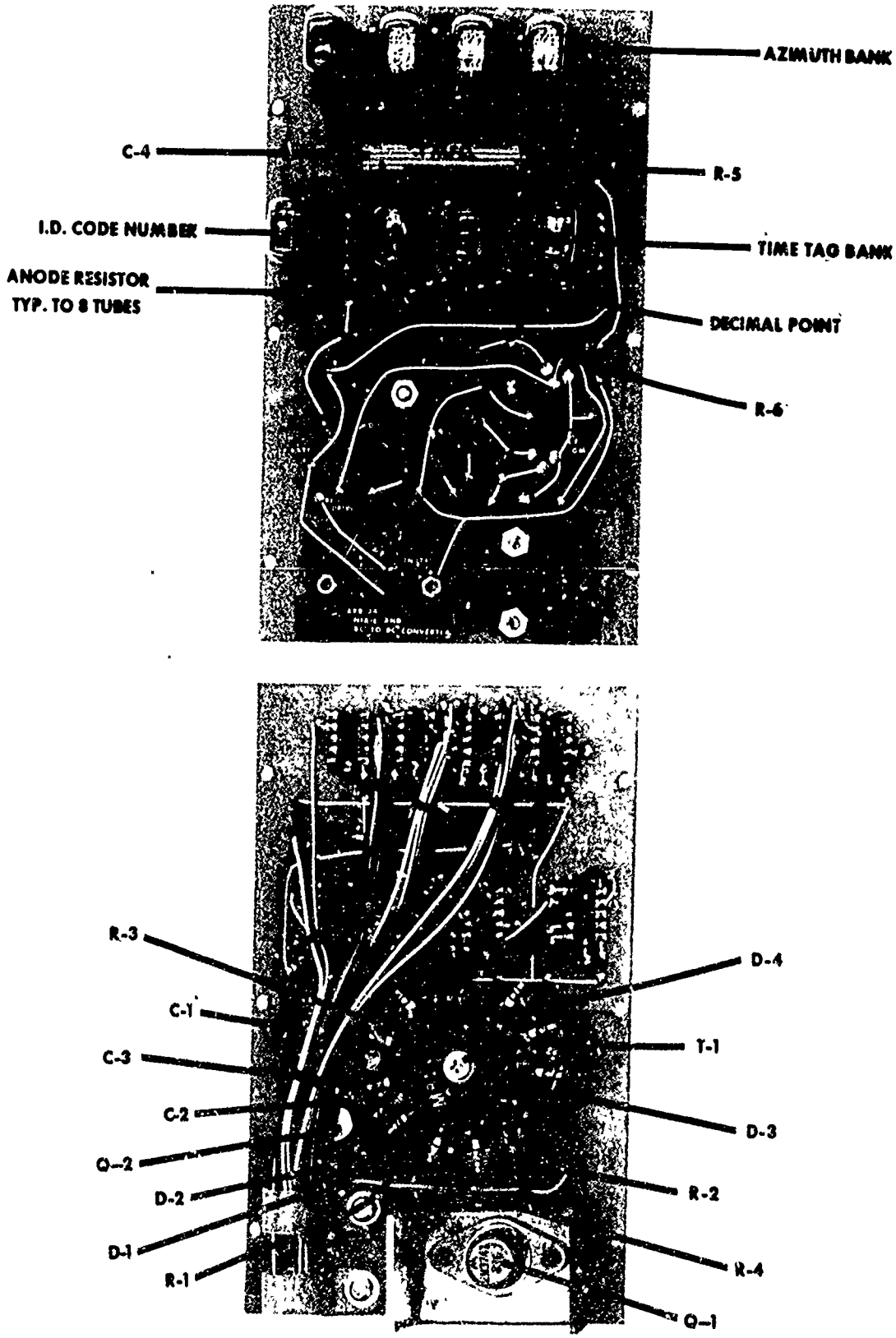


Fig. 7.11b. Board 34 (cont.).

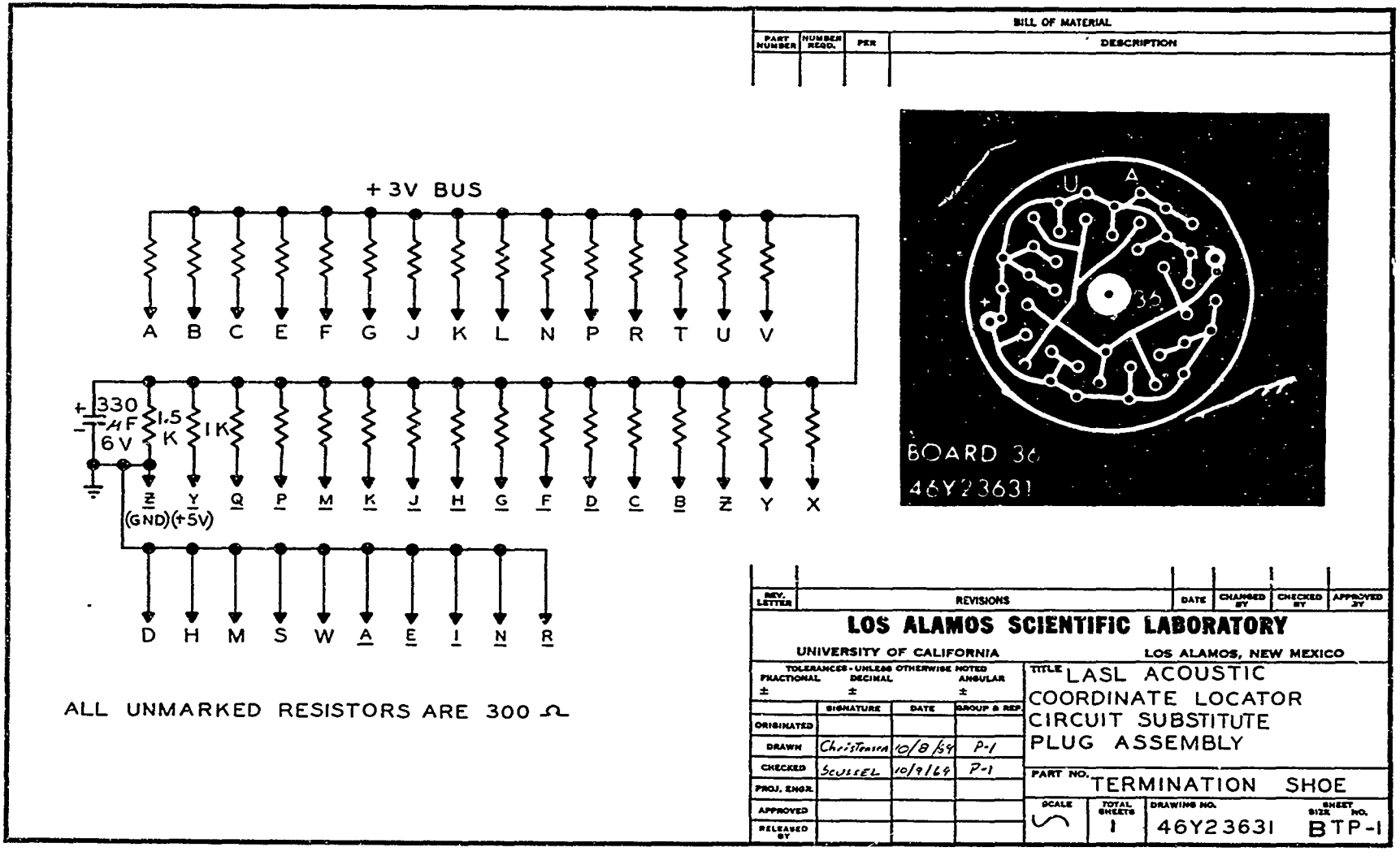
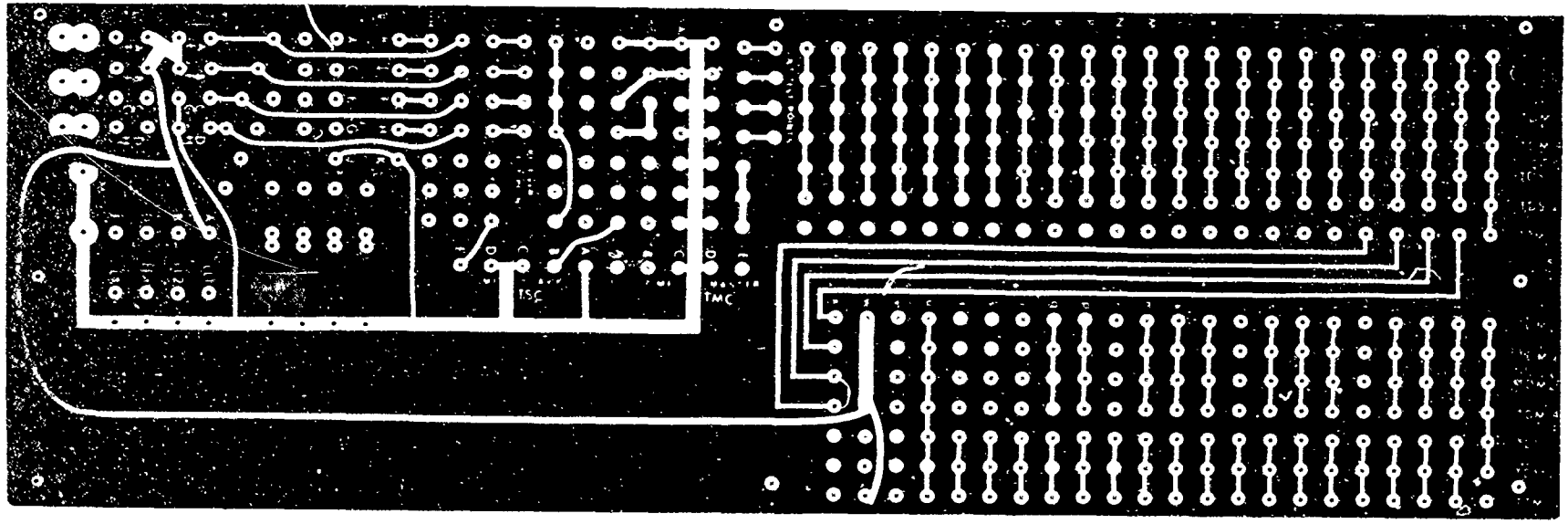
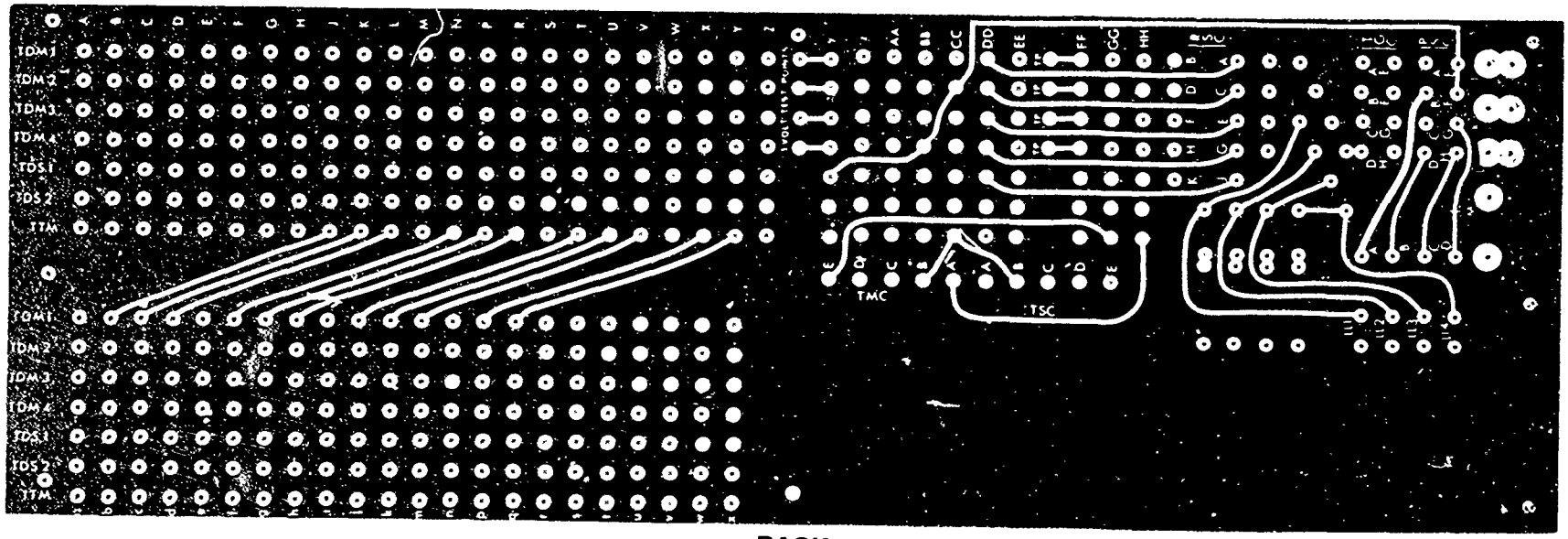


Fig. 7.12. Board 36. Termination shoe for party-line bus.

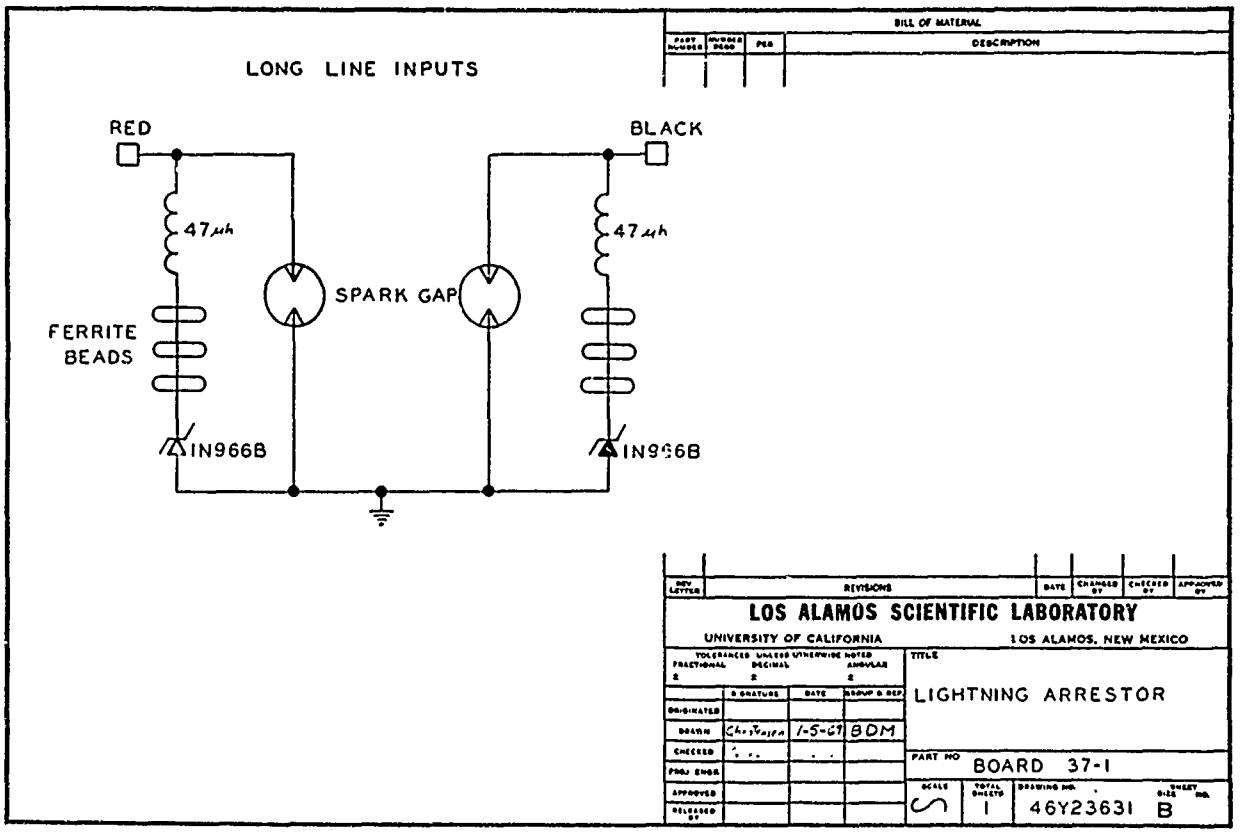


FRONT



BACK

Fig. 7.13a. Board 37. Interconnection board.



Lightning Arrestor

Board 37-1
Parts List

Choke:	47 μH
Ferrite Beads:	Ferroxcube 56-590-65B/3B
Zener Diode:	1N966B
Spark Gap:	Siemens B1-C90/20 (90V, 5 KA)

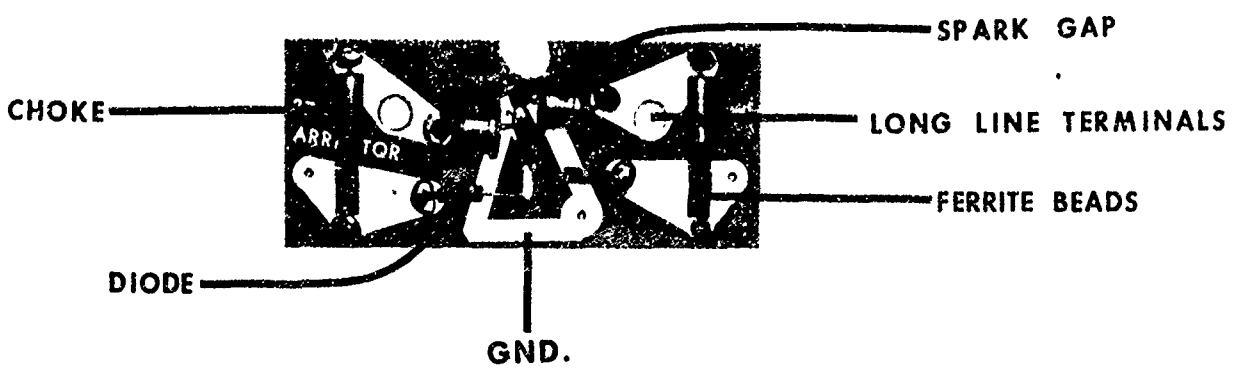


Fig. 7.13b. Board 37 (cont.). Board 37-1. Lightning arrester for long lines.

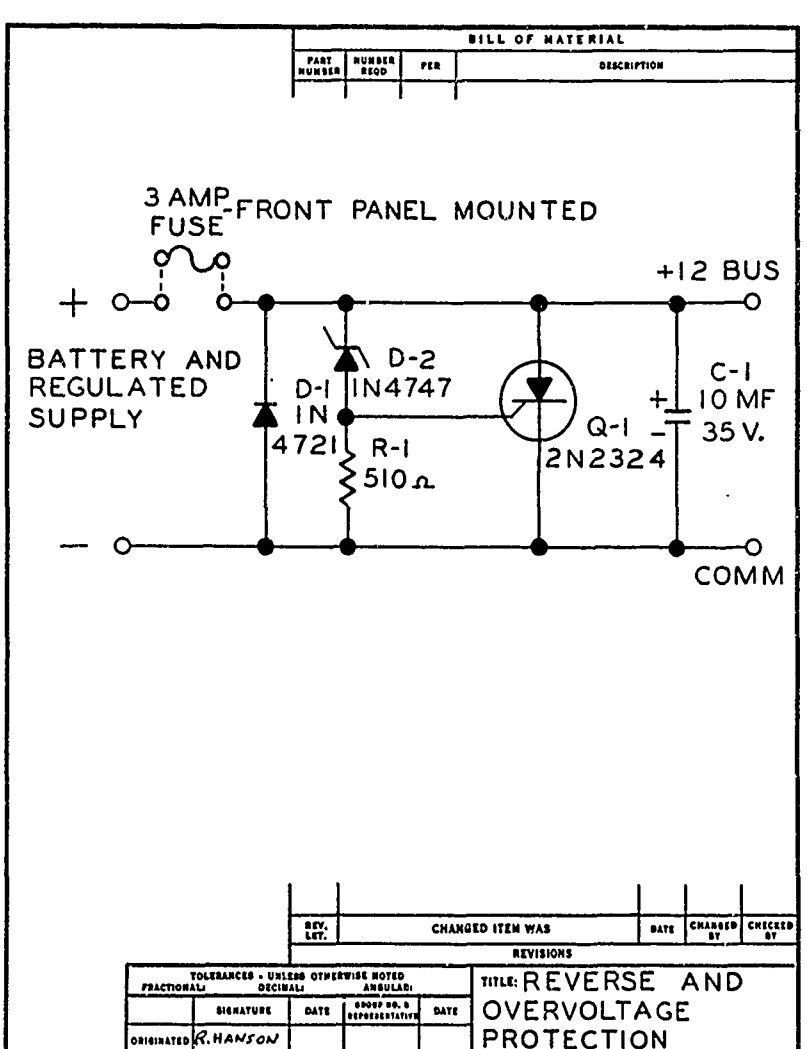


Fig. 7.13c. Board 37 (cont.). Board 37-3. Reverse and overvoltage protection circuit.

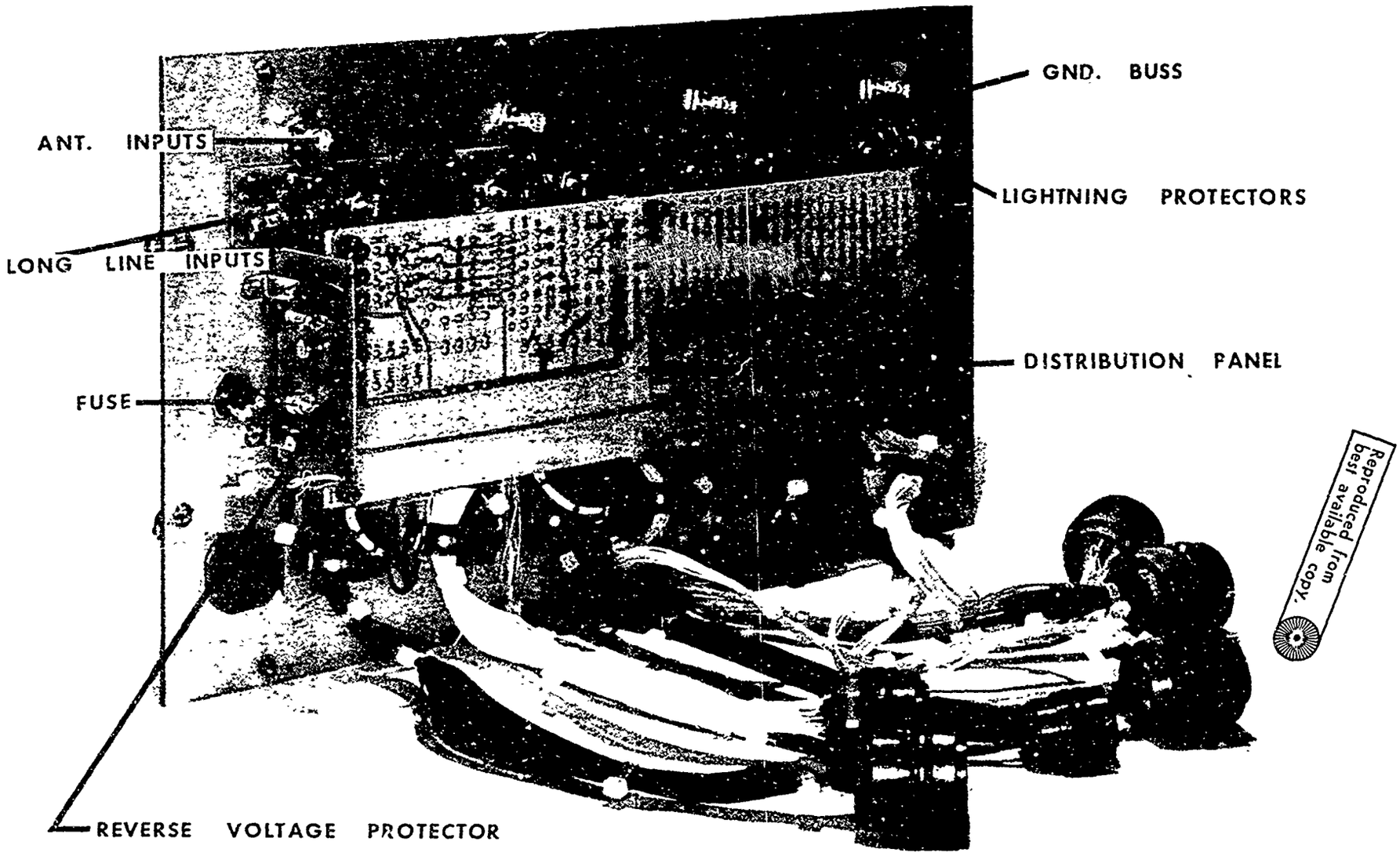
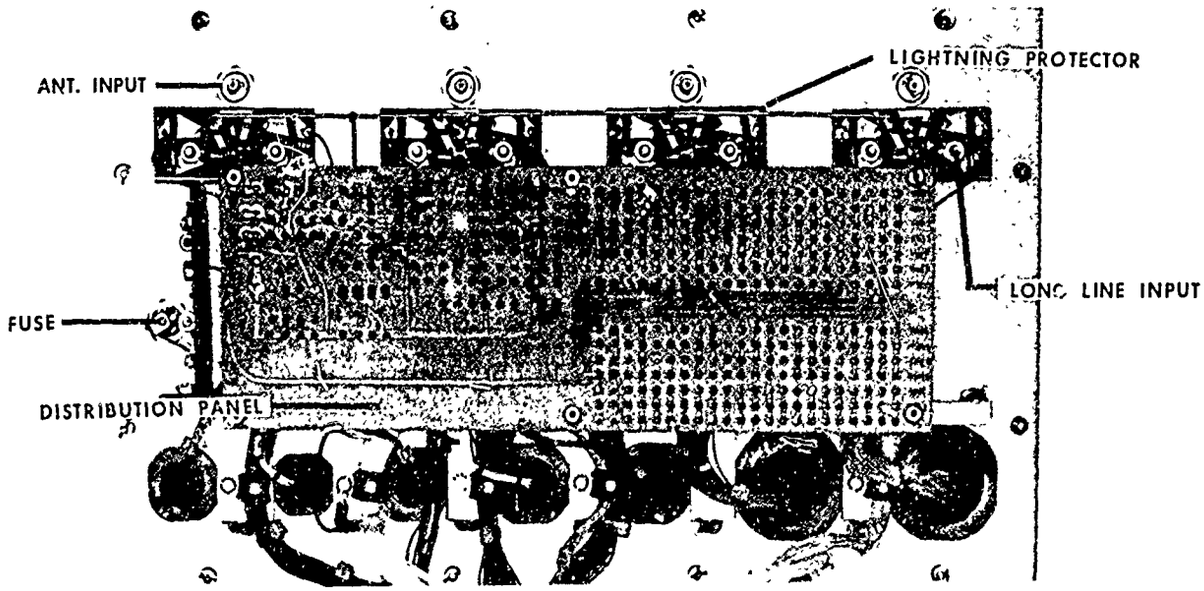


Fig. 7.14a. TDS interconnection panel.



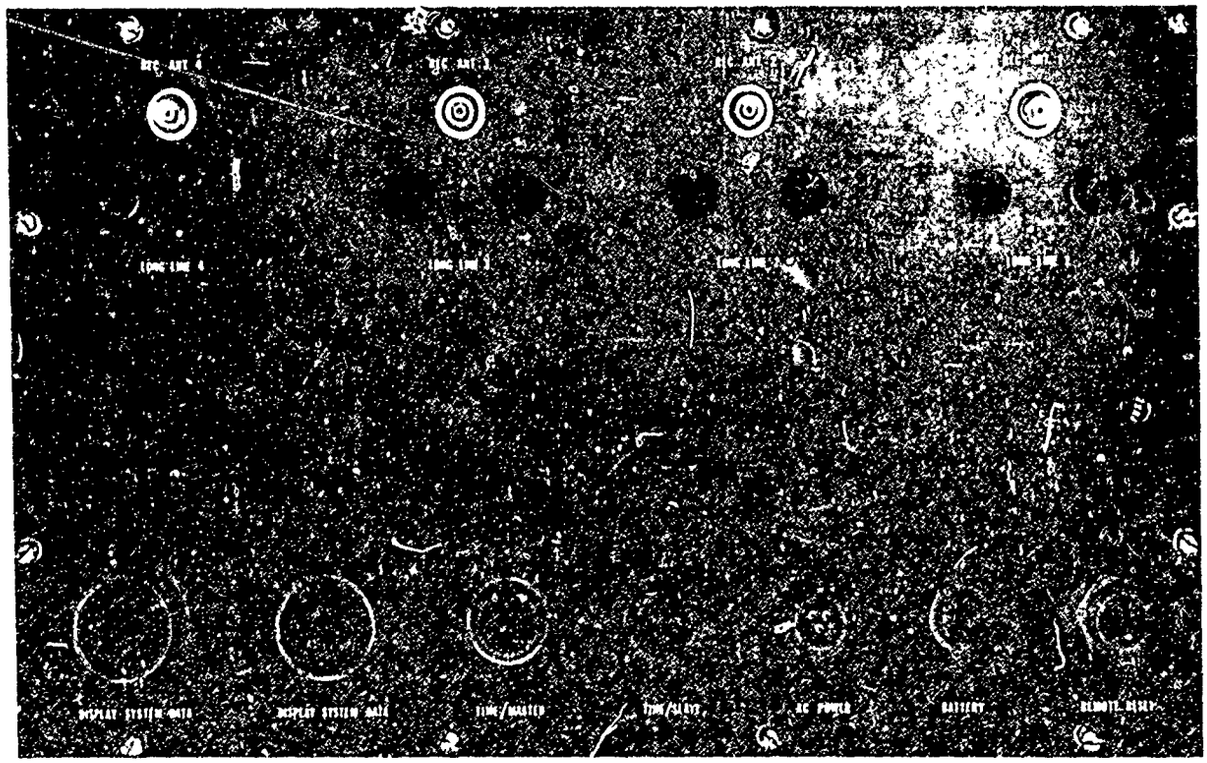


Fig. 7.14b. TDS interconnection panel (cont.).

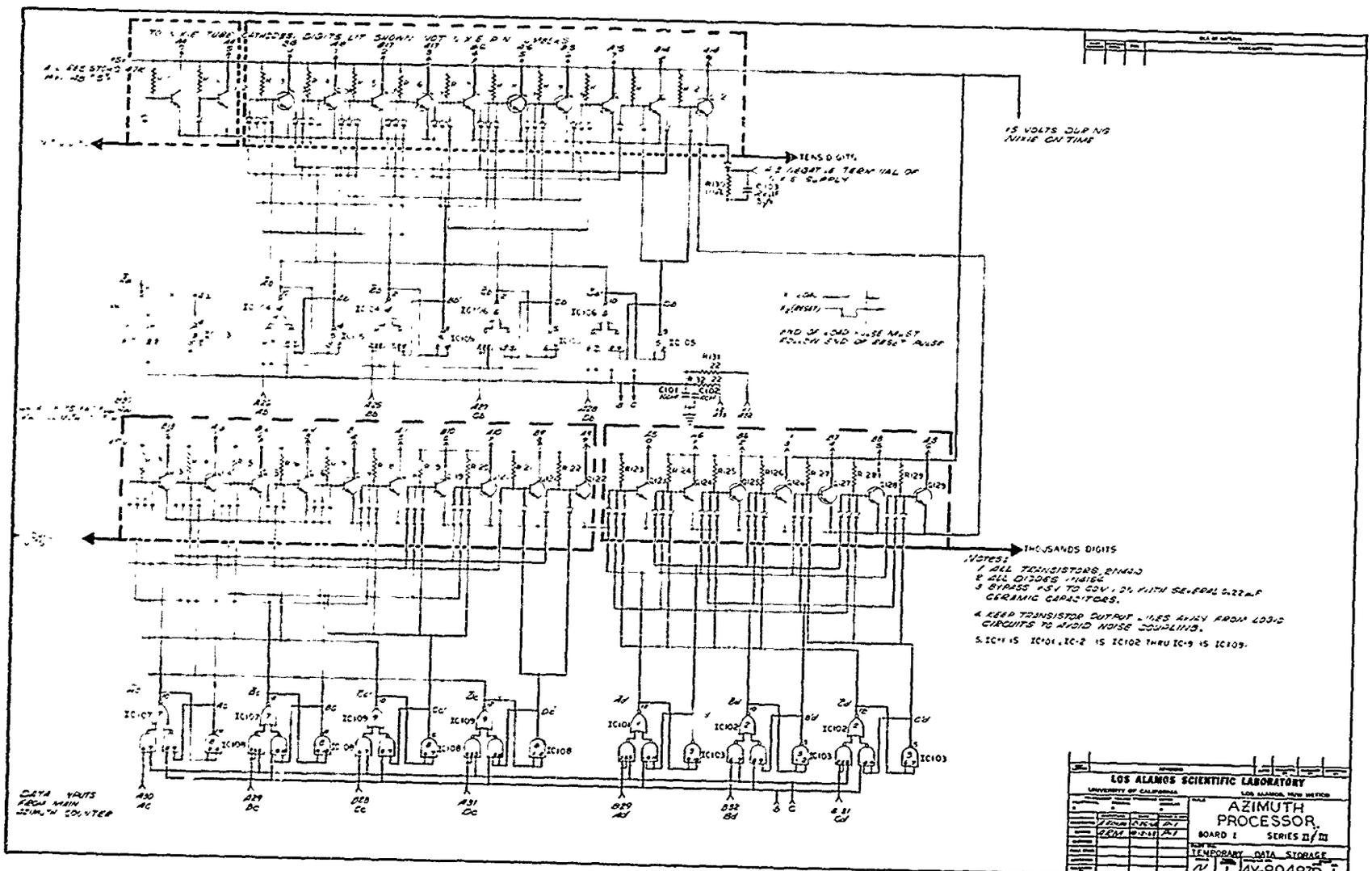


Fig. 7.15a. Board 1. NIXIE store and decode.

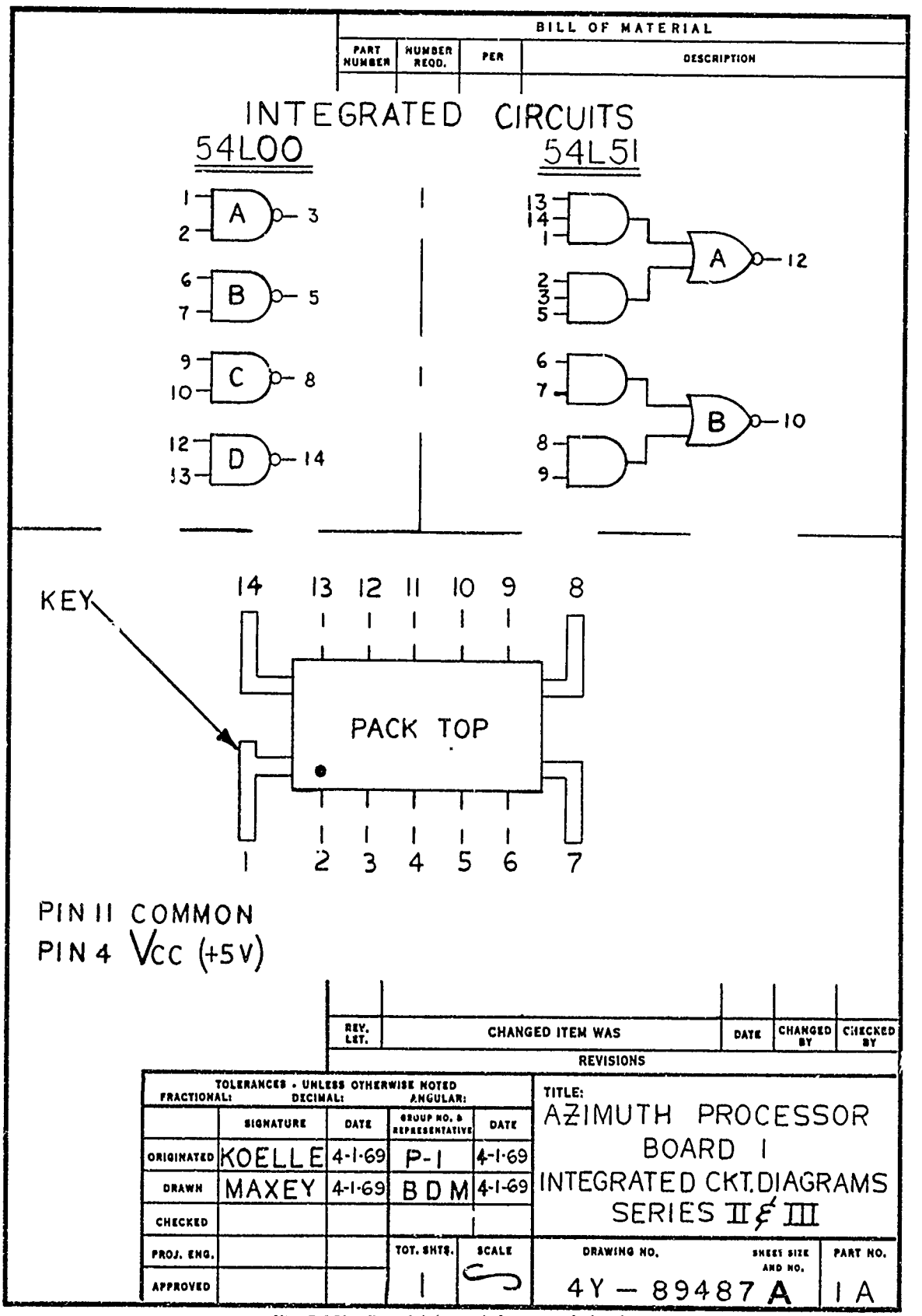


Fig. 7.15b. Board 1 (cont.). Integrated circuits.

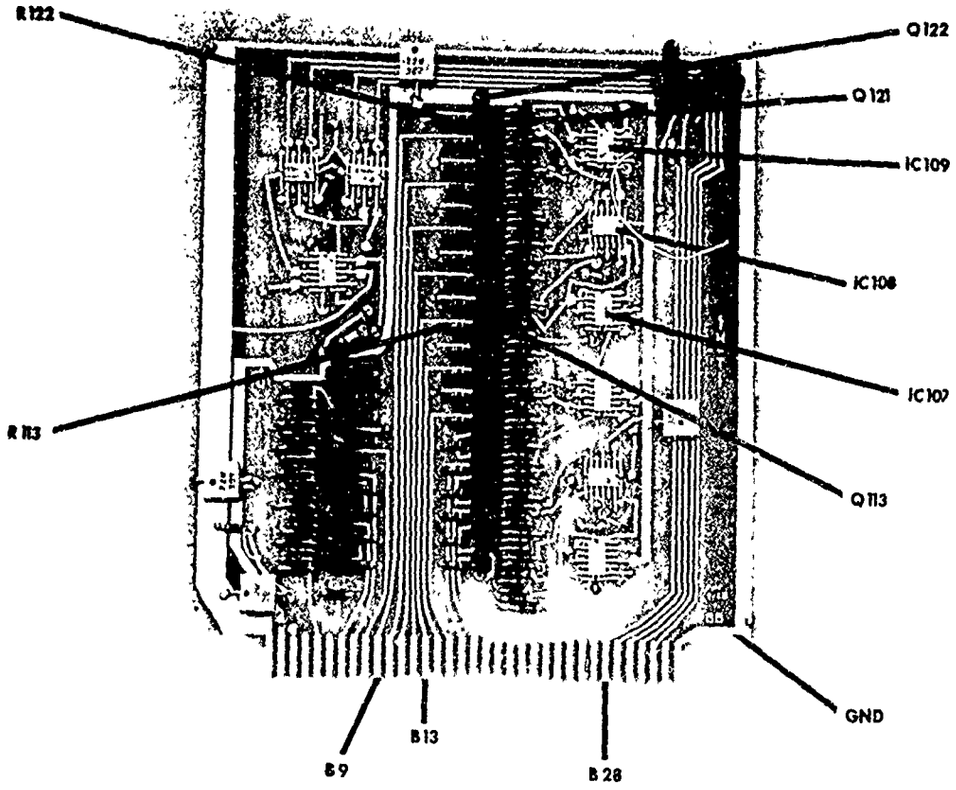


Fig. 7.15c. Board 1 (cont.). Hundreds digits.

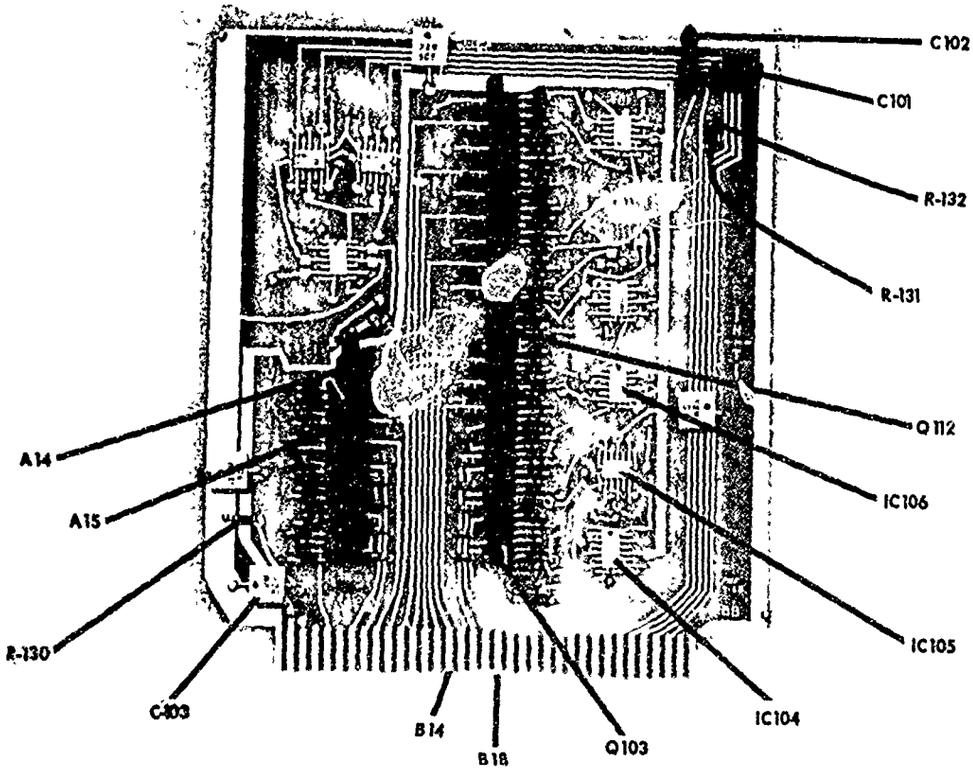


Fig. 7.15d. Board 1 (cont.). Tens digits.

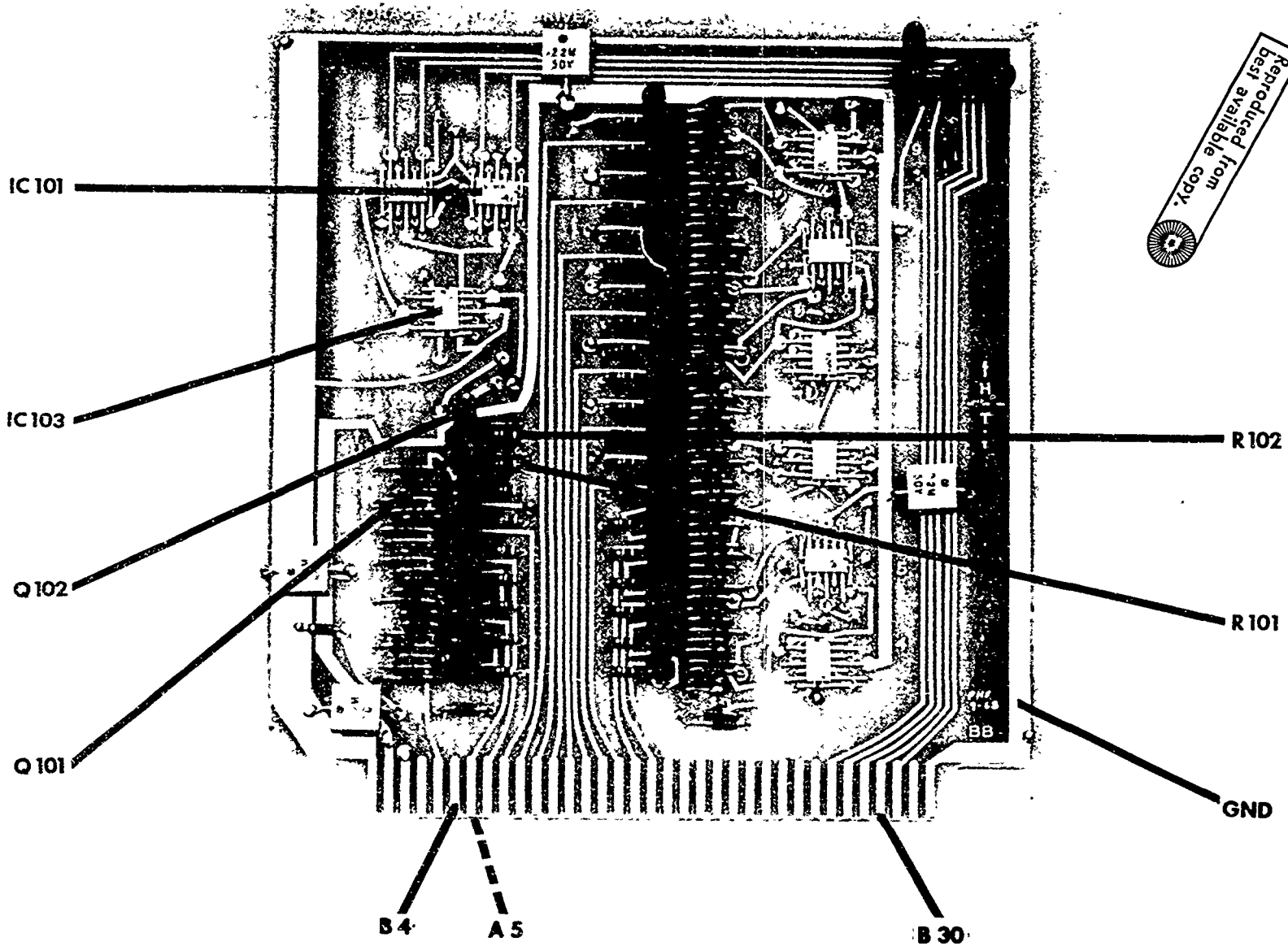


Fig. 7.15e. Board 1 (cont.). Units digits.

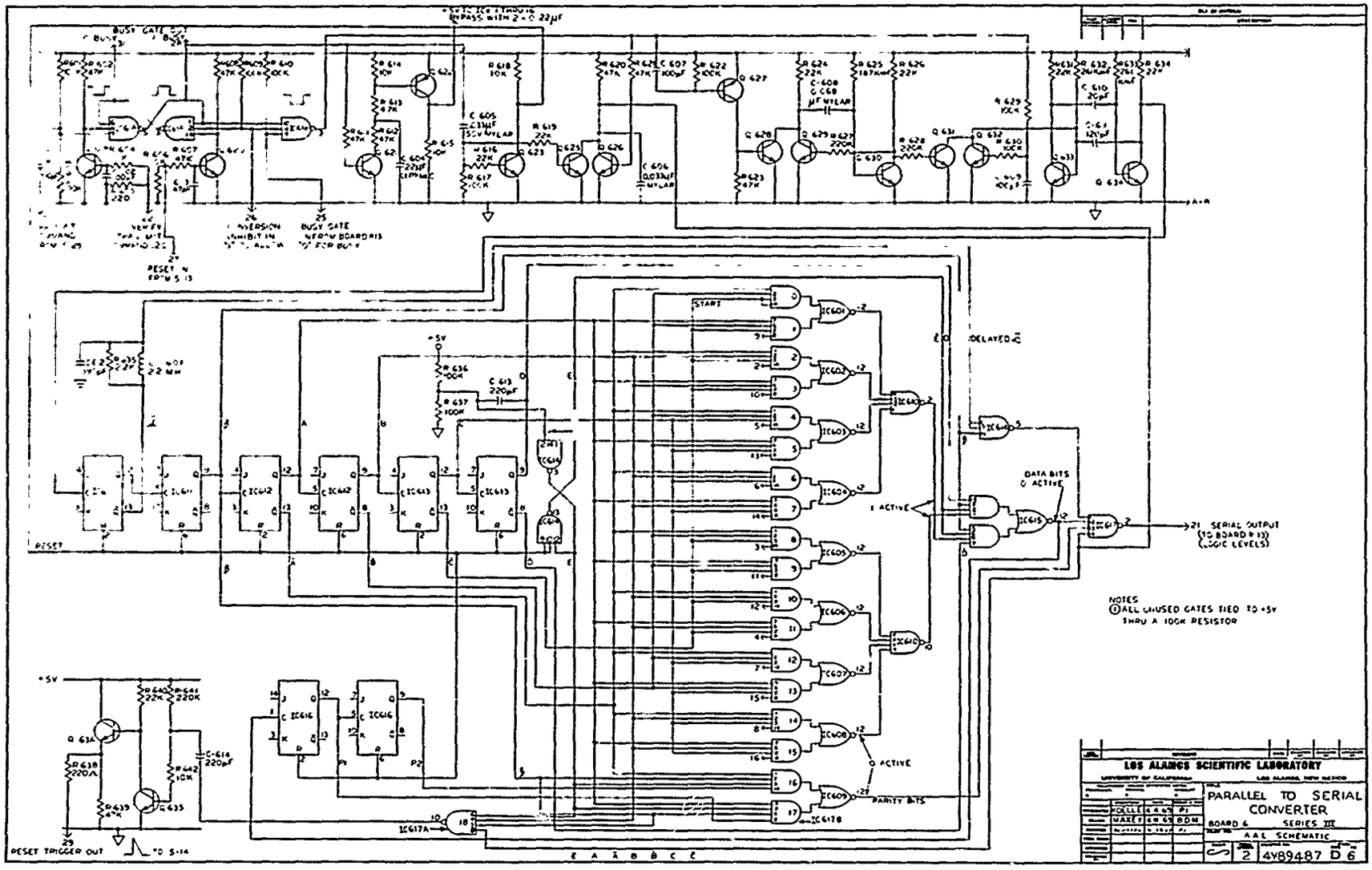


Fig. 7.16a. Board 6. Parallel-to-serial data converter.

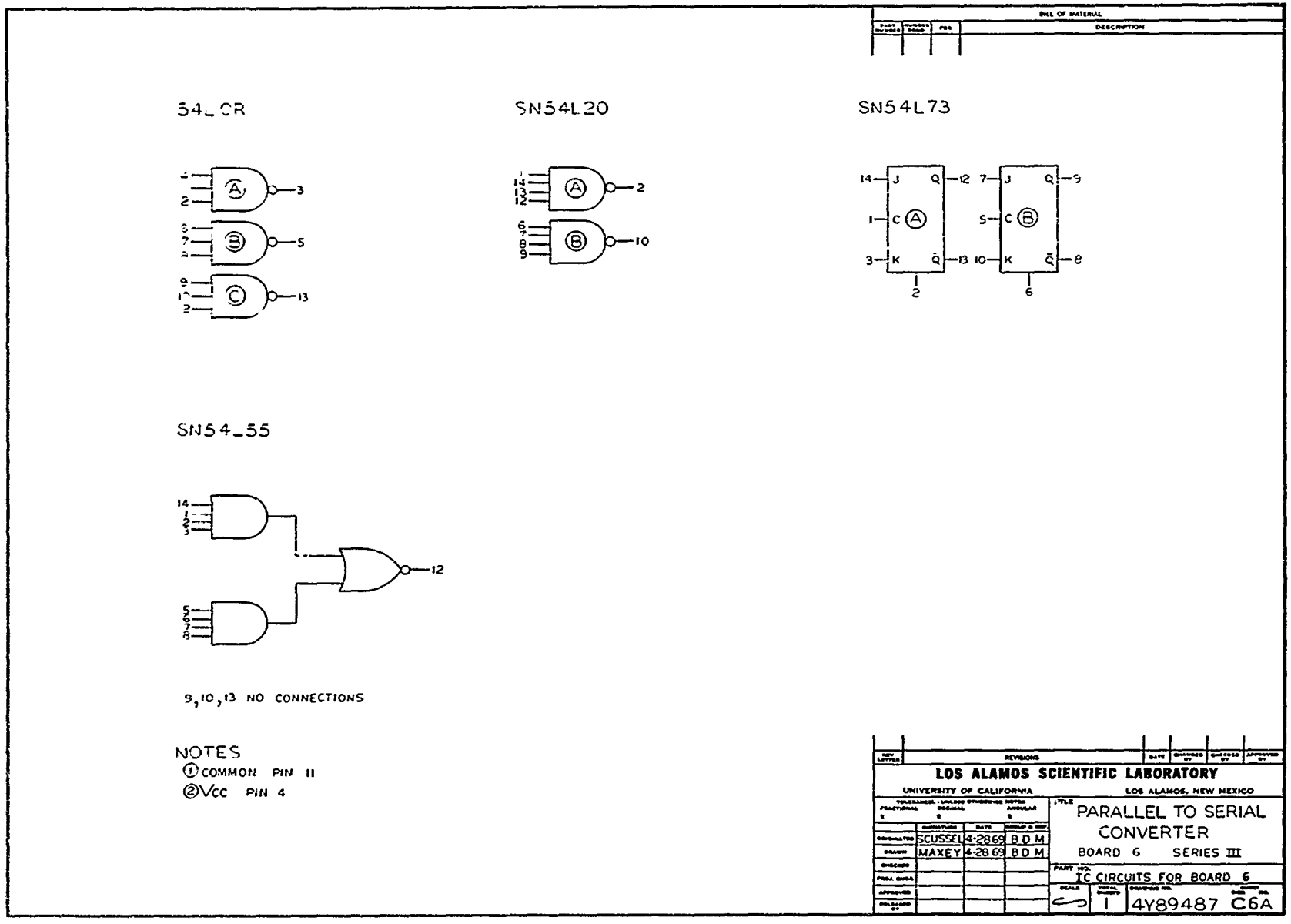


Fig. 7.16b. Board 6 (cont.).

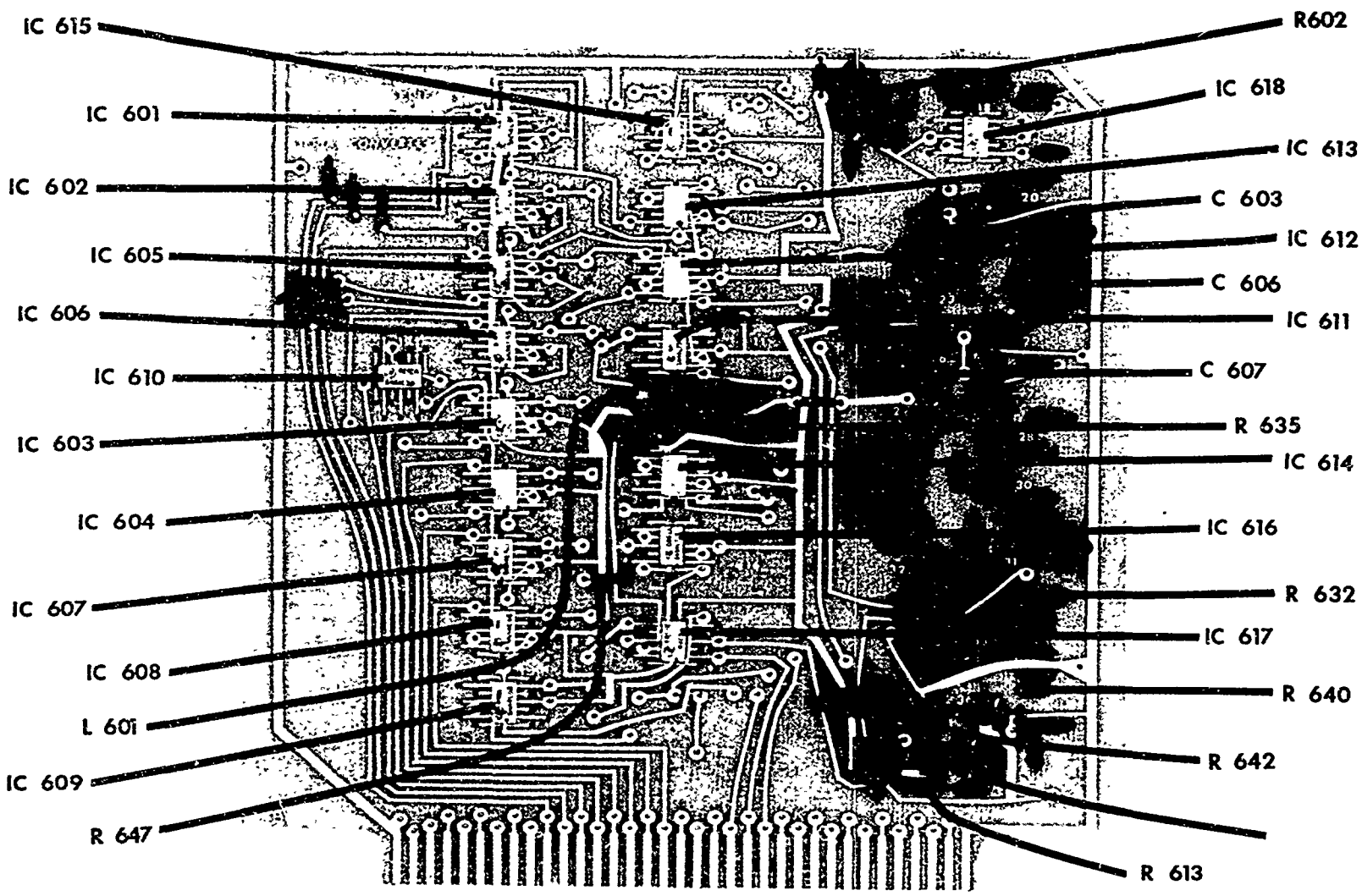


Fig. 7.16c. Board 6 (cont.).

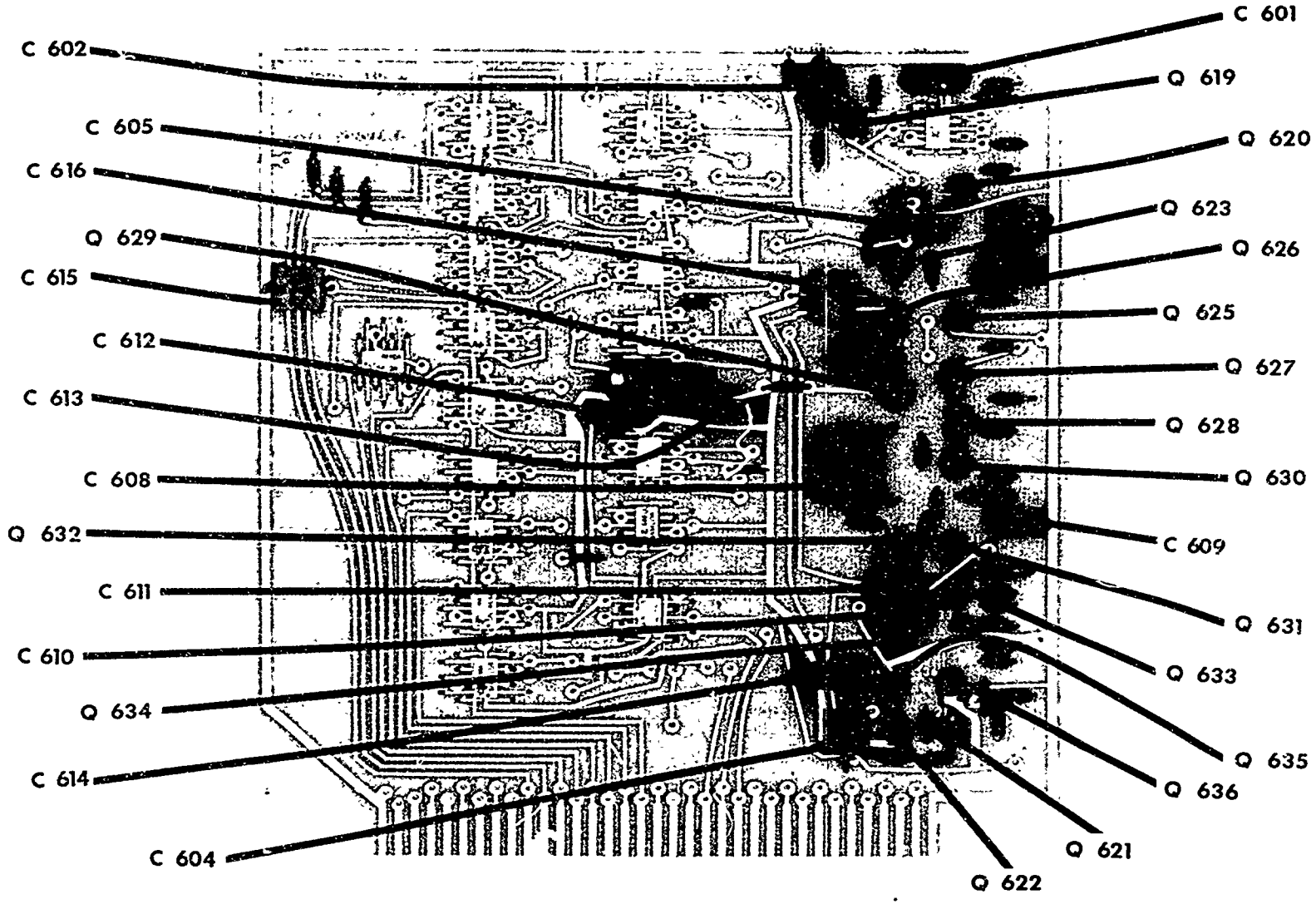


Fig. 7.16d. Board 6 (cont.).

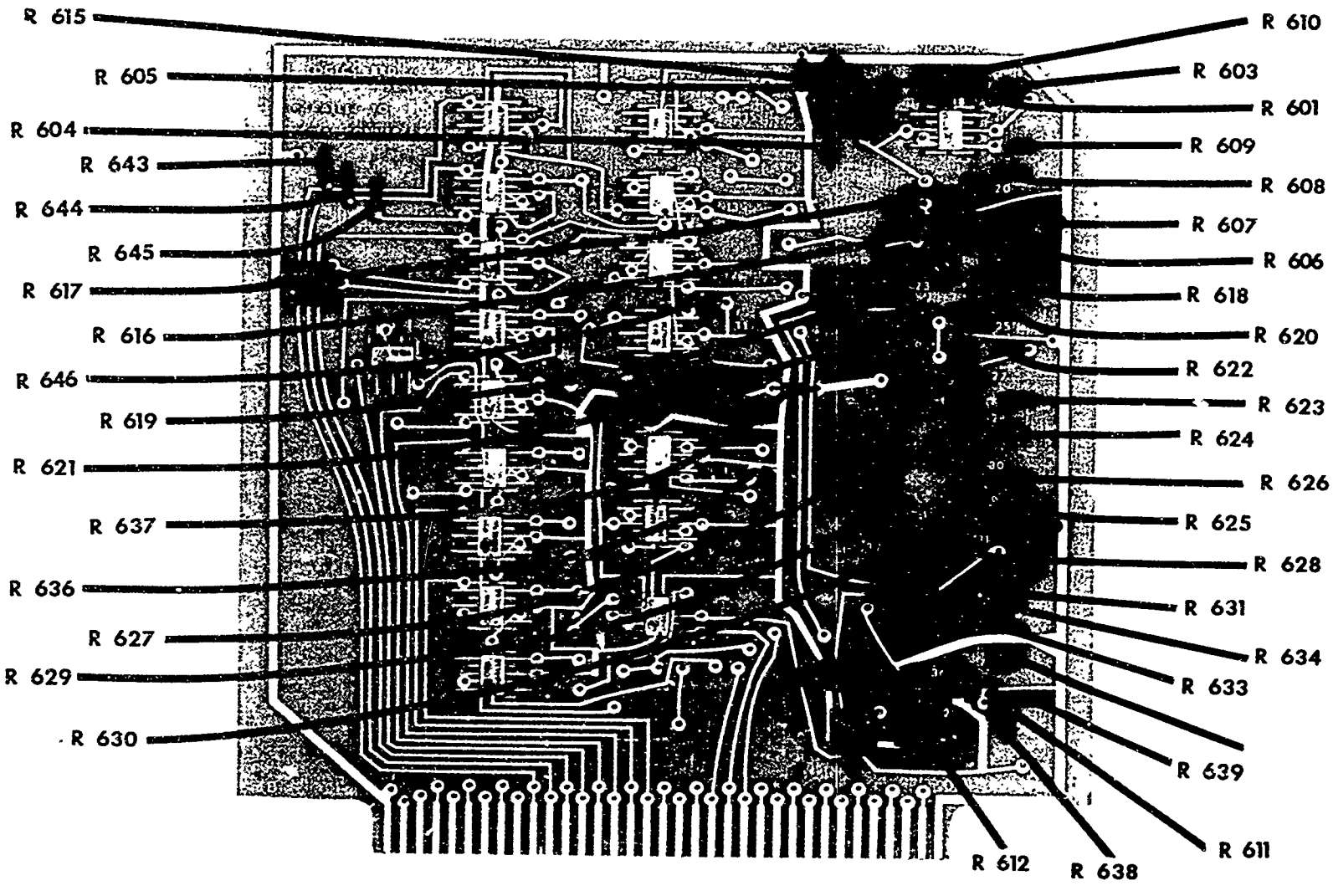


Fig. 7.16e. ,Board 6 (cont.).

CHAPTER 8. INTERMODULE WIRING FOR INTERCONNECTION BOARD 37

The following intermodule wiring lists and module wiring diagrams specify interconnections to be made among board sockets, front panel, and module connectors on the special Interconnection Board 37. Symbols used in Table 8.1 are explained below.

1. An X in two or more columns means that these terminals are connected in parallel. For example, Pin A on the two system connectors, the four TDM connectors, and the time-tag connectors are all connected together.

2. An * in one or more columns means that no connection is made to that pin. For example, Pin F on the Time Tag Module is not connected anywhere, but Pin F of the system connectors and TDM connectors are all connected in parallel.

3. A specific connector pin designation in a column means that that pin connects to the indicated pin. For example, Pin B of the Time Tag Module connects to Telemetry Display Module #1 (TDM1) Pin x.

4. The Comments section contains signal designations. The + or − after a signal designation indicates positive true or negative true logic. Negative true logic is used only for the party-line bus that connects to external equipment.

5. Notes are explained below Pin HH.

TABLE 8.1.

BOARD 37 CONNECTOR INTERWIRING SPECIFICATIONS

Pins	4 Telemetry Display Modules	2 System Connectors	Time Tag Module	Other Connections	Comments
A	X	X	X		Strobe line − Party-Line Bus
B	X	X	TDM1-x		TDM Xmit ID-4 − TTM TDM1 - AGC
C	X	X	TDM2-x		TDM Xmit ID-2 − TTM TDM2 - AGC
D	X	X	TDM3-x		TDM Ground Return TTM TDM3 - AGC
E	X	X	TDM4-x		TDM Xmit ID-1 − TTM TDM4 - AGC
F	X	X	*		Module ID-2 −
G	X	X	*		Module ID-1 −
H	X	X	*		Ground Return
J	X	X	TDM-b		TDM Azimuth 4000 − TTM 40 sec +

TABLE 8.1. (cont)

Pins	4 Telemetry Display Modules	2 System Connectors	Time Tag Module	Other Connections	Comments
K	X	X	TDM-c		TDM Azimuth 2000 – TTM 20 sec +
L	X	X	TDM-d		TDM Azimuth 1000 – TTM 10 sec +
M	X	X	*		Ground Return
N	X	X	TDM-f		TDM Azimuth 800 – TTM 8 sec +
P	X	X	TDM-g		TDM Azimuth 400 – TTM 4 sec +
R	X	X	TDM-h		TDM Azimuth 200 – TTM 2 sec +
S	X	X	*		Ground Return
T	X	X	TDM-j		TDM Azimuth 100 – TTM 1 sec +
U	X	X	TDM-k		TDM Azimuth 80 – TTM 0.8 sec +
V	X	X	TDM-m		TDM Azimuth 40 – TTM 0.4 sec +
W	X	X	*		Ground Return
X	X	X	TDM-p		TDM Azimuth 20 – TTM 0.2 sec +
Y	X	X	TDM-q		TDM Azimuth 10 – TTM 0.1 sec +
Z	X	X	*		Azimuth 5 –
a	X	X	*		Ground Return
b	TTM-J	X	X		TDM 40 sec + TTM 40 sec –
c	TTM-K	X	X		TDM 20 sec + TTM 20 sec –
d	TTM-L	X	X		TDM 10 sec + TTM 10 sec –
e	*	X	X		Ground Return

TABLE 8.1. (cont)

Pins	4 Telemetry Display Modules	2 System Connectors	Time Tag Module	Other Connections	Comments
f	TTM-N	X	X		TDM 8 sec + TTM 8 sec –
g	TTM-P	X	X		TDM 4 sec + TTM 4 sec –
h	TTM-R	X	X		TDM 2 sec + TTM 2 sec –
i	*	X	X		Ground Return
j	TTM-T	X	X		TDM 1 sec + TTM 1 sec –
k	TTM-U	X	X		TDM 0.8 sec + TTM 0.8 sec –
m	TTM-V	X	X		TDM 0.4 sec + TTM 0.4 sec –
n	*	X	X		Ground Bus
p	TTM-X	X	X		TDM 0.2 sec + TTM 0.2 sec –
q	TTM-Y	X	X		TDM 0.1 sec + TTM 0.1 sec –
r	*	X	X		Ground Bus
s	*	X	X		Reset-Preset Time
t	*	X	X		1-Min Time Signal
u	X	X	X		Mode Control Signal
v	*	*	*		No Connection
w	X	*	X		10- to 16-V Power
x	Note 1	*	*		AGC from TDM Receivers
y	Note 2	X	X	5-V Test Points	TDM 5-V Test Points TTM 5-V to System Connectors
z	X	X	X	AA	Power Ground
AA	X	X	X	z	Power Ground
BB	Note 3	*	*	5-V Ground	Module ID-2 Input

TABLE 8.1 (cont)

Pins	4 Telemetry Display Modules	2 System Connectors	Time Tag Module	Other Connections	Comments
CC	Note 3	*	TSC-B TMC-B	TSC-B TMC-B	Module ID-1 Input TTM, 1-Min/Reset Signal
DD	Note 4	*	*	Note 5	External Reset, Normally Open
EE	X	*	X		Alarm Signal
FF	Note 6	*	TSC-E	TSC-E Receiver Test Points	TDM–Receiver Test Points TTM–Oscillator Output
GG	Note 7	*	TMC-E	TMC-E Note 7	TDM Long Lines TTM External Clock Input
HH	Note 5	*	TMC-A		TDM External Reset, N.C. TTM Inhibit Clock

Note 1. See Pins B, C, D, and E.

Note 2. Each 5-V line appears seperatly on Board 37 as a test point for the 5-V power supply in each individual module.

Note 3. The module ID input is hard-wired into the TDM1, TDM2, TDM3, and TDM4 connectors so that the module ID code is associated with the module connector (position) in the TDS. The connections are as follows.

Pins	TDM1	TDM2	TDM3	TDM4
BB	Ground	Ground	+5V	+5V
CC	Ground	+5V	Ground	+5V
ID Code	0	1	2	3

Note 4. These connections are for the purpose of providing an externally operated reset push button. Pins DD and HH connect to the external reset push button connector as follows:

Pins	TDM1	TDM2	TDM3	TDM4	
DD	RSC-A	RSC-C	RSC-E	RSC-G	Normally Open
HH	RSC-B	RSC-D	RSC-F	RSC-H	Normally Closed.

Note 5. The external reset push button operates by grounding either line DD or HH (on the TDM). The ground connection is RSC-J and RSC-K.

Note 6. The receiver outputs from each TDM are seperatly brought to test points on Board 37.

Note 7. Each TDM long-line (field wire) input has a terminating network (0.047μF in series with 150 Ω) on Board 37. From Board 37, the long-line signal is connected to:

a. The lightning arrester for each input channel.

b. The test code generator (Portable Test Azimuth Generator).

MASTER-SLAVE SYNCHRONIZING CONNECTORS (TMC and TSC)

TMC	Connects to	TSC	Connects to
A	TTM-HH	A	Ground
B	TTM-CC	B	TTM-CC
C	Ground	C	Ground
D	Ground	D	Ground
E	TTM-GG	E	TTM-FF

115-V AC CONNECTOR ACC

A	115-V ac 60 Hz, Hot Side of Line
B	115-V ac 60 Hz, Neutral
C	Safety Ground

BATTERY CONNECTOR

A	+ 1 Battery
B	No Connection
C	Common (– Battery)
D	Regulator Voltage Adjust
E	No Connection

POWER SUPPLY MODULE CONNECTOR (PSC)

A	+ Regulated Output	G	Ground Return
B	+ Regulated Output	H	Regulator Voltage Adjust
C	No Connection	J	115-V ac, Hot
D	No Connection	K	115-V ac, Neutral
E	No Connection	L	115-V ac, Safety Ground
F	No Connection	M	Ground Return

TEST CODE GENERATOR MODULE (TGC)

A	TDM1 Test Code	E	+ Battery
B	TDM2 Test Code	F	+ Battery
C	TDM3 Test Code	G	Ground Return
D	TDM4 Test Code	H	Ground Return

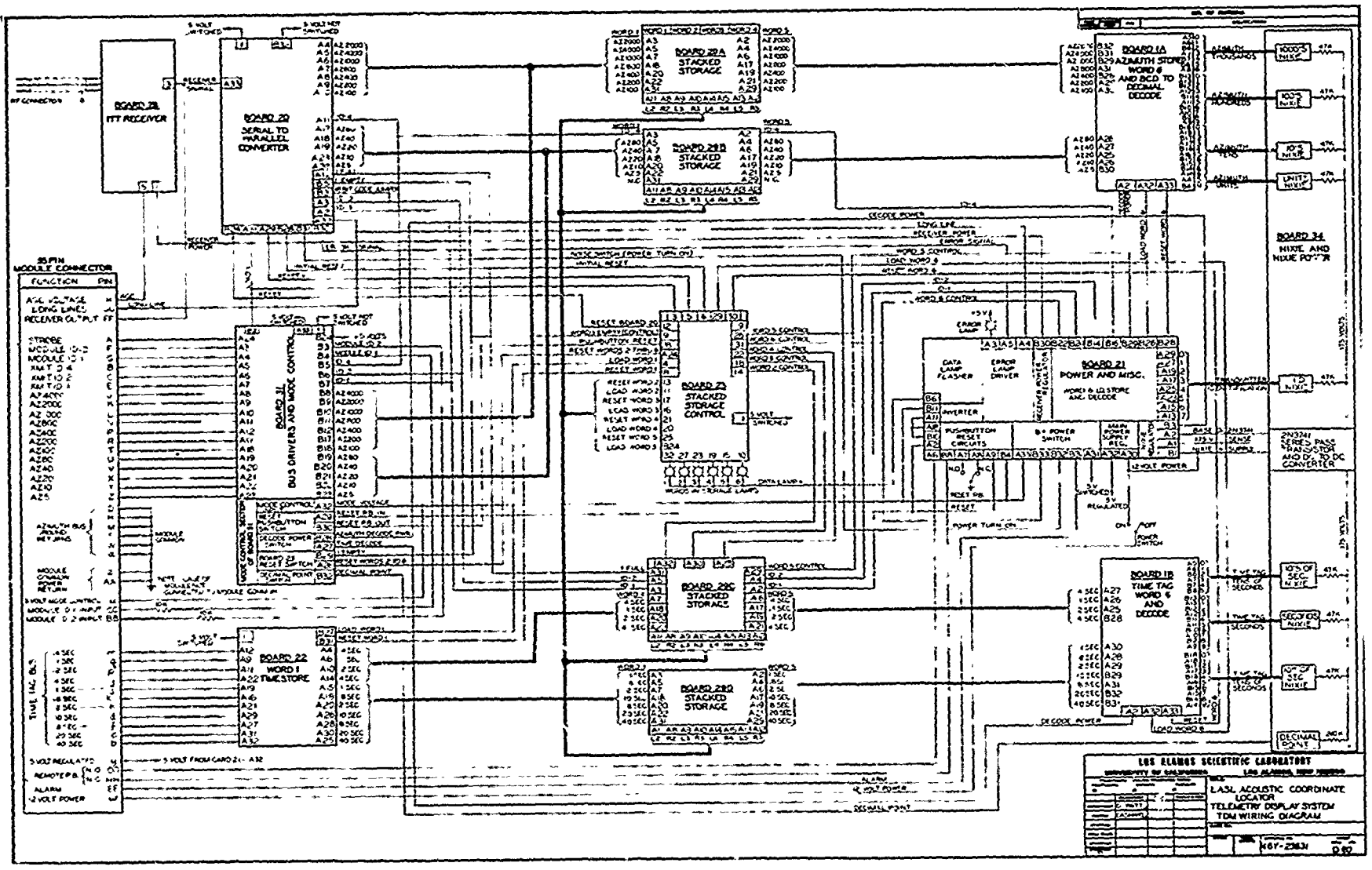


Fig. 8.1 TDM wiring diagram.

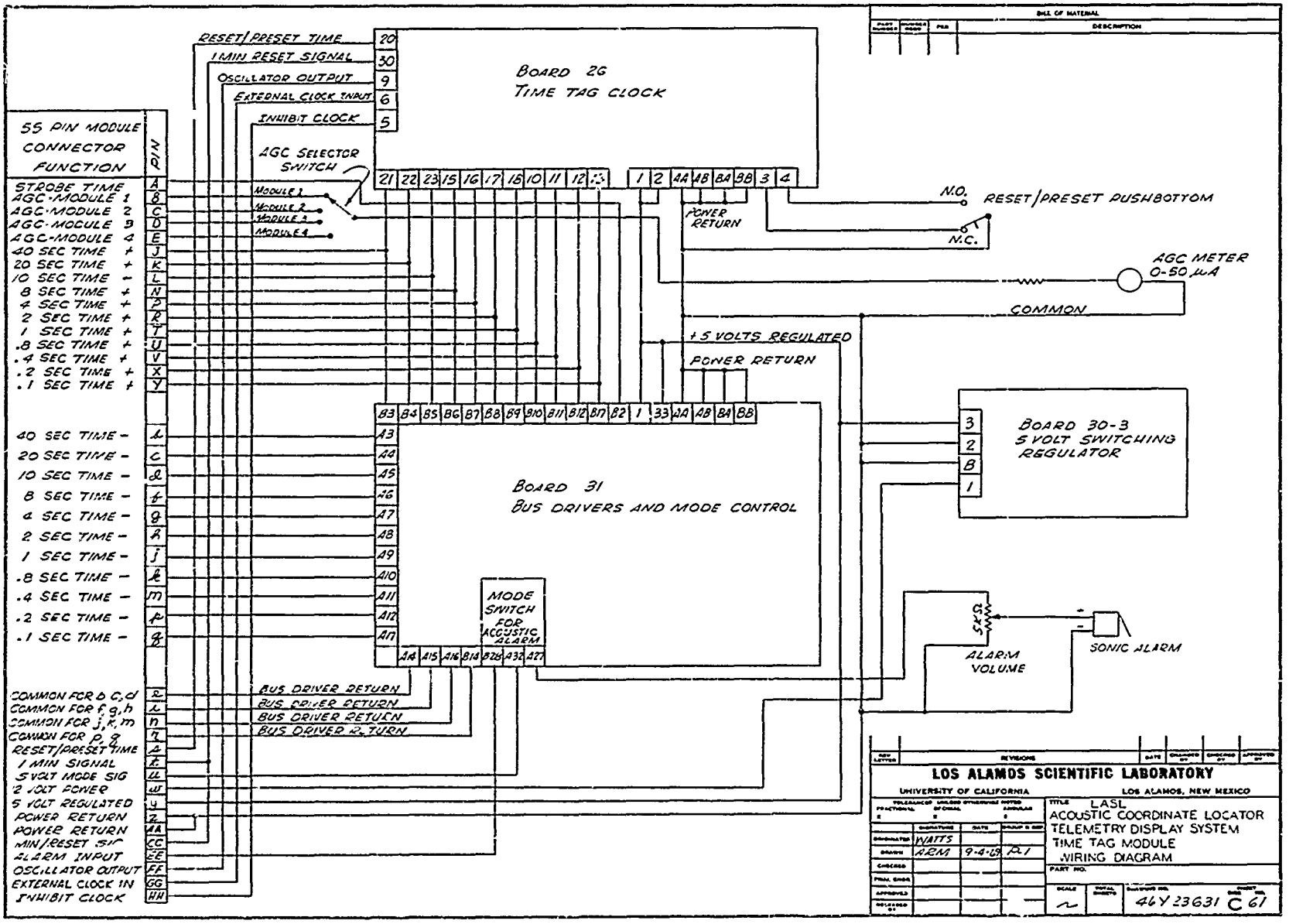


Fig. 8.2. TTM wiring diagram.

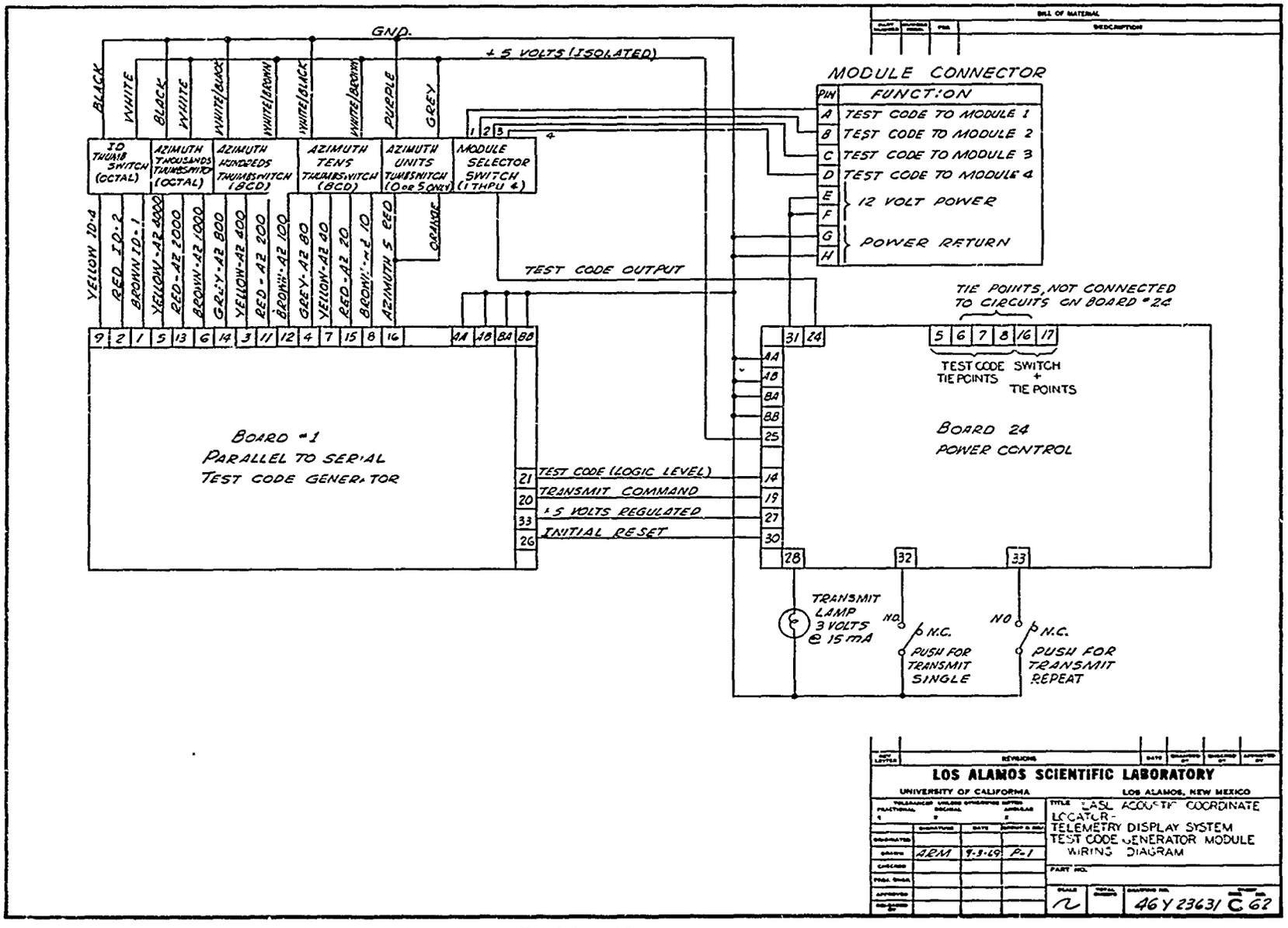


Fig. 8.3. TCG wiring diagram.

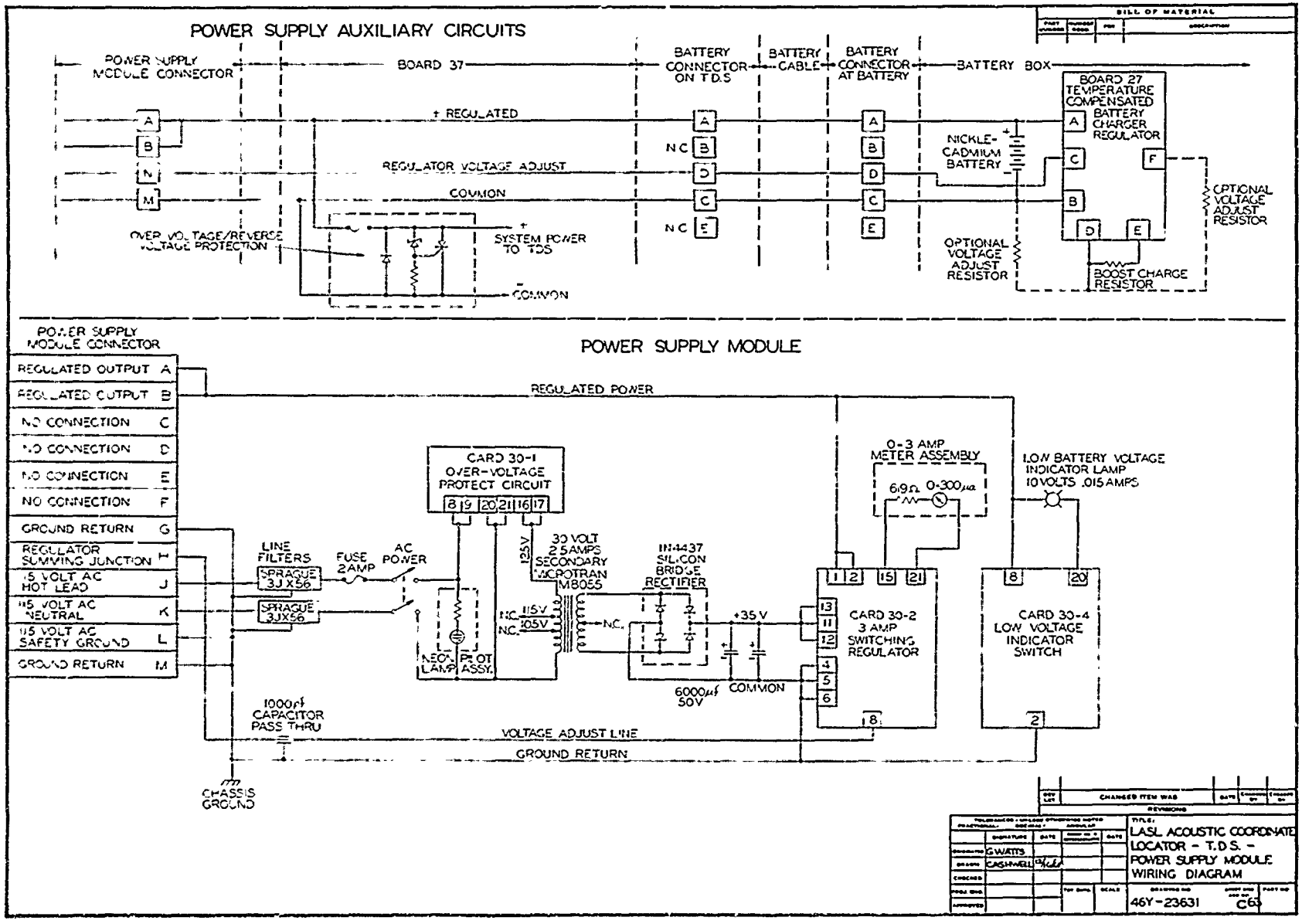


Fig. 8.4. PSM wiring diagram.