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SWITCHABLE ACOUSTIC MATCHED FILTER

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William C. Fifer
Dr. Richard LaRosa
John F. Crush

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William C. Fifer
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John F. Crush

Hazeltine Corporation

Details of illustrations in this document may be better studied on microfiche

FOREWORD

This Final Report was submitted by Hazeltine Corporation, Greenlawn, New York, under contract F30602-71-C-0199, Job Order Number 45190000, to Rome Air Development Center, Griffiss Air Force Base, New York. Identified by the contractor as report number 7974, it covers the period March 1971 to January 1972. Henry J. Bush (CORC) is the RADC program monitor.

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Approved: Henry J. Bush
HENRY J. BUSH, Project Engineer

Approved: Ingrid J. Ryleman
ALVIN TWITCHELL, Colonel, USAF
Chief, Communications & Navigation Division

FOR THE COMMANDER: Fred I. Diamond

FRED I. DIAMOND
Acting Chief, Plans Office

ABSTRACT

The design, fabrication, and evaluation of an experimental, 127-tap electronically programmable, acoustic surface wave sequence generator and matched filter for PSK bi-phase spread spectrum signals is described. This design demonstrates the economic feasibility of electronically programming, on a bit-by-bit basis, the code sequence for a bi-phase PSK sequence generator and matched filter.

EVALUATION

The significance of this report is that it provides an economically feasible design for an electronically programmable, bi-phase, PSK sequence generator and matched filter. The feasibility is derived by combining the acoustic surface wave multiple tap delay line and solid state switching and control logic. The report contains the successful test results of a hybrid implementation of the design. This success is significant in that the design uses two field effect transistors in the switching element rather than a multiplicity of diode bridges and can be considerably reduced in power dissipation and volume through advanced integrated circuit techniques.

Henry J. Bush

HENRY J. BUSH, Project Engineer

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Time synchronization and correlation requirements for advanced wideband, multi-functioned communications, navigation, and IFF systems impose difficult system and component problems. One approach is to provide these functions using pseudo noise modulation, code sequences ranging up to 1000-bits, and matched filter signal processing. Acoustic surface wave phenomena offer a solution to the practical design and development of large frequency-time product matched filters for pseudo noise modulation.

Small size, lightweight, low power drain and signal accessibility are some of the potential advantages to be attained through the use of acoustic signal processing devices. Acoustic surface wave matched filters and sequence generators have been developed for 1000-bit pseudo noise sequences, but have employed hardwired, fixed-tap arrangements, so that the devices operate with only one or two specific code sequences. However, in order to improve the anti-jam capability of advanced systems, it is desirable to provide some form or means to arbitrarily switch the code sequences. One approach might be to pseudo randomly select one sequence generator and matched filter pair from a large bank of hardwired, fixed-tap, devices. Alternatively and more desirable would be to provide the system with only one pair of devices which could be rapidly and automatically programmed to switch the phase of each individual tap or bit. Thus, a large number (up to 2^N, where N is the number of chips in the code sequence) of different but matched code sequences would be simply provided by only two devices.

The main interest or technical problem to be solved on this program was the demonstration of an economically feasible technique for switching, on a bit-by-bit basis, the tap phase (polarity) of an acoustic surface wave matched filter and (simultaneously) an acoustic surface wave sequence generator.

2. PROGRAM OBJECTIVES AND SCOPE

The overall objective of this program was to study acoustic surface wave phenomena and to develop and extend the potential capability of acoustic devices to perform signal processing functions. Specifically this effort was to demonstrate a technique for providing both an electronically programmable acoustic matched filter and an electronically programmable acoustic sequence generator. A matched filter of this type could be used to provide time synchronization for bi-phase pseudo noise coded messages

employing synchronization preambles. An experimental matched filter and its reciprocal experimental sequence generator were to be designed, fabricated, and evaluated to provide verification of the selected technique of tap switching. The desired s' l characteristics of the experimental models are summarized in below.

Operating frequency	10 MHz to 300 MHz
Number of taps	127
Bit rate within burst	10 Mb/s
Burst duration	12.7 microseconds
Burst rate	1 burst each 6 milliseconds
Modulation	bi-phase (pseudo random PSK)
Code sequence library	127-bit subsequences from a 2^{34} -1 bit maximal length sequence (approx 10^{10}-bits)

3. PROGRAM SUMMARY

The experimental development program for the Switchable Acoustic Matched Filter was divided into three parts. Part I was six weeks in duration and consisted of:

a. An investigation of candidate surface wave delay line materials from a viewpoint of temperature stability, material cost and availability, overall insertion loss, shielding requirements and beam spreading effects.

b. An investigation of the available integrated circuits in chip form to insure that the components used in the fabrication of the hybrid electronic memory, switching and control logic were optimum considering: component availability, bonding and fabrication requirements, shift register power vs. speed, and switching circuit frequency response.

c. Preliminary design and layout of the ceramic substrate on which the microcircuits were to be bonded, interwired,and coupled to the acoustic delay line.

Part II was approximately six months in duration and consisted of: the detailed design and layout of the delay lines and the thin film ceramic substrates; the specification and procurement of all material; the final design and fabrication of the sequence generator and the corresponding matched filter; and the design and fabrication of the ancillary support/demonstration electronics.

Part III was approximately two months in duration and dealt with the preparation of the Air Force approved test plan, the bench testing and debugging of the experimental hardware, and the final testing, evaluation and acceptance of the acoustic devices.

This program successfully demonstrated the feasibility of combining an acoustic surface wave tapped delay line and hybrid assembled switching and control microcircuits to form a 127-bit, bit-by-bit switchable sequence generator and a corresponding matched filter. A summary list of the back-to-back performance of sequence generator and matched filter pair when processing a maximal length, 127-bit, bi-phase, pseudo noise code sequence is given below.

Insertion Loss	58.7 dB (peak in to peak out)
Processing gain	20.0 dB
Time Sidelobes	18.2 dB (aperiodic)
Center frequency shift	7.32 kHz per 30^{o}C differential
Compressed pulse amplitude change	0.6 dB per 30^{o}C differential
Code set-up time	25.4 microseconds
Pulse burst time interval	slow -6.0 milliseconds; fast 95.4 microseconds

An enlarged photograph of the 3" x 4" x 1-1/4" LWD switchable matched filter is shown in figure 1. The acoustic surface wave tapped delay line consists of ST-cut quartz with three gold deposited interdigital transducers. There are two input transducers at opposite ends of the delay line (under shields) comprised of six finger-pairs and a central 127-tap output transducer. The delay line is designed to operate at 60 MHz IF and 10 Mb/s code sequence rates.

Quartz was selected for the tapped delay line media primarily because of its low temperature coefficient and low coupling coefficient. The final design of the tapped delay line is based on a satisfactory tradeoff and balance of factors and considerations, such as: beam spreading, insertion loss, shielding and isolation, transducer impedance, mass loading, and amplitude weighting (droop).

The TTL shift register memory, logic control, and NPN switching transistors for a 32-tap subsection of the matched filter are assembled on a 3/4" x 1" x 1/32" ceramic thin film substrate. The hybrid assembly is comprised of individual integrated circuit chips that are cemented to the substrate and electrically connected via conventional gold wire ballbonds. The four subsections that comprise the 127-tap matched filter are packaged

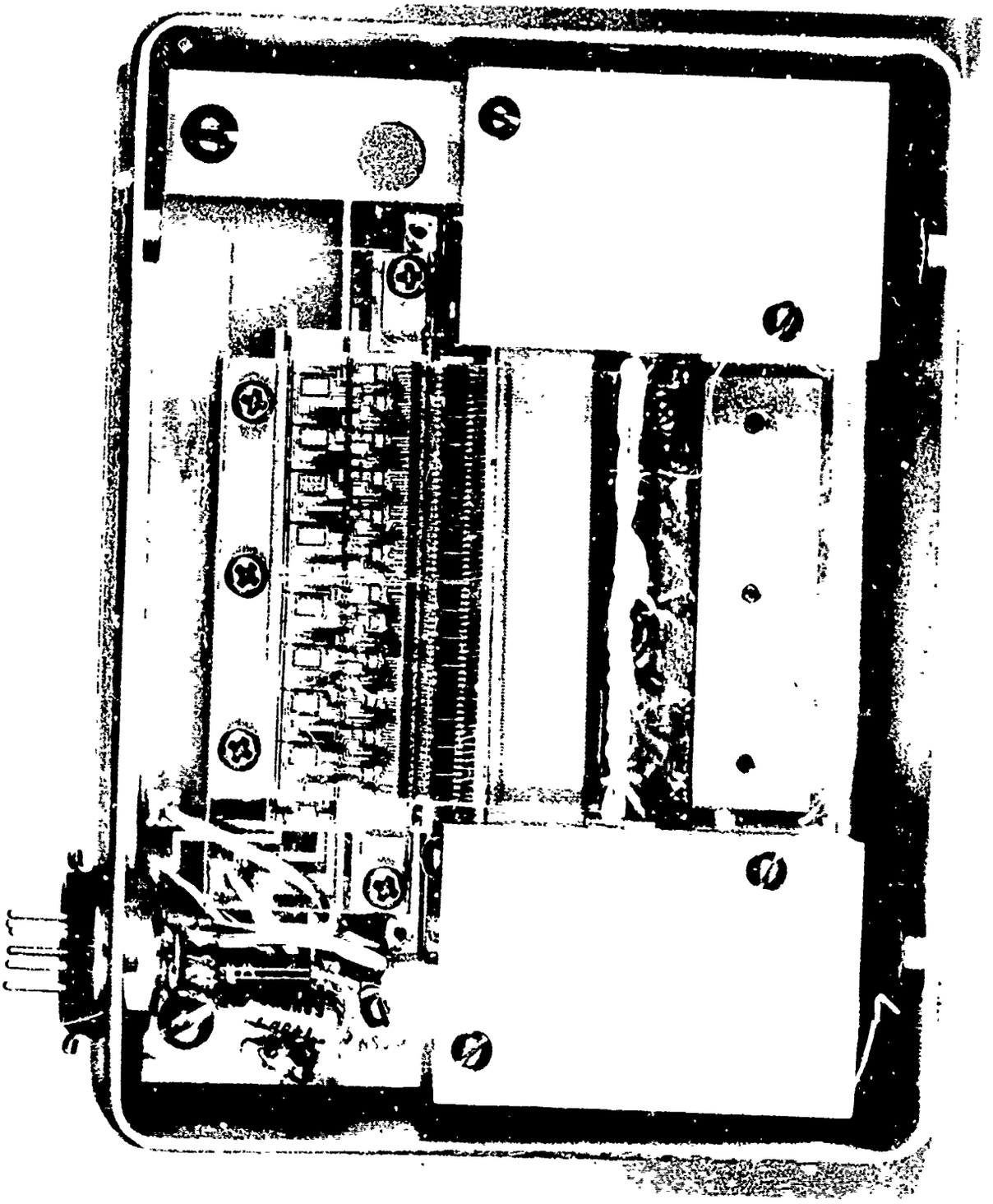


Figure 1. Photograph of Switchable Matched Filter

two deep and two across in order to interface the closely spaced (12.4 mils) delay line taps with minimum component/circuit fanout.

The experimental models developed and the techniques demonstrated on this program met all program objectives and goals. Continued development, miniaturization, and refinement of the hybrid digital memory and switching circuits is recommended. Five specific areas are identified: reduction of standby dc power dissipation; development of hybrid "building block" logic modules; reduction of insertion loss through active matching; development of alternative logic designs using parallel entry for very rapid code sequence switching; and assembly of "building block" modules to form a 512-bit switchable matched filter.

SECTION II

EXPERIMENTAL DEVELOPMENT PROGRAM

1. INTRODUCTION

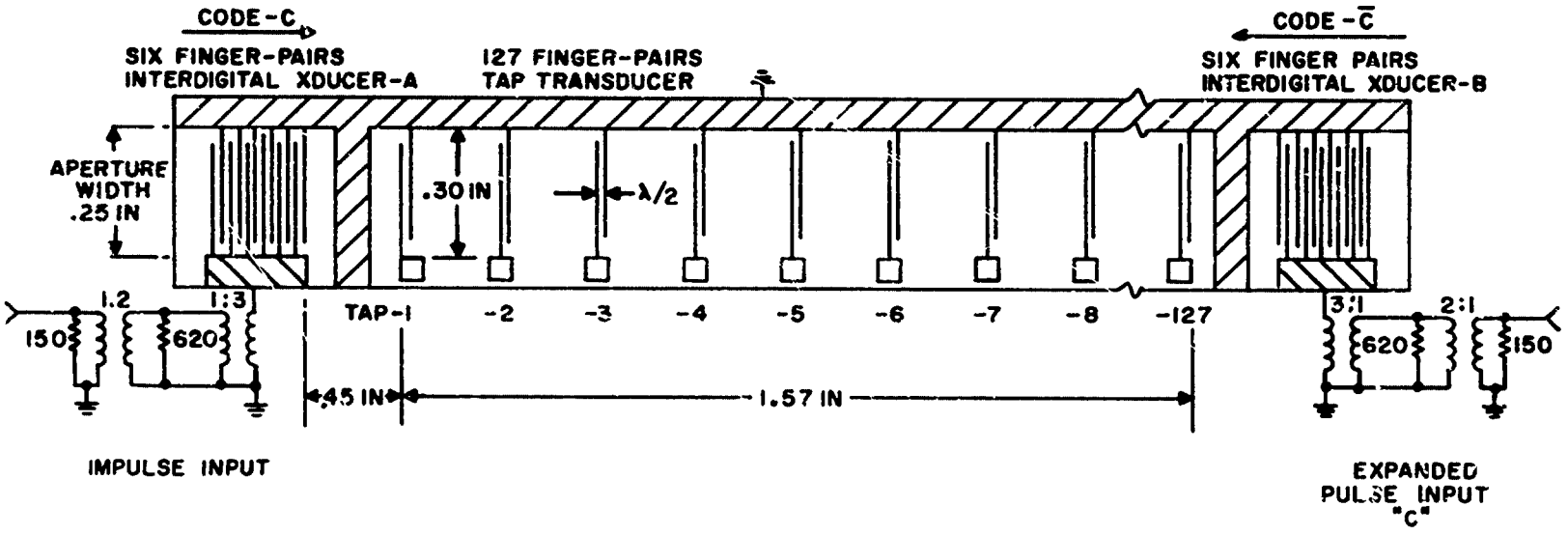
This section of the final report presents the results of the analysis and investigation, performed during Part I of the program, for the selection of candidate surface wave delay line materials and the hybrid, thin film, microcircuit memory and switching circuits. Also included is the design and fabrication information for the tapped delay and microcircuits developed during Part II of the program.

2. ACOUSTIC SURFACE WAVE TAPPED DELAY LINE

The tapped delay line material selected as a result of the material investigation is ST-cut quartz (Ref. 1) with propagation along the X-direction. The prime considerations in the selection of quartz are the low temperature coefficient, the low coupling coefficient, and the availability of material in long lengths. The low temperature coefficient eliminates the need for power consuming temperature stabilizing ovens. A low coupling coefficient minimizes signal dispersion and droop. Lengths of quartz are available up to 10-1/2 inches, at less than $200 in material cost, with which switchable matched filters up to 1000-bits at 10 Mb/s rates can be fabricated.

A diagram of the dual coded acoustic surface wave matched filter is given in figure 2. As can be seen in the figure, each output tap consists of deposited gold electrodes, a finger pair, one ground finger, and one active output finger. The finger pairs are spaced on $\lambda/2$ centers where the operating center frequency is 60 MHz. The spacing between the taps corresponds to 100 nanoseconds, or equivalently 12.4 mils. Each of the 127 output taps is brought out to a bonding pad for a gold wire connection to the external switching circuitry.

Each end of the acoustic delay line has an interdigital transducer (IDT) with 6 pairs of fingers. The theoretical amplitude response of the IDT is sinc x with a 4 dB bandwidth of 10 MHz and a null bandwidth of 20 MHz. This particular amplitude response was selected to optimally match the spectrum of a pseudo random sequence switching at a rate of 10 Mb/s. With an IDT at each end of the tapped delay line, the sequence generator and matched filter digital memory and switching logic can be simply programmed from a common source. The two units have identical tap polarity connections but one unit is the time inverse or matched filter of of the other unit by simply using the IDT at the opposite end. The input



NOTES:

① OPERATING FREQUENCY IS 60 MHZ

② TAP SPACING IS 100 NANOSECONDS (12.4 MILS)

Figure 2. Dual Coded Acoustic Surface Wave Matched Filter

signals to the IDTs are either an impulse at transducer A for generation of a 127-bit PSK signal, or the same PSK signal into transducer B for time compression.

3. DELAY LINE MATERIAL CONSIDERATIONS

The Microwave Acoustics Handbook (Ref 2) gives a great deal of information on the various crystals suitable for surface wave matched filters. Lithium niobate ($LiNbO_3$) and bismuth germanium oxide ($Bi_{12}Ge_{20}$) are desirable materials to use from the standpoint of impedance levels and insertion loss because of their large electroacoustic coupling. Low cost PZT ceramic is undesirable because of its high porosity and unavailability in long plates.

Since every tap must be connected to the external switching circuitry, the acoustic surface wave delay line must be in close thermal proximity to the power dissipated by the switching transistors and the logic elements. If lithium niobate were used as the acoustic surface wave medium, its large temperature coefficient of delay (93 ppm/^{o}C) would require that the sequence generator and matched filter operate at equal temperatures. For 60 MHz center frequency and 12.6 μs between first and last tap, there are 756 wavelengths. The response would null for a fractional delay change of 1/756 or 1.32×10^{-3}. For lithium niobate, a 14.2^{o}C temperature difference between the two lines would give such a null and the response would be 4 dB reduced for a 7^{o}C differential. It can be seen that the two lines would have to be held within a few degrees C of each other.

As an added problem, the 4.5 watts dissipation of the programming circuits would have to be included in a temperature-controlled enclosure. The heat loss rate would then have to be large enough to override the dissipation so that the temperature could be adequately controlled by a heater. The prevention and elimination of thermal "hot spots" with the microcircuit logic could become a difficult and time-consuming task not warranted on this program. ST-Cut quartz has a zero temperature coefficient of delay at room temperature, which eliminates the requirement for temperature control in a laboratory environment. The question to be answered at the outset of the contract was whether the low coupling constant and beam spreading of quartz could be tolerated. The answers to both questions were affirmative.

The untuned insertion loss of quartz lines is 40 dB higher than the same gold electrode pattern on lithium niobate (with a silicon monoxide film to adjust tap coupling), but with proper impedance matching networks some of this 40 dB insertion is recoverable. The beam spreading calculations were worked out for lithium niobate (y-cut, z propagating) and for ST-cut quartz using data provided by A.J. Slobodnik, Jr. of AFCRL.* The refractive index

*Private Communication

diagram for ST-cut quartz was approximated by an ellipse. The calculations can be summarized in the following discussion. At a given range, the radiation pattern for ST-cut quartz is identical to that of an isotropic medium if the broadside radiating aperture dimension (active finger length) on an isotropic substrate is made 0.855 of the aperture dimension on ST-cut quartz. Similarly, at a given range, the radiation pattern for lithium niobate is almost identical to that on an isotropic substrate, provided the radiating aperture on the isotropic substrate is 1.88 times the aperture on lithium niobate. Equivalently, the radiating aperture on ST-cut quartz should be 2.2 times the radiating aperture on lithium niobate in order to have the same radiation pattern. Pieces of ST-cut quartz of sufficient width are more easily obtained than the equivalent, narrower, pieces of lithium niobate, so there is no problem caused by the modest beam spreading. The extra insertion loss and the input-output shielding were examined and it was determined that they could be accommodated without serious deterioration of signal/noise ratio or dynamic range. Therefore, ST-cut quartz was selected as the acoustic surface wave tapped delay line material.

4. BEAM SPREADING CALCULATIONS

Actual mask dimensions are shown in figure 2. The end transducers have 0.250 inch radiating apertures. The longest path length is 2.02 inches. Figure 3(a) shows a circle whose center is the center of the most distant tap and which passes through the ends of an aperture whose dimension is 0.25 (0.855) = 0.214 inches. This is the equivalent aperture for isotropic material. The path length difference to the center of the aperture is given by

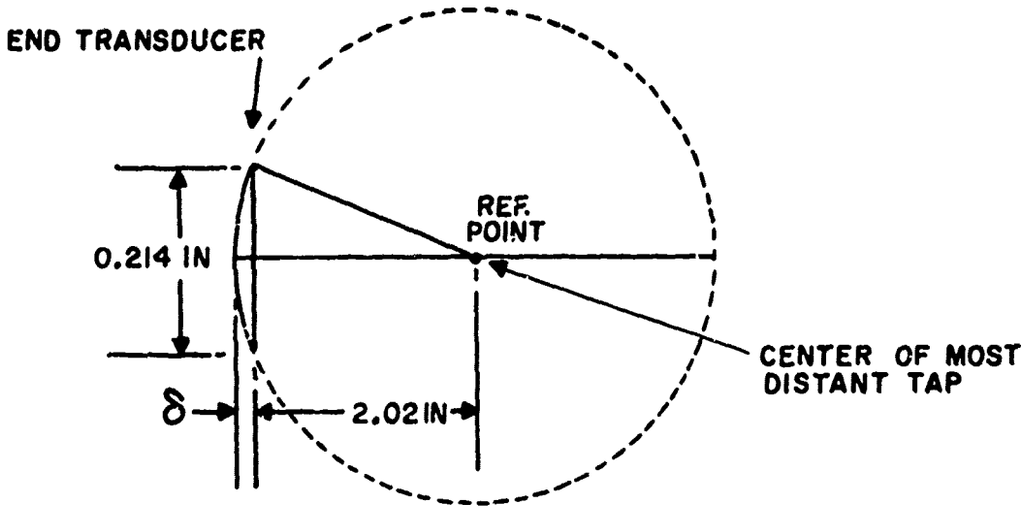
$$= (0.107)^2/4.04 = 0.00284 \text{ inch}$$

At 60 MHz, the wavelength is 0.1243/60 = 0.00207 inches. Hence the path length difference is 1.37 wavelengths. The vector contributions from the end transducer (considered to be the source) add up as shown in figure 3(b). These vectors form a Cornu spiral. The spiral is well wrapped, which means that the radiation pattern is sharply defined at the most distant tap.

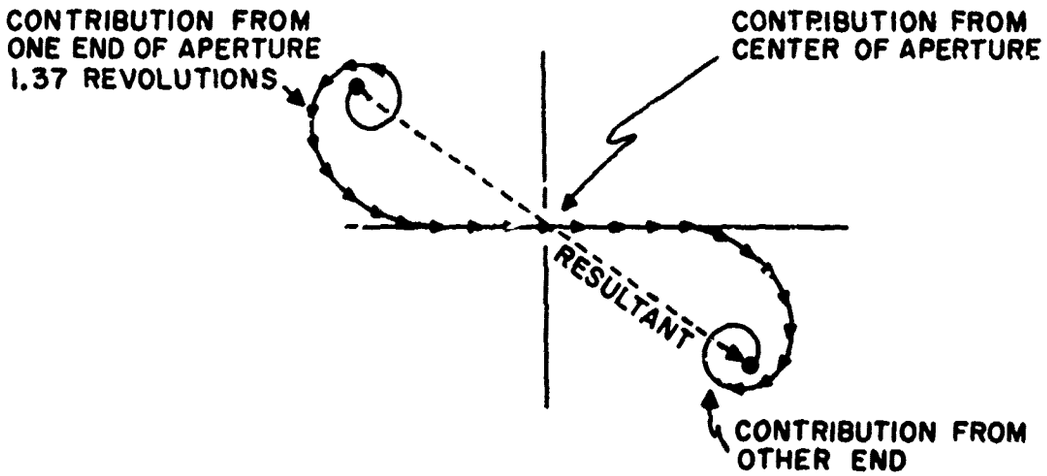
An equivalent statement is that the Fresnel number (Ref 3) is

$$N = (0.107)^2/\quad 2.02(0.00207) = 2.75$$

and the most distant tap is within the Fresnel diffraction region of the source.



(a) GEOMETRY FOR CALCULATING PATH LENGTH DIFFERENCE.



(b) VECTOR CONTRIBUTIONS OF DIFFERENT PORTIONS OF RADIATING APERTURE ON CENTERLINE.

Figure 3. Portion of Cornu Spiral Used in Aperture Design

The aperture could be smaller from the standpoint of radiation pattern, but the impedance levels would increase. The impedances presented by the taps and end transducers are discussed in the next section.

5. IMPEDANCE LEVELS AND INSERTION LOSS

a. End Transducers (IDT). The capacitance of the end transducer is given approximately by

$$C = K (\epsilon_r + 1) (2N-1) w$$

where K = 4.53 pF/meter for equal finger and space widths (Ref 4) and ϵ_r, relative dielectric constant, is 4.0 for quartz. N is the number of finger pairs and w is the radiating aperture width (active finger length). For 6 pairs of 0.250 inch long fingers, the calculated capacitance is 1.6 pF. The measured value for this transducer is typically 3.3 pF, showing that stray capacitance is appreciable.

The Q due to surface wave coupling is obtained from Smith et al (Ref 4) as

$$Q = (\pi/8N)(v/\Delta v)$$

where $\Delta v/v$ is 0.058×10^{-2} for ST-cut quartz and N = 6 for the end transducer. This Q value of 113 cannot be measured because the bulk wave radiation conductance and the electrode series resistance lowers the measured Q.

The active finger capacitive reactance at 60 MHz is 1660 ohms. The shunt conductance appearing across this capacitance due to the surface wave radiation is

$$1/1660 \times 1/113 = 5.3 \text{ micromhos}$$

The most optimistic estimate of total capacitance of this transducer with its wiring is 3.5 pF which has a reactance of 760 ohms. For a single tuned circuit, the loaded electrical Q should be 6 to get a 10-MHz 3-dB bandwidth. This requires a total shunt conductance of 220 micromhos, consisting mostly of generator conductance. The finger resistance and bulk wave conductances are swamped out by the generator.

The reflection coefficient for conversion to surface waves is

$$(220 - 5.3)/(220 + 5.3) = 1 - 0.048$$

and the reflection power loss converting from electrical power to surface acoustic wave is

$$1 - (1 - 0.048)^2 = 0.096 \text{ or } 10.2 \text{ dB}$$

The minimum theoretical loss converting from electrical power to acoustic wave going toward the taps includes another 3 dB due to bi-directionality, so the minimum loss is 13.2 dB.

The actual matching network used is shown in figure 2. When connected to a 50-ohm source, the two damping resistors reduce the available power by 2.1 dB. The network presents 920 micromhos to the transducer, resulting in a reflection loss of 16.7 dB. These two losses added to the 3 dB bi-directionality loss give a total insertion loss of 21.8 dB.

The extra loading of the input transducer results in better pulse fidelity at the expense of 8.6 dB more insertion loss.

The measured input impedance of the two IDTs, A and B, and the output impedance, as a function of frequency, for both the matched filter and sequence generator are given in figure 4 and figure 5, respectively. The nominal design value is 75 ohms at 60 MHz.

b. Tap Transducers. The capacitance of a 2-finger tap cannot be calculated from the formula from (Ref 4) because that formula applies to a periodic structure which is approximated by many finger pairs. The capacitance of 511 2-finger taps on quartz, in parallel, was measured. The result of the measurement is that each tap in the 127-bit switchable matched filter has a capacitance of 0.29 pF. The equivalent reactance is 9.2 kilohms.

The Q due to surface wave coupling is estimated by using N = 1 in the formula from Smith et al (Ref 5). This value is 680. The surface wave conductance in shunt with the tap transducer is 0.16 micromhos. With the common base switching transistor circuit, the entire available current of the transducer flows in the collector load circuit which presents 3.1 ohms to each collector. The insertion loss of the output taps from acoustic surface wave to collector load is the load power divided by the available power of the tap plus 3 dB loss for bidirectionality:

$$10 \log (4 R_L G_T) + 3 \text{ dB}$$

Where R_L is the load impedance (3.1 ohms) and G_T is the tap conductance. The tap insertion loss is 60 dB.

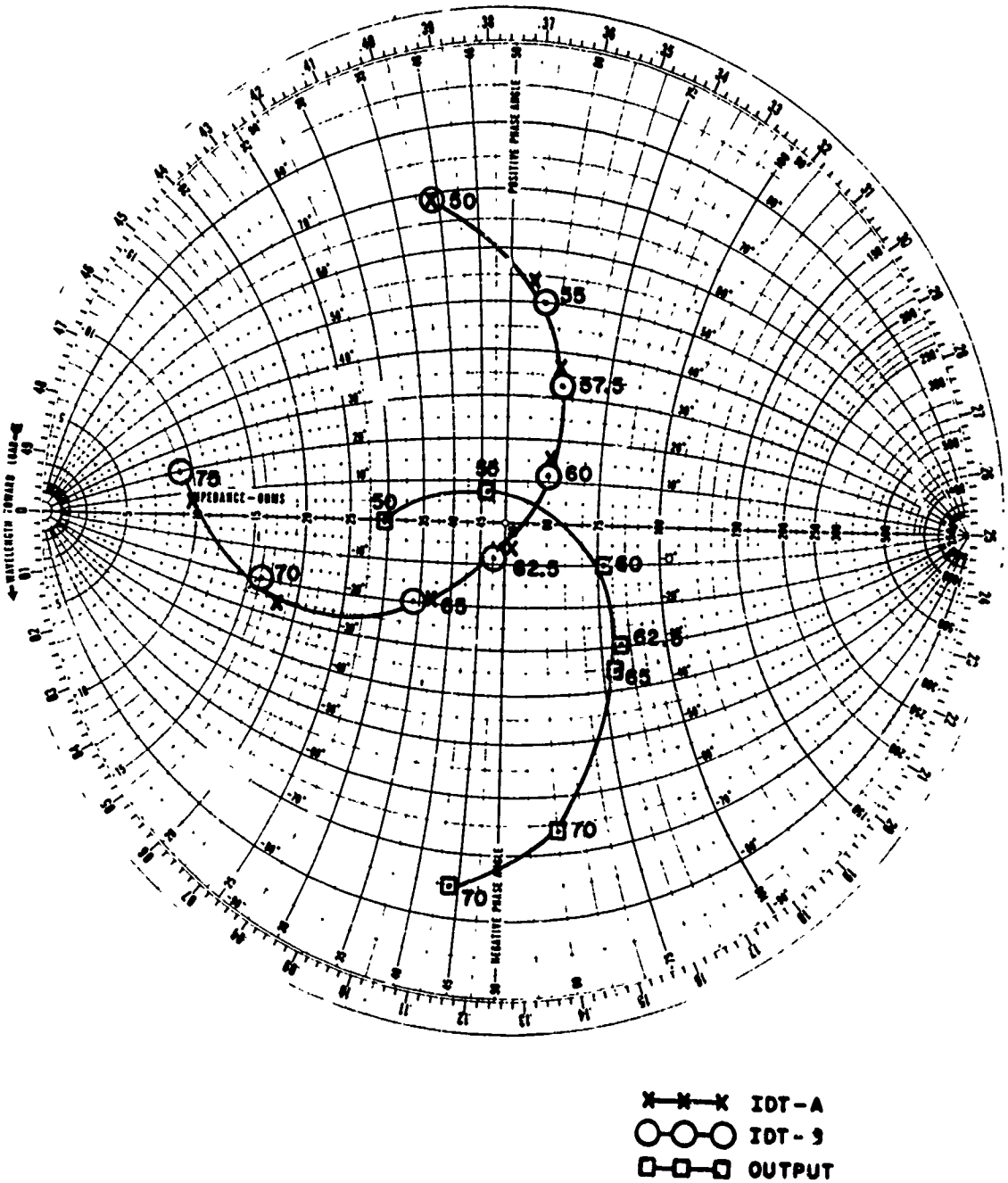


Figure 4. Matched Filter Input Impedance

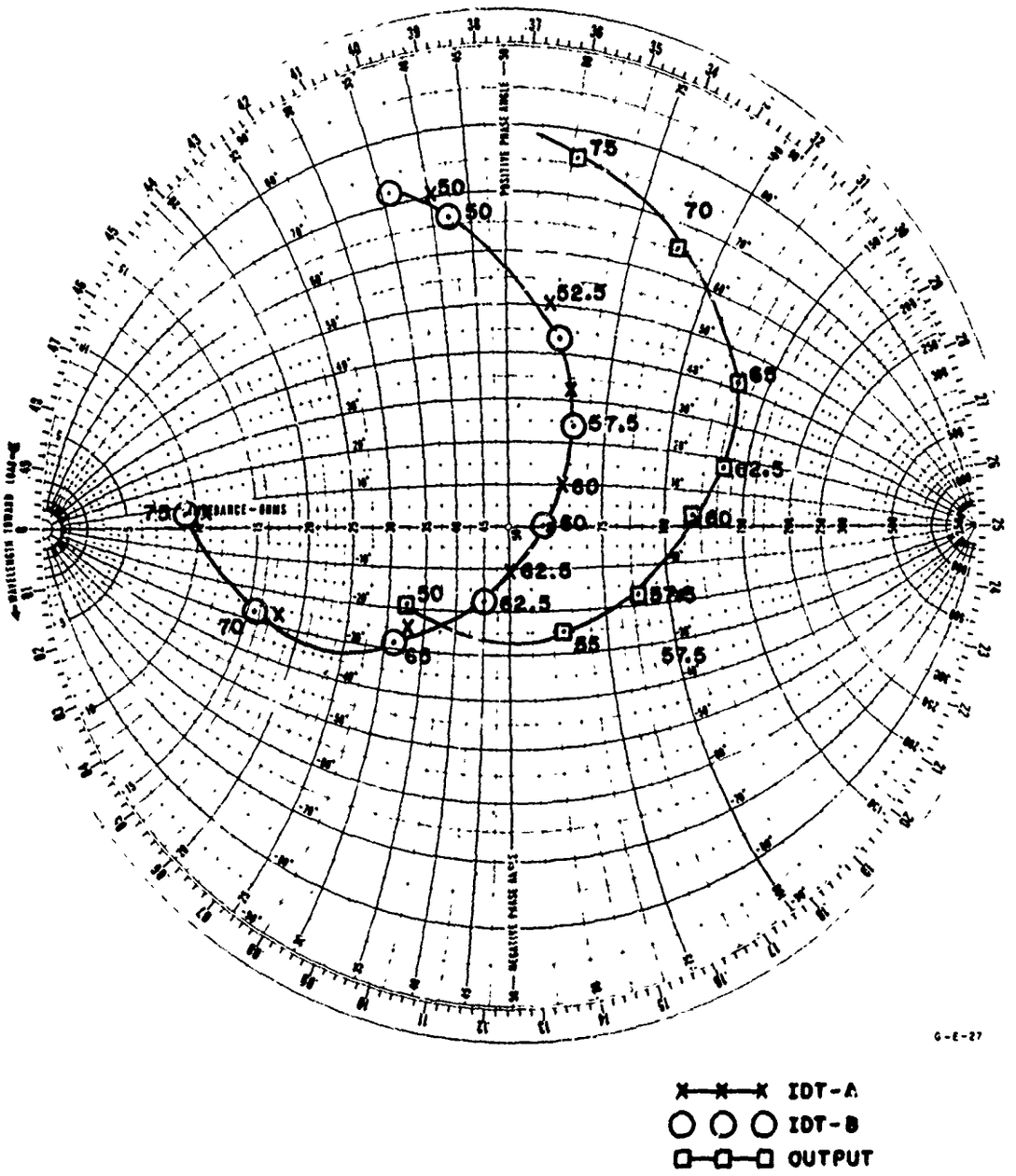


Figure 5. Sequence Generator Input Impedance

6. INSERTION LOSS AND SHIELDING

The insertion loss measured with a 70-nanosecond long 60-MHz pulse is 85 dB. Because the input transducer is 0.1 microsecond long, the 70-nanosecond pulse is only long enough to reach 70 percent of the acoustic wave amplitude which would be reached by cw input. The loss would be 82 dB if a single tap output could be observed on cw.

The calculated insertion loss is the sum of the 21.8 dB calculated in paragraph 5a and the 60-dB calculated in paragraph 5b. This gives exact agreement with the measured value of 82 dB.

The end transducers and their matching networks are enclosed in shield boxes to reduce direct feed-through to 80 dB. This is sufficient shielding to prevent direct leakage from affecting the autocorrelation sidelobes occuring before the main peak response.

7. FABRICATION DETAILS

The quartz plates used are ST-cut with propagation along the X-axis. The length is 3 inches, width 0.75 inch, and thickness 0.1 inch. The entire polished face (other side is saw cut finish) is covered with a chromium flash followed by 400 A of gold. The substrate was unheated. AZ 111 photo-resist was applied, spun, baked and exposed to collimated U-V light through an emulsion mask on a glass plate.

The mask was made as follows. Both end transducers and ten taps were cut in Rubylith at 100 X enlargement on a coordinatograph. Using the large Borrowdale camera, the negative artwork was reduced 5:1, except that extra taps were inserted between the end transducers by step-and-repeat with various parts of the rubylith masked off. Three contact printed (negatives) were made from the 5:1 intermediate, and these were cut and joined together to form the end transducers and 127-taps with bonding pads. The entire composite was reduced 20:1 in one shot to produce a positive emulsion mask. Ground shields between end transducers and taps were put in with opaquing tape. The ground bus for the taps was enlarged with opaquing tape.

After exposure the resist was developed and the gold was etched with an aqueous solution of iodine and potassium iodide. The gold pattern then served as the mask for the chrome etch.

Connection to input matching networks and tap switches is by means of 0.001 inch diameter gold wires. Ultrasonic ball bonds were made to the surface waveline bonding pads. Tail bonds were made to the ceramic hybrid plates and to the printed circuit board.

8. CONTROL AND SWITCHING MICROCIRCUITS

The control and switching microcircuits for the matched filter have been fabricated as thin film hybrid assemblies to be physically and electrically compatible with the surface wave line. Each tap on the surface wave line is connected to the switching circuitry by ball-bonded wire jumpers. Figure 6 is a basic schematic diagram of the tapped delay line, the control logic, and the transistor switches.

The control logic is operated by loading the desired code sequence into a 127-bit serial-in, parallel-out, shift register. Each output from the shift register is connected to an inverter stage in order to provide both Q and $\bar{Q}$ outputs for all bits of the code sequence. The Q and $\bar{Q}$ outputs are used to control the state of a two-transistor switch. This transistor-pair has the emitters connected together and to one of the taps on the surface wave device; the collectors are connected one each to the plus and minus summing buses. Each output of the shift register drives one transistor on and the other is off; thus, the transistor-pair acts as a single pole double throw switch to route the 60-MHz signal output of each delay line tap to either the plus or minus bus according to the code sequence stored in the shift register memory. The transistor switch has approximately unit gain and zero phase shift, so there is no degradation in the composite signal. The electronics associated with the 127-taps have the same amplitude and phase per path, since a random change in either amplitude or phase would result in a degraded signal-to-noise ratio due to mismatch.

The logic elements used are all TTL which has speed, moderate standby power, and noise immunity for this rapid serial load application. The shift registers are eight-bit serial-in parallel-out chips, and the register state complements are of necessity provided using additional hex inverters. The electronic switches are dual, dielectric-isolated transistor chips. Dual devices were selected so that each pair would be matched; dielectric isolation is used to keep capacitive coupling between the collectors of each pair to a minimum.

As a hybrid assembly, the control and switching circuits constitute an extremely large unit. The entire 128-tap assembly requires almost 170 chips (integrated circuits and dual transistors) and 1500 wire bonds per package. To keep yield losses at a tolerable level and the design and layout effort to a minimum, the circuits were designed to be made as four identical 32-bit sections or modules. In this way each module could be tested after every step in the fabrication sequence without paying too high a penalty to locate and repair malfunctions within the modules.

One of the primary constraints on layout is the necessity of avoiding differential phase errors between the taps due to different electrical path lengths,

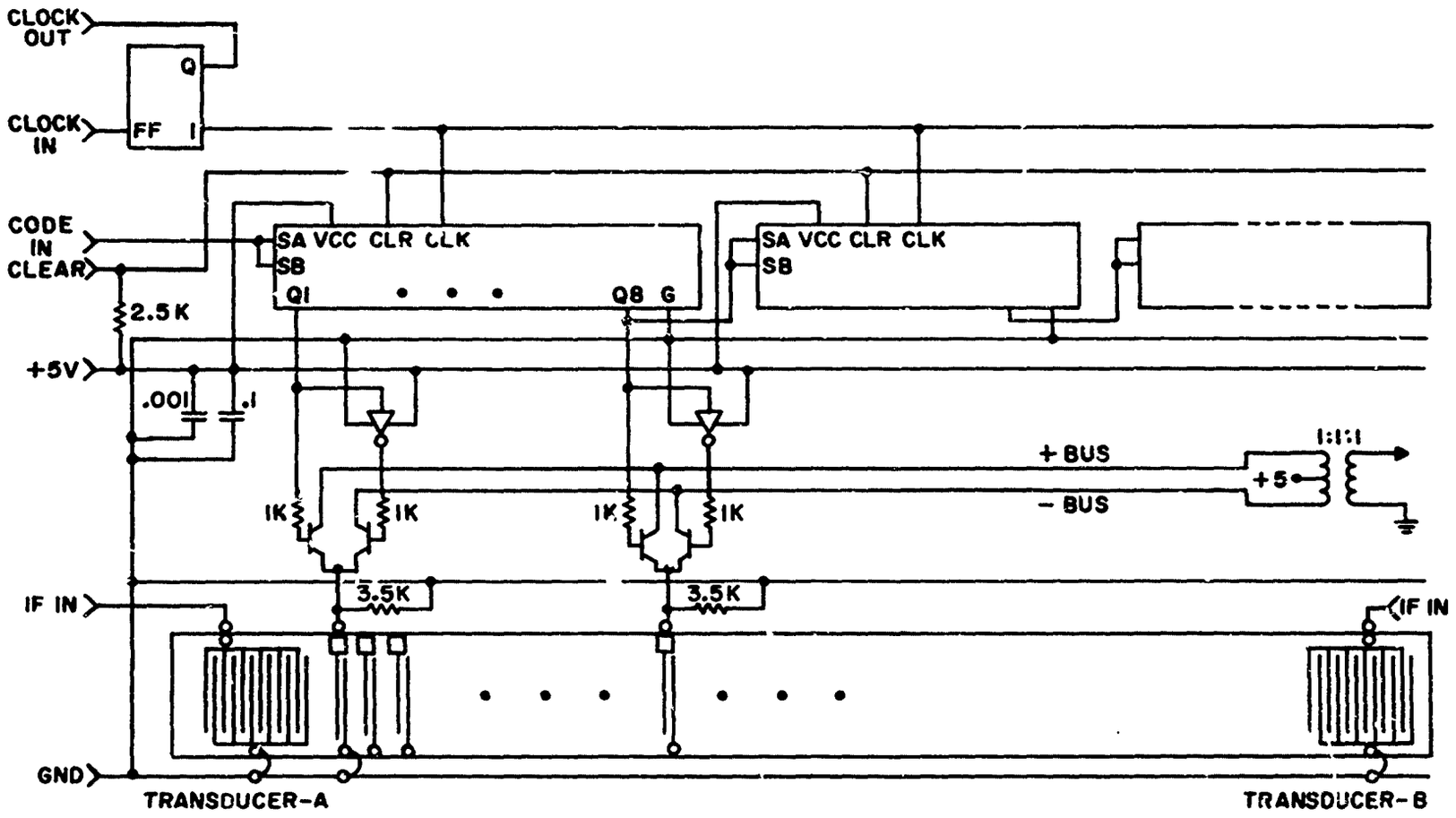


Figure 6. Matched Filter Switching and Control Circuits

stray capacitance and inductive leads from the acoustic surface wave taps via the transistor switches to the summing buses. The center-to-center spacing on the delay line taps is approximately 13 mils, and physical fan-out to suit the electronics cannot be used. The particular difficulty is that each tap requires an associated dual transistor chip, and these chips are 20 mils square. While it might be physically possible to get all these chips positioned in some form of staggered arrangement, this would violate the equal path length requirement. If the chips are placed in a row side by side, they line up well with every other tap on the delay line, but there is no room between the chips for conductors such that a double row could be used. The solution used in this design was to divide the control circuits in half and build them as a two-layered assembly. All the odd numbered taps are connected to the lower level and the even taps are connected to the upper level. This way the dual switching transistors are used in a single row and all electrical paths have the same length. In order to make this configuration of switch taps properly, the reference code sequence to the shift register memory must be routed to the proper level when loaded. This is simply accomplished by commutating the clock signal with a flip-flop. The reference code sequence being loaded is presented to both of the 64-stage shift registers on each level at all times, but the shift registers are alternately clocked by the flip-flop output, and so the bottom level contains all the odd bits and the top level all the even bits when loading is completed.

The modules were designed as thin film hybrids rather than thick film because of the high component density required both by the delay line dimensions and by the large number of interconnections used. In addition, to the 10 integrated circuits and 32 dual transistor chips on each module/substrate, there are also 96 resistors and all the interconnections between these elements. Hence, only thin film technology is tractable. The total power dissipated is 4.5 watts or about 35 milliwatts per tap.

The modules were fabricated by vacuum depositing gold over chromium films on glazed alumina substrates 1" x 1-1/4" x 1/32". Resistor and conductor patterns were delineated by the subtractive process of photo-resisting and selective etching of these two films. The chromium layer is deposition controlled to 100 ohms per square and, when etched, results in all resistors being matched to ±5 percent. All chips were attached using a conductive epoxy instead of attempting a Au/Si eutectic bond, since the yield anticipated from trying 42 eutectic bonds per substrate is virtually zero. All lead bonds required were made by ultrasonic ball bonding.

Each of the four substrates per unit was assembled and tested for proper operation of all logic and switches. The two substrates comprising the lower level electronics were attached to the printed circuit mounting board along with the quartz acoustic surface wave crystal. All necessary wire bonds were made at this level, and the unit was completely retested for logic

and switch operation, as well as checking the delay line performance. When th s level was found to be functioning correctly, the two modules for the second level were installed. Wire bonds were made to the crystal and to the upper level electronics. The completed unit was then checked. A photograph showing the detail layout of the substrates and the acoustic delay line is shown in figure 7. The assembly was then mounted in its 3" x 4" x 1-1/4" aluminum chassis, and the zener diode protective circuit elements were added at the power supply input to guard against catastrophic effects, e.g., reverse- or over-voltage accidentally being applied. No attempt was made to build this total device into a hermetic package at this time, since it is an experimental model. For reasonable protection, all semiconductor chips used were obtained with a glass protective layer on the top surface (except for the bonding pads) and an acrylic shield was attached over the entire hybrid circuit and delay line to protect it against damage during test, checkout, or inspection steps. The acrylic shield also serves to keep dirt and dust particles off the exposed surface of the delay line whenever the package is opened.

The microcircuit chips that are used in each of the 127-tap switching circuits and logic memories are as follows:

Function	Manufacturer		Die Size (inches)	Quantity
8-Stage SR	National Semiconductor Devices	DM8590	0.105x0.057	16
Hex Inverter	National Semiconductor Devices	DM7004A	0.037x0.052	24
Dual Transistor	Dionics, Inc.	DI3424	0.020x0.020	127
FF	Motorola, Inc.	MC5473F-2	0.054x0.060	1

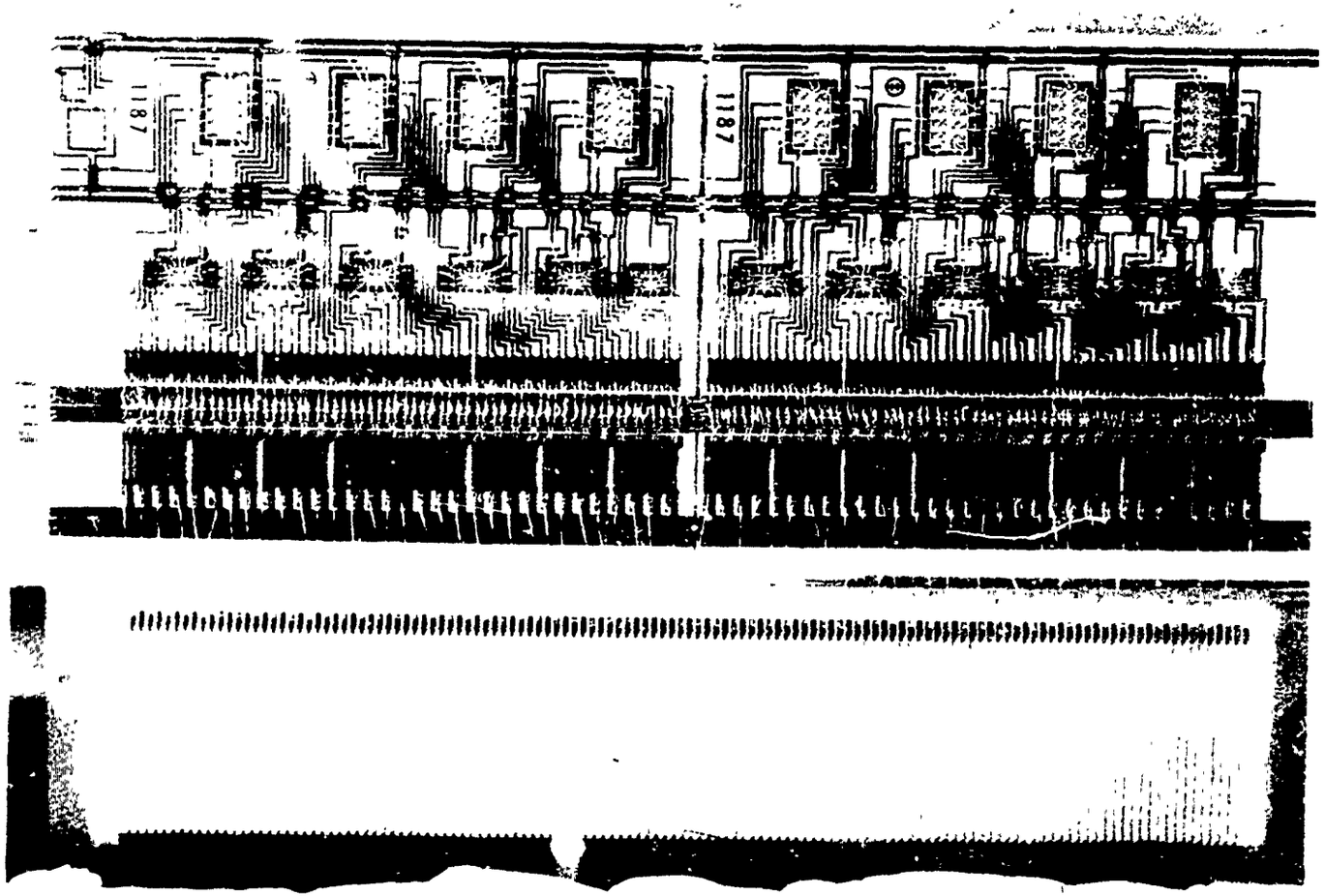


Figure 7. Enlarged Photograph of Substrates and Delay Lines

SECTION III

SYSTEM FUNCTIONAL DESCRIPTION AND OPERATING INSTRUCTIONS

1. FUNCTIONAL DESCRIPTION

The switchable acoustic sequence generator and matched filter system is comprised of four major units. The four units, shown in figure 8, are (1) the ancillary code generator and control unit (CG-CU), (2) the electronically switchable sequence generator, (3) the electronically switchable matched filter, and (4) the power supply.

a. Code Generator and Control Unit. The CG-CU provides all code set-up, digital programming, and impulse signals to operate, test and evaluate the entire system. The detailed logic diagrams and schematics for the CG-CU circuitry are given in Appendix II. The function and purpose of the CG-CU controls and signal outputs (see figure 8) are as follows:

PROGRAMMED CODE - Thirty-four front panel toggle switches are provided to establish the initial starting state of the 34-stage, m-sequence, code generator. The code generator provides the blocks of 127-bits which are used to program both the sequence generator and matched filter shift register memories.

RESET - A manual, one-shot, pushbutton which enables the timing generator. The RESET button should be depressed after dc power is turned on to ensure that the timing generator is not in the inoperative all-zeros state.

SHIFT - A manual switch which when set to ON routes the 5-MHz shift pulses to the 34-stage code generator and the 127-bit sequence generator and matched filter shift register memories. The sequence generator and matched filter shift register memories are reset or cleared when the SHIFT switch is OFF.

CG - A manual switch which when set to SHIFT enables the shift pulses to shift the code generator, and to load the programmed code into the code generator when set to LOAD.

MF - A manual switch which enables the 127-bit code and clock bursts to be fed to the matched filter, once each repetition cycle, when set to CONTINUOUS (with the SHIFT switch ON); when set to FIXED, it enables only one code and clock burst each time the SHIFT switch is moved from OFF to ON. At the burst rate of 5 Mb/s loading is completed in 25.4 microseconds.

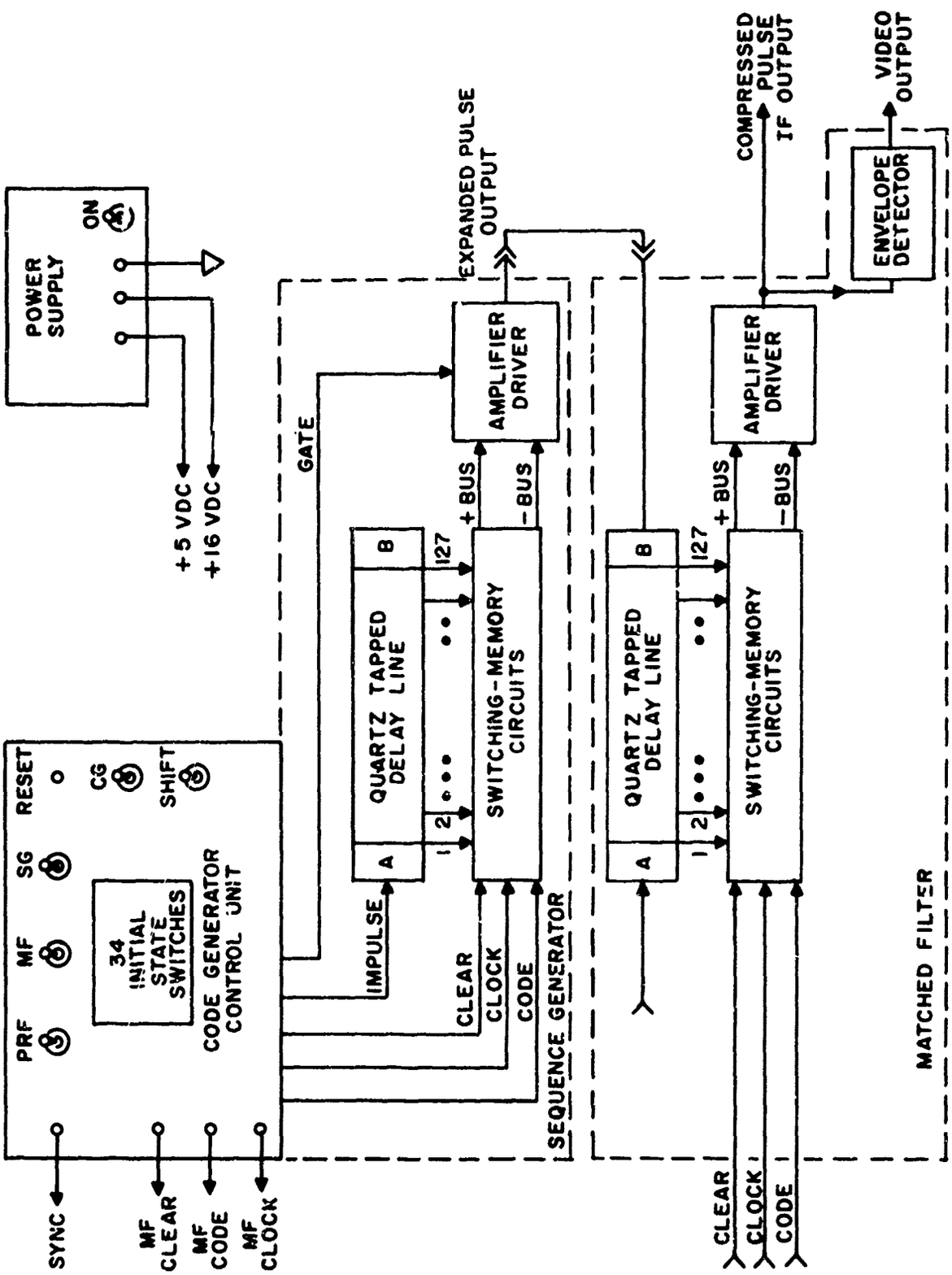


Figure 8. System Functional Block Diagram

SG - A manual switch is identical in function to the MF switch except that it controls the clock and code bursts into the sequence generator. With SG and MF switches set to CONTINUOUS, the burst repeats at the repetition rate. With the SG and MF switches on FIXED, one burst occurs every time the SHIFT switch is changed from OFF to ON. The single burst provides the means to load and hold a desired 127-bit code sequence, and manually change the programmed code sequence.

MF CODE - The output BNC terminal at which a burst of 127 bits of code are provided to program the switching and memory circuit of the surface wave matched filter.

MF CLOCK - The output BNC terminal at which a burst of 127 clock pulses at a 5-MHz rate is provided. The clock pulses are in time synchronism with the 127-bit code in order to serially clock the code into the matched filter shift register memory.

MF CLEAR - The output BNC terminal at which the logic zero is obtained, as required, to clear the matched filter shift register memory.

IMPULSE - The terminal within the CG-CU at which impulses, approximately 12 volts in amplitude and 5.0 nanoseconds in time duration at the half amplitude, are provided to drive the sequence generator which in turn generates the expanded phase-coded IF pulses. The impulse rate is set by PRF switch.

PRF - A manual switch which selects the rate at which the driving impulses are generated. The SLOW rate is one pulse every 6.0 milliseconds. A FAST rate of one pulse every 95.4 microseconds is provided to expedite measurement of processing gain, peak-to-sidelobe levels, and phase linearity of the matched filters.

SYNC - A timing pulse synchronized with the clock and the IMPULSE. The sync pulse is used to drive auxiliary test equipment, e.g., an oscilloscope.

Code, clock, and clear digital signals for programming the sequence generator shift register memory are provided via separable BNC cables within the CG-CU.

A low-noise, 5-stage, time-gated, 60-MHz IF amplifier is included as part of the CG-CU to provide amplification of the low level expanded pulse output (see Appendix II). The amplifier is gated ON during the generation of the expanded phase coded IF pulse.

The CG-CU is packaged in a BUD aluminum portacab cabinet, Model WA-1541, 12" x 6-1/8" x 9" DWH.

b. Sequence Generator and Matched Filter. The electronically switchable sequence generator and matched filter* units are electrically and mechanically identical. Each of these units is comprised of: a 127-tap quartz, acoustic surface wave delay line; 127 single-pole, double-throw, transistor switches; and a 127-bit serial-in parallel-out TTL shift register memory. A detailed description of these individual system components is given in Section II.

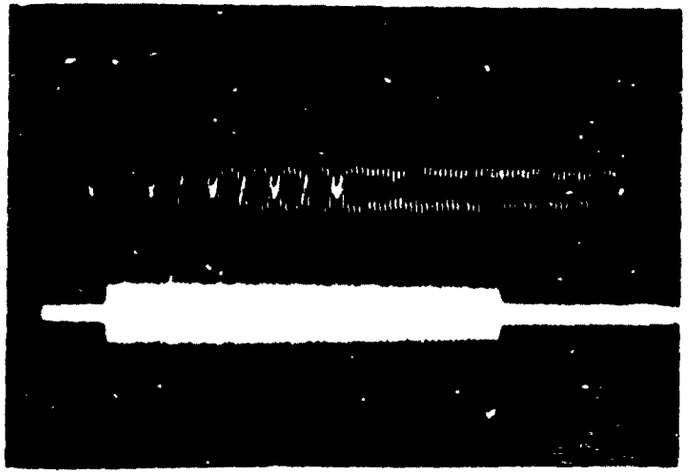
The quartz delay lines are designed to operate at 60-MHz IF and at a code sequence rate of 10 Mb/s. Each delay line has two identical 6-finger pair input transducers (IDTs); one IDT is at the beginning of the line and is identified as "A", and one at the end of the line identified as "B". The surface wave delay lines are bilateral. Thus, they can be driven from either input end. This feature provides a simple means of generating a phase coded expanded pulse and/or a corresponding "time-inverse" expanded pulse.

To generate a 60-MHz IF, bi-phase, coded expanded pulse of 127 bits, the sequence generator switching and memory circuits are preprogrammed via the CG-CU logic. Then, the IMPULSE is injected into IDT-A (or alternatively IDT-B). The output of the IDT is an acoustic pulse, which is essentially a rectangular, 6-cycle 60-MHz IF pulse burst which transverses the delay line surface. As the pulse burst encounters each of the 127 output taps, a small portion of the energy is coupled-out. The phase or polarity of the individual, but contiguous, 127 pulse bursts is determined by the programming and switching circuitry. The resultant output, after suitable amplification, is a 127-bit bi-phase coded pulse at 60-MHz IF.

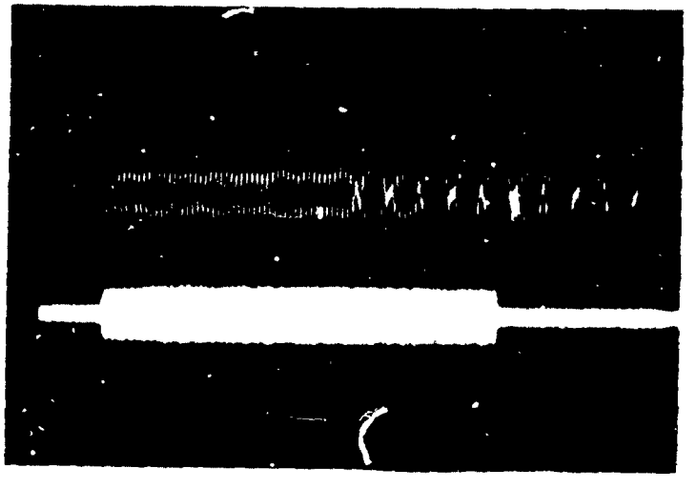
Illustrative photographs of typical expanded pulses are shown in figure 9. Figure 9(a), top trace, is a time expanded view of the impulse response of sequence generator No. 1, programmed for an arbitrary code sequence, with IDT-A as the input. The bottom trace of figure 9(a) shows the entire 12.7 microsecond expanded pulse. The essential features to note are the equal amplitude ones and zeros during the 101010...run and the relative flat, "droopless", response.

Figure 9(b) show the impulse responses, using the identical test setup, but the input is IDT-B. The response is virtually identical to that shown in figure 9(a) but is the "time-inverse". Figure 9(c) and figure 9(d) are the impulse responses of the sequence generator, programmed for an all ones code, i.e., a cw response, for the IDT-A and IDT-B inputs, respectively. For completeness, the identical set of photographs for sequence generator No. 2 are given in figure 10(a, b, c, and d). However, a different pseudo-random sequence was used to program the shift register memory.

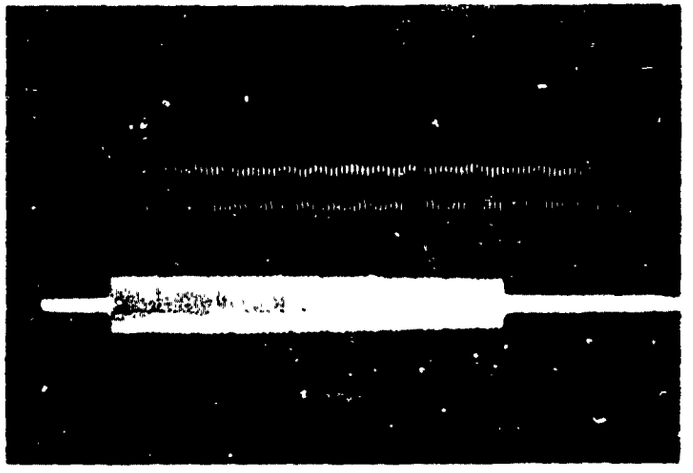
*The nomenclature sequence generator and matched filter are used interchangeably in this report.



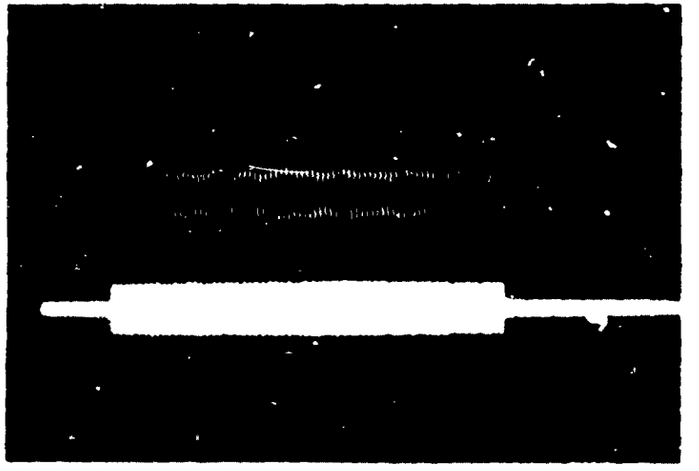
(a) input IDT-A, random code



(b) input IDT-B, random code

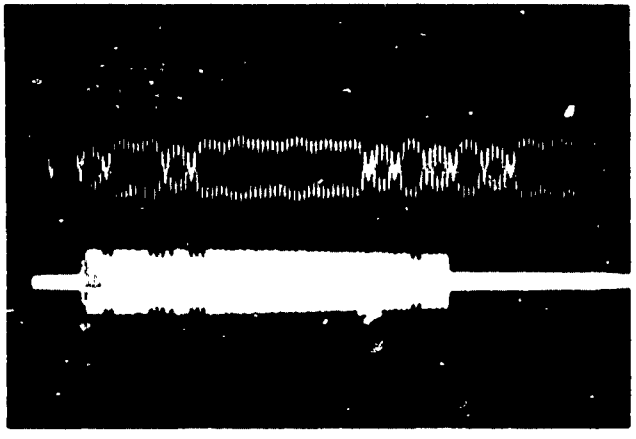


(c) input IDT-A, cw tone burst

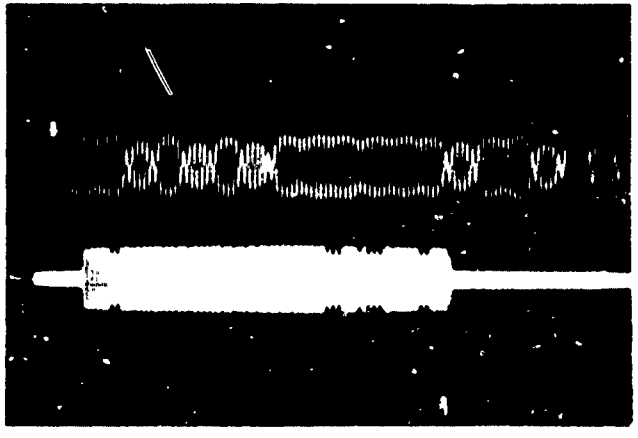


(d) input IDT-B, cw tone burst

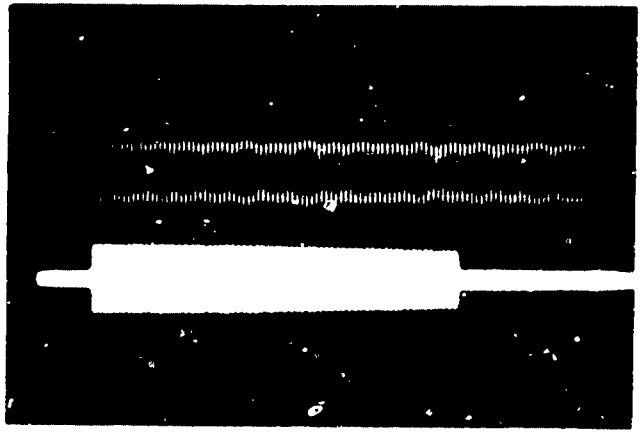
Figure 9. Impulse Responses for Sequence Generator No. 1



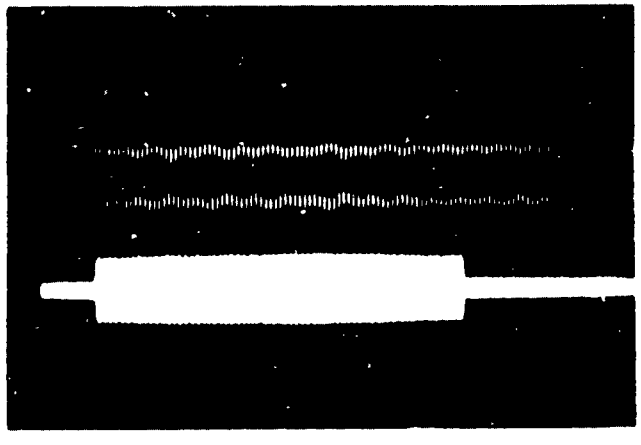
(a) input IDT-A, random code



(b) input IDT-B, random code



(c) input IDT-A, cw tone burst



(d) input IDT-B, cw tone burst
Sweep Speed: top, 20 ns/div
bottom, 2 μs/div

Figure 10. Impulse Responses for Sequence Generator No. 2

The sequence generator is packaged in a self-contained 3" x 4" x 1-1/4" aluminum box and is included within the CG-CU enclosure.

As noted previously, the sequence generator and matched filter units are identical. Thus, when both units are programmed to the identical code sequence they may be coupled back-to-back, using IDT-A on one unit and IDT-B on the second as the signal inputs, to form a complete expansion and matched filter time compression system. Basically, the matched filter performs the function of maximizing the peak signal-to-rms noise at a specific time, and in its elementary form, is simply a device whose impulse response has the same shape as the input signal, (delayed by some arbitrary fixed delay) but is time reversed.

The back-to-back performance of the experimental expansion-compression system is graphically illustrated in the photographs shown in figure 11. Figure 11(a) shows the classic compressed pulse response for an uncoded, cw, 12.7-microsecond tone burst. (See figures 9(c,d) and 10(c,d)).

Figure 11(b) is the compressed pulse time response corresponding to an expanded pulse of 32-ones, 32-zeros, 32-ones and 31-zeros.

Figure 11(c) shows the compressed pulse resulting from the processing of a pseudo random m-sequence. Of necessity, the 127-bit m-sequence used for programming was generated by external test equipment.

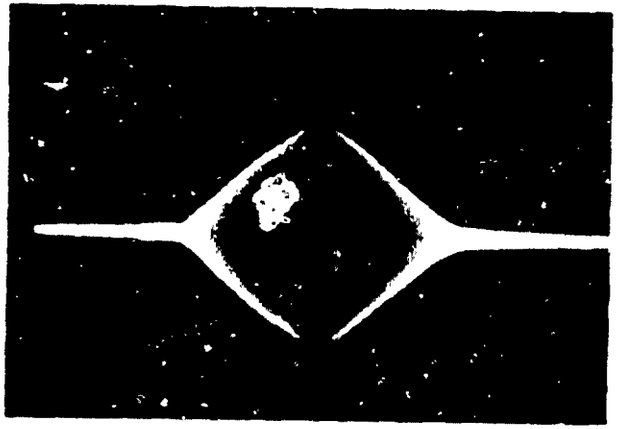
Figure 11(d) shows the RMS time sidelobes and the peak response of the system as the programmed 127-bit sequences are continuously changing every 95.4 microseconds.

The electronically switchable matched filter and a 4-stage, 60-MHz IF, output amplifier and envelop detector (see Appendix II) are packaged in a BUD aluminum portacab cabinet, Model WA-1540, 9" x 6-1/8" x 8", DWH.

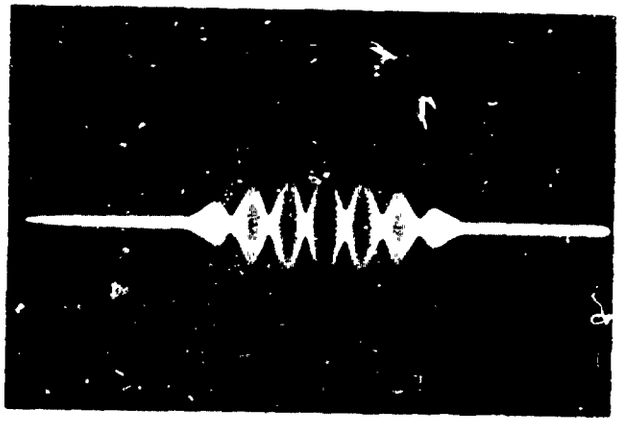
c. Power Supplies. The dc voltages required to operate the system are +5.0 volts for the logic and +16.0 volts for the analog electronics. The dc power is provided by standard Lambda modular power supplies, Model numbers, LM-234 and LCS-3-02 which include overvoltage protectors LM-OV-1 and LC-OV-10, respectively. The power supplies are enclosed in a BUD aluminum portacab cabinet, Model WA-1541, 12" x 8-1/8" x 9", DWH.

2. SYSTEM OPERATING INSTRUCTIONS

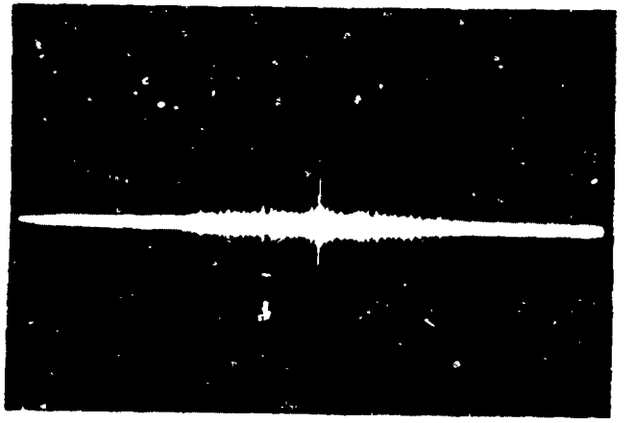
The ancillary electronics, code generator and control unit, sequence generator and matched filter units, which comprise the experimental system, are designed for the three modes of operation described in the following.



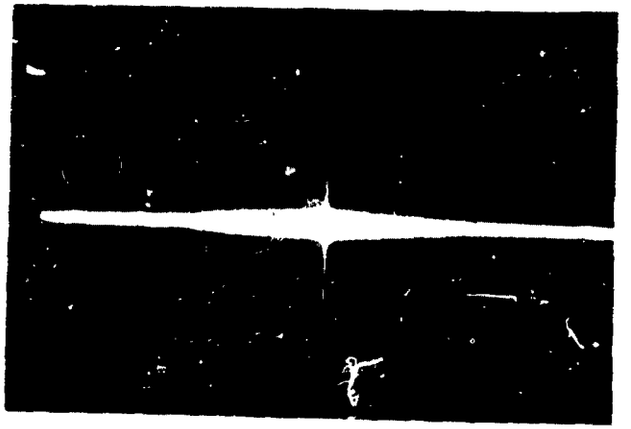
(a) 12.7 μs, cw, tone burst



(b) coded burst of 32 ones, 32 zeros, 32 ones and 31 zeros



(c) pseudo-random, 10 Mb/s, m-sequence



(d) repetitive sequences
Sweep speed: 5 μs/div

Figure 11. Representative Autocorrelation Functions

CONTINUOUS AUTO - wherein both the sequence generator and matched filter are identically and simultaneously reprogrammed at the pulse repetition rate such that the resultant output is a series of time overlapped autocorrelation functions, (see figure 11(d)).

CONTINUOUS CROSS - wherein only the sequence generator (or the matched filter) is reprogrammed at the pulse repetition rate, while the matched filter programming remains fixed, such that the resultant output is a series of cross-correlation functions.

FIXED AUTO - wherein both the sequence generator and matched filter are identically programmed, and the programmed code remains fixed, such that the resultant output is a particular autocorrelation function at the pulse repetition rate (see figures 11 a, b, and c).

Initially, to operate the system in any one of the three modes, interconnect all signal, timing and synchronizing cables as shown in figure 8 and turn dc power ON, then depress RESET and set PRF to either FAST or SLOW.

To operate in the CONTINUOUS AUTO mode, set the MF and SG switches to CONTINUOUS, the SHIFT switch ON, and the CG switch to SHIFT.

To operate in the CONTINUOUS CROSS mode, set the MF switch to FIXED and the SG switch to CONTINUOUS or vice versa, the SHIFT switch ON, and the CG switch to SHIFT.

To operate in the FIXED AUTO mode proceed as follows:

a. Set the 34-initial state switches to the desired positions (corresponding to the code sequence to be evaluated);

b. set the CG to LOAD and the MF and SG switches to FIXED;

c. depress SHIFT switch from ON to OFF (and if necessary from OFF to ON to OFF);

d. set the CG switch to SHIFT and adjust the SHIFT switch from OFF to ON.

The code sequence used in the FIXED AUTO mode can be changed by repeating the same procedure step-by-step. Additionally for demonstration purposes, the programmed code sequence can be simply changed by depressing the SHIFT switch from ON to OFF which clears the memories and programs an all-zeros code sequence, then setting the SHIFT switch from OFF to ON.

SECTION IV

PERFORMANCE TEST RESULTS

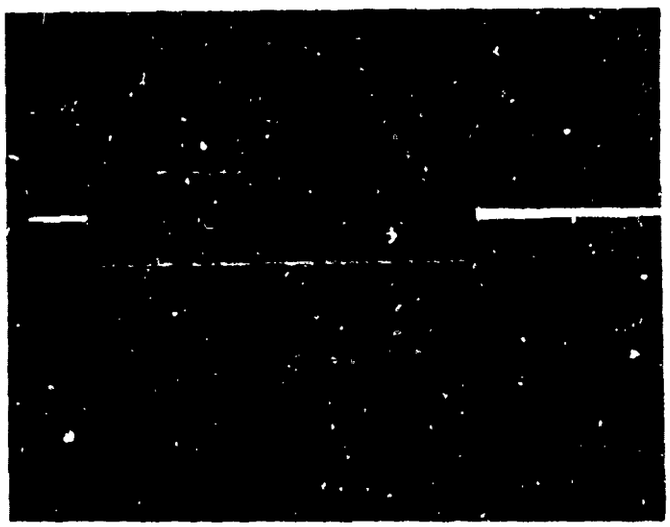
1. SCOPE

This section discusses and presents the results of the preliminary performance tests and the final acceptance tests for the switchable sequence generator and matched filter. During the initial, back-to-back, system performance tests, it was ascertained that spurious coupling, within the hybrid microcircuit switching and control logic, was causing a degradation in time sidelobe performance. The probable cause and the compensation technique use to eliminate the problem are described.

2. PRELIMINARY PERFORMANCE TESTS

During the preliminary performance tests for the experimental system, it was determined that the matched filter autocorrelation peak-to-sidelobe ratio, when using a 127-bit aperiodic m-sequence, was within 1 dB of theoretical. Initially, for this particular test, the 10-Mb/s bi-phase coded test signal, at 60-MHz IF, was generated actively using standard Hazeltine test equipment. The test signal is shown in figure 12(a) and the resulting compressed pulse is shown in figure 12(b). However, the peak-to-sidelobe ratio was degraded by about 6 dB when the test signal was passively generated using the switchable sequence generator as the signal source. As a result of further testing, it was shown that the degraded peak-to-sidelobe ratio condition could also be produced by a modified active test system. The modification to the active test system was the addition of a coherent, 60-MHz, cw signal to the normal phase coded test signal at a 10-dB lower power level. The cw interferrer was adjusted from 0 to 90 degrees relative to the phase coded carrier and no significant difference in sidelobe level was evidenced. This simple test verified the assumption that the switchable sequence generator was generating a low level coherent cw signal in addition to the programmed pseudo random PSK sequence.

As a result of subsequent investigations and tests, it was concluded that the cause of the spurious cw signal within the hybrid microcircuit was due to a combination of effects which can be generally categorized as electrical and mechanical dissymmetry or unbalance. For example, the plus bus and minus bus summing rails have different resistive impedance resulting from a somewhat different line width. The line width difference also results in a different inductance per unit length, which becomes more significant when the reactive coupling across the junctions of the dual switching transistors to the bus rails is included. The location of the pads on the microcircuit substrate to which the tap delay line outputs are bonded adjacent to only

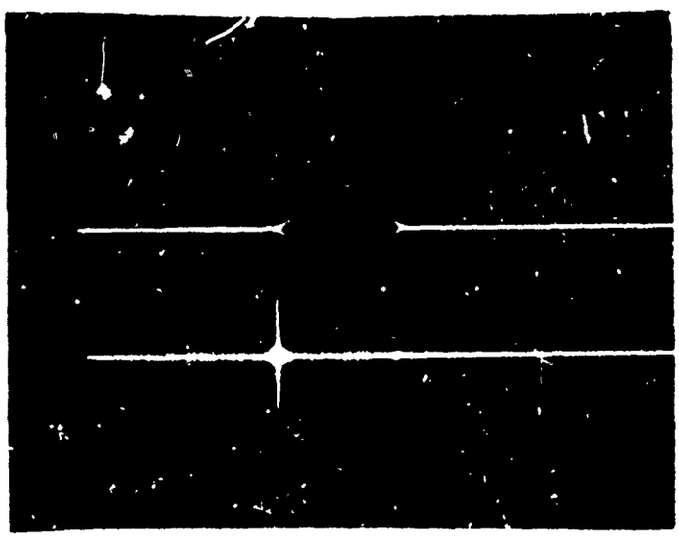


Sweep Speed

5 μs/cm

100 ns/cm

(a) expanded phase-coded sequence



Sweep Speed

100 ns/cm

5 μs/cm

(b) compressed pulse output

Figure 12. Photograph of Phase-Coded Sequence and Compressed Pulse

one bus rail, and the positioning of the dual transistor chips, over the summing buses, favors this bus rail.

Since the spurious coupling is reactive, the phase of this coupled signal to both the plus bus and minus bus summing rails, is changed from the 0 and 180 degrees relationship of the normal signal through the legitimate paths to the rails. This phase differential, and the magnitude differential, of the coupled signals to the summing rails prevents the spurious signal from being subtracted or cancelled in the balanced output summing transformer. To compensate for the spurious coupling, the plus and minus buses of the programmable matched filter were individually phase and amplitude weighted using experimentally determined RC networks. This practical compensation technique was highly successful, as evidenced by the duplication of the peak-to-peak-sidelobe ratio (within 0.8 dB) for the acoustically generated test signal, as referenced to the "standard of comparison", the actively generated test signal.

3. FINAL ACCEPTANCE TESTS

The final acceptance tests for the experimental system consisted of a series of measurements on the individual units and/or the back-to-back combination. The following measurements were taken:

Insertion loss
Phase shift vs frequency
Temperature sensitivity
Peak-to-sidelobe ratio
Processing gain
CW interference.

The test data resulting from these measurements is summarized in the tabulation below.

INSERTION LOSS	Test Source		Loss	
	Active		57.5 dB	
	Acoustic		58.7 dB	
	Includes compression gain: 20 log 127 = 42.1 dB			
TEMPERATURE SENSITIVITY	Temperature Deviation	Frequency Deviation	Loss in Peak Output	Loss in Sidelobe Ratio
	$30^{\circ}C$	7.32 kHz	0.6 dB	1.0 dB

SIDELOBE RATIO	Test Mode	Test Source	Peak-to-Sidelobe Ratio
	Periodic	Active	24.2 dB
	Aperiodic	Active	19.0 dB
	Aperiodic	Acoustic	18.2 dB
	Theoretical aperiodic sidelobe ratios:		19.8 dB
PROCESSING GAIN (Gaussian Noise)	Test Source		Processing Gain
	Active		18.9 dB
	Acoustic		19.4 dB
	Theoretical limit: 10 log 127 = 21.05 dB		

A summary description of all the measurement methods and the results from the temperature sensitivity and cw interference measurements are given in subparagraphs a through f below.

4. MEASUREMENT METHODS AND RESULTS

a. Insertion Loss. The insertion loss of the switchable matched filter was determined by simultaneously measuring the peak-to-peak voltage of the expanded pulse fed into the matched filter (from either the active or acoustic sequence generator) and the compressed pulse output. The ratio between the signal levels is by definition a measure of insertion loss. This measurement includes the compression gain. The midband CW loss, on a per tap basis, would be reduced by the voltage compression gain of 42.1 dB.

b. Temperature Sensitivity. The temperature sensitivity of the switchable matched filter was determined by placing the unit in an oven and measuring the change in center frequency as a function of temperature. This measurement was made by using the active sequence generator as a test source. By varying the center frequency of the test source for the largest compressed pulse output, the effective change in the center frequency of the matched filter as a function to temperature was determined.

The voltage level of the compressed pulse at the output of the matched filter was also measured over temperature with the input test signal derived from the acoustic sequence generator (kept at room temperature). Since, the 4-dB doppler bw of the matched filter is 78.8 kHz and the response varies as sinc x with frequency, the measured variation of ±7.32 kHz would result in a change in compressed pulse voltage amplitude of 0.12 dB. Therefore, the actual measured loss of 0.6 dB is not all attributable to the frequency deviation but is a result of an increase in the insertion loss with temperature and/or measurement accuracy.

c. Peak-to-Sidelobe Ratio. The peak-to-sidelobe ratio of the matched filter compressed pulse output was measured using both the switchable acoustic sequence generator and the active test generator as signal sources. Both the sequence generator and the test generator were programmed to generate a pseudo random m-sequence, with known autocorrelation properties. The sequence generator and matched filter were initially pro grammed by the test generator, rather than internally, because the experimental system, of itself, has no provision to generate m-sequence programming codes. The test results (paragraph 3) for the aperiodic active and acoustic test modes, show that the measured peak-to-sidelobe ratios were within 0.8 dB and 1.6 dB of the theoretical 19.8 dB, respectively.

d. Processing Gain. The following presents a summary of the calculations for determining processing gain and describes the procedure that was used in the actual measurements:

The processing gain, ρ , is defined as

$$\rho = (S/N)\text{out}/(S/N)\text{in} \tag{1}$$

where $(S/N)\text{ out} = E/N_o$ (2)

if the input is (non-band limited) white Gaussian noise

$$(S/N) = E^2 / \left[N_o \frac{1}{\pi} \right] \int_a^b S(\omega)^2 \, d\omega \tag{3}$$

where a and b are the band limits of the signal.

E is the signal energy.
$S(\ )$ is the voltage spectrum of the signal.
N_o is the one-sided noise density.

The input signal-to-noise ratio is

$$(S/N)\text{ in} = (E/T)/(N_o B_N) \tag{4}$$

if the input is (non-band limited) white Gaussian noise. Where B_N is the noise bandwidth of the matched filter, defined as

$$B_N = \left[\int_0^\infty H(\omega)^2 \, d\omega \right] / H(\omega)^2_{max} \tag{5}$$

In equation (5), $H(\omega)$ is the transfer function of the filter and

$$(S/N)\text{ in} = \frac{E/T}{N_p \dfrac{\int_a^b H(\omega)^2 \, d\omega}{H(\omega)^2_{max} \; b - a}} \tag{6}$$

for band limited noise where N_{pin} is the power of the band limited noise.

The test system for measuring processing gain is shown in figure 13. The S/N_{in} was obtained (1) by measuring the sequence generator voltage output and duration with an oscilloscope, (2) measuring the noise power at the input to the matched filter with an rf voltmeter, then calculating

$$\int_a^b \operatorname{sinc}^2 \omega \quad d\omega \tag{7}$$

where a and b are the band limits of the noise source and the transfer function of the matched filter is $\operatorname{sinc} \omega$.

The S/N_{out} was obtained by determining the probability of detection and probability of false alarm output of the fixed threshold circuit. The probability of false alarm was determined by measuring the voltage at the output of the threshold circuit in the "noise only" case, since the voltages for no false alarms and for all false alarms was readily measured and linear interpolation holds. To eliminate spurious threshold crossings (during measurements of the probability of detection) the output of the threshold circuit was gated on at the known epoch time of the pseudo-random m-sequence. The number of threshold crossings at the epoch time were counted by an electronic counter and compared to the total number of possible threshold crossings to yield the probability of detection. The processing gain, , was determined from this data. As an expedient, the noise source used in the processing gain measurement was 30 MHz wide which results in an equivalent noise bandwidth of 9.32 MHz out of the quartz delay line input transducer (IDT)(the IDT has a sinc x response and a 20 MHz null bandwidth). So the reading of the noise power was simply divided by a 30/9.32 (or 3.22) correction factor to compensate for the bandwidth of the noise source. The measured processing gain for the experimental system is within 0.6 dB of theoretical.

e. CW Interference. The technique employed to determine the effects of CW interference on processing gain involved measurements of the J/S ratio at the input and the output of the acoustic matched filter. (The matched filter was programmed to process the test m-sequence.) The data presented is based on measurements of peak-to-peak signals at these points. The results of the tests, summarized in figure 14, show the J/S ratio out as a function of frequency for a constant 0 dB J/S ratio at the input to the matched filter. It is significant to note that there are several deep nulls where a cw jammer could be rendered ineffective.

f. Phase Shift vs Frequency. The phase shift between the input interdigital transducers A and B of the matched filter was measured using a H.P. Vector Voltmeter. The results of this measurement, given in figure 15, show that the acoustic tapped delay line has a linear phase characteristic over the band of interest.

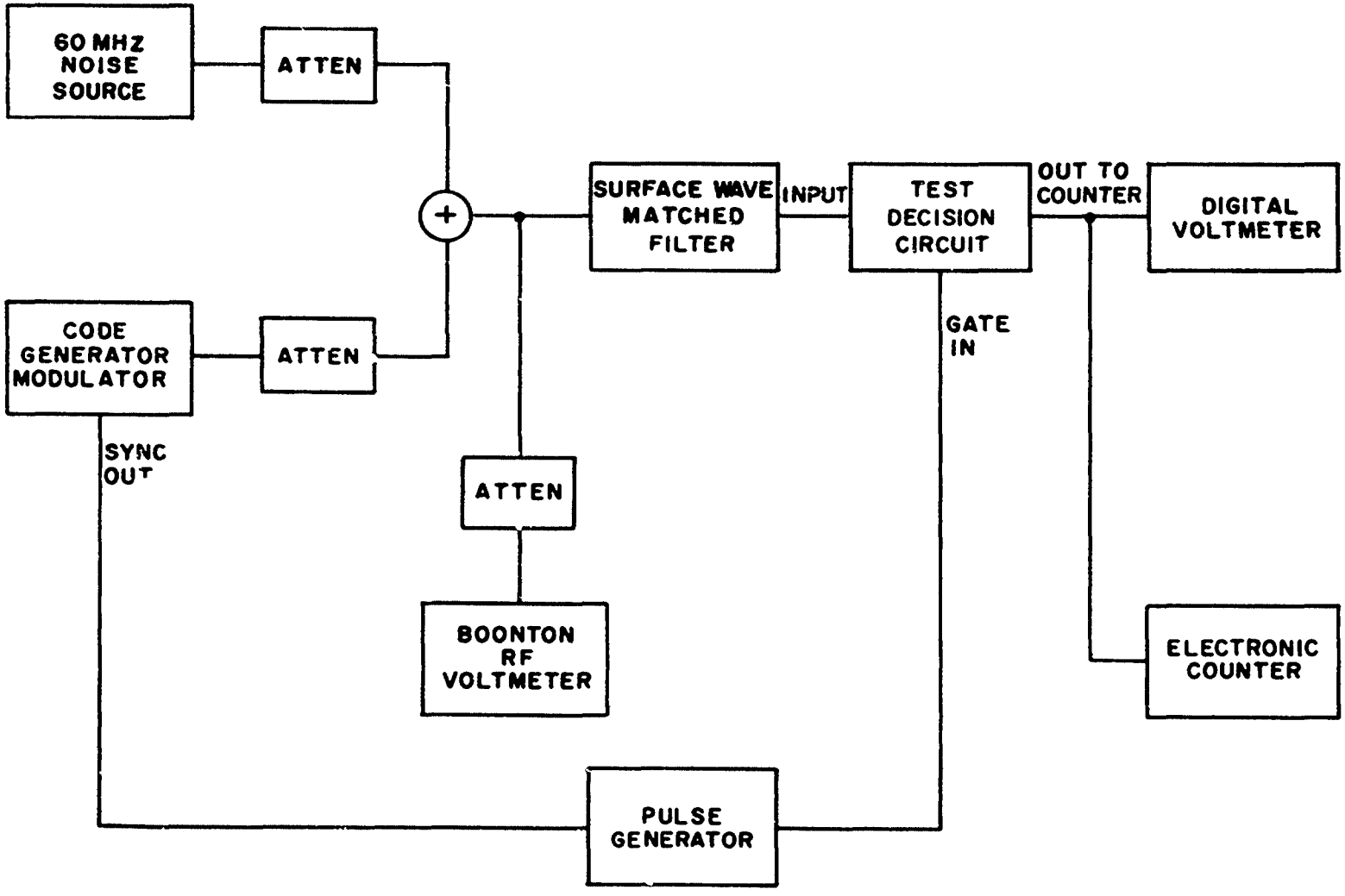


Figure 13. Test Setup for Measuring Processing Gain

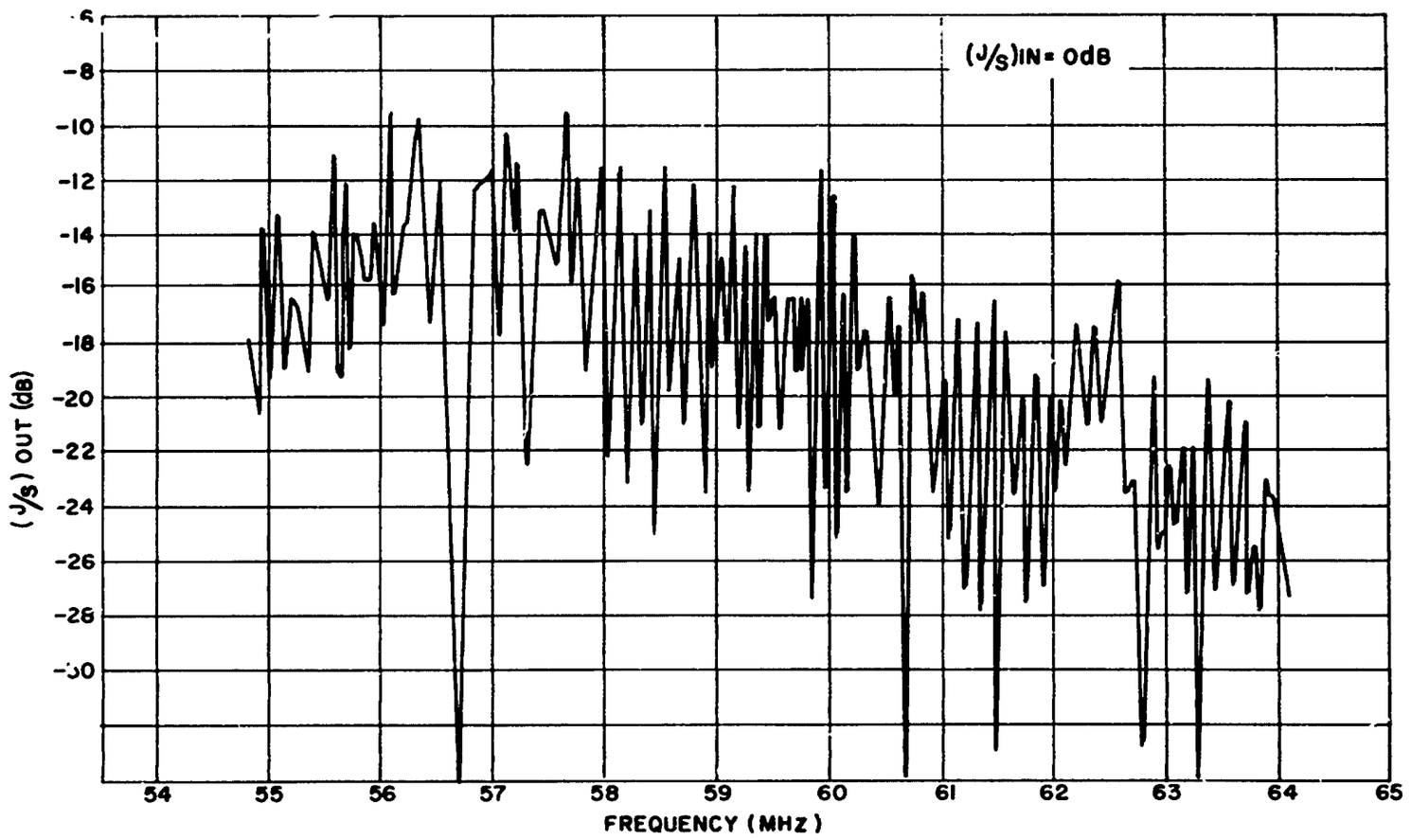


Figure 14. CW Interference Test Results

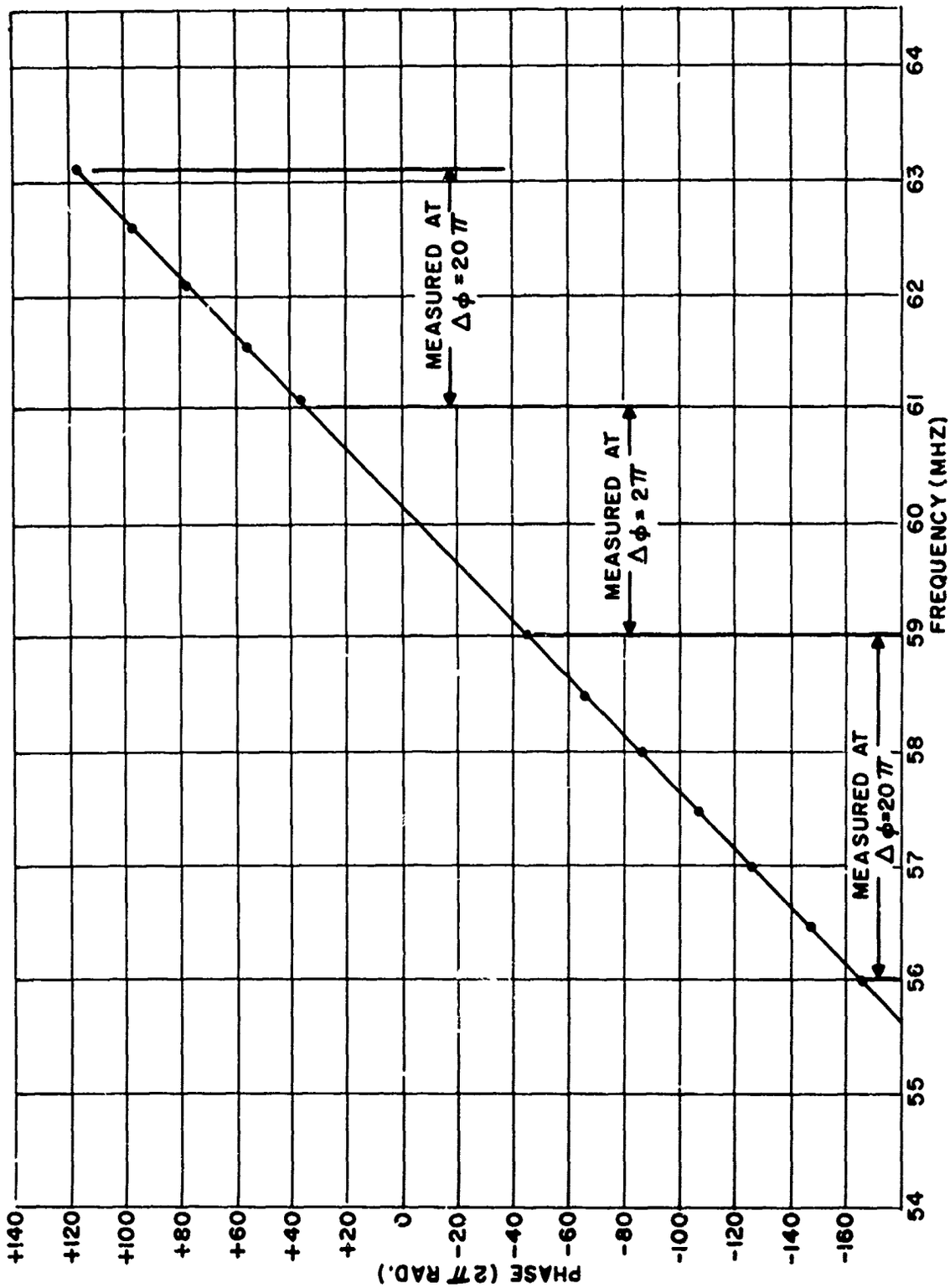


Figure 15. Phase Shift vs Frequency

SECTION V

CONCLUSIONS AND RECOMMENDATIONS

The main interest or technical problem that was solved on this program was the demonstration of an economically feasible technique, using existing state-of-the-art hybrid technology, of electronically programming, on a bit-by-bit basis, the code sequences for an acoustic surface wave sequence generator and an acoustic surface wave matched filter.

An experimental, 127-tap electronically programmable, sequence generator and reciprocal matched filter for PSK spread spectrum signals was designed, fabricated, and evaluated. The satisfactory test results for the composite experimental system provides the verification that the selected design approach was sound and the selected tap switching technique was feasible.

The program results have been sufficiently promising to merit recommendation for future development in this technological area. Therefore, an advanced development program for a switchable acoustic surface wave matched filter is recommended which includes the following:

- reduce the standby dc power dissipation of 35 milliwatts per bit by using high speed CMOS logic or other low power logic,
- modify the physical layout, compact and reduce the volume, and seal the hybrid thin film switching and memory circuits to form "building block" modules of either 32-taps or 16-taps,
- provide, as an alternative a low power parallel-in parallel-out CMOS or MOS logic memory to permit code change in less than one bit duration,
- replace the passive impedance matching of the input interdigital transducers with active (transistor) matching to reduce overall insertion loss of the quartz tapped delay line.
- Assemble "building block" modules to form a 512-bit (or 1024-bit) switchable matched filter with 27 dB (or 30 dB) processing gain.

APPENDIX I

REFERENCES

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(2) A.J. Slobodnik and E.D. Conway, Microwave Acoustics Handbook, AFCRL".

(3) Smith and Sorokin, "The Laser", McGraw-Hill, 1966, p. 37

(4) G.W. Farnell et.al., "Capacitance and Field Distributions for Interdigital Surface-Wave Transducers, IEEE Trans. SU-17 n3 p. 188; July 1970

(5) W.R. Smith et.al., "Analysis of Interdigital Surface Wave Transducers by Use of an Equivalent Circuit Model," IEEE Trans. MTT-17, n. 11, p. 856, Nov. 1969

APPENDIX II

ANCILLARY ELECTRONICS

1. SCOPE

This appendix provides a basic description of the code generator (CG) and the control unit used in the programming, control, test, and demonstration of the matched filter and sequence generator. The applicable logic and wiring diagrams are also included herein.

2. CODE GENERATOR

The code generator is a thirty-four stage m-sequence generator with the seventh, thirty-second, thirty-third, and thirty-fourth stages mod 2 added and fed to the first stage. A logic diagram is shown in figure 16. Briefly, the operation of the code generator is as follows: With the CG switch on, 5 Mb/s pulses from the control circuits are enabled in order to shift the code generator. The output of the thirty-fourth shift register is buffered and fed to both the switchable sequence generator and matched filter code inputs as the programmed code sequence. When the CG switch is on LOAD, shift pulses cause the contents of the thirty-four front panel initial state switches to be loaded into the code generator, which presets the code generator to the starting state anywhere within its $2^{34}-1$ bit duration.

3. TIMING CIRCUIT

The timing circuit, shown in figure 17, consists of a 10-MHz oscillator with TTL outputs, circuitry to provide two interleaved 5-MHz pulse streams (READ-WRITE and SHIFT) from the oscillator, a fifteen stage m-sequence generator (with the fourteenth and fifteenth stages fed back), and decode circuits to decode the desired states of the m-sequence generator. As the m-sequence generator shifts, one of two different 15-bit words are decoded at cycle times which are controlled by a front panel PRF switch. The SLOW time is 6 ms, the FAST time is 95.4 μs. For the SLOW timing, the state of the m-sequence generator is decoded 5.9998 ms after the all "ones" state. This state is ANDed with the READ-WRITE pulses. The resultant output resets a control flip-flop which, in turn sets the m-sequence generator; this control flip-flop is then reset by the next SHIFT pulse. Then a second SHIFT pulse starts shifting the m-sequence generator. The control flip-flop also sets the enable flip-flop which generates a gate that allows SHIFT and READ-WRITE pulses to shift the code generator and matched filter and sequence generator shift registers. A third decode on the timing generator resets the enable flip-flop after 127 pulses have been generated. The impulse generator trigger is generated from a fourth decode which is 2 ms after the all "ones"

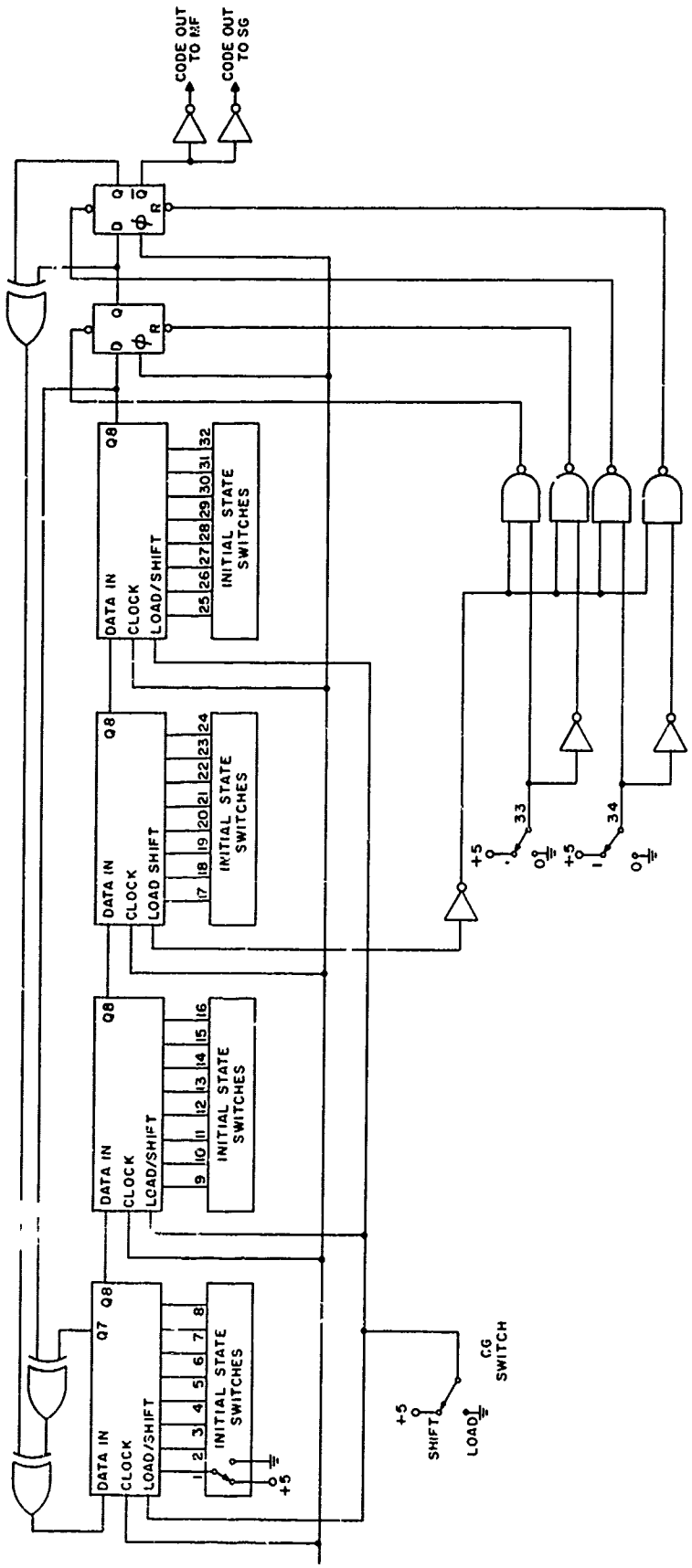

Figure 16. Code Generator Logic Diagram

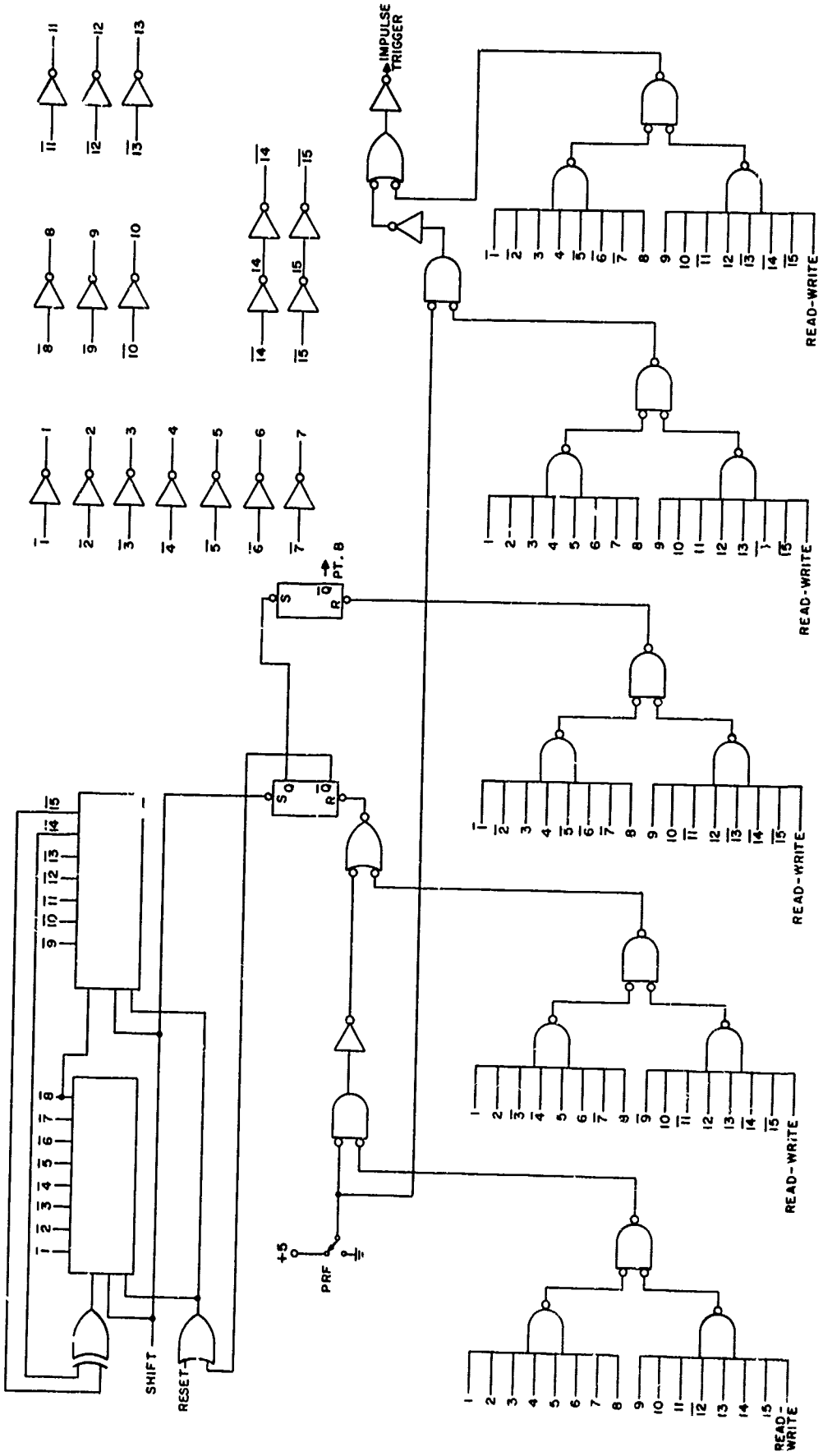

Figure 17. Timing Circuit Logic Diagram

state. The FAST cycle time operates the same way, except that the impulse generator trigger occurs 47.6 ms after the all "ones" state and the timing generator set decode occurs 95.2 ms after the all "ones" state. The FAST cycle time decodes are ANDed with the output of the PRF switch, and then ORed with the SLOW cycle time decodes. If the PRF siwtch is on SLOW the FAST decode is inhibited; if the PRF switch is on FAST the FAST decode resets the timing before the SLOW decode occurs.

4. CONTROL CIRCUITS

The control circuits, shown in logic diagram form in figure 18, control the routing of the SHIFT, CLEAR and READ-WRITE pulses to the code generator, matched filter, and sequence generator. With the code generator switch in the SHIFT position, SHIFT pulses shift the code in the code generator. When the code generator switch is in the LOAD position, SHIFT pulses load the 34 bits from the front panel initial state switches into the code generator, thus programming the initial state of the 34-stage register (for a "1" the switch is up, for a "0" down). The following procedure is used to load the code generator. With the shift switch in the ON position, turn the CG switch to LOAD; turn the shift switch to OFF , the CG switch to SHIFT and then turn the shift switch back to ON. The sequence generator and matched filter may be programmed for all "ones" by turning switch 34 to a "1" (up) and placing the CG switch to LOAD, with the shift switch in the ON position.

5. IMPULSE GENERATOR CIRCUIT

The impulse generator circuit consists of a pulse former and a pulse amplifier as shown in figure 19. The pulse former circuits consist of five ECL gates. The first gate connected as an inverter buffer. When the impulse trigger is applied to the inverter buffer, the output of the buffer goes down causing the output of the NOR gate to go up. The output of the inverter buffer is delayed by the delay time of the three inverters. The resultant positive output pulse is applied to the NOR gate causing it to go down. Since the delay time of each inverter is approximately 1.5 nanoseconds the pulse then generated will be narrow but of ECL levels. The pusle is then amplfied by three transistors which yield the desired 12-volt impulse with a half amplitude width of 5 nanoseconds.

6. AMPLIFIER CIRCUITS

The sequence generator amplifier circuit, shown in figure 20, consists of a low noise input stage (using a RCA 40235 transistor) followed by three stages using the Motorola MC1590 RF amplifiers and a transistor amplifier. The first MC1590 amplifier is gated during the expanded pulse duration by applying an ENABLE gate to the AGC input. The matched filter amplifier,

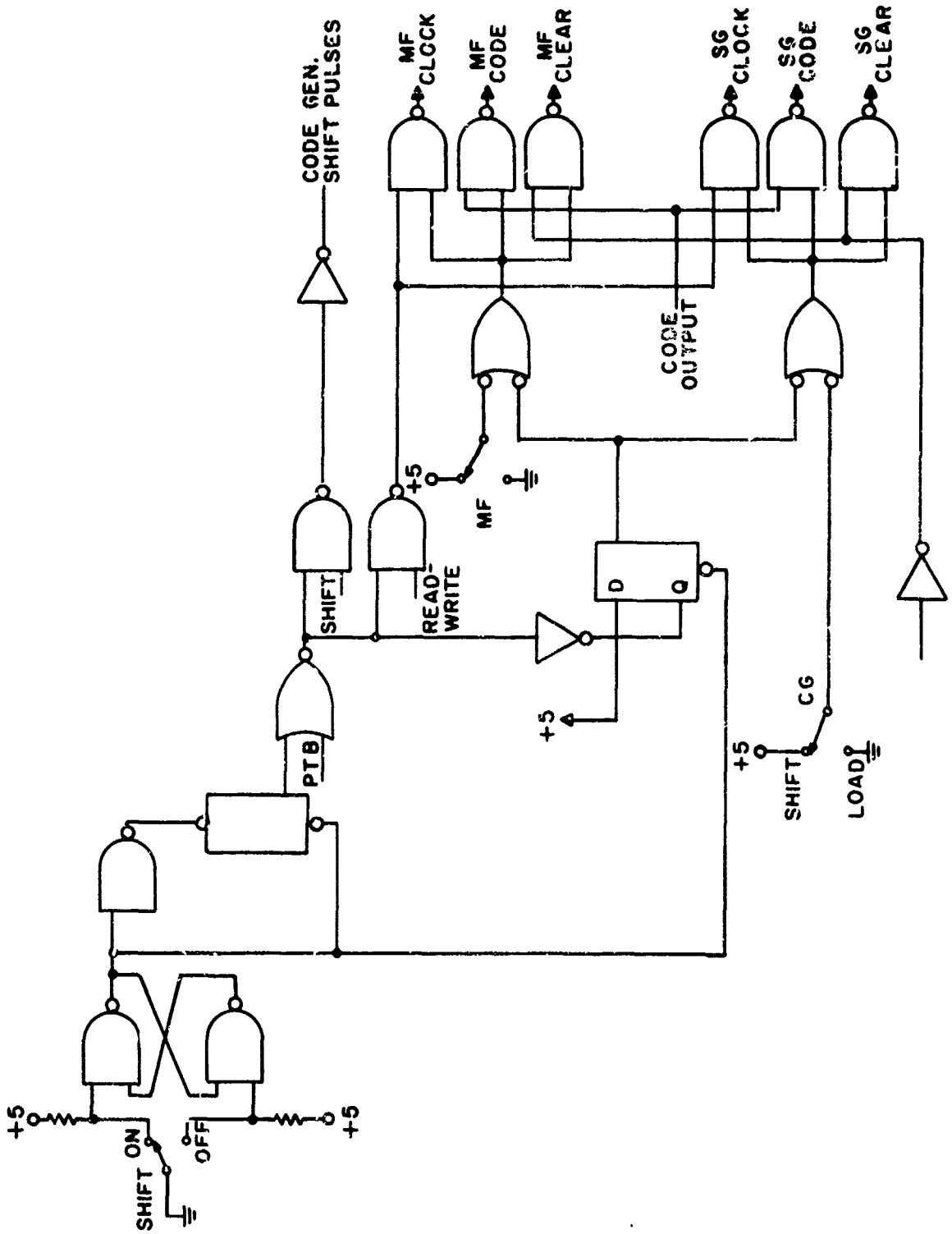

Figure 18. Control Circuit Logic Diagram

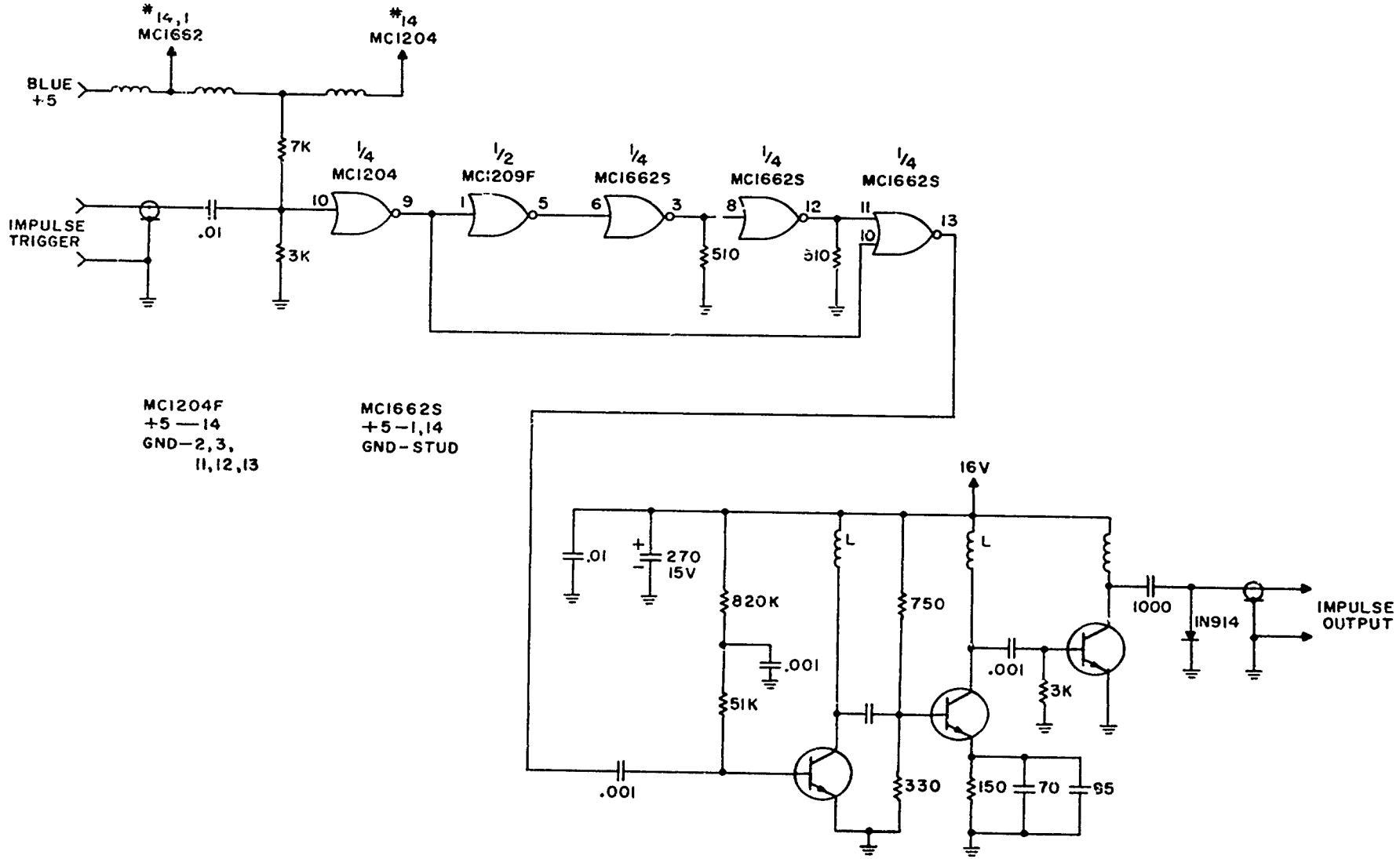

Figure 19. Impulse Generator Schematic Diagram

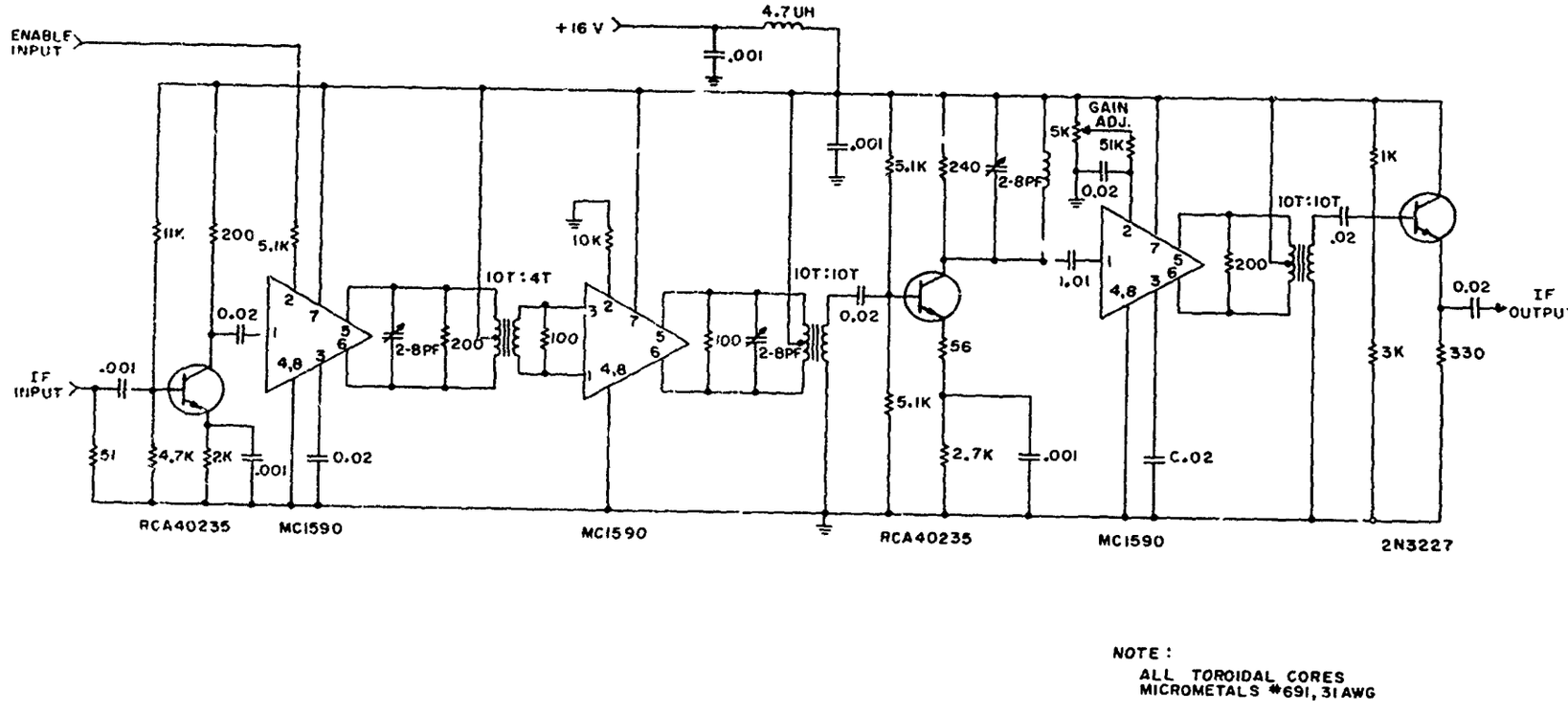

Figure 20. Sequence Generator Output Schematic Diagram

shown in figure 21, is similar to the sequence generator amplifier except that the low noise input stage is eliminated.

7. ENVELOP DETECTOR

The compress pulse envelop detector circuit, shown in figure 21 consists of two emitter coupled 2N3227 transistors operating as a full wave rectifier, followed by a 2nd order low pass filter to recover the envelop and an output video amplifier.

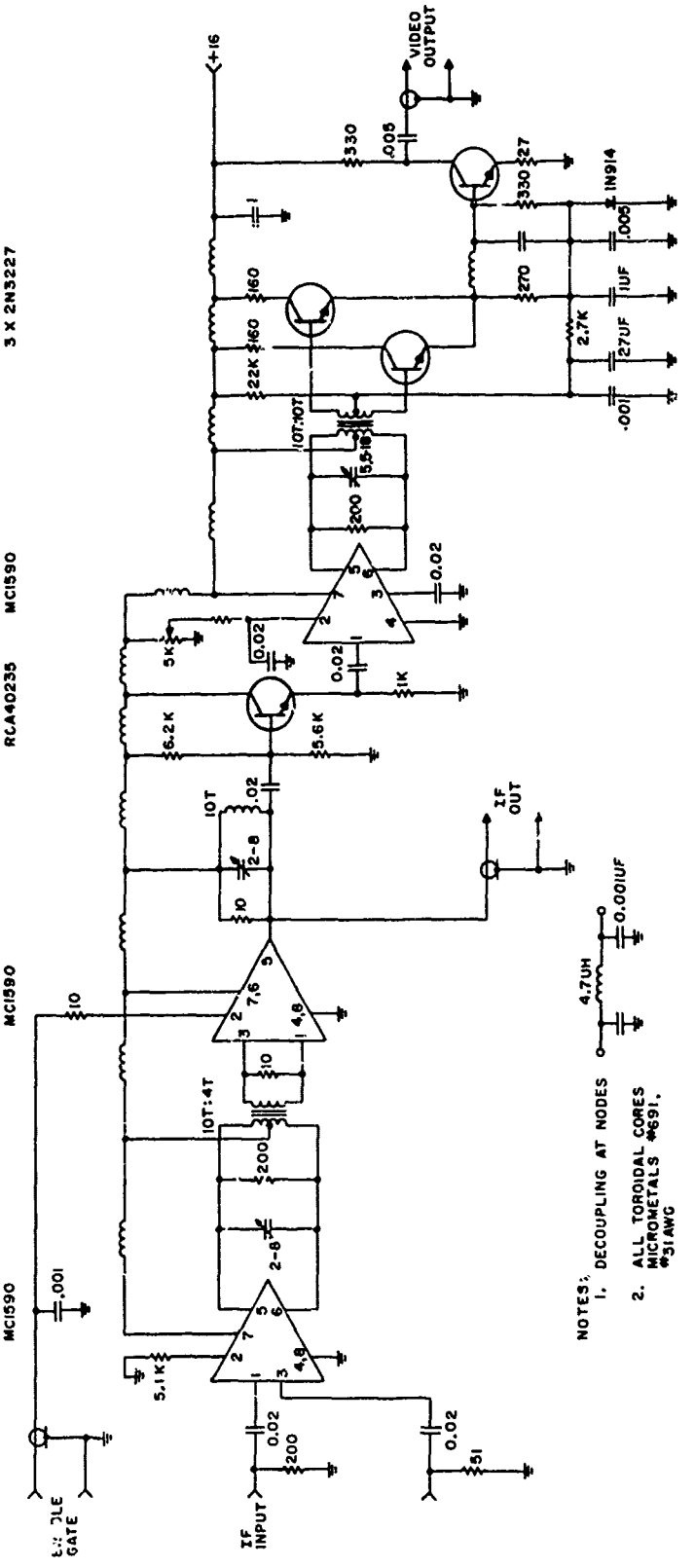

Figure 21. Matched Filter Amplifier and Detector Schematic Diagram