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RELIABILITY PROBLEMS WITH SiO_2 PASSIVATION AND GLASSIVATION

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The effect of differential expansion or contraction on the integrity of silicon integrated circuits is treated in part in this report. Specifically, relaxation of interface stress between Si and SiO_2, cracks in Si or SiO_2 due to upquenching, and problems with glassivation are addressed. The problems are shown to be real, and some suggestions for handling the difficulties are given.

Details of illustrations in this document may be better studied on microfiche

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RELIABILITY PROBLEMS WITH SiO_2 PASSIVATION AND GLASSIVATION

Clyde H. Lane

FOREWORD

This in-house report, prepared under Job Order No. 55190000, has been reviewed by the Office of Information (OI) and is releasable to the National Technical Information Service (NTIS).

Although General Electric Company did not fabricate the chips, they did kindly furnish them, as well as the SEM pictures, and information concerning temperature cycles when crazing occurred. Permission was granted to use this data in the report. Special thanks is given Bob Kelly, Lee Rogers, and Bill Leyshon of GE.

The author also acknowledges the contributions of Janson Engler and Tom Walsh of RADC (RCR).

This report has been reviewed and is approved. For further technical information on this project, contact Clyde H. Lane, RADC/RCRM, 330-4632.

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ABSTRACT

The effect of differential expansion or contraction on the integrity of silicon integrated circuits is treated in part in this report. Specifically, relaxation of interface stress between Si and SiO_2, cracks in Si or SiO_2 due to upquenching, and problems with glassivation are addressed. The problems are shown to be real, and some suggestions for handling the difficulties are given.

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RELIABILITY PROBLEMS WITH SiO_2 PASSIVATION AND GLASSIVATION

INTRODUCTION

As a result of the investigation of stress at the Si-SiO_2 interface[1] and aluminum penetration at the Si-SiO_2 interface[2], it was concluded that stress relaxation at the Si-SiO_2 interface, or in the silicon dioxide itself, may represent a fundamental degradation mechanism in planar silicon devices and circuits. Relaxation mechanisms will operate to relieve the high interface stress, which in turn gives rise to interface states, an increase in surface leakage and, hence, a reduction in transistor beta. Because of the large difference in expansion coefficients, it also seemed possible to generate cracks in thermal SiO_2 by upquenching, i.e., rapidly increasing the oxide temperature. This could happen in alloying or in rapid thermal cycling.

Finally, it has been noted that glassivation layers over silicon planar devices and circuits can craze under thermal cycling or from poor dice handling techniques. Passivation or glassivation layers have been observed to craze when resistors have been trimmed by current or laser pulse techniques. All these phenomena are related by the differential expansion and/or contraction due to large differences in the thermal expansion coefficients of materials in intimate contact.

In this effort, each of the areas was examined for possible impact on device or circuit reliability.

STRESS RELAXATION

The question, "Does the Si-SiO_2 interface stress relax at a significant rate?", has been relevant but unanswered. To examine the subject, we used the techniques described previously[1];

twenty-thousand angstroms of thermal SiO_2 were grown at 1200°C in steam onto a number of silicon (111 orientation) five ohm cm., n-type, chemically polished wafers. The wafers were subjected to various time-temperature conditions to permit various amounts of stress relaxation. Photolithography was used to define a pattern in the thermal oxide. Etching the silicon away through this oxide window allowed undercutting, leaving the overhanging oxide unconstrained by the silicon. The result was that the oxide took on a wave shape. The amplitude-to-wave length ratio is proportional to the stress in the oxide film under these conditions. Figures 1 and 2, coupled with the following equations, demonstrate the method of stress calculation. As one can see from Figure 1, the parameters which can be directly measured are L_{Si} and h. L_{Si}, the length of a segment of silicon at 25°C, is measured with a calibrated reticle; and h, the peak-to-valley separation, is measured by using a calibrated objective lens drive, focusing first at the top of the wave, then at the bottom, and reading the difference in objective lens travel. For the section of the wave shown in Figure 1, an arc and chord arrangement shown in Figure 2 is a good approximation, and it allows the application of Huygen's approximation for small arcs to calculate L_{SiO2}. The two equations are:

$$\text{Huygen's approximation} - L_{SiO_2} = \frac{8C - L_{Si}}{3} \qquad (1)$$

$$C = (h^2 + L_{Si}{}^2)\ 1/2 \qquad (2)$$

Thus, $L_{SiO_2} = 8/3\ \ (h^2 + L_{Si}{}^2)^{1/2} \frac{-L_{Si}}{3}$

The stress in the oxide film may now be calculated from the equation

$$S = E\ \frac{(L_{SiO_2} - LSi)}{LSi} \qquad \text{where E = Young's modulus.}$$

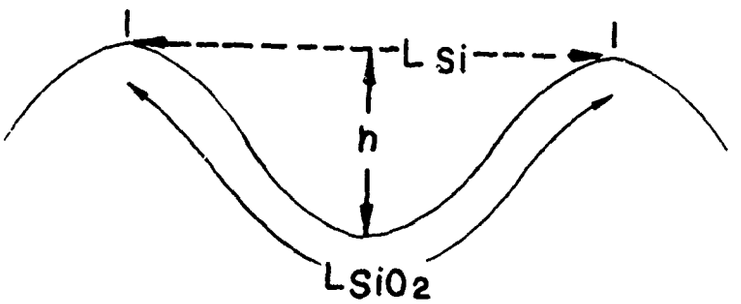

Figure 1. Oxide Wave With Pertinent Parameters

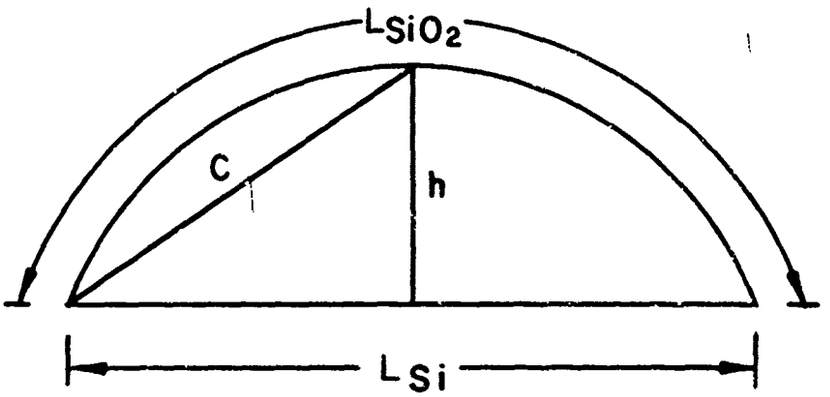

Figure 2. ARC Approximation of a Wave Segment

To calculate the stress in the oxide film, however, it is not necessary to know L_{SiO_2}. From the paper of reference (1), we have the following equation which is valid when h is less than 10 times L_{Si}: $(\alpha_2 - \alpha_1)(\Delta T) \cong \frac{h}{10\, L_{Si}}$, α_1 and α_2 are expansion coefficients and ΔT is the temperature difference in °C. We also know that the stress $S = E(\alpha_2 - \alpha_1)(\Delta T)$ where $E = 1.1 \times 10^7$; and estimated value for Young's modulus for thermally grown SiO_2. By substitution, then, we have $S = \frac{Eh}{10\, L_{Si}} = \frac{1.1 \times 10^6 (h)}{L_{Si}}$

Using this equation, stresses have been calculated for several oxides as noted in Table 1.

The values of L_{Si} and h were averages of about 10 experimentally measured values. To visualize the situation more clearly, a graph, Figure 3, was plotted using Table 1 data. The solid line is the theoretical stress for SiO_2, assuming all the stress is in the oxide and entirely due to the thermal differential contraction between silicon and its oxide. The experimental data points for 25°C essentially verify the correctness of the assumptions used to obtain the above equation. The other points indicate that first, when raised to a higher temperature, the interface immediately assumes the stress it would have had if it had been quenched from the oxide growth temperature to the temperature to which it has been raised. This is due to the purely elastic nature of the interface stress. Second, upon attaining the new state of elastic stress, relaxation of that stress occurs as a function of time at the given temperature. Thus, a point on the solid line in Figure 3 will move up along the line to the higher temperature, say 500°C; it then moves laterally to the left on the 500°C isotherm as a function of time. When the designated time at temperature has elapsed and the wafer is pulled from the oven, the point will fall along a line parallel to the original

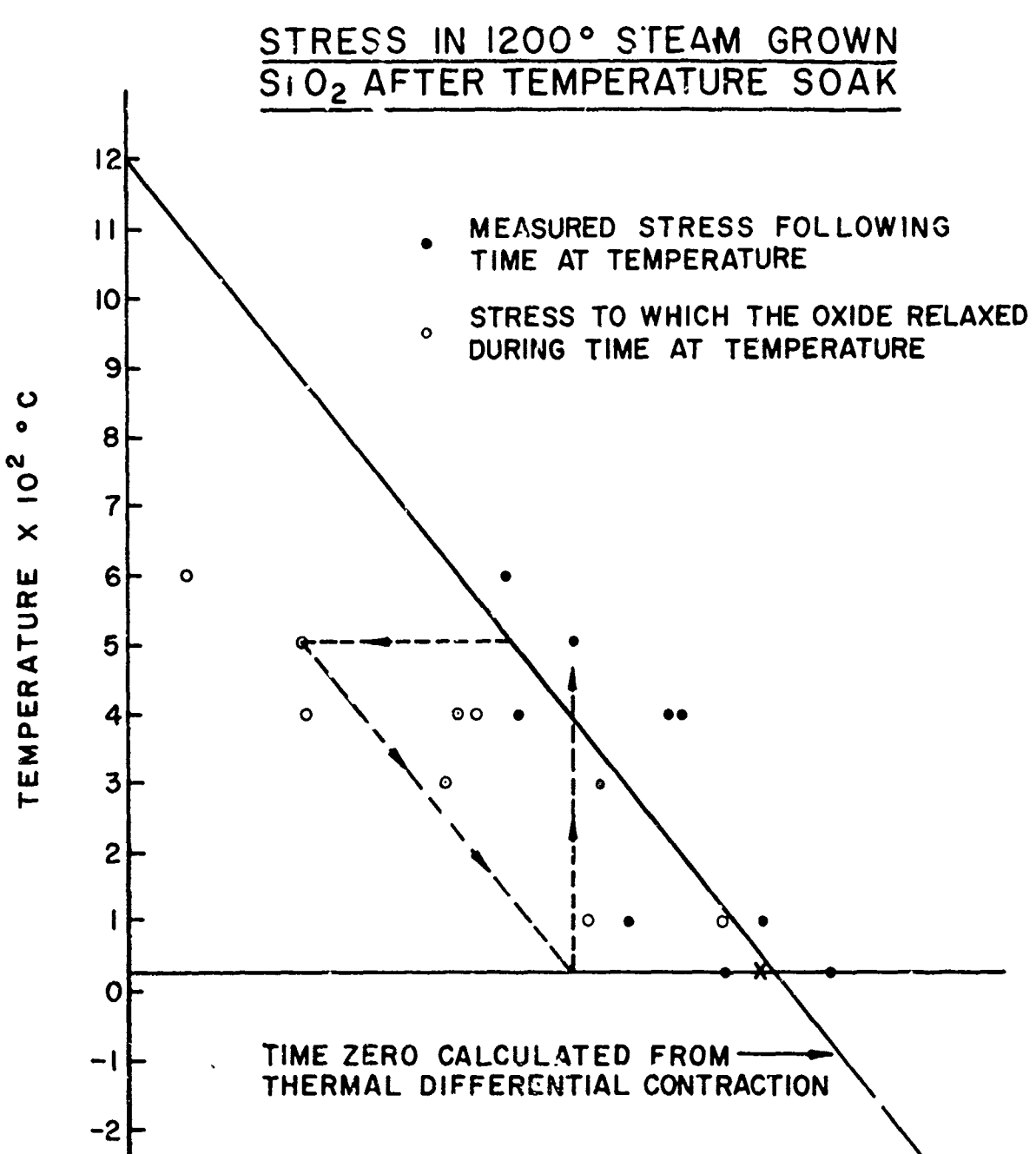

Figure 3. Stress in 1200° Steam Grown SiO_2 After Temperature Soak

TABLE 1

WAFER #	TIME HRS.	TEMP. °C	L MICRONS	h MICRONS	STRESS psi X 10^3
556	1	25	100	4.2	46
557	4	25	58	2.5	47
558	4	100	70	3.0	47
559	16	25	51	2.4	52
560	16	100	88	3.8	47
561	64	25	81	3.2	44
562	64	100	87	3.0	37
563	7	300	88	2.8	35
564	650	30	74	3.2	47
565	5	400	50	1.3	29
566	1.1	400	80	3.0	41
568	2.7	400	80	2.9	40
569	1	500	74	2.2	33
570	1	600	83	2.1	28

EXPERIMENTAL DATA FOR SiO_2 STRESS CALCULATIONS

stress-temperature line until room temperature is reached. That point translated vertically to the furnace temperature line is the solid point which is shown on the graph and was the point measured experimentally. To find how much the oxide stress has relaxed for a given time at a given temperature, simply drop the appropriate point on the graph vertically to the 25°C isotherm, then follow a path parallel to the solid line on the graph until the given temperature is again reached, designated by the open point. The difference between this stress and that given by the intersection of the desired isotherm with the solid line is the amount of relaxation attained.

Table 2 gives a compilation of the oxide stress after various times at several temperatures. The data are plotted in Figure 4. This graph clearly shows stress relaxation occurring, although the exact curves are in doubt, since only a few points were available. Nevertheless, enough points are there to establish approximate curves from which calculations of stress rates at various times and temperatures can be made. When these rates are plotted against the absolute reciprocal temperature, we obtain Figure 5. This graph shows how the stress rate rises as a function of temperature. The slope of the line gives the activation energy for the process which is about 0.28 ev. Stress relaxation occurs then readily at alloying and packaging temperatures.

In MOS devices it will relax during high temperature, reverse bias tests, unless previously annealed. The annealing procedure for interface state reduction and stabilization may well be a stress relaxation and interface state compensation or annealing step. Uncontrolled relaxation can cause an unknown interface state increase, as well as an increase in surface leakage, and an attendant uncontrolled reduction in transistor gain. Relaxation

TABLE 2

TEMP. °C	TIME HRS.	STRESS psi X 10^4
100	0	4.5
100	4	4.4
100	6.4	3.4
300	0	3.7
300	7	2.4
400	0	3.2
400	1.1	2.6
400	2.7	2.4
400	5	1.4
506	0	2.8
506	1	1.3
600	0	2.4
600	1	0.2
700	0	2.0

STRESS IN SiO_2 FOLLOWING TIME-TEMPERATURE TREATMENTS

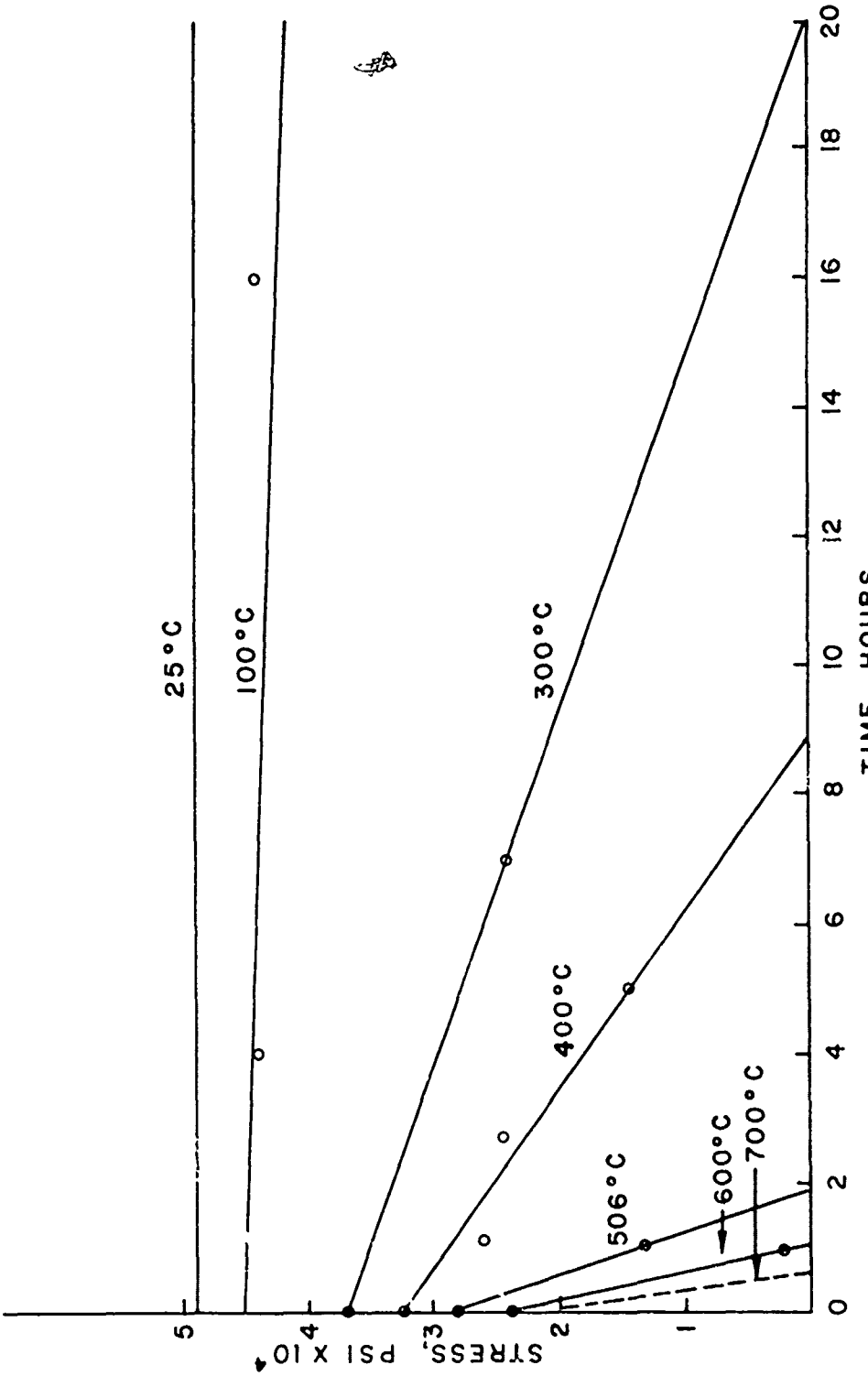

Figure 4. Thermal Oxide Relaxation With Time At Various Temperatures

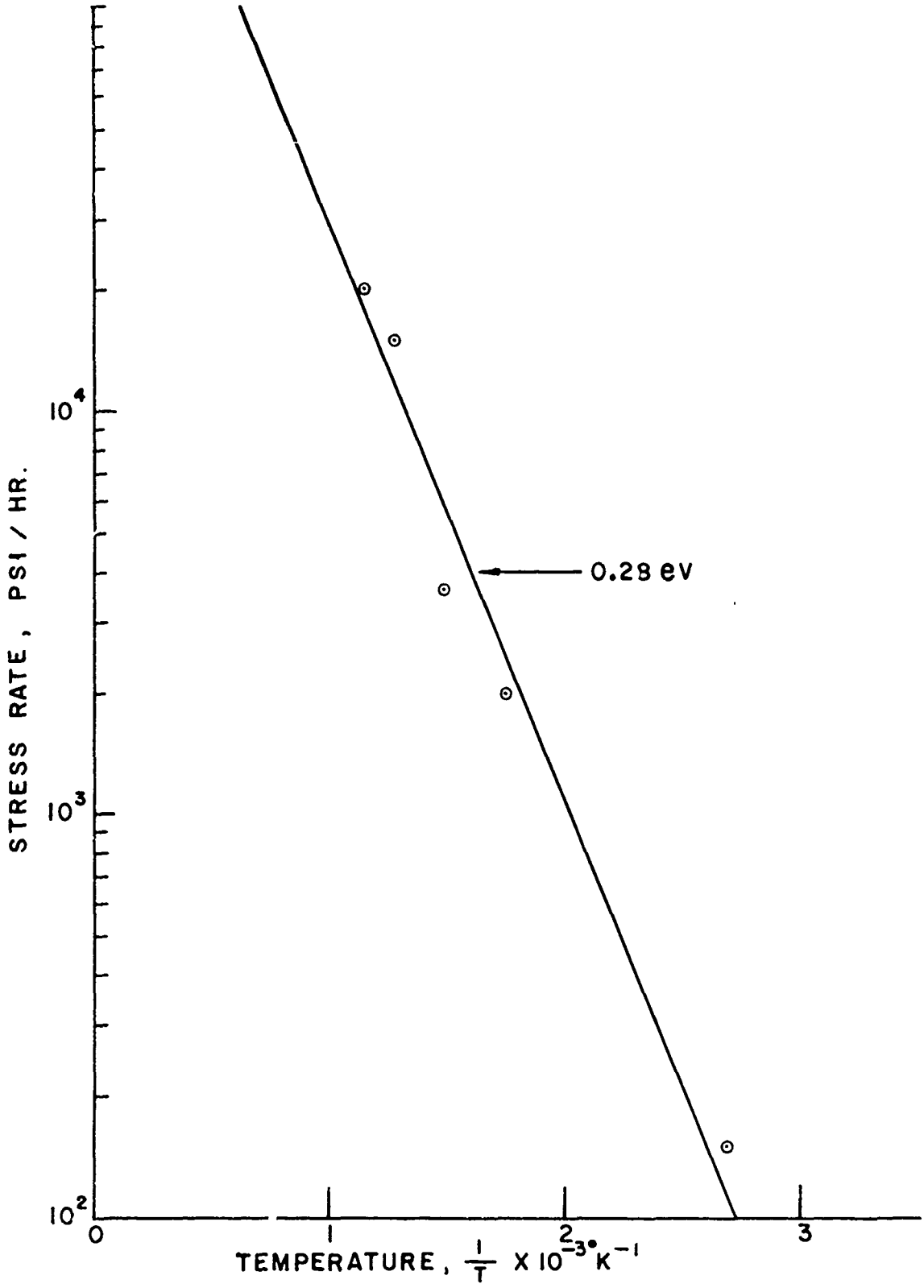

Figure 5. Stress Rate vs Temperature

would seem to occur readily at room temperature from the data we have gathered unless there is a change in mechanism around 100°C. Actually, we have some evidence to suggest that this is, in fact, the case. A silicon wafer oxidized at 1200°C and allowed to remain at room temperature for six months should exhibit little or no interface stress. Such a sample showed considerable (40,000 - 46,000 psi) compressive oxide stress, however. Silica based glasses normally demonstrate a transition in their mechanical properties around 80°C. Silica glass (fused silica) shows a marked change in the slope of its linear thermal expansion as a function of temperature at about zero degrees centigrade [3]. The low quartz to high quartz transition may have pronounced effects despite the fact that we are supposedly dealing with an amorphous material. In this regard, it is interesting that the activation energy for transition from the lower thermal expansion coefficient to the higher expansion coefficient in the region of the low to high quartz transition is 1.1 ev [4], and the activation energy for an electrical stress induced surface state in SiO_2 is also 1.1 ev [5]. This effect may be the explanation for the 1.1 ev activation energy for aluminum migration at the $Si-SiO_2$ interface [2], i.e., the migration process is limited by the availability of point defects (vacancies) supplied by the transition process. One could also point out that many silicon devices and circuits exhibit a degradation expressed as a rate equation having a 1.1 ev activation energy [6]. Of course, this may be entirely coincidental, since most solid state processes of concern in the -55°C to 250°C temperature range proceed by vacancy mechanisms which have activation energies of about 1.0 ev. Our low activation energy (0.28 ev) suggests relaxation by viscous flow rather than any bonding rearrangement. If the simple equation for viscous

relaxation [7] is used, $T = \frac{n}{E}$, where T is the time to reach 33 percent of the initial stress, n is the viscosity in poise, and E is Young's modulus, 1.1×10^7 psi or 7.7×10^{11} dynes/cm^2, then we can calculate the viscosity of thermally grown steam oxide. At 506°C, T is approximately 1.25 hours or 4.5×10^3 seconds; therefore, $n = 7.7 \times 10^{11} \times 4.5 \times 10^3 \frac{\text{dyne}}{\text{cm}^2}$ sec, $n = 3.5 \times 10^{15}$ poise. From a plot of viscosities at various temperatures for pyrex, in Figure 6 [8] one can readily see that our calculated value is quite believable. The viscosity versus temperature for a high alumina glass has been plotted on this graph also, since it may well be of practical interest if Al_2O_3 is used as the gate insulator for radiation hardened metal-insulator-field effect trarsistors. We already know that Al_2O_3 deposited at high temperature, 1000°C, onto silicon will be in a high state of tensile stress when quenched to room temperature. A quick calculation shows that the differential contraction coefficient between silicon and alumina at 1000°C is about 8.5×10^{-6} [9] - 3.5×10^{-6} [10] $= 5 \times 10^{-6}$. Young's modulus for Al_2O_3 is 5.0×10^7 psi [11] or 3.5×10^{12} dynes/cm^2. The stress, S, then is $S = 3.5 \times 10^{12} \times 10^{-6} \times 10^3 = 1.7 \times 10^{10}$ dynes/cm^2 or 240,000 psi. It should be noted that this is already higher than the fracture strength of bulk Al_2O_3 in tension, although bulk Al_2O_3 will take about 410,000 psi in compression before fracture.

Since our technique of stress measurement is difficult and subject to fairly large errors, more samples and preferably another technique are required for verification of these results.

DISCUSSION AND RECOMMENDATIONS

Our results demonstrate that the theoretical amount of stress due to differential thermal contraction of the perfectly elastic interface at the

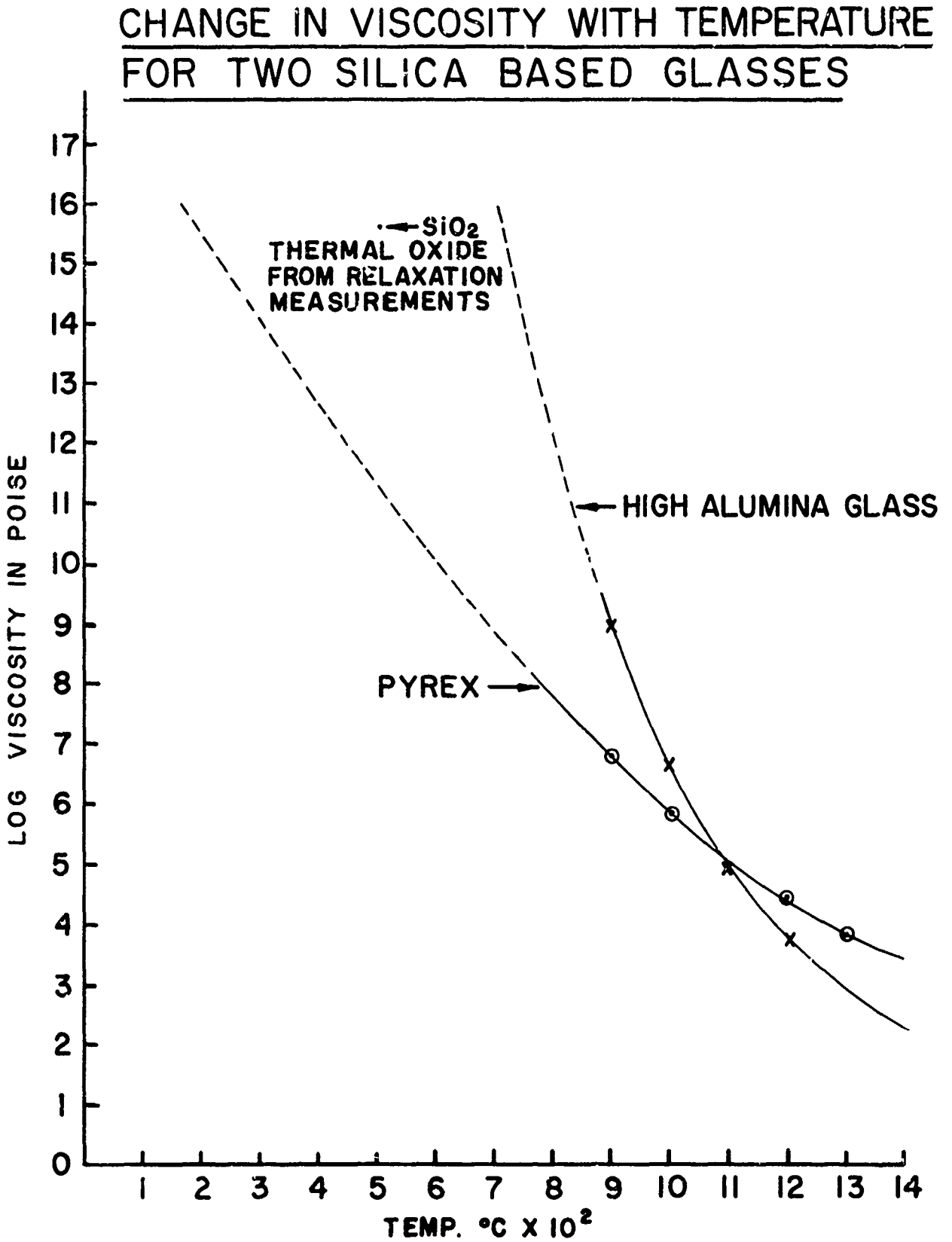

Figure 6. Change in Viscosity with Temperature for Two Silica Based Glasses

junction of single crystal silicon and steam grown silicon dioxide is indeed present. This is verified for dry oxygen grown silica films on silicon[12], but other techniques indicate steam grown oxides have a lower stress for the same growth temperature. The results also show the expected relaxation effect. Now, it is desirable to find out whether it is better to relax the oxide almost completely prior to testing and shipping circuits or devices to prevent any uncontrolled change or if it is better to attempt to maintain as much compression in the oxide as possible, since an oxide in compression offers a more stable film in many ways. In the case of alumina on silicon, the high tensile stress is of concern, and more information should be uncovered to allow a better evaluation of such a condition. It has been suggested by the author for some time[13] that the stress condition of anodized films for capacitors is a potential source of reliability problems. Recently, it was noted that plasma anodized aluminum films on silicon are in a highly stressed condition[14]. This whole problem of the effect of stressed films on the reliability of device and circuits which contain them should be studied, since to assure reliability in today's solid state devices means one must have detailed knowledge of molecular processes involved in any degradation process.

Si-SiO_2 IN THERMAL SHOCK

During studies of reliability problems associated with the interface stress, it was suggested that upquenching the oxide may cause it to crack. To test this idea, 5 cm. n-type wafers oxidized in steam at 1000°C were subjected to thermal cycling. The first wafer was subjected to 10 cycles from room temperature to 650°C and back, allowing 15 minutes in the furnace and 15 minutes out. A control wafer was oxidized at the same time but not

thermally cycled. Both wafers were coated with KMER, and a contact pattern was etched in the oxide. Nothing unusual was seen on the control wafer, but on the thermally cycled unit, numerous lines could be seen emanating from the contact cuts as seen in Figures 7 and 8. These lines are believed to have been cracks in the oxide which were enlarged by the etchant which penetrated along the crack under the photoresist by capillary action. The next wafer was cycled to 520°C by the same procedure. Cracks were again visible, but they were shorter. Another wafer was cycled to 510°C, 20 times. Cracks appeared in the oxide on the second and third cycle prior to etching. The average length of the etched lines was then plotted as a function of oven temperature. Figure 9 shows the graph, a straight line intersecting the ordinate at 485°C. This is interpreted to mean that upquenching with our procedure to less than 485°C will not cause cracks. Normally, alloying is carried out from 520-560°C. If, then, the wafers are quickly placed on a hot quartz carrier just drawn from the oven and immediately returned, as in our experiment, microcracks could be expected.

In one of the wafers, one of the larger cracks seen at the second thermal cycle, prior to etching, was in the silicon as well. Figures 10-12 show the crack as the silicon dioxide is removed. Note that the length of the crack appears to increase as the oxide is removed.

DISCUSSION AND RECOMMENDATIONS

Obviously, thermal shock will introduce microcracks. Therefore, one should make sure that a thermal shock is not actually part of the alloying cycle, either purposely or inadvertently. There is some information from the days of alloy transistors which suggests that thermal shock is beneficial for good alloying. While this may have been true for alloy devices, it is not valid for, and should not be used in, planar processing. Thermal

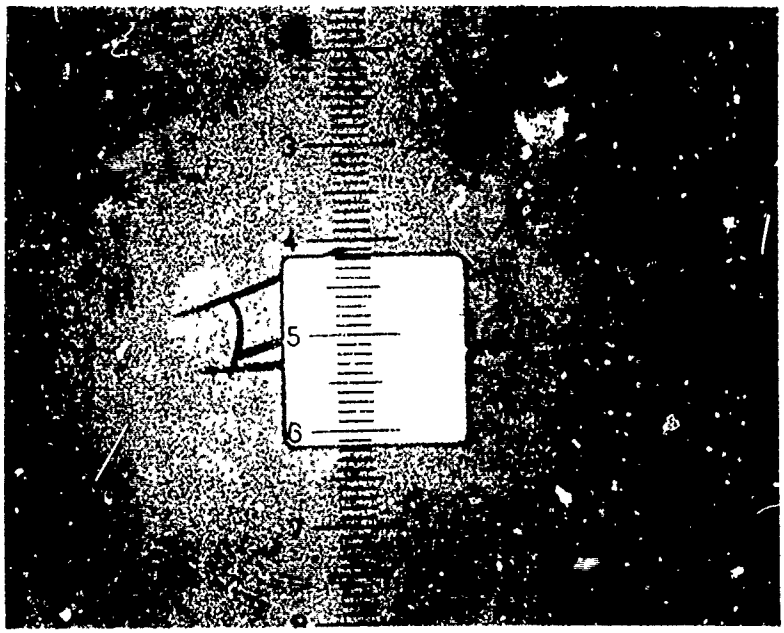

Figure 7 - Microcracks at oxide windows after 10 cycles, 30°-650°C, 2.5 microns/div.

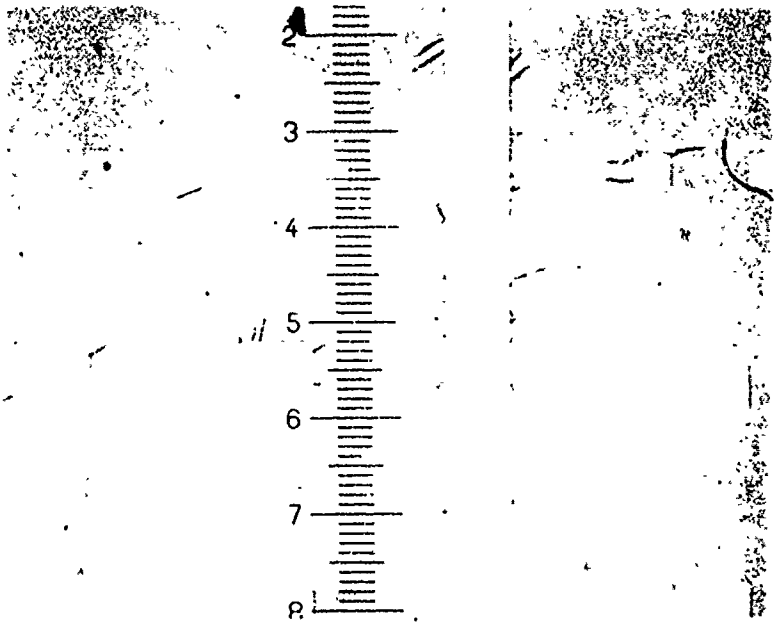

Figure 8 - Microcracks at oxide windows after 10 cycles, 30°-650°C, 2.5 microns/div., 200X mag.

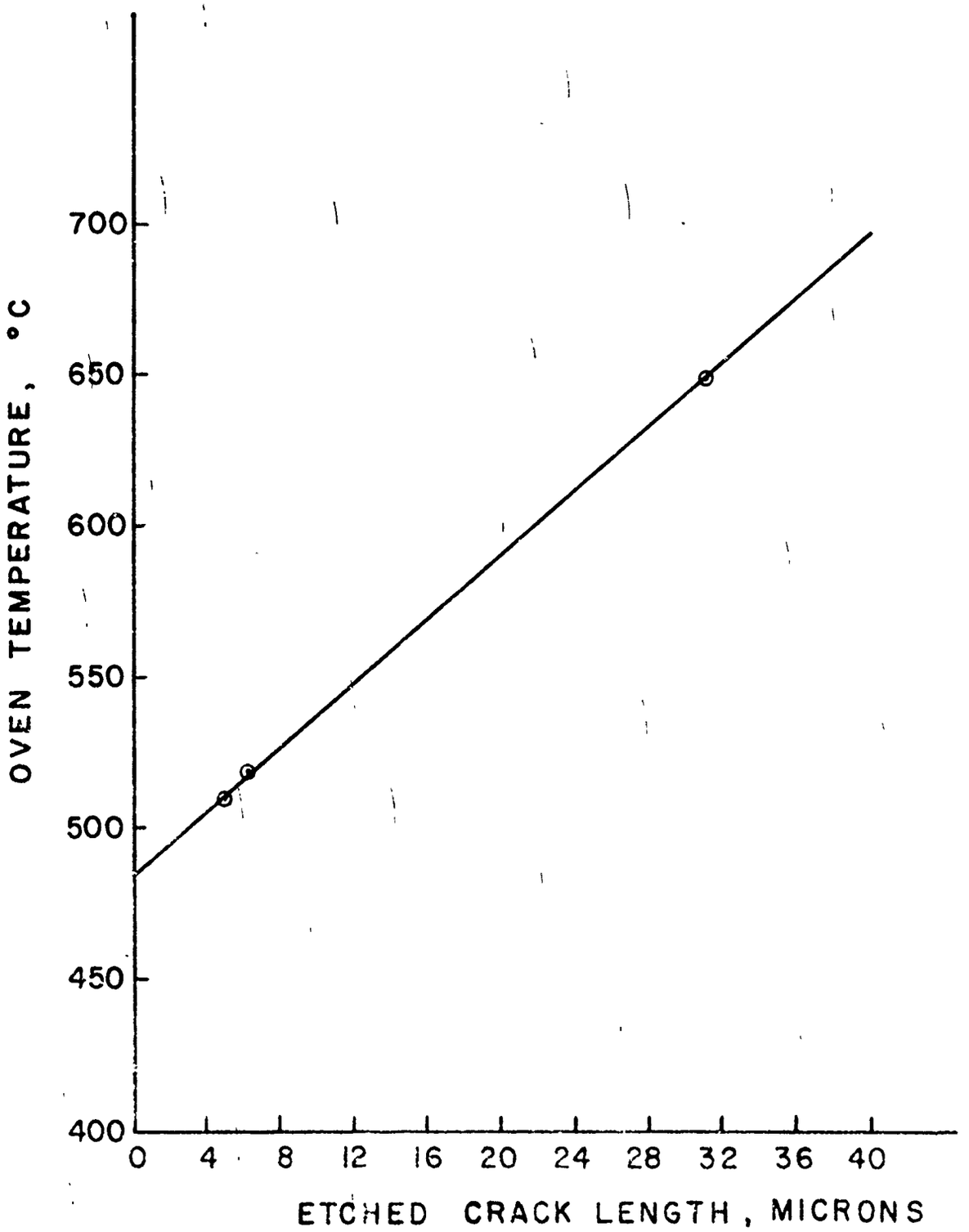

Figure 9. Lengths of Etched Microcracks Following Unquenching

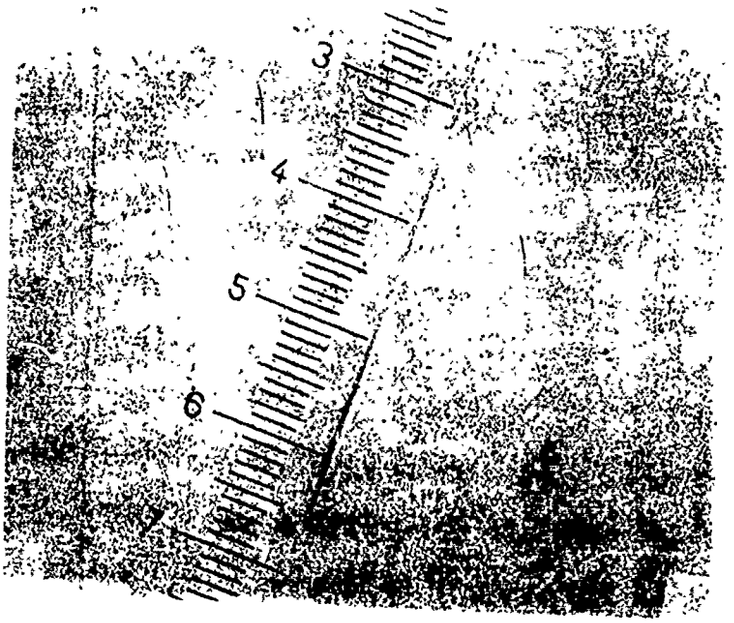

Figure 10

Crack in SiO_2 and silicon substrate after 2 cycles from 30° to 510°C, 26 microns long, 3300 angstroms SiO_2.

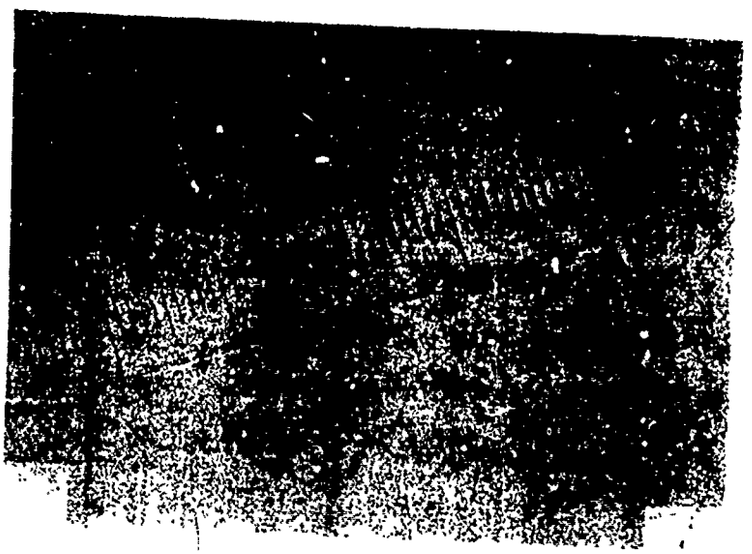

Figure 11

Crack in SiO_2 and silicon substrate after 2 cycles from 30° to 510°C, 31 microns long, 1500 angstroms SiO_2.

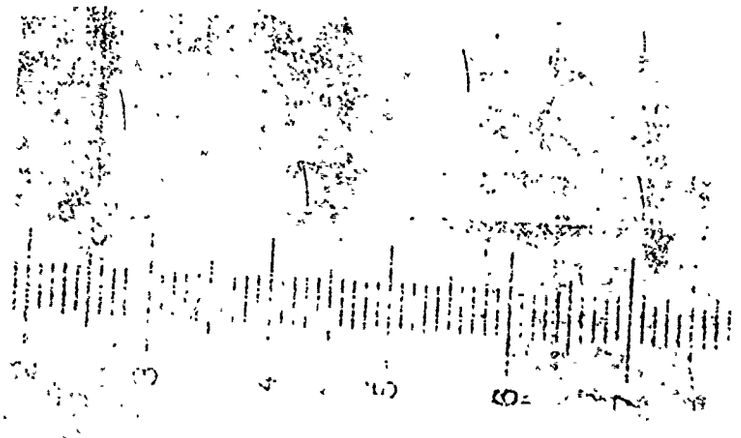

Figure 12

Crack in SiO_2 and silicon substrate after 2 cycles from 30° to 510°C, 34 microns long, oxide removed.

cycling may be performed at lower temperatures or conducted in such a way as to avoid shock without fear of introducing oxide cracks. Shock treatments, such as current pulse trimming of resistors which have been overcoated with SiO or SiO_2 will cause fracture. Laser pulse trimming can also introduce microcracks. Since the cracks are liable to cause the resistor film to crack, their presence should always be considered detrimental even if the unit is placed in a hermetic package. This is again a differential expansion or contraction problem. Material combinations or interfaces having a large difference in expansion coefficients are particularly susceptible to this type of problem. Such a system is glass-aluminum which will be discussed next.

CRAZED GLASSIVATION ON INTEGRATED CIRCUITS

From time to time we have seen evidence of crazing in the protective glass some manufacturers put over their integrated circuit chips. This is not a passivation layer but primarily a mechanical protection layer to prevent scratches and other handling induced defects. Cracks in this layer are, however, grounds for rejection under MIL-STD-883 visual criteria. There is presently no nondestructive way to tell whether or not the cracks go on through the metallization or thermal oxide beneath the glass layer. There is evidence that on occasion the cracks may proceed through the metallization. A Talysurf study of crazed glassivation before and after the glass was removed showed a separation or deep crevice in an aluminum conductor. This was not a definitive study, however, and the crevice may have been a scratch in the aluminum prior to glassivation.

Recently, when this problem was drawn to our attention again, it was

noted by the customer* that virtually all the chips were free of cracks when received, but crazed during die attach in which a thermal cycle from room temperature to 400°C was seen. Some cracks also occurred during the wire bond process. About 80 percent of the chips in the finished hybrid circuits were crazed, but all performed within electrical specifications. The customer noted that the cracks seemed to initiate in the glass layer over the aluminum, particularly over capacitor top plate and large area metallization. Thermal differential contraction, of course, is the culprit in most of the cases, coupled with the aluminum grain growth, while mechanical damage caused by exceeding the yield strength during wire bonding or hitting the glass with a hard object, such as tweezers, accounts for a small portion of the cracks. In our laboratory, several dice were examined both as received chips and chips which had been through the hybrid circuit assembly process.

None of the six as-received chips showed any sign of microcracks under normal vertical illumination up to 1000X in the Leitz Metallograph. They did show several undesirable effects, however. In Figure 13, problems were noted with the photolithography work. Just above that area is an aluminum fiber which is apparently under the glassivation. It extends almost completely across the separation between the two metallization lines. One also notes the extensive aluminum grain growth in this photograph. In Figure 14, aluminum migration at the interface between the thermal SiO_2 and the glass layer is seen. This is quite common on the chips, and fingers of aluminum extending halfway across a 0.5 mil metallization separation have been noted. Figure 15 shows a rather severe crack in the aluminum metallization due to grain growth in aluminum over an oxide step. Although all circuits were satisfactory from an electrical performance point of view, it is only a

*See acknowledgment in the Foreword (page ii).

Figure 13 - Photolithography error and metal fibre protruding from aluminum conductor.

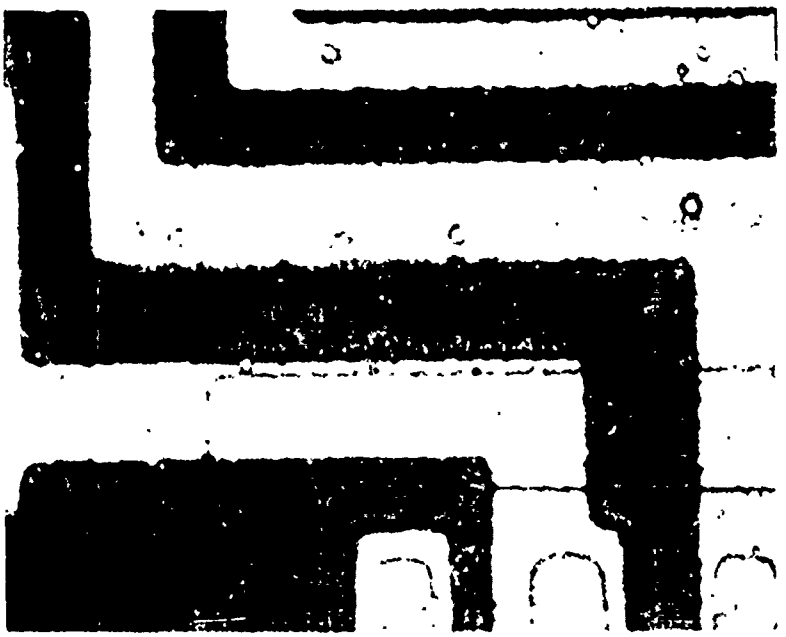

Figure 14 - Aluminum migration at the thermal oxide - deposited oxide interface.

Figure 15 - Crack in metallization due to disruptive grain growth.

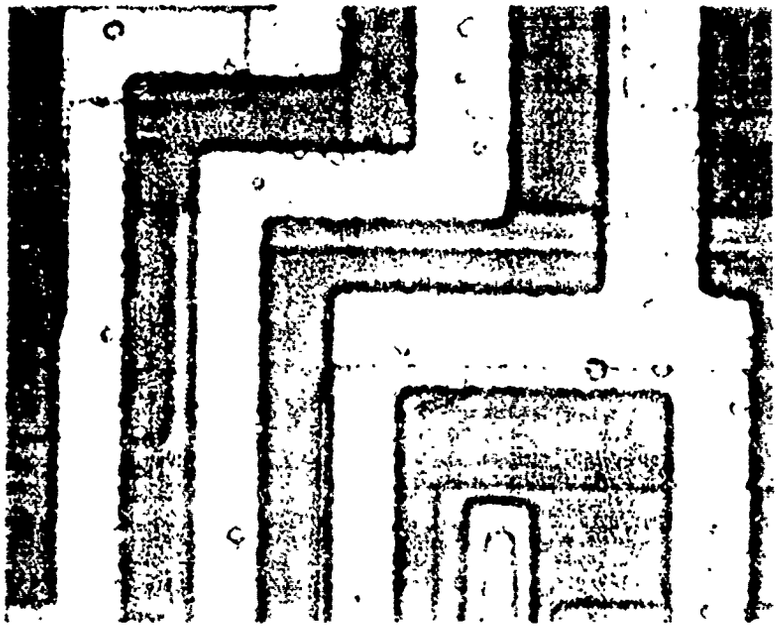

Figure 16 - Whisker protruding from aluminum metallization thru a hole in the glassivation.

question of time before the metallization stripe would increase its resistance significantly. And finally, Figure 16 shows a whisker growing out and up from the edge of an aluminum conductor, through a hole in the glassivation. The whisker was three to four microns high. All these effects, grain growth and cracking, aluminum migration, and whisker growth, were seen on every chip. Migration and grain growth occur during the glassivation, but whisker growth occurs later from exposure to uncontrolled environments. Nevertheless, holes present in the glass layer, which allow whisker growth, result from the glassivation process. This is more evident in photographs of a chip which had been through the hybrid circuit assembly process. Figure 17 is taken from that chip. It shows the holes, cracks in the glass, and separation between glass and SiO_2 as revealed by color variations and seen here as optical density variations. Another photograph from an assembled chip, Figure 18, shows extensive aluminum migration as well as cracks in the glass. This brings up the questions, "Does the aluminum migrate further during die attach or has this all taken place during glassing?" and "Does the aluminum continue to migrate at, say, normal burn-in temperature, 125°C?" A second chip which had been through assembly showed all these problems but displayed extensive whisker growth as well.

Scanning electron microscope (SEM) photographs of an assembled chip, taken by the customer, are instructive but can be misleading. Figure 19 is an SEM picture of a crack in the glass. You will note that over the metallization the glass has a pebbled look and the crack can be readily seen, while glass on SiO_2 has no structure and the crack cannot be seen. The effect is due to the fact that impinging electrons have a discharge path in the glass over the metal but not over the SiO_2. Therefore, a space charge accumulates on the glass over SiO_2, which repels electrons, resulting

Figure 17 - Separation between thermal and deposited oxides and holes in the deposited oxide.

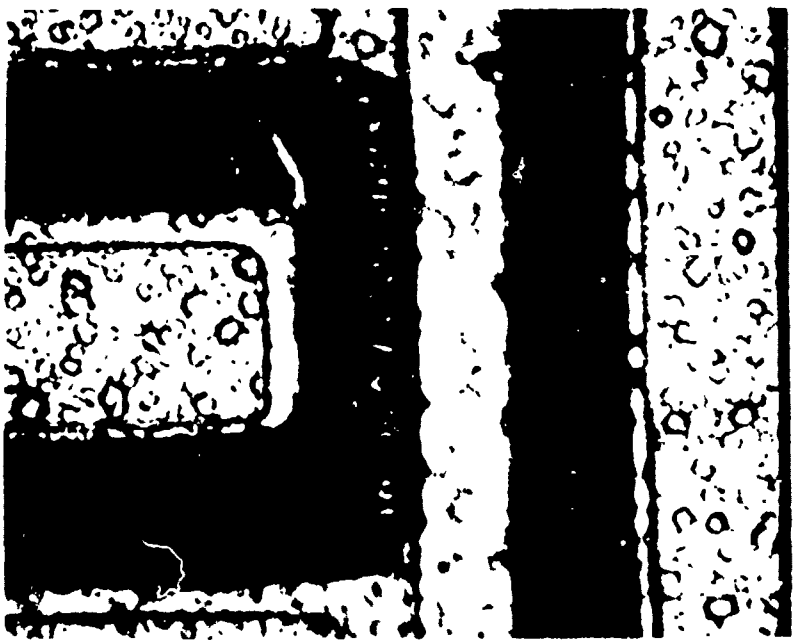

Figure 18 - Aluminum migration at the interface between thermal and deposited oxides.

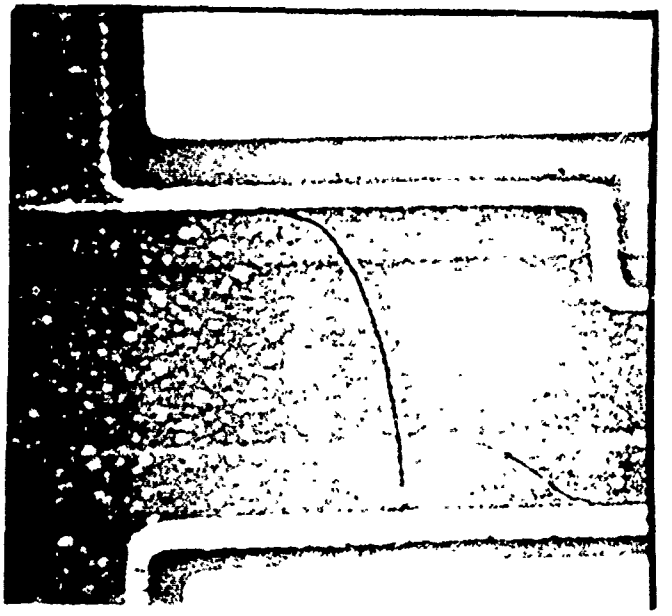

Figure 19 - SEM picture of glassivation cracks over the aluminum.

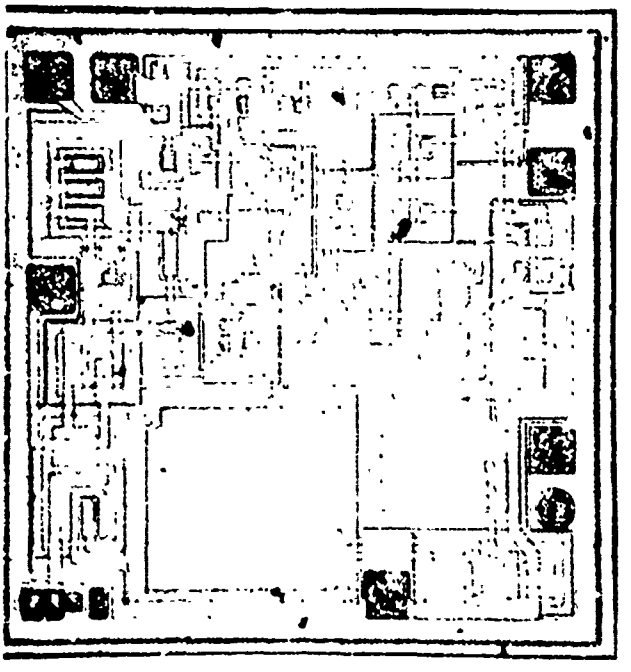

Figure 20 - IC chip with large MOS capacitor over which glassivation crazing readily occurs.

in a featureless surface. One may be tempted to conclude that the cracks are only over the metal, and that the metal has the pebbled appearance. Actually, the cracks are continuous across the metal-oxide boundary, and it is the glass which has the pebbled appearance.

Seeing all the problems which resulted from providing a glass protective layer, one questions the desirability of this approach. When first confronted with the evidence, the vendor indicated this to be a maverick lot. In a reprocurement, however, which involved three suppliers, the original supplier's chips had the same problem; the second vendor's chips showed some cracking over the large capacitor shown in a photograph of the chip design, Figure 20; and the third vendor's chips showed no cracking during the assembly process. It is not known whether the other vendors' chips had any aluminum migration or holes in the glass as seen in the first vendor's product.

DISCUSSION AND RECOMMENDATIONS

Glassivation is an important step in the production of chips for hybrid circuits. It is apparent, however, that this technique may not be a cure-all. The exact process and its control are important in providing a satisfactory mechanical protection layer or conformal hermetic seal. Some companies seem to have a process which provides a protective layer capable of withstanding a 400°C die attach cycle, wire bonding, and general handling without crazing, while others have not found a satisfactory process as yet. From our point of view, the problem is more complicated. Not only must the glassivation itself withstand the stresses encountered during assembly, but the reliability of the chip must not have been impaired by the glassivation process itself. The damage done to the metallization in the process used on the first vendor's chips will certainly influence the lifetime under operating conditions. Lot acceptance criteria must be

established for chips to eliminate the situation in which chips are mounted in circuits and then the circuits are rejected under MIL-STD-883 criteria. The lot acceptance would consist of visual inspection, mechanical stress test, and a thermal cycle test as a minimum.

CONCLUSIONS

We have examined three situations involving stress effects at material interfaces or in dielectric films. Each problem has its own best solution. In all cases, particular processes and process control are involved.

The fact that large stresses, both intrinsic and those due to differential thermal contraction, are introduced into films involved in microcircuit construction is well known. The effects of such stresses and stress relaxation on the long term reliability of integrated circuits are not known, and judging by the literature, little work has been done in the area.

One must be concerned with the rates of thermal rise during processing to avoid introduction of mechanical damage into the microcircuit being fabricated. This is particularly true when materials having large differences in their thermal expansion coefficients are in contact.

Glassivation is an excellent example of a process which is developed and applied to solve a specific problem, but which may itself introduce additional problems if not properly applied and examined, particularly for reliability consequences. In handling chips for hybrid circuit construction, glassivation is certainly a desirable, even a necessary process, but acceptance specifications should consider the physical and thermal aspects of integrated circuit design, as well as electrical, and provide necessary tests or screens to guarantee that the devices or circuits are acceptable on all counts, both before and after hybrid circuit construction.

It has been suggested several times that reliable devices can be made simply by using high temperature processes to fabricate the device and then operating the device at much lower temperature. While that procedure will eliminate some problems, it may generate others. Guidelines are good, but they can never be substituted for intelligent design. Knowledge of thermally induced stresses and the physical and electrical consequences of stress and stress relaxation effects are requirements for intelligent process design.

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