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RESEARCH INVESTIGATIONS ON FEEDBACK TECHNIQUES AND METHODS FOR AUTOMATIC CONTROL

CONTRACT NUMBER DAAB07-67-C-0520

FINAL REPORT

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APRIL 1969

BOSE CORPORATION
NATICK, MASSACHUSETTS

ECOM

UNITED STATES ARMY ELECTRONICS COMMAND · FORT MONMOUTH, N.J.

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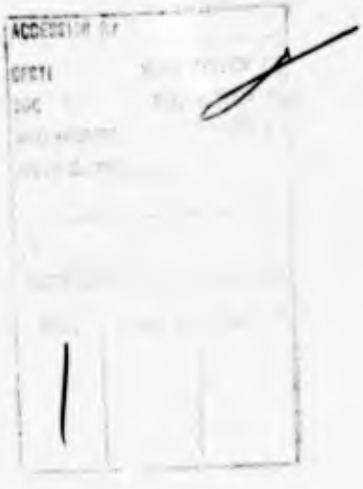

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ABSTRACT

A study of theoretical techniques applicable to the analysis and design of modern power processing equipment is presented.

An organizational structure is developed which defines a meaningful partitioning of a power system into component blocks at various levels. Considerations relevant to the various levels of this structure, both at the block diagram and circuit level, are treated. These areas include discussions of device models, dc power output stages and basic power converter limitations.

A survey of current computer programs applicable to the analysis and design of electrical equipment is presented. Brief treatments of some mathematical techniques, including Hilbert transforms, describing functions, phase-plane analysis and stability criteria are given.

The above theoretical tools are applied to the analysis of a practical power processor, and predicted characteristics compared with those observed in the laboratory.

Bibliographies are provided for three areas: power processors, mathematical methods and computer aided design.

ACKNOWLEDGEMENT

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1. INTRODUCTION

The design of power processing equipment is still in a stage where experimentation and intuition of the designer are often used in lieu of firmly based design concepts. An object of the present study is to alleviate this situation by bringing together those aspects of linear and nonlinear system analysis which are pertinent to the design and evaluation of modern power processing equipment.

Many problems encountered with complex systems show that current design and analysis procedures are far from adequate - systems that perform well in the laboratory may fail in the field; others may be so critical as to defy any attempts at production. In complex systems, compatibility and interconnection considerations cannot be ignored; a large system may fail to operate properly although the component subsystems may perform quite adequately by themselves. On the other hand, approaching the problem by looking only at an entire system is usually fruitless for all but the simplest systems. The separation of an entity into meaningful constituent parts is most useful in analyzing complex power systems.

Our goals have been to 1) formulate an explicit structure in which power systems would logically fit and would serve as a guide in the analysis and design of such systems, and 2) to initiate investigations of the relevant problems at various levels in this structure. A designer may often consider the various levels in this structure automatically when dealing with simple systems while complex systems are often handled by "feel" or intuition - making reliable complex system design difficult. The appropriateness of such a structure becomes clearer when further problems concerning power systems arise. For instance, information about the stability of an interconnection of modules is not best obtained from analysis at the circuit level.

The information obtained in any theoretical investigation of a power system must relate to the behavior of real devices - the models used must reflect the actual physical behavior to the extent required. (The problem of defining appropriate models is almost universal and not unique to power systems - or even electronics, for that matter.) Usually a compromise must be reached between the accuracy of the model and the complexity and interpretation of its analysis. The

division of power systems as presented here is itself a model, and work to this point indicates that it is a reasonable one which is both useful and meaningful.

As mentioned previously, this investigation is concerned with techniques applicable to the design and analysis of power systems. The manner of the investigation was based on four considerations:

1) Definition of the relevant class of systems to be modeled.

2) Development of a structural model for these systems.

3) Research into the relevant considerations at the various levels of this structural model.

4) Compilation of the analytical tools necessary to perform these investigations.

We should note that this report is not intended as an exhaustive study of power systems and analysis techniques. We could not hope to accomplish such a task in the time of this effort and, in fact, it may never be finished since the nature of the task is such that current topics can always be expanded and new ones added with future developments. In particular, a number of mathematical topics normally discussed in relation to feedback systems, such as the Nyquist criterion, Routh-Hurwitz and the root-locus test, have been intentionally omitted since these are part of the usual engineering background. We have assumed a basic knowledge of these topics and have presented instead some areas which may be less familiar but which complement the former topics and provide additional insight into the methods of analysis.

In this context, the topics covered in the next pages represent only only the beginning of the possible work which could be done in the respective areas, but we hope that they will provide a base and guide for future investigations.

2. THE STRUCTURE OF POWER SYSTEMS

Failure of a power processing system to perform its intended mission can often be traced to a design deficiency in some small part of the system. By examining a number of power processor designs, certain fundamental similarities have been discovered among apparently diverse systems. Research presented in this report has been directed toward evaluation of these similarities and development of an orderly procedure for analysis or synthesis of power processing systems. A thorough understanding of the common base shared by power processors, if properly applied, can lead to improvements over present day systems in cost, reliability and performance by serving as a guide to the choice of both the optimum approach and circuitry for a given function.

To facilitate the breakdown of power processing systems, a hierarchical structure describing the manner in which systems are built up has been hypothesized. By an iterative partitioning of a system at each of its levels, attention may be focused on the essence of the power processing system - those portions which actually perform the conversion of the electrical power. The following methodology, applicable to automatic control systems, outlines and defines this structure.

To the uninitiated, a power system imbedded within and perhaps indistinguishable from a total system appears to be a vastly complex aggregate of a variety of components working together to provide the power needs of the still more complex functional system. Our present concern is only with power systems, which will be treated as a separable part of a functional system. The power portion of the total system is distinguished by the following characteristics:

1) Power is the variable being operated upon - i.e., the variables in the circuits are voltages and currents whose magnitudes are the quantities of interest whether or not these voltages and currents are at the same time analogs of other quantities. This is in contradistinction to signal processing circuits where the voltages and currents represent and have some functional relationship to other variables and only the functional relationship is of importance.

2) Power handling is performed in such quantities that thermal parameters associated with the elements of the system must be taken into account in the design of the system. Both the effects of ambient thermal conditions and thermal gradients due to operation of the system are significant design considerations.

Even to an engineer well versed in the power field, a single schematic diagram of a complete power system may be incomprehensible if no other information is furnished. It is evident that some organization or structure must be imposed upon the system if it is to be evaluated or easily comprehended by anyone other than the designer. In fact, it is impractical even to design a power system of just modest complexity if some form of organization is not imposed upon the system in its conceptual stages.

Examination of a number of power systems reveals that a system is composed of an aggregation of parts or modules meeting the above criteria which process power in some way and interconnections which tie the modules together by providing signal and power transmission paths. These modules, along with the circuitry necessary for energizing, sensing, controlling and indicating purposes, whether internal or external to the module, will be defined as the power processors of the power system. Figure 2.1 illustrates an example of one embodiment of a power processor. Our interest will be restricted to power processors which are purely electrical in nature, i.e., those elements which have electrical inputs and outputs. Electro-chemical devices such as batteries, electro-mechanical devices and prime power sources encountered in power systems will be viewed as complete and indivisible power processors and treated as modules to be modeled by their electrical terminal characteristics.

Figure 2.2 illustrates the block diagram of an example of a power system and its constituent power processors. This block diagram represents a high reliability dc power supply operating from an ac prime source. In normal operation, ac power is drawn from the power mains and fed through the line selector to the redundant ac - dc converter/regulator power processors. The output of these modules is fed to a supply selector which connects the output of one of the modules to the dc output terminals, provided that module is functioning properly. At the same time, the battery charger power processor

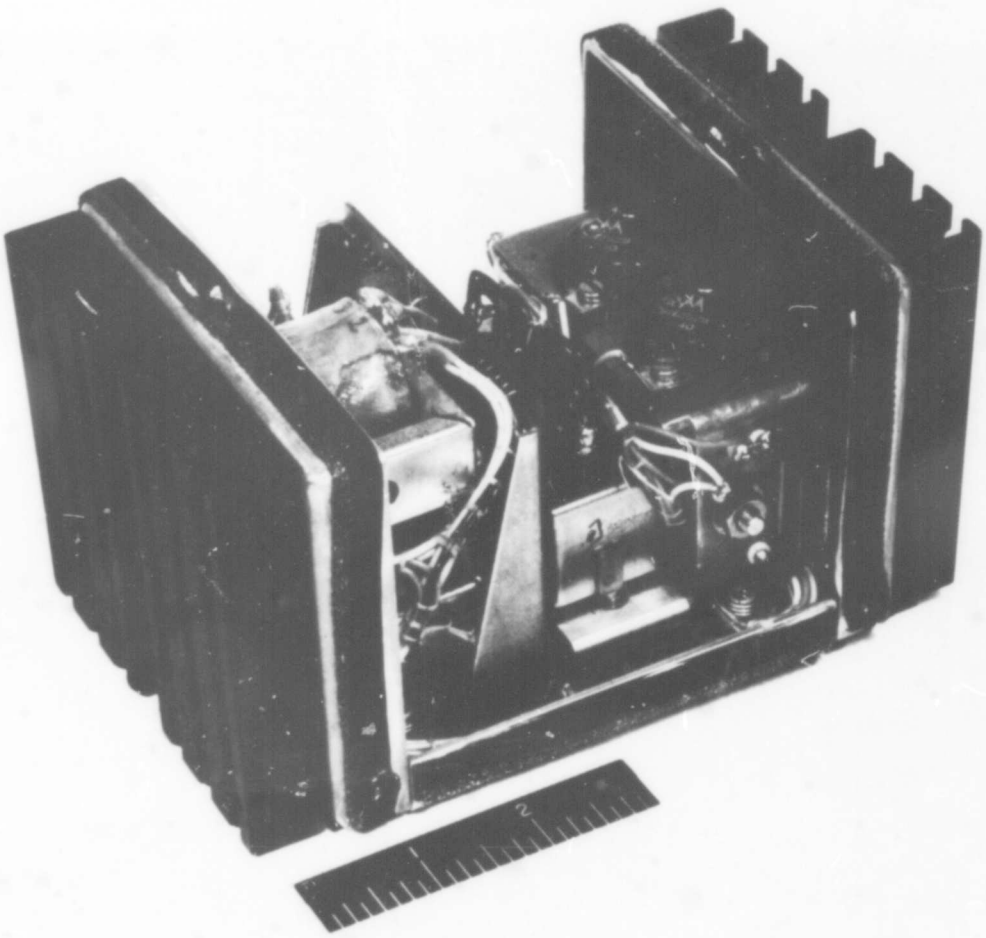


FIGURE 2.1

EMBODIMENT OF A POWER PROCESSOR

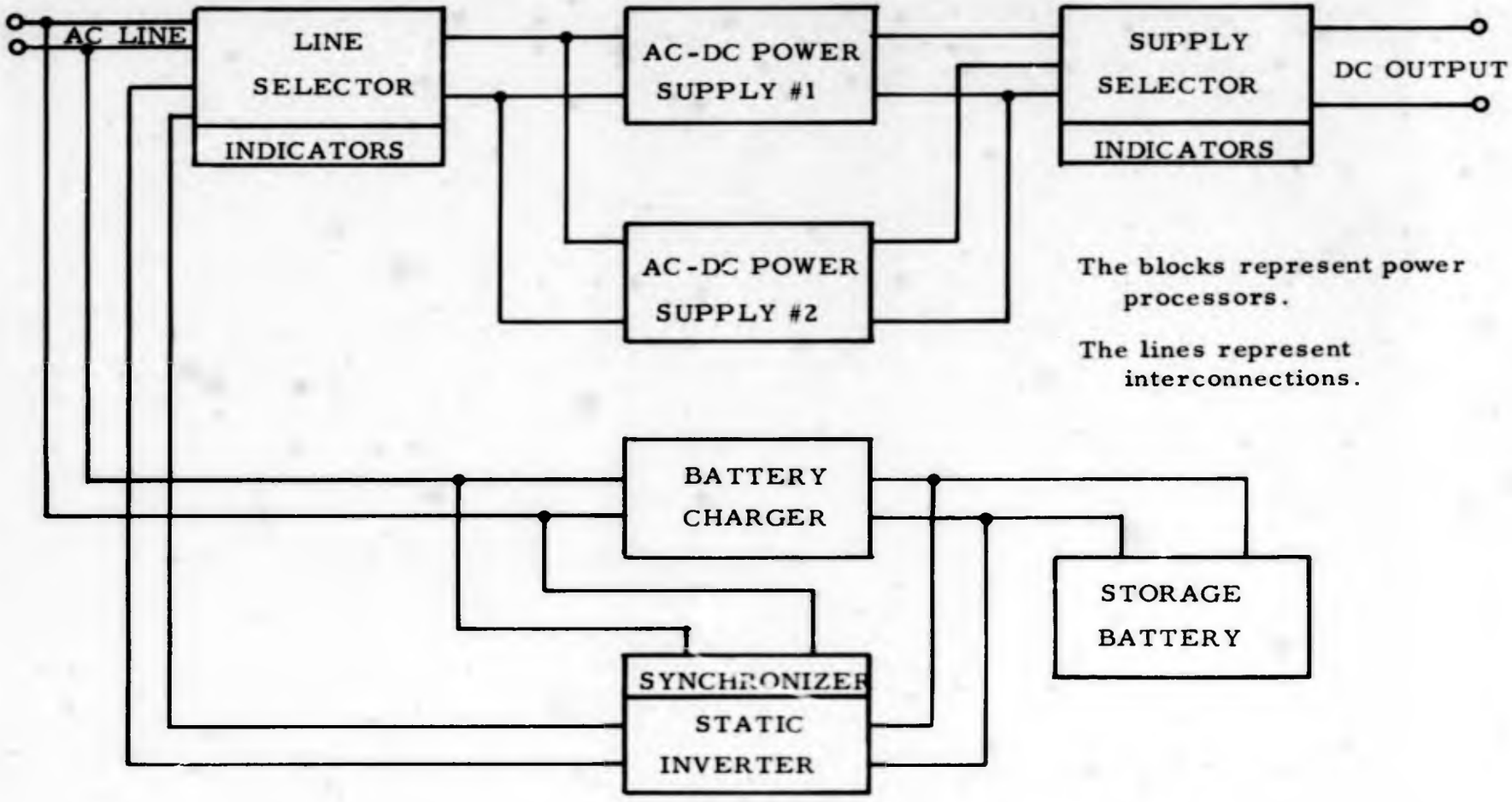


FIGURE 2.2

POWER SYSTEM EXAMPLE

maintains the storage battery in a fully charged state and the synchronizer provides the dc - ac static inverter power processor with a signal which insures that the ac output of the inverter is synchronized with the power mains at all times.

If the prime source of ac power becomes unsuitable for use by the ac - dc power supplies (this can occur by frequency deviation, under and over voltage deviations as well as complete source failure) then the line selector will transfer the power load to the output of the static inverter. The storage battery acts as the source to provide an uninterrupted system output. Upon restoration of the ac mains power, the line selector transfers the power load back to the prime source and the battery charger recharges the storage battery.

In the event of a failure within the ac - dc power supply connected to the system output, the supply selector connects the redundant supply to the output terminals.

This simple example indicates the nature of a power system and the initial partitioning of the system into modules. It is evident that these modules perform a complete power processing function such as regulation, inversion, conversion, limiting or a combination of these functions. It is also evident that the power processor includes all of the auxiliary circuitry necessary to perform its functions --- some of which are internal power regulators, programing, synchronizing and timing facilities, meters, calibration facilities, switches and interlocks. For the purpose of integration into a system, the interface characteristics of power processors are specified in terms of the terminal properties (usually designed or constrained by a set of specifications) of the individual unit. Implicit in the specification of terminal properties is the implication that the circuitry internal to an individual unit will operate in a predesigned and well controlled manner if the terminal constraints dictated by the specifications are observed. The fact that this is not always the case provides the motivation to look beyond the terminal properties of a power processor in evaluating a completed unit to determine whether its performance will be adequate to meet the necessary mission requirements.

An example of a physical embodiment of a power system is illustrated in Figure 2.3. In this example, the individual modules or power

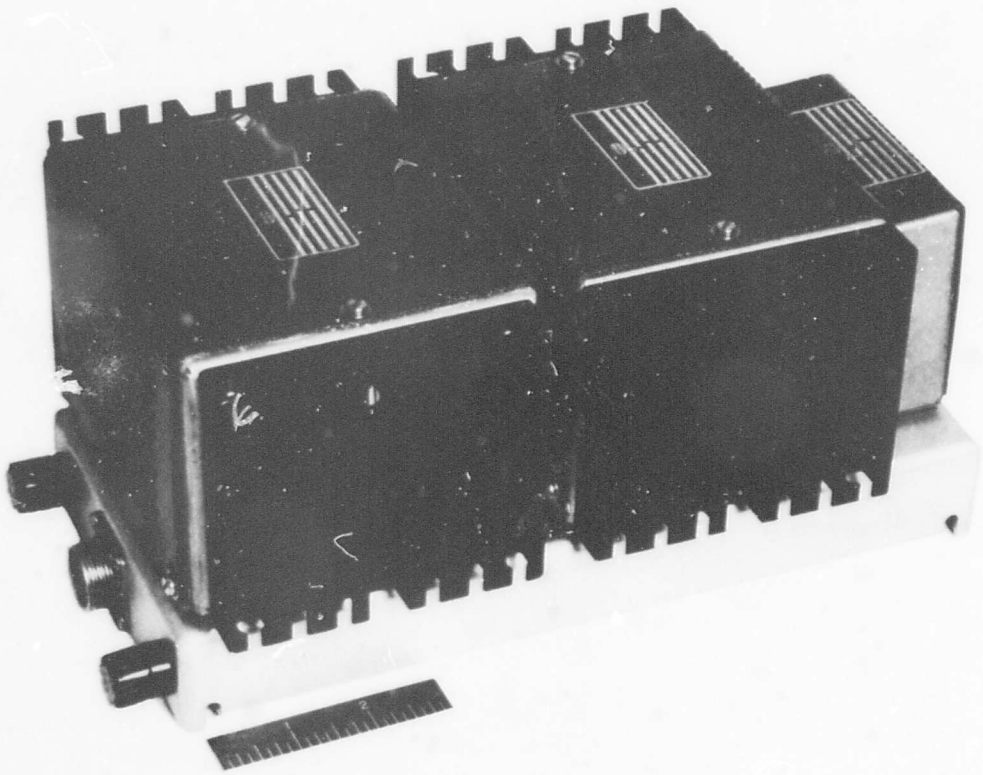


FIGURE 2.3

EMBODIMENT OF A POWER SYSTEM

processors are quite obvious due to the modular construction of the system. Some of the protection circuitry auxiliary to the power processors is also visible on the panel of the unit. It is easy to imagine a multiplicity of these systems combined with others to form larger and more complex power systems. Thus, it is evident that the definition of a power system is recursive, i.e., power systems may, in themselves, contain subsections which could be considered power systems. Of course, in the overall power system, the system shown in Figure 2.3 would be considered a power processor, since it forms only one of the modules of the larger system. Thus, the definition of a power processor is also recursive; power processors may contain a set of individual modules which can also be treated as power processors.

To what level a system need be partitioned depends on the purpose of the partitioning. If the terminal specifications of a particular power processor within a system are considered satisfactory, and the design of that power processor is considered adequate to meet the terminal specifications with the internal circuitry operating in a well controlled manner and all components operating within their individual specifications, then the power processor need not be further partitioned. If any question concerning internal operation exists, then additional partitioning and analysis must be performed until the questions are resolved.

When repeated partitioning of a power system is performed, the system is ultimately separated into power processor blocks which cannot be further subdivided and still meet the definition of a power processor, i.e., a module of a system which performs a complete power processing function. The resultant power processing circuit at this level is usually still too complex to permit a thorough analysis in an efficient and meaningful manner. To facilitate this analysis, further segmentation of the unit into basic power converters and auxiliary circuitry may be performed. A basic power converter is defined as that portion of a power processor which performs a power conversion task, exclusive of the auxiliary circuitry necessary to produce a practical embodiment of the converter.

A power processor may be composed of several basic power converters connected in a series/parallel manner to perform the desired power processing, each power converter performing one step of the total operation. The auxiliary circuitry common to all of these power

converters may be treated separately; e.g., a circuit which processes power for auxiliary functions may be considered a basic power converter while a timing circuit may be viewed as providing a control signal to the power converter. As a specific example, it is common to include a low-power precision-regulated power supply to provide a reference voltage for the main power converter. Such an auxiliary supply could be treated by employing the same approach used to evaluate the main converter, yet it does not handle power which is delivered to the output.

Figure 2.4 illustrates an example of the block diagram of an ac - dc power processor which might be encountered in a battery charger or dc power supply application. With the exception of the auxiliary circuitry block, each of the blocks represent a complete basic power converter. The auxiliary basic power converters, which conditions the power necessary to run the auxiliary control circuitry as well as the main converters, are shown.

The interface characteristics between the blocks may be represented by electrical terminal properties and thermal characteristics as is done with power processors. For design purposes, it is usually necessary to require that terminal specifications be adequate to completely characterize each of the blocks. This insures compatibility of design, i.e., in a design, the basic power converters are expected to be capable of working together after being developed separately.

To further partition the system, the power converter may be modeled as a combination of a control concept and an output power stage. In its essence, a control concept represents a methodology for operating or controlling the output power stages. A complete control concept includes a methodology of control plus a mechanization for receiving signals from sensors, reference and control elements and from these generating a suitable set of control signals which satisfies the chosen methodology for an output power stage. Depending upon the specific control concept and sensors employed, this may be either an open-loop or closed-loop control of some output variable.

The choice of control concept is governed by the following principal constraints:

1) Output power stage selected to perform the power conversion.

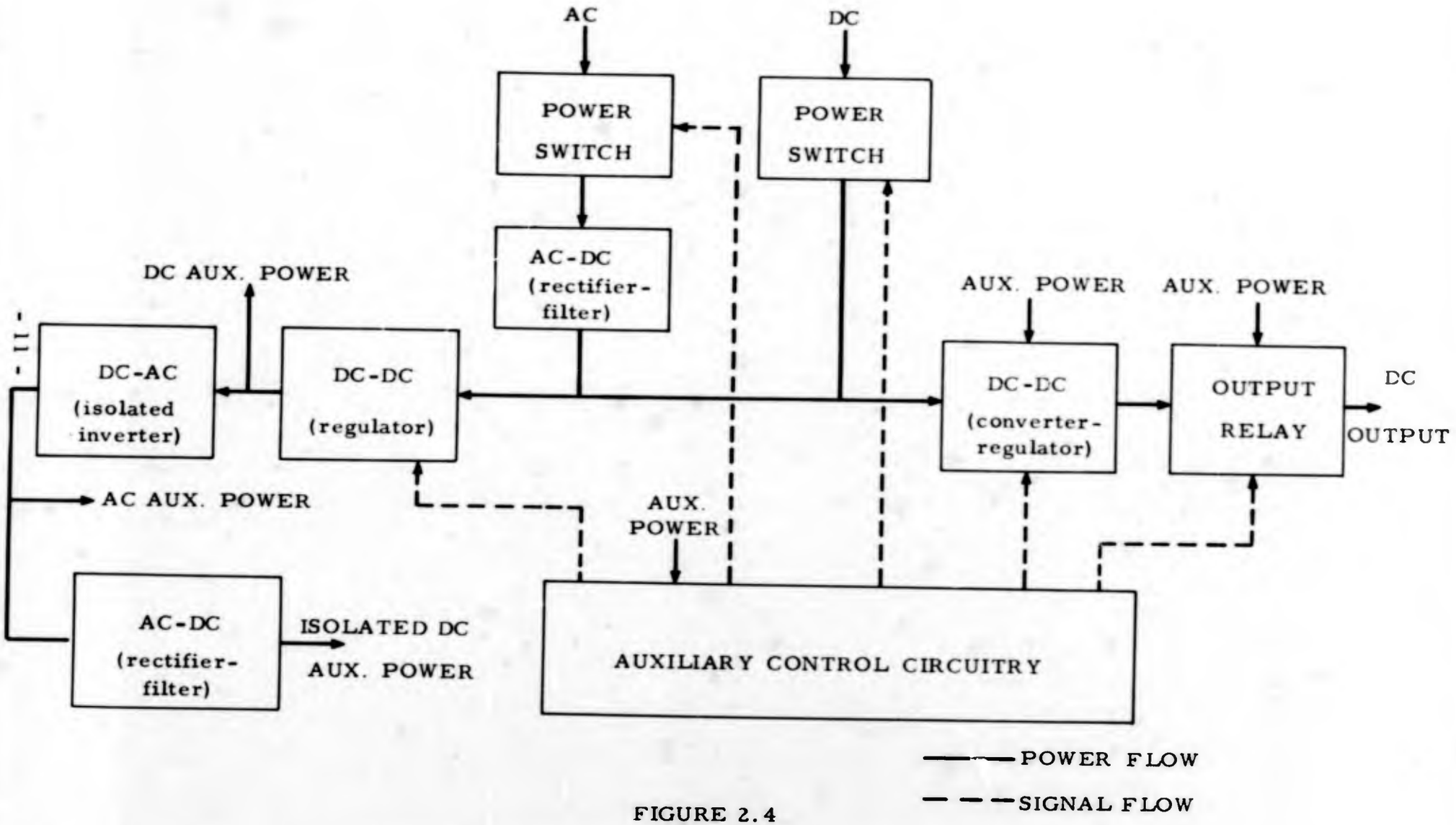


FIGURE 2.4

EXAMPLE OF A BLOCK DIAGRAM OF A POWER PROCESSOR

2) System requirements of the power converter (e.g. efficiency, cost, size and weight, load regulation, source regulation, reliability, isolation, etc.).

The output power stage limits the choice of control concepts to those that are compatible with it. A control concept designed for one particular output stage can often be modified to effect compatibility with other output stages either by minor modification of the methodology and the mechanization or by a modification in the mechanization alone.

The system requirements constrain the choice of control concept both indirectly and directly. Indirectly, the system requirements dictate use of an output stage which has the inherent capability of meeting these requirements. Directly, the system requirements dictate the choice of a control concept that is both compatible with the output power stage and, when combined with the power stage, will yield a power converter which meets the requirements.

The power output stage is defined as the portion of the basic power converter which actually handles the power. There are four major types of power stages which are used to handle electrical energy. These stages are classified by the method of operation of the power control element. These are:

1) Active linear (e.g. tubes, transistors)

2) Mechanical (e.g. relays, variable transformers)

3) Saturable magnetic (e.g. magnetic amplifiers)

4) Switching (e.g. thyristors, switching transistors).

In addition to the control elements, energy storage and filtering elements, mutually coupled magnetic elements (e.g. transformers) and steering and clamp diodes may be included as part of the output stage. Sensors to provide feedback signals to the control circuitry complete the output stage.

Figure 2.5 shows a very simple example which illustrates the salient features of a basic power converter. The converter shown is an ac-ac voltage regulator which achieves regulation by changing taps on an auto-transformer. The output stage, a mechanical type, is

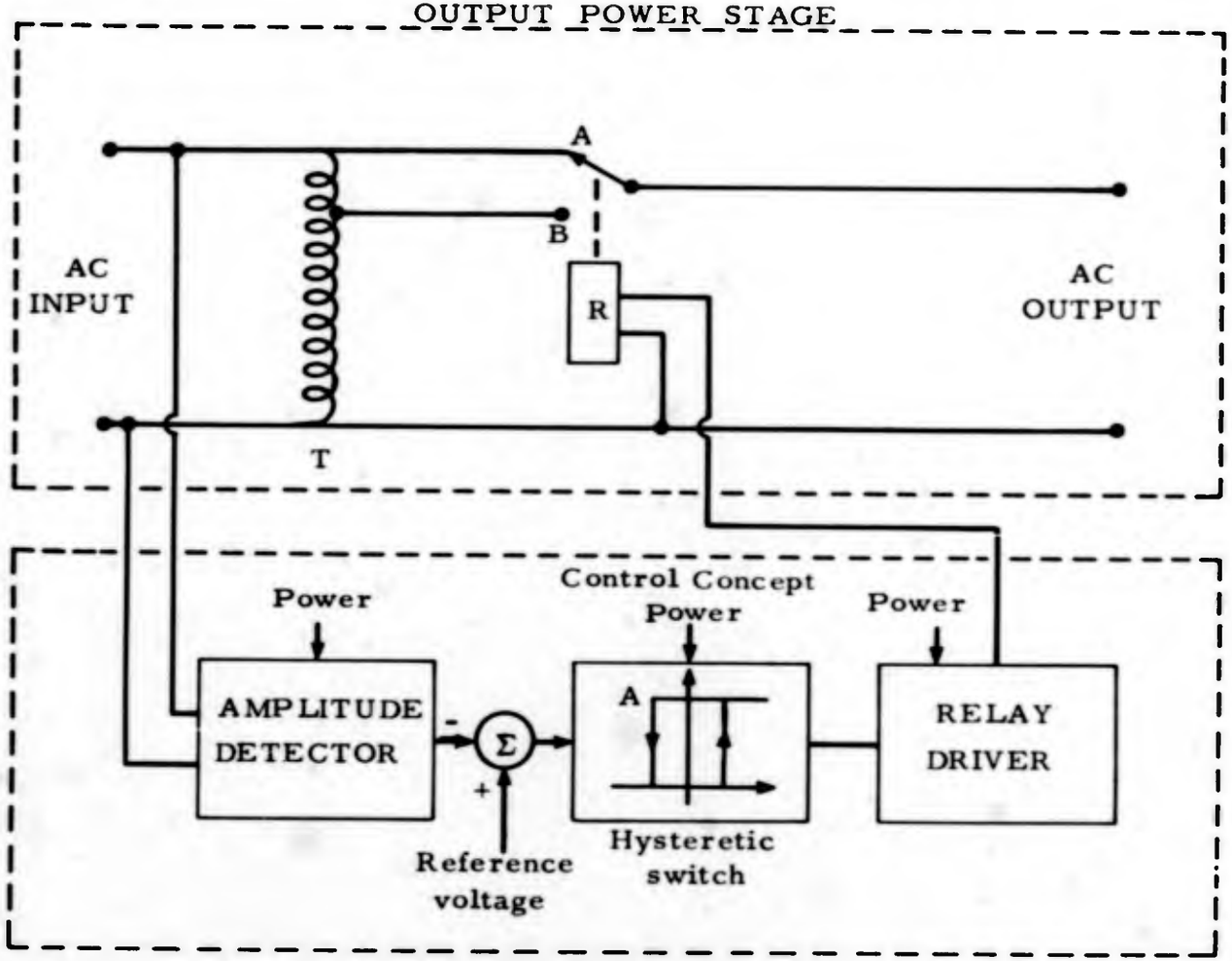


FIGURE 2.5

AN EXAMPLE OF A BASIC POWER CONVERTER:
AN AC-AC VOLTAGE REGULATOR

represented by the tapped auto-transformer T and the relay R which selects between taps A and B on T. The methodology of control is to compare the ac input voltage with a reference. The difference between the two is applied to a threshold detector. Whenever the difference exceeds a given threshold, the relay switches to the appropriate tap to minimize the error. Hysteresis is included in the threshold device to prevent relay chatter near the switching point. The mechanization of the control concept methodology is shown in the figure and consists of an amplitude detector, differential summing network, hysteretic switch to set the threshold and a relay driver to operate R. The auxiliary functions necessary to operate this power converter are a power supply and a reference voltage generator. These functions are not considered part of this converter.

Block diagrams of output stages, control concepts and auxiliary functions may be used to provide valuable information concerning the performance of a power processor. However, to perform a complete evaluation, block diagram analysis is inadequate. The actual circuits within the block must be examined to insure that the block will perform according to its terminal specifications (the model which the block represents) under all conditions. To perform the more detailed circuit analysis, the circuit schematic diagram is required to provide electrical component interconnection information and, in addition, assembly and wiring diagrams are required to provide physical placement and structural information. Since thermal factors and, in many systems, spurious electrical coupling between different portions of the circuit must be evaluated, physical factors are as important in the electrical performance evaluation of a power converter as are the electrical factors represented by the schematic diagram.

Assembly, wiring and schematic diagrams specify the structure of the basic power converter and power processor, i.e. the types of components used (resistors, capacitors, inductors, etc.), their electrical interconnections and their physical placement. This is adequate to perform a qualitative or algebraic evaluation of the power processor and, by suitable combination, a qualitative evaluation of the system. To perform a quantitative evaluation, numerical data pertinent to the components and subassemblies of the power processor must be analyzed. This information may be obtained from sources such as the parts and material lists and specifications, detail drawings, quality control and reliability data,

etc. Only by quantitative analysis can actual performance capability of a power system and its components be verified.

Whether in fact, a system that has been satisfactorily evaluated and is subsequently fabricated actually meets its intended mission requirements depends wholly on the accuracy of the analysis used in the evaluation. Assuming that no numerical error has been made in the analysis (a not unlikely occurrence in a complex problem, but one that is at least in principle, avoidable), the prime source of disagreement between the results of evaluation and actual performance lies in the accuracy of the models used in the analysis to represent the physical components of the system. No component performs ideally and all components have limitations on every variable associated with them which cannot be exceeded without permanently degrading that component. A model used in the analysis must reflect these factors to whatever degree is necessary to insure accuracy in the overall evaluation.

Since very detailed models of each component make analysis difficult and cumbersome, some compromise must be reached in the choice of a model. Some components, because they represent relatively new developments, have not been well characterized by models. Other components, because of the difficults of controlling their parameters, are not well represented by any model. These factors considerably complicate the analysis problem and may require the use of models based on statistical data, rather than the physics of operation.

A diagram summarizing the structure of power processing systems that has been discussed in this section is shown in Figure 2.6. All of the segments are shown in their relation to one another as the system is repeatedly partitioned. It is interesting to note that the ultimate limitation on the accuracy by which performance of the power system may be predicted (first block) is set by the accuracy with which the device and component models may be specified (last block). The entire structure between these two blocks serves to relate these detailed models to the overall system in a logical and orderly manner. The discussion and investigations of power processing systems will cover considerations at the various levels of Figure 2.6.

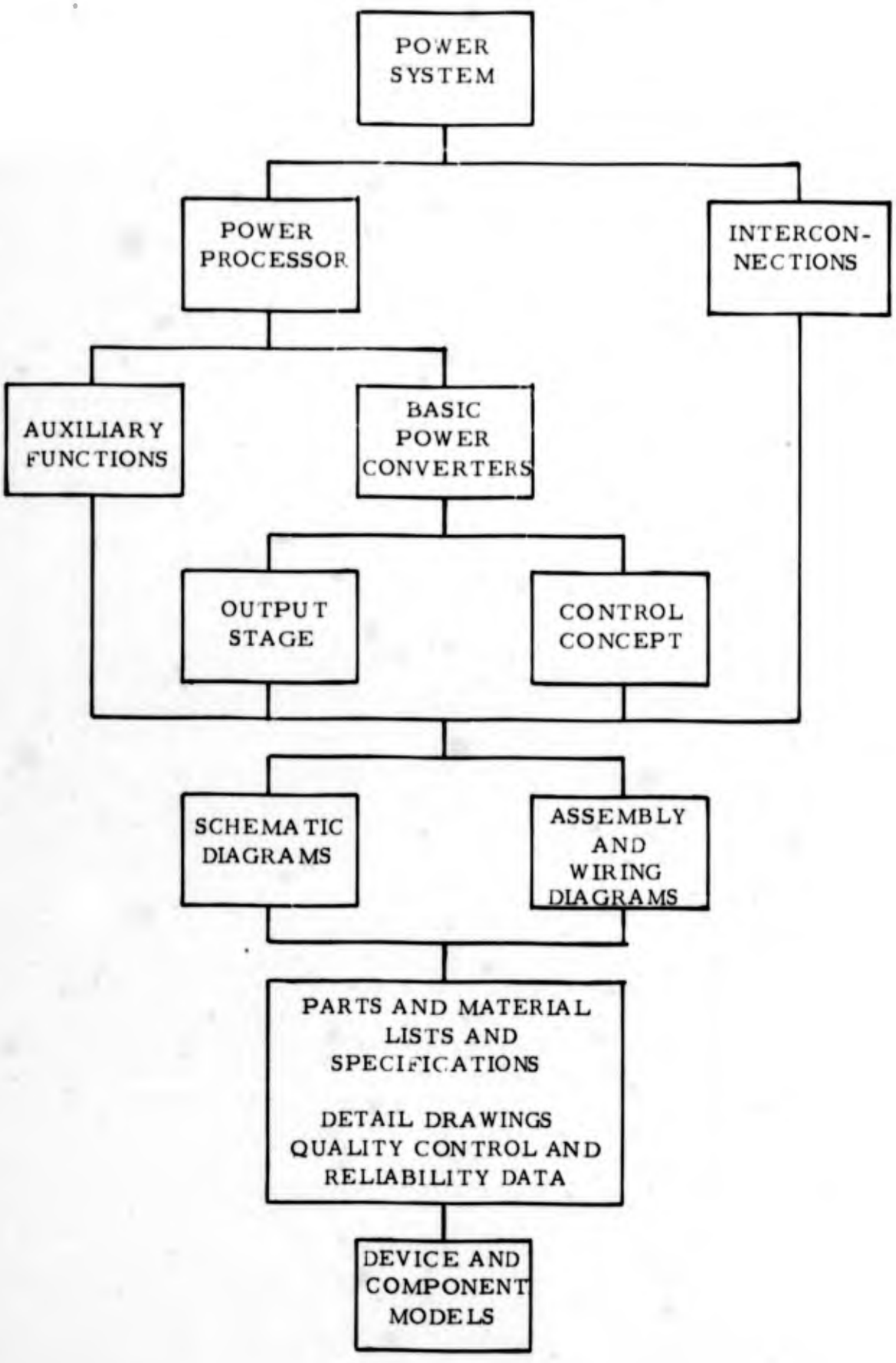


FIGURE 2.6

STRUCTURE OF POWER PROCESSING SYSTEMS

3. DEVICE AND COMPONENT MODELS

In this chapter, the static and dynamic characteristics of practical devices are presented. Where possible, models which relate pertinent device parameters are developed which are suitable for use in circuit analysis. Temperature dependencies of parameters are examined and graphs which allow the effects of temperature to be quantitatively assessed are included. The emphasis here is on the large signal models and characteristics of devices where non-linearities become significant in describing operation. This is the region of operation normally encountered in switching circuits or in the devices used in the output stages of switching power processors.

The models that are developed in this section are simple ones which may be used to assess specific properties of operation of the circuit in which they are embedded, therefore, the model appropriate to the circuit property or characteristic being investigated must be used to obtain meaningful results. These models are simplified in a way which focuses attention on a specific facet of transitor behavior, yet when the models are substituted for the actual device, the ensuing analysis is not impossibly complex. When this type of model is used, the accuracy in predicting the behavior of a specific device suffers, but, for solid state devices, the normal manufacturing spread of individual device behavior is much greater, making the model inaccuracies negligible by comparison.

3.1 SEMICONDUCTOR DIODES

Static Characteristics

The schematic symbol and terminal variable designation for a diode is illustrated in Figure 3.1. For many analysis purposes, the diode may be modelled as a perfect uni-directional switch; one having zero voltage drop in the direction of conduction and zero current flow in the direction of non-conduction. This volt-ampere relationship is graphically shown in Figure 3.2a and the corresponding models for the two regions of operation shown in Figure 3.2b.

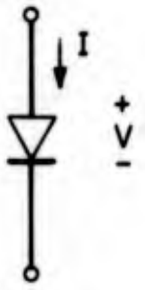
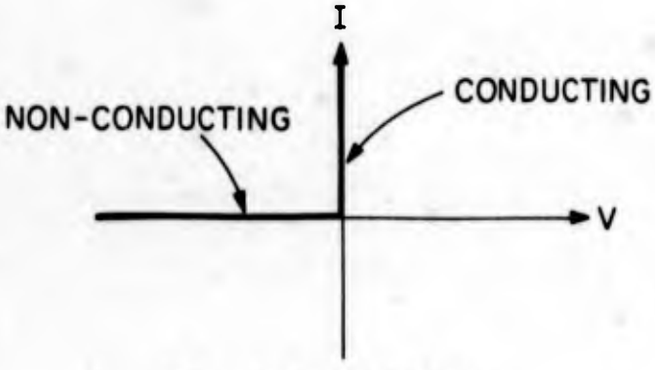


FIG. 3.1 SCHEMATIC SYMBOL AND TERMINAL VARIABLE DEFINITION FOR A SEMICONDUCTOR DIODE



(a) V-I RELATION

(b) MODELS

FIG. 3.2 GRAPHICAL VOLT-AMPERE RELATIONS AND MODELS FOR "PERFECT" DIODE

For applications where a more accurate model is required, a volt-ampere relationship based on the physics of diode operation may be employed. The ideal diode volt-ampere relationship may be expressed algebraically by

$$I = I_s(T)(e^{\frac{qV}{nkT}} - 1) \qquad (3.1)$$

where $I_s(T)$ is a temperature dependent parameter of the diode, T is the absolute temperature of the device, q is the magnitude of electron charge, k is Boltzmann's constant, $\frac{q}{k} = 1.16 \times 10^4 \ \frac{^\circ K}{volt}$ and n is a parameter dependent on the details of fabrication of the diode and lies in the range

$$1 < n < 2.$$

For a given diode n may vary slightly with current level, but for circuit analysis purposes n may be taken as a constant with only minor error.

A plot of Eqn. 3.1 in the normalized form $\frac{I}{I_s} = e^{\frac{qV}{nkT}} - 1$ versus the factor $\frac{qV}{nkT}$ is shown in Figure 3.3. The scales are chosen to represent the current that would be observed for a silicon diode operating near room temperature. It is evident that the crude model of Figure 3.2 closely approximates the physical model of Figure 3.3 and may be used for calculating the gross operation of a circuit.

Figure 3.4 shows a plot of Eqn. 3.1 on a finer scale than Figure 3.3. Superimposed is a plot of

$$\frac{I}{I_s} = e^{\frac{qV}{nkT}} \qquad (3.2)$$

and

$$\frac{I}{I_s} = -1 \qquad (3.3)$$

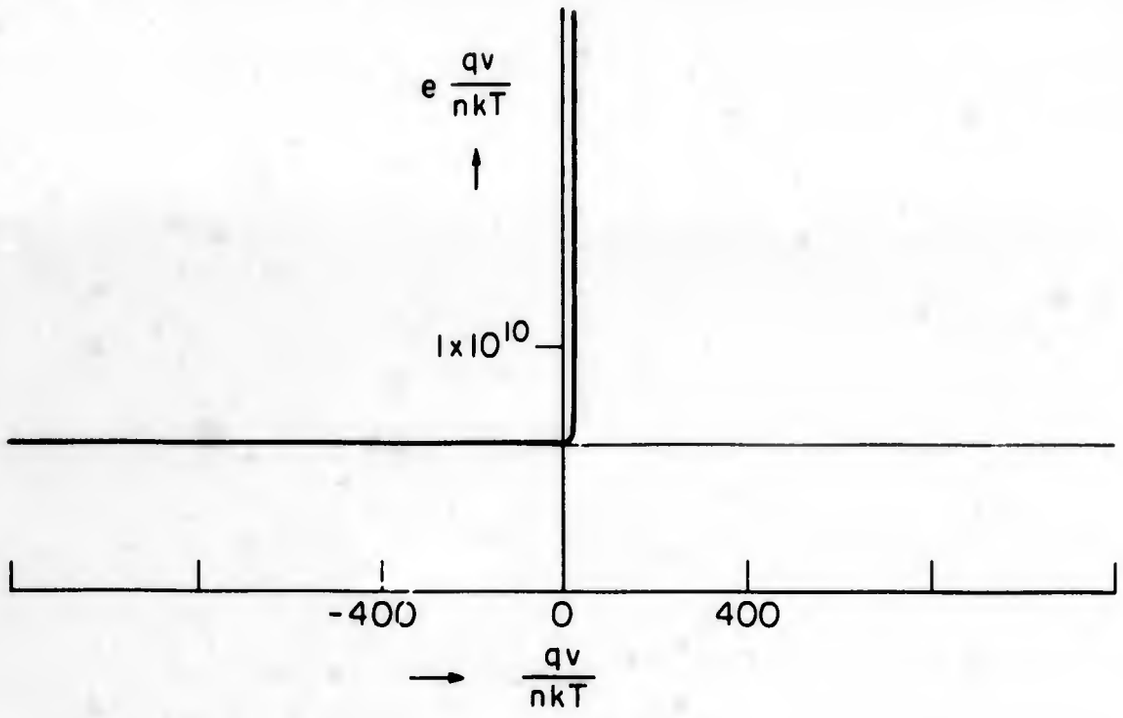


FIGURE 3.3

NORMALIZED IDEAL DIODE CURRENT VERSUS EXPONENT

For $\frac{qV}{nkT}$ greater than about 3, Eqn. 3.2 describes forward conduction with negligible error. For $\frac{qV}{nkT}$ less than about -3, Eqn. 3.3 describes the non-conducting region with negligible error. For the temperature region of practical silicon diode operations, $-50^{\circ}C < T < 150^{\circ}C$, $\frac{qV}{nkT} = 3$ implies $V < 0.22$ volts.

Eqn. 3.1 accurately predicts the conduction region behavior of a diode over the range of moderate current levels for the diode being investigated. As the current approaches the rated value of the diode, series resistive effects in the semiconductor material become predominant. Figure 3.5 is a volt-ampere plot of the forward characteristics of a typical 15 ampere silicon power diode. In the region below about 1 ampere, the diode may be described by the ideal diode law of Eqn. 3.2 with parameters

$$I = 3.0 \times 10^{-12} \, e^{\frac{V}{29 \times 10^{-3}}} \text{ amperes}$$

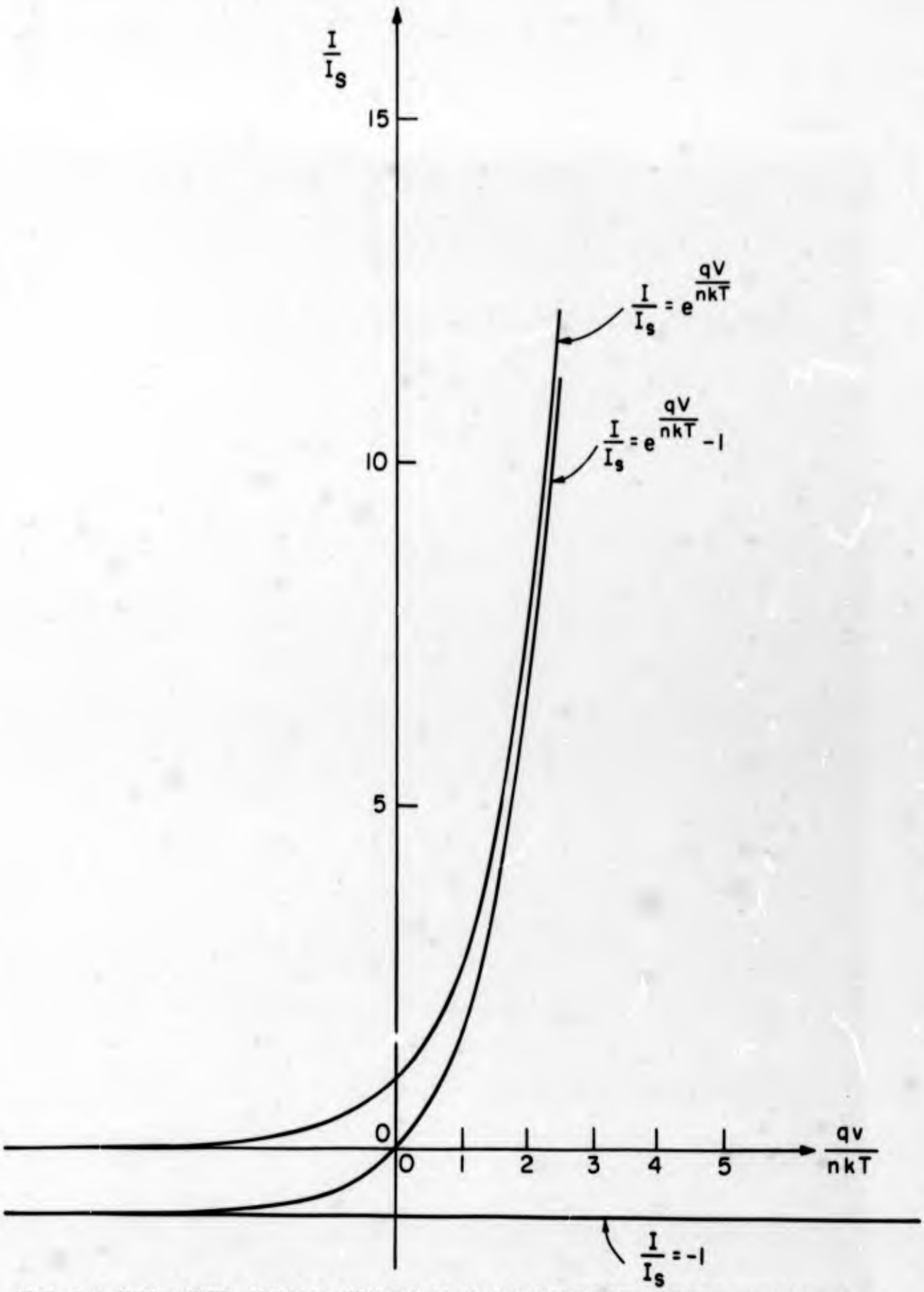


FIG. 3.4 EXPANDED NORMALIZED IDEAL DIODE CURRENT VERSUS EXPONENT AND APPROXIMATIONS

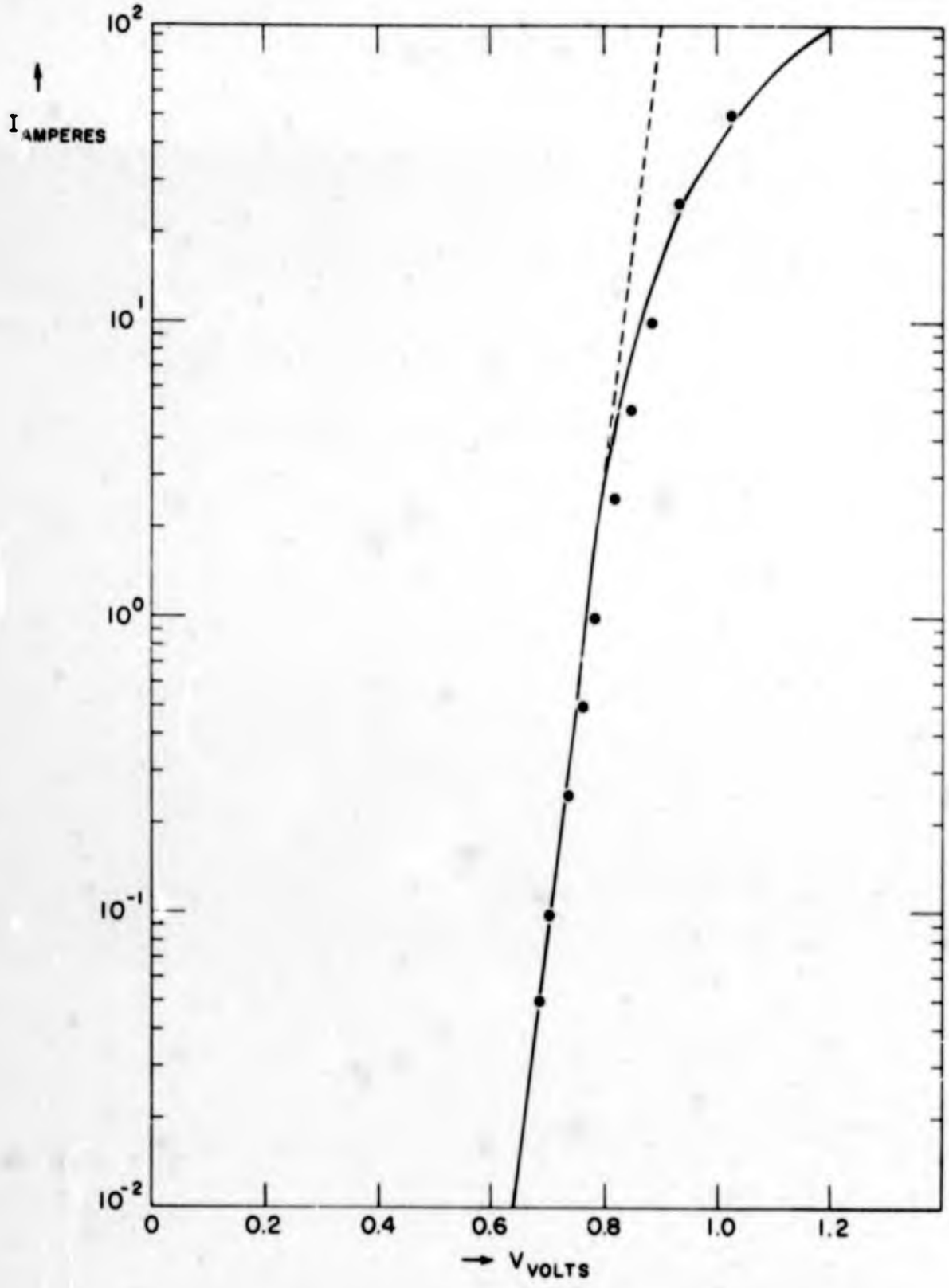


FIGURE 3.5

FORWARD VOLT-AMPERE CHARACTERISTICS OF A SILICON POWER DIODE

Above one ampere, the excess voltage over the ideal diode curve for a given current becomes marked. Typical practice in the maximum average current rating of a diode is to choose a current level where the voltage drop due to resistance of the semiconductor material has become appreciable, but not excessive. This maximum current point might be set at the point where the diode terminal voltage was two to three times the junction voltage for the worst-case device in the line. For static analysis, the bulk resistive effect of the material may be modeled by a fixed resistor in series with an ideal diode as shown in Figure 3.6. The volt-ampere relationship of this diode in the forward direction is

$$V = IR + \frac{nkT}{q} \ln\left(\frac{I}{I_s}\right). \qquad (3.4)$$

This equation is most conveniently solved graphically using measured data or worst-case specified parameters. In Figure 3.5, Eqn. 3.4 is plotted (superimposed on the measured volt-ampere curve) using the parameters of Eqn. 3.3 and an experimentally fitted R of .003 ohms to give the equation

$$V = .003I + 29 \times 10^{-3} \ln\left(\frac{I}{3.0 \times 10^{-12}}\right) \text{ volts}. \qquad (3.5)$$

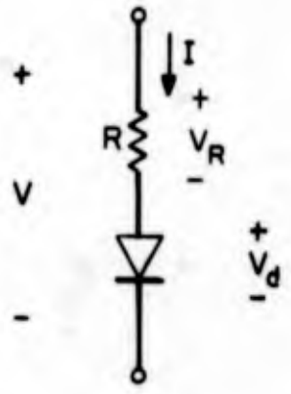


FIGURE 3.6

DIODE MODEL WITH BULK RESISTANCE

It is evident that the model and measured data closely match. The differences may be attributed to the conductivity modulation effect.* Conductivity modulation, associated with operation of the diode junction, causes the bulk resistance to decrease as the diode current increases. For circuit analysis purposes, variation in diode resistance with current due to conductivity modulation does not cause significant errors when the model of Figure 3.6 is used.

When the diode voltage reverses, biasing the diode into the nonconducting region of operation, the characteristics depart from the ideal diode curve of Figure 3.4 due to extraneous leakage effects. The ideal diode model predicts leakage due only to bulk diode operation. In devices presently available, bulk effects predominate under forward and high temperature reverse bias operation. At low and normal temperatures, the extraneous effects may become predominant in determining reverse biased leakage. The normal reverse saturation current predicted by the ideal diode law is independent of the applied reverse voltage (see Figure 3.4). The two principal extraneous effects are both reverse voltage dependent. Surface junction leakage is a component of current which flows around the edges of a semiconductor p-n junction. It is essentially resistive. Depletion region carrier generation is the second leakage effect and is due to currents generated within the diode junction. The magnitude of this current depends on the volume of the depletion region of the diode junction which, in turn, is nonlinearly related to the reverse voltage. This current has a dependence on applied voltage between the limits of $(-V)^{\frac{1}{2}}$ and $(-V)^{\frac{1}{3}}$ depending on the fabrication details of the diode. Figure 3.7 is a volt-ampere plot of the reverse characteristics of the diode whose forward characteristics are plotted in Figure 3.5. At room temperatures, surface effect dominate the leakage and the behavior is anomolous. At elevated temperatures (T = 100°C), bulk effects dominate and the leakage, while greatly increased, is smooth with voltage. Superimposed on the T = 100°C curve is an empirically fitted curve with the equation

$$I = 10^{-7} + 3.25 \cdot 10^{-7} (-V)^{\frac{1}{3}} \text{ amperes}, \qquad V < 0.$$

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* Bibliography III, Reference 24.

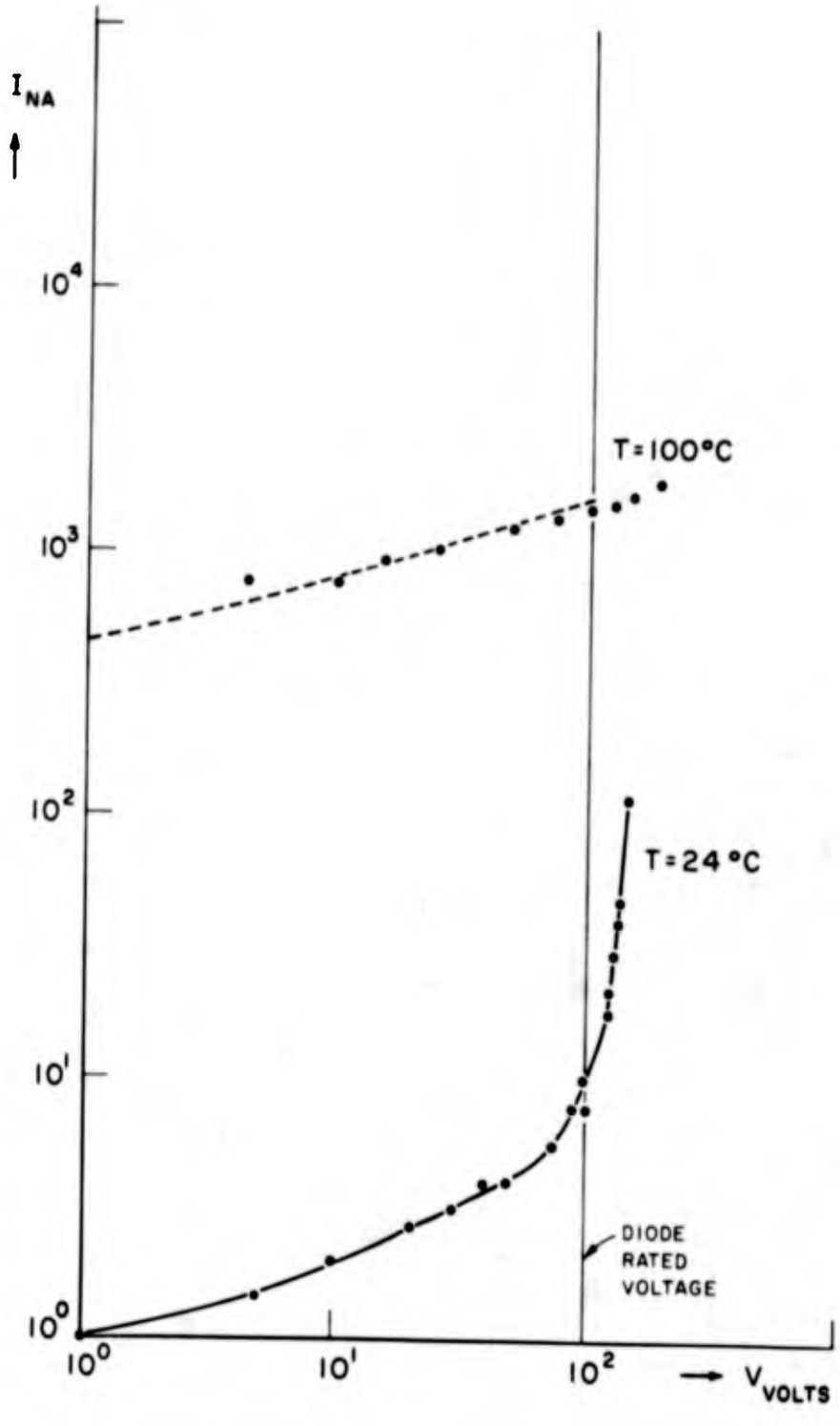

FIG. 3.7 REVERSE VOLT-AMPERE CHARACTERISTICS OF A SILICON POWER DIODE.

The fit of this curve is sufficiently close for use in circuit analysis problems where this leakage may be significant.

Voltage dependent leakage current is generally small (less than 1.0 μampere) in currently available silicon diodes and is dominated by bulk leakage currents at high temperatures. For these reasons, voltage dependent leakages may usually be ignored in circuit analysis and a bulk leakage model used to describe the reverse characteristics. Figure 3.8 illustrates this model. For a diode which exhibits an unusually large amount of voltage dependent reverse current, or for analyses in which low temperature reverse current is important, a model including a resistive reverse current component may be used, as illustrated in Figure 3.9. If resistor R_R is chosen to match the reverse current at the maximum applied voltage, or to match the worst-case room temperature reverse current from a manufacturer's data sheet, the model will be suitably accurate for worst-case circuit calculations.

Diode Temperature Dependence

The principal diode temperature dependencies that are of interest in modelling a diode for circuit analysis purposes are those predicted by the ideal diode model. These invclve the explicit temperature dependence in the $e^{\frac{qV}{nkT}}$ term of Eqn. 3.1 and the implicit temperature dependence of the $I_s(T)$ term of that equation. The principal temperature dependence of this term may be written explicitly as

$$I_s(T) = C\,T^3\,e^{\frac{-E_{go}}{kT}} \qquad (3.6)$$

where C is a parameter of the diode and E_{go} is the zero temperature energy gap - a constant for the semiconductor material used which has the value 0.782 electron volts for germanium and 1.205 electron volts for silicon. The ideal diode equation may then be written as

$$I = C\,T^3\,e^{\frac{-E_{go}}{kT}}\,(e^{\frac{qV}{nkT}} - 1) \qquad (3.7)$$

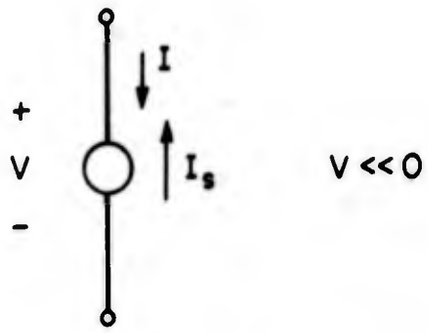

FIG. 3.8 DIODE MODEL FOR NON-CONDUCTING DIODE

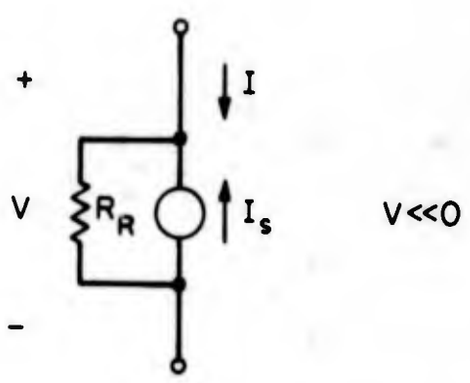

FIG. 3.9 DIODE MODEL FOR NON-CONDUCTING DIODE INCLUDING VOLTAGE DEPENDENT LEAKAGE

Under forward bias conditions, Eqn. 3.7 may be written as

$$I = C\,T^{3}\,e^{\frac{q}{kT}\left(\frac{V}{n} - \frac{E_{go}}{q}\right)} \tag{3.8}$$

The temperature induced drift of current under constant voltage bias may be deduced from the partial derivative of Eqn. 3.8:

$$\frac{\partial I}{\partial T} = \left[\frac{3}{T} - \frac{q}{kT^{2}}\left(\frac{V}{n} - \frac{E_{go}}{q}\right)\right] I. \tag{3.9}$$

Eqn. 3.9 gives the current drift in units of amperes per °C. The fractional or percentage drift per unit change in temperature may be obtained by dividing Eqn. 3.9 by the current:

$$\frac{1}{I}\frac{\partial I}{\partial T} = \frac{3}{T} - \frac{q}{kT^{2}}\left(\frac{V}{n} - \frac{E_{go}}{q}\right) \tag{3.10}$$

Eqn. 3.10 versus normalized voltage $\frac{V}{n}$ is plotted in Figure 3.10 for a silicon diode with temperature as a parameter. The temperature induced current drift is the region of normal diode operating voltages (0.5 to 0.7 volts with n = 1) is appreciable - 5 to 15%/°C depending on the temperature. When a diode is used in a circuit, it is often not biased in a constant voltage condition, but rather the diode "sees" both a Thevenin equivalent voltage source and an incremental source resistance, denoted by R_e. The fractional current drift in this situation can be written as

$$\frac{1}{I}\frac{dI}{dT} = \frac{\left(\frac{1}{I}\frac{\partial I}{\partial T}\right)}{\left(1 + R_e\frac{\partial I}{\partial V}\right)} \tag{3.11}$$

which reduces to Eqn. 3.10 if $R_e = 0$ (constant voltage bias). The expression $\frac{\partial I}{\partial V}$ may be found by partial differentiation of Eqn. 3.8 and is given by

$$\frac{\partial I}{\partial V} = \frac{qI}{kT}. \tag{3.12}$$

This expression is plotted in Figure 3.11 over a range of currents with temperature as a parameter.

Using Eqn. 3.11 and Figures 3.10 and 3.11, the fractional current change per degree temperature change may be found for any silicon diode from a knowledge of the voltage, current and temperature of the diode and the incremental resistance that the diode "sees".

The corresponding temperature induced drift of forward voltage be written in terms of Eqn. 3.11 by

$$\frac{dV}{dT} = -R_e I \left(\frac{1}{I}\frac{dI}{dT}\right). \qquad (3.13)$$

The voltage change in volts per unit change in temperature may be found for arbitrary biasing conditions from Eqn. 3.13.

When the diode is reverse biased, the temperature dependence of the saturation current is due only to the temperature dependence of the $I_s(T)$ term of Eqn. 3.1. Under reverse bias conditions, the ideal diode equation with explicit temperature dependence, Eqn. 3.7 may be written as

$$I = -I_s(T) = -C\,T^3\, e^{\frac{-E_{go}}{kT}} \qquad (3.14)$$

The fractional current change per unit temperature change may be found from Eqn. 3.14 and expressed as

$$\frac{1}{I}\frac{dI}{dT} = \frac{3}{T} - \frac{E_{go}}{kT^2} \qquad (3.15)$$

This equation is plotted versus temperature for a silicon diode in Figure 3.12.

Often the ratio of total change of saturation current relative to a fixed temperature (e.g. 25°C) is of greater interest than the incremental temperature coefficient, which is useful only for small

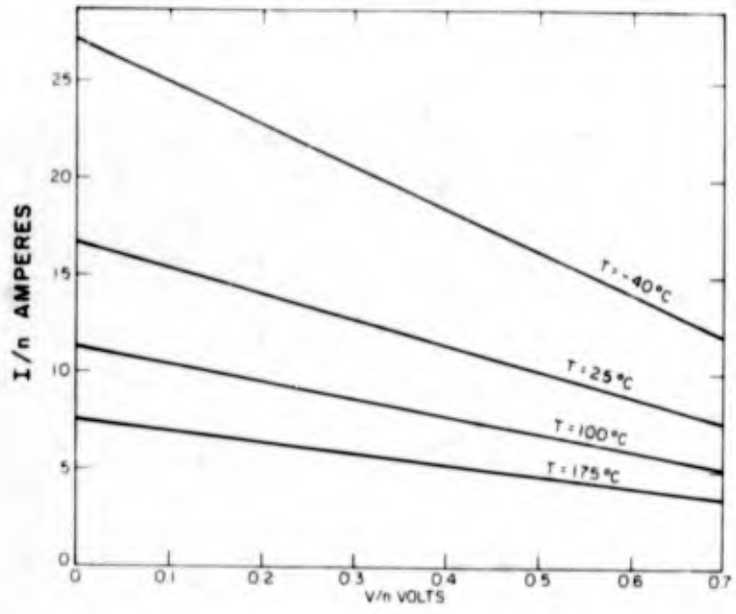

FIG. 3.10 NORMALIZED FORWARD CURRENT-TEMPERATURE COEFFICIENT VERSUS $\frac{V}{N}$ WITH TEMPERATURE AS A PARAMETER

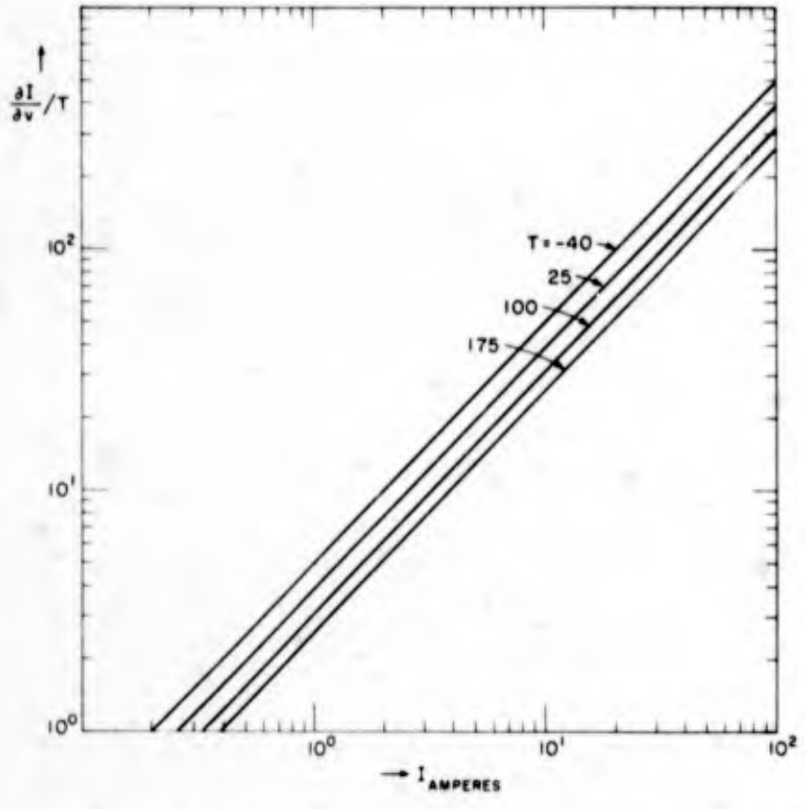

FIG. 3.11 DIODE FORWARD INCREMENTAL CONDUCTANCE VERSUS CURRENT WITH TEMPERATURE AS A PARAMETER

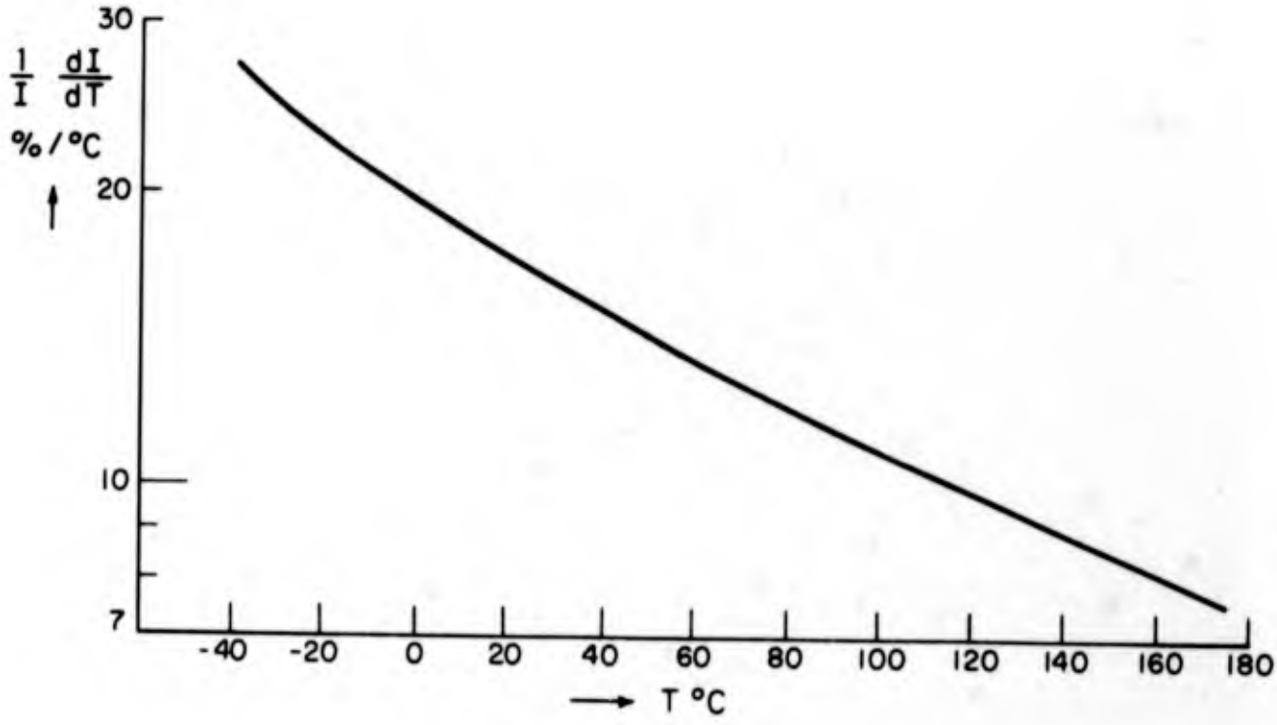

FIGURE 3.12

NORMALIZED REVERSE CURRENT TEMPERATURE COEFFICIENT VERSUS TEMPERATURE

temperature variations. Using Eqn. 3.14, this ratio may be expressed as

$$\frac{I}{I_{ref}} = \left(\frac{T}{T_{ref}}\right)^3 e^{\frac{-E_{go}}{k}\left(\frac{1}{T} - \frac{1}{T_{ref}}\right)}. \qquad (3.15)$$

Where I_{ref} is the saturation current at the reference temperature, T_{ref}. Eqn. 3.15 is plotted in Figure 3.13 versus temperature, using $T_{ref} = 25^{\circ}C$. Since surface effects may dominate in the measurement of reverse current at $T = 25^{\circ}C$, I_{ref} is best inferred at this temperature by measurement of the forward characteristics of the diode at low current levels and extrapolation of the curve to $T = 0$. Alternatively, the I_{ref} current may be measured at an elevated temperature where bulk leakage effects are dominant. Figure 3.14 is a plot of Eqn. 3.15

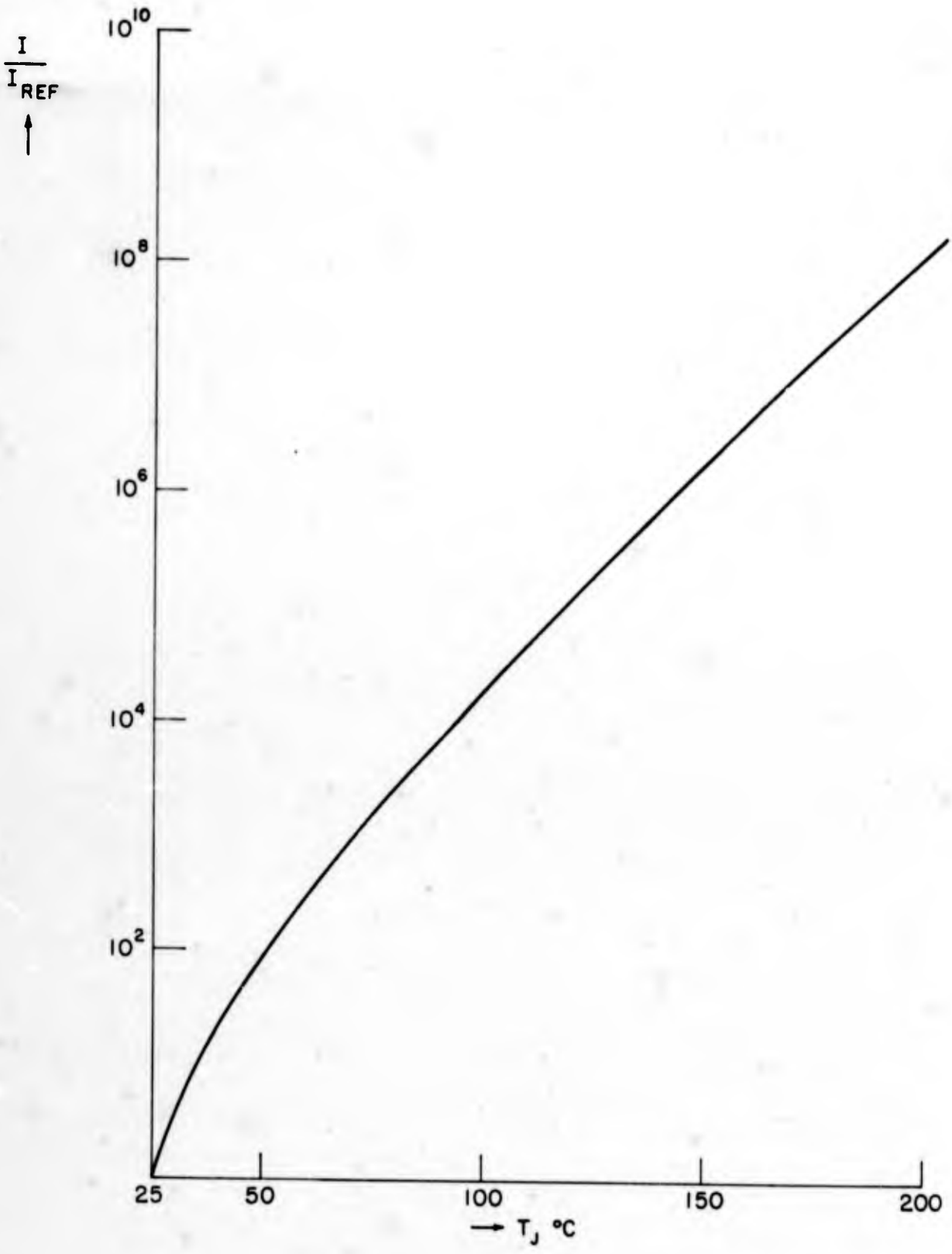

FIG. 3.13 NORMALIZED REVERSE CURRENT CHANGE VERSUS TEMPERATURE RELATIVE TO 25 °C.

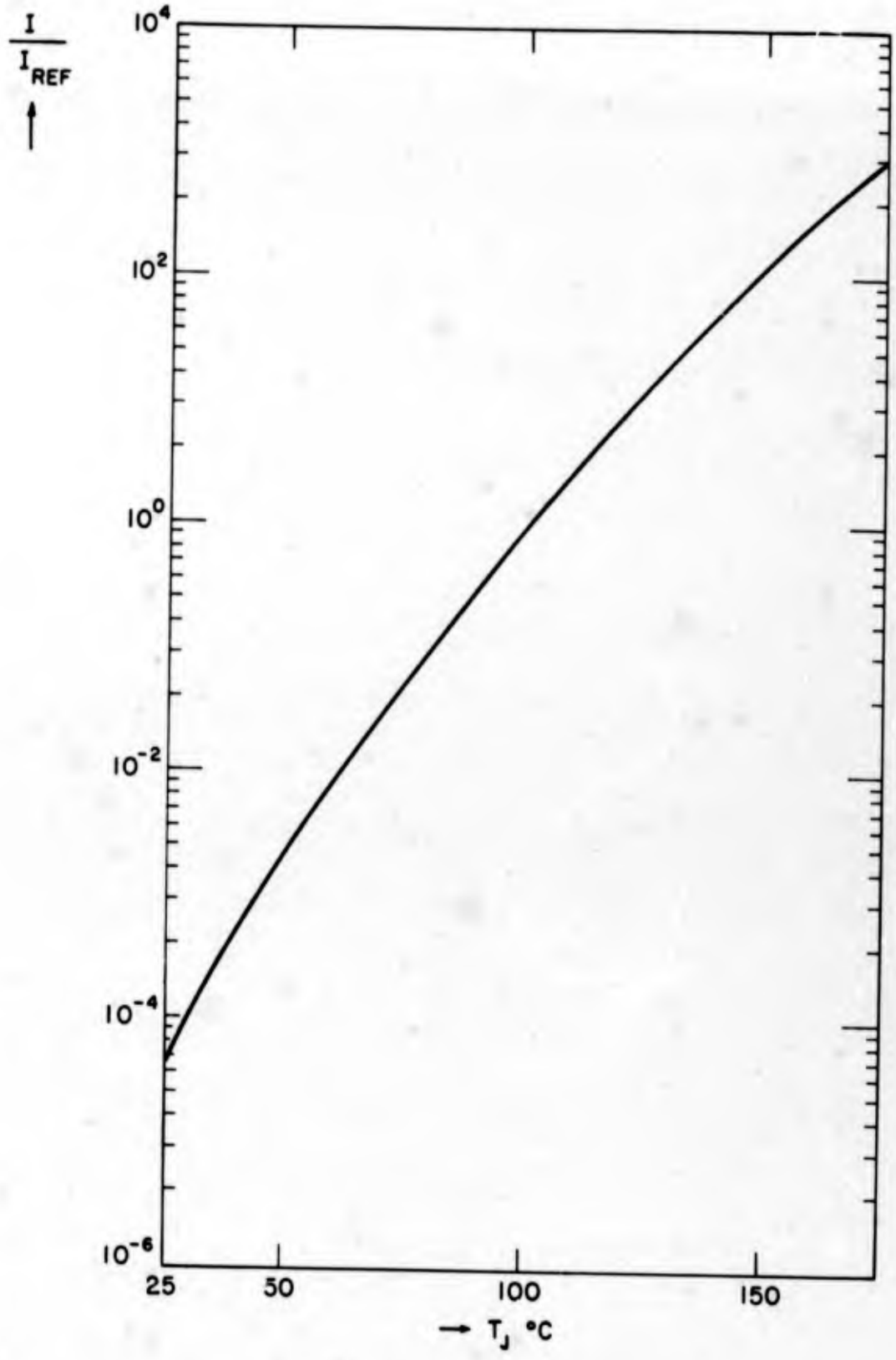

FIG. 3.14 NORMALIZED REVERSE CURRENT CHANGE VERSUS TEMPERATURE RELATIVE TO 100 °C.

versus temperature with $T_{ref} = 100°C$, and may be used with a high temperature I_{ref} to calculate relative reverse current. Either curve shows that when the junction temperature varies from 25 to 150°C, the leakage current due to bulk effects increases by a factor greater than 10^6!

Dynamic Characteristics

The previous discussion has provided a characterization of semiconductor diodes under conditions where the terminal variables of current and voltage associated with the device are time invariant or change slowly with time. When this situation does not hold true, several time dependent effects become evident. For power type circuitry, the most significant of these effects is the reverse recovery phenomena which is encountered when a diode is rapidly switched from the conducting to non-conducting states. In circuits which employ a diode in this manner, the current through the diode is constrained by the external circuitry until the diode becomes non-conducting. Figure 3.15 shows a Thevenin equivalent for this type of circuit. When switch S is in the F position, a current I_F flows in the diode in the steady state, given by

$$I = I_F = \frac{V_F - V}{R_F}, \quad V_F > 0.$$

If $V_F \gg V$,

$$I_F \simeq \frac{V_F}{R_F}, \quad V_F \gg V. \tag{3.16}$$

With S in the R position, the steady-state reverse current that flows is the diode saturation current discussed in the previous sections. However, the diode current does not assume the steady-state value immediately after switch S is thrown from the upper to lower position.

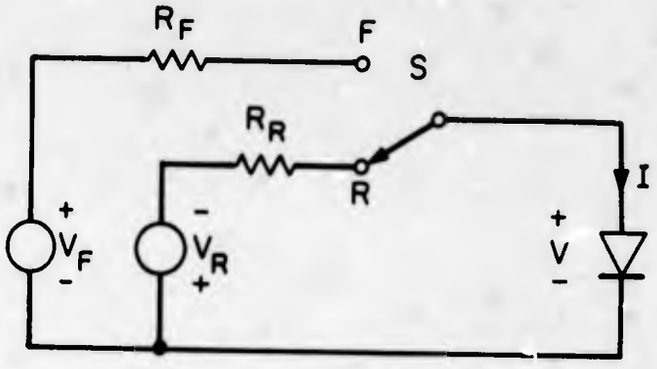

FIGURE 3.15

DIODE SWITCHING TRANSIENT CIRCUIT

This behavior may be understood by examination of a crude dynamic model of the diode as a device whose current is charge controlled rather than voltage controlled as described by the ideal diode equation, (3.1). When the physics of semiconductor diode operations are examined, the diode current is found to be dependent on an amount of charge stored within the device. In the steady-state, the functional relationship between charge and voltage is identical in form to the current/voltage relation of Eqn. 3.1. Thus, the diode current, which is actually charge controlled, may appear to be voltage controlled in the steady-state. When dynamics are examined, the charge-current relations must be considered in greater detail. For a crude model, we will approximate the diode as a parallel combination of a charge storage device and a charge leakage device, as illustrated in Figure 3.16. The terminal variables are input current i and stored charge q. The input current flows into either the charge storage device, where the accumulated charge is governed by the relation

$$q = \int_{-\infty}^{t} i_s dt \qquad (3.17)$$

or the current flows into the charge leakage device, where the rate of charge leakage (current) is expressed as

$$i_d = \frac{q}{\tau_d} \qquad (3.18)$$

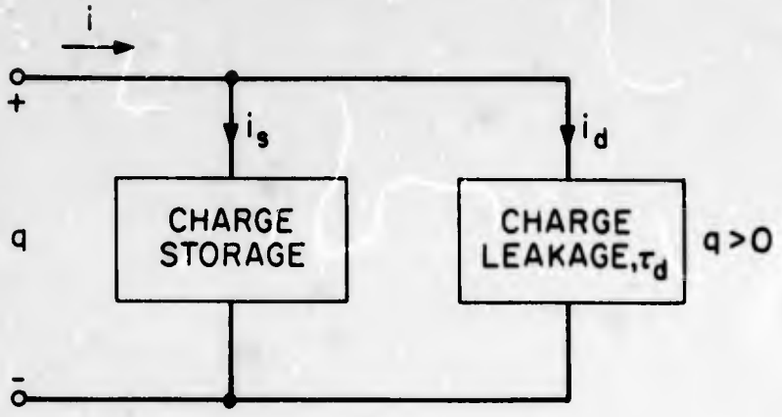

FIGURE 3.16

CHARGE CONTROL MODEL OF A DIODE

where τ_d is a parameter of the charge leakage device. The total current-charge relation of the diode may be found by differentiating Eqn. 3.17 and combining with Eqn. 3.18 to yield

$$i = \frac{q}{\tau_d} + \frac{dq}{dt}. \qquad \text{(conducting state)} \qquad (3.19)$$

Eqn. 3.19 forms the basic charge control equation of a conducting diode. In the non-conducting state, only the saturation current can flow and

$$i = -I_s \qquad \text{(non-conducting state)} \qquad (3.20)$$

Inasmuch as the diode reverse saturation current is much smaller than the forward currents normally encountered, the demarkation between conducting and non-conducting diode states is taken to be the point where the stored charge is zero. Thus, Eqn. 3.19 describes diode behavior for $q > 0$ and Eqn. 3.20 for $q \leq 0$.

Returning now to the problem posed in Figure 3.15, assume that switch S has been left in the F position for a sufficient length of time

to establish steady-state conditions; i.e., Eqn. 3.16 holds, the diode is in the conducting state, and charge control Eqn. 3.19 is valid. Since the current i is unchanging, the time derivative in Eqn. 3.19 is zero and Eqns. 3.19 and 3.16 may be solved to yield

$$q = I_F \tau_d = \frac{V_F}{R_F} \tau_d. \tag{3.21}$$

Assume now that at t = 0, S is moved instantaneously to the R position. Since q is greater than zero, the diode remains in its conducting state and the voltage across it remains small. From Figure 3.16,

$$I = -I_R \simeq -\frac{V_R}{R_R}, \qquad V_R \gg V, \; t > 0. \tag{3.22}$$

Now Eqns. 3.19 and 3.22 may be solved for the ensuing transient with Eqn. 3.21 supplying the initial condition at t = 0. Solving these yields

$$q(t) = \tau_d\left[I_F - (I_F + I_R)\left(1 - e^{-\frac{t}{\tau_d}}\right)\right], \quad q > 0. \tag{3.23}$$

Eqn. 3.23 is plotted versus time in Figure 3.17. When the charge q reaches zero, the diode enters the non-conducting state. A smaller value of I_F, a larger value of I_R or a diode with a smaller value of τ_d will cause faster diode reverse recovery. The reverse recovery time may be calculated by setting q in Eqn. 3.23 to zero and solving for the time, $t = t_{RR}$, the reverse recovery time of the diode. Performing this calculation results in

$$t_{RR} = \tau_d \ln\left(1 + \frac{I_F}{I_R}\right). \tag{3.24}$$

Figure 3.18 displays the normalized reverse recovery time versus $\frac{I_F}{I_R}$.

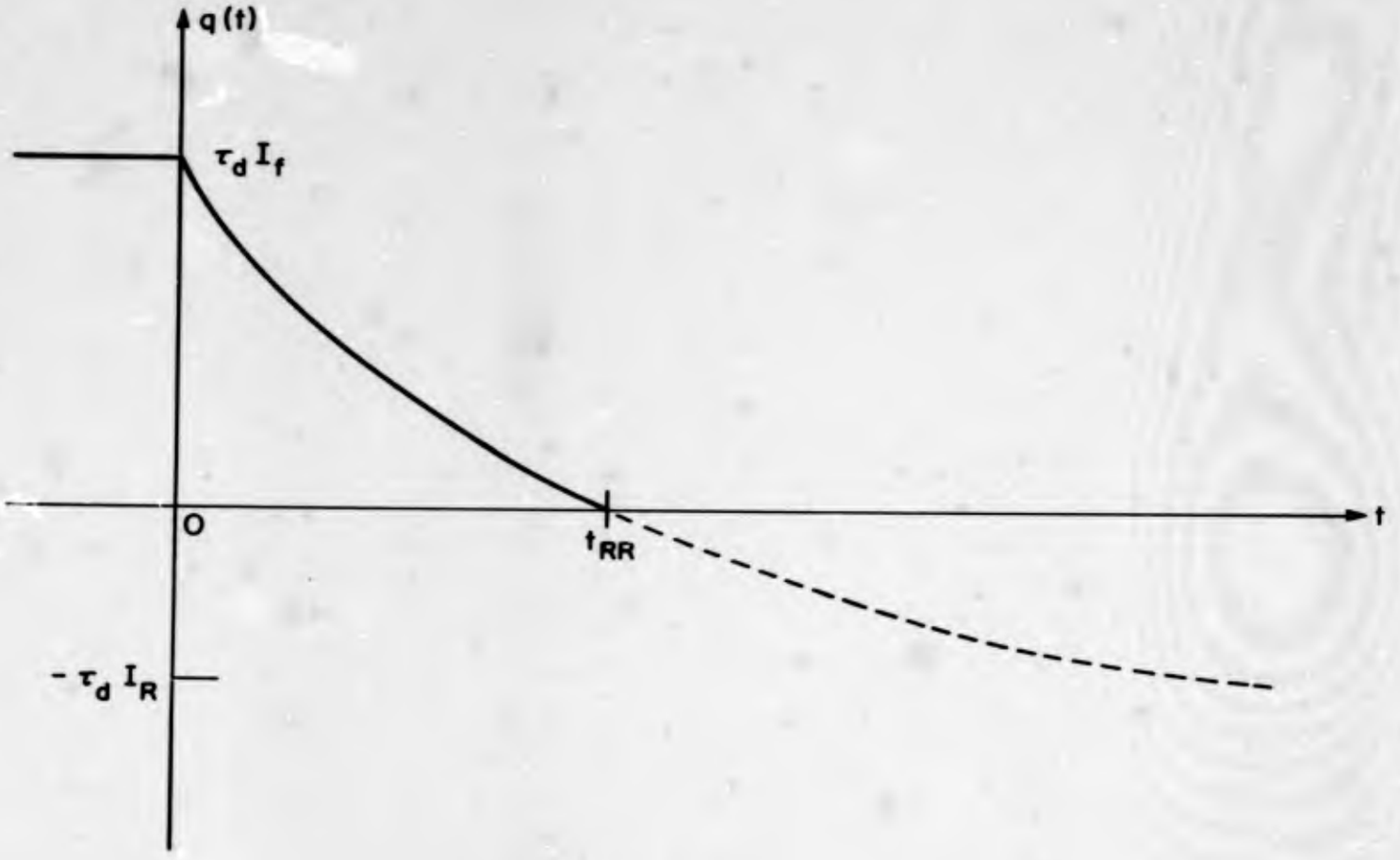

FIGURE 3.17

STORED CHARGE VERSUS TIME DURING DIODE TURN-OFF

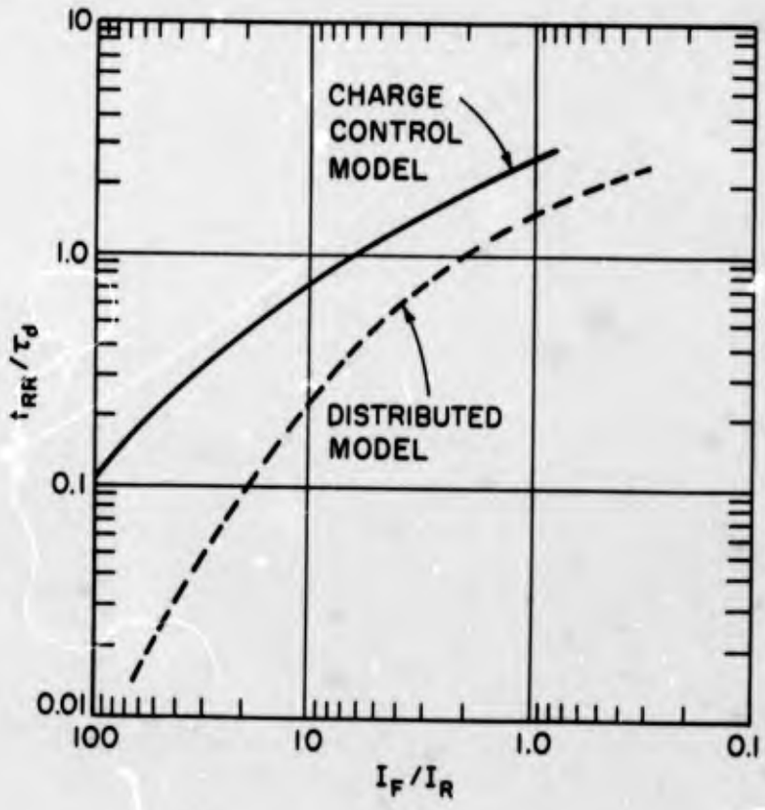

FIGURE 3.18

NORMALIZED DIODE TURN-OFF TIME VERSUS $\frac{I_R}{I_F}$

It should be recognized that the model used for calculating Eqn. 3.24 and Figure 3.18 is a lump approximation to a process which is really continuously distributed through the volume of the diode. Consequently, the results obtained here are only approximations to actual performance. In addition, the junction voltage reverses before the stored charge decays completely to zero, hence Figure 3.18 will yield conservative (overly long) estimates for the diode recovery time. A more accurate analysis, based on the partial differential equations describing the actual distributed behavior of a diode has been performed,* and the results are presented along with the lumped model results in Figure 3.18. This curve may be used to compute recovery time in a circuit if the charge control parameter τ_d is determined for the diode of interest, either by direct measurement or by inference from the manufacturer's data sheet. Figure 3.19 is an oscillogram of the waveforms encountered in a reverse recovery test circuit similar in action to the circuit of Figure 3.16. In this circuit $V_F = V_R = 15$ volts and $R_F = R_R = 25\ \Omega$, hence, $I_F = I_R \simeq .6$ amperes. The top waveform shows the diode voltage and the bottom, diode current. The recovery time, defined as the point at which the diode voltage begins to increase (this is a time less than that for q = 0), is 2.2 microsecond.

The reverse recovery time of a diode constitutes a significant circuit limitation; during the diode reverse recovery interval of a practical circuit, the device which commutates the diode must often handle the sum of both the forward current I_F and the reverse current I_R. In addition, the reverse recovery current is not usually resistance limited but rather depends on second order effects such as transistor β limitations and switching times, semiconductor bulk resistances and stray inductance to limit the current. Consequently, during the reverse recovery interval, large and uncontrolled spikes of current may flow through both the diode and the commutating device, which is typically a solid state switch. The switch current rating must be adequate to safely handle the "spike".

If the reverse recovery "spike" current is appreciable, significant

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* Bibliography III, Reference 157.

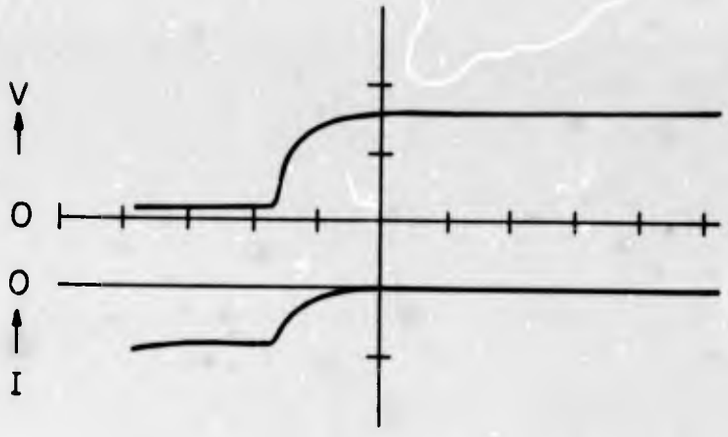


FIGURE 3.19

MEASURED DIODE REVERSE RECOVERY TRANSIENT
TOP TRACE - VOLTAGE. BOTTOM TRACE - CURRENT

power dissipation will occur in a switching circuit as the switching frequency is increased. Figure 3.20 shows an example of a power switching circuit where this can occur. When the power switch first closes, the recovery current I_R flows through both the diode and the power switch. This current, across the supply voltage V_{cc} represents power which is dissipated in the diode and power switch.

If V_{cc} = 30 volts, I_F = 25 amperes, I_R = 50 amperes, the diode recovers in 1.0 microsecond and the switch is turned on every 50 microsecond (20 kHz switching frequency), the power dissipated due to reverse recovery will be

$$P_d = V_{cc} \times I_R \times \frac{t_{recovery}}{t_{period}}$$

$$P_d = 30 \times 50 \times \frac{1.0}{50.} = 30 \text{ watts.}$$

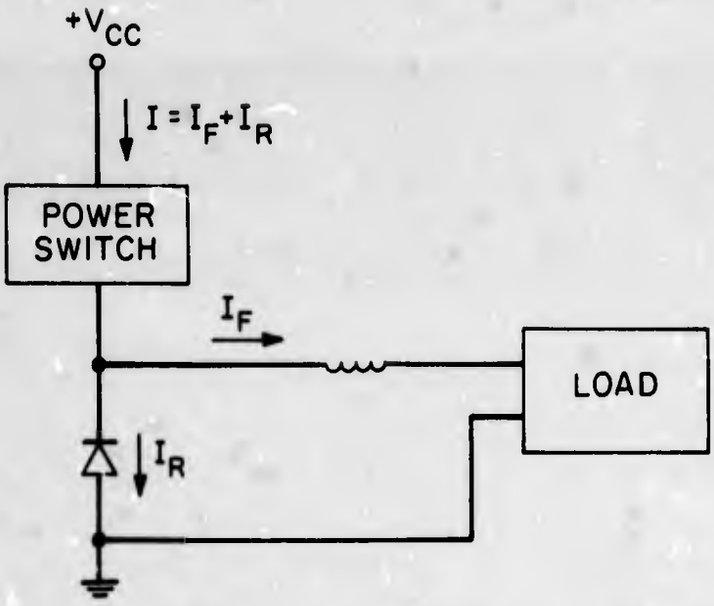


FIG. 3.20 POWER OUTPUT STAGE DURING THE SWITCH TURN-ON INTERVAL

For this example, a faster diode (say $t_{recovery}$ = 0.1 microsecond, yielding P_d = 3.0 watts) should be used.

Two other aspects of dynamic behavior which may be of significance in diode operation will be mentioned here. A complete treatment of these effects may be found in the references.

When a forward current near the diode rating is suddenly applied to a diode that had been non-conducting, an excess forward voltage may be observed across the diode which decays to the steady-state value. The excess voltage across the diode may be as large as five volts, causing additional power dissipation in the diode. If the diode is used to clamp the voltage across some other element (e.g. transistor or thyristor), this excess voltage must be taken into account in selecting the voltage rating of the element.

The second additional effect of significance concerns the junction capacitance of a reverse biased diode. When a semiconductor diode is reverse biased, charge is stored in the region of the junction which

can be modeled as a non-linear capacitance. The stored charge in the junction area can be expressed as

$$q_j = f(V), \tag{3.25}$$

the charge is a function of applied voltage and the incremental capacitance due to this charge storage can be found from

$$C = -\frac{dq_j}{dV}. \tag{3.26}$$

For most diodes, the expression for incremental capacity is of the form

$$C = \frac{K}{(\Psi_o - V)^n}, \qquad V < 0 \tag{3.27}$$

where Ψ_o and n are constants which depend on the construction details of the diode. Ψ_o may lie between 0.2 and 1.0 volt and often can be neglected when compared to V. The parameter n lies between 1/3 and 1/2. The charge needed to change the voltage across this diode capacitance must be taken into account when switching from the conducting to non-conducting state and vice-versa.

Diode Limitations

1) Voltage. The principal diode voltage limitation is that of breakdown of the semiconductor junction under large reverse bias conditions. This breakdown is due to the "avalanche multiplication" effect which causes a rapid increase in reverse current for a small increase in reverse voltage. A diode model which illustrates the avalanche effect is shown in Figure 3.21. The voltage V applied to the diode is negative, hence in the diode portion of the model, only the saturation current, I_s flows. Due to the multiplication effect, the diode terminal current is greater than I_s by a voltage dependent factor, M(V), so

$$I = M(V)\, I_s. \tag{3.28}$$

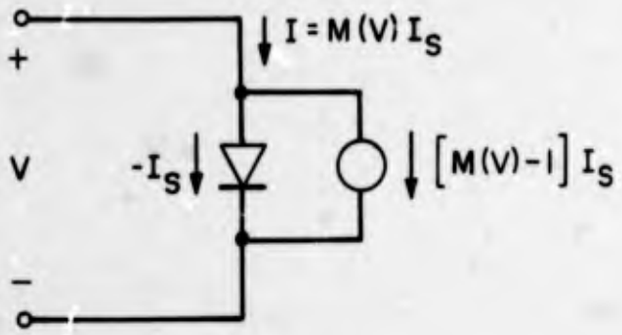


FIG.3.21 DIODE MODEL ILLUSTRATING AVALANCHE MULTIPLICATION

This may be modelled as a current controlled current source in parallel with the diode whose current is $[M(V) - 1]\, I_s$, so the sum of the diode and current source currents are given by Eqn. 3.28. The voltage dependent factor has the form

$$M(V) = \frac{1}{1 - \left(\frac{-V}{V_A}\right)^n}, \qquad V < 0 \qquad (3.29)$$

where n is a parameter with range $1 < n < 4$ and V_A is the avalanche breakdown voltage; the voltage at which M(V) and, hence, I would become infinite. Figure 3.22 is a plot of M(V) versus $\frac{V}{V_A}$ for $n = 1$ and $n = 4$. Due to the sharpness of this curve as V approaches V_A, the reverse breakdown of a diode is often modelled as a threshold breakdown at $V = V_A$, as illustrated in the volt-ampere plot of Figure 3.23.

2) Current. Unlike the case of avalanche voltage breakdown, there is no abrupt mechanism which limits diode forward current. The

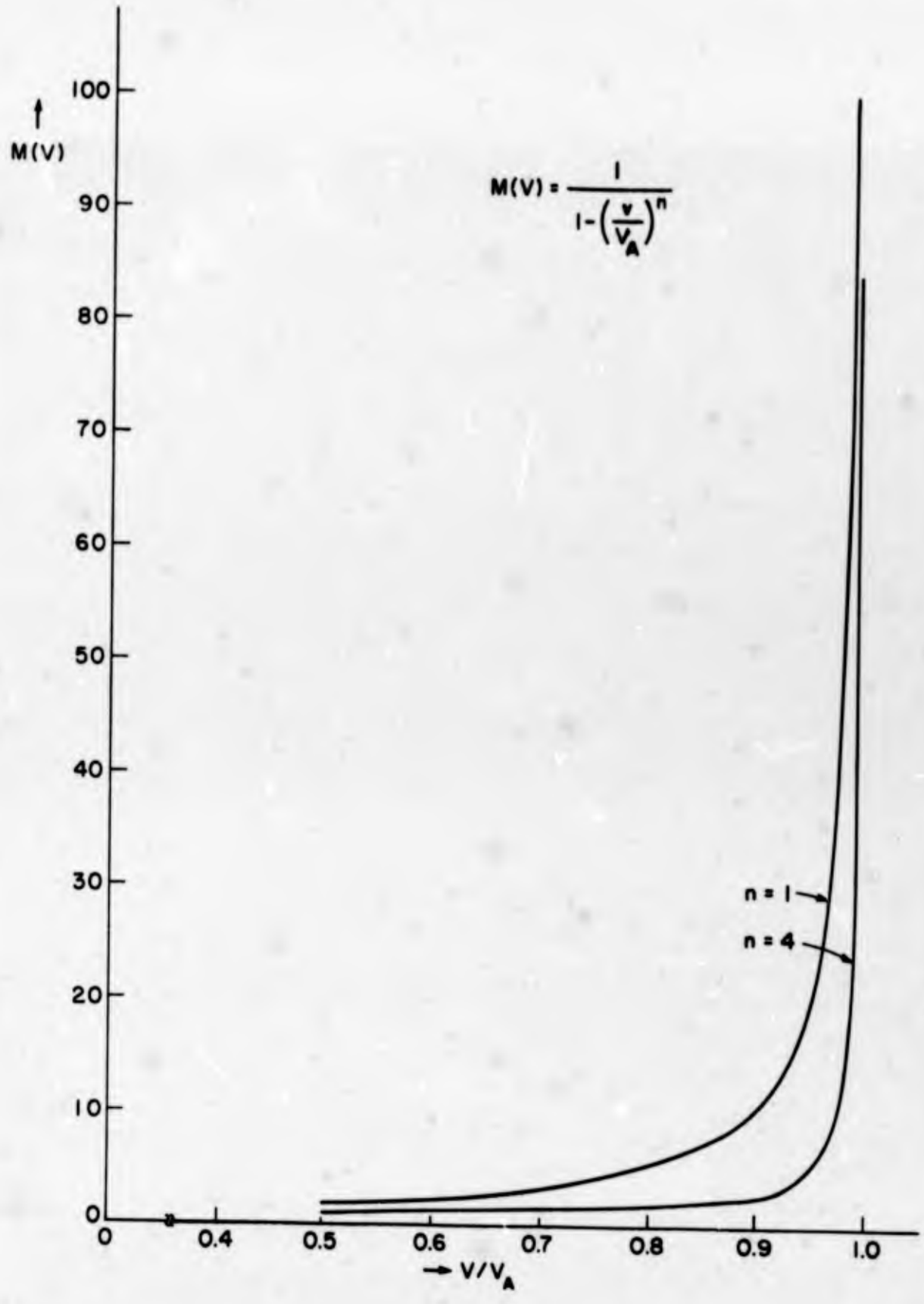


FIG. 3.22 AVALANCHE MULTIPLICATION FACTOR VERSUS NORMALIZED VOLTAGE.

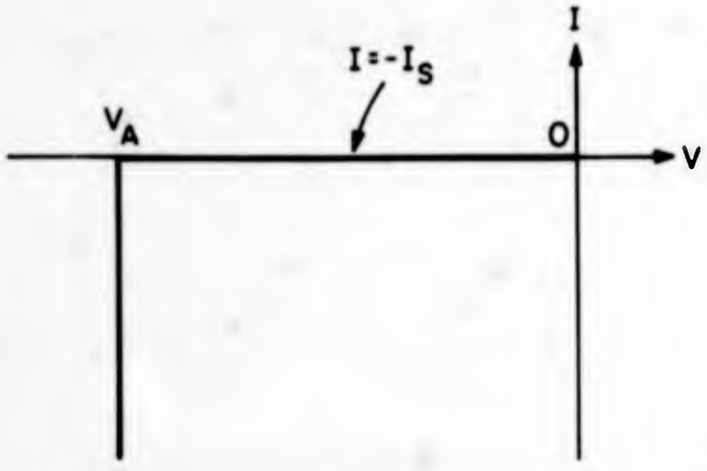


FIG. 3.23 THRESHOLD BREAKDOWN V-I PLOT OF A DIODE

practical limitation is thermal - the static resistive drops previously described may cause an unacceptably large power loss or, at some current the leadwires, metalization, or the diode chip, itself, may melt or fuse. The diode average and peak current ratings encountered in the data sheet are based on these considerations.

3) Temperature. The temperature of the semiconductor junction is a fundamental limitation on diode operation. As we have seen, at high junction temperatures the diode leakage current rapidly increases, rendering the diode temporarily useless for blocking reverse currents. The solders and bonding agents used in constructing the device soften and weaken and the reliability of the diode chip is permanently degraded.

In calculating temperature rises, it is necessary to know the power dissipated in the device. The total power dissipation as a function of time may be found by summing the power dissipations due to the following factors discussed in this section:

a) Forward static dissipation calculated as a succession of steady states.

b) Reverse biased leakage.

c) Reverse recovery transient (turn-off).

d) Forward recovery transient (turn-on).

For a single diode mounted on a heat sink and convection cooled, the junction temperature may be calculated from a static thermal model:

$$T_j = (\theta_{jc} + \theta_{cs} + \theta_{sa})P_d + T_a \qquad (3.30)$$

where T_j is the junction temperature, which is constrained to a maximum value for each device type by the manufacturer. For silicon devices, this maximum lies between 175°C and 200°C. P_d is the power dissipated by the diode, T_a is the ambient temperature of the surrounding air and the θ's are thermal resistances of the physical package. θ_{jc} is the thermal resistance of the junction to the diode case and is specified by the device manufacturer. θ_{cs} is the case to heat sink thermal resistance and is dependent on the case type and how it is mounted to the heat sink. For a specified mounting configuration, the manufacturer's data sheet specifies this parameter. The heat sink to ambient thermal resistance, θ_{sa} may be found from heat sink data sheets or experimentally measured by dissipating a known power on the heat sink and measuring its temperature rise above ambient. A thermal model using electrical circuit analysis techniques may be made for Eqn. 3.30 by identifying θ with a thermal resistance analogous to circuit resistance T with a temperature rise analogous to voltage rise and P_d with a power flow analogous to current flow; this model is illustrated in Figure 3.24. It should be noted that the quantity $T_R = P_d(\theta_{jc} + \theta_{cs} + \theta_{sa})$ is the junction temperature rise above ambient. While this figure is often quoted and calculated, the fundamental limitation is the actual junction temperature, and the maximum ambient temperature must be used in this calculation.

If more than one device is coupled to a common heat sink, then a more elaborate thermal circuit model may be used to aid calculations. Figure 3.25 illustrates a model in which two devices are

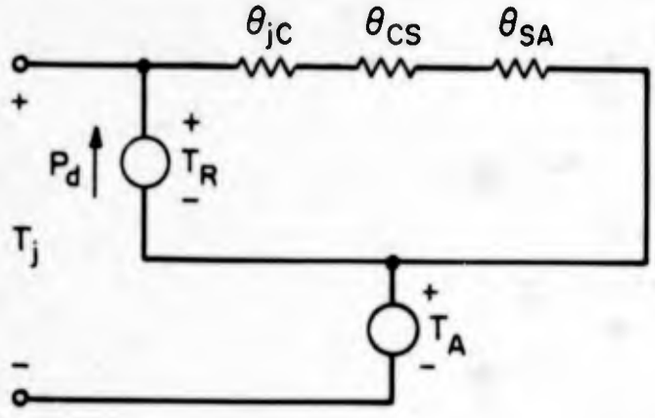


FIG. 3.24 STATIC THERMAL CIRCUIT MODEL FOR SINGLE CONVECTION COOLED DIODE

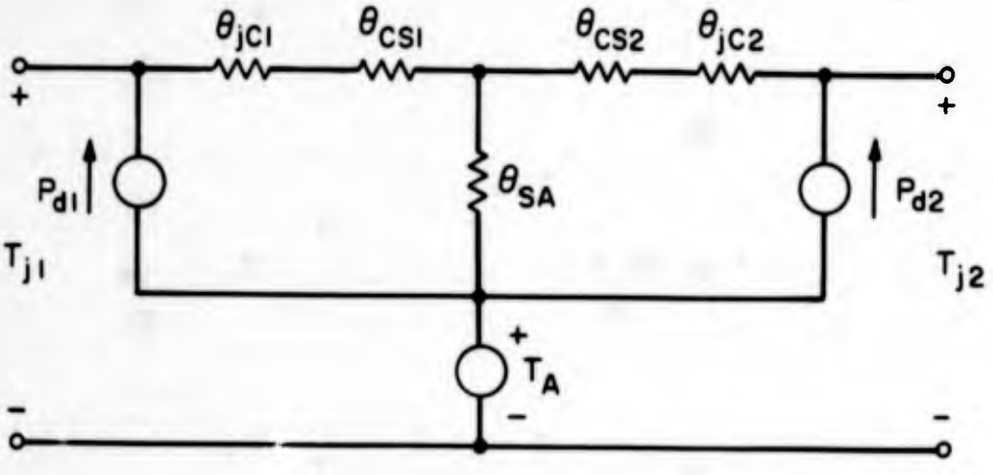


FIG. 3.25 TWO DEVICE CONVECTION COOLED STATIC THERMAL CIRCUIT MODEL

mounted on a common heat sink. The thermal resistance between the mounting points of the devices on the heat sink has been neglected. When the parameters of the model are known, simple circuit calculations can be used to find the junction temperature.

It is important to recognize that this "lumped" thermal model is really an approximation of a distributed thermal system. Therefore, it is necessary to verify the validity of any thermal model by performing measurements on the system modelled which will confirm the assumptions made. Thermal measurements may easily be made by setting up a known pattern of heat dissipation in the elements and measuring temperature rises at accessible key points (e.g. the device cases). The theoretical temperature rises at these points may be calculated from the model. The measured and calculated values should be in approximate agreement and, under no circumstances, should the measured temperatures exceed the calculated ones.

In many circuit applications, the power dissipated in the semiconductors is time varying. The thermal capacity of the chip, case and heat sink delay the attainment of the thermal temperature rises calculated by considering only thermal resistance. If the variations are slow compared to typical thermal time constants, i.e., if the variations occur over several minutes, the steady-state model may be applied on an instantaneous basis with adequate (and conservative) results. If the power variations are fast compared to the thermal time constants, i.e., less than one millisecond, the power variations are completely averaged by thermal capacity - principally that of the semiconductor chip, and only the steady-state (average) power dissipation need be considered in calculating temperature rise. If the variations in power dissipation take place in times between these two extremes, some allowance must be made for the consequent time varying junction temperature. Several approximate procedures have been developed which allow the calculations of transient temperature rise and one of these will be described here. Using this method, a lumped linear model consisting of thermal resistances and thermal capacitances is assumed. The thermal circuit model for a single device is drawn in Figure 3.26. In this model, the static parameters correspond to those of Figure 3.24. C_{jT} represents the thermal capacity of the semiconductor chip. C_c represents the thermal capacity of the component case and, for dynamic analysis, is assumed to be

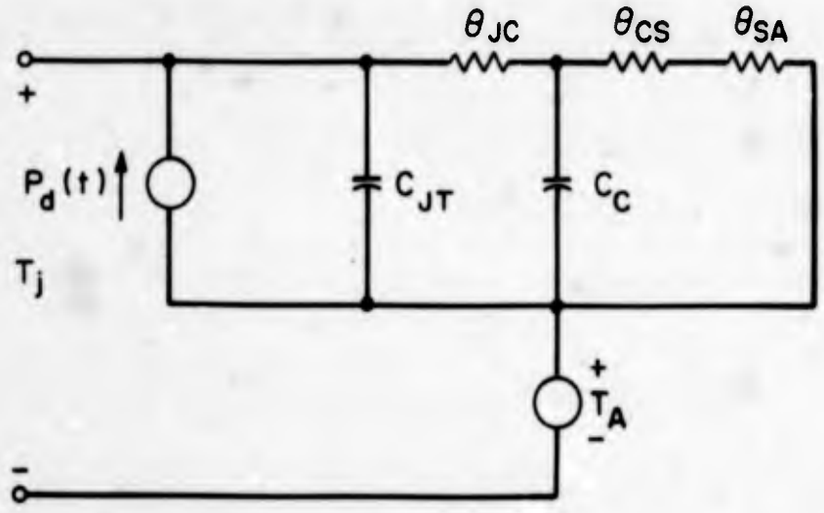
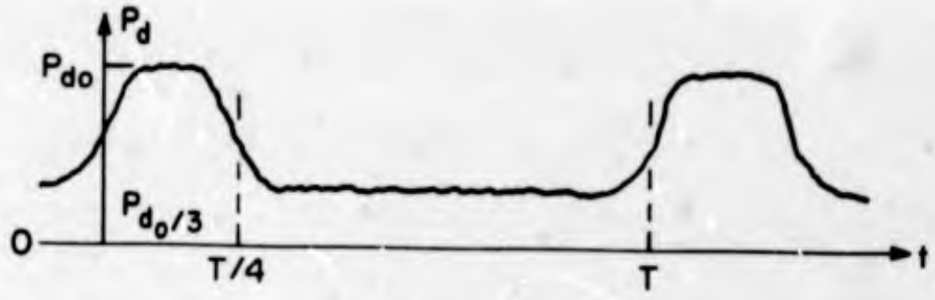


FIG. 3.26 DYNAMIC THERMAL CIRCUIT MODEL FOR A SINGLE DEVICE

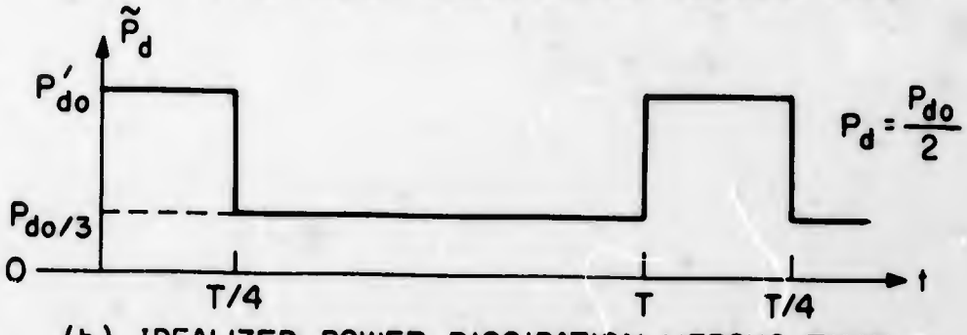
infinite. This limits the validity of this model to cycles of power whose period is small when compared to the case thermal time constant. For most devices, this limitation occurs in the 0.1 to 1.0 second range. For longer times, steady-state conditions are generally assumed. C_{jT} is usually specified implicitly in the thermal time constant of the device, $\tau_T = \theta_{jc} C_{jT}$, and is about 1.0 millisecond.

The analysis proceeds as follows: The instantaneous power dissipated in the device is plotted versus time. A succession of square pulse approximations having equal area to the original curve is constructed. No square pulse need be shorter than $0.1\ \tau_T$. Satisfactory results may be obtained with relatively crude approximations. This process is illustrated in Figure 3.27 for a specific example. The square pulse power approximation, $\tilde{P}_d$ is resolved into two components, the steady-state (dc) value, which is the average power,

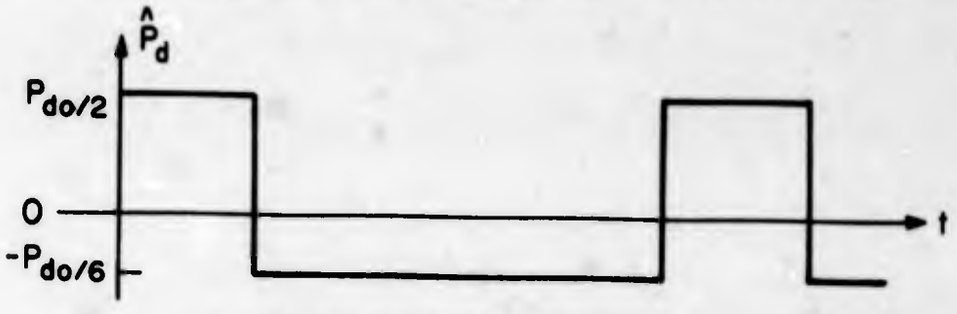
$$\bar{P}_d \triangleq \frac{1}{T} \int_0^T P_d(t)dt \qquad (3.31)$$



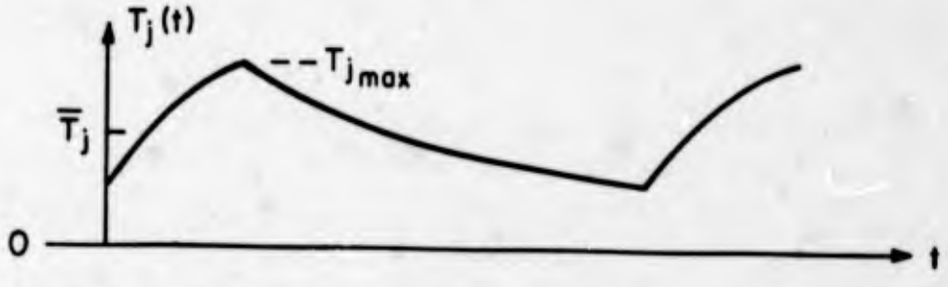
(a) ACTUAL POWER DISSIPATION VERSUS TIME



(b) IDEALIZED POWER DISSIPATION VERSUS TIME



(c) A.C. COMPONENT OF POWER



(d) JUNCTION TEMPERATURE VERSUS TIME

FIG. 3.27 CALCULATION OF MAXIMUM JUNCTION TEMPERATURE

and the ac component,

$$\hat{P}_d \triangleq \tilde{P}_d(t) - \bar{P}_d \qquad (3.32)$$

Now the steady-state junction temperature may be calculated using the model of Figure 3.24. For our example, assume

$$\theta_{jc} = 0.5^\circ C/watt$$

$$\theta_{cs} + \theta_{sa} = 1.0^\circ C/watt$$

$$\bar{P}_d = 20 \text{ watts}$$

$$T_A = 70^\circ C$$

$$\frac{T}{\tau} = 1.0.$$

Then

$$\bar{T}_j = T_A + \bar{P}_d (\theta_{jc} + \theta_{cs} + \theta_{sa}) = 100^\circ C. \qquad (3.32)$$

Using $\hat{P}_d$ and the dynamic thermal model, Figure 3.26, the variations in junction temperature may be calculated by analysis of the circuit drawn in Figure 3.28. $\tilde{T}_R$ denotes the incremental temperature variations about the steady-state value,

$$\tilde{T}_R = T_R - \bar{T}_R. \qquad (3.33)$$

Using the waveform of Figure 3.27c, $T_j(t)$ can be calculated and the results of this calculation are graphed in Figure 3.27d. The analysis shows that the peak instantaneous junction temperature, which occurs at $t = \frac{T}{4}$, has the value

$$T_{j(max)} = 111^\circ C.$$

This must always be less than the maximum permissible junction temperature.

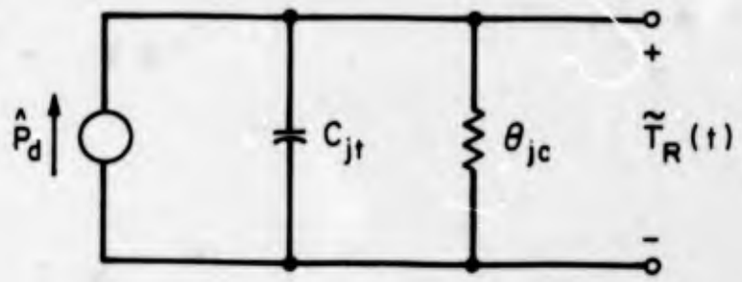


FIGURE 3.28

INCREMENTAL THERMAL CIRCUIT MODEL

3.2 TRANSISTORS

Static Characteristics

Many features of the static behavior of a transistor may be understood in terms of its characteristic curves. Since the transistor is a three terminal device, two families of curves are sufficient, ignoring temperature variations, to statically characterize it. We have selected the common emitter input and output characteristics as appropriate curves to study because these are easy to generate experimentally and are the curves most commonly shown in the literature. Also, for the bulk of transistor applications, these are the curves most appropriate to static circuit analysis. The schematic symbol of a transistor is shown in Figure 3.29. The voltages and currents that are defined are those appropriate to the common emitter configuration. The two families of curves that will be examined are the output characteristics $-I_C$ versus V_{CE} with I_B as a parameter and the input characteristics, I_B versus V_{BE} with V_{CE} as a parameter. The simplest useful large signal characterization of the transistor is the Ebers-Moll model, illustrated in Figure 3.30 for an NPN transistor.

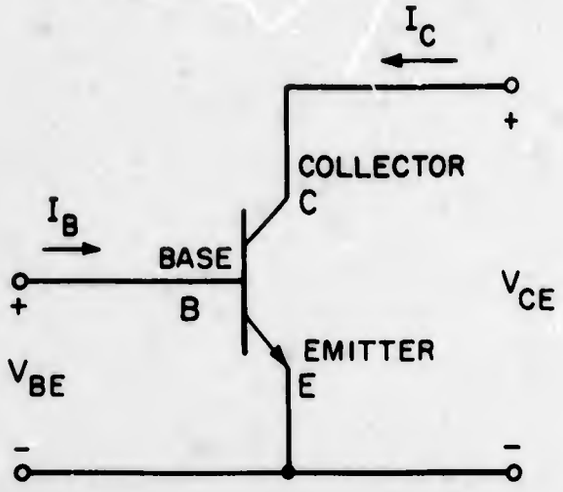


FIG.3.29 SCHEMATIC SYMBOL OF A TRANSISTOR

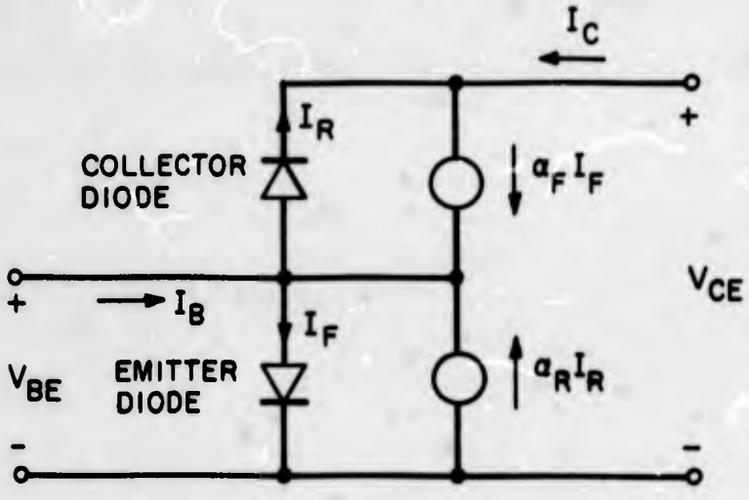


FIG.3.30 EBERS-MOLL TRANSISTOR MODEL

This model illustrates that the transistor can be thought of as a pair of back-to-back diodes with interaction between them (as modelled by the current sources) due to the close proximity of the two junctions. Any of the diode models discussed in Section 3.1 may be used here to obtain a more or less detailed description of the behavior of the transistor, depending on the accuracy of the diode model used. For example, if the "perfect" diode model illustrated in Figure 3.2 is selected, the transistor model of Figure 3.30 may be employed to plot the input and output common emitter curves. To do this, several regions of operations will be examined. Assume $V_{CE} > 0$ and $I_B > 0$. In this region, known as the forward active region, the collector diode is non-conducting, hence $I_R = 0$ and the emitter diode is conducting, so $V_{BE} = 0$. Since $I_R = 0$,

$$I_F = I_B + I_C$$

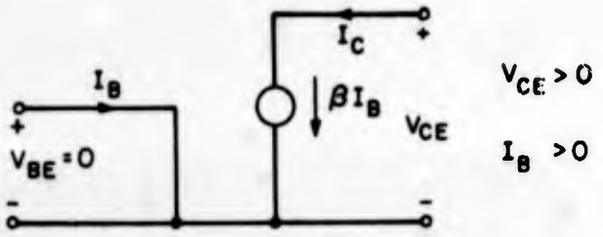
and

$$I_C = \alpha_F I_F = \alpha_F I_B + \alpha_F I_C$$

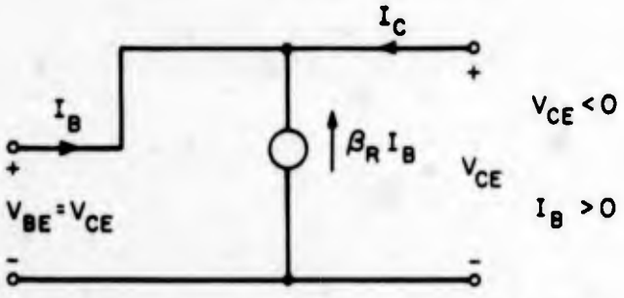
so

$$\frac{I_C}{I_B} = \frac{\alpha_F}{1-\alpha_F} \equiv \beta_F. \qquad (3.34)$$

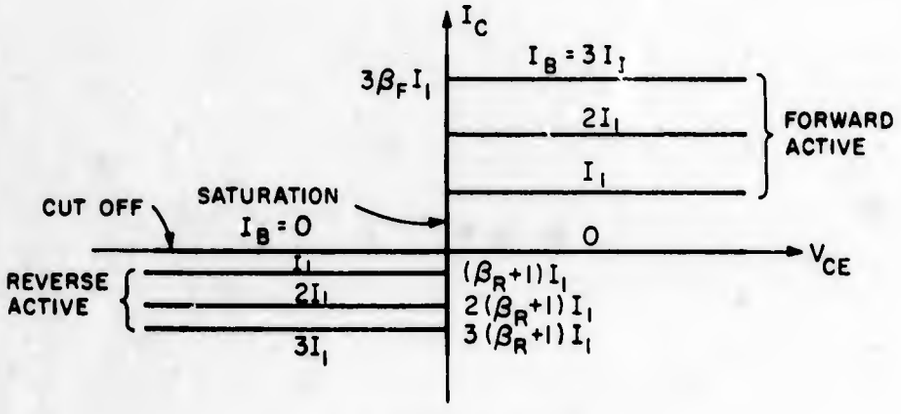
Eqn. 3.34 defines the "β" or current gain of the transistor in the forward active region. Since the collector current is independent of collector voltage and varies directly with base current, a transistor operating in this region may be thought of as a current controlled current source and modelled as in Figure 3.31.



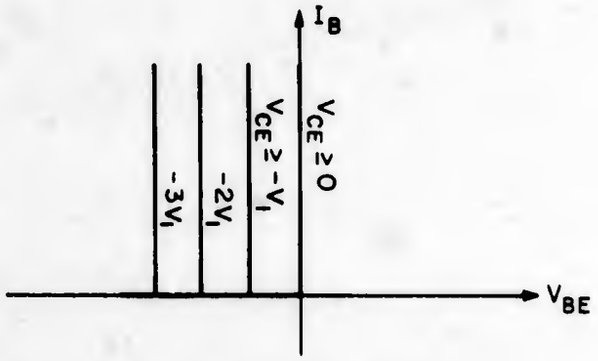
a CURRENT CONTROLLED CURRENT SOURCE MODEL OF A TRANSISTOR



b. CURRENT SOURCE MODEL OF A TRANSISTOR IN THE REVERSE-ACTIVE REGION.



c OUTPUT CURVES



d INPUT CURVES

FIG. 3.31 MODEL AND CHARACTERISTICS OF A PERFECT TRANSISTOR.

If $V_{CE} < 0$, then the emitter diode in the model is non-conducting; therefore, $I_F = 0$, and the collector diode is conducting. Now

$$I_R = \alpha_R I_R + I_B = -I_C$$

or

$$\frac{-I_C}{I_B} = \frac{1}{1-\alpha_R} . \qquad (3.35)$$

The form of Eqn. 3.35 is similar to (3.34). The quantity

$$\beta_R = \frac{\alpha_R}{1-\alpha_R} \qquad (3.36)$$

is defined as the <u>reverse β</u> of the transistor - this is the current gain of the transistor when the collector and emitter leads are interchanged. Eqn. 3.35 may be rewritten, using Eqn. 3.36 as

$$-\frac{I_C}{I_B} = \beta_R + 1. \qquad (3.37)$$

The model for the transistor operating in the reverse direction is shown in Figure 3.31b. The models of Figure 3.31 may now be used to construct the characteristic family of curves for this idealized transistor. For junction transistors, $0 < \alpha < 1$ and generally α_F is near 1, making β_F large, and α_R is somewhat smaller than α_F, making β_R small compared to β_F.

A set of output and input characteristic curves reflecting these considerations are shown in Figure 3.31c and d. Two additional operating regions are evident, the first is "cut-off", where $I_B = 0$ and $I_C = 0$ independent of V_{CE}. The second is "saturation", where $V_{CE} = 0$; in this region both diodes are conducting and I_C is constrained to a region.

$$-\beta_R I_B \le I_C \le \beta_F I_B, \qquad V_{CE} = 0. \qquad (3.38)$$

This very simple model predicts many of the salient features which may be observed in measured static curves. If the ideal diode characterization defined by Eqn. 3.1 is employed, several other features become evident. When the diode reverse saturation currents, designated I_{CS} for the collector diode and I_{ES} for the emitter diode, and the diode forward voltages predicted by the ideal diode characterization are incorporated in the Ebers-Moll model, the characteristic curves of Figure 3.32 result. The four parameters are not independent; a study of the physics of transistor operation shows that a reciprocity relation,

$$\alpha_R I_{CS} = \alpha_F I_{ES}$$

is true. The most obvious deviation of Figure 3.32 from Figure 3.31 is the finite collector to emitter voltage drop when operating in the saturation region. The model predicts that for an NPN transistor this voltage will be

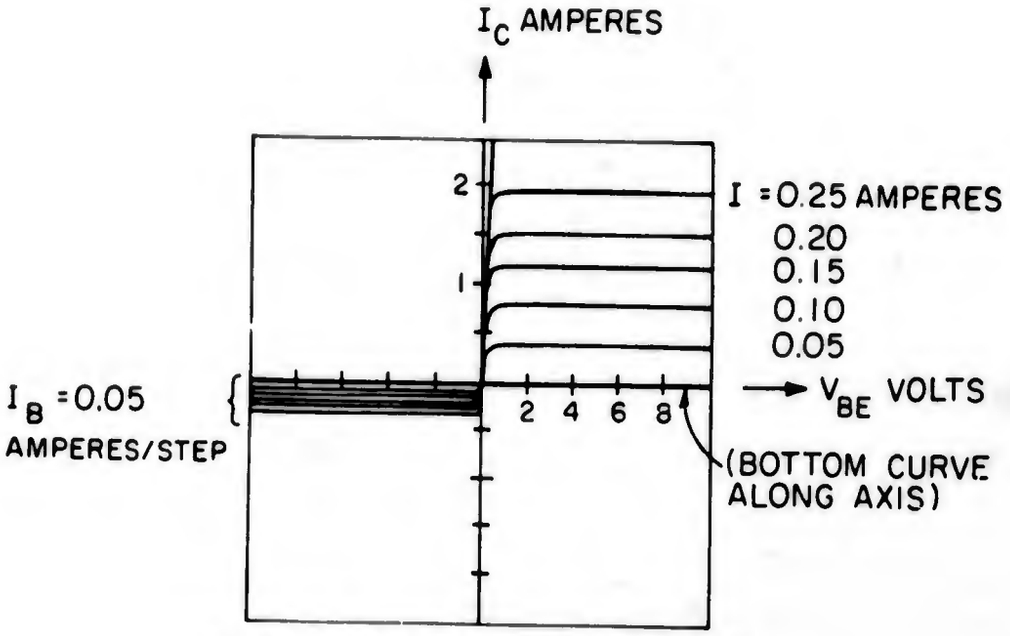
$$V_{CE|SAT} = \frac{nkT}{q} \ln \left[\frac{1 + \frac{1}{\beta_R}\left(\frac{I_C}{I_B} + 1\right)}{1 - \frac{I_C}{I_B}\frac{1}{\beta_F}} \right],$$

$$-\beta_R > \frac{I_C}{I_B} > \beta_F \qquad (3.39)$$

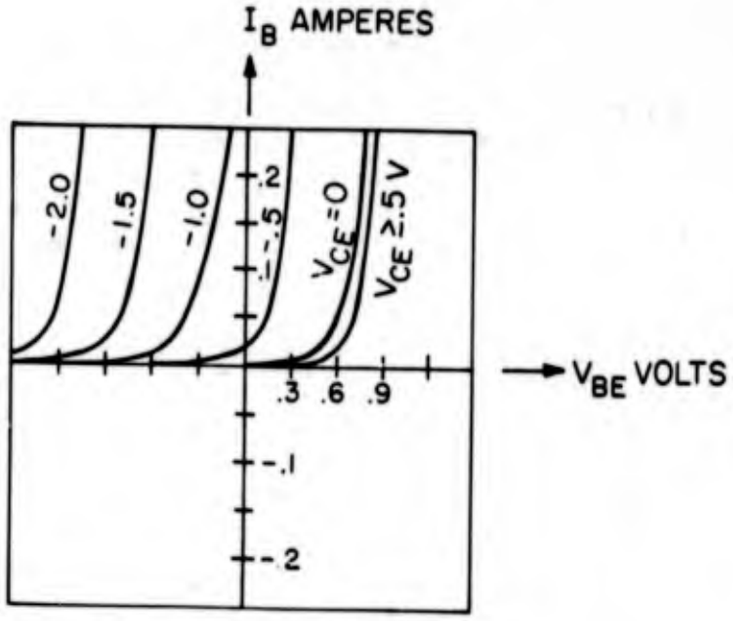
The factor $\frac{I_C}{I_B}$ is known as the "forced beta" in saturation and will be denoted here as

$$\beta_s = \frac{I_C}{I_B} \qquad (3.40)$$

Note that for convenience in preserving the sign of $V_{CE|SAT}$, β_s may



(a) COLLECTOR CHARACTERISTICS



(b) BASE CHARACTERISTICS

FIG. 3.32 "IDEAL" TRANSISTOR CHARACTERISTICS

be positive or negative as determined by the sign of I_C, and Eqn. 3.39 may be rewritten as

$$V_{CE|SAT} = \frac{nkT}{q} \ln \left[\frac{1 + \frac{1}{\beta_R} (\beta_s + 1)}{1 - \frac{\beta_s}{\beta_F}} \right],$$

$$\beta_F > \beta_s > -\beta_R. \qquad (3.41)$$

This equation is plotted in Figure 3.33 for a typical transistor having $\beta_F = 30$, $\beta_R = 10$, and $\frac{nkT}{q} = 35$ millivolts. At a fixed collector current level, as β_s decreases (I_B increases), the saturation voltage decreases - this condition will prevail until bulk resistances in the emitter region of the transistor cause voltage drops due to excess base current which increases the measured $V_{CE|SAT}$. A second deviation of Figure 3.32 from Figure 3.31 occurs in the input family of curves. The non-zero base-emitter diode voltage of the ideal diode model results in a non-zero base-emitter voltage with the shape characteristic of the forward biased diode volt-ampere relation (Figure 3.4). When the collector voltage is negative, the transistor is operating in the reverse-active region and the collector diode volt-ampere curve, displaced negatively by the collector-emitter voltage, is observed. Using Figure 3.30 and the ideal diode law, the general volt-ampere relation for the input characteristics may be written as

$$I_B = I_{ES}(1-\alpha_F)\left(e^{\frac{qV_{BE}}{nkT}} - 1\right)$$

$$+ I_{CS}(1-\alpha_R)\left(e^{\frac{qV_{BE} - V_{CE}}{nkT}} - 1\right) \qquad (3.42)$$

This expression is valid for all regions of operation.

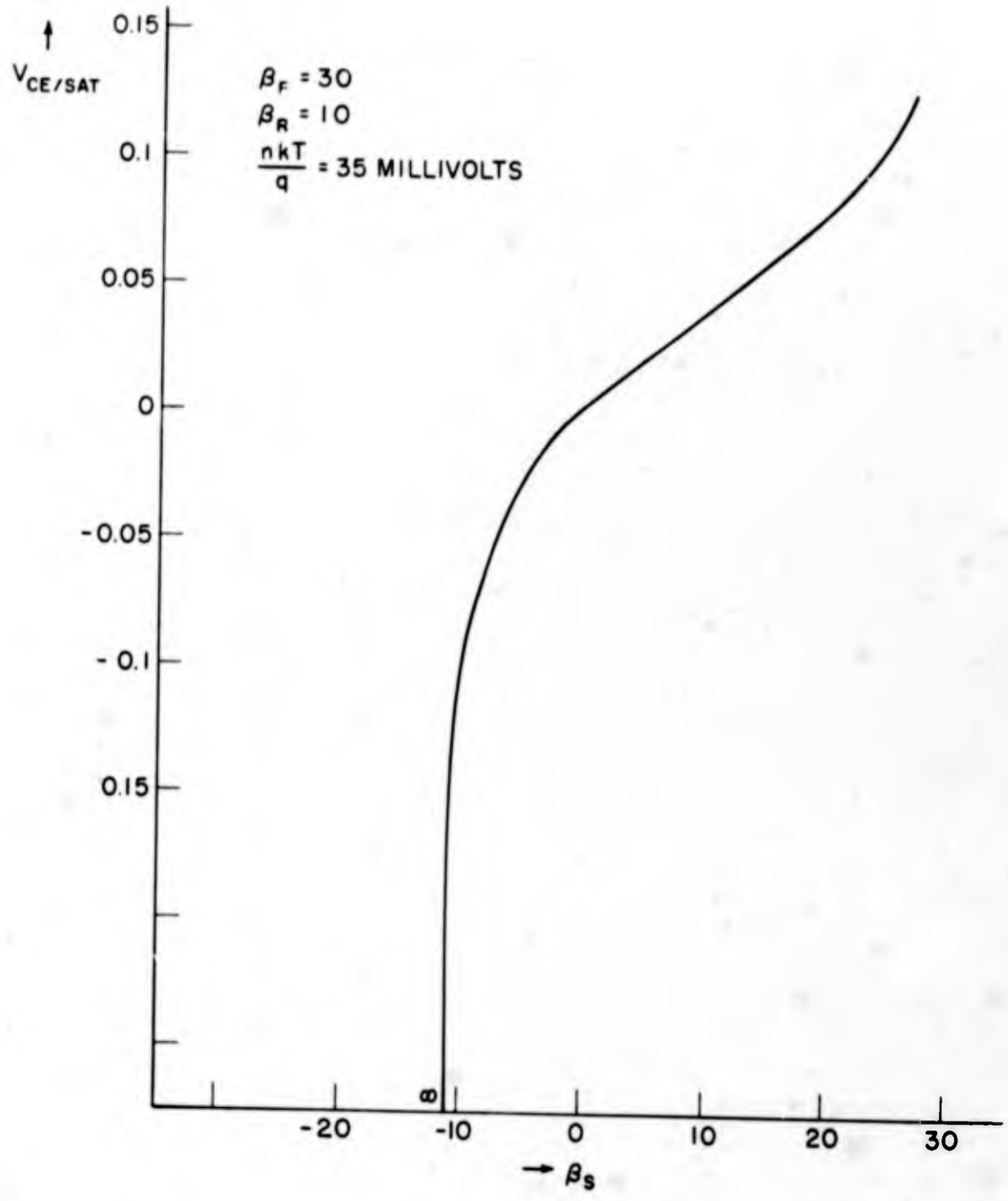


FIGURE 3.33

PLOT OF $V_{CE|SAT}$ VERSUS β_S FOR A TYPICAL TRANSISTOR

In the forward active region, where $V_{CE} >> V_{BE}$, Eqn. 3.42 reduces to

$$I_B \simeq I_{ES}(1-\alpha_F)e^{\frac{qV_{BE}}{nkT}} - I_{CS}(1-\alpha_R).$$

If $|I_{CS}(1-\alpha_R)| << I_B$, as is usually the case with silicon transistors, the input curves in this region may be characterized by the expression

$$I_B \simeq I_{ES}(1-\alpha_F)e^{\frac{qV_{BE}}{nkT}} \qquad (3.43)$$

and is independent of V_{CE}.

In the reverse active region, where $V_{CE} << 0$, Eqn. 3.42 yields

$$I_B = -I_{ES}(1-\alpha_F) + I_{CS}(1-\alpha_R)e^{\frac{qV_{BE}V_{CE}}{nkT}}$$

which reduces to

$$I_B = I_{CS}(1-\alpha_R)e^{\frac{q(V_{BE}-V_{CE})}{nkT}} \qquad (3.44)$$

if the usual case, $|I_{ES}(1-\alpha_F)| << 1$ holds true. Graphically Eqn. 3.44 may be interpreted as representing an ideal diode volt-ampere relation with saturation current $I_s = I_{CS}(1-\alpha_R)$ and displaced along the voltage axis by an amount $V = V_{CE}$. The validity of this interpretation is evident in Figure 3.32.

In the saturation region, either the collector or emitter diodes may operate in the region between the non-conducting and conducting states, therefore simplifications of Eqn. 3.42 cannot be made.

The final important deviation in transistor behavior of the "ideal" diode model from the "perfect" diode model may be placed in evidence by examining the approximations leading to Eqns. 3.43 and 3.44. The terms $I_{CS}(1-\alpha_R)$ and $I_{ES}(1-\alpha_F)$ were neglected in arriving at the final expressions. These terms represent the base current necessary to compensate for the bulk leakage components of the reverse biased collector and emitter diodes respectively - the same type of leakage current discussed in Section 3.1. For the reasons previously discussed, the values of leakage current actually observed at room temperatures and below are greater than those predicted by the bulk model alone. Additionally, the α_F and α_R of transistors are somewhat dependent on the current levels at which they are measured and, in particular, become very small at the leakage current levels commonly encountered in silicon devices. These factors cause poor correlation between leakage currents predicted by any but the most complex theoretical models, hence calculations involving leakage currents are based on actual measured values or on worst-case specifications provided in data sheets. The total leakage may be accounted for in the model by the addition of external current sources in parallel with the collector and emitter diode, as shown in Figure 3.34.

The magnitude of the bulk current source leakage may be found from Figure 3.30 with the collector reverse biased, and is simply the collector diode saturation current, I_{CS}. The current source I_{CS} in parallel with the collector diode, and $\alpha_R I_{CS}$ in parallel with the emitter diode accounts for this term. The additional I_L term in the collector leakage current source accounts for the extraneous collector-base leakage current, including junction edge and transition region effects discussed in Section 3.1. The basic leakage parameter that is usually measured in transistors is I_{CBO} (sometimes called just I_{CO}), the collector-base leakage current with the emitter lead open. From Figure 3.34, this current is

$$I_{CO} \triangleq I_{CBO} = I_{CS}(1-\alpha_R\alpha_F) + I_L. \qquad (3.45)$$

It is worthwhile to investigate one other leakage current which often causes circuit operation problems - this is I_{CEO}, the collector-

emitter current with the base terminal open and collector diode reverse biased. Using the leakage model of Figure 3.34, this current is calculated to be

$$I_{CEO} = \frac{I_{CO}}{1-\alpha_F} = (\beta_F + 1)\, I_{CO}. \qquad (3.46)$$

If β_F is large, I_{CEO} may be appreciable, even with a small I_{CO}.

A similar model may be constructed for emitter diode leakage if reverse-active operation is contemplated. As indicated, at room temperature in silicon transistors the effects of leakage currents on the observed characteristic curves are negligible unless the curves are observed at very low current levels. For this reason, no leakage effects are visible in the characteristic curves plotted in Figure 3.32.

In Figure 3.35 a family of measured input and output curves are presented. On comparing these to the theoretical set of curves, it is evident that all of the essential features predicted by the ideal diode

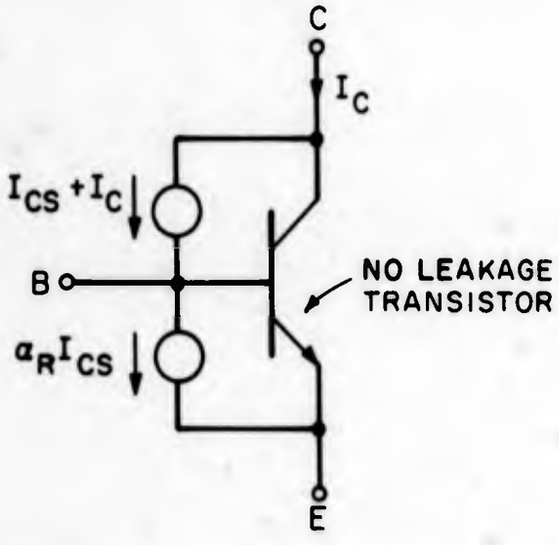
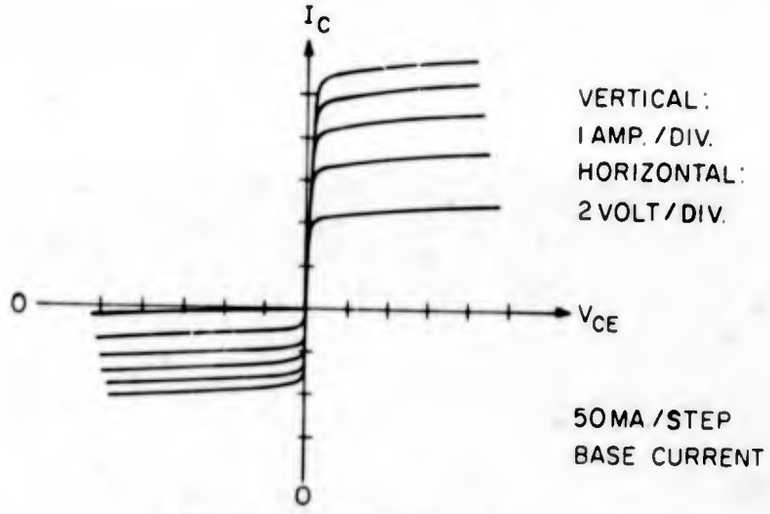
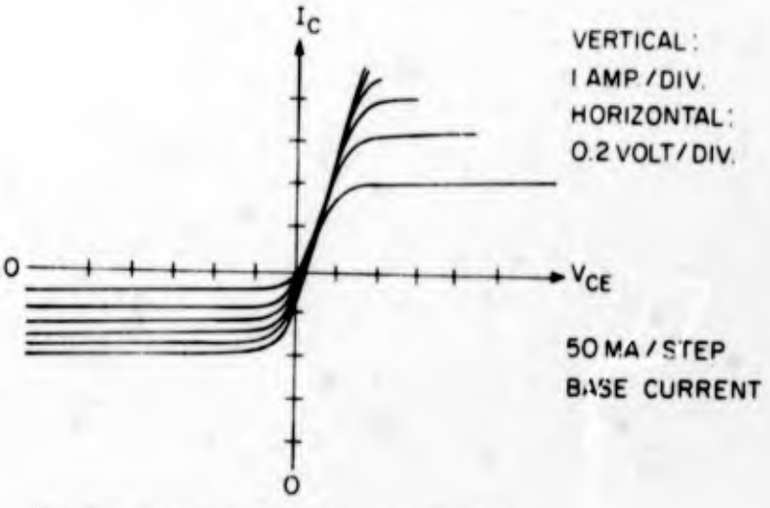


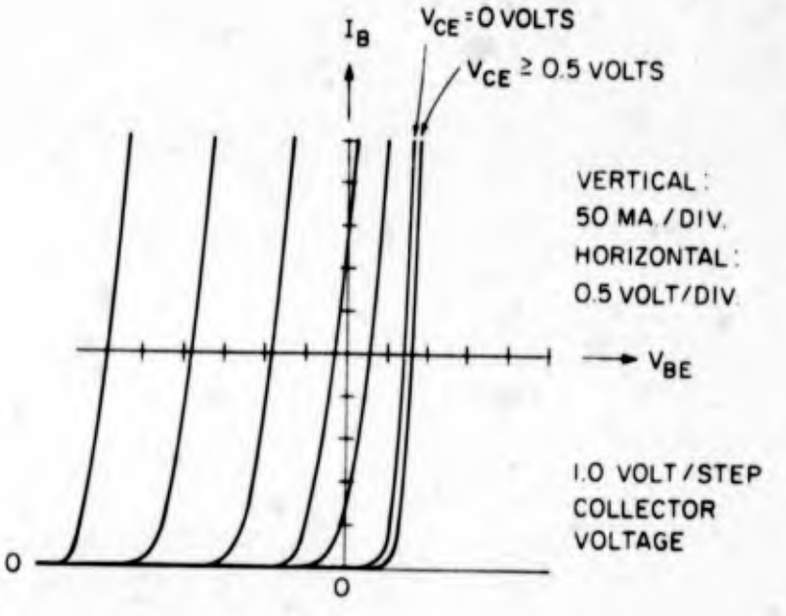
FIG.3.34 COLLECTOR LEAKAGE MODEL



(a) OUTPUT CHARACTERISTICS



(b) EXPANDED OUTPUT CHARACTERISTICS



(c) INPUT CHARACTERISTICS

FIG. 3.35 MEASURED TRANSISTOR CHARACTERISTICS

Ebers-Moll model are contained in the measured data. At an operating point of $|I_C| = 2$ amperes, the measured transistor has the following parameters:

$\beta_F = 20$

$\beta_R = 8$

$V_{CE|SAT} = .170$ volts forward

$V_{CE|SAT} = .80$ volts reverse.

The Ebers-Moll model fails to predict the non-zero slope that can be observed in Figure 3.35a, the output curves in the forward and reverse active operating region. This effect may be traced to changes in the active width of the reverse biased collector diode with voltage variations changing the effective width of the base region of the transistor, and is called base width modulation. The calculations necessary to predict this slope require a detailed knowledge of the construction of the device - parameters which are not generally available. As is the case with leakage currents, measured data or worst-case specifications may be used for analysis purposes. A model which incorporates a resistor to account for the base width modulation effect is shown in Figure 3.36. This model may not be used when the transistor is cut-off, since there collector-emitter current is determined primarily by leakage currents. The data in Figure 3.35 indicates that for this transistor $R_O = 75\Omega$ near an operating point of 2 amperes in both the forward and reverse active regions, and decreases as the collector current level increases. At $I_O = 4$ amperes, $R_O = 40\Omega$.

Transistor Temperature Dependence

As is the case with semiconductor diodes, it is necessary to consider the effects of temperature variations on the characteristics of transistors in order to gain sufficient insight into the operation of these devices to allow evaluation of their behavior in circuits. The discussion in the previous section has shown that a transistor may be

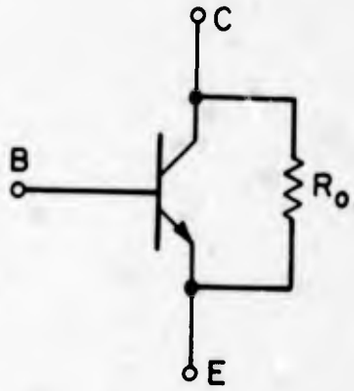


FIG.3.36 TRANSISTOR MODEL WITH RESISTOR TO ACCOUNT FOR BASE WIDTH MODULATION

viewed as a combination of two diodes with mutual interaction, represented by current dependent current sources, between them. As might be expected, the primary effects of temperature may be related to the effects of temperature on the diodes. To study temperature variations, families of input and output characteristic curves will be examined and the changes in model parameters assessed. The parameters of interest here are collector leakage currents (e.g., I_{CO}, I_{CEO}), current gain (β), collector-emitter saturation voltage ($V_{CE|SAT}$) and base-emitter voltage (V_{BE}).

Eqns. 3.45 and 3.46 state that both I_{CO} and I_{CEO} are linearly dependent on the collector diode saturation current I_{CS}. In Section 3.1, we found that this current varied as

$$I_s(T) = CT^3 e^{\frac{-E_{go}}{kT}} \qquad (3.14)$$

and this dependence was plotted in Figures 3.12, 3.13 and 3.14, these graphs are usable for I_{CO} and I_{CEO} calculations. Since I_{CEO} is a leakage current multiplied by $\frac{1}{1-\alpha_F}$, it can get quite large at elevated temperatures if a transistor is used in this mode. If a current

$$I_B = -\frac{I_{CS}(1-\alpha_R\alpha_F) - I_L}{\alpha_F} = -\frac{I_{CO}}{\alpha_F} \qquad (3.47)$$

is injected into the base terminal, then from Figure 3.31,

$$I_C = \frac{I_{CO}}{1-\alpha_F} + \beta_F\left[-\frac{I_{CO}}{\alpha_F}\right]$$

or

$$I_C = 0,$$

and the leakage component has been cancelled. Linear circuits which utilize feedback techniques to set the collector current or its equivalent perform this compensation inherently. Linear circuits which bias the transistor from an incremental low impedance source do not null the change in collector current with temperature, but restrict it to I_{CES}, the reverse biased collector-emitter current with the base terminal shorted to the emitter terminal. The model shows this to be $I_{CES} = I_{CS} + I_L$.

If the transistor is operating in the cut-off region, it may not be possible to perform the compensation required by Eqn. 3.47. From the Ebers-Moll model and Figure 3.34, the minimum collector current in cut-off (both junctions reverse biased) is

$$I_{CEV} = I_L + I_{CS} - \alpha_F I_{ES} = I_{CS}(1-\alpha_R) + I_L. \qquad (3.48)$$

The reciprocity relation which holds for the ideal diode model has been used to simplify Eqn. 3.48. This relation now represents the minimum possible collector cut-off current. If $\alpha_R \ll 1$, which is true in silicon transistors at low current levels, this leakage current may become appreciable at elevated junction temperatures and should be considered in circuit design.

The current gain β is related to the α parameters of the model by Eqn. 3.24, repeated here:

$$\beta = \frac{\alpha}{1-\alpha}. \qquad (3.24)$$

Since the α's may be only slightly less than 1, small variations in α can result in large β changes. No simple model exists which quantitatively predicts the variation in α, but qualitatively the behavior of transistors may be ascertained by observations based on a number of different transistor types. Over the entire operating temperature range, α and, hence, β has a positive temperature coefficient. At a junction temperature of -55°C, β is 40 to 60% of its initial value at 25°C. At 100°C, β increases to 120 to 140% of its initial value. When the current levels in a power transistor become very high, the temperature coefficient of β may have a saddle point as the current increases and at rated current the β may fall with temperature increases. Figure 3.37 is a plot of β versus temperature at various collector currents for a typical silicon signal transistor. Figure 3.38 is the same type of plot for a silicon power transistor. Note that the reversal of β occurs only at currents very near the maximum rated current of the power transistor.

The dependence of $V_{CE|SAT}$ on temperature may be ascertained by interpretation of Eqn. 3.41 and in view of the previous discussion on β variations. The incremental temperature coefficient of collector saturation voltage may be determined by calculating the partial

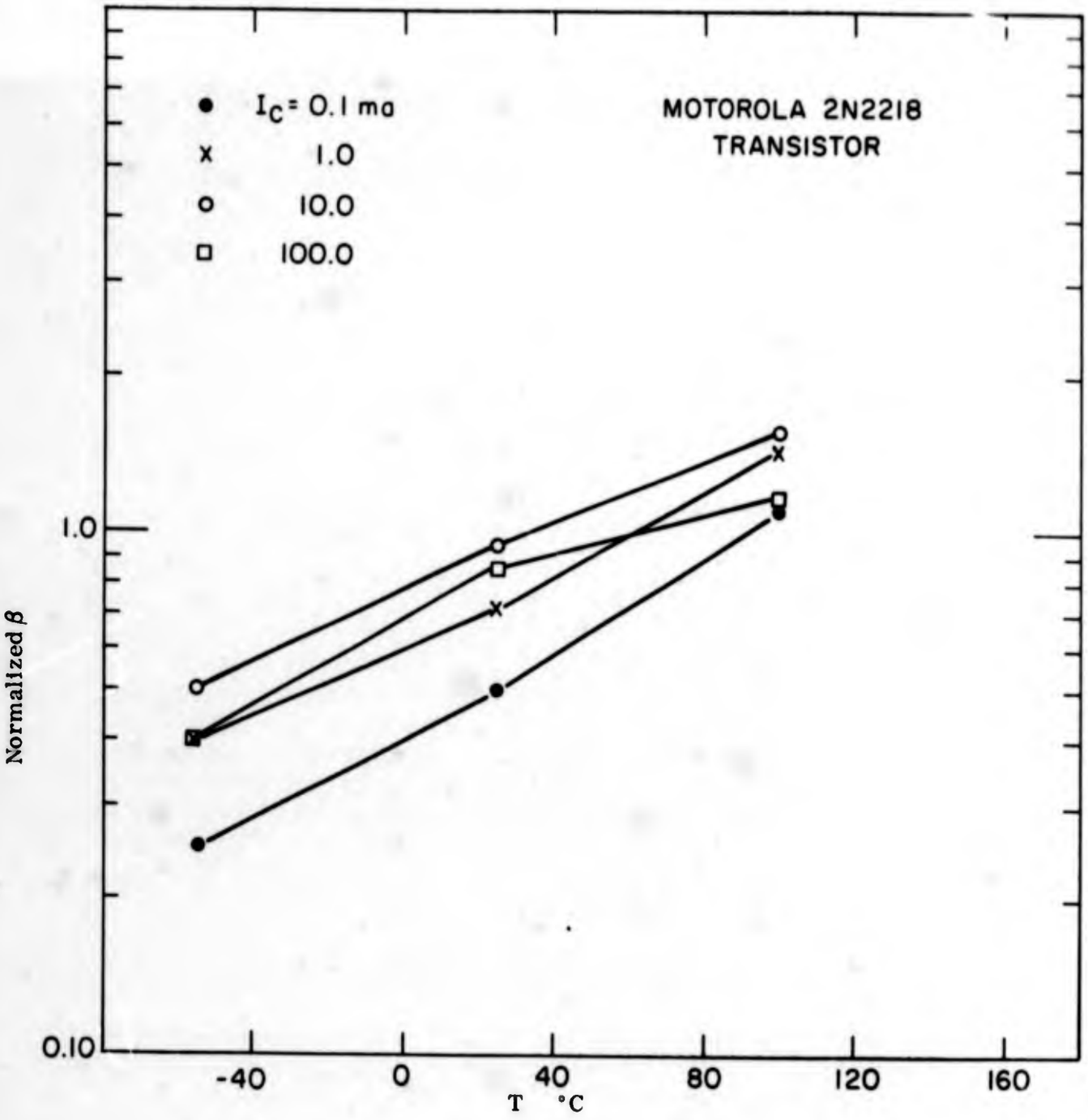


FIGURE 3.37

PLOT OF β VERSUS TEMPERATURE FOR A SILICON SIGNAL TRANSISTOR

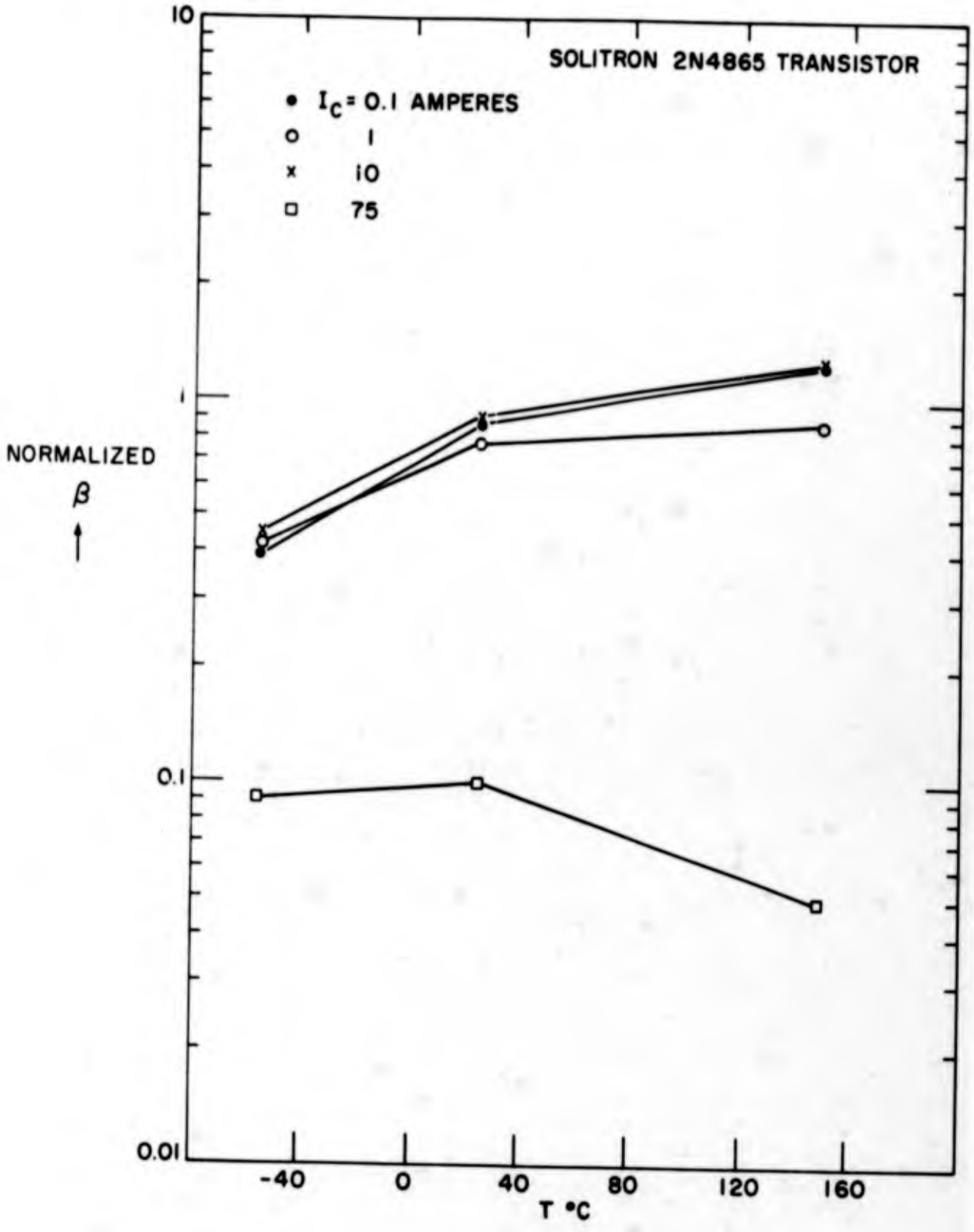


FIG. 3.38 PLOT OF β VERSUS TEMPERATURE FOR A SILICON POWER TRANSISTOR.

differential of $V_{CE|SAT}$ (Eqn. 3.41) with respect to temperature, with the results

$$\frac{\partial V_{CE|SAT}}{\partial T} = \frac{nk}{q}\left\{ \ell_n \frac{1 + \frac{\beta_S + 1}{\beta_R}}{1 - \frac{\beta_S}{\beta_F}} - T\left[\left(\frac{\beta_S + 1}{\beta_R^2}\right)\left(\frac{1}{1 + \frac{\beta_S + 1}{\beta_R}}\right)\frac{\partial \beta_R}{\partial T} + \left(\frac{\beta_S}{\beta_F^2}\right)\left(\frac{1}{1 - \frac{\beta_S}{\beta_F}}\right)\frac{\partial \beta_F}{\partial T}\right]\right\} \tag{3.49}$$

If β_S is positive (positive current into the collector terminal), and the region of current where $\frac{\partial \beta}{\partial T} > 0$ is considered, Eqn. 3.49 indicates that the temperature coefficient can be either positive or negative, depending upon the particular transistor and set of operating conditions considered. Although for most applications in which transistors are used in switching circuits $V_{CE|SAT}$ has a positive temperature coefficient, it is not strongly temperature dependent, and some devices may be found which exhibit a negligible $V_{CE|SAT}$ change over a wide temperature range.

At collector current levels that approach the maximum rated current of the transistor, the temperature coefficient of β is negative. In this instance, both major terms in Eqn. 3.49 are positive, hence, $V_{CE|SAT}$ exhibits a positive temperature coefficient. Additionally, at high current levels bulk resistance in the collector and emitter regions become large enough to add a voltage drop to the measured $V_{CE|SAT}$ and these components also have a positive temperature coefficient. Figure 3.39 is a plot of $V_{CE|SAT}$ versus temperature at various collector current levels for a silicon power transistor, exhibiting the effects described here.

The base-emitter voltage temperature coefficient, like collector-emitter saturation voltage, is the result of two temperature effects of opposite temperature coefficients. These are the temperature variations of the junction voltage

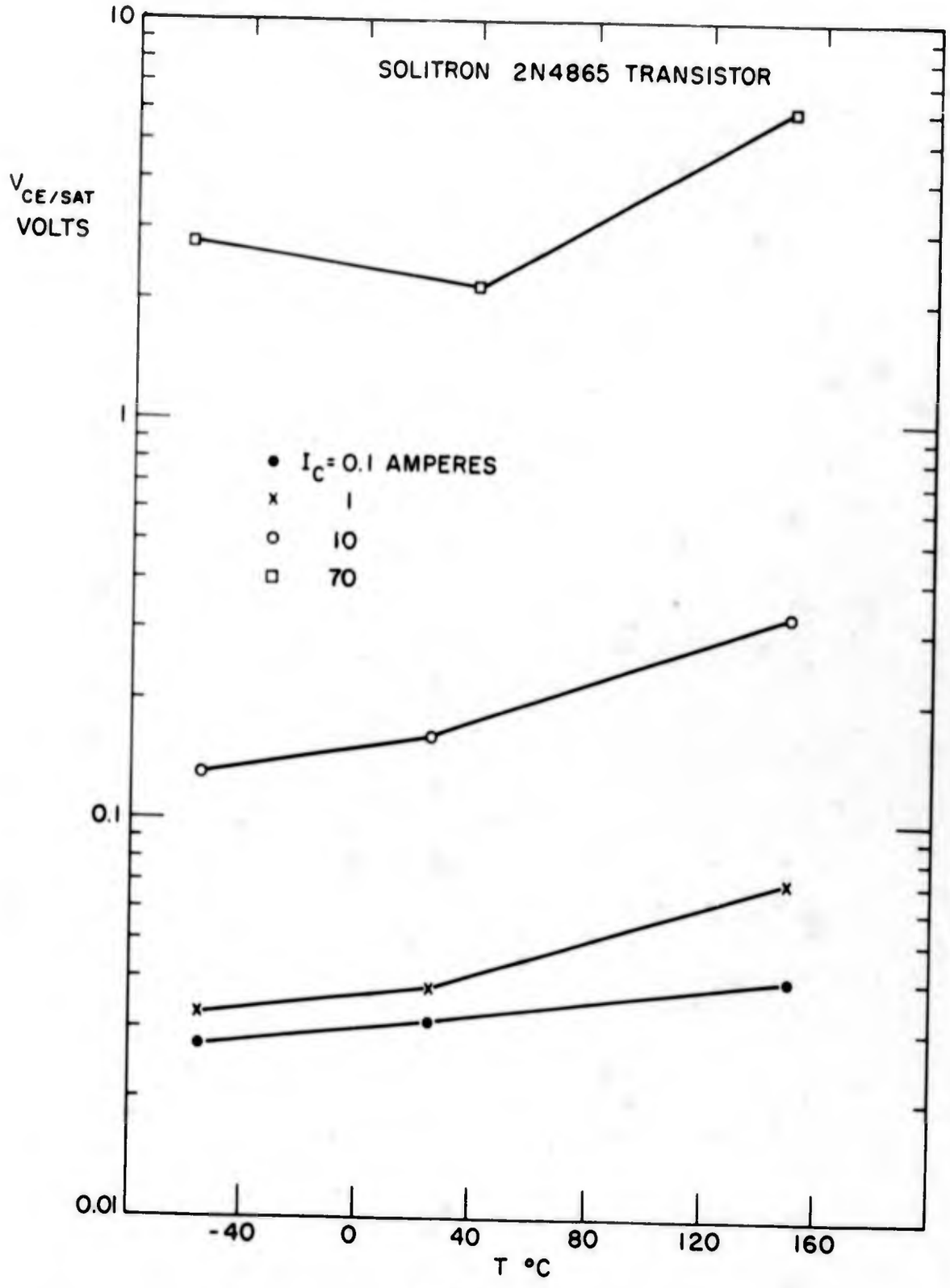


FIGURE 3.39

$V_{CE|SAT}$ VERSUS TEMPERATURE FOR A SILICON POWER TRANSISTOR

of an ideal diode and the variations caused by thermally induced bulk resistance changes in the base and emitter region. Unlike the $V_{CE|SAT}$ case, it is relatively easy to predict the sign of the net temperature coefficient. At emitter currents which are small compared to the rated current, the base-emitter ideal diode volt-ampere characteristic may be observed and the discussion leading to Eqn. 3.13 describes the temperature variations. If the total emitter current is constrained to be a constant independent of temperature variations, as might be the case if the current was controlled by factors external to the transistor, e.g. if the transistor was saturated or if the emitter current was regulated by feedback means, then the temperature coefficient of emitter-base voltage may be found by partial differentiation and solution of Eqn. 3.13 for $\left.\frac{\partial V}{\partial T}\right|_I$. When this is done, the simplified result is

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_I = \frac{nk}{q}\left[\frac{q}{kT}\left(\frac{V_{BE}}{n} - \frac{E_{go}}{q}\right) - 3\right], \qquad V_{BE} \gg \frac{kT}{q} . \tag{3.50}$$

For a silicon transistor with $n = 1.4$, Eqn. 3.50 is plotted versus T in Fig. 3.40, at various values of V_{BE}. Note that the temperature coefficient due to diode effect is always negative and does not vary substantially over the entire practical operating region.

When the emitter current approaches the rated transistor current, voltage drops due to bulk resistance in the base and emitter regions significantly increase the base-emitter terminal voltage, in the same manner as these resistive components effect the terminal voltage of a diode. This component of base-emitter voltage has a positive temperature coefficient and at currents where this drop is significant the voltage will have a less negative temperature coefficient than predicted by Eqn. 3.50, or the coefficient may even be positive. A rule of thumb which appears to hold for most silicon transistors is to use Eqn. 3.50 or Fig. 3.40 to predict the temperature coefficient if V_{BE} at 25°C is less than 0.8 volts. If V_{BE} at 25°C is greater than 1.0 - 1.2 volts, the temperature coefficient is smaller than predicted by Eqn. 3.50, but negative.

Figure 3.41 shows a plot of V_{BE} versus temperature at various collector currents for a silicon power transistor.

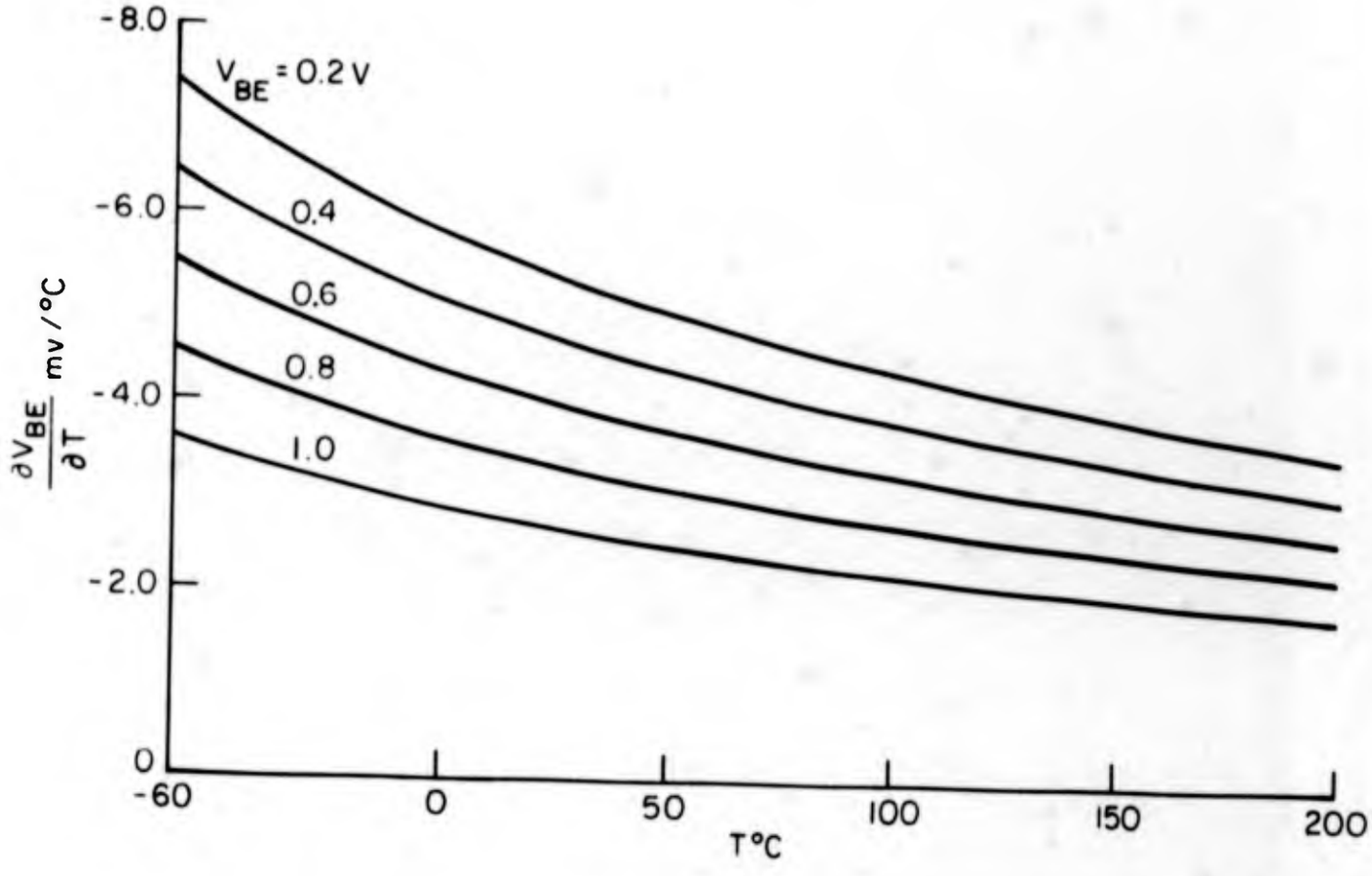


FIG. 3.40 BASE-EMITTER TEMPERATURE COEFFICIENT FOR A SILICON TRANSISTOR.

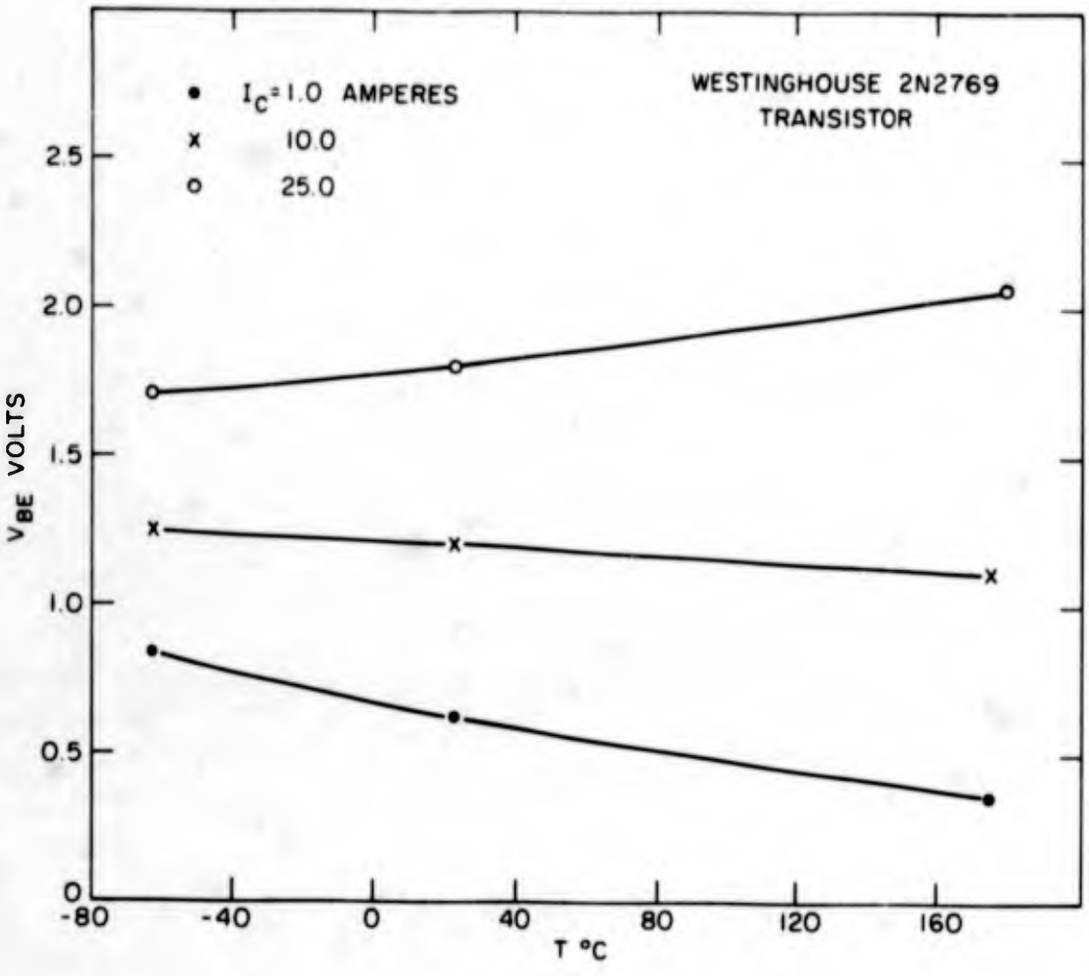


FIGURE 3.41

PLOT OF V_{BE} VERSUS TEMPERATURE FOR A SILICON POWER TRANSISTOR

Transistor Dynamic Characteristics

The transistor exhibits dynamic operating effects due to rapid changes in external terminal constraints which are governed by the same charge storage mechanisms which govern the dynamic operation of diodes discussed in Section 3.1. The effects to be considered in this section are those associated with the operation of transistors as power switches and, in particular, those facets of dynamic switching operation which may result in power being dissipated in the circuit or device. The transistor topics that are covered include the finite turn-on and turn-off time, excess storage time in saturation and the effects of collector capacity on switching time.

For a transistor operating in the forward active region, a charge controlled model identical in form to Eqn. 3.19, the diode charge control equation, may be used to relate charge stored in the base region of the transistor to the base terminal current. This may be expressed as

$$i_B = \frac{q_F}{\tau_{BF}} + \frac{dq_F}{dt} \qquad \text{(forward active region)} \qquad (3.51)$$

where τ_{BF} is the characteristic time constant of charge decay or leakage. The collector current is linearly related to the stored base charge by the relation

$$i_C = \frac{q_F}{\tau_F} \qquad (3.52)$$

where τ_F, known as the collector time constant, is the proportionality constant. Under steady state conditions $\frac{dq_F}{dt} = 0$, and Eqn. 3.51 reduces to

$$I_B = \frac{q_F}{\tau_{BF}} \qquad (3.53)$$

Dividing Eqn. 3.52 by 3.53 yields

$$\frac{I_C}{I_B} = \frac{\tau_{BF}}{\tau_F} = \beta_F \qquad (3.54)$$

which is the constraining relation between the collector and base time constants.

Eqns. 3.51 and 3.53 provide the key to relating transistor change in the base current to the dynamic response of the collector current. For example, suppose that a base current $i_B = I_o$ has been established in the base circuit of a transistor operating in the forward active region and this current has persisted long enough to allow steady state operation to be reached. Now at $t = 0$, a positive increase of base current $\Delta i_B = \Delta I$ is applied to the base terminal. Solving Eqn. 3.51 for these conditions results in

$$q_F = \tau_{BF} I_0, \qquad t < 0$$

$$q_F = \tau_{BF} [I_0 + \Delta I (1 - e^{-t/\tau_{BF}})], \qquad t \geq 0. \tag{3.55}$$

Using Eqns. 3.52 and 3.54,

$$i_C = \beta_F I_0, \qquad t < 0$$

$$i_C = \beta_F [I_0 + \Delta I (1 - e^{-t/\tau_{BF}})] \qquad t \geq 0. \tag{3.56}$$

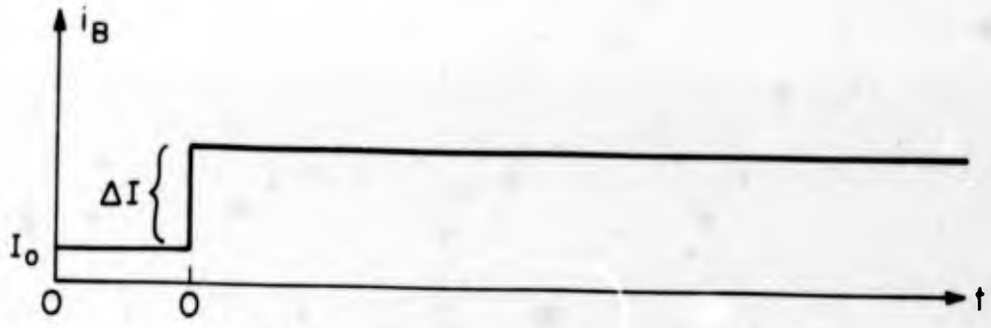
which is the desired collector current transient. The pertinent waveforms for this transient are drawn in Figure 3.42.

In switching applications, the transient in turning on and turning off the device is of greater interest than the change from one active current level to another. Two examples will be examined which demonstrate the significant features of switching operation:

1) "Natural" turn-off

2) Forced turn-off.

To examine natural turn-off, consider a transistor operating in the forward active region in the steady state with $i_B = I_0 > 0$. At $t = 0$, the base drive is removed ($i_B = 0$). Proceeding as in the previous example



(a) BASE CURRENT

(b) STORED CHARGE

(c) COLLECTOR CURRENT

FIG 3.42 WAVEFORMS FOR A STEP CHANGE IN BASE CURRENT

$$q_F = I_0 \tau_{BF}, \qquad t < 0$$

$$q_F = I_0 \tau_{BF} e^{-t/\tau_{BF}}, \qquad t \geq 0, \tag{3.57}$$

and

$$i_C = \beta_F I_0, \qquad t < 0$$

$$i_C = \beta_F I_0 e^{-t/\tau_{BF}}, \qquad t \geq 0. \tag{3.58}$$

These equations describe the natural transistor turn-off; the corresponding waveforms are shown in Figure 3.43.

To examine forced turn-off, consider the same initial conditions as in the previous example ($i_B = I_0$). At $t = 0$, the base current is reversed to $i_B = -I_1$. Solving the charge control equations yields

$$q_F = I_0 \tau_{BF}, \qquad t < 0$$

$$q_F = \tau_{BF} [I_0 - (I_1 + I_0)(1 - e^{-t/\tau_{BF}})], \qquad t \geq 0, \; q_F \geq 0, \tag{3.59}$$

and

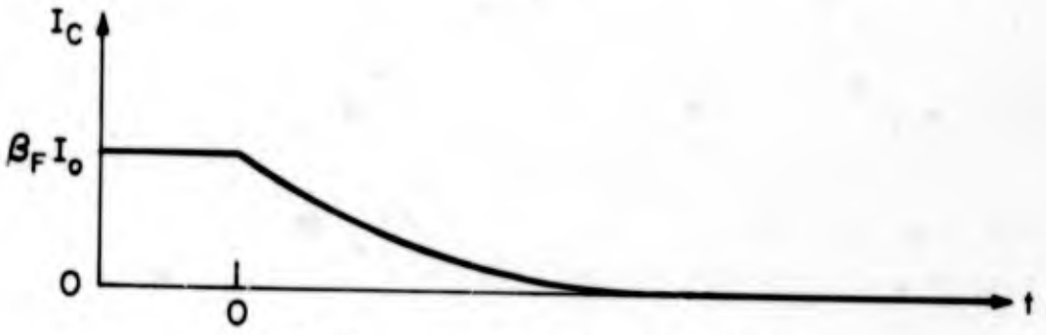
$$i_C = \beta_F I_0, \qquad t < 0$$

$$i_C = \beta_F [I_0 - (I_1 + I_0)(1 - e^{-t/\tau_{BF}})], \qquad t \geq 0, \; I_C \geq 0. \tag{3.60}$$

The restriction that $q_F \geq 0$ and $I_C \geq 0$ must be added to these equations since these conditions deliniate the boundary between the forward-active and cut-off regions. When $q_F = 0$, the transistor enters cut-off, hence this condition signifies the instant of transistor turn-off. The form of Eqn. 3.59 is identical

(a) BASE CURRENT

(b) STORED CHARGE



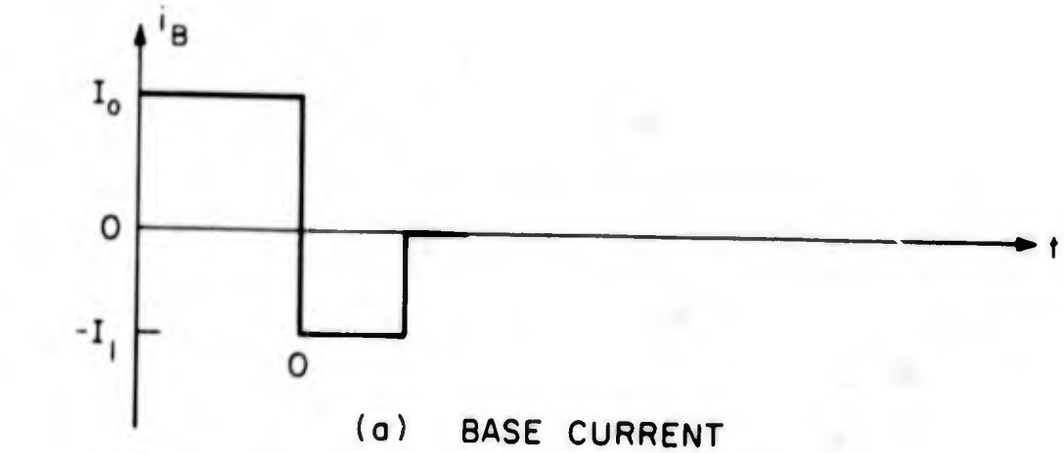
(c) COLLECTOR CURRENT

FIG. 3.43 WAVEFORMS FOR "NATURAL" TURN-OFF

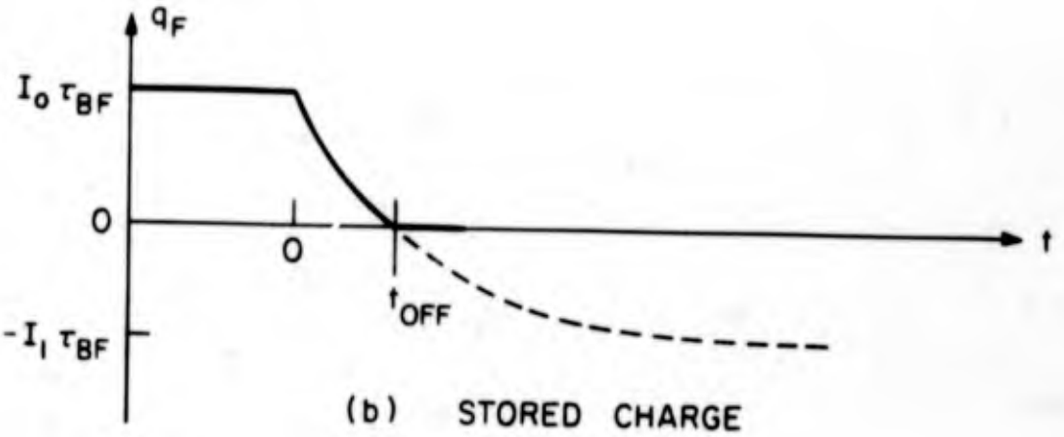
to that of Eqn. 3.23. The turn-off time, t_{off} may be calculated by solving Eqn. 3.59 for t with $q_F = 0$, as was done with Eqn. 3.23. The result is

$$t_{off} = \tau_{BF} \ln \left(1 + \frac{|I_0|}{|I_1|}\right), \tag{3.60}$$

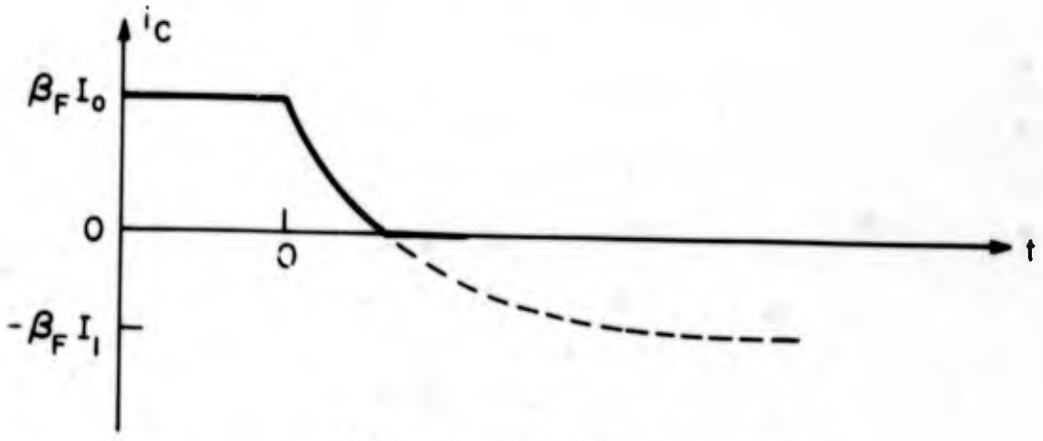
which corresponds to Eqn. 3.24 and the plot in Figure 3.18, which may be used with appropriate substitutions for evaluating Eqn. 3.60. The pertinent waveforms for the forced turn-off case are shown in Figure 3.44. Comparison with Figure 3.43 shows that by forcing, the turn-off time may be made many times faster than the natural turn-off time of the transistor. The actual limitation on forced turn-off time is due to effects attributable to the distributed nature of the actual transistor versus the lumped model presented here. This time limitation is comparable to $t_\tau = \frac{1}{f_\tau}$, where f_τ is the frequency where the incremental β_F about some specified operating point falls to 1. However, t_τ, because it is a small signal parameter, is <u>not</u> a figure of merit for the minimum switching time of various transistors. Actual switching time specifications or measurements must be used to compare devices. Figure 3.45 is an oscillogram of the active region turn-off of a silicon power transistor under both unforced and forced conditions. For the forced cases, $\frac{I_0}{I_1} = 1.0$. On the scale used for viewing the unforced turn-off, the forced turn-off appears to be nearly instantaneous. In practical circuitry using transistor switches, the amount of power dissipated by the device during the switching interval is directly proportional to the switching time; therefore, some form of forced turn-off must be provided to achieve efficient circuit operation.



(a) BASE CURRENT

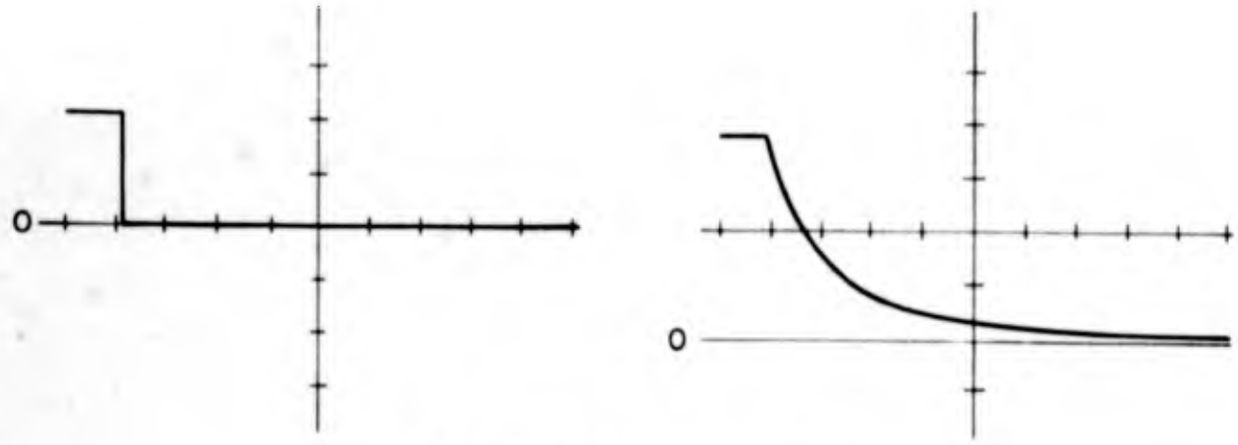


(b) STORED CHARGE

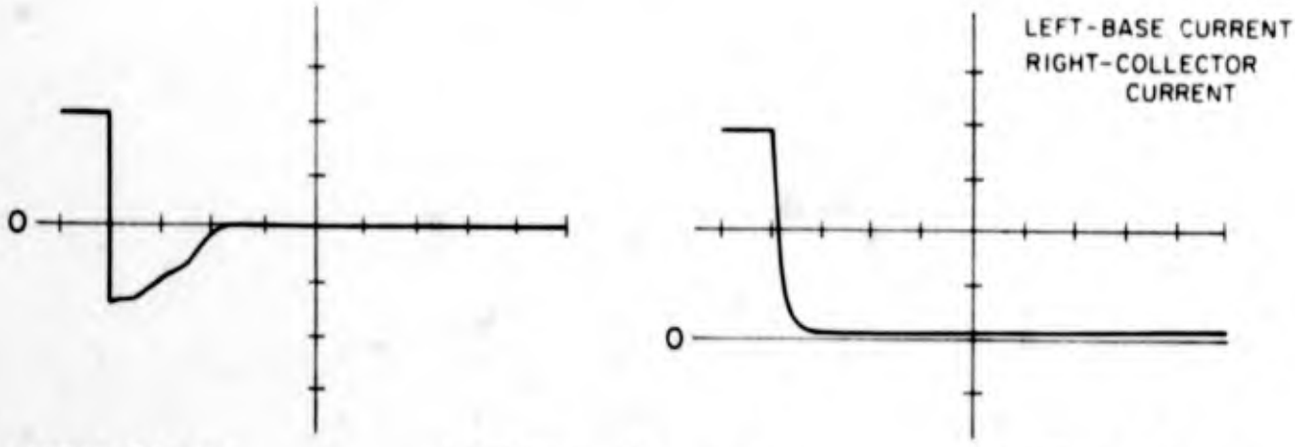


(c) COLLECTOR CURRENT

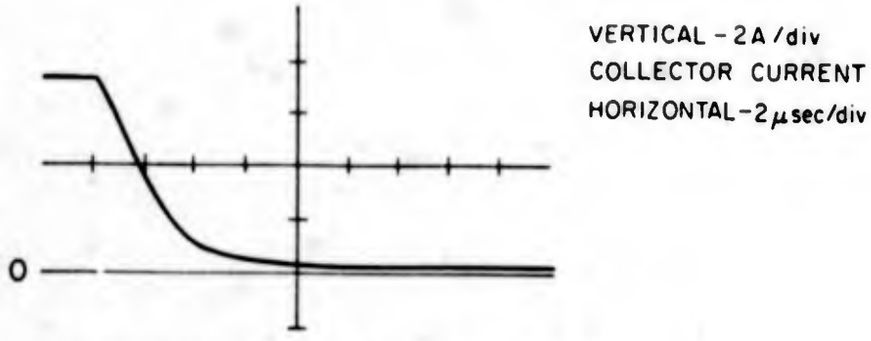
FIG. 3.44 WAVEFORMS FOR FORCED TURN-OFF



(a) UNFORCED TURN-OFF



(b) FORCED TURN-OFF



(c) FORCED TURN-OFF EXPANDED

FIG. 3.45 OSCILLOGRAMS OF TURN-OFF WAVEFORMS.

When a transistor is operated in the reverse active region, the governing charge control equations have a similar form, but different parameters than the forward active case. These expressions are

$$i_B = \frac{q_R}{\tau_{BR}} + \frac{dq_R}{dt}, \tag{3.61}$$

$$i_E = \frac{q_R}{\tau_R} \tag{3.62}$$

and

$$\beta_R = \frac{\tau_{BR}}{\tau_R}. \tag{3.63}$$

where q_R is the charged stored in the base due to reverse active operation, τ_{BR} is the reverse-active base time constant and τ_R is the corresponding emitter reverse-active time constant. Since

$$i_C = -(i_B + i_E),$$

Eqn. 3.62 may be written in terms of the collector current as

$$i_C = -\left(\frac{q_R}{\tau_R} + \frac{q_R}{\tau_{BR}} + \frac{dq_R}{dt}\right). \tag{3.64}$$

These equations may be used to solve for transient responses using the same procedure outlined for forward active operation.

When the transistor operates in saturation, both the collector and emitter diodes are forward biased. Charge that is stored in the base region is contributed by both forward and reverse operation. Because the processes, and hence the equations, of this lumped charge control model are linear, saturation may be thought of as the superposition of both forward and reverse active

operation. Under these circumstances, the appropriate differential equations governing saturation transients are the sum of the two constituent equations. Thus if $q_F > 0$ and $q_R > 0$, then

$$i_B = \frac{q_F}{\tau_{BF}} + \frac{dq_F}{dt} + \frac{q_R}{\tau_{BR}} + \frac{dq_R}{dt} \tag{3.65}$$

and

$$i_C = \frac{q_F}{\tau_F} - \frac{q_R}{\tau_R} - \frac{q_R}{\tau_{BR}} - \frac{dq_R}{dt} . \tag{3.66}$$

When a transistor is used in a switching circuit, the volt-ampere constraint of the collector-emitter load defines the current necessary to reach the boundary between forward-active and saturated operation. This collector current does not change appreciably regardless of how deeply saturated the transistor becomes, since the voltage drop across the transistor and the variations in voltage drop as the transistor becomes more heavily saturated are usually small when compared with the Thevenin equivalent voltage source of the load. In this case, Eqns. 3.65 and 3.66 may be re-written approximately as

$$i_{BS} = i_B - \frac{I_C}{\beta_F} \approx \frac{q_S}{\tau_S} + \frac{dq_S}{dt} , \; q_S \geq 0 \tag{3.67}$$

and

$$i_C = I_C \tag{3.68}$$

where i_{BS} is defined as the <u>excess</u> base current over that needed to bring the transistor to the edge of saturation, q_S is the <u>excess</u> stored base charge over that needed to support the collector current at the edge of saturation, and τ_S is the time constant of decay of the excess stored charge. Comparison of Eqns. 3.67 and 3.68 with Eqns. 3.51 through 3.54 and Eqns. 3.61 through

3.66 shows that the saturation region parameters may be related to the active region parameters by

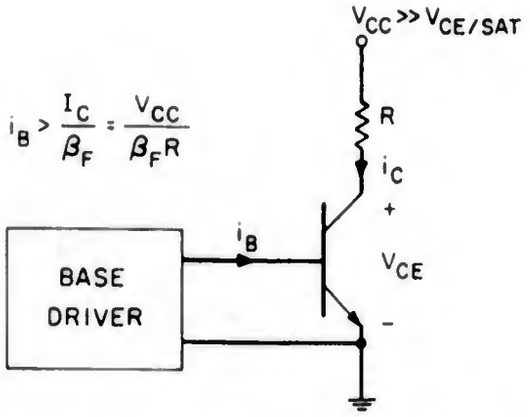
$$q_S = q_F - I_C\tau_F + q_R \tag{3.69}$$

and

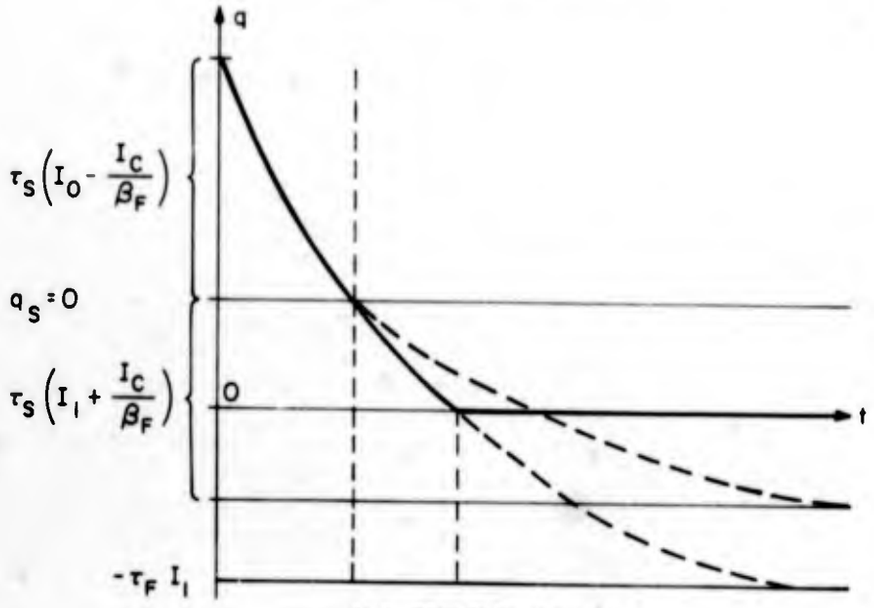
$$\tau_S = \frac{\frac{1}{\tau_F} + \frac{1}{\tau_R} + \frac{1}{\tau_{BR}}}{\frac{1}{\tau_F\tau_{BR}} + \frac{1}{\tau_R\tau_{BF}} + \frac{1}{\tau_{BF}\tau_{BR}}} . \tag{3.70}$$

The term $q_F - I_C\tau_F$ in Eqn. 3.69 may be identified with the excess of forward stored base charge over that needed to bring the transistor to the edge of saturation, and when combined with q_R forms the total excess charge stored in the base region.

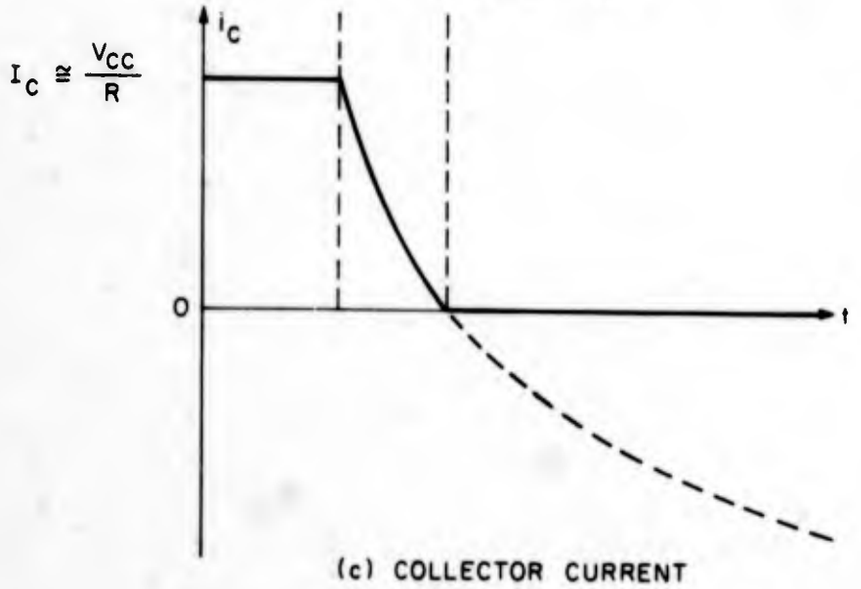
Eqn. 3.69 may now be used to examine the dynamic consequences of saturation: Consider the case of a saturated transistor in the steady state - i.e., $i_B = I_0 > \frac{I_C}{B_F}$. Figure 3.46a shows a circuit where this situation might prevail. Now assume that at t = 0, a reverse base drive of $i_B = -I_1$ is applied to the base, forcing the transistor to turn-off. While the transistor is saturated ($q_s \geq 0$) the collector current remains unchanged at $i_C \simeq \frac{Vcc}{R}$, thus the saturation transient consists of the time required to reduce q_S to zero and is visible from the collector terminal only as a delay in turn-off. At this point the transistor enters the forward-active region and charge control Eqns. 3.57 and 3.58 describe this portion of the transient.



a CIRCUIT FOR THE STUDY OF EFFECT OF SATURATION



(b) STORED CHARGE



(c) COLLECTOR CURRENT

FIG. 3.46 TRANSISTOR SATURATION

Solving Eqn. 3.67 for the stored charge yields

$$q_S = \tau_S\left(I_0 - \frac{I_C}{\beta_F}\right), \qquad t < 0$$

$$q_S = \tau_S\left[\left(I_0 - \frac{I_C}{\beta_F}\right) - \left(I_0 - \frac{I_C}{\beta_F} + I_1 + \frac{I_C}{\beta_F}\right)\left(1 - e^{-\frac{t}{\tau_S}}\right)\right], \qquad t \geq 0,\ q \geq 0. \quad (3.71)$$

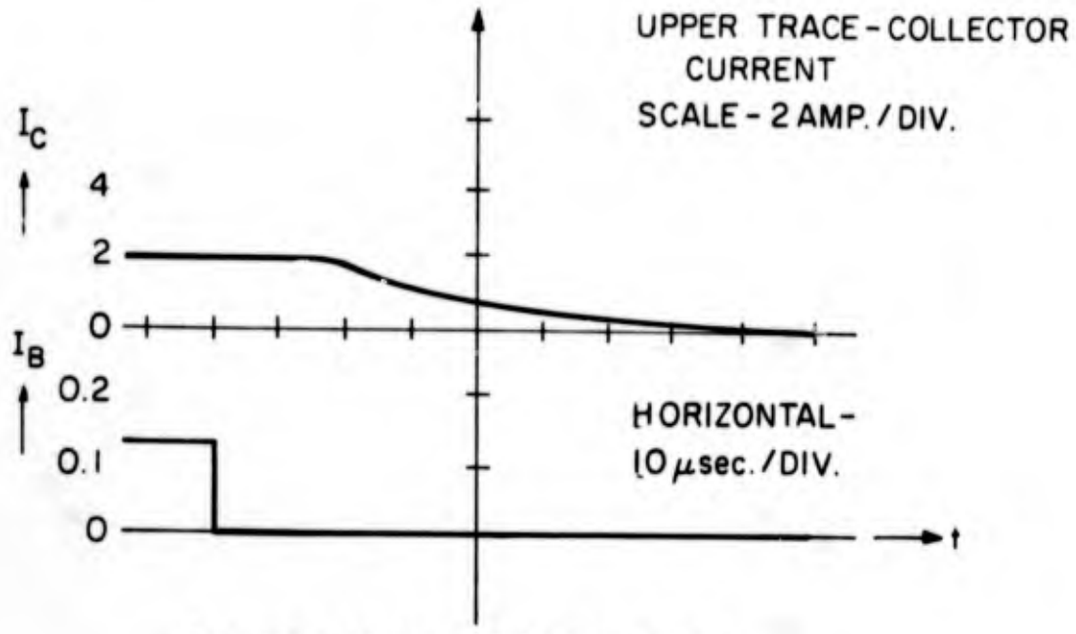
The graphical interpretation of this equation is shown in Figure 3.46b. From its initial value of $q_S = \tau_S\left(I_0 - \frac{I_C}{\beta_F}\right)$, the saturation charge decays with time constant τ_S toward the value $q_S = -\tau_S\left(I_1 + \frac{I_C}{\beta_F}\right)$. Of course when $q_S = 0$, the transistor leaves the saturated region of operation and this solution is no longer valid. The storage time interval may be calculated by solving Eqn. 3.71 for $t \equiv t_S$ with $q_F = 0$. This yields

$$t_S = \tau_S \ln\left[\frac{-I_1 + I_0}{-I_1 + \frac{I_C}{\beta_F}}\right], \quad (3.72)$$

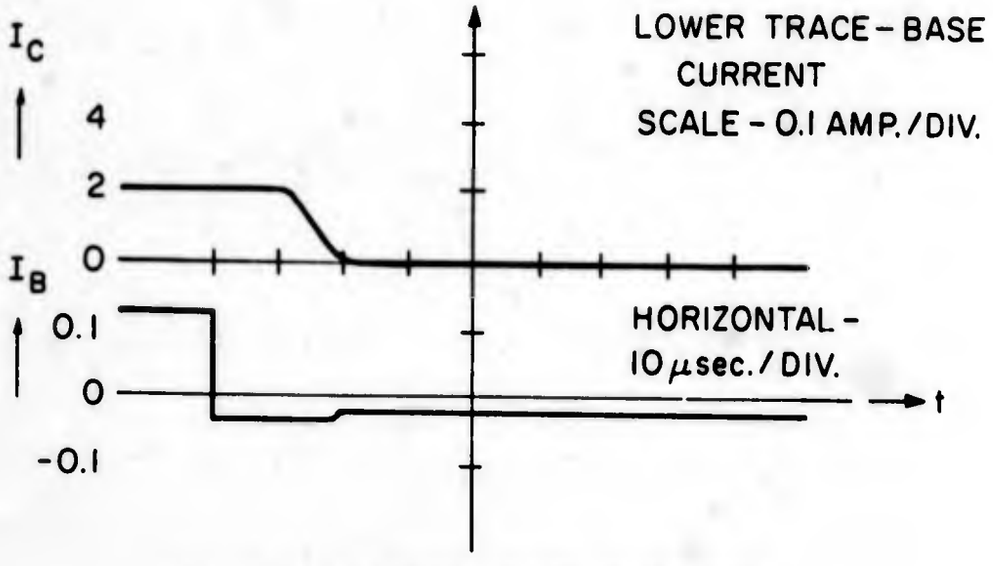
where the sign of the quantities is taken with respect to positive base current. Figure 3.46b and c show the transient charge and current waveforms for the storage and subsequent turn-off intervals.

Figure 3.47 is an oscillogram of the turn-off transient of a silicon power transistor both with and without reverse base drive. Even the small current of reverse base drive supplied shortens the total turn-off interval (storage plus current fall time) by a factor of three.

The charge control transistor model may be employed to investigate the effects of the collector to base capacitance of the collector diode junction on the collector current and voltage transient waveforms. The collector junction capacitance can be crudely modelled as a fixed external capacitor connected



(a) NO REVERSE BASE CURRENT



(b) WITH REVERSE BASE CURRENT

FIGURE 3.47

SATURATION TURN-OFF TRANSIENT OF A SILICON POWER TRANSISTOR

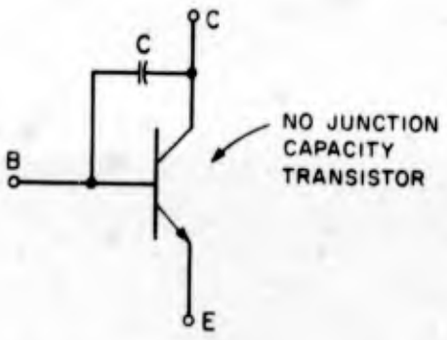


FIG. 3.48a TRANSISTOR MODEL FOR COLLECTOR JUNCTION CAPACITY

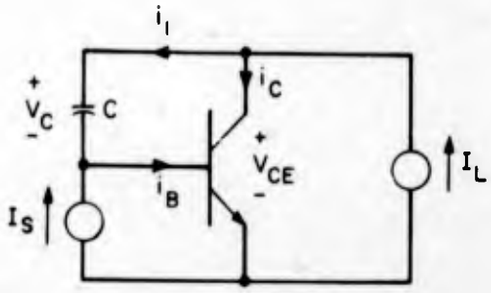


FIG. 3.48b CIRCUIT FOR INVESTIGATING EFFECTS OF COLLECTOR CAPACITY

FIG. 3.48c CAPACITOR CURRENT

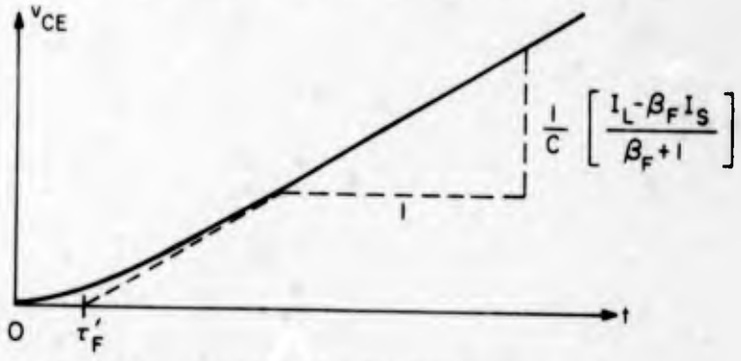


FIG. 3.48d COLLECTOR - EMITTER VOLTAGE

FIG. 3.48 VOLTAGE RISETIME WITH AN INDUCTIVE LOAD

between the collector and base terminals of the transistor as discussed in Section 3.1, and shown in Figure 3.48a. The action to be investigated involves the active turn-on or turn-off interval with a constant current collector load (e.g., on inductor). Figure 3.48b defines the parameters of interest for this example. Assuming that the transistor is in the forward-active region, as it would be during turn-off or turn-on, the capacitor volt-ampere relation may be combined with the transistor charge control equations to yield the differential equations which govern circuit operations. At the collector terminal,

$$I_L = i_1 + i_C. \tag{3.73}$$

At the base terminal,

$$i_B = i_1 + I_S. \tag{3.74}$$

Adding the charge control equations,

$$q_F = i_C \tau_F \tag{3.75}$$

$$i_B = \frac{q_F}{\tau_{BF}} + \frac{dq_F}{dt}, \tag{3.76}$$

Eqns. 3.73 to 3.76 may then be combined to yield the differential equation for capacitor current, i_1, with the result

$$\frac{di_1}{dt} + i_1 \frac{\left(1 + \frac{1}{\beta_F}\right)}{\tau_F} + \frac{I_S - \frac{I_L}{\beta_F}}{\tau_F} = 0. \tag{3.77}$$

If we study the turn-off interval from the instant the transistor comes out of the saturation, then we must seek a solution to Eqn. 3.77 with the initial condition

$$i_1|_{t=0} = 0$$

This solution is

$$i_1(t) = \frac{I_L - \beta_F I_S}{\beta_F + 1}\left[1 - e^{-\frac{1 + \frac{1}{\beta_F}}{\tau_F} t}\right] \tag{3.78}$$

To simplify Eqn. 3.78, define

$$\tau_F' \triangleq \frac{\tau_F}{1 + \frac{1}{\beta_F}} . \tag{3.79}$$

The collector-emitter voltage may be found from the capacitor volt-ampere relation:

$$V_{CE} - V_{CB} = \frac{1}{C}\int_{-\infty}^{t} i_1(t)dt. \tag{3.80}$$

Solving this relation for the turn-off transient using Eqns. 3.78 and 3.79 yields

$$V_{CE} = \frac{1}{C}\left[\frac{I_L - \beta_F I_S}{\beta_F + 1}\right]\left[t + \tau_F' \left(e^{-\frac{t}{\tau_F'}} - 1\right)\right], \tag{3.81}$$

which is sketched in Figure 3.48d for $I_L > \beta_F I_S$. The voltage will continue to rise until an external clamping circuit shunts I_L away from the transistor. During the turn-off interval, i_C is always greater than

$$i_C \geq I_L - \frac{I_L - \beta_F I_S}{\beta_F + 1} \tag{3.82}$$

and cannot fall to zero until the clamping circuit comes into action. The collector current then falls according to the forced turn-off relation, Eqn. 3.60, with $i_B = -I_s$.

Transistor Limitations

The operating limitations encountered in transistors stem from mechanisms which operate in the same manner as those encountered in diodes. The transistor effect causes the external manifestations of these limiting mechanisms to be quite different when compared to those of the diode. In addition, there are limitations which are unique to the transistor.

Collector Voltage:

The fundamental limitation on the collector-emitter voltage is the breakdown due to avalanche multiplication of the reverse-biased collector-base diode. If this diode reverse-biased volt-ampere characteristic is measured by direct collector-base measurement with the emitter terminal left open, the resultant avalanche breakdown voltage is designated V_{CBO}. In circuits, the practical maximum collector-emitter voltage is somewhat less than V_{CBO} due to β multiplication of the avalanche current. To understand this effect, we will examine V_{CEO}, the collector-emitter breakdown voltage with the base terminal left open, and relate this parameter to V_{CBO}.

Using the avalanche diode model of Figure 3.21 in conjunction with the Ebers-Moll model of Figure 3.30, an avalanche breakdown transistor model may be constructed as shown in Figure 3.49. The effect of collector diode saturation current is neglected in this model since it is small and does not appreciably effect the breakdown characteristic. Note that the <u>total</u> primary collector current, diode saturation current and current due to transistor action is multiplied by the avalanche effect. The multiplication current, $[M(V) - 1] I_C$ has exactly the same effect on the base terminal as current injected into the base. Figure 3.49 may be redrawn to show control by the base current I_B', rather than the emitter diode current, as shown in Figure 3.50.

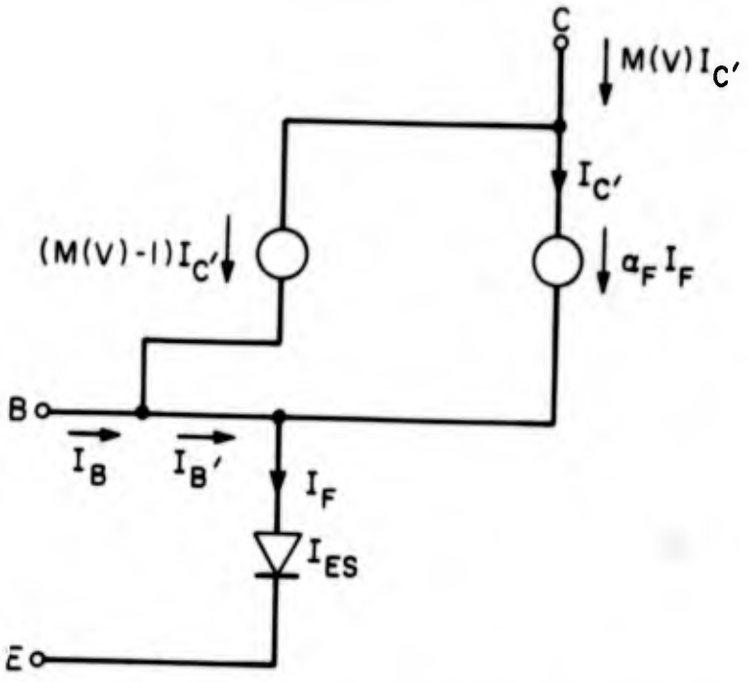


FIG.3.49 BASIC AVALANCHE BREAKDOWN TRANSISTOR MODEL

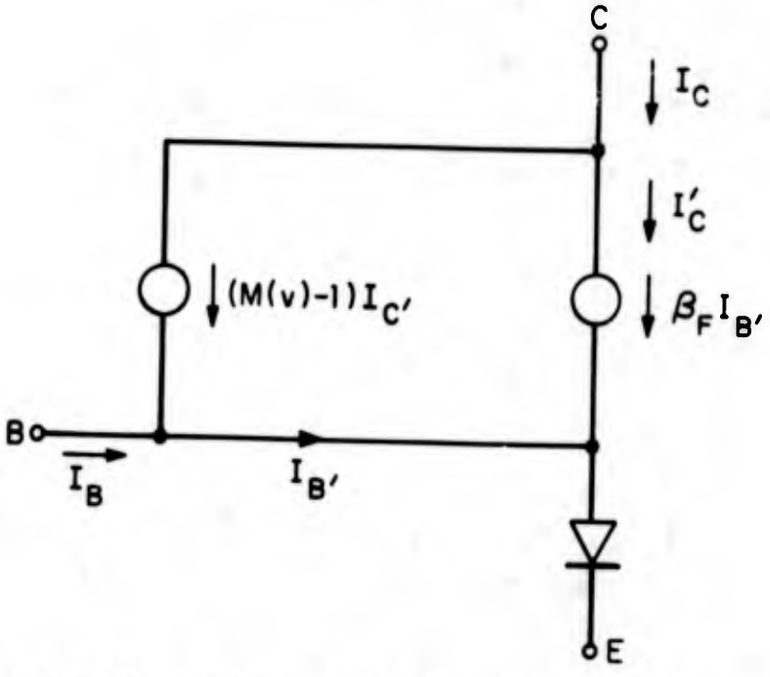


FIG.3.50 BASE CURRENT CONTROLLED AVALANCHE BREAKDOWN MODEL

From this model,

$$I_C' = \beta_F I_B' = \beta_F \{I_B + [M(V) - 1] I_C'\} \tag{3.83}$$

or

$$I_C' = \frac{I_B}{\frac{1}{\beta_F} - [M(V) - 1]} . \tag{3.84}$$

When the voltage is such that the denominator of Eqn. 3.84 is zero, or

$$M(V) = \frac{1}{\beta_F} + 1, \tag{3.85}$$

the collector current will become very large for an arbitrarily small amount of net current into the base region - this current could even be supplied by the collector diode saturation current. Since M(V) is of the form given by Eqn. 3.29 with $V_A = V_{CBO}$, Eqn. 3.85 may be rewritten as

$$\frac{1}{1 - \left(\frac{-V}{V_{CBO}}\right)^n} = \frac{1}{\beta_F} + 1,$$

which, when solved for V becomes

$$V \equiv V_{CEO} = V_{CBO}\left(\frac{1}{1 + \beta_F}\right)^{\frac{1}{n}} . \tag{3.86}$$

This indicates that the apparent breakdown voltage of the transistor, V_{CEO}, is less than V_{CBO} by a β_F dependent factor. As discussed earlier in this section, β_F decreases at very low and very high collector currents, and has a maximum at some intermediate current value. If V_{CEO} is plotted versus collector current, it will have the characteristic shape sketched in Figure 3.51. The incremental

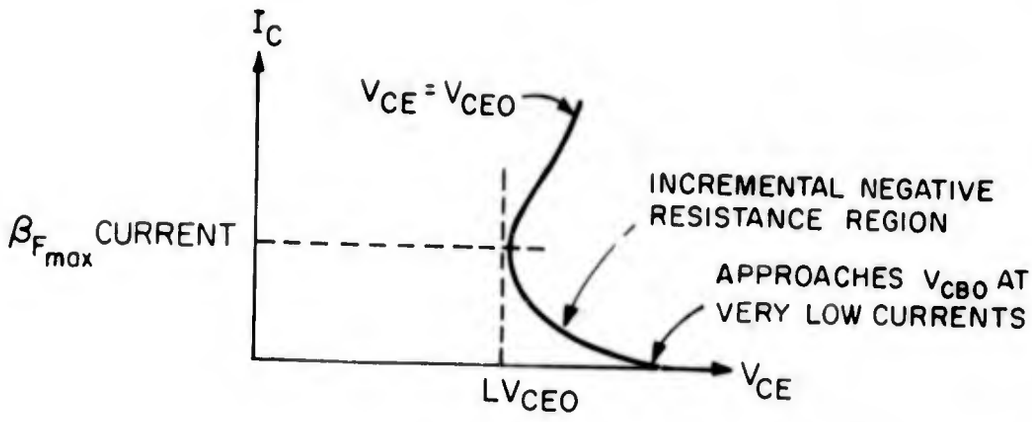


FIG. 3.51 V_{CEO} VERSUS COLLECTOR CURRENT

negative resistance region is often difficult to observe on conventional curve plotting equipment due to circuit instability encountered with stray reactances. The minimum value of V_{CEO}, which corresponds to the collector current at which β_F is maximum, is sometimes designated in the literature as LV_{CEO}, the smallest collector-emitter breakdown voltage.

Eqn. 3.84 shows that for any net positive base current, whether due to actual base current or collector multiplication, avalanche breakdown will occur at a voltage above V_{CEO}. Thus at higher voltages, the transistor must be cut off. It is difficult to design reliable power switching circuits which guarantee cut-off at voltages above any value of V_{CEO}, thus LV_{CEO} usually becomes the practical absolute maximum operating voltage for power switching transistors.

Collector Current

As is true with diodes, there are no inherent current limitations on transistors. Thermal dissipation considerations due to resistive voltage drop often limit the maximum current that a device may carry. In addition, degradation of specifications such as β_F, $V_{CE|SAT}$, and $V_{BE|SAT}$ outside of desirable limits

will encourage a manufacturer to place a maximum specification on collector current or will make use of the device at currents greater than the maximum current at which key design parameters are specified unwise. Therefore, a practical maximum current at which a device may be used is the highest current for which a minimum β_F or saturation value is specified.

Second Breakdown

The fundamental dynamic limitation of transistor operation is known as second breakdown. Because of the nature of power switching circuits, second breakdown is the most significant limitation in transistor applications. The effect has been attributed to lateral differential heating in the base region which causes collector current to concentrate in one area of the base region, causing further localized heating which leads to even more current concentration. Ultimately the silicon material in the vicinity of the concentration of current becomes hot enough to melt and fuse between the collector and emitter, causing either a collector-emitter short circuit or greatly altered β and collector-emitter breakdown characteristics. In either case, the device is permanently and irreversibly degraded.

The onset of second breakdown is dependent on collector-emitter voltage, collector current and energy that is dissipated in the transistor, and has been characterized by plots which constrain the operating point of the transistor to an area within the V_{CE} - I_C plane. The allowable operating area decreases as the time spent within the area increases. A typical "safe operating area" is reproduced in Figure 3.52. High collector-emitter voltages aggravate the conditions under which second breakdown occurs, hence the allowable current falls as the voltage increases. Because second breakdown is a dynamic effect, a transistor with a V_{CEO} and $I_{C\,MAX}$ rating may not be able to sustain these quantities simultaneously. For the transistor whose safe operating area curve appears in Figure 3.52, the V_{CEO} value of 80 volts may be accompanied by no more than 0.2 amperes of collector current. Similarly, the $I_{C\,MAX}$ current of 10. amperes may be safely achieved with no more than 67 volts appearing across the transistor. These values of voltage and current may be sustained for only very short time intervals.

When a switching transistor is turned off with a large inductive load in the collector circuit, the discussion of dynamic operation showed that this turn-off occurs at substantially constant current until the collector-emitter

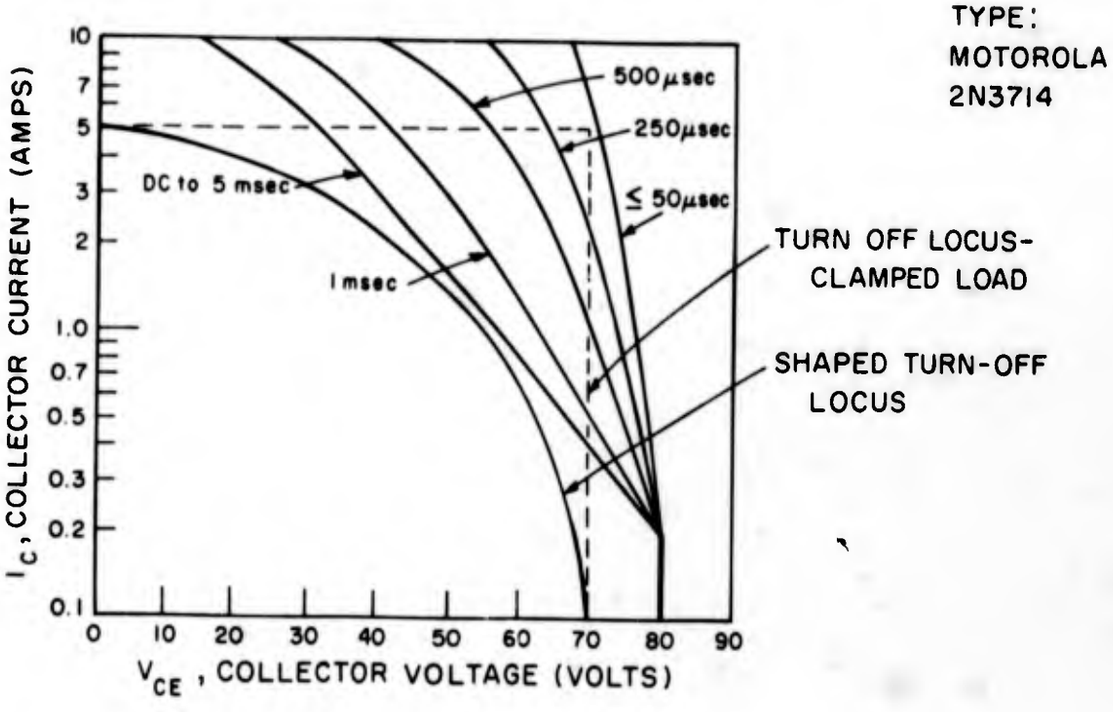


FIG.3.52 TYPICAL SAFE OPERATING AREA DATA FOR A SILICON POWER TRANSISTOR

voltage is constrained by an external clamp. Only then is the collector current allowed to fall to zero. The corresponding turn-off locus of operation is shown dotted in Figure 3.52. If a reasonable amount of forced turn-off drive is supplied to the transistor base, the device will completely turn off in a time that is less than the allowable time for the largest specified safe operating area contour which applies. Thus in switching applications where stray inductance is unavoidable, this contour sets the practical maximum values of voltage and current for which the transistor may be used; each point on the contour defines a maximum set of volt-ampere parameters for a given circuit employing this transistor. Techniques for adding elements to the load, changing its inductive nature, can result in shaping of the turn-off locus to allow the maximum value of voltage and current that appear on the contour to be utilized in the circuit (but not, of course, simultaneously). A "shaped" turn-off locus is shown in Figure 3.52.

All transistors have second-breakdown limitations, and for most power transistors these limitations fall within the area defined by V_{CEO} and $I_{C\ MAX}$. Since second breakdown is a destructive failure mode, it is imperative that safe operating area data be available and examined under worst-case circuit conditions if a device is to be successfully used in circuit application. Typically, the worst case with respect to transistor volt-ampere operating point occurs during transients applied to the circuit; these transients must be carefully analyzed to guarantee safe operation.

Temperature

The junction temperature limitations described for diodes are also applicable to transistors. Those considerations which involve power dissipation become more significant limitations in transistors because of the possibility of the device simultaneously conducting a relatively large current across a substantial voltage. In switching circuits, where the transistor is operated either saturated or cut-off, the power dissipation of the transistor is usually small when compared to the power being handled, but variations in the temperature coefficients of parameters involved in power dissipation (e.g., $V_{CE|SAT}$, $V_{BE|SAT}$) cause the power dissipated in a device to be a nonlinear function of temperature. Since the heat sink for a device is sized on the basis of the expected device dissipation regardless of the power being handled, the possibility exists for a thermal runaway condition even in a high efficiency switching circuit. To see how this might occur in a convection cooled system, refer to Figure 3.53,

which is a plot of the average generated power dissipation of a hypothetical device versus junction temperature. Superimposed on this plot is a family of heat sink cooling curves, represented by the equation

$$T_J = T_A + \theta_{JA} P_d$$

where θ_{JA} is the total junction to ambient thermal resistance. This equation is plotted for several values of ambient temperature, T_A, and represents the power removed from the device junction versus junction temperature. The intersection of these two curves is the point where power dissipated by the device equals the power removed by the heat sink - this is a possible operating point of the system. In Figure 3.53, T_{A1} is an ambient temperature in which there is only one possible operating point.

Operating point stability considerations require that if the power dissipation is changed slightly from an operating point value, the system tends to return conditions to the operating point. In other words, if the junction temperature of the device increases slightly, the power removed must be greater than the power dissipated in order to cool the device to its original temperature. Conversely, if the junction temperature is decreased, the power removed must be less than that generated to heat the device to the equilibrium temperature. Mathematically, this requirement may be stated as

$$\left.\frac{dP_R}{dT_J}\right|_{T_J = T_{eq}} > \left.\frac{dP_G}{dT_J}\right|_{T_{eq}} \qquad (3.87)$$

where P_R is the power removed by the heat sink, P_G is the power generated by the transistor and T_{eq} is the equilibrium temperature being investigated. If Eqn. 3.87 is not satisfied at the intersection of the P_R and P_G curves, then the operating point is unstable and cannot be achieved. Examination of Figure 3.53 shows that point B on the T_{A2} curve is unstable.

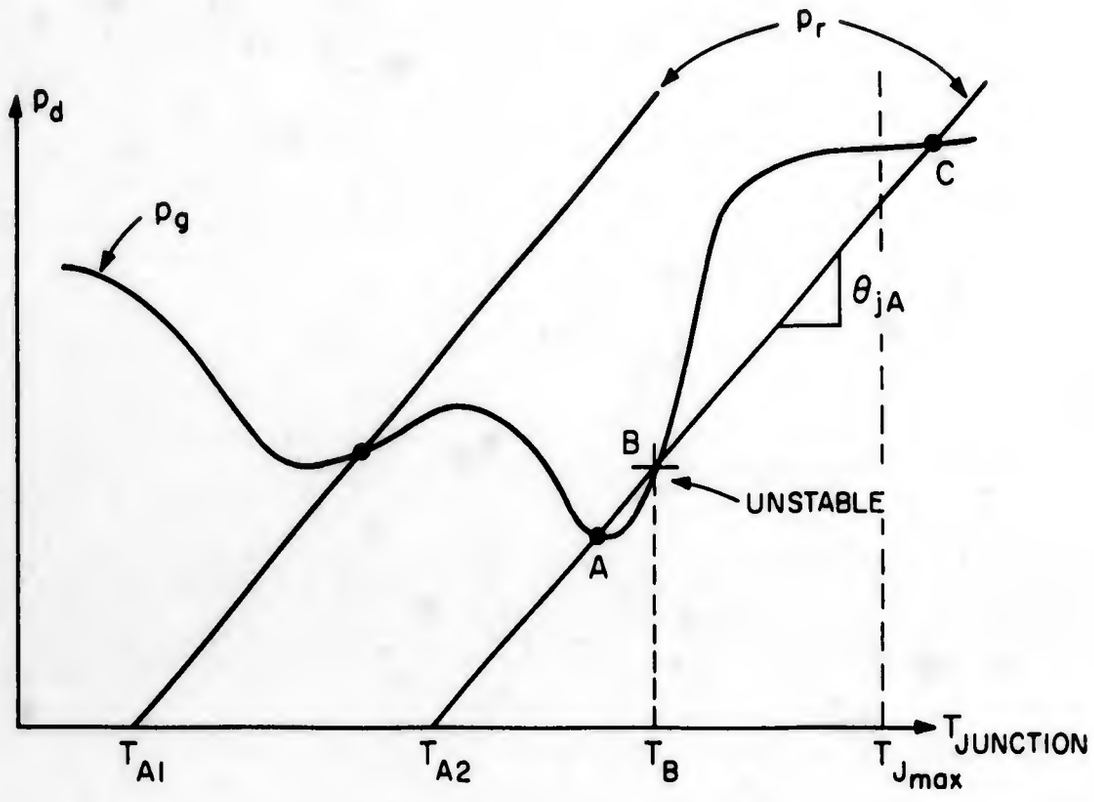


FIGURE 3.53

AVERAGE POWER GENERATED AND REMOVED VERSUS

JUNCTION TEMPERATURE

Figure 3.53 shows the average dissipation of the device. Assume that the transistor is operating with $T_A = T_{A2}$ and has established an equilibrium at point A. If a transient is encountered in normal operation, or if superimposed upon the average dissipation, there are some cyclical power variations of the type analyzed in Section 3.1, then the junction temperature may momentarily deviate from that at point A. If this temperature exceeds T_B, the stability equation predicts that operation will shift to point C and remain there. Since the junction temperature at this point exceeds the maximum allowable, device failure will follow. This example, which shows the basic mechanism of thermal runaway, indicates the importance of thermal analysis, even in high efficiency type circuits.

4. CONSIDERATIONS AT THE SCHEMATIC DIAGRAM LEVEL

In Chapter 3 terminal models for transistors and diodes were developed to account for actual device operation. In this chapter some of the circuit techniques will be examined which provide a power transistor with the base drive necessary for proper operation in a power switching output stage. First, techniques which provide the static base drive requirements will be discussed; then techniques to provide dynamic drive to speed up switching action will be presented. A practical switching output stage will be composed of some combination of these techniques to provide optimum performance under a given set of conditions.

The circuit techniques presented in this chapter form some of the basic building blocks necessary to realize practical versions of the output stages discussed in Chapter 5. When combined with realizations of the control concepts presented in Chapter 6, basic power converters are formed. By recognizing these circuit building blocks as parts of the complete output stage, very simple output stage models suitable for system analysis may be constructed from the schematic diagram of a power processor. A knowledge of the common circuit building blocks allows the segregation of a number of output stage components into functional groupings which, while necessary to proper circuit operation, are secondary to the basic power conversion process. In this manner attention may be focussed initially on the factors governing the power conversion and secondarily on the factors governing the operations of the actual device and sensing circuitry. As new circuit techniques are invented, they may be added to those included here, thus establishing a perpetual catalog of available circuit techniques. These techniques are so fundamental that they form the basis for vast numbers of different types of output stages, limited only by the ingenuity of the circuit designer. Thus a ready solution to a particular power conversion problem will not be found here: however, an approach to a specific circuit problem in switching power output stage design may be suggested by the considerations presented here.

4.1 TRANSISTOR BASE DRIVE METHODS

Resistive Drive

Resistive drive is characterized by the model drawn in Figure 4.1. When

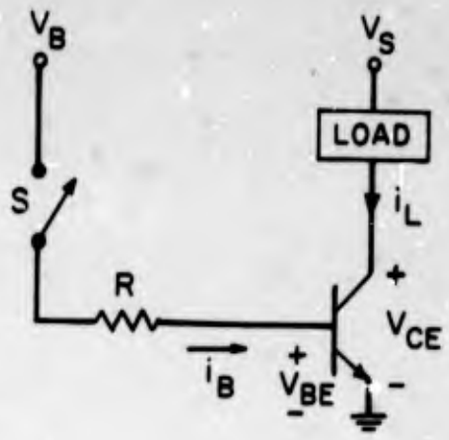


FIGURE 4.1

MODEL FOR RESISTIVE BASE DRIVE

switch S is closed, resistor R is connected to voltage source V_B. A base current

$$i_B = \frac{V_B - V_{BE}}{R} \tag{4.1}$$

flows into the base of the transistor, turning the device on. The total power drawn by the base circuitry is

$$P_{TOT\ BASE} = V_B i_B = \frac{V_B (V_B - V_{BE})}{R} \tag{4.2}$$

while the power actually dissipated in the transistor base, which is the power required to activate the device, is

$$P_{BASE} = V_{BE} i_B = \frac{V_{BE} (V_B - V_{BE})}{R} . \tag{4.3}$$

The ratio of power dissipated in the transistor base to total power delivered

to the base drive circuitry may be defined as the base circuit efficiency, η_{BASE}, and in this case is the ratio of Eqn. 4.3 to Eqn. 4.2 or

$$\eta_{BASE} = \frac{V_{BE}}{V_B} . \tag{4.4}$$

The power dissipated in the collector regions of the transistor while it is saturated is

$$P_{COLLECTOR} = V_{CE|SAT}\, i_L . \tag{4.5}$$

The total power dissipated in a transistor is the sum of Eqns. 4.3 and 4.5:

$$P_{TRANSISTOR} = \frac{V_{BE}(V_B - V_{BE})}{R} + V_{CE|SAT}\, i_L . \tag{4.6}$$

A figure of merit for a given transistor in a circuit may be derived by calculating the ratio of the minimum total transistor losses (Eqn. 4.6), which is a property of a particular transistor, to the total power required to supply these losses and drive the transistor. A figure of merit of 1.0 denotes a lossless drive circuit while a figure that approaches zero indicates a very inefficient circuit. From Eqns. 4.2 and 4.6, this figure of merit, M, for resistive drive is

$$M = \frac{\frac{V_{BE}(V_B - V_{BE})}{R} + V_{CE|SAT}\, i_L}{\frac{V_B\,(V_B - V_{BE})}{R} + V_{CE|SAT}\, i_L} \tag{4.7}$$

For example, suppose a transistor with parameters $V_{CE|SAT} = 0.5$ volts and $V_{BE} = 1.0$ volts with $i_B = 1.0$ ampere and $i_C = 10.$ amperes operates in a resistive drive circuit with $V_B = 28$ volts, $R = 28\Omega$ (to give $i_b = 1.0$ amperes).

Then:

$$\eta_{BASE} = .036$$

$$P_{TRANSISTOR} = 5.97 \text{ watts}$$

$$P_{TOTAL} = 32.0 \text{ watts}$$

$$M = 0.186.$$

This calculation shows that at high power levels resistive drive is an exceedingly inefficient means of providing base current to a transistor.

Darlington Drive

This method is one of several which improves the overall efficiency for actuating a power transistor. The basic circuit configuration is drawn in Figure 4.2. When switch S closes, base drive is supplied to transistor Q_2 through resistor R. This current is multiplied by $(\beta_2 + 1)$ of Q_2 and supplied to the base of Q_1 which, in turn, multiplies its base current by β_1. The collector voltage V_{CE} falls to the point where Q_2 saturates, thereby decreasing the base drive to Q_1 and establishing an equilibrium operating point. Q_1 operates at a collector-emitter voltage $V_{CE} = V_{BE1} + V_{CE2|SAT}$, just outside of saturation. Under these operating conditions,

$$i_{B2} = \frac{(V_B - V_{BE1} - V_{BE2})}{R} \tag{4.8}$$

$$P_{BASE\,1} = V_{BE1}\, i_{B1} = V_{BE1}\, i_{B2}\beta_{2|SAT} \tag{4.9}$$

$$P_{TOT\,BASE} = V_B\, i_{B2} \tag{4.10}$$

$$\eta_{BASE} = \frac{V_{BE1}\beta_{2|SAT}}{V_B} \tag{4.11}$$

To calculate the total power dissipated by the power transistor, the entire

collector current dropped across V_{CE} must be included, even though some of this power is dissipated in Q_2. In the absence of Q_2, the total i_L would have to be handled by Q_1, thus the losses must be charged to Q_1. This yields

$$P_{TRANSISTOR} = V_{CE}\, i_L + V_{BE1}\, i_{B2}\, \beta_{2|SAT} \tag{4.12}$$

and the figure of merit, M, based on a saturated Q_1 is

$$M = \frac{V_{CE1|SAT}\, i_L + V_{BE1}\, \beta_{2|SAT} \dfrac{(V_B - V_{BE1} - V_{BE2})}{R}}{(V_{CE2|SAT} + V_{BE1})\, i_L + V_B \dfrac{(V_B - V_{BE1} - V_{BE2})}{R}} \tag{4.13}$$

Consider the previous example with the transistor parameters applying to Q_1. In addition, assume that the parameters of Q_2 are $V_{CE2|SAT} = 0.5$ volts and $V_{BE2} = 1.0$ volts at $i_{C2} = 1.0$ ampere and $i_{b2} = 0.1$ amperes, so that $\beta_{2|SAT} = 10$, and let R = 280 ohms. Then

$$\eta_{BASE} = .36$$

$$P_{TRANSISTOR} = 16.0 \text{ watts}$$

$$P_{TOTAL} = 17.6 \text{ watts}$$

$$M = .34$$

This example indicates that even though the power transistor dissipates more power than with resistive drive, the overall power dissipated in generating the drive is less, hence the figure of merit for the Darlington drive circuit is higher. Even with the increase in overall efficiency, the M figure indicates that two-thirds of the power dissipated is not contributing to useful transistor drive.

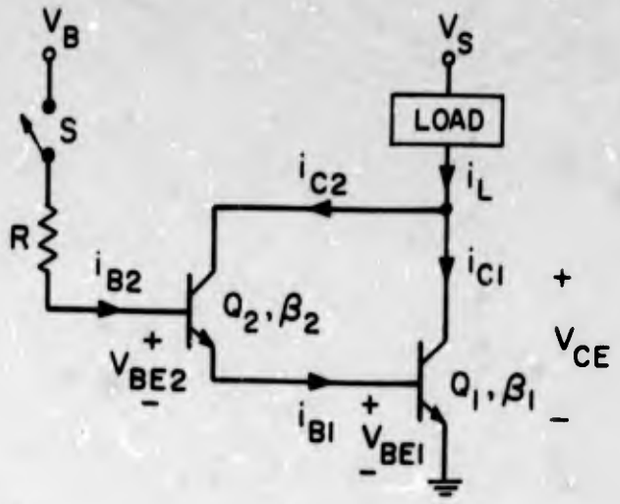


FIGURE 4.2

DARLINGTON DRIVE CIRCUIT MODEL

The merits of resistive versus Darlington base drive with variations of V_B may be assessed by examining the ratios of P_{TOTAL} for resistive to P_{TOTAL} for Darlington drive. This ratio, defined as K, is

$$K = \frac{V_B i_{B1} + V_{CE1|SAT} i_L}{V_B i_{B2} + (V_{CE2|SAT} + V_{BE1})\, i_L} \quad . \tag{4.14}$$

For the device parameters given in this example, R must be adjusted for each value of V_B to give the required base current. This can be accomplished analytically by setting the i_B terms in Eqn. 4.14 to constants. For the example presented here, $i_{B1} = 1.0$ ampere and $i_{B2} = 0.1$ ampere. Eqn. 4.14 is plotted in Figure 4.3 versus V_B with the same parameters used in the examples. $K < 1.0$ implies that resistive drive affords less dissipation; $K > 1.0$ favors Darlington type drive. Figure 4.3 indicates that 10 volts is roughly the crossover point of K in this example. For most commonly encountered transistor parameters, this crossover lies between 5 and 15 volts. For any particular case, Eqn. 4.14 may be used to optimally select between these two drive schemes.

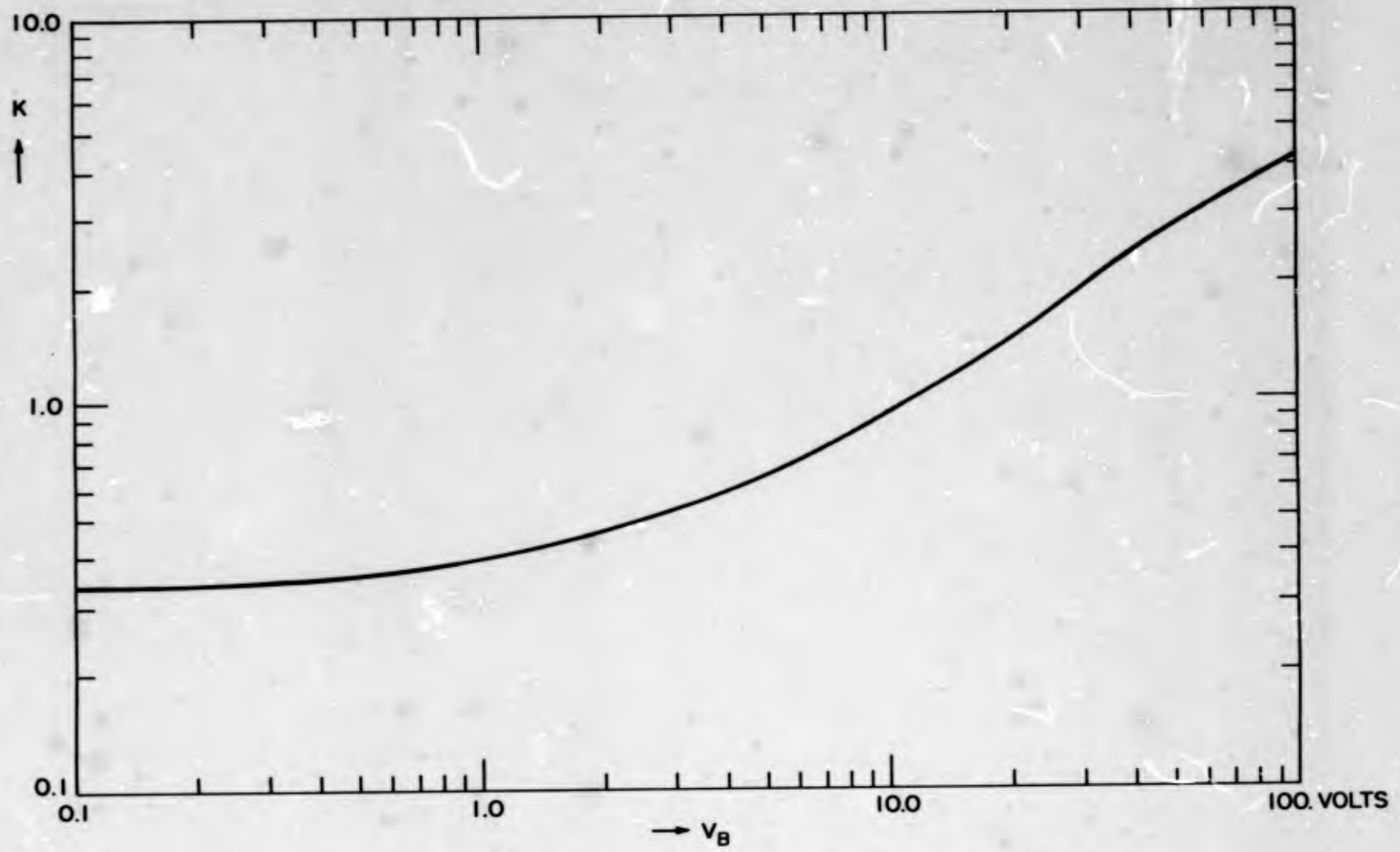


FIG. 4.3 POWER EFFICIENCY OF RESISTIVE VERSUS DARLINGTON DRIVE

Transformer Drive

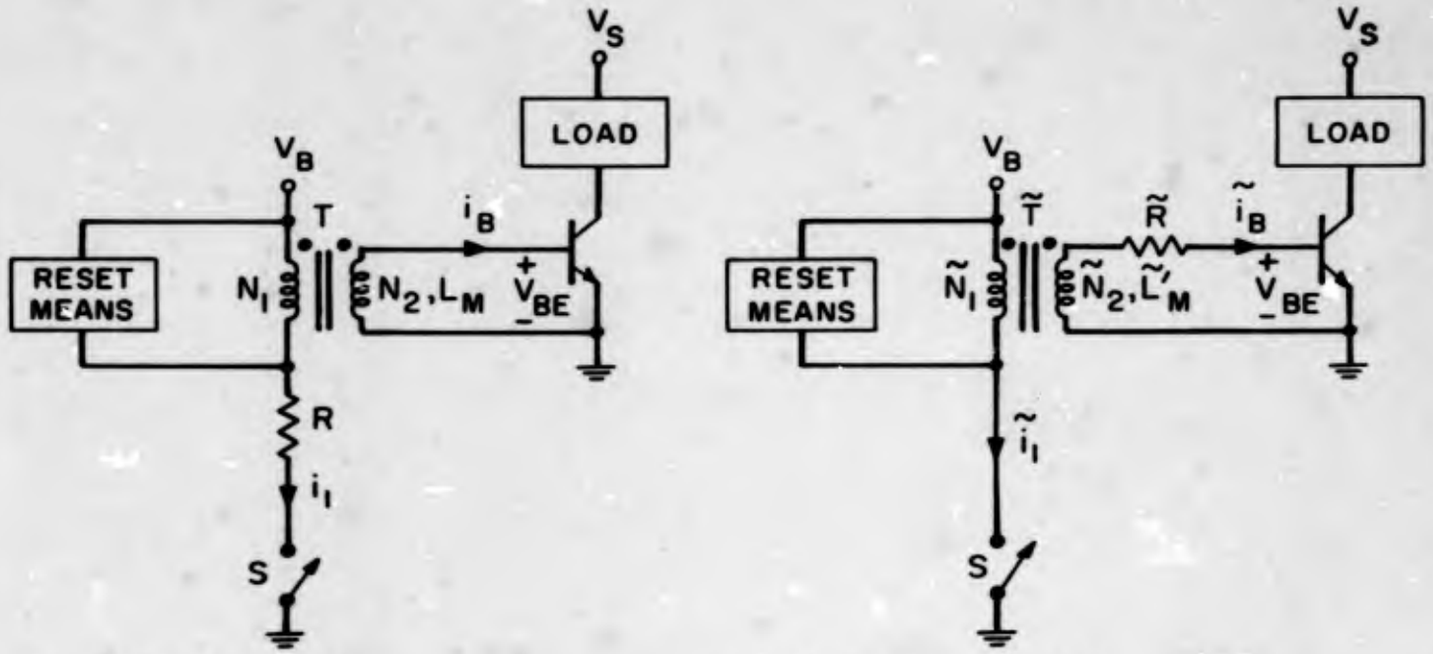
The inefficiency of the resistive and Darlington base drive methods occur because of the mismatch between the base supply voltage V_B and the base-emitter voltage V_{BE} of a transistor. One method of minimizing this disparity is to use a matching transformer between the base voltage source and the transistor base. Figure 4.4 illustrates two methods of transformer drive. In the circuit of Figure 4.4a, when S closes V_B is applied across the series combination of the primary of transformer T and resistor R; in Figure 4.4b, V_B is applied wholly across $\tilde{T}$. How these circuits act to provide activating base power may by understood by referring to the models of the circuits of Figure 4.4 that are valid when S is closed, as shown in Figure 4.5. Here we have assumed that the transformers are ideal; i.e., there is no significant leakage inductance between the N_1 and N_2 windings, and the resistance of these windings and losses in the transformer core are negligible. The models have been formed by reflecting the elements on the primary side of the transformer to the secondary, and the primes denote the elements that have been reflected.

Since the magnetizing inductance of the transformer, L_M, is a dynamic element, the base drive to the transistor is time varying. In Figure 4.5a, V_{BE} is approximately constant, so i_M will be a ramp of current and i_1' will be constant, with this current splitting between the transformer magnetizing inductance L_M and the transistor base. From the figure,

$$i_1' = \frac{V_B' - V_{BE}}{R'} = \frac{V_B\left(\frac{N_2}{N_1}\right) - V_{BE}}{R\left(\frac{N_2}{N_1}\right)^2}, \qquad (4.15)$$

and

$$i_M(t) = i_M(0) + \frac{V_{BE}}{L_M}\, t \qquad (4.16)$$

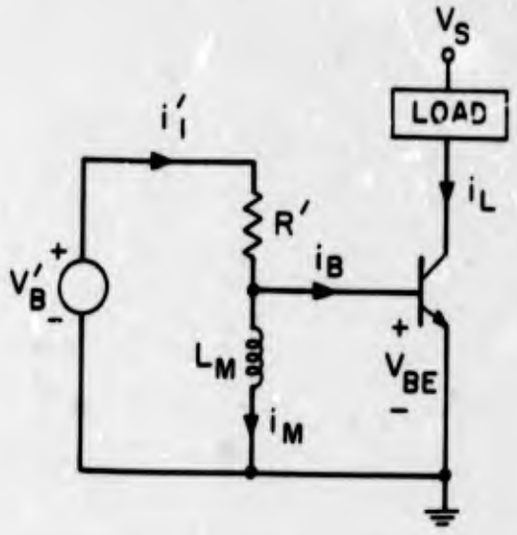


a) Resistor in Primary

b) Resistor in Secondary

FIGURE 4.4

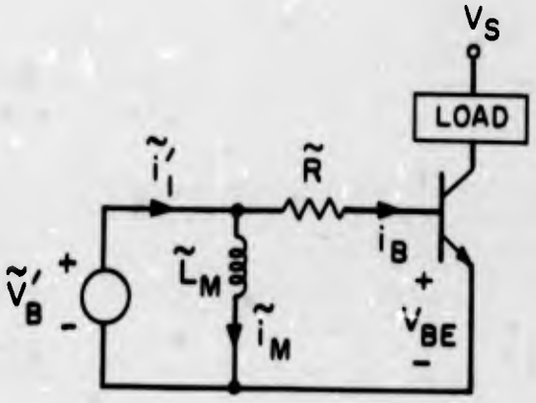
TRANSFORMER DRIVE SCHEME



$$V_B' = V_B\left(\frac{N_2}{N_1}\right)$$

$$R' = R\left(\frac{N_2}{N_1}\right)^2$$

a) Model of Resistor in Primary Circuit



$$\tilde{V}_B' = V_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right)$$

b) Model of Resistor in Secondary Circuit

FIGURE 4.5

MODELS OF CIRCUITS OF FIGURE 4.4 WITH S CLOSED

where $i_M(0)$ is the current that remains flowing in L_M when switch S is initially closed at t = 0. The base current is the difference between Eqns. 4.15 and 4.16;

$$i_B(t) = \frac{V_B\left(\frac{N_2}{N_1}\right) - V_{BE}}{R\left(\frac{N_2}{N_1}\right)^2} - i_M(0) - \frac{V_{BE}}{L_M}\,t \geq \frac{i_L}{\beta\,|\,SAT} \,. \qquad (4.17)$$

The available base current decreases linearly with time, but the inequality of Eqn. 4.17 must be satisfied at all times. Thus, when switch S initially closes an excess amount of base current must be provided in order to insure that there will be sufficient base current at $t = T_{ON}$, the end of the switch closure period, to satisfy Eqn. 4.17. This excess base current is essentially wasted power, since it is not necessary to maintain transistor saturation.

At T_{ON}, switch S opens and i_1 goes to zero. However, the current in L_M continues to flow, as this represents energy stored in inductance L_M. Some means must be provided during the off time of S to reduce this stored energy in order to prevent L_M from accumulating energy and eventually magnetically saturating on successive switching cycles. The process of reducing the stored energy and/or controlling the level of remnant flux in the core will be referred to as "resetting" of the transformer. Although Eqn. 4.17 indicates that all of the energy need not be removed from L_M [$i_M(0) = 0$] before S is reclosed, any remaining energy [$i_M(0) > 0$] subtracts from the available base current, placing more stringent requirments on the drive circuit. We will assume that all of the energy stored in L_M is removed before S is reclosed. Several methods are available for removing this energy, one of which is shown in Figure 4.6. When S is closed, diode D is reverse biased and the reset zener diode D_Z does not effect circuit operation. When S is opened, magnetizing current flows through D and D_Z which absorbs and dissipates the stored energy across the zener diode breakdown voltage, V_Z. With this method, all of the stored energy is dissipated in D_Z. Other reset methods are available which recover this energy by returning it to the supply. The reset conditions presented here apply primarily to inductors made with linear magnetic systems. If the system used has an appreciable amount of magnetic hysteresis, the reset circuit must also return the remnant flux level in the magnetic material to a controlled level. A discussion of various

reset methods for accomplishing these functions and the trade-offs governing their selection may be found in "Two State Modulation Techniques for Power Systems", Report No. ECOM-02282-3, by T. A. Froeschle. To evaluate the figure of merit for these circuits, two cases will be examined - one in which all of the stored energy is dissipated, and a second in which the energy is completely returned to the supply.

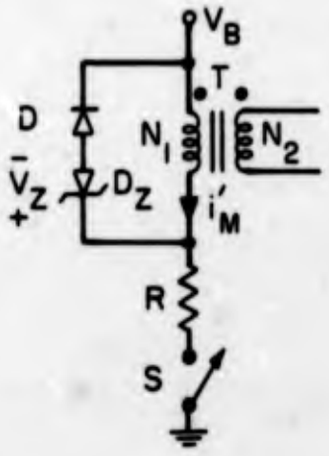


FIGURE 4.6

A METHOD OF RESETTING T

The reset action sets a certain minimum time during which S must be off. If the reset occurs with a fixed voltage across T, as in Figure 4.6, and reset is complete each cycle, then the minimum "off" time for volt-second balance across the transformer is

$$T_{RESET} = \frac{V_{BE}}{V_z}\left(\frac{N_1}{N_2}\right) T_{ON} \tag{4.18}$$

From Eqn. 4.18 the maximum duty cycle $D = \frac{T_{ON}}{T_{ON} + T_{RESET}}$ that may be achieved with transformer drive may be derived as

$$D_{MAX} = \frac{1}{1 + \frac{V_{BE}}{V_z}\left(\frac{N_1}{N_2}\right)} . \tag{4.19}$$

This equation indicates that transformer drive is not a static method of obtaining base drive; operation of the circuit must guarantee that the D_{MAX} constraint is observed. In addition, any practical transformer is limited in the total flux that can be supported by the core material, necessitating an operating constraint on the total volt-seconds that can be accumulated across the transformer during any one "on" time.

The power dissipated in the base circuit may be calculated from Figure 4.5a and Eqn. 4.15. This consists of power dissipated in the base drive resistor and the transistor base itself, and may be expressed as

$$P_{TOT\ BASE}(t) = \frac{V_B\left(V_B - \frac{N_1}{N_2} V_{BE}\right)}{R} - \frac{V_{BE}^2}{L_M} t \qquad (4.20)$$

The second term in Eqn. 4.20 is the rate of change of energy stored in L_M. Since the power dissipated by the drive circuit is time dependent during the switch "on" time, it is necessary to evaluate the average power dissipated during this time to allow a meaningful comparison with the static drive methods. If all of the energy stored in L_M is dissipated during reset, then the power supplied to L_M during the "on" time must be charged as power dissipated; in this case, the second term in Eqn. 4.20 must be neglected. The current required by the base is the minimum value of available base current, which may be found from Eqn. 4.17 at $t = T_{ON\ max}$ and is

$$i_{B\ min} = \frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}}{L_M} T_{ON\ max} \qquad (4.21)$$

and the corresponding base power is

$$P_{BASE\ min} = V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2}{L_M} T_{ON\ max} \qquad (4.22)$$

which is the minimum base power necessary to operate the transistor. The ratio of Eqn. 4.22 to Eqn. 4.20 with the second term neglected is the base circuit efficiency,

$$\eta_{BASE} = \left(\frac{V_{BE}}{V_B}\right)\left(\frac{N_1}{N_2}\right)\left[1 - \frac{\left(\frac{R\,T_{ON}}{L_M}\right)}{\frac{1}{\left(\frac{V_{BE}}{V_B}\right)\left(\frac{N_2}{N_1}\right)} - 1}\right] \tag{4.23}$$

Using Eqns. 4.21 and 4.22, the figure of merit for transformer drive with total energy dissipation may be expressed as

$$M = \frac{V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2}{L_M} T_{ON\,max} + V_{CE|SAT}\, t_L}{\frac{V_B\left[V_B - V_{BE}\left(\frac{N_1}{N_2}\right)\right]}{R} + V_{CE|SAT}\, t_L}. \tag{4.24}$$

If all of the energy stored in L_M is returned to the supply with no losses, then the average base power drawn is the power drawn according to Eqn. 4.20 averaged over $0 < t < T_{ON}$ or

$$\langle P_{TOT\,BASE} \rangle = \frac{V_B\left(V_B - \frac{N_1}{N_2} V_{BE}\right)}{R} - \frac{V_{BE}^2 T_{ON}}{2 L_M} \tag{4.25}$$

In this case, the base circuit efficiency is given by

$$\eta_{BASE} = \frac{V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2 T_{ON\,max}}{L_M}}{V_B\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right] - \frac{V_{BE}^2 T_{ON}}{2 L_M}} . \qquad (4.26)$$

and the corresponding figure of merit is

$$M = \frac{V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2 T_{ON\,max}}{L_M} + V_{CE|SAT}\, i_L}{V_B\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right] - \frac{V_{BE}^2 T_{ON}}{2 L_M} + V_{CE|SAT}\, i_L} . \qquad (4.27)$$

In both Eqns. 4.24 and 4.27, if the collector saturation losses are large when compared to the total base drive power, the figure of merit approaches 1.0. Low base drive power can be achieved by choosing the turns ratio $\frac{N_1}{N_2}$ on T so that V_B' in Figure 4.5a nearly equals V_{BE}, and winding the transformer such that $\frac{T_{ON}}{L_M}$ is minimized (high L_M). With R' chosen to give the minimum required base current at $t = T_{ON\,max}$, these steps will minimize $P_{TOT\,BASE}$. Unfortunately, if there are any variations in V_B or V_{BE} (due to junction temperature variations, for example), the base current will vary wildly, since it is determined by the difference between V_B' and V_{BE}, which has been made small by design, and under these circumstances the figure of merit may become very small or, worse yet, insufficient base current drive will be available under the

worst case conditions. For these reasons, the design of transformer drive circuitry must be a compromise between efficiency and control of base current in the face of fluctuation of circuit variables.

Using this same approach, the resistor in secondary transformer drive scheme of Figure 4.4b modelled in Figure 4.5b may be evaluated. With the notation in Figures 4.4b and 4.5b, we have

$$i_B = \frac{\tilde{V}'_B}{\tilde{R}} \tag{4.28}$$

and

$$i_M(t) = \frac{\tilde{V}'_B}{\tilde{L}_M} t + \tilde{I}_M(0). \tag{4.29}$$

Assuming complete reset each switching cycle,

$$\tilde{I}'_1(t) = \left(\tilde{V}_B - V_{BE}\right)\left(\frac{1}{\tilde{R}} + \frac{t}{\tilde{L}_M}\right) \tag{4.30}$$

With this scheme, the available base current (Eqn. 4.28) is constant, whereas in Eqn. 4.17, resistor in primary, this current decreases linearly with time. The total base power drawn is

$$P_{TOT\ BASE}(t) = \tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right)\left[\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}\right]\left(\frac{1}{\tilde{R}} + \frac{t}{\tilde{L}_M}\right). \tag{4.31}$$

The first term in this equation represents power dissipated; the second is the rate of change of energy in L_M. If all of this energy is returned to the supply during reset, then the second term in Eqn. 4.31 is neglected. The base circuit efficiency is expressed by

$$\eta_{BASE} = \frac{V_{BE}}{\tilde{V}_B}\left(\frac{\tilde{N}_1}{\tilde{N}_2}\right) \tag{4.32}$$

and the figure of merit is

$$M = \frac{V_{BE}\left[\frac{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}}{\tilde{R}}\right] + V_{CE|SAT}\, i_L}{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right)\left[\frac{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}}{\tilde{R}}\right] + V_{CE|SAT}\, i_L} \tag{4.33}$$

If the energy stored in the magnetizing inductance is dissipated, the average power drawn from the supply during the "on" time may be used to account for this loss. In this case,

$$\eta_{BASE} = \frac{V_{BE}\left[\frac{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}}{\tilde{R}}\right]}{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right)\left[\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}\right]\left[\frac{1}{\tilde{R}} + \frac{T_{ON}}{2\,\tilde{L}_M}\right]} \tag{4.34}$$

and

$$M = \frac{V_{BE}\left[\frac{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}}{\tilde{R}}\right] + V_{CE|SAT}\, i_L}{\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right)\left[\tilde{V}_B\left(\frac{\tilde{N}_2}{\tilde{N}_1}\right) - V_{BE}\right]\left[\frac{1}{\tilde{R}} + \frac{T_{ON}}{2\,\tilde{L}_M}\right] + V_{CE|SAT}\, i_L} . \tag{4.35}$$

The principal differences between the two schemes of transformer drive lie in the manner in which the transformer affects circuit operation. With the resistor in the secondary, the available base current is time independent. However, the transformer is placed across the full base voltage supply during the "on" time as opposed to the resistor in primary circuit which places the transformer primary

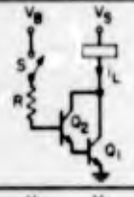
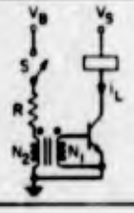
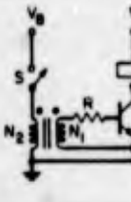
across the reflected base-emitter voltage, which is always smaller than V_B. This means that the flux capability, hence size, must be greater for the resistor in secondary transformer. In both cases, to insure safe circuit operation the transformer must be protected from conditions which would lead to transformer saturation or, in the case of resistor in primary, saturation must be controlled in a manner which will guarantee safe turn-off of the power transistors.

The base efficiency, η_{BASE}, and the figure of merit, M, for all of the circuits that have been discussed here are summarized in Table 4.1. Selection of one of these schemes would include a comparison of other factors which are dependent on a particular application and parameters of a specific design such as cost, size and weight, effects of circuit variable fluctuations and duty cycle requirements. A complete discussion of these factors is beyond the scope of this report; the relations given in Table 4.1 apply to considerations of power efficiency which is one of the major selection criterion in high efficiency power handling circuits.

The transformer coupled circuits of Figure 4.5 can be used only if the "on" time and duty cycle of the output switches is well constrained. For applications where this is not so, two transformer drive circuits may be used in a "push-pull" arrangement, as shown in Figure 4.7 for a resistor in secondary circuit. During the power transistor "on" time, switches S_1 and S_2 are operated alternately with a switch closed time compatible with the volt-second capability of the transformer. During the interval when S_1 is closed and S_2 open, base drive is delivered to Q_1 via transformer T_1 while transformer T_2 is resetting across the zener diode voltage V_z. With S_1 closed and S_2 open, the opposite action takes place. If the switches are operated at 50% duty cycle during the Q_1 "on" time, then V_z need only be greater than V_B to guarantee proper reset for any Q_1 duty cycle. The power efficiency of this configuration may be evaluated from the appropriate column of Table 4.1 by replacing V_{BE} in the denominator of all expressions with $V_{BE} + V_D$ which accounts for the extra series diode drop. During the "off" time of Q_1 both switches are left open, both transformers reset, and the circuit is at rest. Naturally, the "push-pull" arrangement may be used with any of the other transformer drive variations.

Table 4.1

EFFICIENCY COMPARISON OF DRIVE METHODS

	Configuration	η_{BASE}	M
Resistor		$\frac{V_{BE}}{V_B}$	$\frac{\frac{V_{BE}(V_B - V_{BE})}{R} + V_{CE\|SAT}\, I_L}{\frac{V_B(V_B - V_{BE})}{R} + V_{CE\|SAT}\, I_L}$
Darlington		$\frac{V_{BE1}\beta_{2\|SAT}}{V_B}$	$\frac{I_L \cdot V_{BE1}\beta_{2\|SAT}\frac{(V_B - V_{BE1} - V_{BE2})}{R}}{(V_{CE2\|SAT} + V_{BE1})I_L + V_B\frac{(V_B - V_{BE1} - V_{BE2})}{R}}$
Transformer Drive Resistor in Primary Stored Energy Recovered		$\frac{V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2 T_{ON\ MAX}}{L_M}}{V_B\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right] - \frac{V_{BE}^2 T_{ON}}{2L_M}}$	$\frac{V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2 T_{ON\ MAX}}{L_M} + V_{CE\|SAT}\, I_L}{V_B\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right] - \frac{V_{BE}^2 T_{ON}}{2L_M} + V_{CE\|SAT}\, I_L}$
Transformer Drive Resistor in Primary Stored Energy Lost		$\left(\frac{V_{BE}}{V_B}\right)\left(\frac{N_1}{N_2}\right)\left[1 - \frac{\left(\frac{R\, T_{ON}}{L_M}\right)}{\frac{1}{\left(\frac{V_{BE}}{V_B}\right)\left(\frac{N_2}{N_1}\right)} - 1}\right]$	$\frac{V_{BE}\left[\frac{V_B - V_{BE}\left(\frac{N_1}{N_2}\right)}{R}\right]\left(\frac{N_1}{N_2}\right) - \frac{V_{BE}^2}{L_M} T_{ON\ MAX} + V_{CE\|SAT}\, I_L}{\frac{V_B\left[V_B - V_{BE}\left(\frac{N_1}{N_2}\right)\right]}{R} + V_{CE\|SAT}\, I_L}$
Transformer Drive Resistor in Secondary Stored Energy Recovered		$\frac{V_{BE}}{V_B}\left(\frac{N_1}{N_2}\right)$	$\frac{\frac{V_{BE}\left[V_B\left(\frac{N_2}{N_1}\right) - V_{BE}\right]}{R} + V_{CE\|SAT}\, I_L}{\frac{V_B\left(\frac{N_2}{N_1}\right)\left[V_B\left(\frac{N_2}{N_1}\right) - V_{BE}\right]}{R} + V_{CE\|SAT} I_L}$
Transformer Drive Resistor in Secondary Stored Energy Lost		$\frac{V_{BE}\left[V_B\left(\frac{N_2}{N_1}\right) - V_{BE}\right]}{R}$ / $V_B\left(\frac{N_2}{N_1}\right)\left[V_B\left(\frac{N_2}{N_1}\right) - V_{BE}\right]\left[\frac{1}{R} + \frac{T_{ON}}{2L_M}\right]$	$\frac{V_{BE}\left[V_B\left(\frac{N_2}{N_1}\right) - V_{BE}\right]}{R} + V_{CE\|SAT}\, I_L$ / $V_B\left(\frac{N_2}{N_1}\right)\left[V_B\left(\frac{N_2}{N_1}\right) - V_{BE}\right]\left[\frac{1}{R} + \frac{T_{ON}}{2L_M}\right] + V_{CE\|SAT}\, I_L$
Current Feedback Stored Energy Recovered		$\frac{I_L\left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M} T_{ON}}{I_L\left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}\frac{T_{ON}}{2}}$	$\frac{V_{BE}\left[I_L\left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M} T_{ON}\right] + V_{CE\|SAT}\, I_L}{V_{BE}\left[I_L\left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}\frac{T_{ON}}{2}\right] + V_{CE\|SAT}\, I_L}$
Current Feedback Stored Energy Lost		$\frac{I_L\left(\frac{N_2}{N_1}\right)\frac{V_{BE}}{L_M} T_{ON}}{I_L\left(\frac{N_2}{N_1}\right)}$	$\frac{V_{BE}\left[I_L\left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M} T_{ON}\right] + V_{CE\|SAT}\, I_L}{\left[V_{BE}\left(\frac{N_2}{N_1}\right) + V_{CE\|SAT}\right] I_L}$

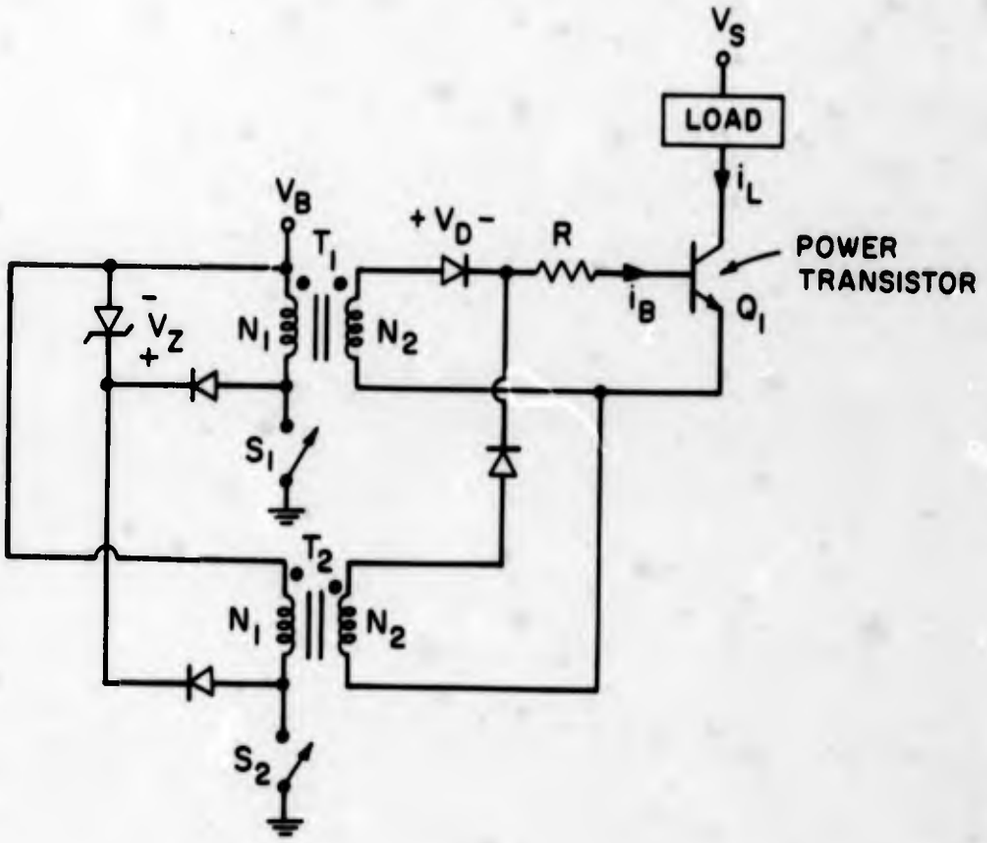


FIGURE 4.7

"PUSH-PULL" TRANSFORMER DRIVE

Voltage Feedback

A variation of the transformer drive schemes involves the use of positive feedback of the voltage in parallel with the load to provide base current for the power switch. One transformer drive scheme employing a resistor in the secondary is shown in Figure 4.8. It is apparent that when power transistor Q_1 in "on", the circuit is equivalent to that of Figure 4.4b with

$$V_B = V_s - V_{CE|SAT}.$$

Since the feedback which holds the transistor "on" is positive, to switch the state of the drive circuit the loop must either be broken or overridden by an external current. The loop may be broken by a switch in series with either the primary or secondary of T or by saturation of this transformer. The base drive may be overridden by removing a current i from the base current supplied by feedback,

$$|i| \geq \frac{\left[V_s - V_{CE|SAT}\right]\left(\frac{N_2}{N_1}\right) - V_{BE}}{R} \quad . \tag{4.36}$$

During the off time, some means must be found for resetting T without disturbing the load. A diode in series with the load in the positive current direction will allow unconstrained reset and may be used if the additional losses of this series diode are not a serious penalty.

A familiar example of voltage feedback in a push-pull configuration is the dc converter or "chopper" drawn in Figure 4.9. This circuit relies on saturation of T to cause switching action. In this example, the magnetizing current is not wasted, but is used to turn on the opposite transistor after T saturates and the first transistor turns off. The duty cycle for each transistor is 50% and the "on" time is controlled by the volt-second capability of T. One serious disadvantage of this circuit is that when T saturates, the power transistor that is on must come out of saturation to collapse the voltage across T before turn-off can begin. Thus, a large, uncontrolled "spike" of current will flow in the power transistor before it turns off, which could lead to a decrease in the lifetime of the device. For high power circuits, two transformers are generally used in parallel; one is a linear power transformer which couples the load to the transistor switches, the second is a small saturable transformer with a resistor

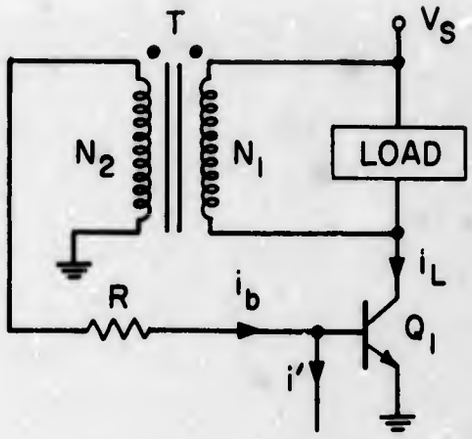


FIGURE 4.8

VOLTAGE FEEDBACK DRIVE CIRCUIT

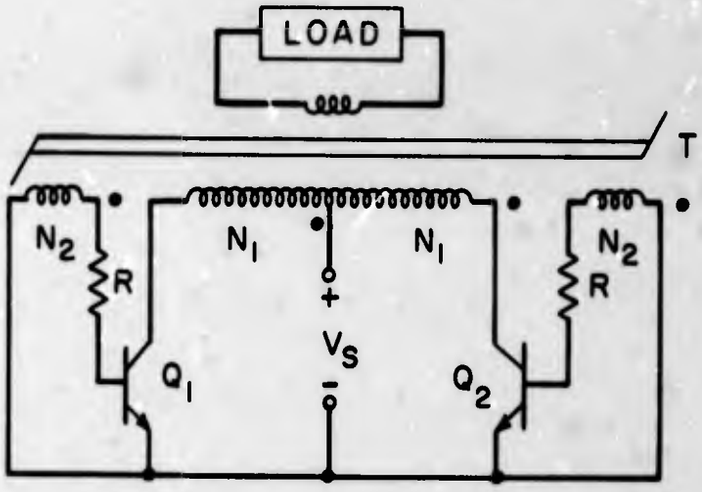


FIGURE 4.9

PUSH-PULL "CHOPPER" CIRCUIT

in series with the primary which provides the voltage feedback drive. When the transformer saturates, the primary current is limited by the resistor to a safe value until the transistor can turn off.

Current Feedback

Another scheme for transformer drive using feedback of the collector current utilizes a drive transformer in series with the load which forces a fraction of the load current through the base in a positive feedback arrangement. An example of this scheme is shown in Figure 4.10. If the current in the magnetizing inductance of T as seen from the primary is small when compared to i_L, then

$$i_B \simeq \frac{N_2}{N_1} i_L, \tag{4.37}$$

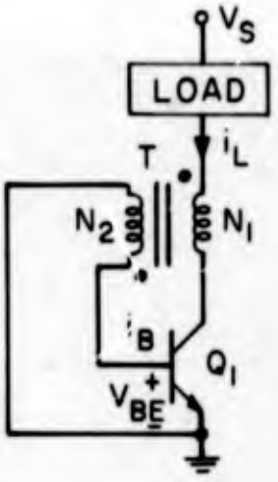
i.e., the base current is a fixed fraction of the collector current which is dependent only on the turns ratio $\frac{N_1}{N_2}$ of T. This is exactly the requirement to meet a given forced β specification of a transistor, and this forced β is provided at any collector current level. The circuit may be analyzed in more detail by referring to the model drawn in Figure 4.10b. If Q_1 is turned on at $t = 0$, then

$$i_M(t) = \frac{V_{BE}}{L_M} t + i_M(0) \tag{4.38}$$

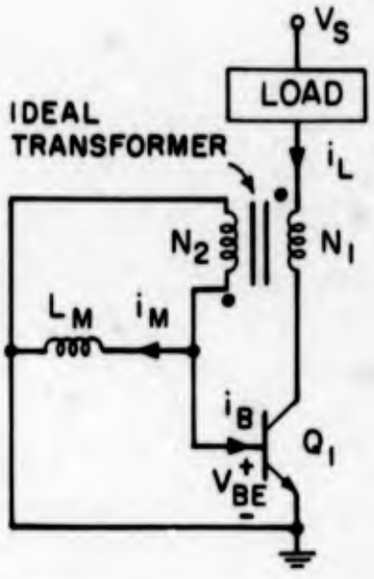
and

$$i_B(t) = i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M} t - i_M(0). \tag{4.39}$$

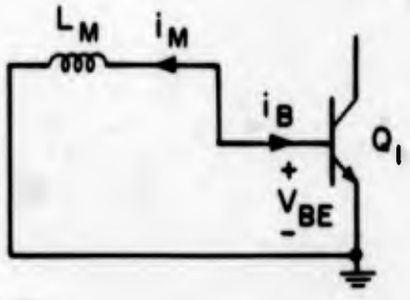
As before, there are two cases to consider. If all of the energy stored in L_M is returned to the power source, then the only power dissipated in the base



a) Circuit



b) Model During "On" Time



c) Model During "Off" Time

FIGURE 4.10 CURRENT FEEDBACK DRIVE

circuit is dissipated in Q_1. The minimum base current supplied occurs at the end of the "on" time of Q_1, and this must be adequate to drive Q_1, i.e.

$$i_B(T_{ON}) = i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}(T_{ON}) \geq \frac{i_L}{\beta} \tag{4.40}$$

where here we have assumed that T is completely reset when Q_1 is turned on at $t = 0$ [$i_M(0) = 0$]. It follows, then, that the minimum power that must be dissipated in the base-emitter of Q_1 to provide proper drive is

$$P_{BASE\ MIN} = V_{BE}\left[i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}(T_{ON})\right] \tag{4.41}$$

The actual power dissipated in the base-emitter of Q_1 when all of the energy stored in L_M is returned to the supply and averaged over the "on" time of Q_1 is

$$\langle P_{TOT\ BASE}\rangle = V_{BE}\left[i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}\frac{T_{ON}}{2}\right]. \tag{4.42}$$

Using Eqns. 4.41 and 4.42

$$\eta_{BASE} = \frac{i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M} T_{ON}}{i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}\frac{T_{ON}}{2}} \tag{4.43}$$

and

$$M = \frac{V_{BE}\left[i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M} T_{ON}\right] + V_{CE|SAT}\, i_L}{V_{BE}\left[i_L \left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}\frac{T_{ON}}{2}\right] + V_{CE|SAT}\, i_L}. \tag{4.44}$$

Examination of Eqns. 4.43 and 4.44 shows that if the magnetizing current in T can be made to be a small fraction of i_B, the efficiency of this scheme can be made to approach unity. In practical designs, this condition can be approached with no serious design compromises.

In circuits where the energy stored in T is dissipated, only the first term in Eqn. 4.39 is considered for calculating power dissipation. Then

$$P_{TOT\ BASE} = V_{BE}\left[i_L\left(\frac{N_2}{N_1}\right)\right]. \tag{4.45}$$

$$\eta_{BASE} = \frac{i_L\left(\frac{N_2}{N_1}\right)\frac{V_{BE}}{L_M}T_{ON}}{i_L\left(\frac{N_2}{N_1}\right)}. \tag{4.46}$$

and

$$M = \frac{V_{BE}\left[i_L\left(\frac{N_2}{N_1}\right) - \frac{V_{BE}}{L_M}T_{ON}\right] + V_{CE|SAT}\,i_L}{\left[V_{BE}\left(\frac{N_2}{N_1}\right) + V_{CE|SAT}\right]i_L}. \tag{4.47}$$

This case can also be made very efficient in practice.

During the "off" time of Q_1, T must be reset. With Q_1 off, $i_L = 0$ and the model of Figure 4.10c is appropriate for analysis of this case. The magnetizing current must continue to flow through L_M until all of the stored energy is removed. The only path provided is through the base-emitter diode of Q_1 in the reverse direction, which will cause zener breakdown of this diode, characterized by the V_{EBO} rating of the transistor. In presently available silicon

transistors, V_{EBO} is not large when compared to the base-emitter voltage encountered when the transistor is "on". This limits the maximum duty cycle of the circuit of Figure 4.10 to

$$D_{MAX} = \frac{V_{EBO}}{V_{BE} + V_{EBO}} \tag{4.48}$$

if complete reset is to take place. For a typical silicon power transistor with $V_{BE} = 1.0$ volt, $V_{EBO} = 8$ volts,

$$D_{MAX} = 0.89$$

and all of the stored energy is dissipated.

The circuit of Figure 4.10 may be modified to allow higher reset voltages and other reset means to be used by the addition of a diode in series with the base lead of Q_1, as shown in Figure 4.11. D_1 blocks any reverse base current that would otherwise flow and allows the voltage across the secondary of T to rise to the combined reverse breakdown of both Q_1 and D_1, which can be made quite large when compared to V_{BE}. Also shown in Figure 4.11 is a reset means which returns energy stored in T to the collector source via winding N_3 and D_2. When Q_1 is "on" and $i_L > 0$, N_3 is polarized such that D_2 is reverse biased. When Q_1 is off, magnetizing current flows out N_3 and through D_2 in its forward direction, since this is the only path available to the magnetizing current. The current is in a direction to return stored energy to V_S, so Eqns. 4.43 and 4.44 may be used to evaluate this circuit. The equations must be modified to account for the power dissipated in D_1 when Q_1 is "on". (The power dissipated in D_2 is usually minute, and will be neglected here.) This may be done by substituting

$$V_{BE} = V'_{BE} + V_D$$

in the denominator only of Eqns. 4.43 and 4.44, where V_D is the diode "on" voltage and V'_{BE} is the "on" base-emitter voltage of Q_1 in Figure 4.11. In Figure 4.11 the reset voltage seen by the N_2 winding is

$$V_R = V_S \left(\frac{N_3}{N_2}\right) \tag{4.49}$$

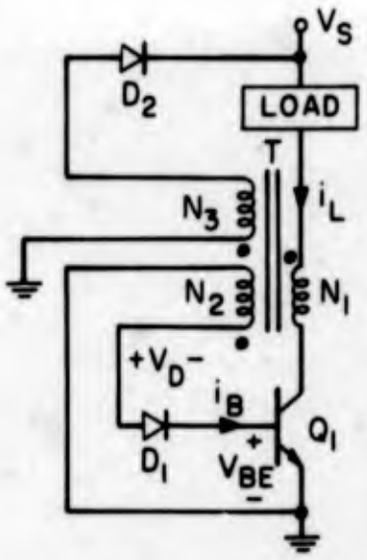


FIGURE 4.11

MODIFIED CURRENT FEEDBACK CIRCUIT

Using Eqn. 4.48 for this case.

$$D_{MAX} = \frac{V_s \left(\frac{N_3}{N_2}\right)}{V_{BE} + V_s \left(\frac{N_3}{N_2}\right)} \quad (4.50)$$

Since N_3 is unconstrained. it may be chosen to make V_R as large as practical for available D_2 diodes. thereby optimizing D_{MAX}.

Current feedback drive circuits may be turned on and off by any of the means discussed under voltage feedback schemes. Since the transformer works across the base-emitter of Q_1. its volt-second capability is less than that required for a voltage feedback scheme having the same maximum T_{ON}. hence the transformer will be smaller and lighter weight for the same job.

4.2 TRANSISTOR "SPEED-UP" METHODS

The "turn-on" and "turn-off" times of transistors are dependent on the parameters of the transistor and upon external circuit constraints. As discussed and demonstrated in Chapter 3, the charge control equations governing transistor switching time may be dominated by an external base drive in excess of that required for steady state operation, which causes a rapid change in stored base charge. This section will discuss techniques which generate this excess base drive current during the switching intervals. Because charge storage effects slow the total interval of turn-off while leaving turn-on unaffected, the turn-off time is considered most critical with respect to speed-up requirements and most of the techniques presented here are aimed at minimizing this time.

Negative Bias

One of the simplest schemes to speed up turn-off relies upon the negative base current generated when a resistor is connected between a power transistor base and a negative supply voltage, as drawn in Figure 4.12. Resistor R_1 has been chosen such that with S closed, sufficient current flows to supply R_2 and to hold Q_1 "on" for the anticipated maximum collector current. When S opens a negative base current of value

$$i_B = -\frac{V_n}{R_2}$$

flows out of the base of Q_1, removing stored charge and, thereby, speeding up turn-off. The pertinent waveforms during this interval are identical to those shown in Figures 3.44 and 3.45 with

$$i_{B-} = -\frac{V_{BE} + V_n}{R_2} .$$

After Q_1 turns off, the base voltage will drop to $-V_n$. If this voltage is larger than the V_{EBO} of Q_1, it will cause emitter-base diode breakdown. While this breakdown is not necessarily harmful, no specification or data is usually given with the transistor as to the allowability or effect upon device reliability of repeated junction breakdown, and so circuits are generally designed to avoid

this condition. A way to avoid this in the circuit of Figure 4.12 is to place a diode from emitter to base, as shown dotted in the figure. After Q_1 turns off, the base voltage goes negative and the added diode conducts, clamping the base voltage slightly negative and, thereby, preventing breakdown. For some transistors, a multiplicity of diodes in series may be necessary to insure that the diodes do not conduct until Q_1 is turned off completely.

The negative bias scheme is a relatively simple method of providing reverse base current, but it is very inefficient. For example, in the circuit of Figure 4.12, if i_L = 10 amps, i_{B1} = 1 amp, i_{B2} = -1 amp, V_B = 28 volts and V_n = -15 volts, then the power dissipated in driving Q_1 and assuming that no negative bias is used is

$$P_{TOT\ BASE} = 28 \text{ watts.}$$

With negative bias, 1 ampere must be provided for base drive and an additional 1 ampere must be provided through R_2. This yields

$$P_{TOT\ BASE} = 56 + 15 = 71 \text{ watts}$$

which is considerably more power than the minimum required. With this circuit,

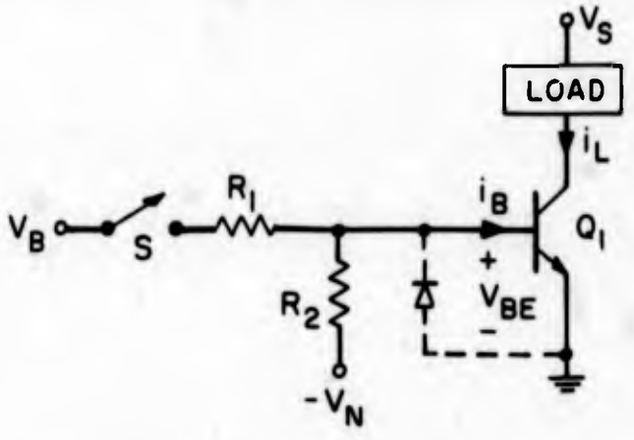


FIGURE 4.12

NEGATIVE BIAS TURN-OFF CIRCUIT

the negative bias must be continually supplied, even though it is only used during turn-off. If a switch is inserted in series with R_2 and is closed only during the turn off interval, the efficiency of this circuit can be improved considerably at the expense of an increase in complexity.

Resistor-Capacitor

If a capacitor is placed in parallel with the base resistor in a resistive base drive circuit, then some "speed-up" action due to charge transfer from the capacitor will result. The schematic diagram of Figure 4.13 illustrates one circuit in which a capacitor is used to provide dynamic charge transfer. This is a shunt drive circuit in which Q_1 is "on" when switch S is open and turns off when S is closed. Assume that S has been open long enough for steady state conditions to prevail. Then

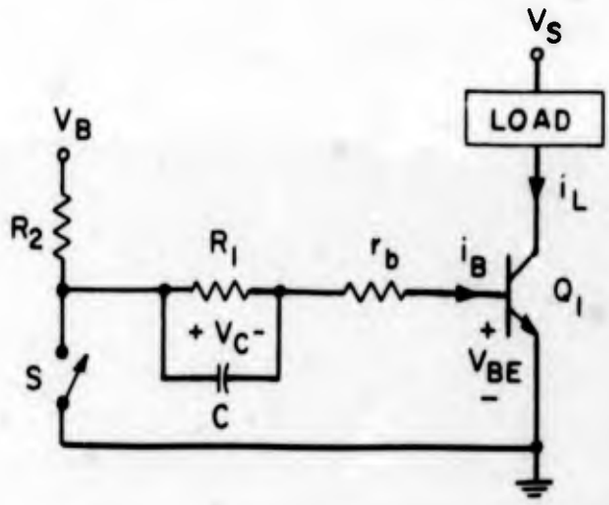
$$V_C = V_B\left(\frac{R_1}{R_1 + R_2 + r_b}\right) - V_{BE} \tag{4.51}$$

and

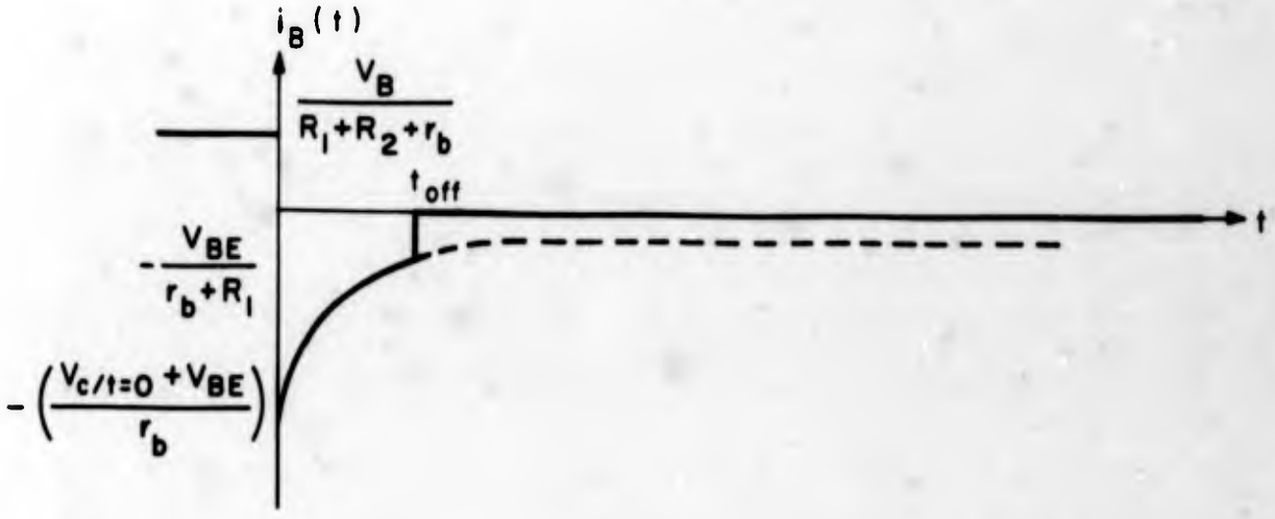
$$i_B = \frac{V_B - V_{BE}}{R_1 + R_2 + r_b}, \tag{4.52}$$

where r_b represents the base region resistance inherent in any transistor. This resistance is usually small compared to the normal external base resistance and is usually ignored when it appears in series with an external resistor. However, in this circuit it is non-negligible, and governs the rate that dynamic charge is delivered to the active portion of the transistor. At $t = 0$, S closes and turn-off begins. From the figure,

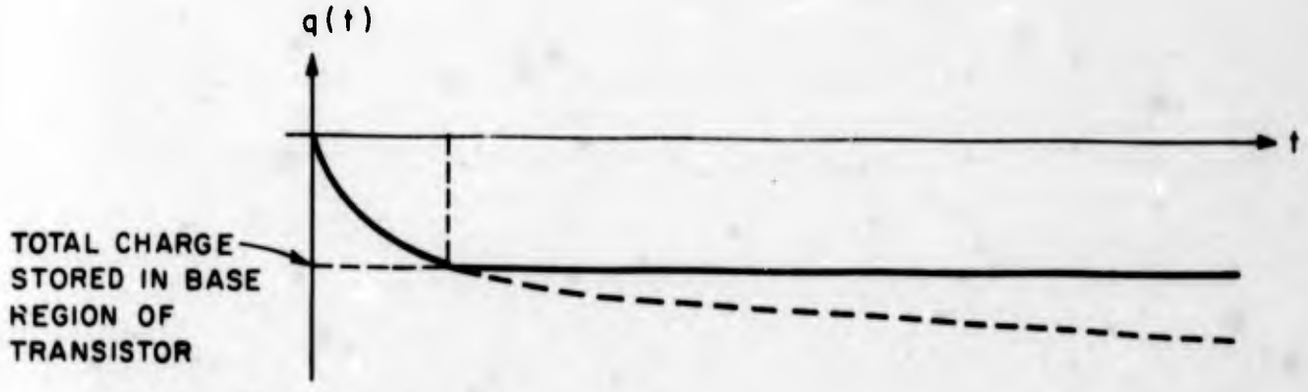
$$i_B(t) = -\left(\frac{V_{C|t=0} + V_{BE}}{r_b}\right)e^{-\frac{t}{r'C}} - \frac{V_{BE}}{R_1 + r_b}\left(1 - e^{-\frac{t}{r'C}}\right) \tag{4.53}$$



a) Circuit



b) Base Current During Turn-Off



c) Charge into Base Versus Time

FIGURE 4.13

CAPACITOR-RESISTOR SPEED-UP

where

$$r' = \frac{R_1 r_b}{R_1 + r_b} \simeq r_b$$

if

$$r_b \ll R_1,$$

which is usually the case, and $V_{C|t=0}$ is given by Eqn. 4.51. This current is sketched in Figure 4.13b. This negative base current removes charge stored in the base region according to the relation

$$q(t) = \left(\frac{V_{C|t=0} + V_{BE}}{r_b}\right)\left(e^{-\frac{t}{r'C}} - 1\right) - \frac{V_{BE}}{r_b + R_1}\left[t - r'C\left(e^{-\frac{t}{r'C}} - 1\right)\right] \qquad (4.54)$$

which is sketched in Figure 4.13. At $t = t_{off}$ all of the charge is removed from the base region of the transistor and turn-off is completed. At this instant the collector current reaches zero, the base-emitter junction becomes reverse biased and no further base current flows. Capacitor C then discharges through R_1 to zero volts. During turn on of Q_1, the opposite action takes place and C charges through R_2 and r_b to provide an excess amount of base current to speed the turn on action. During turn-off an amount of charge

$$Q = C \Delta V \simeq C V_{C|t=0} \qquad (4.55)$$

is removed from the base of Q_1. If C is chosen such that Q is approximately equal (or slightly greater) than the total stored in the transistor, which may be determined by the techniques discussed in Chapter 3, rapid turn-off will result. If C is too small, the speeding up of turn off will be incomplete. On the other hand, if C is too large, a good deal of excess base charge may be injected when the transistor is turned on and it may be so heavily saturated that the charge removed during turn-off is inadequate to complete the rapid turn-off when turn off is attempted shortly after turn on.

Inductor-Resistor

Dynamic speed up action may also be obtained by placing a series inductor-resistor network in shunt with the base-emitter of the power transistor, as diagrammed in Figure 4.14. If i_L is initially zero, when S is closed,

$$i_B(t) = \frac{V_B - V_{BE}}{R_1} - \frac{V_{BE}}{R_2}\left(1 - e^{-\frac{R_2 t}{L}}\right). \tag{4.56}$$

If sometime after this transient has been completed S is opened, then

$$i_B \approx -\frac{V_{BE}}{R_2} e^{-\frac{R_2 t}{L}}, \tag{4.57}$$

thus providing negative base current to speed the turn-off of Q_1. During turn-off an amount of charge

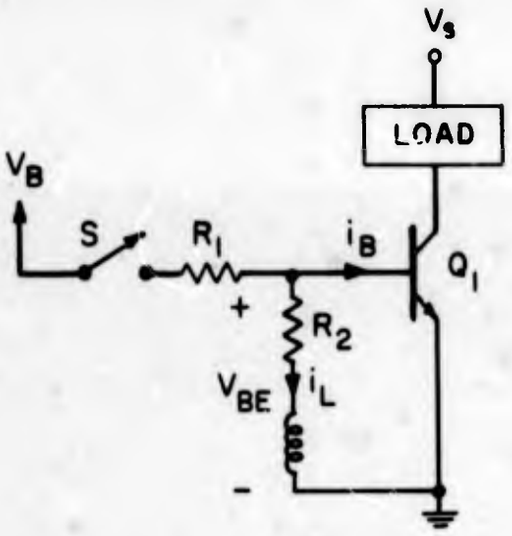
$$Q(t) = \int_0^t i_B dt \tag{4.58}$$

is delivered to the Q_1 base. Using Eqn. 4.57, Q may be evaluated as

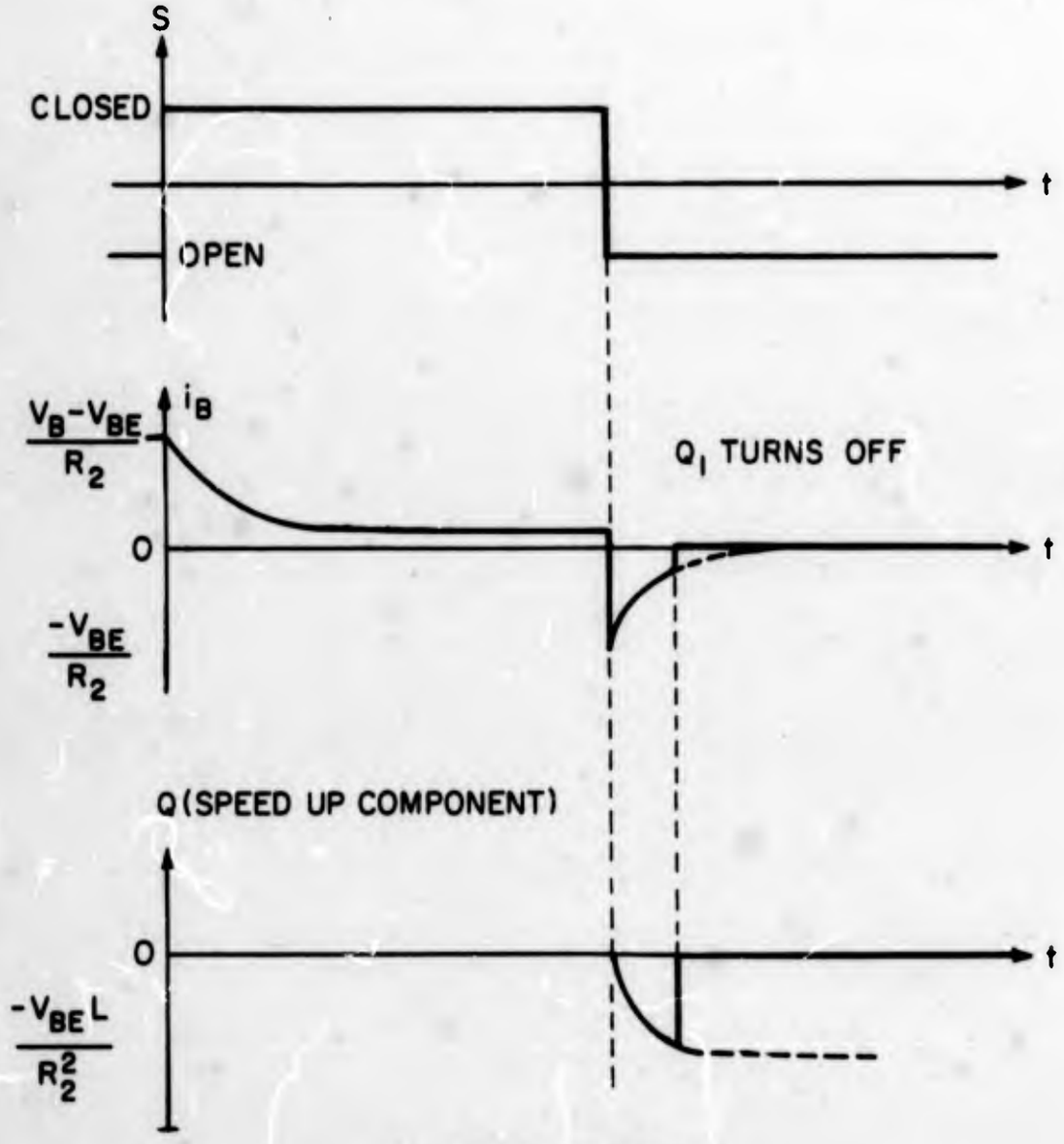
$$Q(t) = -\frac{V_{BE} L}{R_2^2}\left(1 - e^{-\frac{R_2 t}{L}}\right). \tag{4.59}$$

The pertinent waveforms for this case are drawn in Figure 4.14. During the Q_1 on time, an amount of power

$$P = \frac{V_{BE}^2}{R_2}$$



a) Circuit



b) Switching Waveforms

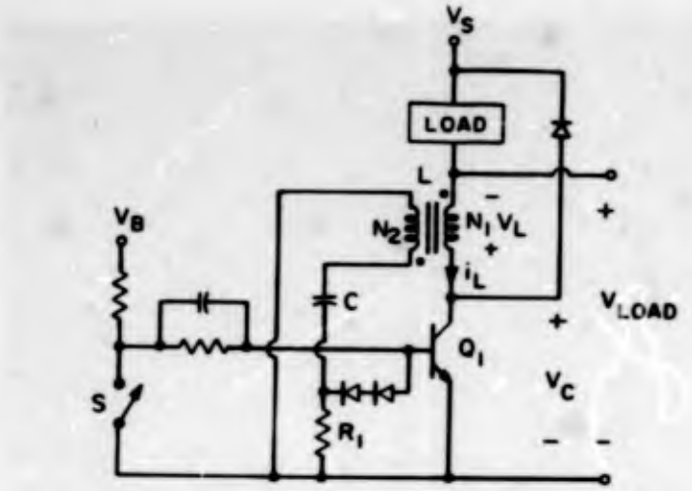
FIGURE 4.14 INDUCTOR-RESISTOR DRIVE

is dissipated continuously, making this method less efficient than capacitor-resistor speed-up at large duty cycles. However, since this method does not require a shunt drive switch, it can show efficiency advantages for short duty cycles. If power dissipation is not a consideration, capacitor-resistor speed-up is generally favored if a shunt S is used and inductor-resistor is favored if S is a series switch.

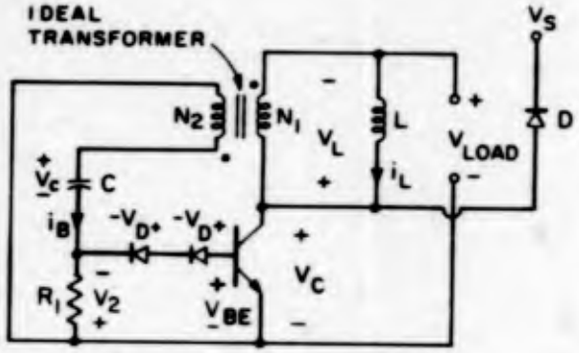
Voltage Feedback

All of the techniques that have been discussed derive the charge that is injected to speed up power transistor operation from the base drive power source. If this source is not well matched to the transistor and if switching occurs at intervals relatively short when compared to the transistor's speeded-up switching time, large amounts of power can be dissipated by the process. Positive feedback techniques have been used to borrow energy from the collector circuit to speed up turn-off while dissipating very little excess power, both under static and dynamic conditions. The first technique to be discussed is the use of voltage feedback, and one version of this circuit is drawn in Figure 4.15. In this particular circuit, the collector load of Q_1 consists of a smoothing inductor L, having an auxiliary winding, placed in series with the normal load. The base drive is shown as a normal shunt resistive drive circuit with capacitor-resistor speed-up. This speed-up circuit is designed only to remove enough base charge to pull Q_1 out of saturation. When this occurs, the voltage across V_C begins to rise. Since L is a relatively large inductor, its current is continuous and it absorbs any voltage across V_C. This increase in V_L is reflected to N_2 as a negative voltage with respect to the base of Q_1 and the two diodes become forward biased. As far as the transistor is concerned, the circuit model during the turn off interval (ignoring the capacitor resistor circuit) appears as shown in Figure 4.15b. As V_C rises, it is clamped by the reflected base-emitter voltage of Q_1 in series with the two diodes and capacitor C, which is

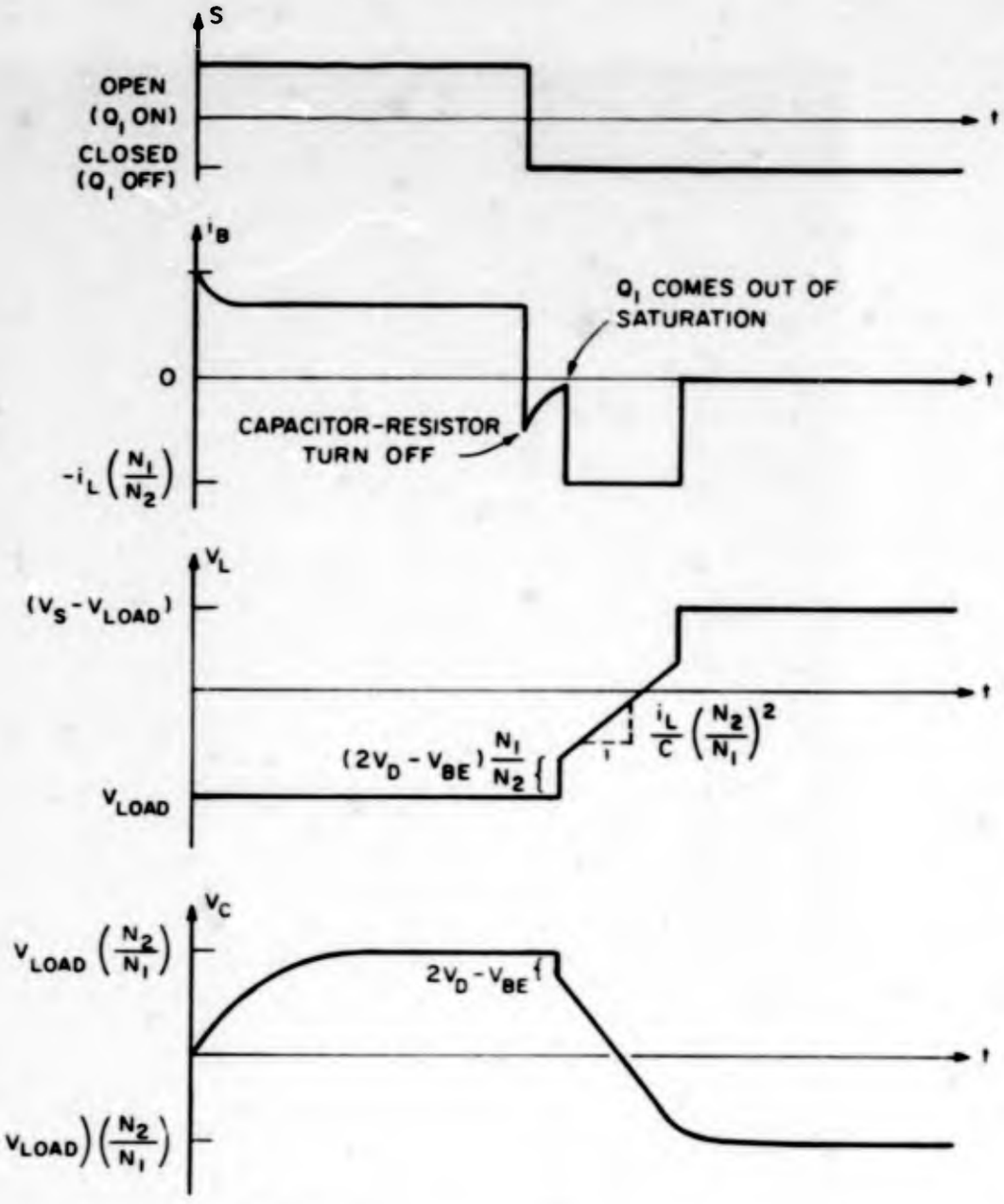
$$V_L = [2V_D - V_{BE} - V_C(0)] \frac{N_1}{N_2} . \qquad (4.60)$$



a) Voltage Feedback Turn-Off Circuit



b) Model During Turn-Off



c) Switching Waveforms

FIGURE 4.15 VOLTAGE FEEDBACK TURN-OFF

At this time, the bulk of the inductor current flows out of the base of Q_1 and (approximately) linearly charges C. That is

$$i_B = -i_L \left(\frac{N_1}{N_2}\right) \tag{4.61}$$

and

$$V_L(t) = \left[2V_D - V_{BE} - V_C(0)\right] \frac{N_1}{N_2} + \frac{i_L}{C} \left(\frac{N_2}{N_1}\right)^2 t. \tag{4.62}$$

If Q_1 turns off when

$$V_C = V_L(t) + V_{load} < V_s$$

then V_C will rapidly rise to V_s when the base-emitter of Q_1 becomes reverse biased and D will close, clamping V_C to V_s. Capacitor C will charge to the reflected value of $V_s + V_{load}$ through R_1. When Q_1 is subsequently turned on, C charges back through R_1 to its intial value of

$$V_C(0) = V_{load} \left(\frac{N_2}{N_1}\right)$$

completing the cycle and resetting the circuit for the next turn-off. As long as there is energy stored in L, some may be borrowed to help turn off Q_1. This entire turn-off circuit does not come into operation until Q_1 is in the active region, with V_C rising. The waveforms covering this operation are shown in Figure 4.15c.

Current Feedback

A second feedback technique for obtaining dynamic base drive employs feedback of the collector current through a transformer to force a current out of the transistor base until all of the stored charge is removed. An example of this type

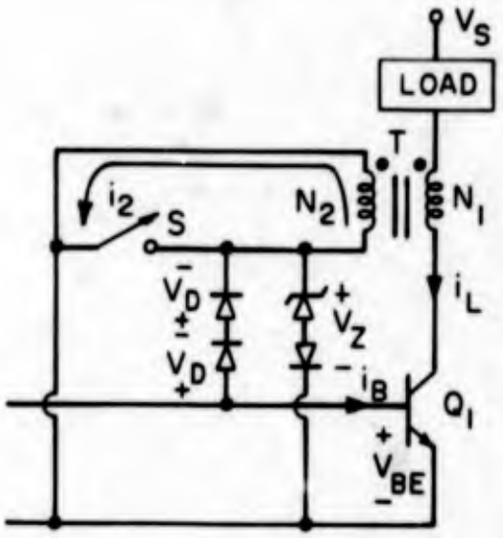
of circuit is shown in Figure 4.16, with the circuits for providing static drive omitted. When Q_1 is "on", S is closed and i_L flows through T and the collector of Q_1. The primary current in winding N_1 of T induces a current $i_2 = \frac{N_1}{N_2}$ in winding N_2 which circulates through switch S. V_{BE} is insufficient to forward bias the two series diodes to any appreciable current level, so the turn-off circuit does not affect operation during the "on" time. When Q_1 is to be turned off, S is opened and the static drive is turned off. Then the current that had flowed through S is forced to flow through the two series diodes and out of the base of Q_1, so during the turn-off interval

$$i_B \sim i_L \left(\frac{N_1}{N_2}\right). \tag{4.63}$$

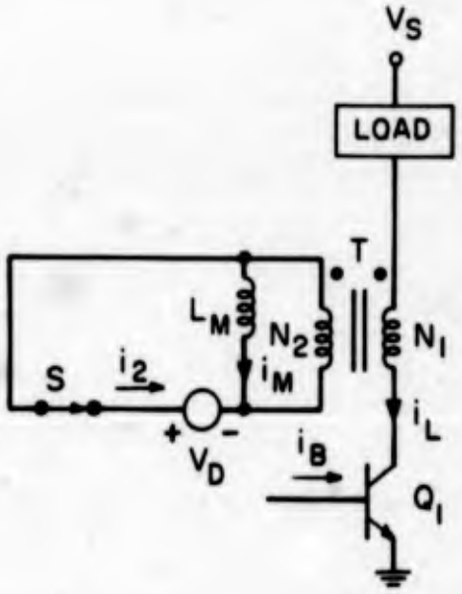
The turn off current is set by the actual collector current and proportionally tracks this current until Q_1 turns off completely. If any energy remains in the magnetizing inductance of T, it is dissipated across V_z in the zener diode. In practice this lost energy can be made negligible by designing the transformer with as large a magnetizing inductance as is practical. Switch S may be reclosed any time after reset of T is complete, readying the circuit for the next switching cycle.

While this current feedback circuit operates only during the turn-off interval of Q_1, it is a dynamic circuit and sets limitations on the maximum time that Q_1 may be "on". This may be seen from a model of the circuit of Figure 4.16a during the Q_1 "on" time, as drawn in Figure 4.16b. Here we have assumed that S has a finite voltage drop across it when current flows through it. This is modelled by a voltage source V_D in series with S. If Q_1 turns on at t = 0 and S is closed, the voltage across the N_2 winding of T during the "on" time is V_D and the current in the magnetizing inductance is

$$i_M(t) = \frac{V_D}{L_M}\, t. \tag{4.64}$$



a) Circuit



b) Model During Q_1 "on" Time

FIGURE 4.16

CURRENT FEEDBACK TURN-OFF CIRCUIT

The magnetizing current subtracts from the current which turns off Q_1, leaving a current available for turn-off of Q_1 of

$$i_{B|available} = -\left[I_L \left(\frac{N_1}{N_2}\right) - \frac{V_D}{L_M} T_{ON}\right] \tag{4.65}$$

at the end of the "on" time. If a second term of Eqn. 4.65 is appreciable compared to the first, the approximation leading to Eqn. 4.63 is invalid and the magnetizing current must be taken into account. When Eqn. 4.65 equals zero at

$$T_{ON|MAX} = \frac{L_M}{V_D} I_L \left(\frac{N_1}{N_2}\right) \tag{4.66}$$

or at any "on" time greater than $T_{ON|MAX}$ the turn-off speed up circuit will be completely inoperative when an attempt is made to turn off Q_1. If T magnetically saturates at a time less than $T_{ON|MAX}$ the speed-up circuit also will not operate. Care must be taken in the design of T to insure proper operation at the maximum "on" time to be encountered and this scheme may only be used in circuits where the maximum "on" time is well controlled. An advantage of this technique over voltage feedback is that turn-off action begins as soon as S is opened, and is independent of whether Q_1 is saturated or not. Since the saturation charge may be the dominant charge storage term, this is a significant advantage of this approach.

5. CONSIDERATIONS AT THE OUTPUT STAGE LEVEL

The power processors or modules considered previously are composed of a number of basic power conversion units together with any additional control and logic functions needed to make these units function in the desired manner. A basic power converter is defined here as that circuitry which performs a single power conversion. It has the property that it cannot be further divided without destroying its power conversion ability. Familiar examples of basic power converters are dc-dc converters, ac-dc rectifiers and dc-ac inverters.

A study of basic power converters shows that the power flow from input to output is usually through a small number of circuit elements. We shall call that portion of the circuit which handles the main power flow and which is essential to power conversion the basic output stage. This definition eliminates some input and output networks, if any, and any low level control circuitry; the former since they are not essential to the power conversion, and the latter since they are not handling the transferred power. A study of a number of circuits shows that a basic output stage may, for example, consist solely of a transistor, a diode and an energy storage element. With this distinction, we may model a basic power converter by the block diagram in Figure 5.1. Here, N_1 and N_2 are networks coupling the input and output of the converter to the basic output stage, and the control function is the circuitry which determines the operating characteristics of the basic output stage.

This chapter will consider some of the characteristics and limitations of idealized basic output stages. This is a fruitful endeavor since many limitations of the entire converter are determined by the output stage used, regardless of the control concept incorporated in the converter.

5.1 BASIC OUTPUT STAGES

Output stages may be broken down into two broad classes, linear and nonlinear. Nonlinear circuits normally encountered usually incorporate switches and/or nonlinear magnetic elements, although they are

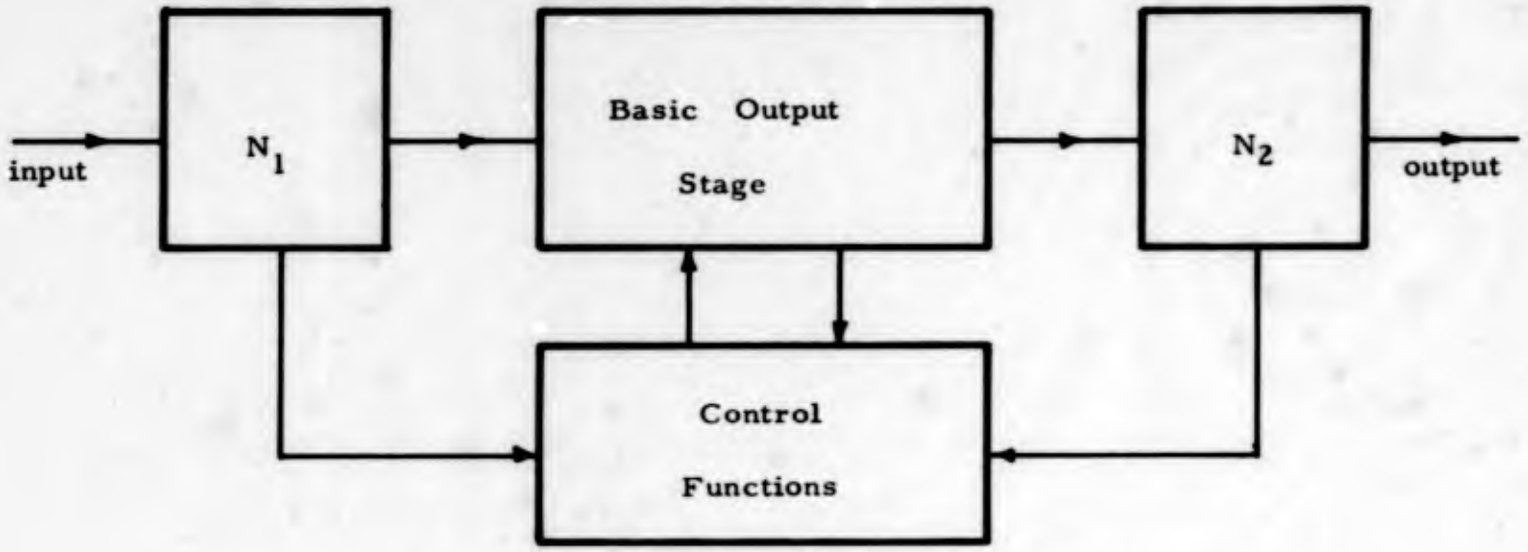


FIGURE 5.1

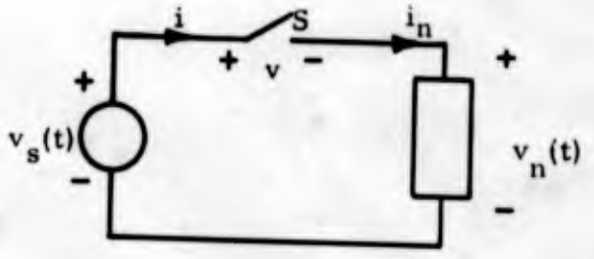
BLOCK DIAGRAM OF A BASIC POWER CONVERTER

not necessarily restricted to these. Nonlinear magnetics will not be discussed here since the topic would not aid in understanding the behavior of the circuits to be discussed in this chapter.

Circuits of Some Commonly Encountered Output Stages

At this point, we shall develop a number of commonly used circuits by a series of simple modifications on one basic circuit. The development of these circuits as presented here is not unique and, in any case, is done mainly to show the degree of similarity between the circuits. Only the static transfer characteristics will be considered at first. Quasi-static approximations and practical limitations will be discussed later.

A circuit with a single switch is shown in Figure 5.2. Without a more detailed description of N, we cannot state any general relations other than the obvious voltage and current constraints shown in Figure 5.2.



$v_n(t) = v_s(t)$ when S is closed

$i_n(t) = 0$ when S is open

FIGURE 5.2

OUTPUT CIRCUIT WITH A SERIES SWITCH CONTROL

A frequently encountered situation is that in which $v_s(t)$ is periodic and N is a parallel RC network. If the switch is opened and closed at a frequency equal to the fundamental frequency of $v_s(t)$, the circuit becomes a half-wave, phase-sensitive rectifier. If a diode is used, as shown in Figure 5.3, then the voltage across the diode is the parameter which controls the diode state.

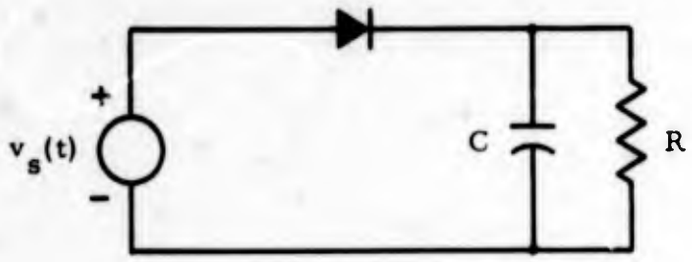


FIGURE 5.3

A HALF-WAVE RECTIFIER

Some problems exist in this circuit if $v_s(t)$ is a rectangular wave or some other waveform with fast risetimes. One is that the diode currents can be quite large due to the dv/dt current into the capacitor and may be limited only by the source resistance. Another less obvious problem is that of circuit efficiency. Under certain conditions of charging the capacitor C, this circuit may be extremely inefficient, even though the diode may be an almost ideal element. This problem is of interest in that it illustrates some of the pitfalls one may succumb to without a careful study of the concepts involved.

Similar problems are encountered with a single switch if the load is a series RL network, as shown in Figure 5.4. In this case, large voltages can be developed across the switch as it opens if there is current in the inductor. This can be seen from the inductor v-i characteristic, $v_L = L\frac{di_L}{dt}$, showing that large voltages can be generated by rapidly forcing the inductor current to zero. In this circuit, this problem can be eliminated by the addition of a second switch as shown in Figure 5.5.

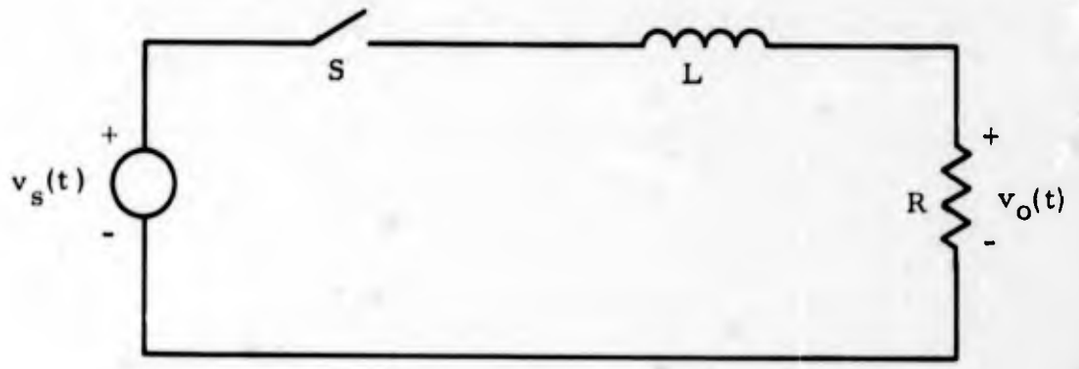


FIGURE 5.4

SINGLE SWITCH CIRCUIT WITH AN INDUCTIVE LOAD

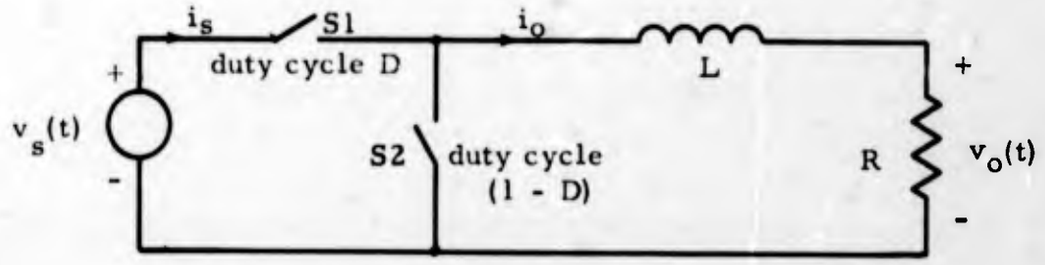


FIGURE 5.5

CHOPPER OUTPUT STAGE

Assuming that the switches are alternately opened and closed, there is never a current constraint placed on the inductor by the switches. This basic circuit, called a chopper, is used quite often in switching regulator systems. The symbols (D) and (1-D) next to the switches denote the switch duty cycles - the fraction of the time that each switch is closed. Hence, the duty cycle must always lie in the range 0 - 1.

There is always a voltage constraint across the RL imposed by

the source and switches if the switches alternately open and close. Thus, as far as the load R is concerned, we may model the switches and source by an equivalent voltage source as shown in Figure 5.6. If the source $v_s(t)$ in Figure 5.5 is a constant V_s and the on-time duty cycle of S1 in Figure 5.5 is D, then the time average value of the input source $v_{eq}(t)$ in Figure 5.6 is given by

$$\langle v_{eq}(t) \rangle = DV_s$$

independent of the actual switching period T. The symbol < > is used to denote a time average.

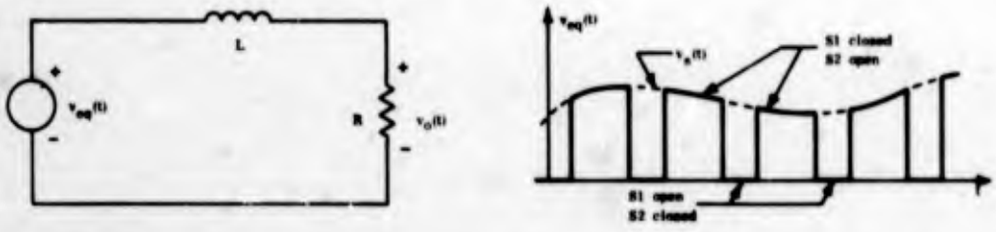


FIGURE 5.6

AN EQUIVALENT CIRCUIT FOR THE CHOPPER

Since the RL circuit has a voltage transfer ratio of 1 at dc, we have

$$\langle V_o(t) \rangle = \langle v_{eq}(t) \rangle = DV_s.$$

Thus, the dc component of the output (V_o) is just the duty cycle times the input voltage. An upper case letter will be used to denote the dc components of the appropriate variables if it is not a constant. Since $0 < D < 1$, we have for $V_s > 0$,

$$\langle V_o \rangle = DV_s \qquad (5.1)$$

$$0 < (\langle V_o \rangle) < V_s \qquad (5.2)$$

If the rate at which S1 and S2 alternate is high enough, the alternating components of $v_{eq}(t)$ will be greatly attenuated at the output due to the low-pass characteristic of the series RL network, and the output $v_o(t)$ will essentially be the dc component $V_o = \langle v_o \rangle$.

From Eqn. 5.2 above, we may plot the average output voltage V_o as a function of duty cycle D for fixed V_s as in Figure 5.7, which again illustrates the bounds on V_o implied by Eqn. 5.2.

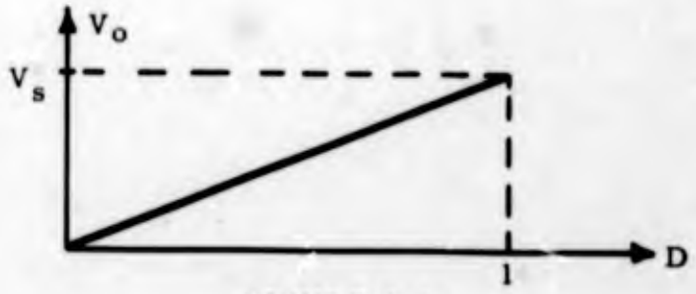


FIGURE 5.7

CHOPPER OUTPUT VOLTAGE VS. DUTY CYCLE

Referring to the original circuit in Figure 5.5, let us find the relation between the average load current I_o and the average source current I_s. Since the voltage across R is essentially constant, the current through R and hence L is constant. Thus, a current I_o flows in whichever switch is closed. Switch S1 is closed a fraction D of the time, so that the current through it is shown in Figure 5.8. From this we see that

$$I_s = \langle i_s(t) \rangle = DI_o,$$

or the dc components of current are related by

$$I_s = DI_o. \qquad (5.3)$$

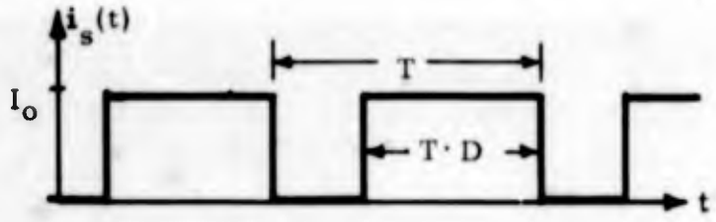


FIGURE 5.8

SOURCE CURRENT WAVEFORM FOR A CHOPPER OUTPUT STAGE

From Eqns. 5.1 and 5.3, we see that the circuit in Figure 5.5 behaves like an ideal transformer at dc with turns ratio 1:D at dc and, furthermore, that it is lossless. Thus, at dc we may model the chopper in Figure 5.5 by the equivalent dc model shown in Figure 5.9.

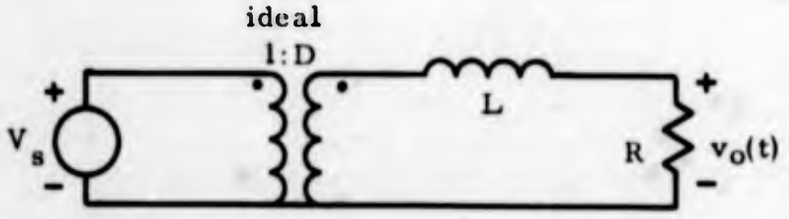
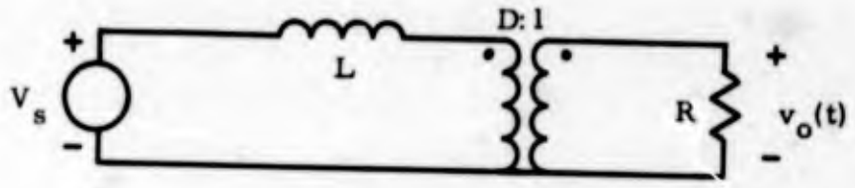


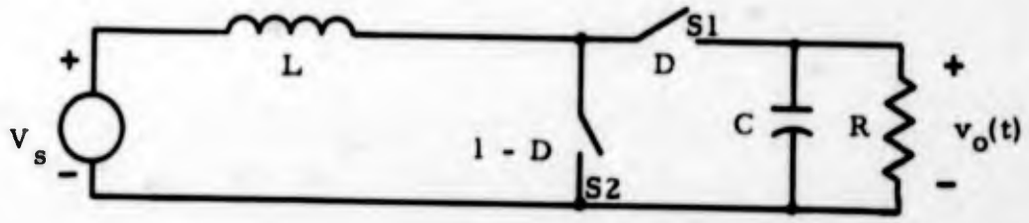
FIGURE 5.9

IDEAL DC TRANSFORMER MODEL OF A CHOPPER

One major limitation of this circuit is the property that it can only step down in voltage, since physical limitations constrain D to be $0 < D < 1$. Thus, the output voltage is always less than the input voltage. However, from the representation in Figure 5.9, we see that a step up in voltage might be obtainable by reversing the transformer and inductor as shown in Figure 10a.



a. Proposed Model of Step-Up Circuit



b. Output Circuit with Switches Reinserted

FIGURE 5.10

DEVELOPMENT OF THE FLYBACK OUTPUT STAGE

The circuit with the switches reinserted is shown in Figure 5.10b. A capacitor must be added across the output to satisfy the requirement of an essentially constant output voltage. This configuration is commonly called a "flyback" or "bucket" output. The dc components are given by Eqns. 5.1 and 5.3 with source and load subscripts reversed.

$$V_s = DV_o$$

$$I_o = DI_s \qquad (5.4)$$

or, we have

$$V_o = \frac{1}{D} V_s. \qquad (5.5)$$

The latter relation is plotted in Figure 5.11 for the allowable range of D.

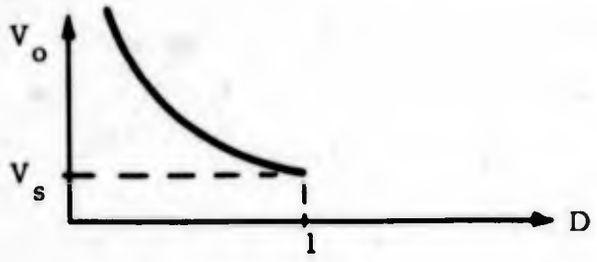


FIGURE 5.11

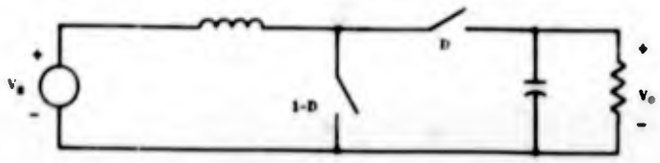
OUTPUT DC VOLTAGE VS. DUTY CYCLE FOR A FLYBACK OUTPUT STAGE

From either Figure 5.11 or Eqn. 5.5, we can see that the average output voltage of a flyback stage is always greater than the source voltage and, thus, it is inherently a step up device, with the range of output voltages given by $V_o \geq V_s$.

If we subtract a voltage V_s from the output, the range of average output voltages obtainable will be given by $V_o > 0$. The development of a circuit which does this is shown in Figure 5.12. For the circuit shown in Figure 5.12f, the output voltage is given by

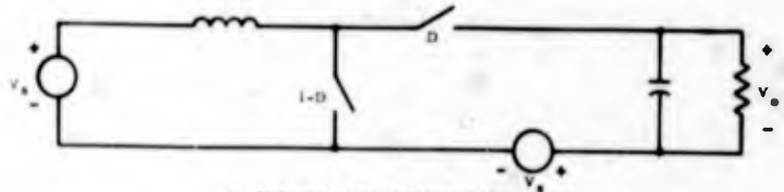
$$V_o = -\left(\frac{1}{D} V_s - V_s\right) = -\frac{1-D}{D} V_s. \qquad (5.6)$$

This relation is plotted in Figure 5.13. We can obtain an output voltage of any magnitude from this circuit, but there is always a sign inversion with respect to the common ground. A circuit which does not produce a sign inversion can be obtained from that in Figure 5.12f. One method of doing this is illustrated in Figure 5.14. Here an unrealizable ideal transformer is realizable as two coupled inductors, as illustrated in Figure 5.14d. If isolation is not necessary, the coupled inductors may be replaced by a single tapped inductor as shown in Figure 5.14e.



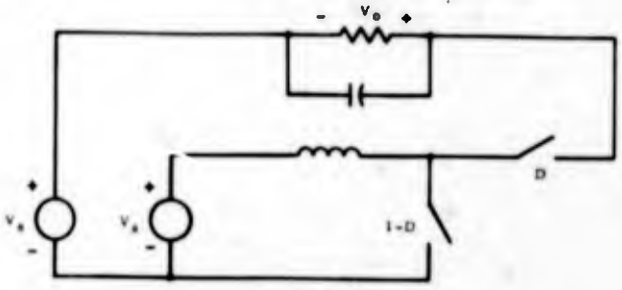
$V_o > V_s$

a. Basic flyback output.



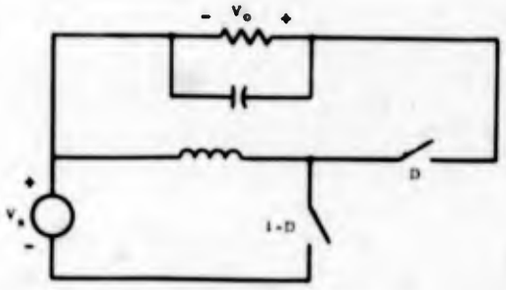
$V_o > 0$

b. Flyback with V_s subtracted from output.



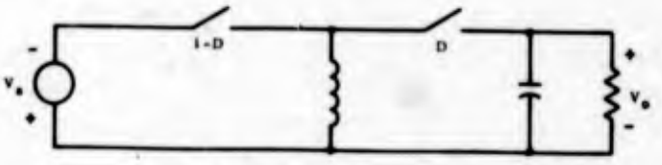
$V_o > 0$

c. Circuit in b) redrawn.



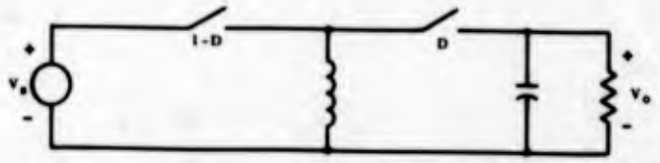
$V_o > 0$

d. One voltage source eliminated.



$V_o > 0$

e. Circuit in d) redrawn.



$V_o < 0$

f. Circuit in e) with source polarity reversed. Note the change in the polarity of allowed output voltages.

FIGURE 5.12

DEVELOPMENT OF A MODIFIED FLYBACK OUTPUT

The basic output stage of most dc to dc converters currently in use will be one of the basic circuits developed here. These circuits together with their dc transfer characteristics versus duty cycle are catalogued in Figure 5.15 for comparison.

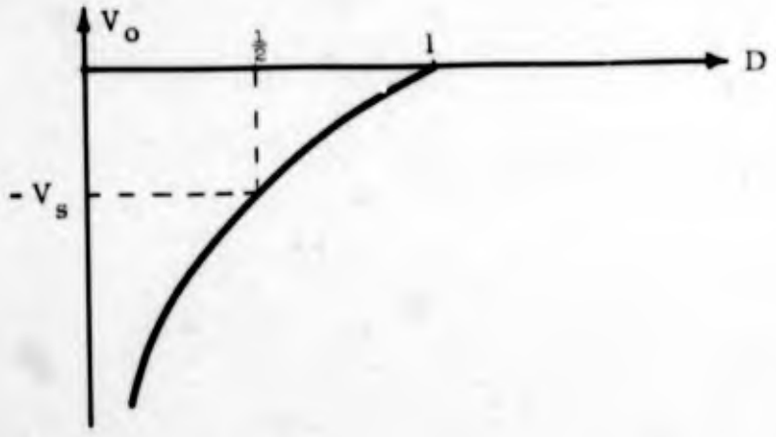


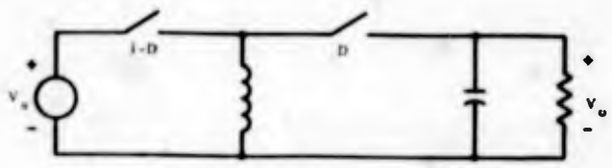
FIGURE 5.13

OUTPUT VOLTAGE VS. DUTY CYCLE D FOR THE FLYBACK CIRCUIT IN FIGURE 5.12f.

5.2 QUASI-STATIC APPROXIMATIONS

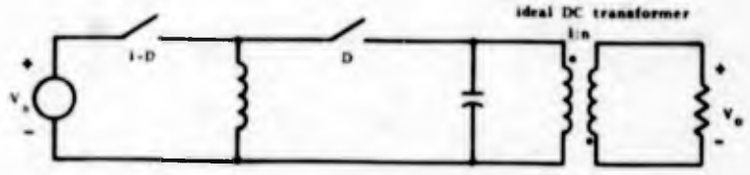
The results obtained in the preceding section assumed that the source voltage and the duty cycle of the switches were constant. Under these circumstances, it is meaningful to talk about dc components of the source and output voltages regardless of the actual frequency at which the switches are opened and closed. In practice, both the source voltage and the switch duty cycle may be time varying so that it is no longer meaningful to talk about dc components. In fact, we must consider what we mean when we treat the duty cycle as a function of time, since it is essentially time discrete and defined over an entire on-off switching period.

We may define a waveform D(t) which we will call the duty cycle of a rectangular wave by letting D(t) take the value of the duty cycle



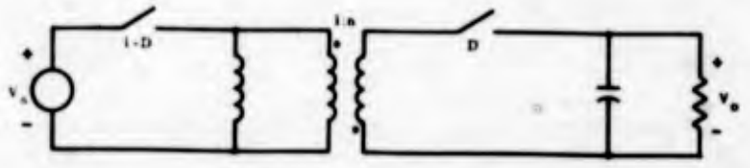
$V_o < 0$

a. Modified flyback



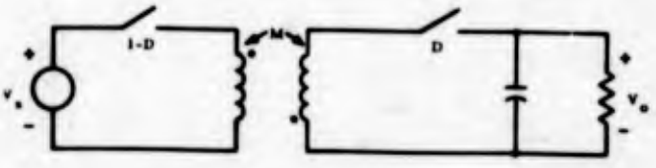
$V_o > 0$

b. Addition of an ideal transformer to obtain a sign inversion.



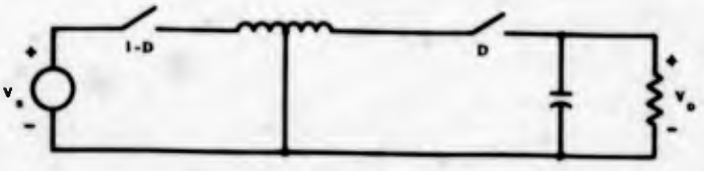
$V_o > 0$

c. Reflecting the switch and the capacitor to the secondary.



$V_o > 0$

d. Modeling the transformer and inductor as two unity-coupled inductors.



$V_o > 0$

e. Modeling the coupled inductors as a tapped inductor if there is a common ground.

FIGURE 5.14

DEVELOPMENT OF A MODIFIED FLYBACK CIRCUIT WITHOUT AN OUTPUT SIGN INVERSION

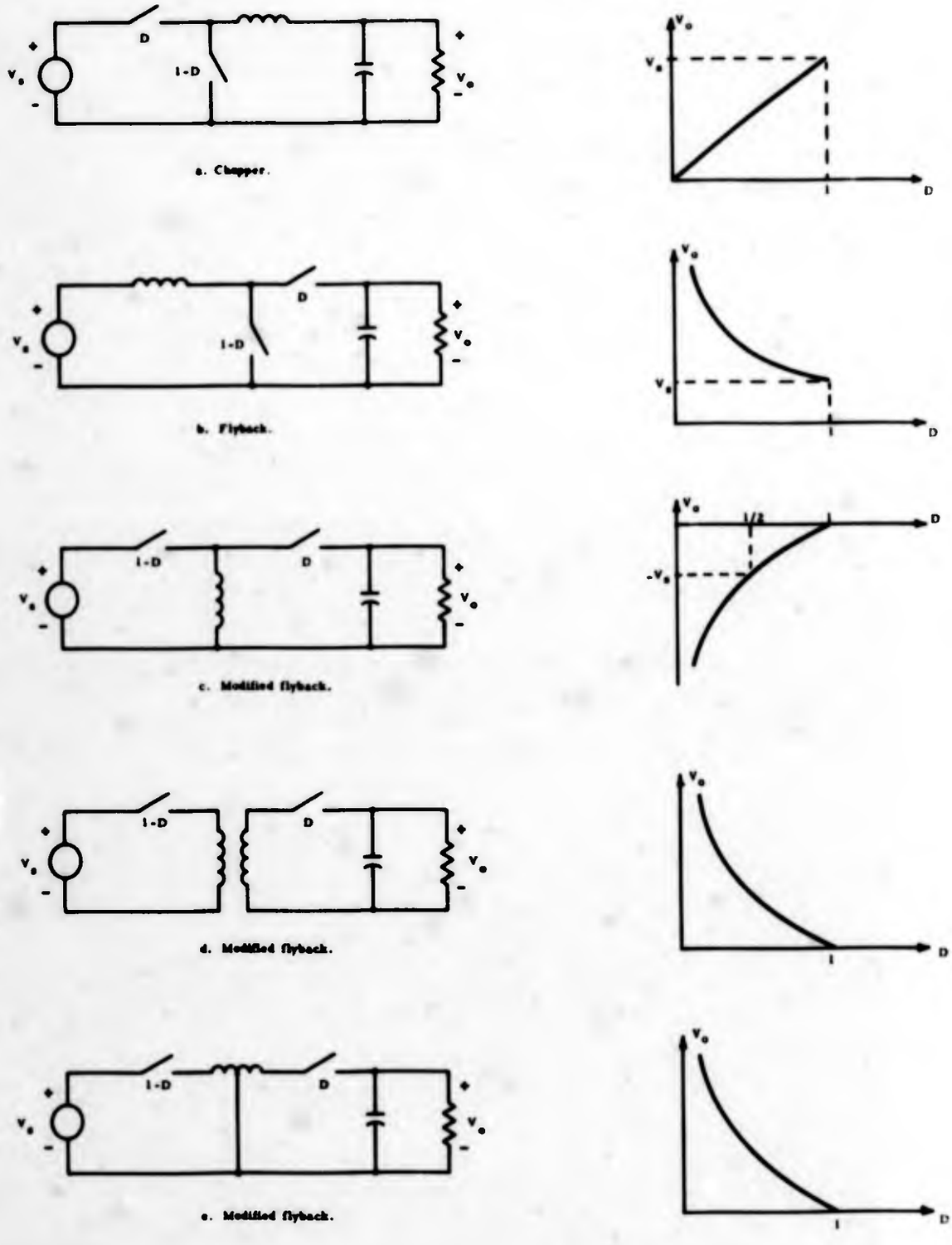
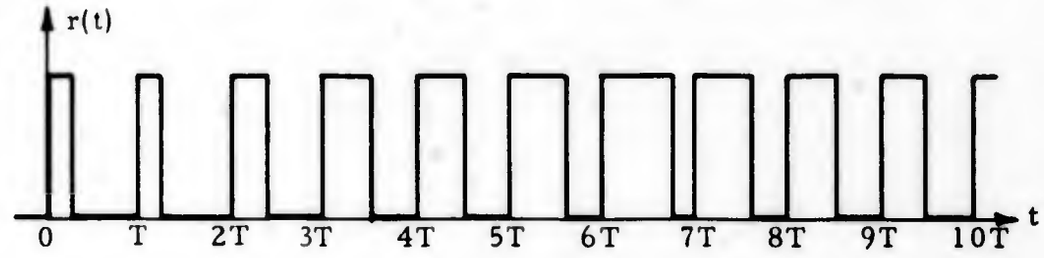


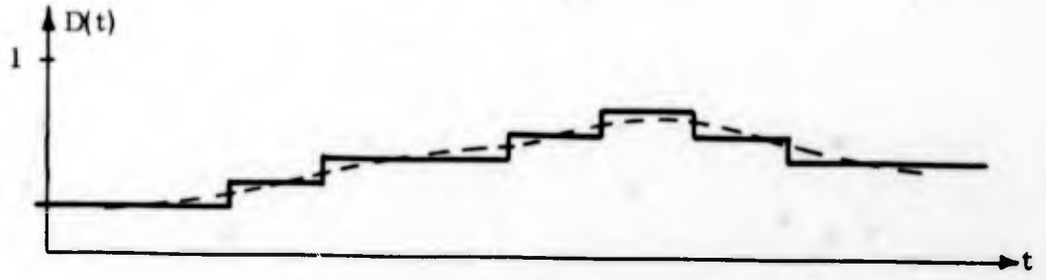
FIGURE 5.15

OUTPUT STAGES COMMONLY USED IN DC-DC CONVERSION AND THEIR DC CONTROL CHARACTERISTICS

of each period of the rectangular wave for the duration of that period as shown in Figure 5.16b.



a) Waveform



b) Duty Cycle

FIGURE 5.16

A RECTANGULAR WAVEFORM r(t) AND ITS ASSOCIATED DUTY CYCLE WAVEFORM D(t)

By definition, D(t) has the property that it is constant within any full period of the associated rectangular wave, so that the rectangular wave is well defined if just D(t) is given. We shall say that the duty cycle of the rectangular wave r(t) is also given by a continuous approximation of D(t), as shown in Figure 5.16b.

Let us consider a band limited waveform x(t) such that $X(\omega) = 0$, $|\omega| > \omega_o$ and with the further restriction that $0 < x(t) < 1$ for all t. If we divide the time axis into intervals $\tau_k (k = \ldots -2, -1, 0, 1, 2, \ldots)$ such that $\tau_k << \frac{1}{\omega_o}$ for all k, then x(t) will be essential constant over

each interval τ_k. Thus, we may approximate x(t) by a step-wave which, in each interval τ_k, takes on the value of x(t) for some point within the interval.

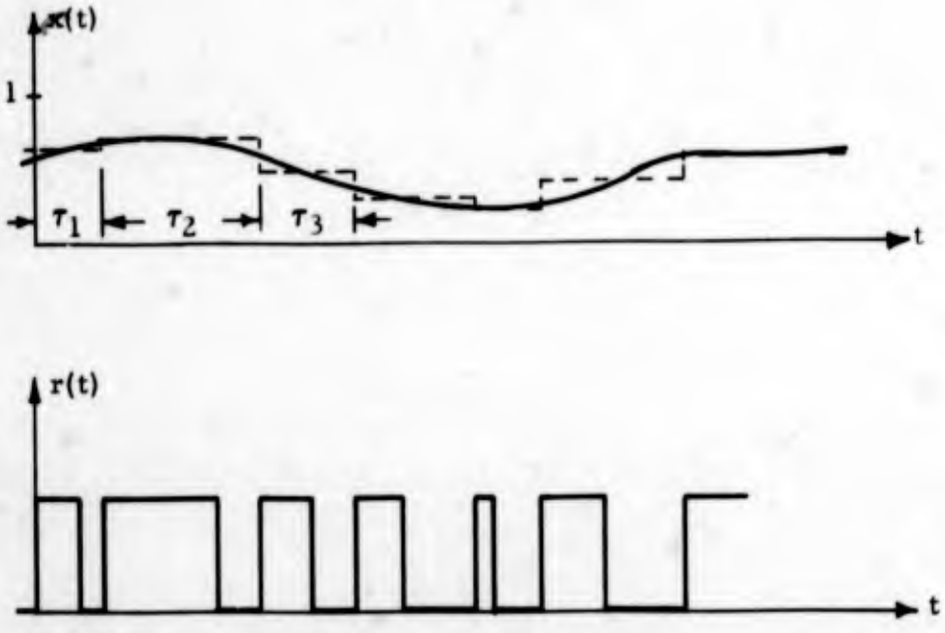


FIGURE 5.17

CONSTRUCTION OF A RECTANGULAR WAVEFORM FROM AN AMPLITUDE AND BANDWIDTH LIMITED FUNCTION x(t).

We can now construct a rectangular wave with periods τ_k with the duty cycle of each period given by the value of the step-wave approximation to x(t) in the corresponding period. A sample waveform x(t), a time partitioning τ_k, and the associated step-wave and rectangular wave are illustrated in Figure 5.17. Note that both the waveform x(t) and the time partition τ_k must be specified in order to uniquely determine the associated rectangular wave. Thus, we can construct an infinite number of rectangular waves each of which has the approximate duty cycle waveform x(t) by choosing different partitions τ_k. If the

partitions are chosen such that all the τ_k are equal, then the associated rectangular wave is a pulse-width modulated waveform. By appropriate choice of the τ_k, pulse frequency and other modulation waveforms may be realized. Each of these will still have the same duty cycle waveform by construction.

What has been described is a method of generating a rectangular waveform from a continuous band limited waveform. This process approximates the realizations of a number of control schemes for switching power converters, since it converts an analog signal into a two-state, or on-off, signal which controls the switching devices in the converter.

Let us consider the system in Figure 5.18, where the input r(t) is the rectangular waveform of Figure 5.17b, which is constructed to have a duty cycle as a function of time given by the band limited waveform x(t). If $|X(\omega)| = 0$ for $|\omega| > \omega_o$ and all the periods τ_k of r(t) are such that $\tau_k << \frac{1}{\omega_o}$ for all k, then the output of the low-pass filter, y(t), will be given by $y(t) \simeq x(t)$.

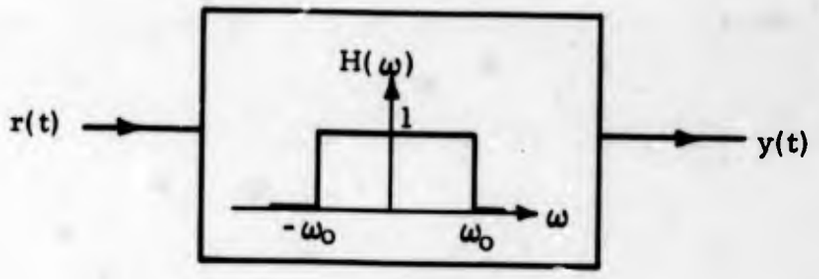
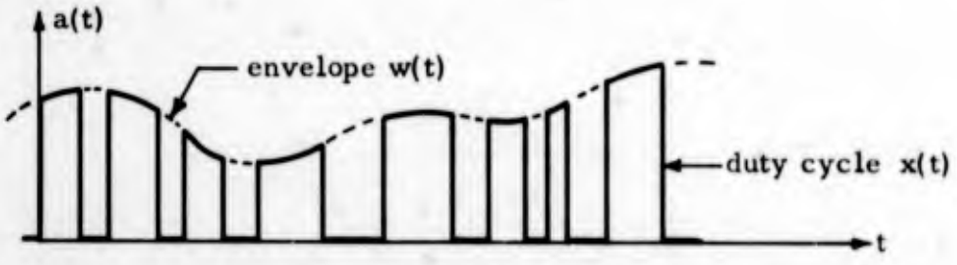


FIGURE 5.18

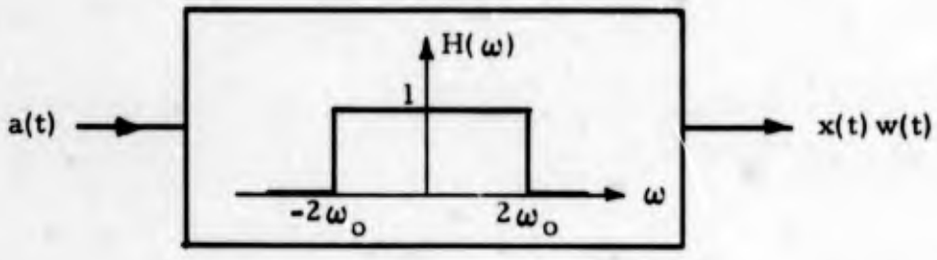
DETERMINATION OF THE DUTY CYCLE OF A RECTANGULAR WAVEFORM BY LOW-PASS FILTERING

Although this result is intuitively satisfying, it is difficult to obtain correct analytical expressions in the general case. Furthermore, the error between y(t) and x(t) is dependent on the relation between the switching times τ_k of r(t) and the bandwidth ω_o of x(t).

Suppose the waveform r(t) is amplitude modulated by a function w(t) which is band limited to ω_o. A consideration of the spectra of r(t) and r(t) modulated by s(t), which we shall denote by a(t), shows that the result of low pass filtering the modulated waveform is to give w(t)x(t), where x(t) is the duty cycle of the modulated time waveform. An example of such a waveform is shown in Figure 5.19. This property will prove extremely useful in making quasi-static models of switching systems.



a. Amplitude-Modulated Waveform



b. Isolation of Low-Frequency Components of a(t)

FIGURE 5.19

A WAVEFORM WITH BOTH AMPLITUDE AND DUTY CYCLE MODULATION

The Quasi-Static Equation for the Chopper

Let us consider the basic chopper circuit shown in Figure 5.15a with the addition of an output filter capacitor, as shown in Figure 5.20.

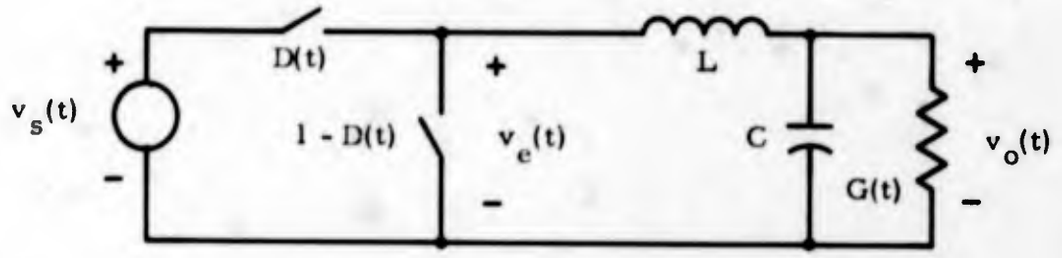


FIGURE 5.20

BASIC CHOPPER OUTPUT STAGE

We shall allow the source voltage $v_s(t)$ and the switch duty cycle D(t) to be slowly time-varying, and we shall consider the case where the load conductance is variable. The switch duty cycle D(t) will be a function of various voltages, currents and other parameters of the system, but the exact functional relationship will not concern us at the moment.

The voltage $v_e(t)$ is completely specified once D(t) and $v_s(t)$ are specified, as seen from Figure 5.20. The transfer function from $v_e(t)$ to $v_o(t)$ is that of a two-pole, low-pass filter, so that only the low-frequency components of $v_e(t)$ need be considered as affecting $v_o(t)$. The quasi-static approximation rules out a consideration of ripple at the switching frequencies. We assume that the ripple is small and can be treated separately, although this is not true for some control schemes. Thus, ignoring all components of $v_e(t)$ except at low frequencies, we see that the effect of $v_e(t)$ on $v_o(t)$ is the same as that of a source with a value given by $v_e(t) = v_s(t)D(t)$. For low frequencies, we may now replace the chopper model of Figure 5.20 by the model shown in Figure 5.21.

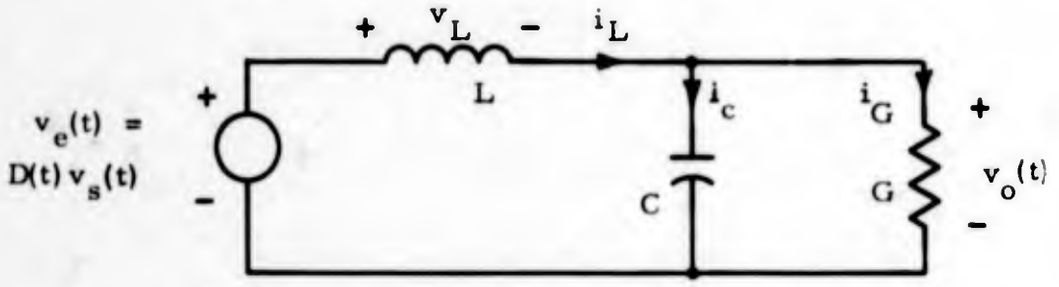


FIGURE 5.21

QUASI-STATIC MODEL OF A CHOPPER OUTPUT STAGE

A differential equation relating the quasi-static variables in Figure 5.21 can now be written. We have

$$v_L(t) = D(t)v_s(t) - v_o(t)$$

$$i_L(t) = i_c(t) + i_G(t)$$

Using the element V-i relations,

$$\frac{1}{L}\int_{-\infty}^{t} [D(\beta)v_s(\beta) - v_o(\beta)]\, d\beta = C\frac{dv_o}{dt} + G(t)v_o(t)$$

Differentiating and regrouping, we obtain

$$LC\frac{d^2v_o}{dt^2} + LG(t)\frac{dv_o}{dt} + \left[L\frac{dG}{dt} + 1\right]v_o(t) = D(t)v_s(t), \qquad 0 \le D(t) \le 1. \quad (5.7)$$

This is the quasi-static differential equation for the simplified chopper shown in Figure 5.20, and it is valid for dc and low frequencies. At

dc we let G(t) be constant, $v_o(t) = V_o$, $v_s(t) = V_s$, $D(t) = D$, so that all time derivatives are zero. Eqn. 5.7 then gives

$$V_o = DV_s \tag{5.8}$$

which is the expression determined previously. If in addition to Eqn. 5.7 we are given the characteristics of the control concept, we may then determine the static and quasi-static behavior of the resulting basic power converter. Some of the limitations of basic power converters employing the output stages described above will be discussed in Chapter 7.

6. CONTROL CONCEPTS AND REALIZATIONS

In the preceding chapter, we mentioned that a basic power converter consists of two parts - a basic output stage and a control concept. We shall define the control concept as a methodology for operating the output stage - which we consider distinct from possible realizations of the control concept. Within this definition and because of the behavior of various output stages described in the previous chapters, schemes such as pulse-width and pulse-frequency modulation are usually means of realization of a control concept and not an inherent part of the control methodology. This should become clearer after the discussion below.

In our discussion of output stages and quasi-static models, we determined that the parameter which controls the quasi-static output stage operation is the switch duty cycle D. Since the quasi-static terminal characteristics of a basic power converter are usually those of interest, the control scheme should be concerned with the generation of an appropriate duty cycle.

Here we would like to discuss a breakdown of a control concept into two parts. This division is meaningful and can be quite useful in constructing a control realization. Although this division is artificial in the sense that these two sections may not be separable in a circuit, we shall see that it may be an excellent aid in visualizing and planning control concepts for complex systems.

The control concept can be modeled as consisting of two mapping operations. The first, which is the quasi-static constraint, assigns a given value to the duty cycle D for every set of values of the controlling variables. These latter quantities may include output voltage, current, power and input voltage. For the quasi-static models discussed in the previous chapter, it will be this mapping which determines the characteristics of the basic power converter, i.e., whether it behaves like a voltage source, current source, etc.

The second mapping assigns a timing signal(s) to each value of the duty cycle D obtained above. This timing signal which defines the switching period, must satisfy the given duty cycle constraint. In addition, this second mapping may assign the timing signals subject to other

constraints such as a minimum "on" and "off" time or a maximum period. These additional constraints may be necessary to insure proper internal operation of the output stage, drive circuitry, and other instantaneous constraints. The quasi-static terminal characteristics will be satisfied by the duty cycle constraint alone. A block diagram of this control concept model is shown in Figure 6.1.

Consider the basic power converter shown in Figure 6.2 consisting of a chopper output stage and a specific control scheme. The control scheme for this converter is easily seen to involve some processing of the output variables (both v and i) and the input voltage V_s followed by a pulse-width modulator which generates the appropriate timing signals in this example.

Let us look at the basic characteristics of the control methodology. We see that the duty cycle will be zero if either v or i is greater than V_{ref} or I_{ref} respectively. If one of these is less than the respective reference, the duty cycle will vary from zero to its maximum value when the remaining variable varies about its reference. The duty cycle is also scaled inversely with the source voltage V_s. If we define a function f by

$$f(x) = \begin{cases} 1, & x < -\frac{1}{2} \\ \frac{1}{2} - x, & |x| < \frac{1}{2} \\ 0, & x > \frac{1}{2}, \end{cases} \qquad (6.1)$$

then we may describe the control methodology by the relation

$$D = \frac{K}{V_s} f[\, a(i - I_{ref})\,] \cdot f[\, b(v - V_{ref})\,] \qquad (6.2)$$

where K, a and b are fixed gain constants. The analog expression in Eqn. 6.2 is converted into an appropriate switch timing signal by the pulse-width modulator. More will be said about this example in the next chapter.

The expression in Eqn. 6.2 defines the control methodology - the

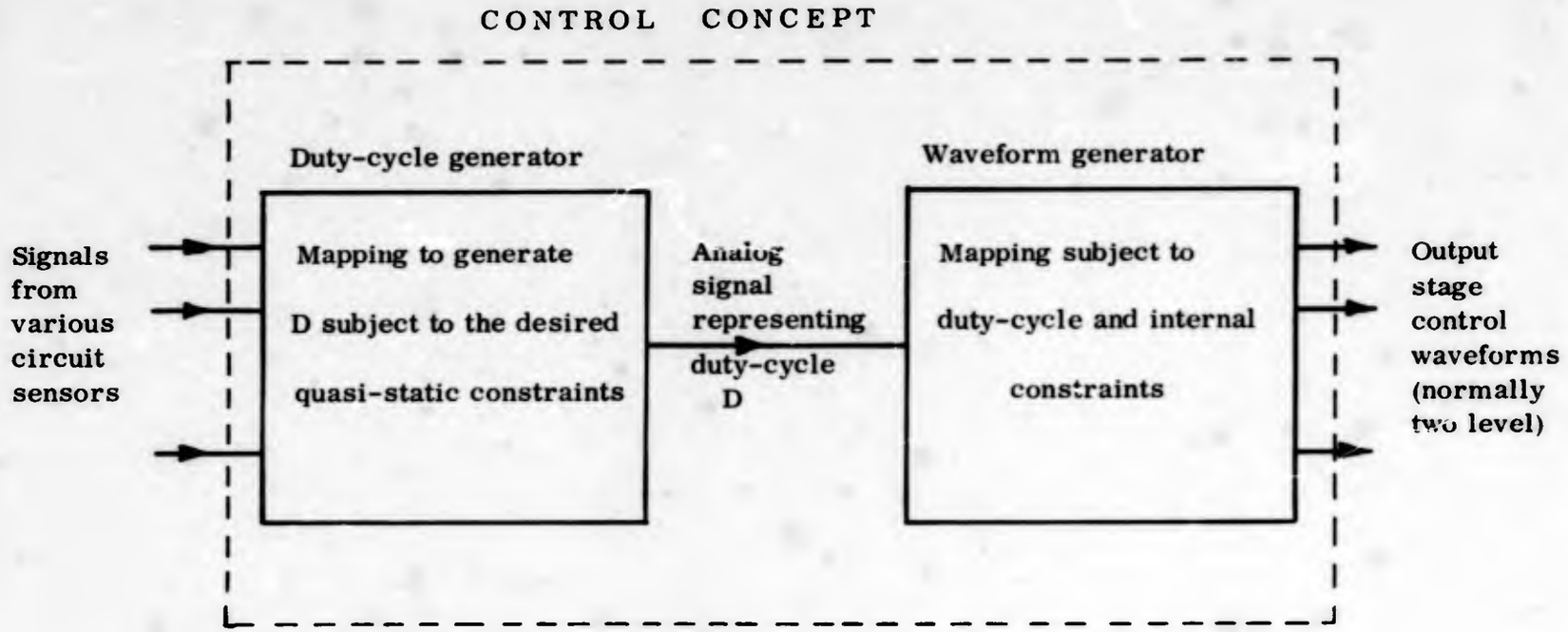

CONTROL CONCEPT
Duty-cycle generator
Waveform generator
Signals from various circuit sensors
Mapping to generate D subject to the desired quasi-static constraints
Analog signal representing duty-cycle D
Mapping subject to duty-cycle and internal constraints
Output stage control waveforms (normally two level)

FIGURE 6.1

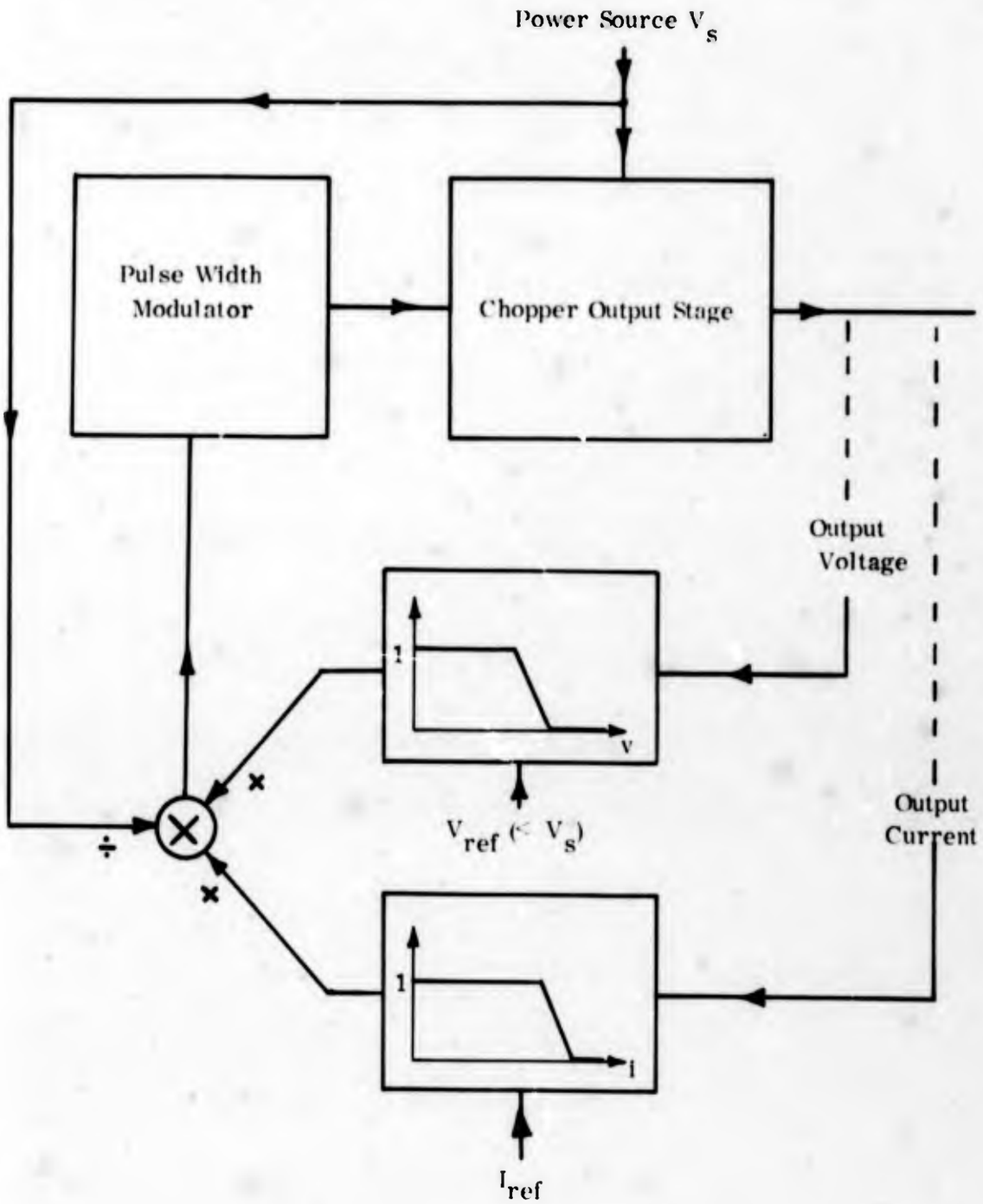


FIGURE 6.2

A BASIC POWER CONVERTER

effect that various circuit variable perturbations have on the output stage control. This we distinguish from the method used to effect the desired control on the output stage. Quasi-statically at least, a pulse-frequency modulator could be used instead of the pulse-width modulator illustrated to realize the identical control characteristics. The reasons affecting a decision as to what type of realization is needed will depend on other considerations as mentioned before. The circuitry which generates the switch control signals defines two time intervals - the "on" time and "off" time of the output switches. Any realization must satisfy the desired quasi-static constraint

$$\frac{T_{on}}{T_{on} + T_{off}} = D. \qquad (6.3)$$

An infinite number of values are allowed for T_{on} and T_{off} which satisfy Eqn. 6.3. These times may also be constrained (but not by quasi-static considerations) by instantaneous considerations, device and component behavior, power levels, speed, etc.

The breakdown of a control scheme into a functional methodology and a controlled timing generator can be quite useful since many systems are readily modeled by such a division. In most cases, the quasi-static characteristics of the basic power converter are determined by the control methodology and the output stage characteristics, with the timing circuitry not explicitly affecting operation.

The topic of control concepts and associated areas could, of course, occupy much more room than we have allotted here. We have only attempted to point out the function of a control concept and a useful means of visualizing its structure.

7. CONSIDERATIONS AT THE BASIC POWER CONVERTER LEVEL

In Chapters 5 and 6, the basic characteristics of output stages and control concepts were discussed. A number of considerations can be meaningfully explored by considering these areas separately. However, when we combine an output stage with a control concept, we have essentially constructed a basic power converter, and a discussion of the characteristics of this combination can be handled separately from the component considerations.

In Chapter 5, we derived the differential equation describing the quasi-static behavior of the chopper output stage. Here we shall explore some of the limitations of basic power converters employing this output stage and the flyback output stage.

If we wish, we may divide questions about basic power converters into two classes. One consists of questions concerning terminal behavior of a basic power converter given a specific control concept and output stage while the other consists of questions concerning the characteristics of control concepts and/or output stages which yield given terminal characteristics. Questions of the latter type can be quite useful in uncovering basic limitations. We shall address ourselves to a few questions of this type.

7.1 LIMITATIONS OF BASIC POWER CONVERTERS WITH A CHOPPER OUTPUT STAGE

A number of limitations inherent in basic power converters employing the chopper output stage may be derived from Eqn. 5.7. One is the static constraint

$$|V_o| \leq |V_s| \tag{7.1}$$

which is due to the limitation of the duty cycle between zero and one.

Let us consider some dynamic limitations of the system. We shall not specify any control scheme. Instead, we shall see if there is an optimum choice of such a relation for a given set of conditions. One frequently occurring situation is that for which a constant output voltage

V_o is desired for both line and load changes. If there is a control relation which provides the desired output characteristic, then we may find it by assuming $v_o(t) = V_o$ in Eqn. 7.1. Since all time derivatives of $v_o(t)$ will be zero with this assumption, we obtain

$$\left[L\frac{dG}{dt} + 1 \right] V_o = D(t)v_s(t), \qquad 0 \le D(t) \le 1. \qquad (7.2)$$

If we consider input line variations only and assume that the load conductance G(t) is constant, then we get

$$V_o = D(t)v_s(t)$$

or

$$D(t) = \frac{V_o}{v_s(t)} \qquad (7.3)$$

as the desired control relation to maintain a constant voltage output V_o. Since D(t) must be between zero and one, we obtain the restriction

$$v_s(t) \ge V_o \text{ for all } t. \qquad (7.4)$$

The implication of Eqns. 7.3 and 7.4 is that a transient must occur if the input $v_s(t)$ drops below the desired output V_o, and that no control relation exists which can eliminate it, although some may provide a more tolerable transient than others.

Similarly, if the source is a constant V_s and the load is allowed to vary, we obtain the equation

$$\left[L\frac{dG}{dt} + 1 \right] V_o = D(t)V_s$$

or

$$D(t) = \frac{\left(L\frac{dG}{dt} + 1 \right) V_o}{V_s} \qquad (7.5)$$

This is the required control relation for a fixed input V_o and a variable load. Immediately, we can see that it is impossible to maintain a constant output V_o when there is a step load change, since the right side of Eqn. 7.5 is infinite for such a case. Again, this is true regardless of the control scheme used. Interestingly, Eqn. 7.5 places a constraint on the time rate-of-change of the load but not on the value of the load itself. This limitation may be found as follows:

$$0 \leq D(t) \leq 1.$$

Therefore,

$$0 \leq \frac{\left(L \frac{dG}{dt} + 1 \right) V_o}{V_s} \leq 1,$$

$$-V_o \leq V_o L \frac{dG}{dt} \leq V_s - V_o,$$

$$-\frac{V_o}{L} \leq \frac{d\left[V_o G(t) \right]}{dt} \leq \frac{1}{L}\left(V_s - V_o \right)$$

or. since the load current is $i_G(t) = V_o G(t)$, we obtain

$$-\frac{V_o}{L} \leq \frac{di_G}{dt} \leq \frac{1}{L}\left(V_s - V_o \right) \qquad (7.6)$$

This result is simply a current constraint due to the inductor L since the left-most and the right-most expressions in Eqn. 7.6 are just the limits on the time derivative of the inductor current when the duty cycle takes the values zero and one respectively. Note that the larger the output voltage V_o is, the smaller the allowable current slope is in the positive direction.

The two cases just discussed show some of the limitations basic to basic power converters employing the chopper output stage. One case of interest for which these limitations are exceeded is that of a

step change in load. As mentioned before, it is impossible to avoid a voltage transient, regardless of the control scheme used. However, an optimum control relation exists which will minimize the transient if an error criterion is given, although finding this relation presents analytical difficulties. Such an optimum relation may be a function of the input voltage $v_s(t)$ and the load current $i_G(t)$ as well as the load voltage $v_o(t)$.

A more detailed model than the one illustrated in Figure 5.21 may be developed by accounting for various non-ideal element behavior. For example, if we wish to model the ESR (equivalent series resistance) of the capacitor C, the equivalent loss resistance of the inductor L and the "on" resistance of the switches, we can use the model shown in Figure 7.1.

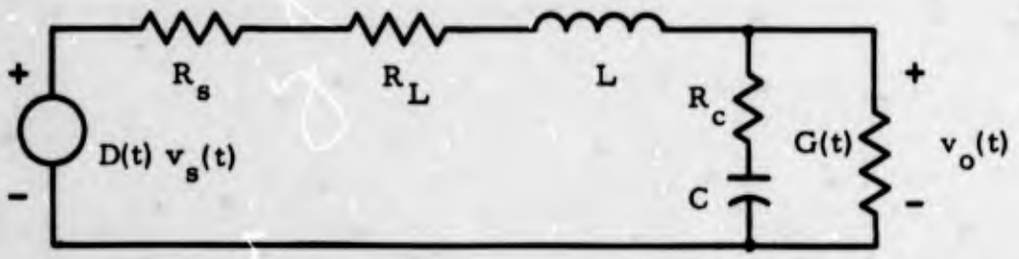


FIGURE 7.1

QUASI-STATIC MODEL OF A CHOPPER WITH SOME OF THE ELEMENT LOSSES MODELED

The differential equation describing the behavior of this model can be written using the usual techniques. The basic limitations, both static and dynamic, which applied to the model of Figure 5.21 also apply here.

7.2 LIMITATIONS OF BASIC POWER CONVERTERS EMPLOYING THE FLYBACK OUTPUT STAGE

We may derive some limitations on the performance of a basic power converter when the flyback output stage is used. In order to do this, we shall need the quasi-static equation describing the flyback

output stage. Since this was not done in Chapter 5, we shall do it here first and then proceed to derive some limitations of this output stage.

The derivation of the quasi-static equations for the basic flyback output and the modified flyback output circuits of Figure 5.15 is similar for all of these circuits, so that only the equation describing the basic flyback circuit of Figure 5.15b will be derived here. Using the notation of Figure 7.2, we have for the quasi-static components, ignoring switching frequencies,

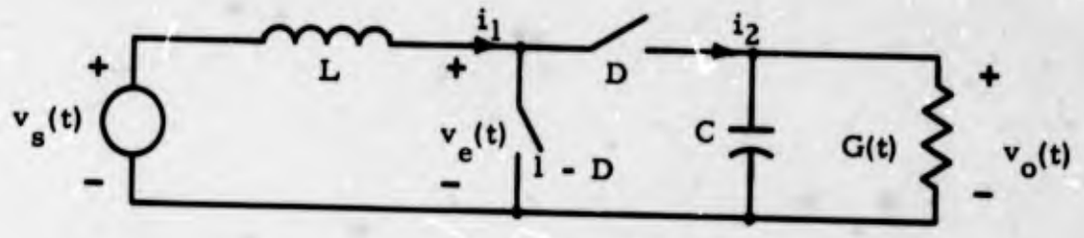


FIGURE 7.2

BASIC FLYBACK OUTPUT STAGE

$$v_e(t) = D(t)v_o(t)$$

$$i_2(t) = D(t)i_1(t) \qquad (7.7)$$

where D(t) is the switch duty cycle as indicated. Writing KVL around the left-most loop and KCL at the top right node, we get

$$L\frac{di_1}{dt} + v_e(t) = v_s(t)$$

$$C\frac{dv_o}{dt} + G(t)v_o(t) = i_2(t) \qquad (7.8)$$

With the four equations in 7.7 and 7.8, we may eliminate the three variables $i_1(t)$, $i_2(t)$ and $v_e(t)$ to obtain a differential equation relating $v_s(t)$, $v_o(t)$ and $D(t)$. If this is done, the resulting equation is

$$\frac{LC}{D(t)}\frac{d^2v_o}{dt^2} + \frac{L}{D^2(t)}\left[G(t)D(t) - C\frac{dD}{dt}\right]\frac{dv_o}{dt}$$

$$+ \left[D(t) + L\frac{d}{dt}\left(\frac{G(t)}{D(t)}\right)\right]v_o(t) = v_s(t), \qquad 0 \le D(t) \le 1. \quad (7.9)$$

The static transfer characteristic of the basic flyback output is obtained from Eqn. 7.9 by assuming all quantities are constants and all time derivatives are zero. This gives

$$V_o = \frac{1}{D}V_s. \qquad (7.10)$$

Limitations on dynamic behavior of basic power converters employing this circuit can be investigated by considering Eqn. 7.9 in more detail. Again, as with the chopper, we shall assume that the output $v_o(t)$ is to be kept at a constant voltage V_o. If the load $G(t)$ is kept constant and the source voltage $v_s(t)$ is allowed to vary, we obtain the following equation from Eqn. 7.9:

$$LG\frac{dD}{dt} = D^3(t) - \frac{1}{V_o}D^2(t)v_s(t), \qquad 0 \le D(t) \le 1. \qquad (7.11)$$

When the source voltage is a step from V_o to $V_o + \Delta V$ and the system is in steady-state operation before the step is applied, the resulting control function $D(t)$ which maintains a constant output V_o after the step is sketched in Figure 7.3. The resulting solution shows that the required $D(t)$ exceeds one for $\Delta V < 0$ which makes realization theoretically impossible. For $\Delta V > 0$, a transient solution is obtained for which $D(t) \longrightarrow 0$ as $t \longrightarrow \infty$.

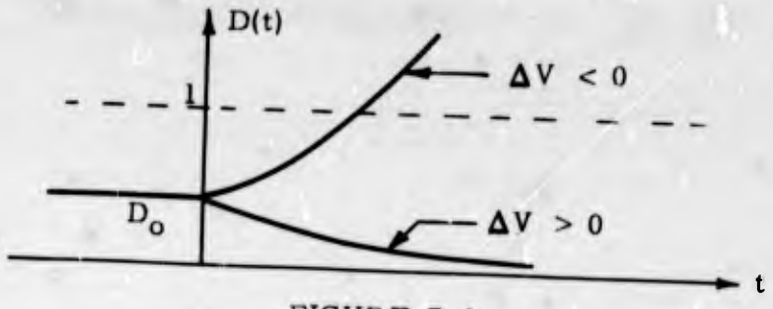


FIGURE 7.3

OPTIMUM THEORETICAL CONTROL FUNCTIONS FOR A FLYBACK OUTPUT WITH A STEP SOURCE CHANGE

This solution is theoretically realizable with ideal components since $0 \leq D(t) \leq 1$, but is practically unrealizable for two reasons. First, this solution requires the inductor current to approach infinity for large t. Second, a physically realizable solution should approach the static solution for D(t) when $t > 0$. This asymptotic value is given by

$$D_{static} = \frac{V_s + \Delta V}{V_o} . \qquad (7.12)$$

There are two interesting points which result from a consideration of Eqn. 7.11. One is that theoretically realizable solutions for D(t) exist which are time-varying, yet will yield a constant output voltage with a constant source voltage. Second, the results obtained above show that any control function D(t) which is constrained to approach the static solution in Eqn. 7.12 after a step source change must produce a transient in the output voltage. Since all physical control systems are so constrained, the flyback output necessarily produces an output transient in response to a step source change. (The transient may possibly be made acceptably small. It is only the complete absence of a transient that is theoretically prohibited with the given control constraints.)

The behavior of the flyback output in response to load transients can be found from Eqn. 7.9. Here, we shall assume that $v_s(t) = V_s$

and that $v_o(t) = V_o$ are both constants. With this assumption, we obtain the equation

$$D(t) + L\frac{d}{dt}\left[\frac{G(t)}{D(t)}\right] = \frac{V_s}{V_o} = D_o \qquad (7.13)$$

where D_o is the static solution to Eqn. 7.9. If G(t) takes a step change at t = 0, a closed form relation describing D(t) can be found from Eqn. 7.13. The resulting D(t) is sketched in Figure 7.4 for both step increases and decreases in the load G(t). There is a theoretically realizable solution for step decreases in load ($\Delta G < 0$) and none for step increases in load. Practically, none of these are realizable since none approach the static solution D_o. Therefore, any control function which does approach the static solution must produce an output voltage transient, although it may be small.

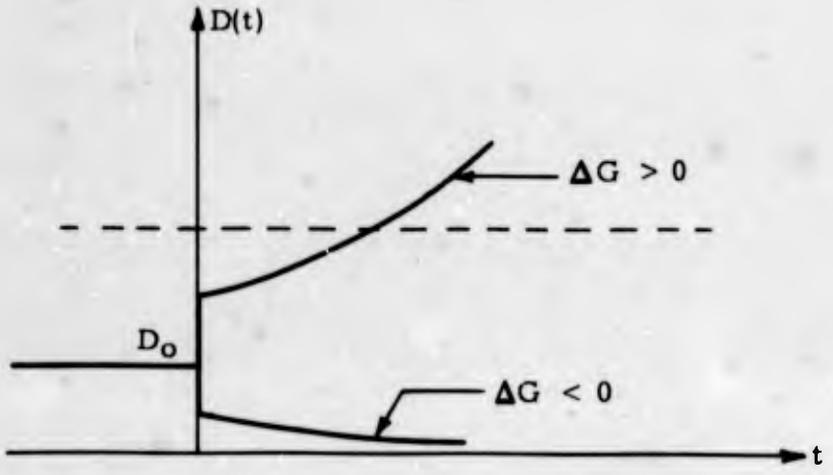


FIGURE 7.4

OPTIMUM THEORETICAL CONTROL FUNCTIONS FOR A FLYBACK OUTPUT WITH A STEP LOAD CHANGE

The flyback output stage is thus incapable of compensating for either load or source changes without producing a transient in the output voltage. This limitation applies with any control scheme which is required to approach a static solution.

The two quasi-static models just analyzed show some of the limitations inherent in the respective output stages. Since the quasi-static models are approximations, these models must be used carefully when predicting or describing the behavior of the actual output stages. Limitations of a circuit which are derived from an approximate model can often be useful and reasonably accurate. However, when an accurate description of the dynamic behavior of an actual circuit is desired, much more care is needed to insure the validity of the approximations used to derive the model.

These examples serve to illustrate the kinds of general limitations we may place on basic power converters by assuming certain terminal characteristics. Other questions concerning basic power converters may involve the terminal characteristics of a specific basic power converter. As an example, we shall determine the approximate static output characteristics of the basic power converter illustrated in Figure 6.2.

7.3 STATIC OUTPUT CHARACTERISTICS OF A SPECIFIC BASIC POWER CONVERTER

The control concept shown in Figure 6.2 has three controlling parameters - input voltage, output voltage and output current. This is connected with a chopper output stage to form a basic power converter. We shall determine the approximate static v-i characteristic seen looking into the output terminals by means of a qualitative discussion.

Assume that the output current i is less than the reference I_{ref}. In this case, a small change in the output voltage v about V_{ref} causes a large change in the output stage duty cycle. This duty cycle change is such as to move v toward V_{ref}. Thus, the converter acts similar to a common voltage regulator. Now, if we assume that $v < V_{ref}$, we

see that the duty cycle (and hence output voltage) is determined by the output current i such that v goes to zero if i exceeds I_{ref}. In this mode, the converter acts as a current regulator. A sketch of the output v-i characteristic is shown in Figure 7.5.

The v-i characteristic of this converter is that of a current-limited voltage source, the current limiting being introduced by the current feedback in the control concept. (We could just as well call it a voltage-limited current source, but its use as the former is more common.)

There is one remaining part of the control concept that we have not considered as yet - the dependence of the duty cycle on the input voltage V_s. Assume that the output voltage and current are fixed. As the input voltage changes, the duty cycle will vary inversely with the input voltage. The control relation of the chopper output stage is such that the output voltage v is given by $v = DV_s$. If D varies inversely with V_s, we see that v will tend to remain fixed without effects due to the output voltage feedback. In essence, we may consider this part of the control concept to be an "open-loop" control in that it tends to regulate the output voltage without direct reference to the output voltage. Introducing this type of feedback into a control concept can often improve the line regulation of the basic power converter as should be the case here.

We may summarize these results a little more quantitatively by looking at the two constraints imposed on the basic power converter. The output stage places the terminal constraint

$$v = DV_s \tag{7.14}$$

on the converter characteristic. The control concept places the constraint

$$D = \frac{K}{V_s} f\left[a(i-I_{ref})\right] f\left[b(v - V_{ref})\right] \tag{7.15}$$

which was determined in Chapter 6. By combining these relations,

we can obtain the implicit output terminal relation

$$v = Kf[\,a(i-I_{ref})\,]\; f\;[\,b(v-V_{ref})\,] \qquad (7.16)$$

which we readily observe is independent of input voltage. This result gives this idealized model its perfect line regulation.

Our purpose here has been to illustrate with quite simple examples some of the questions which are relevant in discussing basic power converters. There are many other questions, both theoretical and practical which we have not touched upon, some of which concern power losses, static and dynamic errors and baseband stability. These are all topics which must be considered in a good design or evaluation of a basic power converter.

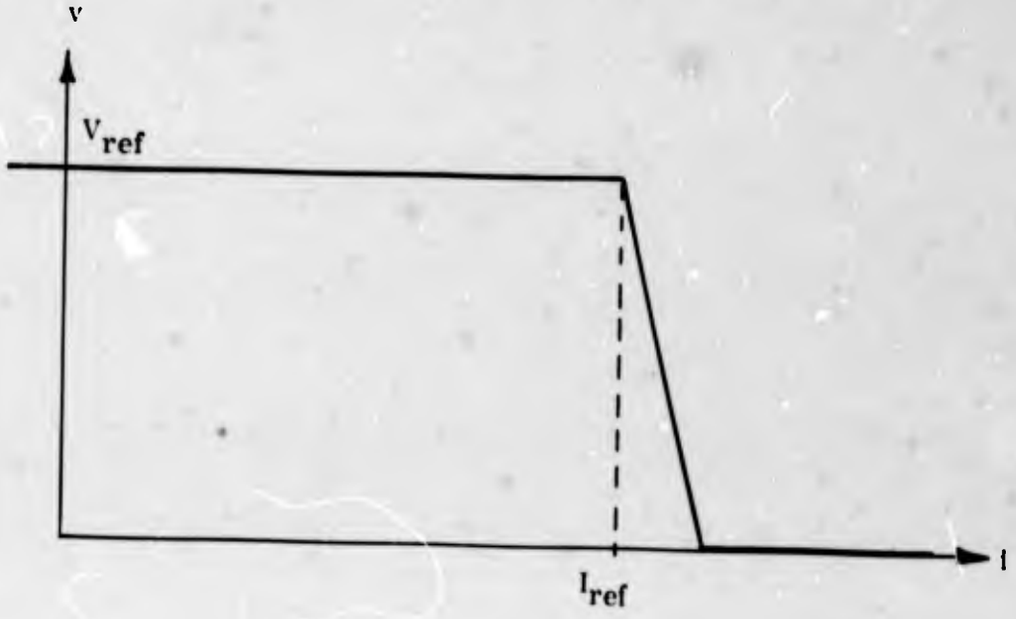


FIGURE 7.5

OUTPUT v-i CHARACTERISTIC OF THE BASIC POWER CONVERTER IN FIGURE 6.2

8. CONSIDERATIONS AT THE POWER PROCESSOR LEVEL

This section will present some elementary considerations pertinent to power processors and their internal building blocks.

As discussed in Chapter 2, a power processor is composed of basic power converters and auxiliary circuitry. The auxiliary circuitry contains all of the functions necessary to support the operation of the basic power converters. These auxiliary functions fall into two broad classes, those associated with signal processing and those associated with power processing. The power processing portions of the auxiliary circuitry, including items such as voltage converters, regulators and inverters to power the main basic power converters and signal processing circuitry may themselves be treated as basic power converters and decomposed and evaluated accordingly.

The signal processing portion of the auxiliary circuitry performs all of the functions necessary to coordinate the operation of the basic power converters and to control the operation of the power converters to meet the power processor terminal requirements. Functions such as programing or sequencing, timing, metering, signalling, interlocking, calibrating and mode switching are all types of signal processing commonly encountered in power processing. Those functions associated with switches and logic signals may be analyzed by a Boolean representation of the variables using logic analysis techniques such as those presented in Chapter 10. Switching control functions in power processors are generally designed in a straightforward intuitive manner to suit the control requirements. If the logic is combinatorial (i.e., the output of the switching network depends only on the position of the control switches), this procedure usually results in an adequate realization which performs the desired functions. If, however, the logic is sequential (i.e., the output of the switching network depends on both the position and the past history of the control switches), it is possible to realize a network which will perform properly for the normal sequence of switching, but will result in improper or undesirable operation when an abnormal, but realizable, sequency of switch operations is encountered. For this reason, sequential networks must be rigorously examined for all possible switch operating sequences and undesirable operating conditions

eliminated. Rigorous techniques, based on Boolean state variable representations of the network, for performing this analysis exist and readily lend themselves to mechanization on a computer. The techniques for circuit analysis of switching (digital) circuits have been well developed to a high level of sophistication and mechanization by computer circuit designers. These techniques are described in Bibliography II, Reference 12.

The signal processing functions which require linear or quasi-linear operations such as amplification, modulation, demodulation, function shaping, etc., generally employ circuitry which can be accurately modeled in a straightforward manner, using simple component models such as those developed in Chapter 3. Since signal processing circuitry of this type has applications which go far beyond that of power processors, analysis and evaluation of these circuits, while by no means trivial, has been the subject of intensive study and is well documented in the literature. In general, the methods employed are linear circuit analysis, if applicable, or for nonlinear circuitry, assumed state analysis as described in Section 10.4. An example of auxiliary circuitry considerations is presented in Section 12.1.

A power processor may contain one or more basic power converters. Usually the converters are connected in cascade to perform the complete power processor functions. For example, an ac - ac (frequency converter) power processor might employ an intermediate dc link between input and output. Thus, the processor would consist of an ac - dc (rectifier) basic power converter followed by a dc - ac (inverter) basic power converter to complete the conversion. Basic power converters may also be connected in parallel for redundancy (employed to achieve greater reliability), to select alternate functions, or to provide increased output capability.

A power processor is externally modeled in terms of its terminal constraints. When performing an evaluation of a power system, the concept of terminal constraints may be broadened beyond those of an electrical nature. Thermal characteristics among others may also be modeled (in a lumped approximation) as a set of terminal characteristics. The values of the variables at the terminals (e.g. power flow and temperature in the thermal case) are a function of the model internal to the power processor as well as the external load presented

to the terminals (c.f. Chapter 10 discussion on output impedance). In a more abstract sense, one can conceive of power processor terminal constraints relating conceptual variables such as reliability, cost, size and weight, etc. Figure 8.1 illustrates the manner in which a generalized power processor might be modeled from terminal constraints alone. Significant in a terminal constraint model is that in general the terminal constraints at any one set of terminals are a function of all the other terminal variables which, in turn, depend on the external loads. The function relating the variables is, of course, dependent on the particular power processor being examined.

The notion of terminals on a power processor which relate conceptual variables such as reliability and cost to real variables such as voltages and currents is quite obviously an artifice for the modeling of a power processor. Yet if the internal relations among the variables can be expressed in terms of terminal constraints for each of the parameters of interest, it is not difficult to see how a system composed of a multiplicity of power processors might be evaluated. Figure 8.2 shows a very simplified system of three cascaded power processors with the terminal parameters represented as signals related to the terminal parameter rather than the actual variables. The interactions between the conceptual parameters of the three power processors are not shown for simplicity. For given source and load profiles (dictated by the mission requirements), the overall system performance for the conceptual parameters can be evaluated by a suitable combination of the individual parameters. Cost, size and weight and power dissipation are simple sums of the corresponding individual parameters. Reliability is evaluated according to the pertinent mathematics from the individual reliability parameters. The real terminal variables and, hence, system performance with respect to these variables can be evaluated by system analysis techniques such as those presented in Chapter 10. The effects on the system performance of changes in the source, loads or the power processors are readily evaluated with this generalized model.

The multi-terminal power processor model might be thought of as the ultimate step in the modeling process. The detailed interrelationship among the terminal variables considered here is exceedingly complex and at the current state-of-the-art can be evaluated

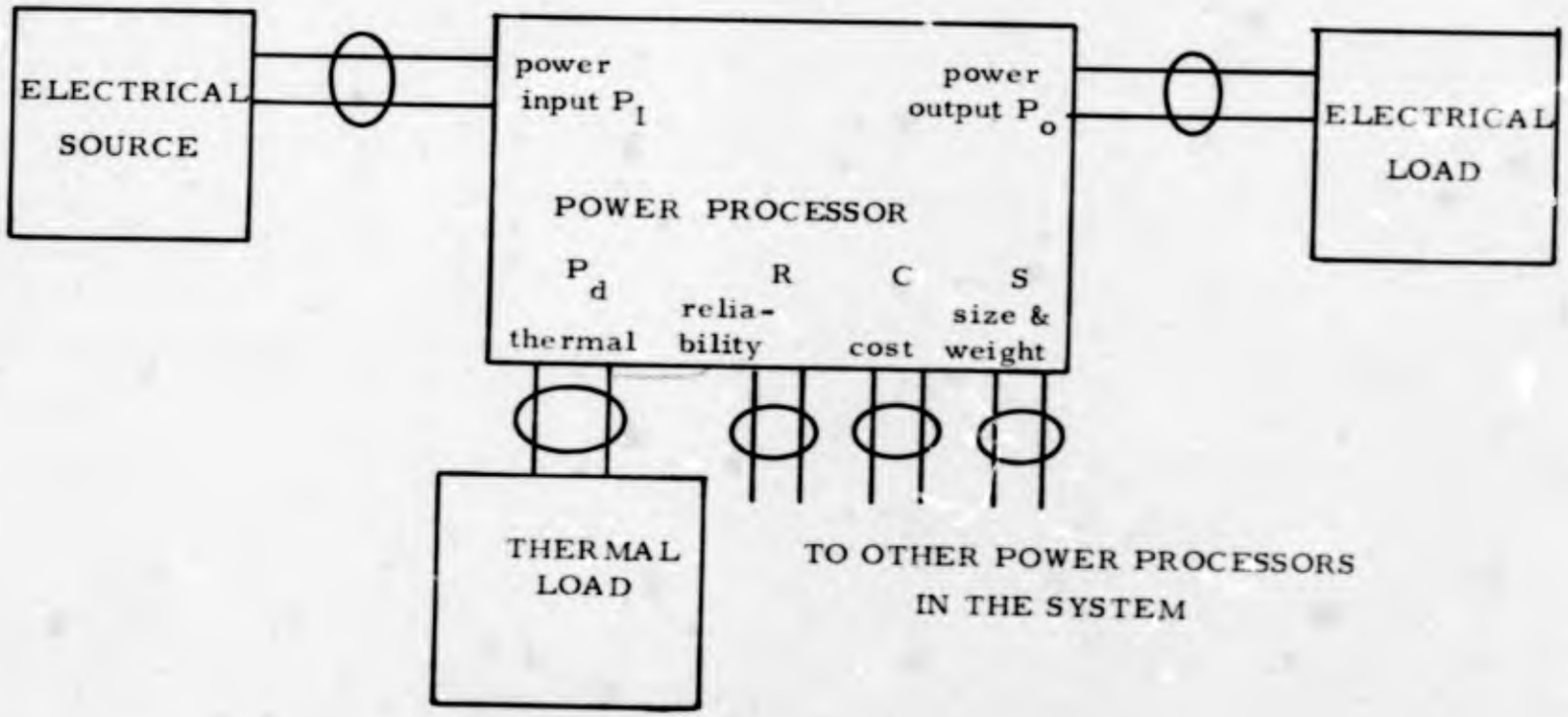


FIGURE 8.1

GENERALIZED POWER PROCESSOR MODEL

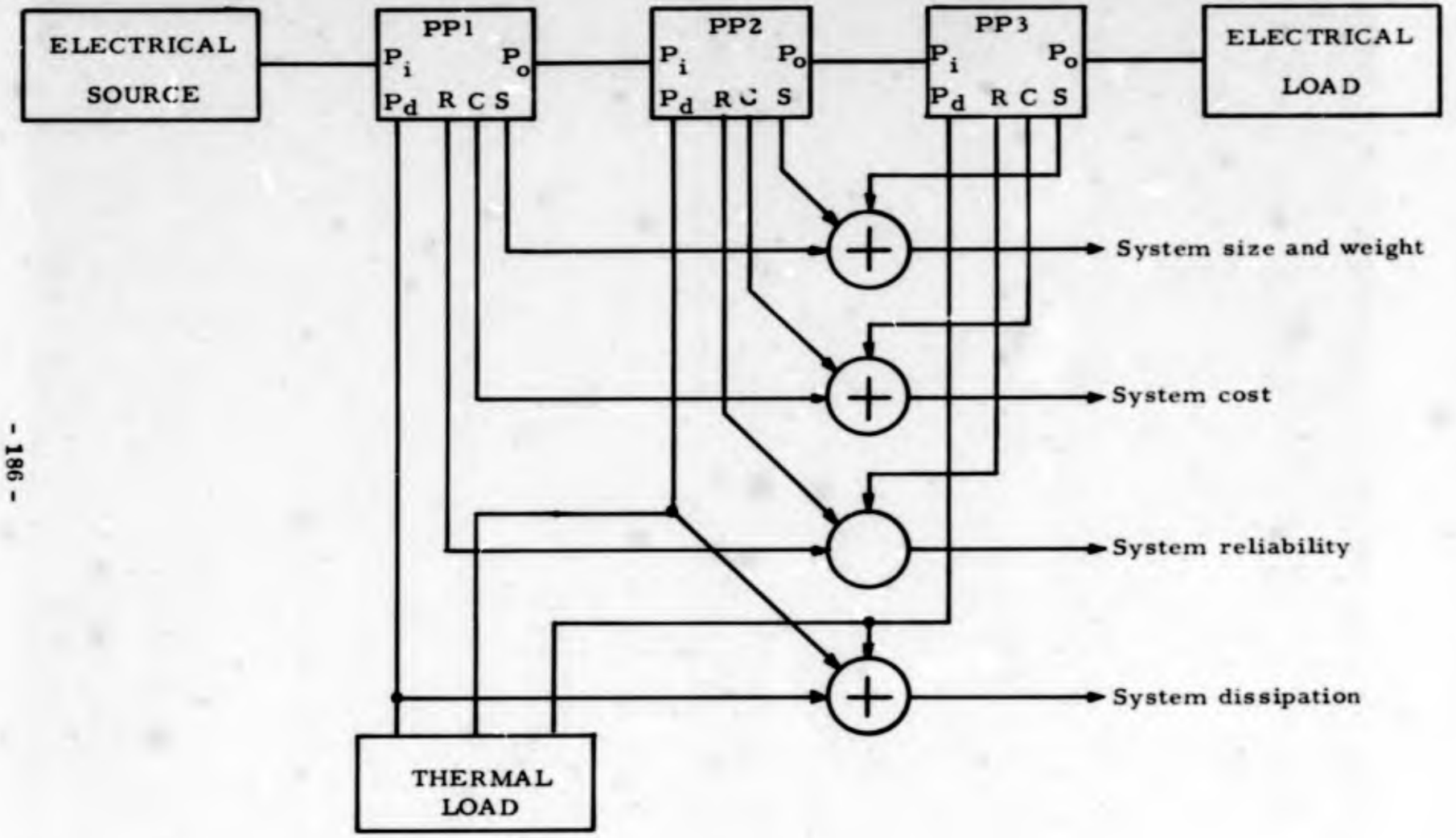


FIGURE 8.2

SIMPLIFIED SYSTEM EVALUATION

only in the most rudimentary cases. The use of computer aids holds the promise of making problems of this nature, presently intractable principally because of their complexity, manageable.

9. RECOMMENDATIONS FOR DESIGN

The bulk of this report has been concerned with problems associated with the analysis and evaluation of existing designs. This is, of course, an area of great importance and interest, but is often overshadowed by techniques and methods that lead to new designs, i.e., synthesis techniques. In the field of complex power processors, especially those employing switching or other grossly nonlinear elements, comprehensive techniques for the synthesis of practical new equipment designs do not exist. In this case, the principal design technique consists of blending a broad background of experience in the area of the desired design with analysis techniques applicable to the evaluation of proposed new approaches. Experience provides a foundation of circuit and system techniques such as those covered in the earlier portions of this report which may be combined, perhaps with new techniques added to form a possible solution to the specific design problem under consideration. Suitable analysis techniques may then be used to verify the appropriateness of the proposed design, to predict system performance with a given design and to compare various designs. In addition, experimental measurements made on a realization of the proposed design are necessary to verify the validity of the analysis. This, then is the basic approach to the synthesis of power processing systems.

When a designer begins work on a new power processor design, he finds that there are many different systems and circuits that are capable of meeting any given set of terminal specifications. Thus, we can say that we have many more degrees of freedom in our circuit design than are necessary to meet specific terminal specifications. For high efficiency power processing, switching systems such as pulse width, pulse frequency, bang-bang and different forms of two state modulation systems are all candidates for most applications in power processing. Similarly, at the circuit level, flyback circuits, direct coupled circuits, resonant pulse circuits, single ended switching circuits, push-pull and bridge circuits can be used to meet a broad class of terminal specifications.

In specific practical designs,some of the approaches can be immediately ruled out by factors such as limitations of the switching devices. For example, voltage limitations on solid state power switches may eliminate the use of single ended and some double ended circuits for certain high voltage applications. However, after such salient factors have been considered there still remain as many approaches as there are designers. From this point on, the design often proceeds on the basis of familiarity of the designer with a specific circuit or system.

It is easy to criticize this approach but much harder to construct an improved one. Technology in this field is still a long way from enabling one to synthesize an optimum system, in any sense, to meet prescribed terminal constraints. In addition, it is generally not practical for a designer to make a complete appraisal of competitive approaches because the factors that determine the ultimate merits of an approach are usually imbedded in intricacies which are revealed only after a complete design and development effort is brought to bear on the specific approach. Thus, it is not surprising that the field of power processing tends to be represented by isolated groups each promoting their specific approach. On the one hand, this phenomena brings out the best in each approach. On the other hand, in the absence of completely parallel developments for the same specifications, comparison and evaluation of competitive approaches is at best difficult and limited. Some extrapolations can be made regarding size, weight, cost and efficiency; however, crucial factors like safety margins for reliability are often hard to determine. Even for the former comparisons, the conclusions often reflect the skill of the designer as much as they do the merit of the approach. This is particularly evident in the design of the magnetics which is often a significant factor in cost, size and weight.

Thus we see that there are many approaches to the same problem and many different products all meeting the same terminal specifications. Based on these considerations and the material presented in this report, a set of design steps have been formulated which serve as a guide to the selection of an optimum power processor from the set of those that are available to the designer. Naturally, design steps are no substitute for designer creativity; however, by following these steps a designer can choose the best power processor design from among those he is capable of creating. Another designer might create a better (or worse or even equal) design because of his wider experience or creative talents, even though he follows the same procedure. The design steps serve merely as a guide to system synthesis but not as a synthesis procedure in themselves. These design steps may be stated as follows:

1) Structure the design problem as outlined in the earlier chapters of this report. This will allow attention to be focussed at the appropriate level as the design progresses.

2) Select a system configuration - a combination of power processors - that meets the system needs. This will result in a block diagram of the proposed system which performs the desired overall power processing.

3) Examine all ways of achieving the power processing required by the block diagram. Experience in the particular area of power processing and study of the available literature in the area will serve a valuable background for setting down possible combinations of power converters to form the complete power processor.

4) Analyze the approaches for theoretical efficiency and transient energy storage. Choose for further investigation the approaches which promise the highest efficiency and require a minimum of peak energy storage for proper operation. This will lead to the smallest overall system by minimizing the size of both heat removal and energy storage components.

5) Examine all known approaches to the realization of the power converters of the selected system configuration. Apply the parameters of the current problem to the various possible approaches. Some approaches may be eliminated because they place requirements on circuit components beyond the present state of the art, e.g. unreasonably high peak voltage or current levels. Others may be so clearly inferior that their further investigation would be warranted only if the more favorable approaches could not be used.

6) Analyze the performance of the possible power converter realizations under static operating conditions. Eliminate those realizations which cannot meet the requirement of the problem in terms of operation, cost, reliability, efficiency, size and weight.

7) Analyze the performance of the remaining power converter approaches under transient operating conditions. Consider turn-on and turn-off of the system and line and load fault conditions. These often represent the overall worst-case terminal constraints. One of the foremost causes of failure in switching systems is current surges in the power switching devices. These surges may appear under operation that is perfectly normal as observed from the output terminals of the system. Transformers used in a power converter realization are subject to flux limitations which can disrupt the operation of the power converter if exceeded. Therefore, it is imperative that internal operation, as well as terminal performance, be analyzed under transient conditions. Those realizations which cannot meet transient performance requirements or which cannot safely meet transient requirements without the addition of excessive circuit artifacts tacked on to the original design may be eliminated.

8) Select the most promising power converter approaches from among those remaining for detailed study. Perform a paper design of the circuit and

attempt to discover the practical limitations of the approach, e.g. maximum voltage, current and power that may be handled with available components and devices, output ripple versus load transient response, power efficiency, cost, size and weight, and reliability that may be expected.

9) Breadboard the circuit and verify the design predictions. In addition, assess the importance of difficult to model or non-ideal effects such as leakage inductance in magnetically coupled elements, diode reverse recovery time and semiconductor switch performance on operation.

10) If circuit deficiencies are found which are not fundamental in nature, concentrate research and development in the troublesome area to effect an improvement. For example, a more efficient drive circuit, faster switching power devices or a redesigned magnetic element may be tried to optimize performance. This technique provides dividends if one component or sub-circuit forms a dominant limitation on the power converter.

11) Based on the above work, select power converter designs which provide optimal performance in the particular system under study. The definition of optimal performance is a difficult one and the ultimate choice will, in all probability, reflect the personal prejudices of the designer. However, the reasons for choosing one design over others should be as explicit as possible to insure that the choice is based on rational grounds.

12) Re-evaluate overall system performance in view of any constraints that the practical realization of the power converters place on the total system.

13) Proceed with final packaging and system integration. Experience and breadboard measurements may be used to design package dependent portions of the system such as electro-magnetic interference and decoupling filters.

To finalize a design, iterations of all or a portion of the above design steps may be necessary. Iteration should be continued until an acceptable design is realized. Further iteration may be employed to refine and optimize the overall system. By following this procedure, it is hoped that the "hit or miss" method of choosing an approach to a power processing problem common in today's designs can be altered to guide the designer to the right choice of approach at the beginning of the design for a specific problem.

10. MATHEMATICAL METHODS*

Within the last decade, there has been a sharply increasing use of non-linear systems for power conversion. This is a consequence both of the high efficiency attainable with active devices operating in the switching mode and of the development of high power solid state switches.

The applications of nonlinear techniques in power conversion have developed more rapidly than have formal methods of analysis for these techniques. This fact, coupled with the additional complexity of nonlinear systems, has let to unpredicted failure modes and prototype designs unsuitable for production.

In examining the task of bringing appropriate mathematical tools to the aid of the designer, one is initially confronted with extensive literature covering the gamut from nonlinear differential equations to functional representations. However, a look at the field of power processing reveals that it is characterized by a very special class of nonlinear systems.

Switches are the interesting elements that define the class of networks to which modern power processing systems belong. In such systems, it is primarily through the switches and the characteristics of magnetic elements that nonlinearity appears. The nonlinearity introduced by the switches is of a nature that is best described analytically by defining several distinct operating regions or states for the system. Within each of these regions linear models serve to give many of the desired results. The nonlinearities introduced by the magnetic elements may be grouped into those for which the state approach is appropriate and those that are best handled by graphical or precise linear techniques.

Thus, even though the operation of power processing systems is highly nonlinear, we shall find that linear techniques, properly

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* It will be assumed that the reader is familiar with the basic concepts of linear systems as presented, for example, in Bibliography II, Reference 1.

applied and interpreted, form the basis for most of the analysis. We shall present a brief review of the basic linear techniques and follow this by a few examples of their application to nonlinear power processing systems.

10.1 REVIEW OF THE BASIS OF LINEAR SYSTEM ANALYSIS*

Definition of Linearity

The range of applicability of linear system analysis and the reasons for its relative simplicity when compared to nonlinear analysis is best understood by considering the definition of a linear operation.

Consider an operation T which, when applied to a time function x(t), yields a unique time function $T[x(t)]$. Then T applied to the time function x_1 yields $T(x_1)$ and T applied to x_2 yields $T(x_2)$. The operation T is linear if and only if

$$T(ax_1 + bx_2) = aT(x_1) + bT(x_2) \tag{10.1}$$

for all complex time functions x_1 and x_2 and for all complex constants a and b. From this definition, it is [illegible] that a linear operation has the following two properties:

1) Applying it to a constant times a function x is equivalent to applying it to x and then multiplying the result by the constant, and

2) Applying it to the sum of two functions is equivalent to applying it to each function separately and then adding the results.

We shall define a linear system as one whose excitation x and response y are related by a linear operation $T(x) = y$. A linear system

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* See Bibliography II, Reference 1.

thus has the following properties:

1) Its response to any excitation is unique,

2) Multiplying the excitation by a constant multiplies the response by the same constant,

and

3) The response to the sum of two or more excitations can be evaluated by finding the response for each excitation acting separately and then adding the responses. The latter property is commonly called the superposition property of linear systems.

Consequences of Linearity - Fourier and Convolution Techniques

The superposition property of linear systems is responsible for the relative simplicity of analysis of these systems. It enables excitations of linear systems to be handled by decomposition into elemental building blocks by techniques such as Fourier series and Fourier integral which, in turn, form the basis of the useful frequency domain considerations.

Key to the decomposition of excitations into a sum of building blocks is the notion of the eigenfunction of the system. The exponential excitation of such a system yi[illegible] an exponential response. In order for computational simplicity [illegible] result from the decomposition of an excitation into basic building b[illegible]s, these building blocks must be the eigenfunctions of the system. [illegible]r only then can the system output for each input building block be determined by simple multiplication. The Fourier series and Fourier integral are special cases of the exponential decomposition of functions which form the basis of much of linear system analysis. For periodic time functions x(t), the exponential form of the Fourier series can be written

$$x(t) = \sum_{k=-\infty}^{\infty} A_k e^{jk\omega_0 t} \qquad (10.2)$$

where k is any integer and $\omega_0 = \frac{2\pi}{T}$ where T is the period of the periodic function x(t). Taking advantage of the orthogonality of the

exponential functions under the summation in Eqn. 10.2, we obtain the following relation for finding the coefficients A_k to represent a given x(t):

$$A_k = \frac{1}{T}\int_0^T x(t)e^{-jk\omega_o t}dt \qquad (10.3)$$

Similarly, in the case of aperiodic functions, the Fourier integral enables the determination of Fourier spectrum $X(\omega)$ of a time function x(t) by the relation

$$X(\omega) = \int_{-\infty}^{\infty} x(t)e^{-j\omega t}dt. \qquad (10.4)$$

The function x(t) can be represented in terms of its Fourier spectrum $X(\omega)$ by the relation

$$x(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} X(\omega)e^{j\omega t}d\omega. \qquad (10.5)$$

Eqn. 10.5 is recognized as the limiting form of a discrete exponential decomposition of x(t) with coefficients $X(\omega)$. A time function x(t) can thus be thought of directly in the time domain or it can be interpreted in the frequency domain through examination of the Fourier spectrum $X(\omega)$.

Both the Fourier transform mentioned above and the Laplace transform, often referred to in the literature, can be thought of as special cases of an exponential transform which can be written

$$X(s) = \int_{-\infty}^{\infty} x(t)e^{-st}dt \qquad (10.6)$$

in which s is called the complex frequency. The inverse transform is

$$x(t) = \frac{1}{2\pi j}\int_{-\infty}^{\infty} X(s)e^{st}ds \qquad (10.7)$$

in which care must be taken to evaluate the integral along a proper path in the s-plane.

As mentioned earlier, these transform techniques are useful in linear system analysis because they are decompositions of time functions into exponentials which are eigenfunctions of linear systems. It is a relatively simple task to determine the response of linear systems to an exponential of any complex frequency s. Let the input to a stable linear network be $x(t) = Xe^{st}$ where X is called the complex amplitude of the input. The output for this input will be of the form $y(t) = Ye^{st}$. The ratio of the complex amplitude Y of the output to the complex amplitude X of the input is defined as the system function H(s) of the linear system. That is

$$H(s) = \frac{Y(s)}{X(s)}. \tag{10.8}$$

Thus, if the spectrum X(s) is known for the input x(t) then the spectrum Y(s) for the output y(t) is obtained simply from Eqn. 10.8 by the relation

$$Y(s) = X(s)H(s) \tag{10.9}$$

and y(t) can be obtained from an inverse exponential transform of the type given in Eqn. 10.7

$$y(t) = \frac{1}{2\pi j}\int_{-\infty}^{\infty} X(s)H(s)e^{st}ds.$$

Fortunately, H(s) is easily calculated by direct algebraic means from network equations written in terms of impedances. Thus, the exponential transforms, which are tabulated for many cases, offer a relatively simple means of calculating responses of linear systems. Equally important, however, is the insight they provide into the frequency domain picture of time functions and networks.

We have briefly discussed transform methods of relating the responses of linear systems to their excitations and have seen that these techniques depended upon the superposition property of linear systems and upon eigenfunction decomposition. There is, however, another

decomposition which is not in terms of eigenfunctions but which does depend upon superposition for its usefulness in system analysis. This is the decomposition of an excitation time function into short duration pulses (analogous to the decomposition often discussed in Riemann integration). The result is the well known convolution or superposition integral

$$y(t) = \int_{-\infty}^{\infty} h(\tau)\, x\,(t-\tau)\,d\tau \qquad (10.10)$$

expressing the response y(t) in terms of the excitation x(t) and the impulse (narrow pulse of unit area) response h(t) of the linear system. This relation enables direct computation of a system response in the domain without introducing the notion of frequency domain. However, it is often simpler to perform the Fourier transformation, the multiplication by the system function, and the inverse transformation than it is to analytically evaluate the convolution integral. This fact is often true as well for computer numerical evaluation because of the recently developed fast Fourier transform methods.

Differential Equations

The analysis of power processing systems involves considerations at both the system and circuit levels. While the Fourier and convolution techniques discussed earlier in this section are applicable to both levels, additional insight at the circuit level is often obtained directly from the use of a differential equation approach. For this reason and for the reasons that this approach establishes the concept of a system function and provides the foundation for stability analysis, we shall discuss it at this time.

All the equations that can be written for any electrical network have their origin either in the Kirchhoff laws or the voltage-current (v-i) relations of the elements. The Kirchhoff law equations consist of Kirchhoff's current law constraints on the current at connection points of a network and Kirchhoff's voltage law constraints on the voltages around closed paths in the network. These constraints always result in linear algebraic equations regardless of the nature of the elements in the network. The remaining set of constraints, the v-i

relations of the elements, describe the terminal properties of the elements and are independent of their interconnection. It is this set of constraints that reflects whether or not the network has energy storage elements and whether or not it is linear.

For a network containing linear elements, the simultaneous solution of the Kirchhoff law equations and the v-i equations for the elements yield the following general form of differential equation relating the excitation time function x to the response time function y.

$$a_n\frac{d^n y}{dt^n} + a_{n-1}\frac{d^{n-1} y}{dt^{n-1}} + \ldots + a_1\frac{dy}{dt} + a_0 y$$

$$= b_m\frac{d^m x}{dt^m} + b_{m-1}\frac{d^{m-1} x}{dt^{m-1}} + \ldots + b_1\frac{dx}{dt} + b_0 x. \qquad (10.11)$$

As discussed earlier, if the response of a linear system is known to an excitation of the form

$$x(t) = Xe^{st} \qquad (10.12)$$

for all s (where X is a complex constant known as the complex amplitude of the exponential excitation) then the response can be found to any excitation by superposition. The general solution of Eqn. 10.11 for an exponential excitation x given by Eqn. 10.12 has two parts. One part, $y_p(t)$, has the form

$$y_p(t) = Ye^{st} \qquad (10.13)$$

where Y is determined by direct substitution of x(t) and $y_p(t)$ into Eqn. 10.11 as follows:

$$\left(a_n s^n + a_{n-1} s^{n-1} + \ldots + a_0\right) Ye^{st}$$

$$= \left(b_m s^m + b_{m-1} s^{m-1} + \ldots + b_0\right) Xe^{st} \qquad (10.14)$$

which can be written in the factored form

$$Y = \frac{b_m \left(s - {}_1s\right)\left(s - {}_2s\right) \cdots \left(s - {}_ms\right)}{a_n \left(s - s_1\right)\left(s - s_2\right) \cdots \left(s - s_n\right)} X \qquad (10.15)$$

in which the ${}_ks$ and the s_k are complex constants denoting roots of the numerator and denominator respectively. The other part of the solution to Eqn. 10.11 is called the homogeneous solution $y_h(t)$ and is the solution for the excitation x(t) set equal to zero. The general form of the homogeneous solution is

$$y_h(t) = \sum_{k=1}^{n} A_k e^{s_k t} \qquad (10.16)$$

where the s_k are the roots of the denominator in Eqn. 10.15 and the A_k are the complex constants determined from initial conditions. The s_k are called the natural frequencies of the network since they represent frequencies at which it is possible (as a result of initial conditions) to have response without any excitation (i.e. x = 0). The solution is the sum of $y_h(t)$ and $y_p(t)$ which is

$$y(t) = \sum_{k=1}^{n} A_k e^{s_k t} + \frac{b_m \left(s - {}_1s\right)\left(s - {}_1s\right) \cdots \left(s - {}_ms\right)}{a_n \left(s - s_1\right)\left(s - s_2\right) \cdots \left(s - s_n\right)} X e^{st}, \qquad (10.17)$$

Steady state is said to exist when the last term in Eqn. 10.17 dominates the homogeneous solution. In such a case, the ratio of polynomials in this last term is equal to the ratio of the complex amplitudes Y of the response to the complex amplitude X of the excitation. This ratio plays a large role in the theory of linear networks. It is given the name of system function, denoted by H(s). Thus

$$H(s) = \frac{Y}{X} = \frac{b_m \left(s - {}_1s\right)\left(s - {}_2s\right) \cdots \left(s - {}_ms\right)}{a_n \left(s - s_1\right)\left(s - s_2\right) \cdots \left(s - s_n\right)}. \qquad (10.18)$$

It is interesting to note that although the system function was defined from only a part of the total solution, it contains within it enough information to completely reconstruct the original differential equation as can be seen by simply retracing the steps from Eqn. 10.15 back to Eqn. 10.11.

The system function given by Eqn. 10.18 is seen to be a function of the excitation frequency s. The magnitude of H(s) as a function of frequency $s = j\omega$ is called the frequency response of the network and the angle of H(s) as a function of frequency is known as the phase response of the network.

If the excitation frequency s coincides with any root of the denominator of H(s), the system function becomes infinite and is said to have a pole at this frequency. If s corresponds to any root of the numerator of H(s), the system function becomes zero and is said to have a zero at this frequency. At this point, we should again recall that the roots of the denominator of the system function are the frequencies s_k in the homogeneous solution. That is, the poles of the system function are the natural frequencies of the network. This relation is very useful when establishing criteria for stability as discussed below.

Basic Stability Condition

Although the literature contains different statements of stability of a linear system, the following definition enjoys wide acceptance. A linear system is stable if its response is bounded for every bounded input.

Consider first the response of a network which has some non-zero initial conditions (non-zero A_k's in Eqn. 10.17) but which has $x(t) = 0$. In order for the response y(t) to remain finite, it is clear that the real part of all of the s_k must be equal to or less than zero. (This results in constant terms or exponentially damped terms in the homogeneous solution.) Because of the identity between the natural frequencies s_k of the network and the poles of its system function, we conclude from our first consideration that stability requires all

the poles of the network system function to lie in the left half of the s-plane or on the imaginary axis.

If we now consider the complete solution for the response of a linear network as given in Eqn. 10.17, we find that poles of H(s) on the imaginary axis of the s-plane are inadmissible since they could result in an unbounded response if the excitation frequency corresponds to a pole of the system function. However, this case is often regarded as pathological in the sense that it cannot occur exactly in a physical system. For this reason, many authors simply state that a necessary and sufficient condition for the stability of a linear system is that its system function have no poles in the right half of the s-plane.

Techniques for Investigating Stability

This simple statement of no right half-plane poles for stability is very basic and is often confused with methods of testing for right half-plane poles such as the Routh-Hurwitz criterion, the Nyquist criterion, and the Root-Locus method. All of these criteria are only methods for testing for right half-plane poles and they in no way imply any more fundamental notions of stability.

The Routh-Hurwitz criterion is simply an algebraic process for testing the denominator polynomial of the system function for right half-plane zeros without actually factoring the polynomial.*

The Root Locus method is a procedure in which the roots of the denominator of the system function are plotted as a function of a particular system parameter, say the gain of an amplifier in the network, for example. The resulting locus of roots then indicates what range of the parameter is permitted for the roots to remain in the left half-plane.**

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* See Bibliography II, Reference 7.

** See Bibliography II, Reference 3.

The Nyquist criterion is a method of plotting the system function in the complex plane as a function of frequency $s = j\omega$. The method detects the number of excess poles over zeros of the system function in the right half-plane by the number of net counterclockwise encirclements of a specific point as $s = j\omega$ ranges from $-j\infty$ to $+j\infty$.*

While the various procedures mentioned are simply tests for the presence of right half-plane poles, they can sometimes also give us useful information beyond the direct issue of stability. In particular, they can sometimes give us performance measures such as the gain and phase margins made obvious by the plot constructed for the Nyquist criterion.* These gain and phase margins in turn relate to performance specifications such as ringing and overshoot. The latter, and for that matter all performance properties of the system, can also be determined directly from the system function and its uniquely related step response.

Closed-Loop Systems

The preceding discussion of stability assumed no constraint on the systems other than linearity (and time invariance which was not discussed). It can be shown that networks consisting entirely of positive resistance, capacitance and inductance elements are stable. The possibility of instability, which implies, as we have seen, that the network could exhibit a continued increasing output with no excitation, arises in such networks only through the introduction of amplifiers and feedback. Such situations can be modeled by block diagrams of the type shown in Figure 10.1. The system function for such a system can be written

$$H(s) = \frac{Y}{X} = \frac{K(s)}{1 + \beta(s)\, K(s)} . \qquad (10.19)$$

As we have discussed, stability implies and is implied by the statement that H(s) has no right half-plane poles. In practical designs,

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* Bibliography II, Reference 7.

K(s) and $\beta(s)$ never have any right half-plane poles so stability requires that the denominator in Eqn. 10.19 have no right half-plane zeros. This is,

$$1 + \beta(s)\, K(s) \neq 0 \text{ for any } \mathrm{Re}\,[s] > 0, \qquad (10.20)$$

where Re [ ] denotes the real part of the quantity within the brackets. The quantity $\beta(s)$ K(s) can be interpreted (Figure 10.1) as the open-loop gain of the feedback system. Thus, the concept of stability of a closed-loop system can be investigated as a function of the open-loop gain of the system. For example, the Nyquist criterion which involves encirclements of the origin for the denominator of H(s) simply involves encirclements of the point -1 for the open-loop gain $\beta(s)$ K(s).

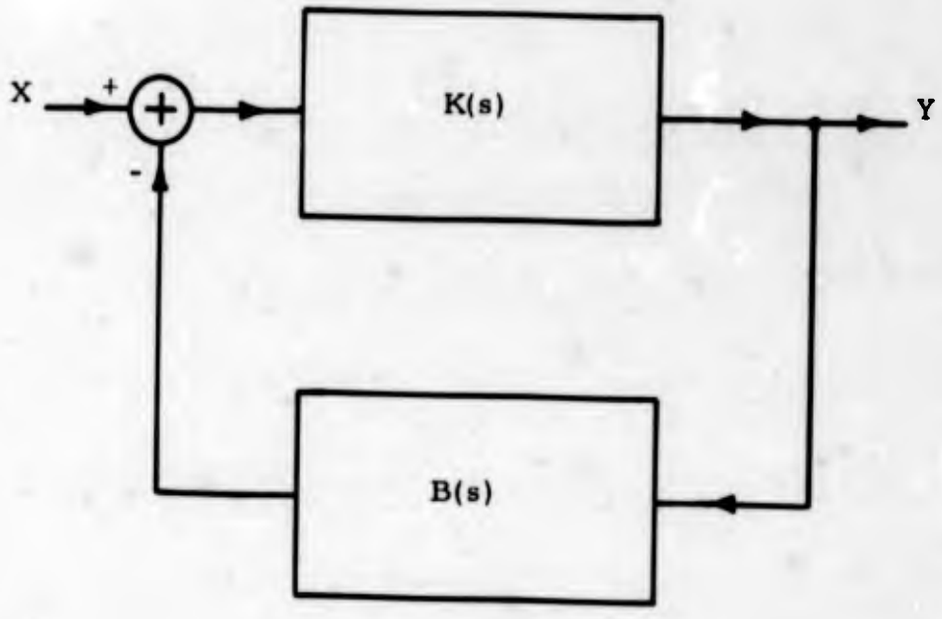

FIGURE 10.1

BLOCK DIAGRAM FOR A SIMPLE FEEDBACK SYSTEM

While it is a relatively straightforward process to determine stability for a given linear closed-loop system by the methods discussed, it becomes more challenging to design a stable system under high performance constraints which usually require a very high open-loop gain. This is the subject of linear control system design and is well documented in the literature. In the scope of the present work, we shall discuss such problems only as they appear in the design of switching-type power processors.

We have taken the time to briefly review the basis of linear system analysis because so much of it is useful in the analysis of power processing systems for which the primary source of nonlinearity is switches. In this report, we shall proceed to illustrate some of the analytic tools that are particularly useful to nonlinear switching systems. It will be seen that most of these tools will call, in one form or the other, on the linear analysis discussed in this section.

10.2 OUTPUT IMPEDANCE AND STABILITY OF SWITCHING-MODE POWER PROCESSORS

For any system which must deliver power into some load, the output impedance of the system is an important parameter which yields information relating to load regulation, transient response, frequency response and stability. Although a system may perform reasonably well even with degraded response and/or regulation characteristics, stability is probably the most important consideration, since an unstable system is usually intolerable.

In this section, we shall consider a certain class of high frequency switching systems which can, for certain purposes, be modeled by equivalent linear systems. This class of systems, including pulse-width and pulse-frequency modulation, is characterized by a switching frequency much higher than the frequencies of the signals to be processed. The low frequency band (including dc) occupied by the signals of interest is called the baseband. For these systems, we shall define the term unconditional stability and state the criterion a system must satisfy in order to be unconditionally stable. Here our stability criterion applies only to baseband operation, since we know a priori that the system is oscillating internally at the switching

frequency. The success of this procedure depends on the ability to construct a linear model of the system which ignores switching frequencies and considers the system to be operating solely in the baseband. The application of this technique should be made clear by the following examples, in which we shall compare the terminal characteristics of two switching regulator/amplifiers, a pulse-width system and a current-controlled two-state system.

First, let us consider the pulse-width system illustrated in Figure 10.2. Here the output voltage $v_o(t)$ is compared with a reference $v_r(t)$ and the resulting error signal $v_e(t)$ is then amplified and used to control the duty cycle of the pulse-width modulator. In this example, the error amplifier has a single time constant rolloff. This may be due to the inherent bandwidth of the amplifier or it may be specifically introduced to reduce any ripple components at the switching frequency. If the switching frequency of the PWM is much higher that the cutoff frequency of the LC filter (which is usually true by design), then we may assume that ripple components at the output terminals are small. We shall also assume that no ripple components appear at the input to the PWM. With these assumptions, the output of the PWM may be replaced by its average value as far as the output terminals are concerned. The average value of the PWM output is proportional to the modulator duty cycle, which in turn is dependent on the input to the modulator. Based on these postulates, we may model the PWM as a voltage-controlled voltage source to obtain the linear model shown in Figure 10.3. Here we have used a unity voltage transfer characteristic for the modulator model since we may lump any gain factor into the error amplifier gain K without loss of generality.

The model in Figure 10.3 contains only linear elements and sources so that we may determine a Thevenin equivalent network, composed of one voltage source in series with a single impedance as shown in Figure 10.4, which has terminal characteristics identical to the original model. This implies that the original system may be completely described by two parameters, the Thevenin equivalent voltage $v_{oc}(t)$ and the Thevenin equivalent impedance $Z_o(s)$, as far

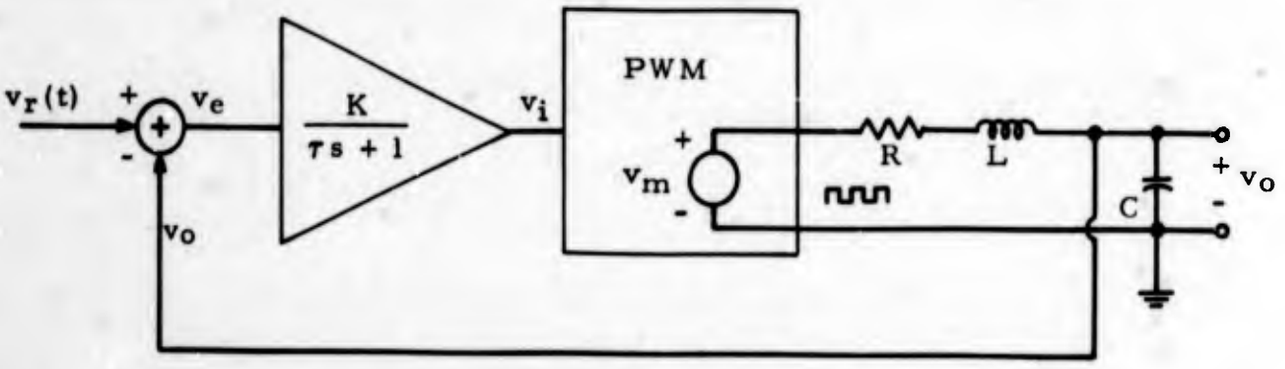

FIGURE 10.2

SIMPLIFIED MODEL OF A PWM REGULATOR

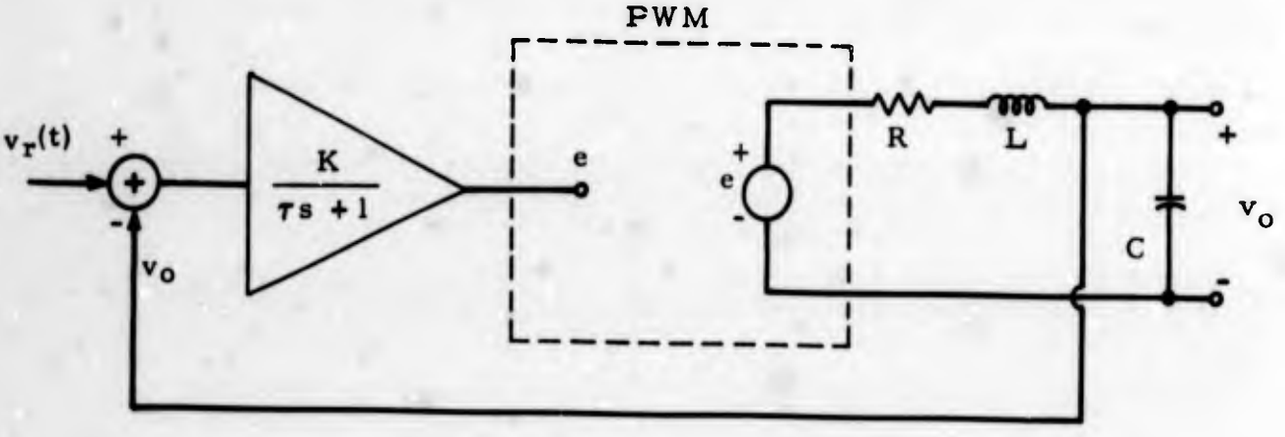

FIGURE 10.3

LINEAR EQUIVALENT OF THE PWM SHOWN IN FIGURE 10.3

as terminal characteristics are concerned. Applying the techniques of linear analysis to the model in Figure 10.3, we find for the Thevenin parameters

$$Z_o(s) = \frac{L\tau s^2 + (L + R\tau)s + R}{LC\tau s^3 + (LC + RC\tau)s^2 + (RC + \tau)s + 1 + K} \qquad (10.21)$$

$$V_{oc} = \frac{K}{LC\tau s_o^3 + (LC + RC\tau)s_o^2 + (RC + \tau)s_o + 1 + K} V_r \qquad (10.22)$$

where V_{oc} and V_r are the complex amplitudes of $v_{oc}(t)$ and $v_r(t)$ and s_o is the complex frequency of these sources. As we can see from Figure 10.4, $v_{oc}(t)$ is the open circuit (or no load) output voltage and $Z_o(s)$ is the output impedance of the system. The dc ($s = o$) output resistance is given by

$$Z_o\big|_{s = o} = \frac{R}{1 + K} \qquad (10.23)$$

and the no load dc output voltage is given by

$$V_{oc}\big|_{s_o = o} = \frac{K}{1 + K} V_r \qquad (10.24)$$

assuming that the reference $v_r(t)$ is a constant V_r.

The load regulation of a system is a function of the output resistance of the system, with smaller resistances providing better load regulation. From Eqn. 10.23, we see that the output resistance of the system can be lowered by increasing K, the gain of the error amplifier, and that an arbitrarily low dc output resistance could be obtained by making K large enough. This statement is true as far as output resistance is concerned, but it neglects consideration of the system stability.

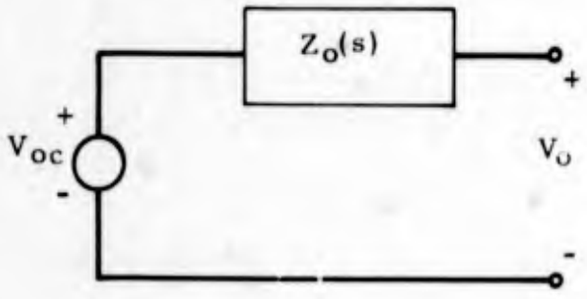

FIGURE 10.4

THEVENIN CURRENT EQUIVALENT OF PWM IN FIGURE 10.2

The system function relating two variables in a linear system is stable if that system function has no poles in the right half-plane. The presence of such poles would indicate the existence of natural behavior modes with constant or exponentially increasing amplitudes. Since V_{oc} and $Z_o(s)$ given by Eqns. 10.21 and 10.22 completely describe the system, we may be tempted to impose the condition that $Z_o(s)$ have no right half-plane poles, which in turn will place limits on the allowed values of K. However, this condition will insure stability of the system only when no load is connected, as shown in Figure 10.4. It does not give any stability information about the system when a load is connected to the system, as shown in Figure 10.5. The reason for this will be apparent from the following discussion.

Here we must point out the distinction between a circuit and a system function. A system function is an explicit relation between two variables in a linear system. Various system functions may be determined in any given circuit. The distinction above becomes quite important when we discuss networks with terminals. For such systems as voltage regulators for example, we would like to be able to connect any of a number of different load networks to the regulator. The resulting overall network, of course, will change whenever the load network changes - and the system function relating any two network

variables will, in general, also change. Thus, when we evaluate the stability of a system function for such a system, any results obtained relate only to the specific overall network analyzed - the regulator and a specific load.

Certain systems of interest can be completely specified in that there are no terminals to which some unknown load may be connected. For these systems, we may unambiguously write any desired system function and test it for stability. Only one such system function need be tested to determine the stability of the entire system. Any of a number of procedures, such as the Routh-Hurwitz criterion or a Nyquist plot, may be used to determine the presence of right half-plane poles. It should be remembered that all of the procedures for testing a system for stability are just means of determining the locations of the poles, a fact which is often obscured by the seeming complexity of some of the techniques used.

For systems such as that depicted in Figure 10.2, the system function of interest cannot be written explicitly unless we know the characteristics of the network attached to the terminals of the system. Without such a characterization, we have no system function to which we may apply a test for stability. In order to illustrate this problem, let us consider the system in Figure 10.2 for which we have constructed the Thevenin equivalent shown in Figure 10.4. If we attach a load $Z_L(s)$ to the terminals of the system, we have the network illustrated in Figure 10.5. Assuming that the transfer characteristic from V_{oc} to V_o is the system function of interest, we may write

$$H(s) = \frac{V_o}{V_{oc}} = \frac{Z_L(s)}{Z_o(s) + Z_L(s)}. \qquad (10.25)$$

Since $Z_L(s)$ is not necessarily known, we cannot apply the test for stability in the usual manner. If, however, $Z_L(s)$ is restricted to a certain set of load impedances, we may ask if there are any constraints we can impose upon V_{oc} and $Z_o(s)$ which will insure that the system function given by Eqn. 10.25 will be stable as long as $Z_L(s)$ is restricted to a given set of loads. We have not changed our criterion for the stability of a system function, but we have asked if the

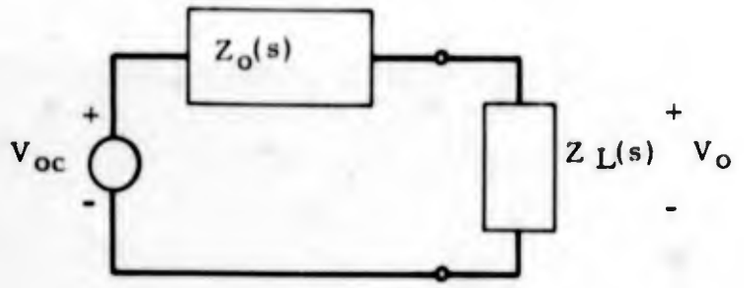

FIGURE 10.5

THEVENIN EQUIVALENT OF PWM WITH A LOAD CONNECTED

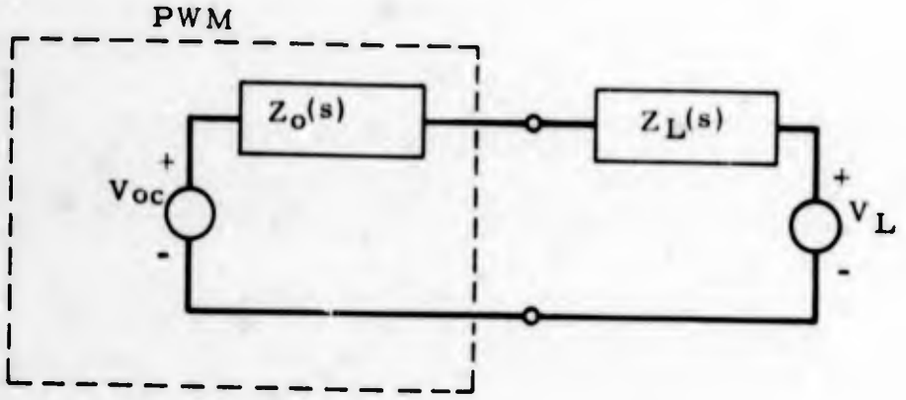

FIGURE 10.6

LINEAR MODEL OF THE PWM WITH A LOAD CONTAINING AN EQUIVALENT VOLTAGE SOURCE

stability criterion for the system function H(s) in Eqn. 10.25, which we cannot explicitly determine, can be satisfied by imposing suitable constraints on $Z_o(s)$, which is independent of the load $Z_L(s)$.

We shall determine the constraints which must be placed on $Z_o(s)$ when $Z_L(s)$ is restricted to be a linear, passive load. A passive impedance will be defined as one which cannot deliver average power under any circumstances. (A negative resistor is an active impedance and not passive since it can deliver average power). Mathematically this is equivalent to requiring $Z_L(s)$ to be a positive real function of the complex frequency s, which means that $Z_L(s)$ is real when s is real and

$$\mathrm{Re}[Z_L(s)] \geq 0 \text{ whenever } \mathrm{Re}[s] \geq 0. \qquad (10.26)$$

All impedances composed of positive R's, L's and C's are passive, although the class of passive impedances is not restricted to these. The absence of right half-plane poles and zeros is a necessary but <u>not</u> sufficient condition for passivity.

We shall define a system with terminals to be <u>unconditionally stable</u> if the system is stable when any incrementally passive load is connected to it. This allows a load of the form shown in Figure 10.6 which in toto is active but whose incremental or Thevenin equivalent impedance $Z_L(s)$ is passive. Such an equivalent might be a reasonable model for a motor when acting in its generating mode. In any case, the presence of the independent source V_L in Figure 10.6 does not affect the constraint which must be imposed on $Z_o(s)$, so that we may consider the situation illustrated in Figure 10.5 without loss of generality.

The system function H(s) relating V_{oc} and V_o in Figure 10.5 is given by Eqn. 10.25. A necessary and sufficient condition for H(s) to be stable for any passive $Z_L(s)$ is that $Z_o(s)$ be a passive impedance. It is worth repeating that requiring $Z_o(s)$ to be passive is more restrictive than requiring $Z_o(s)$ to have no poles or zeros in the right half-plane.

There are a number of simple tests by which a function may be tested for passivity or positive real character.*

We may now apply one of these tests, which requires only the $j\omega$-axis behavior of the function, to the impedance $Z_o(s)$ in Eqn. 10.21, which gives the output impedance of the PWM system shown in Figure 10.2. After performing such a test, we find that $Z_o(s)$ is passive, or that the PWM system is unconditionally stable, when

$$-1 < K < \frac{R\tau}{L}. \tag{10.27}$$

This bound on K guarantees the stability of the system when any incrementally passive load is connected to it, assuming, of course, that the linear model we have constructed is valid in the baseband.

Not all passive impedances can be realized as an RLC network, but passive impedances which are rational functions of s (the ratio of two polynomials in s) can be so realized. With K restricted by Eqn. 10.27 above, $Z_o(s)$ can be realized as an RLC network. This network, together with the Thevenin equivalent voltage given by Eqn. 10.22, determines the terminal characteristics of the system. A realization of this open-loop model with element values is shown in Figure 10.7. The source in this model is represented by a complex amplitude and not a time function. Although this model completely determines the terminal behavior of the system, it is difficult to visualize what the system does. An equivalent open-loop model with identical terminal characteristics can be derived which shows more clearly the signal processing involved. Such a model is shown in Figure 10.8. In this model, the effects of feedback have been modeled by the reduced series resistance, the introduction of a parallel RL network, and the amplifier and filter following the reference $v_r(t)$.

At this point, we shall illustrate the consequences of not satisfying the passivity constraint. For the system shown in Figure 10.2,

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* Bibliography II, Reference 9.

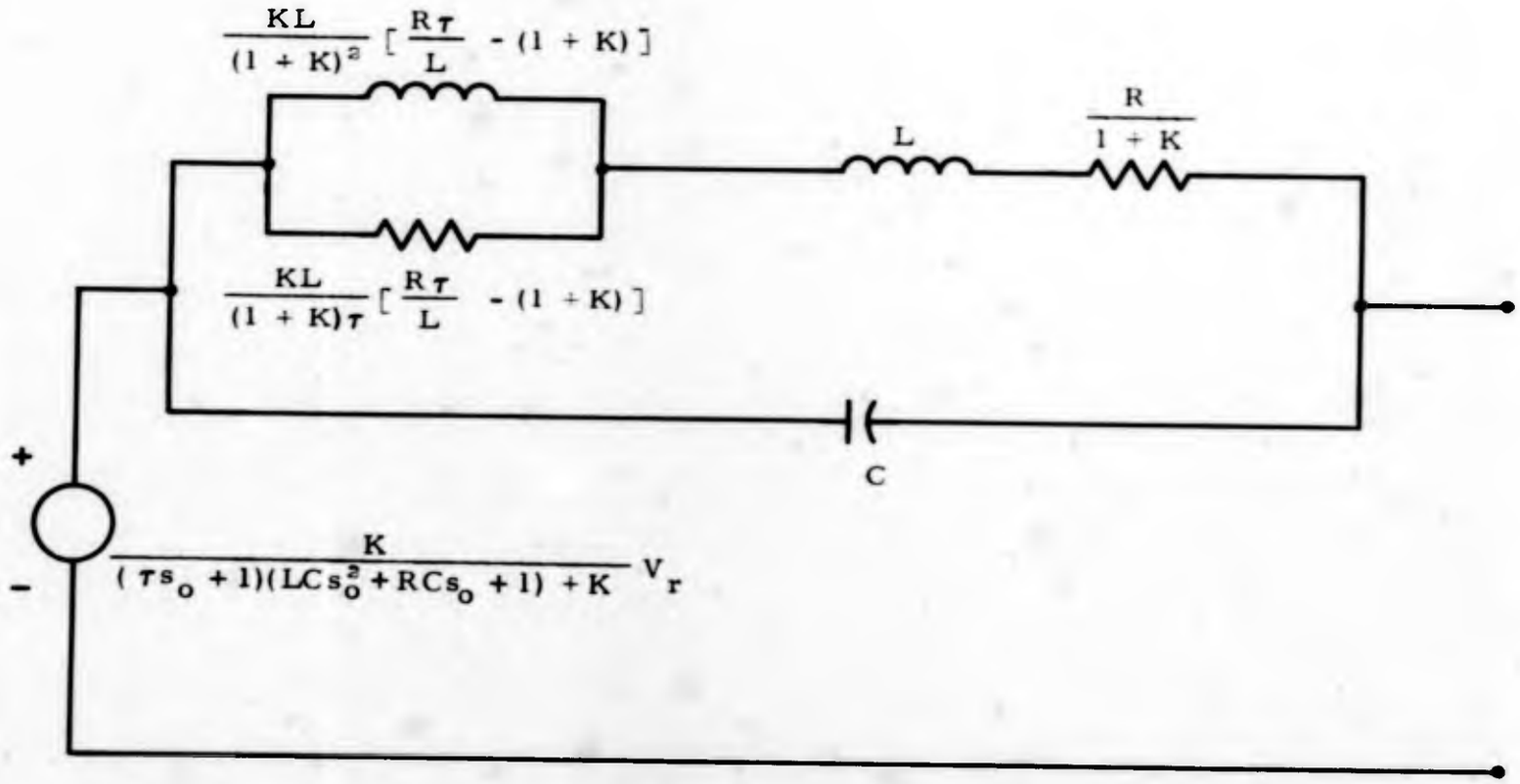

FIGURE 10.7

REALIZATION OF THEVENIN EQUIVALENT WITH ELEMENT VALUES

$$R_1 = \frac{KL}{(1+K)\tau}\left[\frac{R\tau}{L} - (1+K)\right] \qquad L_1 = \frac{KL}{(1+K)^2}\left[\frac{R\tau}{L} - (1+K)\right]$$

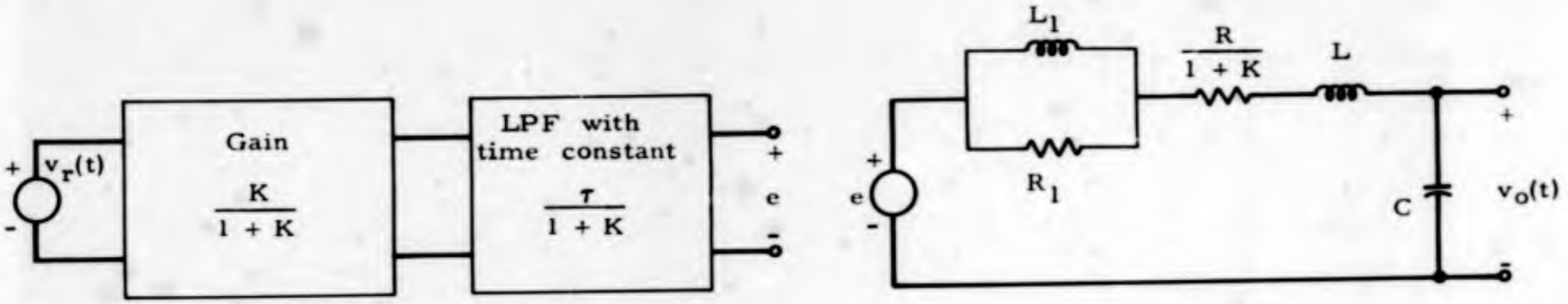

FIGURE 10.8

ANOTHER EQUIVALENT OPEN-LOOP REALIZATION OF THE PWM SYSTEM IN FIGURE 10.2

we can only determine the Thevenin equivalent parameters and not a voltage transfer function, since we do not know a priori what specific load will be connected. If we treat the output impedance $Z_o(s)$ and the equivalent open circuit output voltage V_{oc} as system functions and proceed to use the standard test for stability - no poles in the right half-plane - we find that the amplifier gain K will be upper-bounded by some number $M > \frac{RL}{\tau}$. If we pick K so that

$$\frac{RL}{\tau} < K < M, \tag{10.28}$$

the output impedance will not be passive and the system will be stable when no load is connected or perhaps for a certain, restricted set of loads. However, there will always be a set of passive loads that will cause instability in the system, even though it is stable with no load. Instability with a capacitive load of many otherwise stable amplifiers is a common example of this fact.

Why such a phenomenon exists even though $Z_o(s)$ has no poles in the right half-plane will become apparent if we consider the criterion that $Z_o(s)$ be passive, or positive real. For a value of K chosen to satisfy Eqn. 10.28, $Z_o(s)$ will have no poles in the right half-plane but it will not be passive. For such a case, it is always possible to find a band of frequencies $j\omega$ such that the real part of $Z_o(s)$ will be negative, and we can write $Z_o(s)$ at one such frequency ω_o

$$Z_o(j\omega_o) = -R_o + jX_o,\ R_o > 0, \tag{10.29}$$

where $-R_o$ is the real part of $Z_o(j\omega_o)$ and X_o is the imaginary part of $Z_o(j\omega_o)$, the reactive component. If the load $Z_L(s)$ has an impedance at $s = j\omega_o$ given by

$$Z_L(j\omega_o) = R_o - jX_o,$$

which is realizable by an RL or an RC network, depending on the sign

of X_o, then the transfer function H(s) in Eqn. 10.25 will have a pole at $s = j\omega_o$ and the resulting system will be unstable. This instability is due to the ability of certain passive loads $Z_L(s)$ to "cancel" the negative resistance of $Z_o(s)$ at some frequencies. Clearly, the requirement that $Z_o(s)$ always have a positive real part on the $j\omega$-axis will alleviate this condition.

For purposes of comparison, let us perform a similar analysis on the switching system shown in Figure 10.9. Again, we shall assume that the switching frequency is much higher than the cutoff frequency of the LC filter. In the present example, the output stage constrains the output current instead of the output voltage, i.e., it is a voltage-controlled current source.

If we assume that the ripple current is not observable at the output terminals due to the filtering action of the capacitor C, then we may model the output stage by a linear voltage-controlled current source as shown in Figure 10.10. Now we may apply linear techniques to find the equivalent Thevenin parameters, the equivalent open-circuit voltage V_{oc} and the Thevenin output impedance $Z_o(s)$. For the system in Figure 10.10, these are

$$Z_o(s) = \frac{\tau s + 1}{\tau C s^2 + Cs + Kg}, \tag{10.30}$$

$$V_{oc} = \frac{Kg}{\tau C s_o^2 + C s_o + Kg} V_r, \tag{10.31}$$

where s_o is the complex frequency of the reference $v_r(t)$. At dc ($s = 0$), these become

$$Z_o(0) = \frac{1}{Kg}$$

$$V_{oc} = V_r. \tag{10.32}$$

Note that the inductor L and the resistor R do not appear in any of the

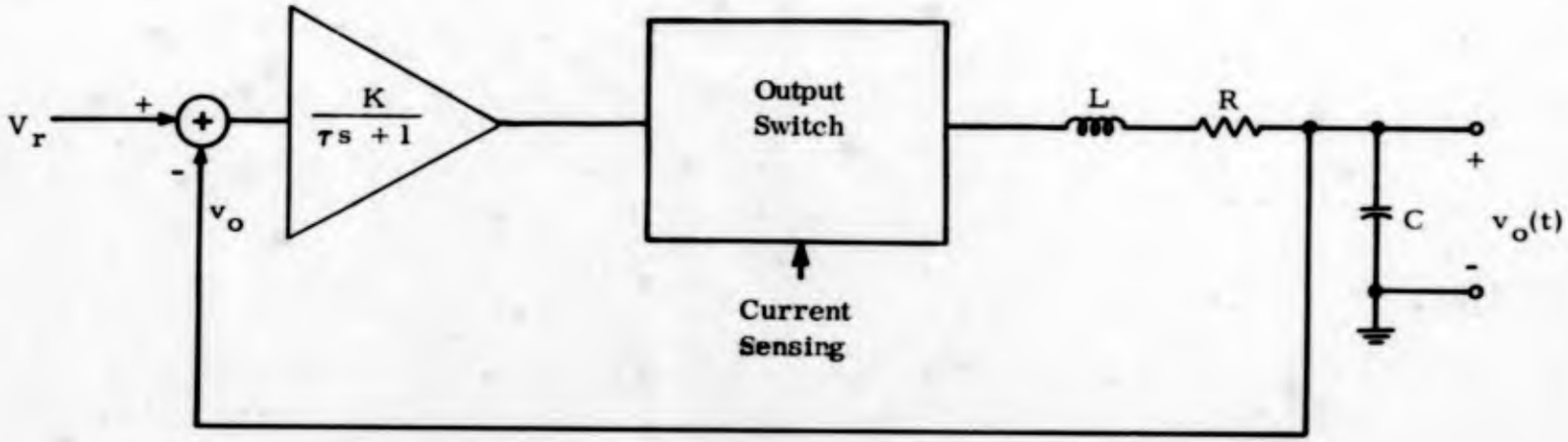

FIGURE 10.9

A CURRENT-CONTROLLED MODULATION SYSTEM

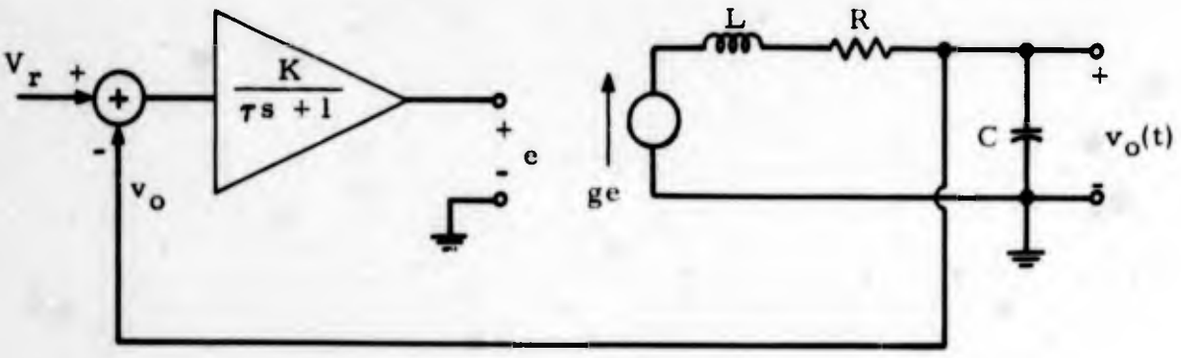

FIGURE 10.10

LINEAR EQUIVALENT OF THE CURRENT-CONTROLLED TWO-STATE MODULATION SYSTEM SHOWN IN FIGURE 10.9

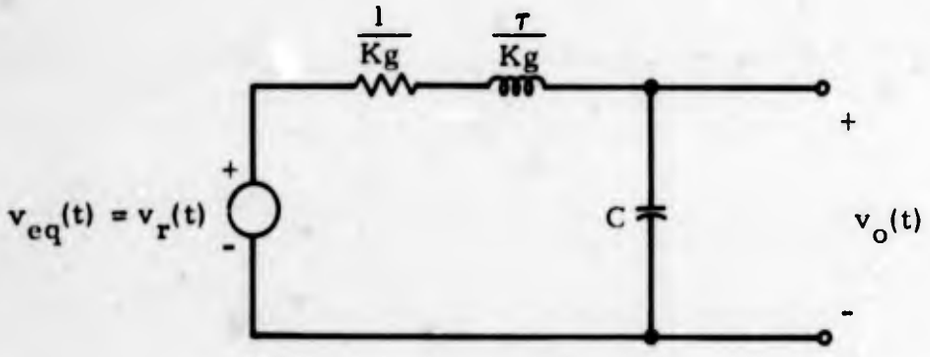

FIGURE 10.11

AN OPEN-LOOP EQUIVALENT MODEL FOR THE SYSTEM OF FIGURE 10.10

expressions in Eqns. 10.30 and 10.31. This is expected since these elements are in series with a current source and hence can be eliminated from the model of Figure 10.10 without affecting the terminal characteristics.

If we apply the test for positive real character to $Z_o(s)$, we find that $Z_o(s)$ is passive if K satisfies

$$Kg > 0. \tag{10.33}$$

Thus, the system loop gain is not limited for this system, and it will be stable with any passive load with an arbitrary gain. We may construct an open-loop model of this system as shown in Figure 10.11 similar to that shown in Figure 10.8. This is not a strict Thevenin equivalent network, but it is in a form which better illustrates the effects of various parameters. The major differences between this model and the model of the PWM shown in Figure 10.8 are:

1) In the present case, the equivalent inductor $\frac{\tau}{Kg}$ is a manifestation of the finite bandwidth of the error amplifier (in fact the only one) and bears no relation to the inductor in the original system, shown in Figure 10.9,

and

2) In the present model, the equivalent source is identical to the reference and is not low-pass filtered.

The purpose of these examples has been to illustrate how various techniques of linear analysis can prove useful in evaluating stability, frequency response, output impedance, regulation and other performance indices of some basically nonlinear systems. The use of the appropriate stability criterion will be dictated by the particular use of the system. Care must be taken when applying a stability test to a system and even more care in interpreting the results, relevance and applicability of such a test.

This type of analysis can yield useful information concerning the baseband stability of certain types of systems if the required

assumptions are satisfied. Assuming the ripple feedback to be negligible is one postulate that is not necessarily satisfied in practice. In such cases, the above analysis is not valid and other techniques must be used. The method presented in the next section may be useful in these situations.

10.3 THE DESCRIBING FUNCTION

In many nonlinear systems, we would like to know if any oscillatory modes can exist. Such oscillations may be damaging to some systems, while others, such as the "bang-bang" controller, depend on a nonlinear oscillation for their operation. For a certain class of nonlinear systems, the amplitude and frequency of oscillation can be determined with the aid of the describing function.

A describing function is a means of representing a nonlinear device in a manner which allows techniques of linear analysis to be used as long as the systems meets certain conditions. The describing function can be defined for systems with memory and discontinuities in their input-output characteristics, which allows this method to be used with some systems not handled by techniques requiring continuous, analytic approximations.

In this section, we shall consider systems with the configuration shown in Figure 10.12. We shall assume that the nonlinear element is frequency independent and symmetric and that the filter $G(j\omega)$ exhibits a magnitude response which decreases with increasing ω.

Let us consider the nonlinear element shown in Figure 10.13 with an input $x(t) = E \cos \omega t$. The output $y(t)$ of the nonlinear element will, in general, be some complex periodic waveform of frequency ω. The describing function for this element is defined as the ratio of the complex amplitude of the fundamental component of the output, as shown in Figure 10.13, to the complex amplitude of the input. We have assumed that the nonlinear characteristic is independent of frequency so that the describing function will be frequency independent. If we denote the describing function of this nonlinear element by $K(E)$, we then have, by reference to Figure 10.13

$$K(E) \triangleq \frac{A(E)}{E} e^{-j\phi(E)} \tag{10.34}$$

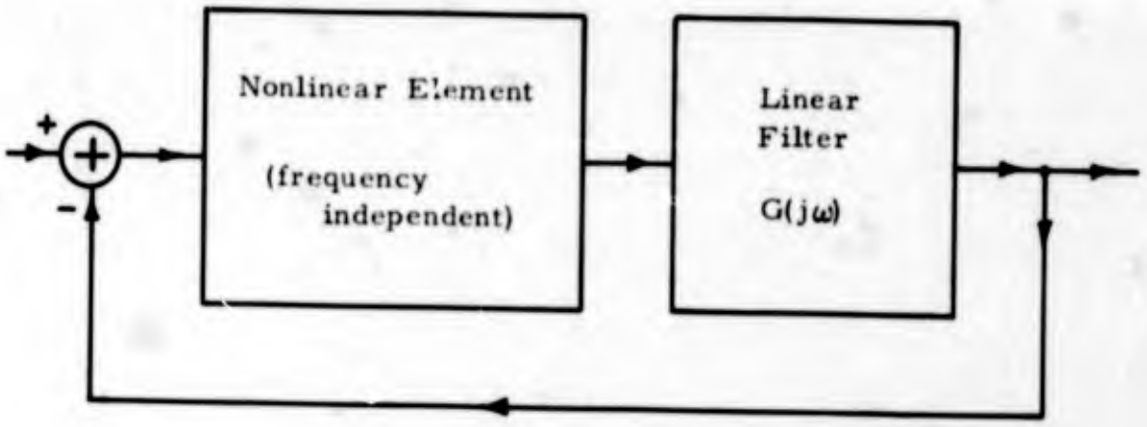

FIGURE 10.12

A TYPE OF NONLINEAR SYSTEM

where ϕ is the phase angle between the input and the fundamental component of the output and where the functional dependence of K, A and ϕ on E is shown to emphasize the fact that these variables are functions of the input amplitude. The describing function is in some sense the gain of the nonlinear element and it is amplitude dependent. The interpretation of the describing function as a gain is illustrated in Figure 10.14. If $G(j\omega)$ has a characteristic which decreases with increasing frequency ω, then we can assume that only the fundamental component of the filter input y(t) will appear at the output since the harmonic components will be attenuated by the filter. Since the linear filter does not respond to the harmonics of y(t), the filter output will be the same for an input $y_1(t)$, the fundamental component of y(t), as it will be for an input y(t). By definition of the describing function, the fundamental component $y_1(t)$ of the output y(t) is given by $y_1(t) = E\,K(E) \cos \omega t$. Therefore, as far as observations made at the output z(t), we may replace the nonlinear element by a linear gain of K(E). The overall system shares with a linear system the property that a sinusoidal input produces a sinusoidal output except the gain of the overall system is now amplitude as well as frequency dependent.

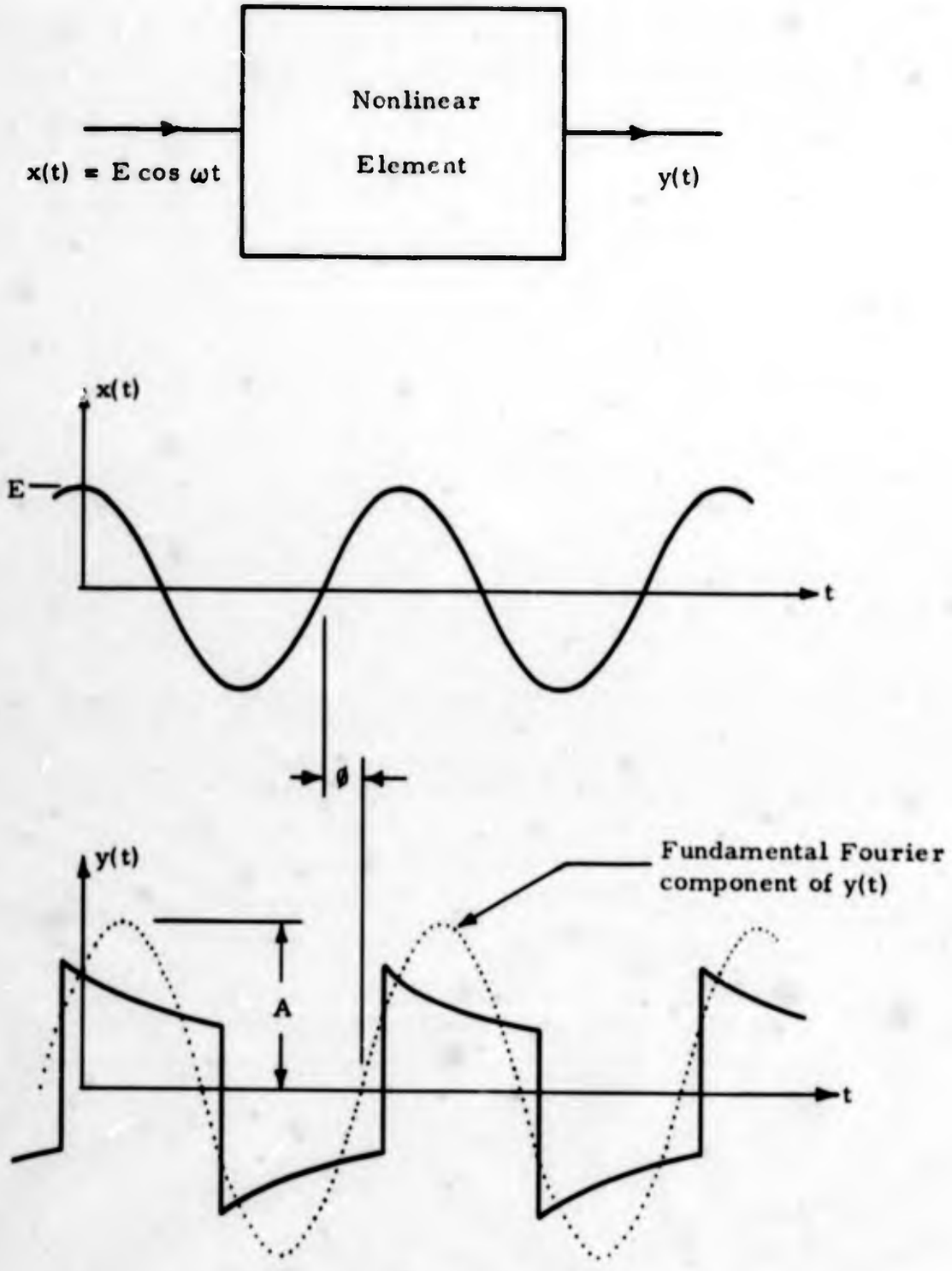

FIGURE 10.13

NONLINEAR ELEMENT USED IN DEFINING THE DESCRIBING FUNCTION

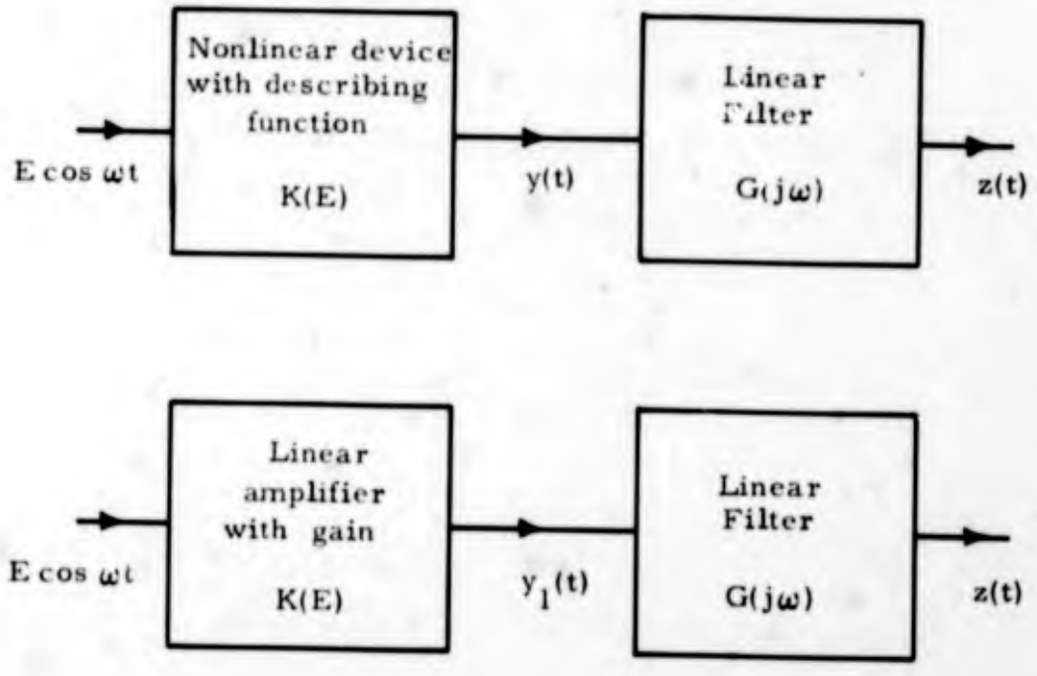

FIGURE 10.14

A NONLINEAR SYSTEM AND A LINEAR EQUIVALENT

If, in Figure 10.14, we close the system by introducing a unity negative feedback loop from the output of the linear filter to the input of the nonlinear element, we obtain the system shown in Figure 10.12 with zero input. Since a sinusoidal input to the nonlinear element produces a sinusoid in the feedback loop, a necessary and sufficient condition for an oscillation to exist is that the loop gain be unity. The amplitude as well as the frequency of an oscillation, if it exists, will be specified due to the amplitude dependence of the nonlinear element. Since the feedback is negative, the constraint on loop gain can be expressed as

$$K(E)G(j\omega) = -1,$$

or

$$-K(E) = \frac{1}{G(j\omega)} \qquad (10.35)$$

where K(E) is the describing function of the nonlinear element. Note that the left side of Eqn. 10.35 is a function of the amplitude of a sinusoid and that the right side is a function of the frequency of a sinusoid. Except for the constraint placed on the amplitude and frequency by Eqn. 10.35, both of these parameters may be chosen independently. This suggests that one method for finding a set of values (E_o, ω_o) which satisfies Eqn. 10.35 is to plot the real and imaginary parts of -K(E) and $\frac{1}{G(j\omega)}$ on the same graph while varying their respective parameters and note if the two resultant loci intersect. The values of E and ω at any such intersection correspond to the amplitude and frequency of a possible mode of oscillation.

Let us use the system illustrated in Figure 10.15 as an example. For this system, the linear filter characteristic is given by

$$G(s) = \frac{1}{LCs^2 + RCs + 1},$$

$$\frac{1}{G(j\omega)} = (1 - LC\omega^2) + jRC\omega. \qquad (10.36)$$

The describing function for the nonlinear element can be found by assuming the input to the element is a sinusoid of amplitude E. By inspection we see that no periodic output is obtained when $E < b$. For $E > b$, the output is a square wave of amplitude M as shown in Figure 10.16. The transitions of the square wave occur when the input crosses the threshold levels $\pm b$. Since the fundamental component of the square wave is in phase with the square wave, we see from Figure 10.16 that the phase lag between the input and the fundamental component of the output is given by the angle required for the input to reach an amplitude b. Thus, we have

$$E \sin \phi = b,$$

or

$$\phi(E) = \sin^{-1} \frac{b}{E}, \qquad E > b. \qquad (10.37)$$

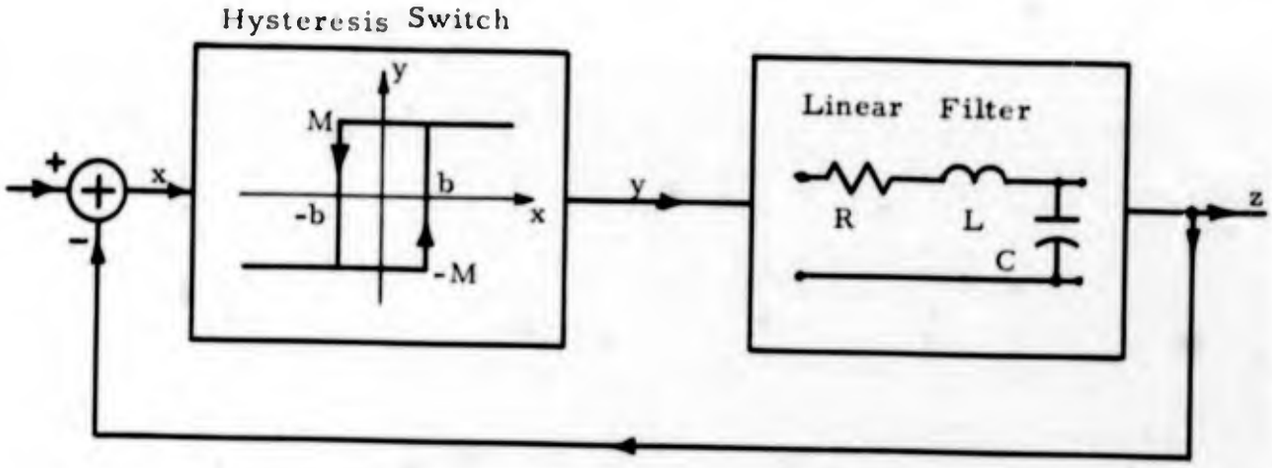

FIGURE 10.15

NONLINEAR SYSTEM TO BE ANALYZED BY THE DESCRIBING FUNCTION

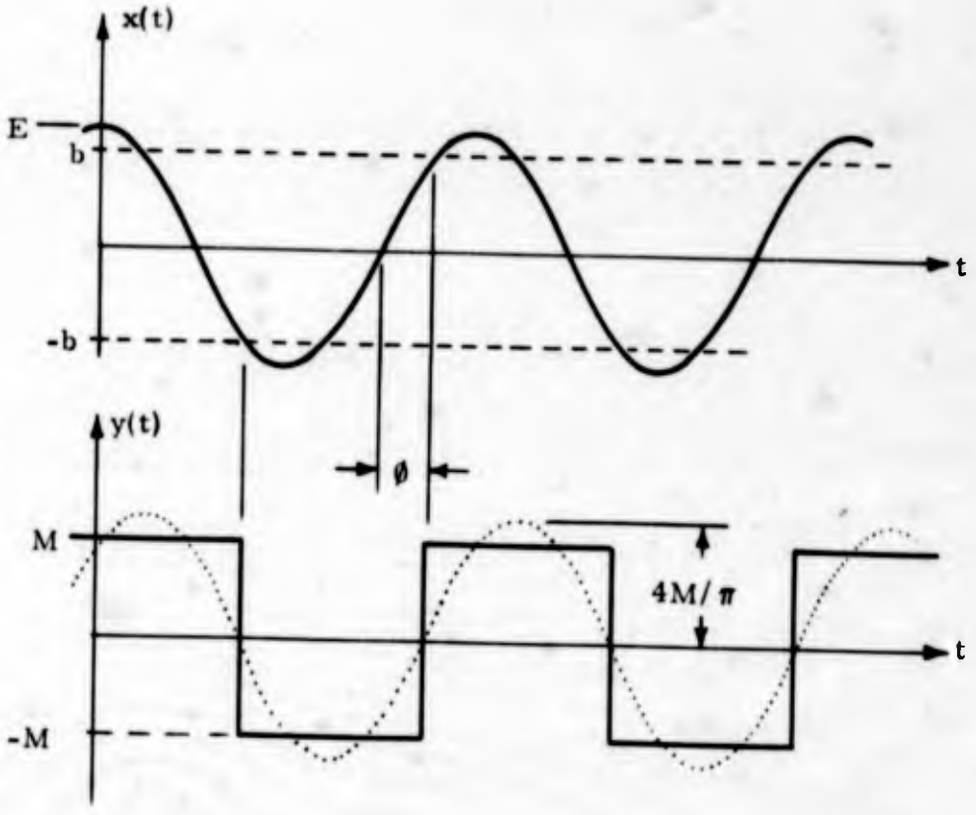

FIGURE 10.16

WAVEFORMS USED TO DETERMINE THE DESCRIBING FUNCTION FOR THE NONLINEAR ELEMENT IN FIGURE 10.15

The amplitude of the fundamental component of a square wave with amplitude M is given by $\frac{4M}{\pi}$. Therefore, we have

$$|K(E)| = \frac{\frac{4M}{\pi}}{E},$$

or

$$|K(E)| = \frac{4M}{\pi E}. \tag{10.38}$$

Combining Eqns. 10.37 and 10.38, remembering that $\phi(E)$ in Eqn. 10.37 is a lag, we have

$$K(E) = \frac{4M}{\pi E} e^{-j \sin^{-1}\left(\frac{b}{E}\right)}, \quad E > b. \tag{10.39}$$

If we write K(E) in terms of its real and imaginary parts, we obtain

$$K(E) = \frac{4M}{\pi E}\sqrt{1 - \frac{b^2}{E^2}} - j\frac{4Mb}{\pi E^2}. \tag{10.40}$$

Either of the expressions in Eqns. 10.39 and 10.40 gives the describing function for the hysteresis switch shown in Figure 10.15.

If solutions for E and ω exist which satisfy Eqn. 10.35, then modes of <u>sinusoidal</u> oscillation can exist in the associated nonlinear system. Since both $-K(E)$ and $\frac{1}{G(j\omega)}$ are complex quantities, we can plot the values of these functions on the complex plane as their respective parameters are varied over their allowed ranges. In Figure 10.17, this has been done for the K(E) given by Eqn. 10.40 and for $G(j\omega)$ given by Eqn. 10.36. The locus of $-K(E)$ is a semicircle with center $j\frac{2M}{\pi b}$ and radius $\frac{2M}{\pi b}$. The locus of $\frac{1}{G(j\omega)}$ is a parabola with a vertex at 1 and an imaginary axis intercept at the point $jR\sqrt{\frac{C}{L}}$. By

inspection, we see that there is at most one point of intersection A and that this intersection exists only if

$$\frac{4M}{\pi b} \geq R \sqrt{\frac{C}{L}}$$

or

$$b \leq \frac{4M}{\pi R} \sqrt{\frac{L}{C}}. \tag{10.41}$$

If we note that the Q of the linear filter is given by

$$Q = \frac{\sqrt{\frac{1}{LC}}}{\frac{R}{L}} = \frac{\sqrt{\frac{L}{C}}}{R},$$

we may put Eqn. 10.41 into the interesting form

$$b \leq \frac{4}{\pi} MQ \tag{10.42}$$

which shows that a sinusoidal oscillation can exist with the hysteresis width b larger than the hysteresis output height M if the Q of the linear filter is large enough.

We may determine a number of properties of this system by inspecting the plot in Figure 10.17. First, we see that ω_o, the frequency corresponding to the point A, must be greater than $\frac{1}{\sqrt{LC}}$, the resonant frequency of the filter. Second, as the Q of the linear filter is increased, the intercept $R \sqrt{\frac{C}{L}} \left(= \frac{1}{Q}\right)$ becomes smaller and the parabolic arc of $\frac{1}{G(j\omega)}$ compresses toward the real axis. This lowers the point of intersection A, which corresponds to an increase in the amplitude of the oscillation.

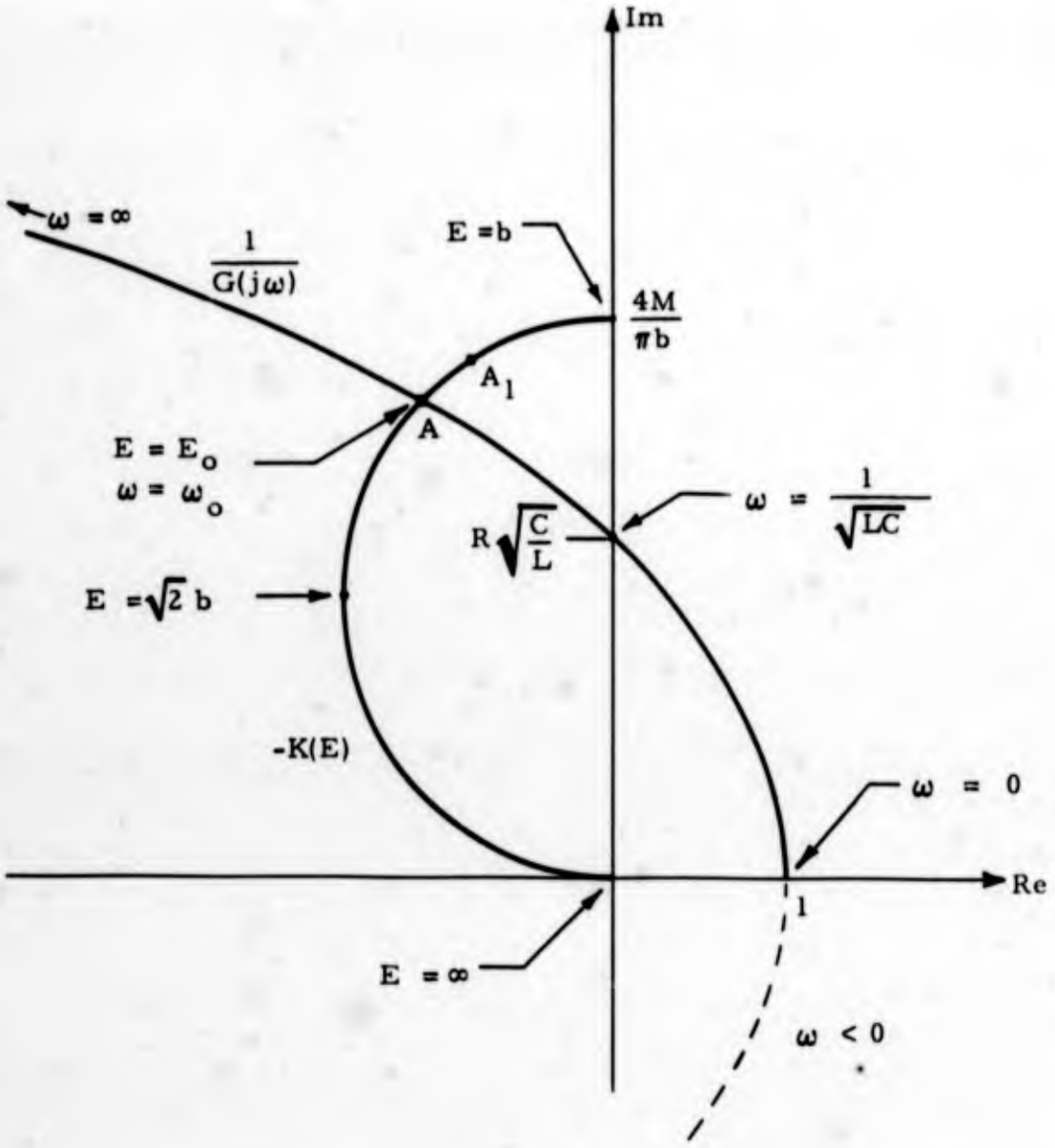

FIGURE 10.17

PLOT TO DETERMINE POSSIBLE MODES OF OSCILLATION FOR THE NONLINEAR SYSTEM DEPICTED IN FIGURE 10.15

Some information concerning the relative stability of a mode of oscillation can also be obtained from such a plot. For this plot, let us assume that the oscillation has a reduced amplitude E_1 corresponding to the point A_1. Since this point on the -K(E) locus is farther from the origin than the point A, the magnitude of $K(E_1)$ is greater than the magnitude of $K(E_o)$, corresponding to the point A. Thus, the gain of the system is increased and the amplitude of the oscillation will tend to increase, moving the operating point toward the equilibrium point A. Similarly, an increase in the amplitude of oscillation past E_o causes a gain of the system and the operating point again will move toward point A. Such an observation will tell only if the indicated mode of oscillation is potentially stable. We may expect this mode to be unstable if the operating point moves away from the equilibrium point if it is displaced. However, if the operating point tends to return to the equilibrium point, we cannot tell if it will finally settle at the equilibrium point or if it will itself oscillate about the equilibrium point without settling - a mode called a hunting mode.

When used on certain types of systems, the describing function method will not necessarily yield any useful information although the necessary approximations may be valid. As an example, if applied to a pulse-width modulation system, the describing function may tell us that the system is indeed oscillating at the switching frequency, a rather unenlightening fact.

The describing function as presented here is also limited by the fact that only modes of oscillation in which the output of the linear filter is sinusoidal can be detected. In fact, the system of Figure 10.15 will always oscillate if $b < M$, even though the bound in Eqn. 10.41 is violated. This latter bound only tells us that a sinusoidal oscillation will not occur if the bound is not satisfied. The failure of this technique is due to the fact that the assumptions made about the frequency behavior of the filter are no longer valid when the bound of Eqn. 10.41 is not satisfied, so that any predictions made with this assumption will not necessarily be valid. Some work has been done to allow for the presence of various harmonics in the feedback signal* since these are not completely eliminated by the linear

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* Bibliography II, Reference 7.

filter, but such techniques only increase the accuracy of the basic method and are still subject to the same general assumptions originally made.

10.4 ASSUMED STATE ANALYSIS

Systems which contain components or blocks with nonlinear characteristics or memory can often be analyzed more easily by the method of assumed states than by an analysis involving a complete description of all nonlinearities. Basically, this technique consists of postulating states for one or more elements (for example, assuming a given diode to be conducting and a certain magnetic core to be saturated in a given direction) and performing an analysis based on these assumptions. The assumptions will have been correctly chosen only if a solution exists consistent with the assumptions and the network laws.

Assumed state analysis is perhaps most useful with systems containing devices with a number of distinct, well-defined modes of operation. A few simple examples will illustrate the application of this technique.

Let us consider the network in Figure 10.18. The diodes D1 and D2 are ideal with v-i characteristic

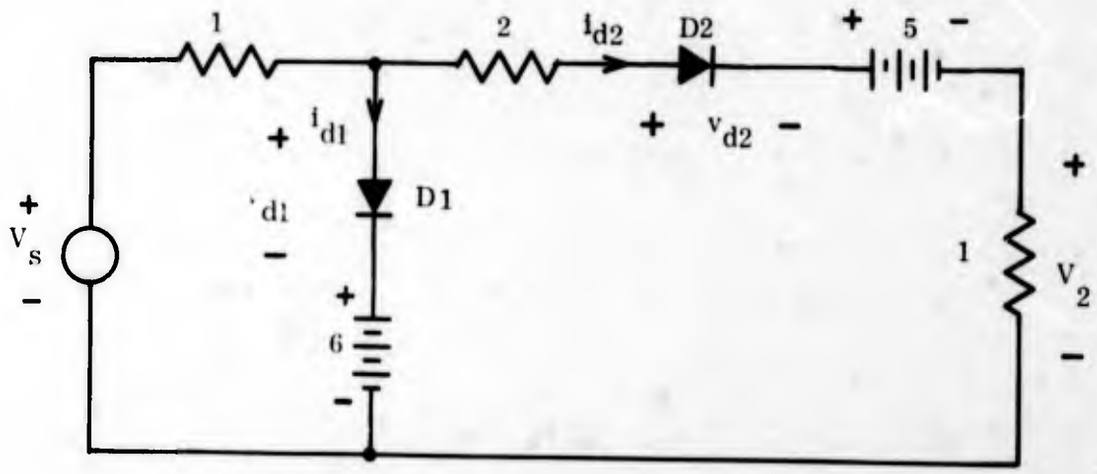
$$v_d = 0, \text{ when } i_d \geq 0$$

$$i_d = 0, \text{ when } v_d \leq 0, \tag{10.43}$$

and we wish to determine the voltage v as a function of the source voltage v_s. We shall initially assume that both diodes are open so that the network appears as shown in Figure 10.19a. For this network, we see by inspection that $v = 0$. However, this is true only if both diodes are actually open. When this is indeed the case, we must have

$$v_{d1} = v_s - 6 < 0,$$

$$v_{d2} = v_s - 5 < 0.$$



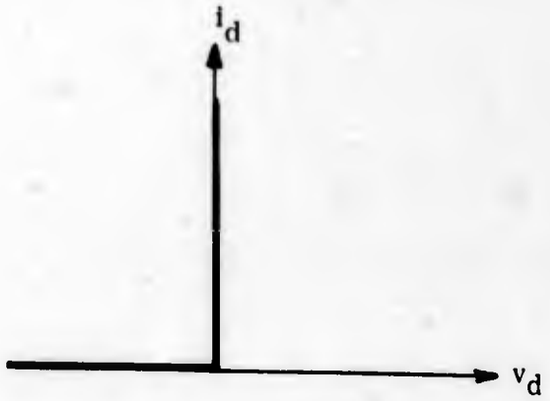


FIGURE 10.18

NONLINEAR NETWORK

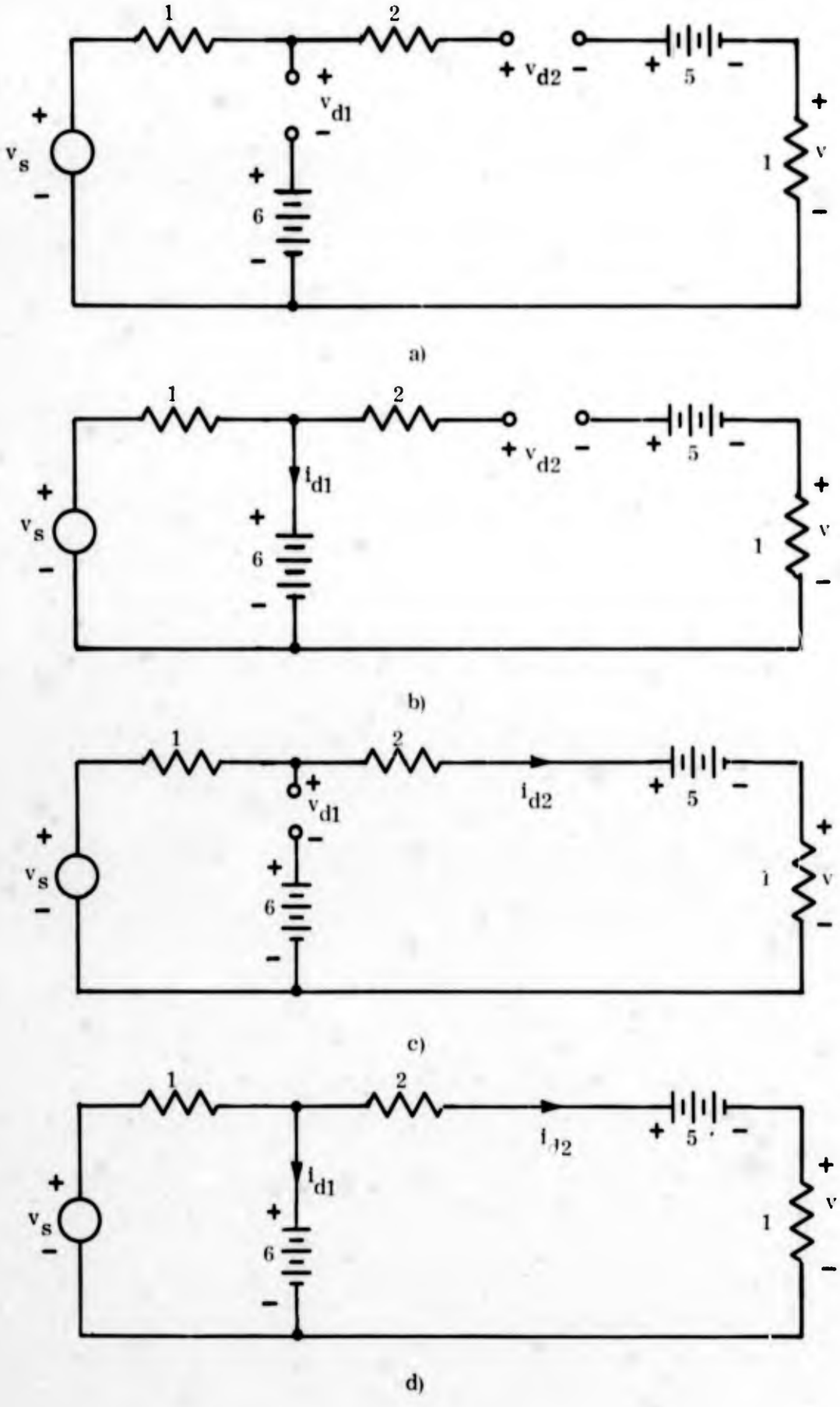


FIG. 10.19 NONLINEAR NETWORK WITH ASSUMED DIODE STATES

Both of these will be satisfied when $v_s < 5$, so that we may write

$$v = 0, \qquad v_s < 5. \tag{10.44}$$

Now let us assume that D1 is closed and D2 is open, so that the original network takes the form shown in Figure 10.19b. In this case, we again have $v = 0$. If the diodes are to be in this state, then we must have

$$i_{d1} = v_s - 6 > 0,$$

$$v_{d2} = 1 < 0.$$

Since the latter condition is obviously false, we must conclude that the state [D1 closed, D2 open] cannot occur in this network, regardless of the value of v_s.

Continuing in this manner with the remaining two states, we find that

$$\left.\begin{array}{l} v = \frac{1}{4}(v_s - 5), \\ \\ \text{D1 open, D2 closed} \end{array}\right\} \quad \text{when } 5 < v < 6\tfrac{1}{3}$$

$$\left.\begin{array}{l} v = \frac{1}{3}, \\ \\ \text{D1 closed, D2 closed} \end{array}\right\} \quad \text{when } v_s > 6\tfrac{1}{3} \tag{10.45}$$

Together, Eqns. 10.44 and 10.45 describe the transfer characteristic of the network in Figure 10.18. This transfer characteristic is plotted in Figure 10.20.

The technique of assuming a state can be quite useful in situations other than the piecewise-linear example just completed. Steady-state time domain analyses may be aided in many cases by such an

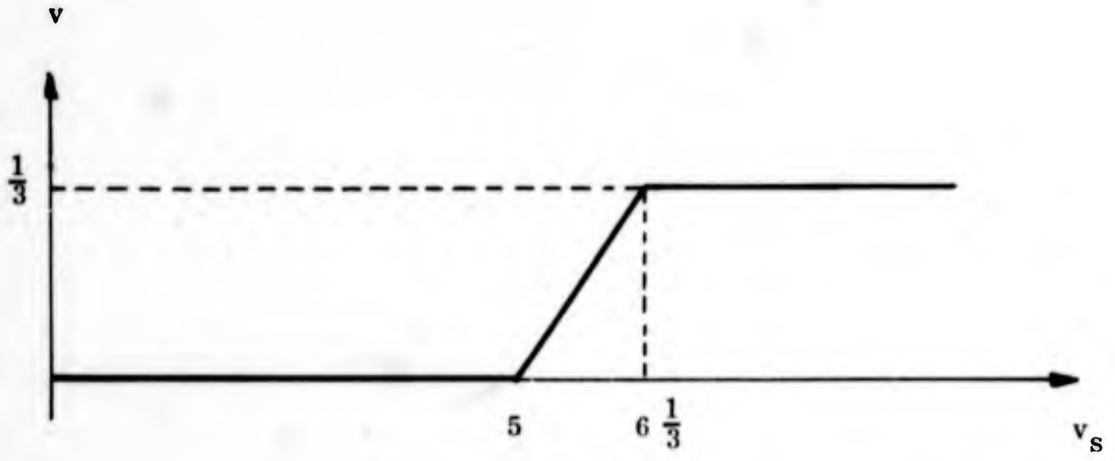


FIGURE 10.20

TRANSFER CHARACTERISTIC OF NONLINEAR NETWORK

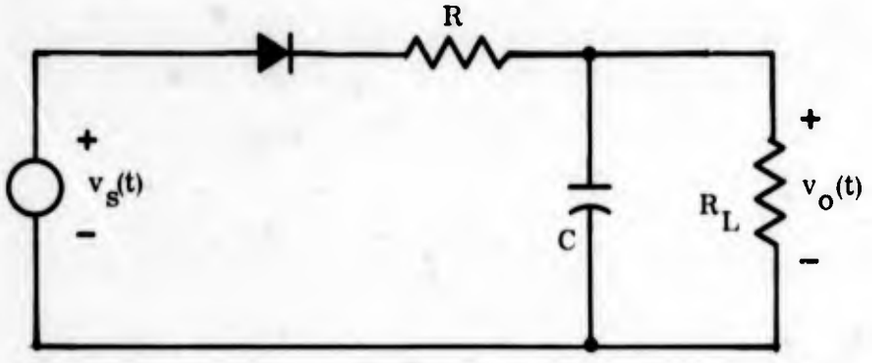


FIGURE 10.21

HALF-WAVE RECTIFIER

approach. Here, the procedure is to assume an initial value for the desired output and compute the resulting value of this output one cycle later. If a steady-state situation exists, then these two values must be equal, and the steady-state results may be obtained from the constraint placed on the initial value by this equality. The basics of this technique should be made clear by the following example.

We shall consider the half-wave rectifier circuit shown in Figure 10.21, where $v_s(t)$ is a symmetric square wave source with peak amplitude V_s and period T followed by an RC filter and a resistive load R_L. We wish to determine the peak-to-peak ripple component of $v_o(t)$. In Figure 10.22, the time origin has been chosen to coincide with the positive transition of $v_s(t)$. At this time, we shall assume that $v_o(t) = v_1 < \frac{R_L V_s}{R + R_L}$. For this case, the diode will be closed and $v_o(t)$ will charge toward $\frac{R_L V_s}{R + R_L}$ with a time constant $\tau_1 = (R \,||\, R_L)\, C = \frac{R R_L C}{R + R_L}$ as long as $v_s(t) = V_s$. Thus, for $0 < t < \frac{T}{2}$, we have

$$v_o(t) = \frac{R_L V_s}{R + R_L} - \left(\frac{R_L V_s}{R + R_L} - v_1\right) e^{-\frac{t}{\tau_1}}, \qquad 0 < t < \frac{T}{2} \tag{10.46}$$

The voltage v_2 is found from Eqn. 10.46 by setting $t = \frac{T}{2}$. Thus,

$$v_2 = \frac{R_L V_s}{R + R_L} - \left(\frac{R_L V_s}{R + R_L} - v_1\right) e^{-\frac{T}{2\tau_1}}. \tag{10.47}$$

At $t = \frac{T}{2}$, $v_s(t)$ goes negative, shutting off the diode. The capacitor C can then discharge only through the load R_L. With the value v_2 at

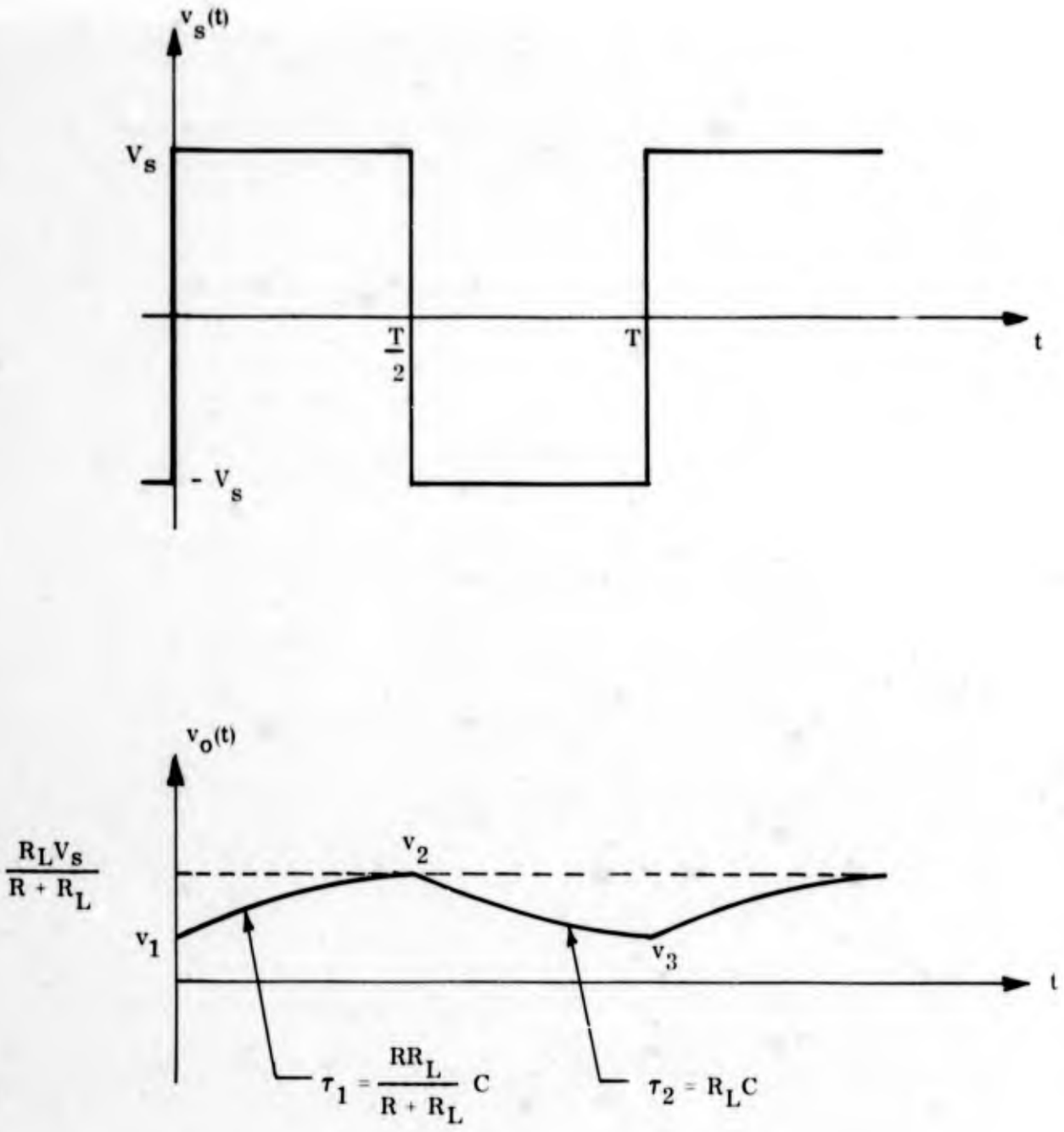


FIGURE 10.22

WAVEFORMS IN HALF-WAVE RECTIFIER

$t = \frac{T}{2}$ and a time constant $\tau_2 = R_L C$ for $\frac{T}{2} < t < T$, we have

$$v_3 = v_2 e^{-\frac{T}{2\tau_2}} \tag{10.48}$$

where v_3 is the value of $v_o(t)$ at $t = T$. If the circuit has reached steady-state conditions, then we must have $v_3 = v_1$. This together with Eqns. 10.47 and 10.48 enable us to find v_1, which is given by

$$v_1 = \frac{R_L V_s}{R + R_L} \cdot \frac{\exp\left(\frac{T}{2\tau_1}\right) - 1}{\exp\left(\frac{T}{2\tau_1} + \frac{T}{2\tau_2}\right) - 1} . \tag{10.49}$$

Using Eqns. 10.47 and 10.49 we may then determine the peak-to-peak ripple voltage $\Delta v = v_2 - v_1$. After some algebraic simplification, this becomes

$$\Delta v = \frac{R_L V_s}{R + R_L} \cdot \frac{\left[\exp\left(\frac{T}{2\tau_1}\right) - 1\right] \left[\exp\left(\frac{T}{2\tau_2}\right) - 1\right]}{\exp\left(\frac{T}{2\tau_1} + \frac{T}{2\tau_2}\right) - 1} . \tag{10.50}$$

The result given by Eqn. 10.50 is an exact expression for any T and any τ_1 and τ_2. If $\tau_1 \gg T$ and $\tau_2 \gg T$, the ripple will be small and the exponentials in Eqn. 10.50 can be approximated by first order expansions. For this case, the ripple Δv is given approximately by

$$\Delta v \simeq \frac{T}{2\left(R_L + 2R\right) C} V \tag{10.51}$$

where the expressions for τ_1 and τ_2 in terms of R, R_L and C have been included in the result.

The use of assumed state analysis in more complex situations is illustrated in the analysis of the magnetic circuits in Chapter 12. For these cases, both the piecewise-linear and time domain methods prove relevant.

10.5 STATE VARIABLES*

The importance of the state concept has grown in recent years due to the steadily increasing complexity of the systems to be designed and analyzed. State representation of systems offers a number of advantages over transfer function methods, two important ones being the ease with which the representation may be simulated on a computer and an inherent description of all the dynamics, both terminal and internal, of a system.

Let us consider a single input - single output linear system with a known structure. In order to determine the output $y(t)$ for $t_o < t < t_1$, we must know the input $v(t)$ for $-\infty < t < t_1$ or we must know $v(t)$ for $t_o < t < t_1$ and sufficient "initial" conditions at $t = t_o$. These conditions may be the inductor currents and capacitor voltages (for an electrical network) or the value of a specific variable and its derivatives at $t = t_o$. In either case, we need to know a certain amount of information about the network at $t = t_o$ in order to determine the output $y(t)$ with the input $v(t)$ specified only for $t > t_o$. The information required pertains to the state of the system at $t = t_o$, and it lumps the effects of the past history of the system into a specific set of values at $t = t_o$.

In talking about multiple input-output systems, we shall use matrix notation for simplicity. Matrices will be denoted by underlined upper case letters in general, e.g., $\underline{A}$. The special case of column vectors (n x 1 matrices) will be denoted by underlined lower case letters, e.g., $\underline{x}$. For a multiple input system with inputs

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* Bibliography II, References 5 and 6.

$v_1, v_2, \ldots v_m$, we shall define the input vector $\underline{v}$ by

$$\underline{v} \triangleq \begin{bmatrix} v_1 \\ v_2 \\ \cdot \\ \cdot \\ \cdot \\ v_m \end{bmatrix} \tag{10.52}$$

with other multivalued functions such as the outputs of the system or the state similarly defined.

We shall not discuss the techniques of matrix algebra here, since these are perhaps best learned from the references.* We shall assume a basic knowledge of matrix algebra so that we may center our discussion on the interpretation of results rather than manipulation.

The concept of state is quite fundamental and difficult to define. However, we may express in a slightly more formal manner than above the properties of a state defined system. Let $\underline{x}(t)$ denote the state of the system. Then the system has the following characteristics:

1) Given $\underline{x}(t_o)$ and the input $\underline{v}(t_o, t)$ which denotes the input over the interval t_o to t, the state $\underline{x}(t)$ for $t > t_o$ is uniquely determined.

2) Given $\underline{x}(t_o)$ and the input $\underline{v}(t_o, t)$, the output $\underline{y}(t)$ for $t > t_o$ is uniquely determined.

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* Bibliography II, Reference 5.

We may express these algebraically as

$$\underline{x}(t) = f[\underline{x}(t_o),\ \underline{v}(t_o,\ t)].$$

$$\underline{y}(t) = g[\underline{x}(t_o),\ \underline{v}(t_o,\ t)]. \qquad (10.53)$$

If the system is linear, in most cases these can be written in the form

$$\dot{\underline{x}}(t) = \underline{A}(t)\underline{x}(t) + \underline{B}(t)\underline{v}(t)$$

$$\underline{y}(t) = \underline{C}(t)\underline{x}(t) + \underline{D}(t)\underline{v}(t) \qquad (10.54)$$

where the dot denotes a time derivative.

Note that the state vector $\underline{x}(t)$ contains all the information about the system necessary to determine the future response given the input vector $\underline{v}(t)$. We may think of the system as being described by a point in state space - a space spanned by $\underline{x}(t)$ with one dimension for each component of $\underline{x}(t)$ - which starts at a point $\underline{x}(t_o)$ and is moved along a unique trajectory by an input $\underline{v}(t_o,\ t)$ to a point $\underline{x}(t)$. The time progress of this trajectory together with the input $\underline{v}(t_o,\ t)$ completely describes all aspects of the system.

In general, there is no unique choice for a set of state variables. The set chosen may be influenced by the ease of visualization or by computational ease. Let us illustrate the point by considering the network in Figure 10.23, which is a two input - one output system, the output y(t) being the capacitor current $i_c(t)$. If we choose the state vector components to be $x_1 = v_c(t)$, $x_2 = i_L(t)$, then we may write the following equations describing the system:

$$\dot{x}_1 = -5x_1 - 2x_2 + 2e + 2i$$

$$\dot{x}_2 = 3x_1$$

$$i_c = -\frac{5}{2}x_1 - x_2 + e + i. \qquad (10.55)$$

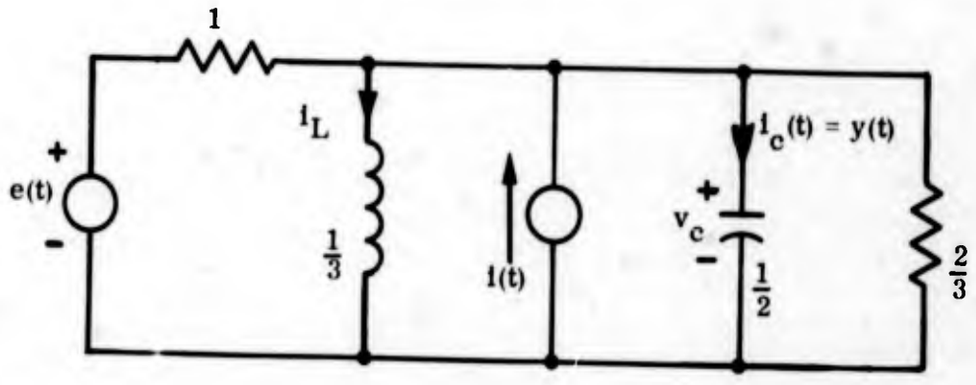

FIGURE 10.23

LINEAR NETWORK

In the matrix form of Eqn. 10.54, these are

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -5 & -2 \\ 3 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 2 & 2 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} e \\ i \end{bmatrix}$$

$$\begin{bmatrix} i_c \end{bmatrix} = \begin{bmatrix} -\frac{5}{2} & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} e \\ i \end{bmatrix} . \qquad (10.56)$$

Here it is worth pointing out that we cannot write the output equation as

$$i_c = c\dot{x}_1 = c\dot{v}_c$$

since this does <u>not</u> have the properties we desire in a state representation, i.e., the present values of the state and the input vectors will not give the present value of the output from this equation.

We shall not delve into the procedures used to solve the matrix equations in Eqn. 10.56 here. The necessary tools may be found in the references. Instead, we shall point out some of the more general characteristics of state representation.

First, let us take the system in Figure 10.23 and define a new state vector $\underline{q}$ by

$$\begin{bmatrix} q_1 \\ q_2 \end{bmatrix} = \begin{bmatrix} 3 & 2 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} . \qquad (10.57)$$

Now in terms of this new state vector $\underline{q}$, we may write the state equations of this system as

$$\begin{bmatrix} \dot{q}_1 \\ \dot{q}_2 \end{bmatrix} = \begin{bmatrix} -3 & 0 \\ 0 & -2 \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} + \begin{bmatrix} 6 & 6 \\ 2 & 2 \end{bmatrix} \begin{bmatrix} e \\ i \end{bmatrix}$$

$$\begin{bmatrix} i_c \end{bmatrix} = \begin{bmatrix} -\frac{3}{2} & 2 \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} + \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} e \\ i \end{bmatrix} \qquad (10.58)$$

Thus, we see that there is no unique state representation and that the choice of one may be influenced by many considerations. For the first state vector $\underline{x}$ chosen in Eqn. 10.56, the components of the state vector represent the inductor current and the capacitor voltage. This choice is a good one for an intuitive grasp of the state concept.

For the state vector $\underline{q}$ defined by Eqn. 10.57, there is no simple physical significance to the components of this vector. However, the use of this state vector leads to some desirable mathematical properties. In Eqn. 10.58, we see that the $\underline{A}$ matrix of Eqn. 10.54 has nonzero terms only on its main diagonal. If Eqn. 10.58 were expanded in scalar form, we would obtain an uncoupled pair of first order equations. Each component of $\underline{q}$ can, therefore, be determined from the input vector and the initial value of that component only and is unaffected by the behavior of the remaining components of $\underline{q}$. This kind of system is intuitively pleasing in a mathematical sense and often leads to computational ease. Furthermore, when the $\underline{A}$ matrix is in diagonal form, the elements on the diagonal are the natural frequencies of the system, a fact which may be quite useful.

The linear transformation in Eqn. 10.57, which defines $\underline{q}$, was selected to provide a diagonalized $\underline{A}$ matrix. There are well-defined techniques which allow us to determine the appropriate transformation. These will be found in a study of matrix algebra and will not be presented here.

The matrix $\underline{A}$ contains enough information to completely describe the natural behavior of a system. In fact, if we set the inputs to zero, we obtain the homogeneous state equation

$$\dot{\underline{x}} = \underline{A}\underline{x} \tag{10.59}$$

Not too surprisingly, we may express the solution to this equation in matrix form as

$$\underline{x}(t) = e^{\underline{A}t} \cdot \underline{x}(0). \tag{10.60}$$

One point we should note is that the exponential term, which is a square matrix of the same order as $\underline{A}$, must premultiply the initial state $\underline{x}(0)$. This is true since matrix multiplication is not commutative.

If the matrix $\underline{A}$ is in the diagonal form

$$\underline{A} = \begin{bmatrix} \lambda_1 & 0 & \cdots & \\ 0 & \lambda_2 & \cdots & \\ & \cdot & & \\ & & \cdot & \\ & & & \lambda_n \end{bmatrix} \tag{10.61}$$

then the exponential term in Eqn. 10.60 is given by

$$e^{\underline{A}t} = \begin{bmatrix} e^{\lambda_1 t} & 0 & & \\ 0 & e^{\lambda_2 t} & & \\ & \cdot & & \\ & & \cdot & \\ & & & e^{\lambda_n t} \end{bmatrix} \tag{10.62}$$

If the system is stable $\underline{x}(t)$ will approach $\underline{0}$ as $t \longrightarrow \infty$. Thus, the system will be stable if the real parts of all λ_k are negative, which amounts to the requirement that there be no right half-plane poles.

Two other important concepts become readily apparent in a state variable formulation - controllability and observability. A system is said to be controllable if every state variable is coupled to the input and observable if every state variable is coupled to the output. An uncontrollable system will have natural modes which cannot be excited or affected by an input while an unobservable system may have natural modes which are not measurable at the outputs of the system. Clearly, neither of these properties are desirable in a system.

These properties relate to one weakness in a transfer function description of a system. The transfer functions describe only the controllable and observable parts of a system. Thus, any mode of the system which is uncoupled to either the input or the output will not appear in a transfer function description of the system. In complex systems, this phenomenon may lead to incorrect conclusions about operation and stability.

The criteria for controllability and observability can be expressed, in general, for a state described system defined by Eqn. 10.54. We shall give the necessary conditions for the case where the $\underline{A}$ matrix is diagonal and the state variables are uncoupled, since the conditions are more simply stated and offer better insight into the definitions.

If $\underline{A}$ is diagonal and we then write the scalar equations for Eqn. 10.54, we desire at least one nonzero input term in each state variable equation if the system is to be controllable. In terms of the matrix $\underline{B}$, this places the constraint that $\underline{B}$ have no all zero rows.

Similarly, if the system is to be observable, then we require that every state variable appear in at least one output equation. In terms of the coefficient matrices of Eqn. 10.54, this requires that the matrix $\underline{C}$ have no all zero columns.

We see that the system shown in Figure 10.23 and described by the state formulation in Eqn. 10.58 is both controllable and observable. This follows since $\underline{B}$ in Eqn. 10.58 has no zero rows and $\underline{C}$ in Eqn. 10.58 has no zero columns.

As an example, we shall determine the response $i_c(t)$ in Figure

10.23 to a unit step in i(t) with zero initial conditions using the state formulation of Eqn. 10.58. The two scalar state equations for e(t) = 0, i(t) = $u_{-1}(t)$ (the unit step) are

$$\frac{dq_1}{dt} = -3q_1 + 6u_{-1}(t)$$

$$\frac{dq_2}{dt} = -2q_2 + 2u_{-1}(t). \qquad (10.63)$$

If the initial conditions are zero, the solutions to Eqn. 10.63 are easily found by inspection to be

$$q_1(t) = 2 - 2e^{-3t}, \qquad t > 0$$

$$q_2(t) = 1 - e^{-2t}, \qquad t > 0. \qquad (10.64)$$

From Eqn. 10.58, the output $i_c(t)$ is given by

$$i_c(t) = -\frac{3}{2} q_1(t) + 2q_2(t) + i(t) = 3e^{-3t} - 2e^{-2t}, \qquad t > 0 \qquad (10.65)$$

We may obtain the capacitor voltage and inductor current quite easily since these quantities are the state variables in our original formulation. Using Eqn. 10.64 and the inverse transformation of Eqn. 10.57, we obtain

$$v_c(t) = x_1(t) = 2(e^{-2t} - e^{-3t}), \qquad t > 0,$$

$$i_L(t) = x_2(t) = 1 + 2e^{-3t} - 3e^{-2t}, \qquad t > 0. \qquad (10.66)$$

The results given in Eqns. 10.65 and 10.66 are plotted in Figure 10.24. The trajectory of the state vector $\underline{q}$ for this input is shown in Figure

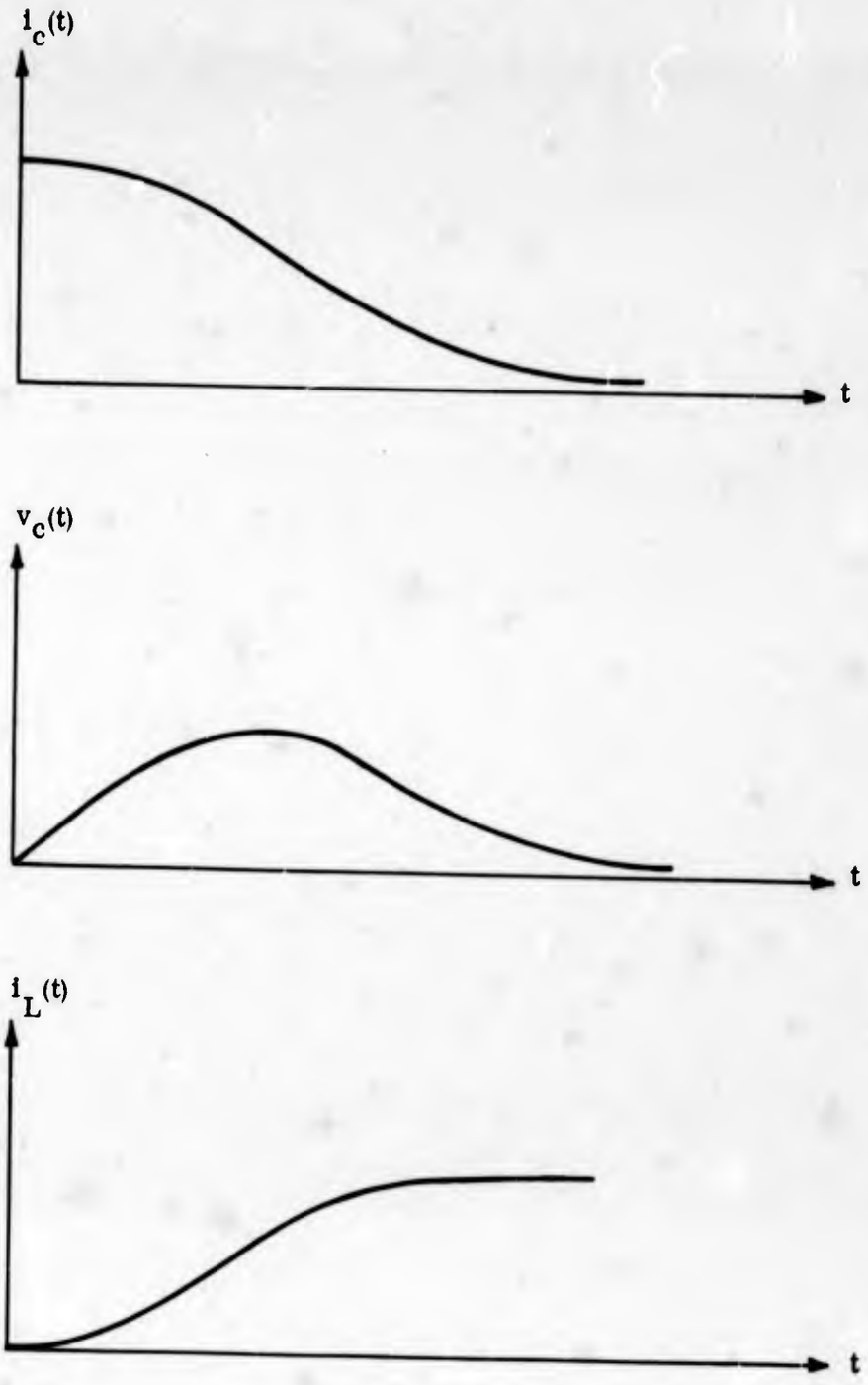

FIGURE 10.24

WAVEFORMS IN NETWORK OF FIGURE 10.23

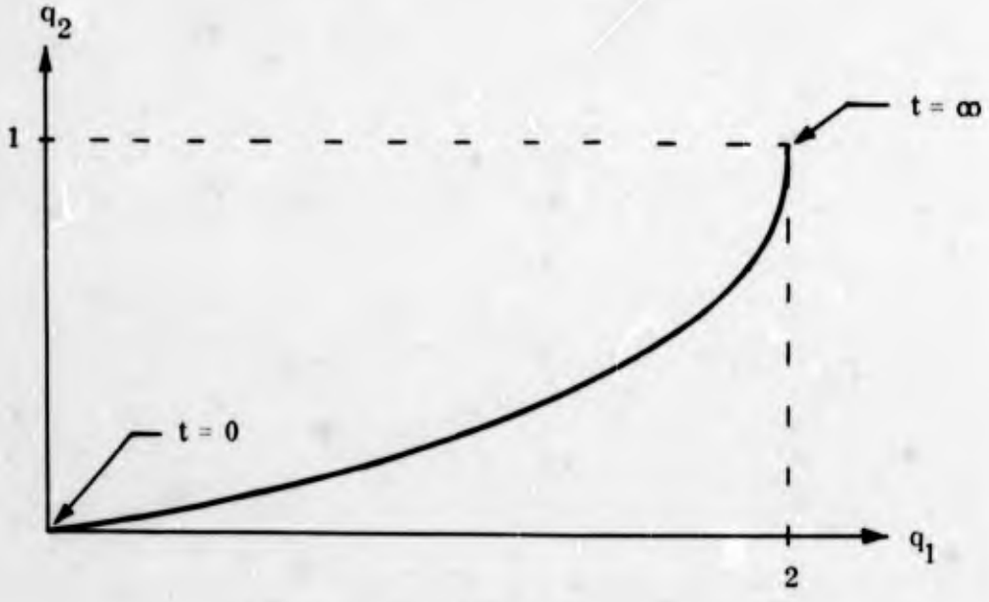

FIGURE 10. 25

LOCUS OF NETWORK STATE q

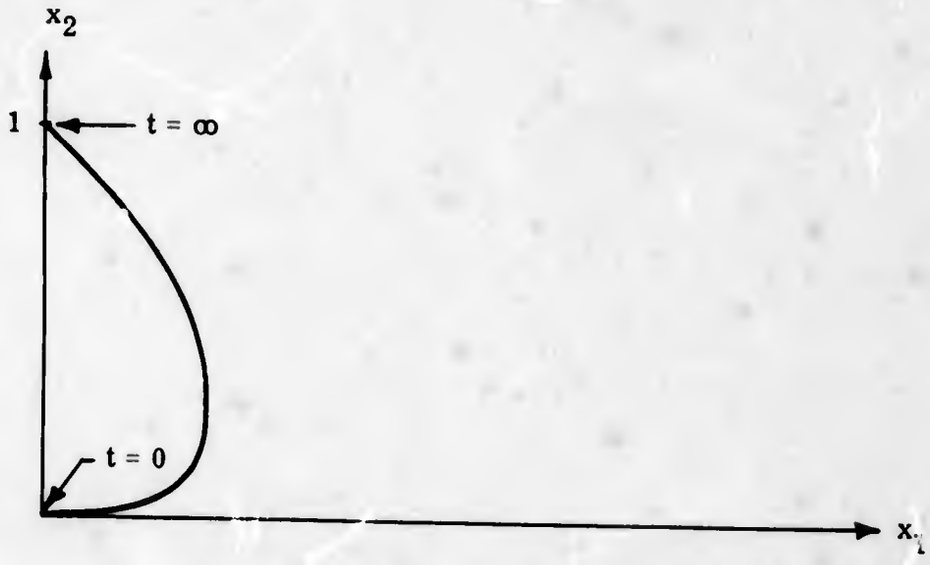

FIGURE 10.26

LOCUS OF NETWORK STATE x

10.25. A similar plot for the state vector $\underline{x}$ is shown in Figure 10.26. Either of these loci is sufficient to describe the network behavior.

The example presented here was a linear network, but the state formulation is, of course, not restricted to this class of systems. The state approach to design and analysis will probably become more widely used as system complexity increases and with the increasing use of computers as design and evaluation tools. Computers will prove particularly useful since the state formulation can usually be written as a set of first order equations (perhaps nonlinear) which are readily integrated by computer techniques.

10.6 PHASE-PLANE ANALYSIS*

Phase-plane analysis is a graphical technique for solving certain types of first and second-order equations. It is essentially a graphical approach to a specific state variable formulation. We shall consider second-order systems here. For systems with an output x(t) which can be described by an equation of the form

$$\frac{d^2x}{dt^2} = f[x(t), \frac{dx}{dt}] \tag{10.67}$$

we may take as state variables of the system the variable itself and its first derivative. Thus, if we define

$$x_1 = x,$$

$$x_2 = \frac{dx}{dt}, \tag{10.68}$$

we have

$$\frac{dx_2}{dt} = f(x_1, x_2),$$

$$x = x_1, \tag{10.69}$$

as the relevant state equations in standard form.

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* Bibliography II, References 4 and 7.

In the previous section, we mentioned that a state-described system could be totally specified by the time history of the state vector, or in other words, by its state trajectory. This idea is precisely the basis for phase-plane analysis, and it is limited to second-order systems mainly to maintain an ease of graphical construction and intuition.

We shall deal with equations similar to Eqn. 10.67, which represents an autonomous system since the independent variable "t" does not appear explicitly. This limitation allows us to find the natural behavior of a system with no input or perhaps for a constant input with arbitrary initial conditions in either case. There are techniques for phase-plane constructions with a forcing function of time present, but we shall not go into these methods here.

We may put Eqn. 10.67 in a form involving x_1 and x_2 only by making use of the relation

$$\frac{d^2x}{dt^2} = \frac{d^2x_1}{dt^2} = \frac{dx_1}{dt}\frac{d}{dx_1}\left(\frac{dx_1}{dt}\right) = x_2\frac{dx_2}{dx_1} \tag{10.70}$$

Eqn. 10.67 then becomes

$$\frac{dx_2}{dx_1} = \frac{f(x_1, x_2)}{x_2} \tag{10.71}$$

The solution to this first order equation, given the initial conditions $x_1(0)$ and $x_2(0)$, yields a trajectory in the x_1 - x_2 plane in which the variable t is involved implicitly. There is a one-to-one correspondence between each value of t and a point on the curve described by Eqn. 10.71. Some general properties which are useful in determining the motion of a point on this trajectory with time are given below.

Let us consider some properties of systems governed by equations of the form in Eqn. 10.67 in terms of the locus of the state vector in the x_1 - x_2 plane. Since $x_2 = \dot{x} = \dot{x}_1$, x_1 must be increasing with time if $x_2 > 0$ and decreasing with time if $x_2 < 0$. Further,

if x_2 is finite then x_1 must be a continuous function of time, since a discontinuity in x_1 would imply an infinite value of $x_2 = \dot{x}_1$.

If any static solutions $x(t) = x_1(t) = C$ exist, then $x_2 = \dot{x}_1 = 0$ and these solutions must correspond to points on the x_1-axis. This also implies that any point in the $x_1 - x_2$ plane not on the x_1-axis cannot correspond to a static solution and, consequently, the state vector (x_1, x_2) must move with time at such a point with a finite velocity in the $x_1 - x_2$ plane.

The time behavior near the x_1-axis may be investigated by considering two cases. First, let us take the case where the trajectory approaches the x_1-axis with $\frac{dx_2}{dx_1}$ being finite. Here, near the x_1-axis, we can approximate the trajectory by a straight line and write

$$x_2 = \frac{dx_1}{dt} = \alpha(x_1 - x_o) \tag{10.72}$$

where x_o is the x_1-axis intercept and α is the slope $\frac{dx_2}{dx_1}$ of the trajectory at the intercept. Eqn. 10.72 has the solution

$$x_1(t) = Ke^{\alpha t} + x_o. \tag{10.73}$$

Thus, if α is negative, the state vector approaches the point $(x_o, 0)$ with increasing time but takes infinite time to reach it. If α is positive, the tip of the state vector clearly moves away from the intercept with finite velocity.

Similarly, we may show that if the trajectory intercepts the x_1-axis with $\frac{dx_2}{dx_1}$ infinite, then the tip of the state vector will reach

the intercept in a finite time and have a finite velocity at the intercept if it approaches the intercept at all.

In order to illustrate these points, let us assume that the solution to Eqn. 10.71 with the initial conditions $[x_1(0), x_2(0)]$ is as shown in Figure 10.27. We may immediately place arrows on the plot in Figure 10.27 to show the motion of the solution with time. Thus, the solution (or tip of the state vector) must move to the right in the upper half-plane where $\frac{dx}{dt} > 0$ and to the left in the lower half-plane where $\frac{dx}{dt} < 0$. We shall assume that $t = 0$ corresponds to the point A in Figure 10.27. As t increases, this point must move to the left. Since $\dot{x}$ is essentially constant from A to B, x will decrease linearly with time as shown in Figure 10.28. At $t = t_1$, the phase-plane solution is at the point B. The solution cannot move from B toward C since x must b e decreasing and, further, it cannot remain at B for any finite time since $\dot{x} \neq 0$. The only remaining possibility which is consistent with the properties mentioned above is that the solution must instantaneously jump to the point D with x remaining constant. Now x must increase (again linearly along DE) as shown in Figure 10.28. As the solution moves along EF, $\dot{x}$ decreases but remains positive, so that x(t) continues to increase but with a slope approaching zero. Since the trajectory crosses the x_1-axis at F with infinite slope, x(t) reaches x_F in finite time as shown and then begins to decrease as the solution passes through F and travels along the arc FO. Since the trajectory intercepts O with a finite slope, x(t) will approach x_O exponentially, so that the complete behavior of x(t) for $t > 0$ is given approximately by the sketch in Figure 10.28.

Now we shall describe some of the methods by which the phase-plane trajectory may be found. In some cases, an analytic solution to Eqn. 10.71 may be found which satisfies the initial conditions $[x_1(0), x_2(0)]$. The curve in the $x_1 - x_2$ plane may then be plotted directly from this solution.

Another method of constructing a phase-plane trajectory is by the isocline method. This consists of finding the loci of constant slope

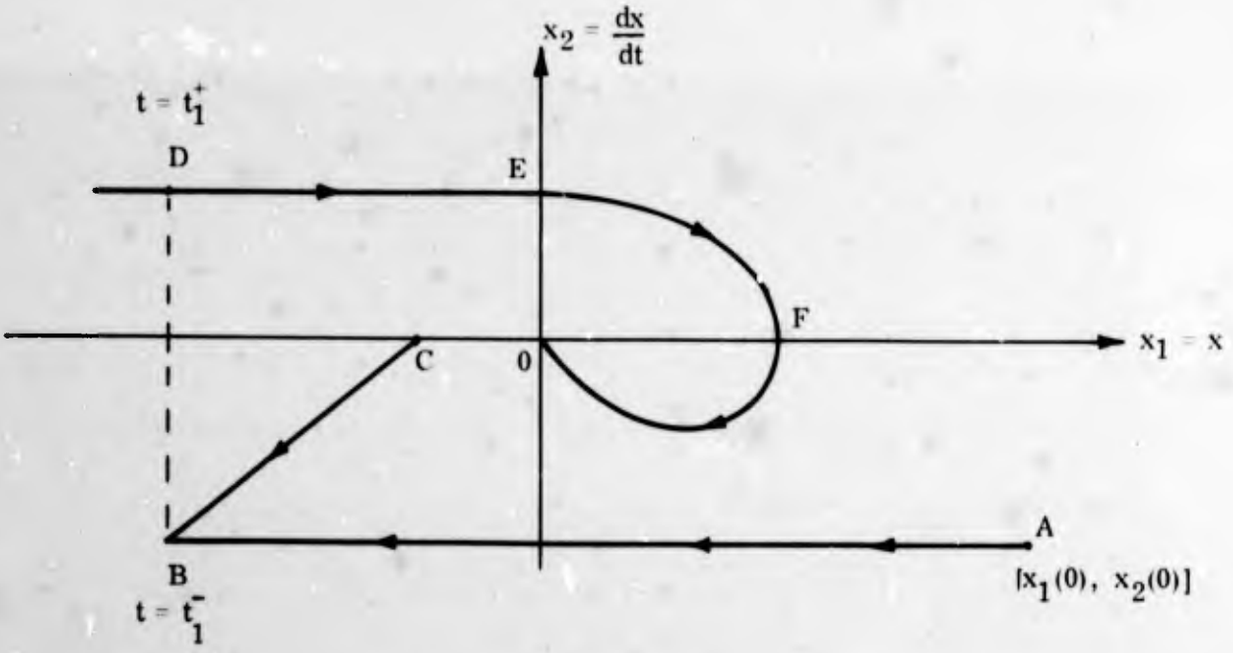

FIGURE 10.27

A POSSIBLE PHASE-PLANE TRAJECTORY

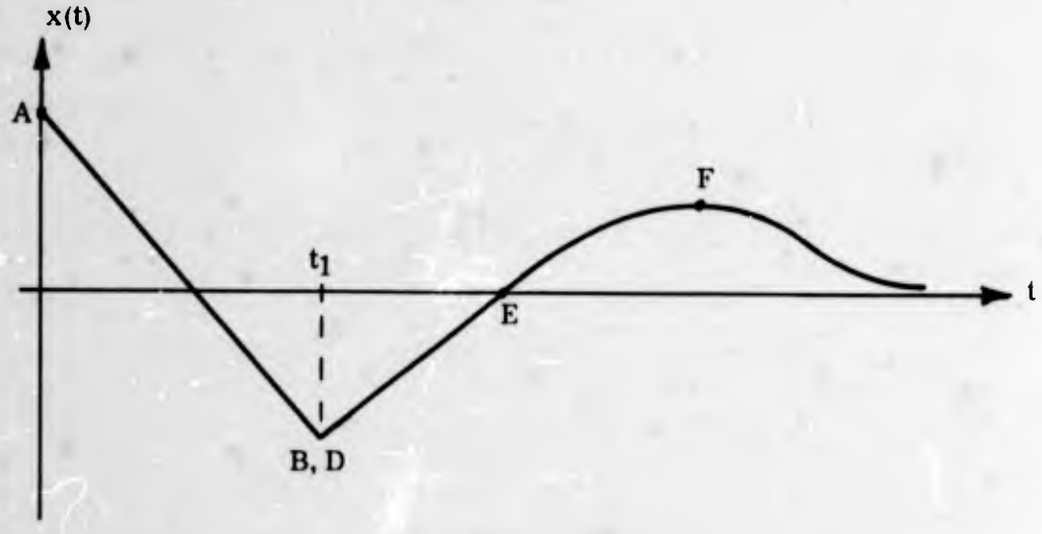

FIGURE 10.28

TIME PLOT OF PHASE TRAJECTORY IN FIGURE 10.27

in the $x_1 - x_2$ plane. In general, the locus of points at which $\frac{dx_2}{dx_1} = m$ may be described by some function $f_m(x_1, x_2) = 0$. Some of these loci are plotted in the $x_1 - x_2$ plane and small segments of slope m are then drawn at points along $f_m(x_1, x_2) = 0$. Given a starting point in the plane (a set of initial conditions), the general character of the phase trajectory can then be sketched. A simple example should serve to illustrate the application of this technique.

We shall consider the nonlinear oscillator in Figure 10.29. The voltage-variable capacitance is a reasonable model for a reverse-biased varactor diode. For this system, we have

$$i = \frac{d}{dt}[vC(v)],$$

$$v_L = \frac{di}{dt} = \frac{d^2}{dt^2}[v \cdot C(v)].$$

Writing Kirchhoff's voltage constraint, we then obtain

$$\frac{d^2}{dt^2}[v \cdot C(v)] + v = 0 \qquad (10.74)$$

as the governing equation. Substituting the expression for C(v) given in Figure 10.29, we have

$$\frac{d^2v}{dt^2} - \frac{2}{1+v}\left(\frac{dv}{dt}\right)^2 + v(1+v)^2 = 0. \qquad (10.75)$$

At this point, we make the substitutions

$$\frac{dv}{dt} = \dot{v},$$

$$\frac{d^2v}{dt^2} = \dot{v}\frac{d\dot{v}}{dv}. \qquad (10.76)$$

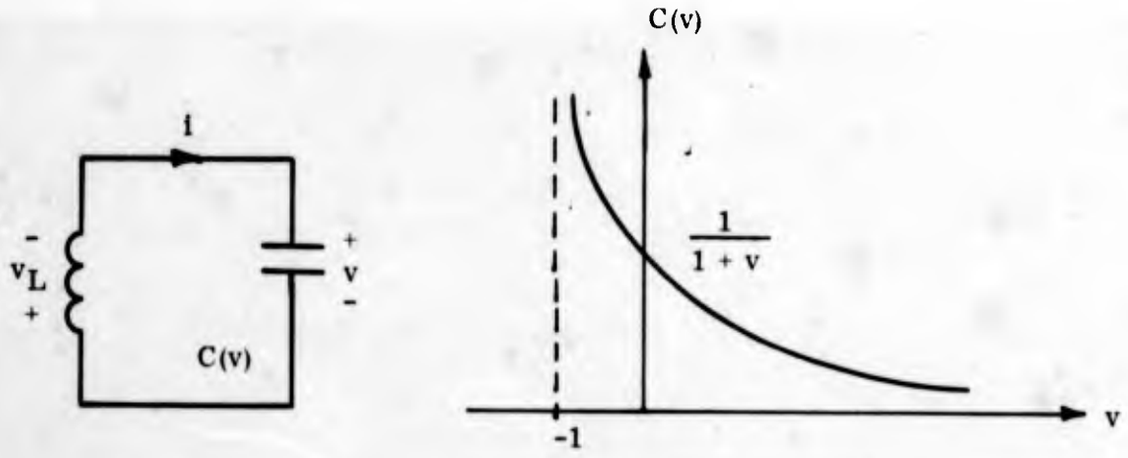

FIGURE 10.29

NONLINEAR OSCILLATOR

Eqn. 10.75 then becomes the first-order equation

$$\frac{d\dot{v}}{dv} = \frac{2\dot{v}}{1+v} - \frac{v(1+v)^2}{\dot{v}} \tag{10.77}$$

Now we shall find the loci of constant slope m in the v - $\dot{v}$ plane. Setting the right side of Eqn. 10.77 equal to m and then solving for $\dot{v}$, we obtain

$$\dot{v} = \frac{m}{4}(1+v)\left[1 \pm \sqrt{1 + \frac{8}{m^2}v(1+v)}\right] \tag{10.78}$$

as the locus of points at which the solution to Eqn. 10.77 has slope m. A number of these curves are plotted in Figure 10.30 for various values of m. The line segments across each curve are segments with the corresponding slope m.

A set of initial conditions [v(o), $\dot{v}$(o)] will determine a point in the phase-plane. We may then sketch the resulting phase-plane locus since this locus must cross <u>every</u> isocline with the indicated slope. Three such loci are shown in Figure 10.30, each corresponding to different initial conditions. For the example chosen, these loci close upon themselves as we would expect since the system is lossless, although nonlinear.

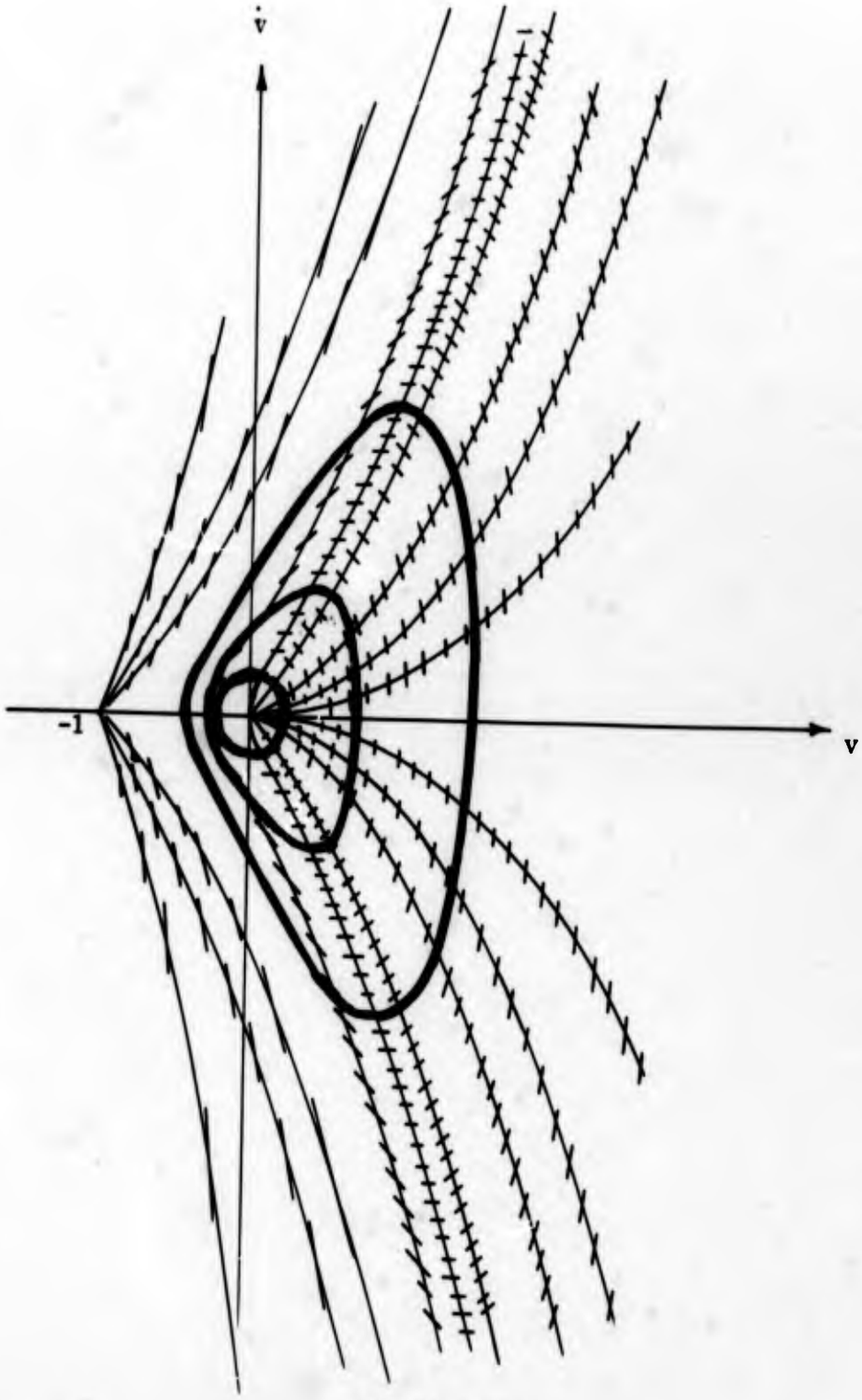

FIGURE 10.30

PHASE-PLANE ISOCLINES FOR NONLINEAR OSCILLATOR

For small amplitude values of v, we observe that the phase-plane locus is almost circular, which corresponds to a sinusoidal time waveform. For larger amplitudes, the locus is quite irregular and indicates that the time history of v(t) [or $\dot{v}(t)$] is nonsinusoidal, as we would expect from a nonlinear oscillator. Note that the peak positive amplitude is larger than the peak negative amplitude. Referring to the circuit, we see that the time average of v(t) must be zero in the steady state due to the inductor constraint. With this additional fact, we may roughly sketch v(t) for the largest contour in Figure 10.30. The resulting v(t) is shown in Figure 10.31.

A number of other methods exist for geometrically constructing a phase-plane trajectory, two of which are called the delta-method and Pell's method. The application of these techniques may be found in the references.*

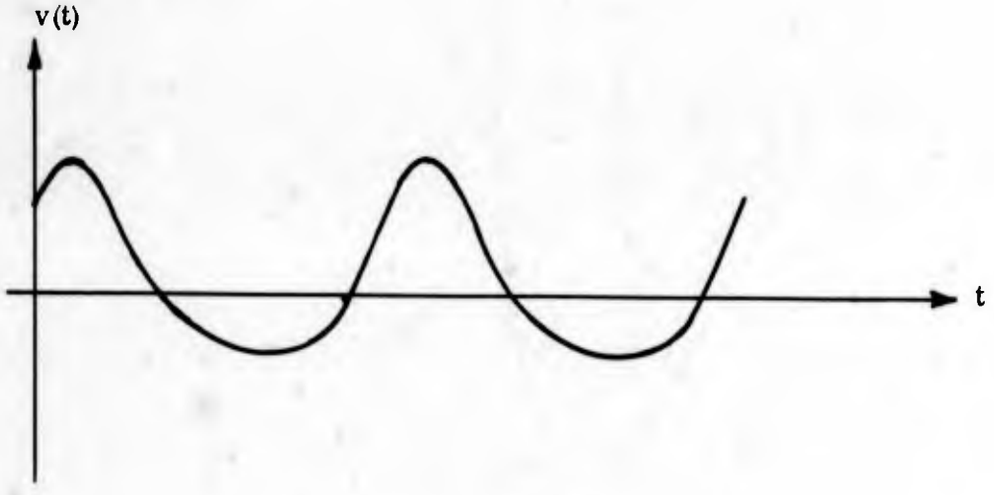

FIGURE 10.31

VOLTAGE WAVEFORM OF NONLINEAR OSCILLATOR

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* Bibliography II, References 4 and 7.

In some simple cases, an analytic solution of Eqn. 10.71 can be found. The phase-plane trajectories may then be plotted directly from this solution. Further, if the solution to Eqn. 10.71 can be written as

$$x_2 = g(x_1),$$

we then have from Eqn. 10.68 that

$$\frac{dx}{dt} = g(x),$$

or

$$t = \int \frac{dx}{g(x)} + c. \tag{10.79}$$

Eqn. 10.79 defines x(t) implicitly. This form may or may not have an explicit form in terms of elementary functions.

We see that phase-plane analysis can be quite useful in handling certain second-order systems. The graphical representation of the system can often yield some insight into the behavior of the system. Further, the system operation is found by solving two first-order equations instead of a second-order equation. Of course, there are certain limitations to the usefulness of this technique. The system must have some reasonably analytic description so that the governing equation(s) can be written, For continuous nonlinear devices (diodes, transistors, nonlinear inductors, etc.) this is usually the case. Also by defining various regions of operations, piecewise - linear devices may be handled by phase-plane analysis. We have only considered autonomous systems. This is a limitation in the sense that the complexity of analysis is significantly increased when forcing functions are present. The references should be consulted for a more detailed discussion of these points. *

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* Bibliography II, Reference 7

10.7 HILBERT TRANSFORMS *

The stabilization of all linear and certain nonlinear control systems can be regarded as the manipulation of the magnitude and phase of the open-loop gain to insure that the closed-loop transfer function has no poles in the right half-plane. As presented in most texts, this stabilization is usually accomplished by inserting into the loop selected members of a class of networks, such as lead and lag networks, whose magnitude and phase have been tabulated. This approach, while providing useful solutions to many problems, is basically dependent upon the structure of the tabulated corrective networks. As such, it does not offer much insight into questions of whether or not it is possible to stabilize a given system within imposed constraints such as loop gain and bandwidth, for example. Insight into such questions requires examination of the basic relationship between the magnitude and phase of linear system functions. The Hilbert transform is the key to this relationship and an understanding of it provides qualitative guidelines as well as quantitative designs for system stabilization.

Hilbert transforms are transforms that relate the real and imaginary parts of analytic functions of a complex variable. Consider the complex variable

$$s = \sigma + j\omega \tag{10.80}$$

with real part σ and imaginary part ω. Now consider the function f(s) of the complex variables s. This can be written

$$f(s) = u(\sigma, \omega) + jv(\sigma, \omega) \tag{10.81}$$

where $u(\sigma, \omega)$ is the real part of f(s) and $v(\sigma, \omega)$ is the imaginary part of f(s). The Cauchy-Riemann equations, which assure the

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* Bibliography II, Reference 8

uniqueness of the derivative of a complex function, show that the real and imaginary parts of the function are related. These equations are

$$\frac{\partial u}{\partial \sigma} = \frac{\partial v}{\partial \omega} \tag{10.82}$$

and

$$\frac{\partial u}{\partial \omega} = -\frac{\partial v}{\partial \sigma} \tag{10.83}$$

Hilbert transforms, which apply to any complex function that satisfies the Cauchy-Riemann equations at every point in either the left or the right half of the complex plane of the argument, place this relation between real and imaginary parts of the function in a particularly useful form along the ω-axis. The Hilbert transform relations are

$$u(\omega) = \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{v(\eta)\,d\eta}{\omega - \eta} \tag{10.84}$$

and

$$v(\omega) = -\frac{1}{\pi} \int_{-\infty}^{\infty} \frac{u(\eta)\,d\eta}{\omega - \eta} \tag{10.85}$$

where we have written $u(0, \omega) = u(\omega)$ and $v(0, \omega) = v(\omega)$. Notice that either transform can be obtained from the other by simply interchanging u with v and reversing the algebraic sign of one of the functions.

Now, let us see how these transforms are useful in system theory and in stability problems. The system function of any realizable linear passive system is analytic in the right half of the s-plane. Also, without any loss of generality in the practical case, we can exclude all ω-axis poles from system functions of passive physical networks. Thus, we can safely assume that for all passive physical networks any system function is analytic along the ω-axis as well as throughout

the right half-plane. Therefore, the Hilbert transforms enable us to determine the real part of the system function from the imaginary part along the ω-axis and vice versa. Said in another way, a knowledge of either the real part or the imaginary part along the ω-axis is sufficient to construct the entire system function. This is a useful result in network theory. However, in stability problems of control systems, it is usually more convenient to think in terms of the magnitude and phase of a system function rather than its real and imaginary parts.

To this end, consider a system function H(s) in which the argument s is the complex frequency $s = \sigma + j\omega$. We can represent H(s) in the form

$$H(s) = |H(s)|\, e^{j\theta(s)}. \tag{10.86}$$

If we take the logarithm of H(s), we obtain

$$\ln H(s) = \ln |H(s)| + j\theta(s). \tag{10.87}$$

The real part of this expression is the logarithm of the magnitude of the system function and the imaginary part is the angle or phase of the system function. It is tempting at this point to conclude that if the system function H(s) is analytic in the right half-plane then the logarithm of the magnitude of the system function is related to the phase of the system by Hilbert transforms. This conclusion is premature, however, because ln H(s) is not analytic for frequencies at which H(s) = 0. Therefore, the logarithm of the magnitude of H(s) and the phase, $\theta(s)$, of H(s) are related by Hilbert transforms only if H(s) has no zeros or poles in the right half-plane. As has been mentioned, the H(s) of all linear passive systems have no poles in the right half-plane. Those H(s) that, in addition, have no zeros in the right half-plane are called minimum phase system functions. [This terminology is used because many system functions can have the same ln $|H(s)|$ with different $\theta(s)$. The particular system function that has no right half-plane zeros in H(s) has the <u>minimum</u> phase among all these functions.]

Since Hilbert transforms relate the log-magnitude and the phase only of minimum phase networks, it is clear that if the phase is

determined from a given log-magnitude by a Hilbert transform, then the phase so determined will be the minimum phase function that can be associated with the given magnitude function.

Thus, for minimum phase system functions, we can write

$$\ln |H(\omega)| = \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{\theta(\eta) d\eta}{\omega - \eta} \tag{10.88}$$

and

$$\theta(\omega) = -\frac{1}{\pi} \int_{-\infty}^{\infty} \frac{\ln |H(\eta)|}{\omega - \eta} d\eta \tag{10.89}$$

where

$$H(\omega) = |H(\omega)| e^{j\theta(\omega)}$$

As a first illustration of the Hilbert transform, we shall select a very simple example which will serve to explain a useful graphical evaluation technique. Consider a filter network with the idealized log-magnitude characteristic shown in Figure 10.32. By direct application of the Hilbert transform Eqn. 10.89, we obtain the phase function

$$\theta(\omega) = -\frac{1}{\pi} \int_{-\omega_1}^{\omega_1} \frac{d\eta}{\omega - \eta} = \frac{1}{\pi} \ln \left| \frac{\omega - \omega_1}{\omega + \omega_1} \right| \tag{10.90}$$

The function $\theta(\omega)$ given by this equation is sketched in Figure 10.33.

While the evaluation of the Hilbert transform was relatively easy for the above example, it is readily appreciated that the integration can become very involved for rather simple filters of practical interest. However, inspection of the Hilbert transform pair Eqns. 10.88 and 10.89 reveals that the integrals are simply the convolution

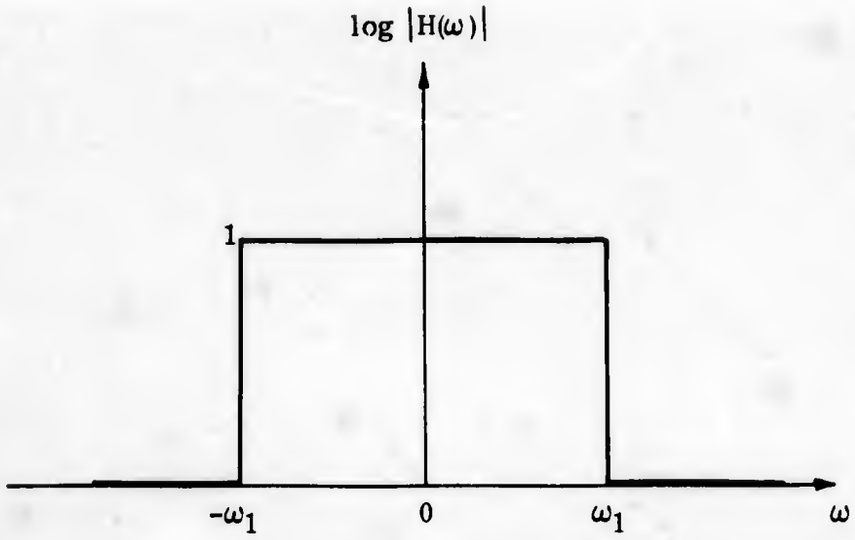

FIGURE 10.32

IDEALIZED FILTER

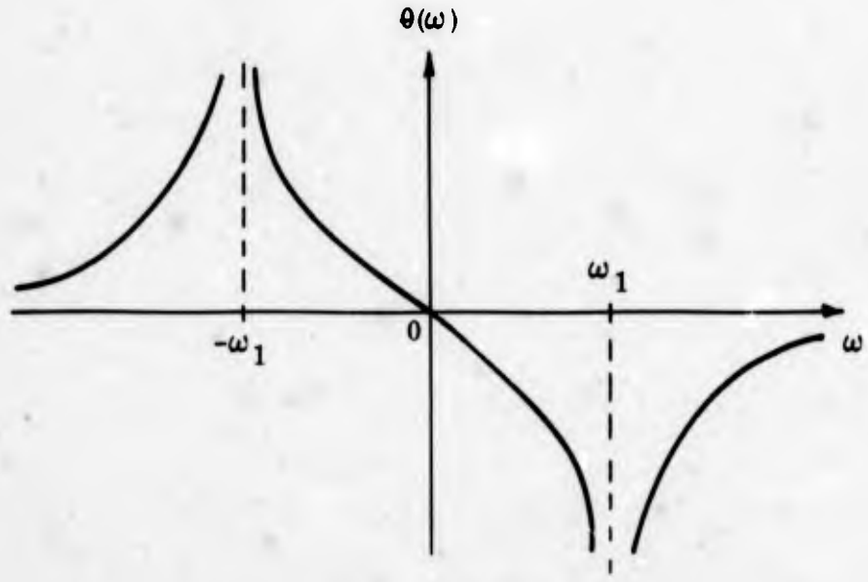

FIGURE 10.33

MINIMUM PHASE FUNCTION ASSOCIATED WITH THE IDEAL FILTER OF FIGURE 10.32

of $\theta(\omega)$ and $\ln |H(\omega)|$ respectively with the function $\frac{1}{\omega}$. Thus, we can directly use any of the familiar graphical techniques for the evaluation of the integrals.*

Inspection of Eqn. 10.89 indicates that $\theta(\omega)$ can be evaluated, for any specific value of ω, by taking the area under the product of $\ln |H(\eta)|$ with $\frac{1}{\omega - \eta}$. Both of these functions are sketched on the same graph in Figure 10.34 for the example given by Figure 10.32. As ω is increased, the function $\frac{1}{\omega - \eta}$ simply translates to the right along the η-axis. With very little practice, it is easy to visualize the area under the product of the functions as ω is increased and, thus, it is easy to qualitatively sketch the form of $\theta(\omega)$. [Remember that $\theta(\omega)$ is $-\frac{1}{\pi}$ times the area under the product of the curves shown in the example of Figure 10.34.] This should be done for this example as an exercise and the result should be checked against that shown in Figure 10.33.

The inspection technique mentioned above can be used to obtain surprisingly basic results in filtering and stabilizing applications without ever precisely calculating the transform. To illustrate this point, we shall select an example of a power processing system employing closed-loop pulse-width techniques.

Consider the simplified pulse-width system shown in Figure 10.35. It is necessary, for proper operation of the system, to filter out all of the switching components of the pulse-width signal before it is fed back for comparison to the input. It is also necessary that the system be stable with respect to the usual linear criterion of no poles in the right half of the s-plane. Let us suppose that the desired system bandwidth is ω_b and that it has been decided that all the harmonics of the switching frequency must be attenuated by, at least, a factor of M relative to the filter attenuation in the signal bandwidth ω_b.

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* Bibliography II, Reference 10

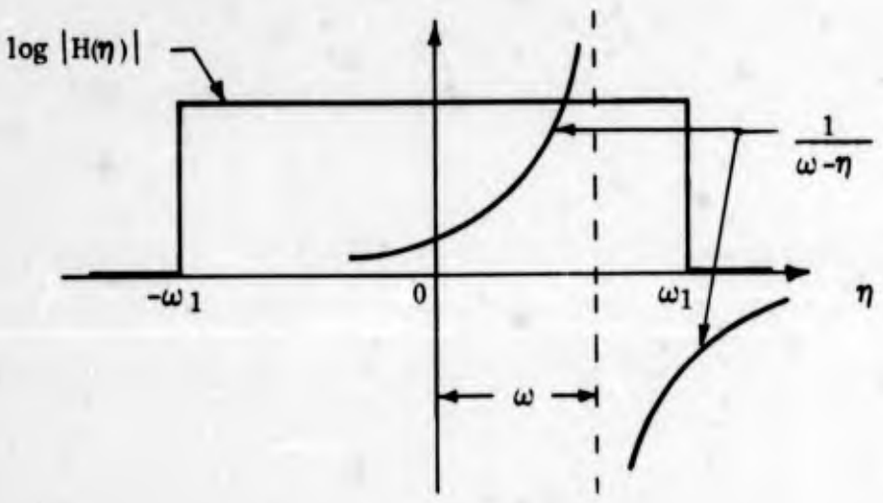

FIGURE 10.34

GRAPHICAL INTERPRETATION OF THE HILBERT TRANSFORM

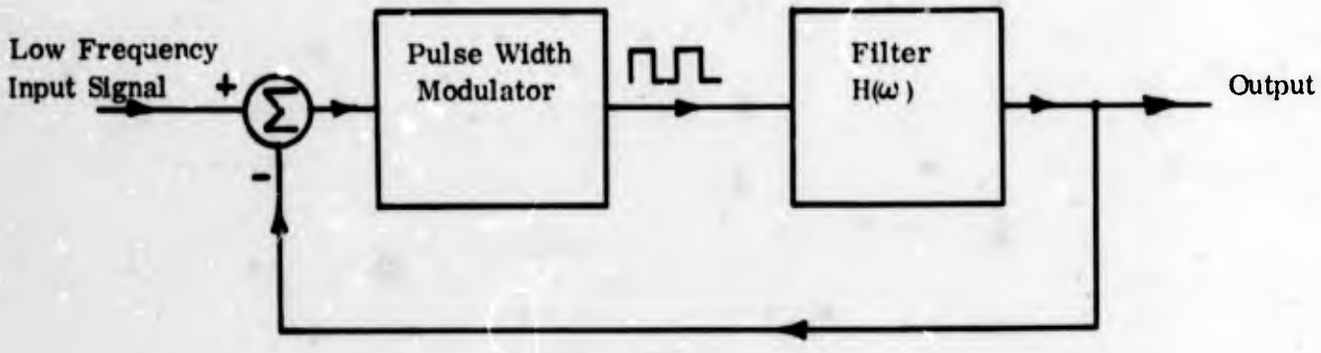

FIGURE 10.35

SIMPLIFIED BLOCK DIAGRAM OF PULSE WIDTH CONTROL SYSTEM

We shall now compare the performance of three different filter characteristics, each of which has the desired bandwidth ω_b and the desired harmonic attenuation. The log-magnitudes of the three filter characteristics are shown in Figure 10.36. Filter No. 1 continues to roll off beyond ω_s. Filter No. 2 levels off to a constant attenuation (slightly greater than a factor of M) above ω_s. Filter No. 3 dips at each of the frequencies present in the pulse width switching waveform and returns to a relatively high gain between these frequencies.

It is of direct interest to investigate the relative amounts of phase shift inherent in each of the filters since this will determine the maximum loop gain that can be employed with stable operation. A qualitative result, sufficient to select the filter with the minimum phase shift, can be obtained by direct inspection of the graphical interpretation of the Hilbert transform as previously presented for the simple example of Figure 10.34. For convenience in visualizing the Hilbert transform, the function $\frac{1}{\omega-\eta}$ is superimposed on the filter characteristics of Figure 10.36. The phase functions of Figure 10.37 were sketched, without calculation, by visually estimating the area under the product of the filter log-magnitude with $\frac{1}{\omega-\eta}$ as a function of ω. The qualitative results are sufficient to draw conclusions regarding the effect of the behavior of $\ln |H(\omega)|$ outside the bandwidth ω_b upon the phase, $\theta(\omega)$, inside the bandwidth ω_b. From the graphical interpretation of the Hilbert transform, it is immediately apparent that in order to reduce the phase shift in the filter bandwidth it is necessary to shape the magnitude response outside the passband in the direction to give the same area under the product of $\ln |H(\omega)|$ with $\frac{1}{\omega-\eta}$ for both the positive and negative tails of $\frac{1}{\omega-\eta}$. Thus, the Hilbert transform tells us that to achieve the smallest phase inside ω_b the magnitude of $H(\omega)$ should not be rolled off outside ω_b any more than is absolutely necessary to meet the filtering requirements - in this case, the specification on the harmonic attenuation. The Hilbert transform also shows us that, when applicable, a band-stop filter always outperforms a low-pass filter with respect to lower phase

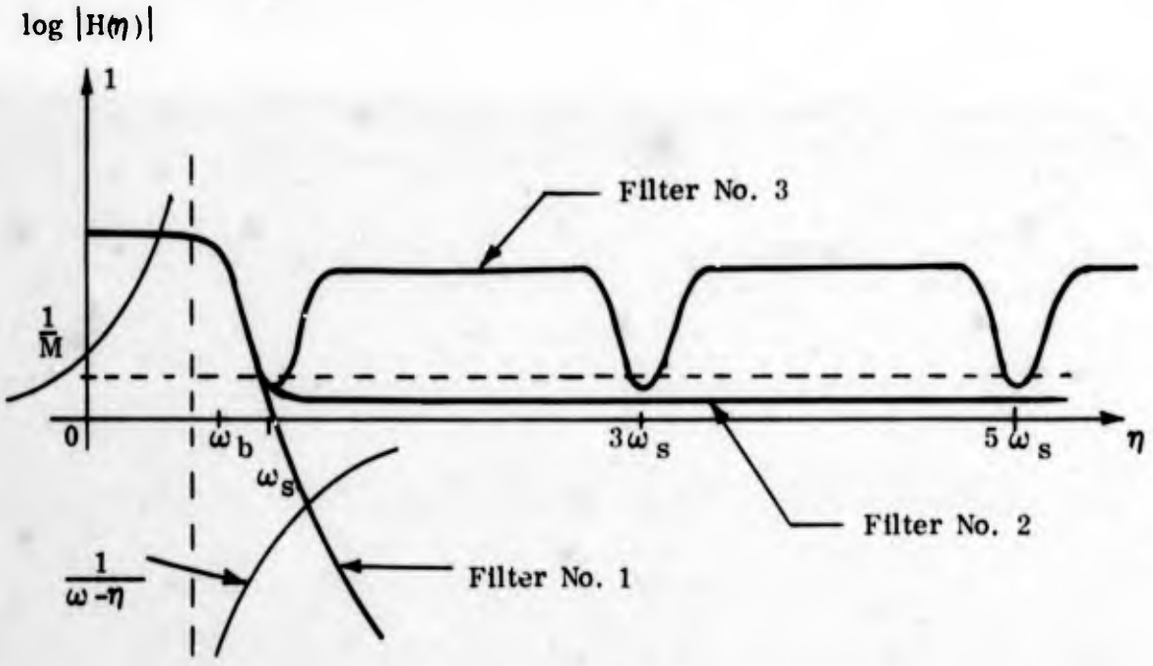

FIGURE 10.36

LOG-MAGNITUDE CHARACTERISTICS FOR THREE FILTERS HAVING THE SAME BASEBAND BEHAVIOR

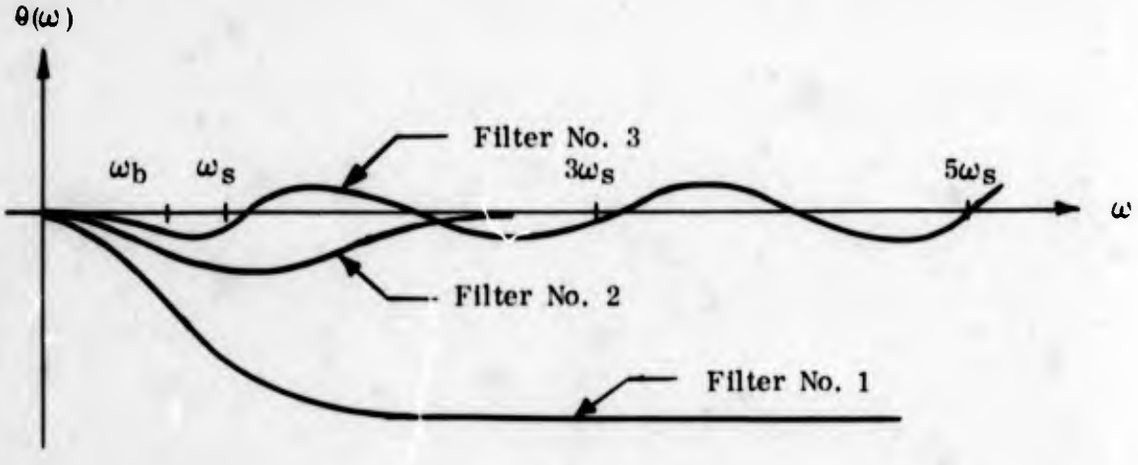

FIGURE 10.37

SKETCHES OF MINIMUM PHASE FUNCTIONS ASSOCIATED WITH THE MAGNITUDE RESPONSES OF FIGURE 10.36

shift in the pass band. It is interesting that these basic conclusions can be obtained without quantitative evaluation of a single expression and, further, that they are not limited to any specific network structure.

In summary, the Hilbert transforms provide the relations between the log-magnitude of a system function and the minimum phase that can be associated with this function. If the system function has no zeros in the right half-plane, then the Hilbert transforms directly relate its phase to its log-magnitude. If zeros are present in the right half-plane, then the Hilbert transforms relate the given log-magnitude function to the phase of a system function having the same log-magnitude function but having all the right half-plane zeros mirror imaged into the left half-plane. The phase of the latter system function is the minimum phase that can be associated with the given log-magnitude function. The Hilbert transforms are particularly useful in modern power processing systems because they provide both insight and quantitative information for the complex problem of designing stable closed-loop systems in the presence of undesirable switching frequency spectrum components.

10.8 BOOLEAN ALGEBRA

It should be evident that the algebra which we use in most analysis does not describe the operation of certain binary processes such as logical switching functions. The rules under which we must handle such functions are quite alien to the axioms of normal algebra. We can, however, define an algebra which is applicable to the analysis of such problems although the domain, axioms and definitions in this algebra will be quite different from those to which we are accustomed. We shall relate a mathematical structure called Boolean algebra and discuss some of the properties of this algebra. It will become evident that the manipulations in this algebra are exactly those which are needed to describe the logical operation of switching circuits. As is true for many mathematical structures, the axioms of Boolean algebra apply to other areas. Boolean algebra is the appropriate structure for the algebra of logic and the algebra of sets, although we shall be concerned with its application to switching circuits only.

Boolean algebra is defined on the two-element set [0, 1]. A

Boolean variable is a variable which may take on either the value 0 or 1. Since the domain is limited to two elements, we may state the following concerning a Boolean variable (denoted here by upper-case letters):

$$A \neq 0 \text{ implies } A = 1,$$

$$A \neq 1 \text{ implies } A = 0.$$

Two operations are defined and will be denoted by + and · as in ordinary algebra, although the interpretation of these operations will not be the same. As in ordinary algebra, the juxtaposition of two variables will be taken to be "multiplication" so that $AB \triangleq A \cdot B$. In Boolean algebra, these operations are defined by

$$\left.\begin{aligned} &0 + 0 = 0, \\ &1 + 0 = 0 + 1 = 1, \\ &1 + 1 = 1, \end{aligned}\right\} \tag{10.91}$$

$$\left.\begin{aligned} &0 \cdot 0 = 0, \\ &0 \cdot 1 = 1 \cdot 0 = 0, \\ &1 \cdot 1 = 1. \end{aligned}\right\} \tag{10.92}$$

Both operations are commutative and associative, which we may express as

$$\left.\begin{aligned} &A + B = B + A, \\ &AB = BA, \end{aligned}\right\} \tag{10.93}$$

$$\left.\begin{aligned} &(A + B) + C = A + (B + C), \\ &(AB)C = A(BC). \end{aligned}\right\} \tag{10.94}$$

Theorems in Boolean algebra, such as Eqns. 10.93 and 10.94 may be proven by exhaustion. That is, we may show that the relation in question is true for all values of the variables involved. This

process is clearly applicable solely due to the finite size of the domain. Theorems concerning variables with an infinite number of allowed values clearly cannot be proven by testing all possibilities. This fact can be of great use in proving theorems.

We also define a complementing operation, denoted by a bar over a Boolean value, by

$$\left.\begin{aligned}\overline{0} &= 1,\\ \overline{1} &= 0.\end{aligned}\right\} \tag{10.95}$$

With the complement thus defined, we have for a Boolean variable A,

$$\left.\begin{aligned}\overline{A} &= 1 \text{ when } A = 0,\\ \overline{A} &= 0 \text{ when } A = 1.\end{aligned}\right\} \tag{10.96}$$

A number of theorems which are quite useful in manipulating Boolean expressions are listed here. Their proofs, although simple, will not be given.

$$1 + A = 1 \tag{10.97a}$$

$$1 \cdot A = A \tag{10.97b}$$

$$0 + A = A \tag{10.97c}$$

$$0 \cdot A = 0 \tag{10.97d}$$

$$A + A = A \tag{10.97e}$$

$$A \cdot A = A \tag{10.97f}$$

$$A + \overline{A} = 1 \tag{10.97g}$$

$$A \cdot \overline{A} = 0 \tag{10.97h}$$

$$A + AB = A \tag{10.97i}$$

$$A + \overline{A}B = A + B \tag{10.97j}$$

$$A(B + C) = AB + AC \tag{10.97k}$$

$$A + BC = (A + B)(A + C) \tag{10.97ℓ}$$

$$\overline{A + B} = \bar{A}\bar{B} \tag{10.97m}$$

$$\overline{(AB)} = \bar{A} + \bar{B} \tag{10.97n}$$

Eqn. 10.97k is the distributive law of ordinary algebra. Eqn. 10.97ℓ, however, has no such counterpart. Its presence here may be interpreted as a result of the complete duality between the two Boolean operations, which it is again worth stressing are <u>not</u> ordinary multiplication and addition, as some of the above theorems readily assert.

As an example, let us consider the Boolean function

$$f(A, B, C) = A + \bar{B}(C + A)(C + B). \tag{10.98}$$

By using Eqns. 10.93, 10.94 and 10.97, we may find a simpler but equivalent expression. We shall proceed as follows:

$$\begin{aligned}
f(A, B, C) &= A + \bar{B}(C + A)(C + B) \\
&= A + \bar{B}(C + B)(C + A) && \text{(by Eqn. 10.93)} \\
&= A + (\bar{B}C + \bar{B}B)(C + A) && \text{(by Eqn. 10.97k)} \\
&= A + (\bar{B}C + 0)(C + A) && \text{(by Eqn. 10.97h)} \\
&= A + \bar{B}C(C + A) && \text{(by Eqn. 10.97c)} \\
&= A + \bar{B}CC + \bar{B}CA && \text{(by Eqn. 10.97k)} \\
&= A + \bar{B}C + \bar{B}CA && \text{(by Eqn. 10.97f)} \\
&= A + A\bar{B}C + \bar{B}C && \text{(by Eqns. 10.93 \& 10.94)} \\
&= A + \bar{B}C. && \text{(by Eqn. 10.97i)}
\end{aligned}$$

This is by no means the only sequence of steps by which we may simplify the given expression, nor is the result in a unique form. We may desire to write the result in the form

$$f(A, B, C) = (A + \overline{B})(A + C) = A + \overline{B}C \qquad (10.99)$$

which follows from Eqn. 10.97*l*. This example should serve to illustrate the manipulation of Boolean expressions.

Now, we should like to show how Boolean algebra applies to the analysis of switching circuits. We consider a single pole switch and say the switch may be in one of two possible states - open or closed. If we denote the state of the switch by a variable A, we shall define A by

A = 0 when the switch is open,

A = 1 when the switch is closed.

We can now consider the state of the switch to be synonomous with the Boolean variable A.

If we consider a network of switches between two points, as shown in Figure 10.38, we may then wish to ask when there is a transmission path between the terminals of the network. The same letter by two or more switches simply denotes the fact that these switches are either all open or all closed. The states B and $\overline{B}$ by two switches indicates that one switch is closed whenever the other is open and vice versa. We may define a transmission function T_{12} for this network

$$T_{12} = \begin{cases} 0, \text{ when there is no conducting path between 1 and 2} \\ 1, \text{ when there is a conducting path between 1 and 2.} \end{cases}$$

We may then ask how we can describe T_{12} in terms of the states A, B and C of the component switches. In order to accomplish this, let us first consider the following simple examples.

We may consider a short circuit as a switch that is always closed and, thus, its state can be represented by "1". Similarly, an

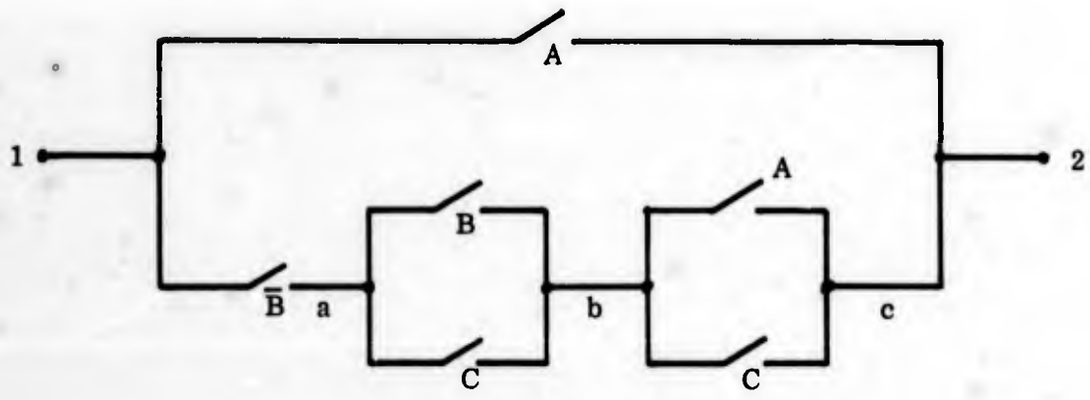

FIGURE 10.38

SWITCHING NETWORK TRANSMISSION

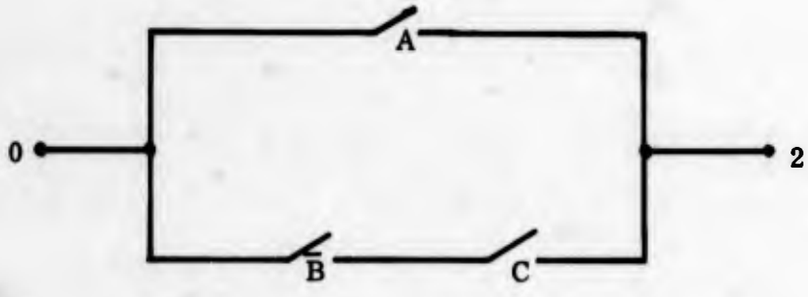

FIGURE 10.39

EQUIVALENT TRANSMISSION FOR NETWORK IN FIGURE 10.38

open circuit can be represented by "0". A conducting path exists through two series switches if and only if both switches are closed. If we denote this transmission by T and the states of the switches by A and B, we may then write

$$T = AB.$$

Clearly, the Boolean "multiplication" operation defined by Eqn. 10.92 has the desired property.

Similarly, if the switches are connected in parallel, the transmission T is given by

$$T = A + B.$$

Boolean "addition" as defined in Eqn. 10.91 has the desired property that the "sum" is 1 if at least one component of the "sum" is 1, corresponding to the fact that a transmission is achieved if at least one switch is closed.

Thus, if the operations + and · correspond to "in parallel with" and "in series with" and the Boolean variables correspond to the states of network switches then the transmission function satisfies all of the postulates of Boolean algebra. In such a case, all the Theorems of Boolean algebra may then be used to handle transmission functions. For example, let us consider the theorem of Eqn. 10.97a. In terms of a switching network transmission, this may be stated as "the transmission of a switch in parallel with a short circuit is always closed (or a short circuit)". The remaining theorems may be stated in an equivalent manner.

Let us return now and use these results on the network in Figure 10.38. If we denote the transmission from a to b by T_{ab}, we have

$$T_{ab} = B + C.$$

Similarly,

$$T_{bc} = (A + C),$$

and also

$$T_{ac} = T_{ab}T_{bc} = (B + C)(A + C).$$

Proceeding in this manner, we obtain the overall transmission

$$T_{12} = A + \bar{B}(B + C)(A + C) \tag{10.100}$$

From Eqn. 10.99, we saw that this transmission can be written

$$T_{12} = A + \bar{B}C \tag{10.101}$$

By reading "+" as "in parallel with" and "·" as "in series with", we may realize the transmission function in Eqn. 10.101 as shown in Figure 10.39. Given any states for A, B and C this switch network has a transmission identical to the network in Figure 10.38, even though it is much simpler.

As a synthesis example, let us find a switch network such that there is a transmission through the network if two and only two of three switches are in the "1" state. We allow a switch to control any number of contact sets, all of which are operated together. If we denote the three independent states by A, B and C, we may set up the following table defining the desired transmission T:

	A	B	C	T
1	0	0	0	0
2	0	0	1	0
3	0	1	0	0
4	0	1	1	1
5	1	0	0	0
6	1	0	1	1
7	1	1	0	1
8	1	1	1	0

Looking at line 4, we see that T = 1 when (A, B, C) = (0, 1, 1). An expression in A, B and C which has the value one for the given values

of A, B and C and zero otherwise is seen to be $\bar{A}BC$. Similarly, the expressions giving T = 1 for lines 6 and 7 are $A\bar{B}C$ and $AB\bar{C}$ respectively. Since we desire T = 1 if any one of these combinations is one, we write

$$T = \bar{A}BC + A\bar{B}C + AB\bar{C} \tag{10.102}$$

which is easily shown to yield the values in the above table. A switch network which realizes this transmission is shown in Figure 10.40.

In this network, let us consider the effects of joining nodes 4 and 5 and nodes 6 and 7 as indicated by the dotted lines. Clearly when A = 1, nodes 4 and 5 are connected through the switches and we have not disturbed the transmission function by joining these nodes. When A = 0, any path through the 4 - 5 connection cannot pass through A (since it is open). The only other paths including the connection between nodes 4 and 5 must pass through B and $\bar{B}$ in series. Since one of these is always open, we conclude that the transmission function is unaffected by connecting nodes 4 and 5. A similar argument will show that connecting nodes 6 and 7 is also allowed. By connecting these nodes, we have paralleled two A contacts, which we may replace by a single A contact, and similarly for C (by Eqn. 10.97e.). The resulting network is shown in Figure 10.41.

Consider the double-throw switch shown in Figure 10.42 with the switch position described by A as shown. We may easily see that the transmission functions for this three-terminal device are given by

$$T_{12} = A$$

$$T_{13} = \bar{A}$$

$$T_{23} = 0. \tag{10.103}$$

Using this result, we may then realize the switch network in Figure 10.41 by the network in Figure 10.43. Comparing this with the network in Figure 10.40, we observe that the desired transmission can be realized by two single pole, double-throw switches and one double-pole, double-throw switch. Note from Figure 10.41 that this realization is not a series/parallel network.

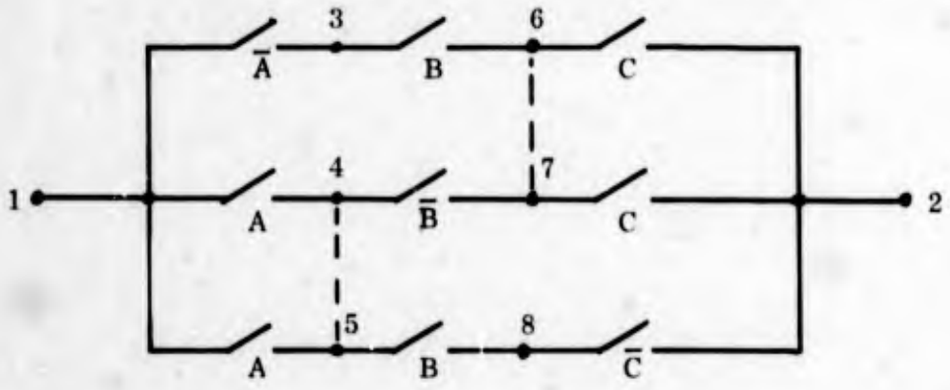

FIGURE 10.40

REALIZATION OF A TRANSMISSION FUNCTION

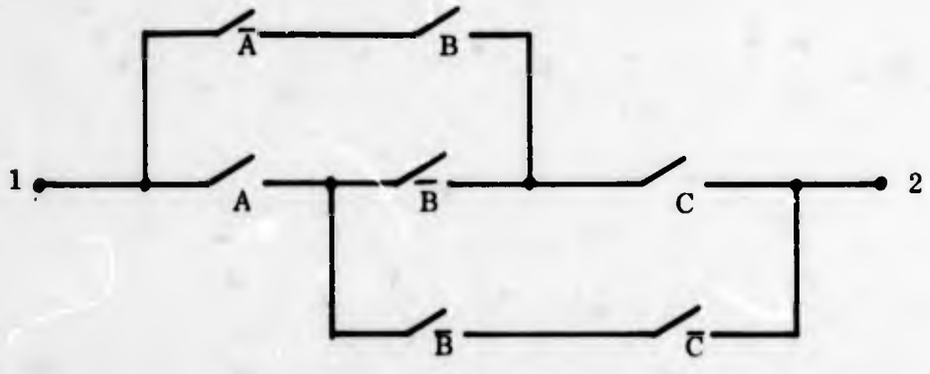

FIGURE 10.41

NETWORK OF FIGURE 10.40 AFTER NODE REDUCTION

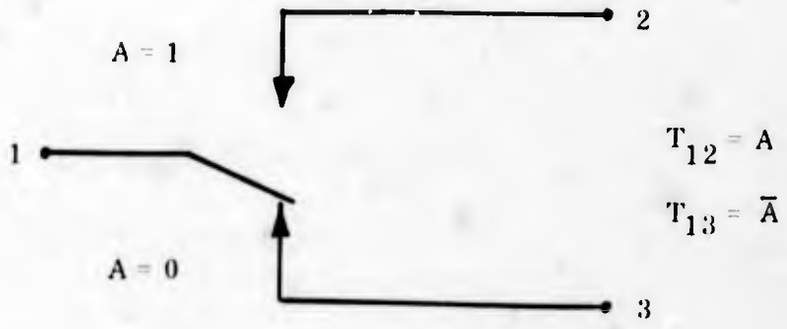

FIGURE 10.42

DOUBLE-THROW SWITCH

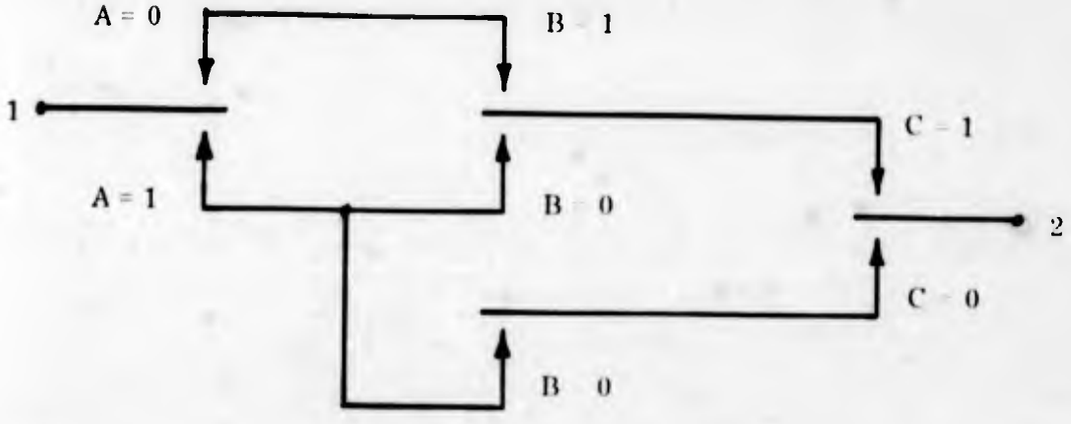

FIGURE 10.43

REALIZATION OF NETWORK IN FIGURE 10.41 USING DOUBLE-THROW SWITCHES

These simple examples are obviously not intended as an exhaustive study of Boolean analysis and design, but they should serve to indicate the basic concepts involved in combinatorial switching circuit analysis.

Sequential Switching Circuits

In the preceding examples, we assumed that the switch states were given and the desired network transmission was to be found. One parameter which we did not consider was time - that is, we assumed no time dependence or sequencing in the networks. Networks whose behavior can be described solely as a function of switch states are called combinatorial.

Another class of switching networks has properties which depend on time relationships in the networks. For this class, the state of a network will be a function of the "input" states and also a function of the past history of the network. Such networks, called sequential switching circuits, are encountered in computers and relay circuits. The complications arising in sequential circuit analysis are due to the interdependence of various switches in the network. The dependent nature of sequential circuits gives these circuits their interesting properties - and problems.

The salient features of sequential analysis are perhaps best illustrated by means of an example. We consider the relay network shown in Figure 10.44. Here there are two multipole "input" switches, A and B, whose positions are determined independently of any of the network properties. We assume that all the A labeled switches are in the "A" position when A = 1 and in the "$\overline{A}$" position when A = 0, and similarly for B. The C_1 - $\overline{C}_1$ contacts are operated by relay coil K_1 and the C_2 - $\overline{C}_2$ contacts by relay coil K_2. These relay contacts will be in the complemented positions ($\overline{C}_1$ or $\overline{C}_2$) when the corresponding coils are not excited. The interesting properties of this network are due to the effects of the relay contacts on the relay coil excitations.

We can observe that the voltages and currents in the coils at any time are uniquely determined if the positions of all switches

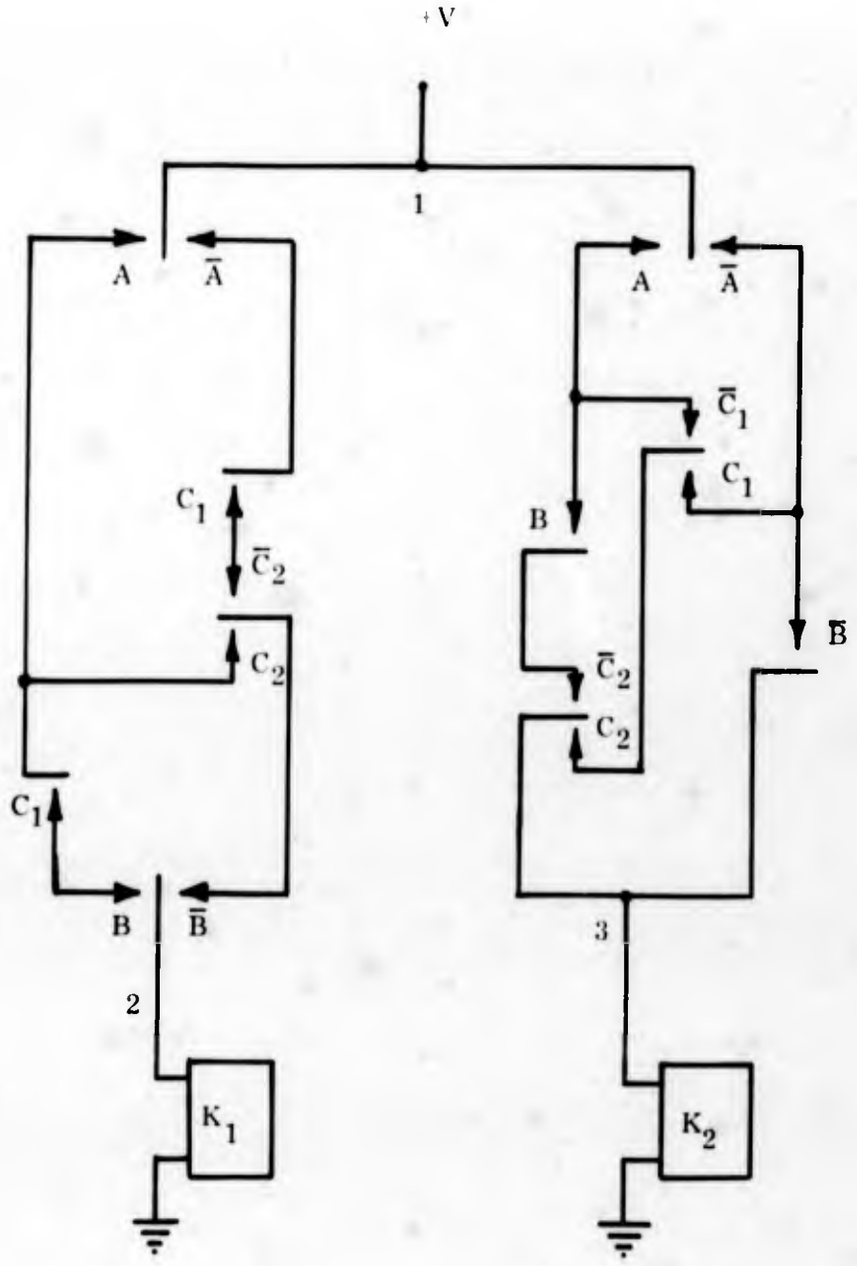

FIGURE 10.44

EXAMPLE FOR SEQUENTIAL ANALYSIS

(including relay contacts) are known at that time. Thus, for any set of switch contact states at time t, we may calculate the relay coil excitations at time t in terms of these contact states. At this point, we shall use K_1 and K_2 as Boolean variables describing the excitation of the respective relay coils, so that $K_1 = 0$ when relay coil K_1 is not excited and $K_1 = 1$ when the coil is excited. From Figure 10.44 we see that $K_1 = 1$ if and only if there is a transmission path from node 1 to node 2, so that we may write

$$K_1 = T_{12}$$

and similarly,

$$K_2 = T_{13}.$$

The two networks defining these transmissions are not series/parallel networks, so that the previous technique of writing transmission functions is not applicable. Even so, we may write the transmission functions by taking the Boolean sum of <u>all</u> possible paths through the network. A moments reflection will show that this method does indeed yield the correct transmission, since if all switches in a given path are closed, then the corresponding Boolean term will be one and the transmission will be one, and if at least one switch in <u>every</u> path is open, then the transmission will be zero since every term in the written sum will be zero.

At time t, we shall denote the positions of the switches in the network, including relay contacts, by A(t), B(t), $C_1(t)$ and $C_2(t)$. These variables are, of course, still Boolean variables and their complements $\bar{A}(t)$, $\bar{B}(t)$, etc. are defined in the usual manner. With this notation, we may then write the state of the coil K_1 at time t as

$$K_1(t) = A(t)C_1(t)B(t) + \bar{A}(t)C_1(t)\bar{C}_2(t)\bar{B}(t) + A(t)C_2(t)\bar{B}(t)$$

$$+ \bar{A}(t)C_1(t)\bar{C}_2(t)C_2(t)C_1(t)B(t).$$

Note that the last term in this expression contains the product $\bar{C}_2 C_2$, which is <u>always</u> zero, so that this term may be dropped from the sum. In the network, this says that there is no transmission between the two sides C_2 and $\bar{C}_2$ of the switch, as we saw previously from Eqn. 10.103 and Figure 10.42. Using this fact, we may write $K_1(t)$ and $K_2(t)$ as

$$K_1(t) = A(t)C_1(t)B(t) + \bar{A}(t)C_1(t)\bar{C}_2(t)\bar{B}(t) + A(t)C_2(t)\bar{B}(t)$$

$$K_2(t) = A(t)B(t)\bar{C}_2(t) + A(t)\bar{C}_1(t)C_2(t) + \bar{A}(t)C_1(t)C_2(t)$$

$$+ \bar{A}(t)\bar{B}(t). \qquad (10.104)$$

The positions of the relay contacts are determined by the coil excitations, so that the contact positions on the right sides of Eqn. 10.104 are, in fact, functions of the terms on the left sides. Here is where the time element becomes important in our considerations. Let us assume that at a certain time t, we have $K_1(t) = 1$ and $C_1(t) = 0$. (We do not worry about how C_1 happens to be open at this time, we just assume this state.) With $K_1(t) = 1$, we have coil K_1 excited which will then close the C_1 contacts. In any relay system (or physical system), there will be some finite delay before the C_1 contacts close due to the influence of the coil. If we assume that the relay has an operate time δ, then we may state that the contact position is given by the coil excitation state with a delay δ. Thus, we have

$$C_1(t + \delta) = K_1(t)$$

$$C_2(t + \delta) = K_2(t) \qquad (10.105)$$

assuming the parameter δ is appropriate to both relays.

Let us assume that $A(t) = 0$ (always in the $\bar{A}$ position), $B(t) = 1$ (always in the B position) and that $C_1 = C_2 = 1$ at $t = 0$. With these

values, we have the coil excitations from Eqn. 10.104 given by

$$K_1(t) = 0,$$

$$K_2(t) = C_1(t)C_2(t), \tag{10.106}$$

or

$$K_1(0) = 0,$$

$$K_2(0) = 1. \tag{10.107}$$

From Eqns. 10.105 and 10.107 we see that the C_2 contacts remain unchanged and that after a time δ, the C_1 contacts change state, so that

$$C_1(\delta) = 0,$$

$$C_2(\delta) = 1. \tag{10.108}$$

Now, from Eqns. 10.106 and 10.108, we obtain

$$K_1(\delta) = 0,$$

$$K_2(\delta) = 0. \tag{10.109}$$

The excitation to K_2 is removed and from Eqn. 10.105, we have that

$$C_1(2\delta) = 0,$$

$$C_2(2\delta) = 0. \tag{10.110}$$

Let us consider what has happened. From the state at $t = 0$ (which we may assume was constrained until $t = 0$ by some unseen demon) relay contacts C_1 opened after a delay δ removing the drive from coil K_2.

After another operate delay δ, the C_2 contacts then opened. Eqns. 10.105, 10.106 and 10.110 will show that both C_1 and C_2 remain open with no further relay operations (as long as A and B do not change).

If at some later time the inputs A and B assume different states, the reduced expressions for $K_1(t)$ and $K_2(t)$ may be found from Eqn. 10.104 and the resulting sequencing calculated. This procedure may be followed for any input time history of (A, B).

We observe from the above discussion that the contact states at a time $t + \delta$ are uniquely determined by the coil excitations at time t, which themselves are uniquely determined by the input and contact states at time t. Knowing the latter, we may then determine the contact states at time $t + \delta$. In the present example, we may eliminate K_1 and K_2 from direct consideration by combining Eqns. 10.104 and 10.105 to obtain

$$C_1(t + \delta) = A(t)B(t)C_1(t) + \overline{A}(t)\overline{B}(t)C_1(t)\overline{C}_2(t) + A(t)\overline{B}(t)C_2(t)$$

$$C_2(t + \delta) = A(t)B(t)\overline{C}_2(t) + A(t)\overline{C}_1(t)C_2(t)$$

$$+ \overline{A}(t)C_1(t)C_2(t) + \overline{A}(t)B(t). \qquad (10.111)$$

If we think of a space with each possible combination of values for A, B, C_1 and C_2 represented by a distinct point representing that state, then the state at time t, corresponding to some point in this space, will define the state at time $t + \delta$, also corresponding to some point in the space. Thus, for any initial state, we may pictorially represent the time sequencing of the network by indicating for every state the state which is assumed in the next time interval. This is easily done by an arrow from a state to the next state assumed. Such a picture for the above example is shown in Figure 10.45. We associate a time δ with each arrow since this is the time assumed for each transition of relay contacts. Note that we draw a relay state diagram for each AB state. The arrows show transitions only in a horizontal direction, which we expect since a change in the relay states cannot affect the states of A and B. We shall also assume that a change in the AB state is much faster than the relay operate time, so that any

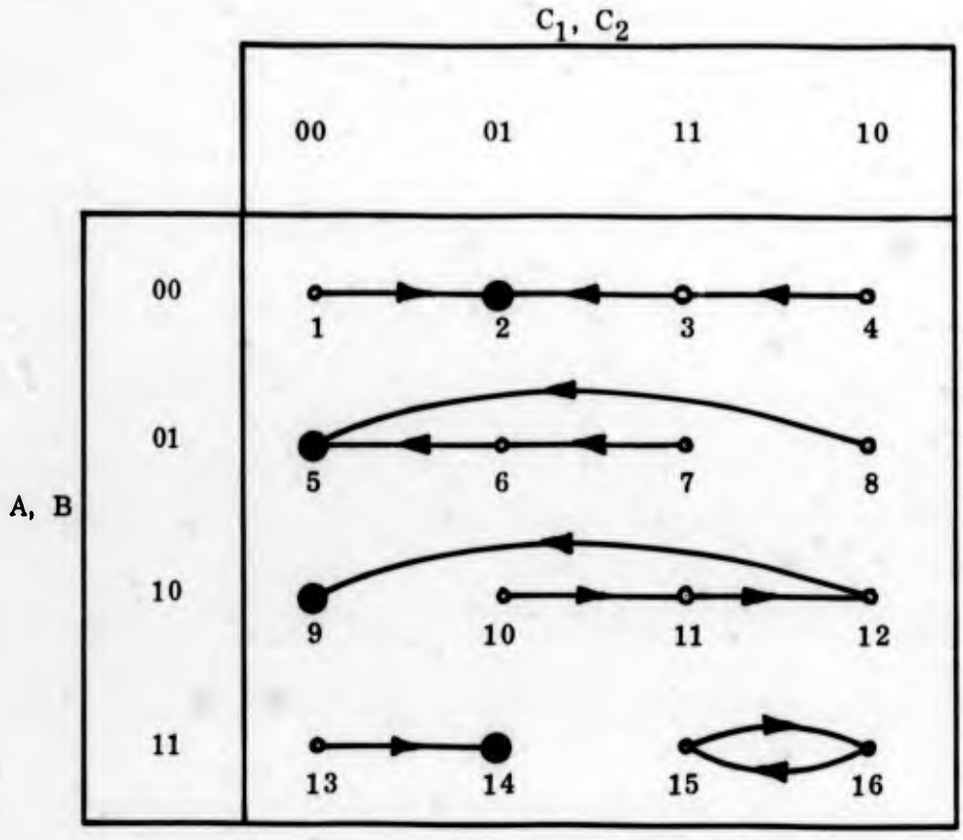

FIGURE 10.45

STATE CHART FOR NETWORK IN FIGURE 10.44

such change will correspond solely to a vertical motion in the state table, with any subsequent horizontal motions (corresponding to relay operations only) occurring later.

There are a number of important features which may be obtained from such a map. First, the state transitions due to any input time functions A and B can be written down immediately from the graph. Second, the state diagram shows all possible transitions and states and not just those corresponding to normal operation. Undesirable operating modes, which may not occur during normal operation, will show immediately on such a diagram. Stable states, in which the system will remain indefinitely as long as the inputs remain fixed, also show immediately from the state graph.

We shall use the state graph in Figure 10.45 and follow the transitions calculated above. We had assumed that $A(t) = 0$, $B(t) = 1$, $C_1(0) = C_2(0) = 1$. This corresponds to the state denoted by point 7. We see that this state is not stable, and that the network assumes the state 6 [C_1, C_2 = 01] after a time δ, corresponding to the C_1 contacts opening. This state is not stable either and the network assumes the state 5 [C_1, C_2 = 00] after another operate time, during which the C_2 contacts open. We see that this state is stable and the network will remain in this state until the inputs A and B change.

Let us suppose that now A changes to 1. This means an input state change during which time the contact state remains the same. Since the network was at the state point 5, the change in A causes the network to assume the state 13. This is an unstable state and the network changes to the state 14, which is stable. Now, let us suppose that the physical system represented by this state diagram is dropped, causing the C_1 contacts to temporarily close. (This essentially can be modeled by the input state and a set of initial conditions on C_1 and C_2.) If C_1 closes, then the network is forced to the state 15 from the state 14. This state is unstable and the network goes to state 16, corresponding to C_2 opening. However, this state is also unstable, and we see that C_2 closes and the network again assumes the state 15. Thus, we see that the system oscillates between states 15 and 16, corresponding to

C_2 "chattering". Clearly, this is an undesirable occurrence. Furthermore, it is one which would not be evident by following the "normal" operation of the system, but is readily evident in the closed-loop present in the state diagram.

The same trouble could be encountered in another manner. Assume the system is in state 14 and that B is momentarily opened (perhaps due to some intermittent connection). The network state will jump to state 10 and then proceed through states 11 and 12 toward state 9. If B closes while the network is in either of the states 11 or 12, then the network will be trapped in the oscillation between states 15 and 16.

This example should be sufficient to point out some of the hazards which may be encountered in sequential circuits which would not cause any problems in combinatorial circuits. Of course, the results obtained from the models of either type of circuit will depend on the accuracy of the models. In combinatorial circuits this is not usually a problem. In sequential circuits, however, the timing and sequencing of contacts is extremely important and can often be poorly modeled. One point which should be considered (which was not done here for simplicity) is the choice of a proper model to use for a contact, i.e., make-before-break or break-before-make. Also, the operate and release times of a relay may be different and also distinct from those of other relays. Such limitations might have us place certain constraints on the types of transitions that we allow in the state table. For instance, we may require that any single transition between states involve a change in only one variable. It is these kinds of limitations and constraints which make sequential analysis more complex than combinatorial analysis and far more challenging.

11. COMPUTER AIDED DESIGN AND APPLICATION

In designing or evaluating any system, it is essential to be sure the values of the many parameters involved are chosen so the system will perform as desired over the range of operating conditions and manufacturing tolerances expected. There appear to be two ways this determination can be made. One is to build the proposed system and perform sufficient tests until it can be assured of operating as desired. The other way is to construct a mathematical model which accurately predicts the behavior of the system and perform sufficient analysis of the model to insure proper operation. In instances where system limitations are to be studied, the model must accurately reflect the non-ideal nature of many of the system components. Both techniques offer advantages, and any serious attempt to evaluate a complex system will use a mixture of both analysis and testing. The decision when to apply which method is a matter of engineering judgement. Mathematical analysis must be coordinated with experimental measurements to verify its validity. The success of analysis is absolutely dependent on the accuracy with which the models chosen predict behavior.

Computational difficulty usually increases rapidly with increasing model complexity. Very often adequate results about one aspect of system performance may be obtained from an appropriately simplified model, with different models being used for different aspects of performance. The model used need only reflect accurately the phenomenon or parameters being investigated. Use of such an ad hoc model can often yield excellent results with huge savings in computational effort. The selection of an analytical model for a system or subsystem is thus an important step, and one to which considerable forethought should be given.

Computer-aided design and evaluation of power processing systems involves the bringing together of three key factors.

1) The models of the system's internal circuitry and its interaction with source and load, and also models of its response to the various environmental factors which affects its operation, such as heat, humidity, shock and vibration. Many of

the device and subsystem models will be constructed out of consideration of the fundamental physical principles involved, and others will be constructed on the basis of experimental evidence obtained from the device or subsystem. An example of the former process is the hybrid - π model of the bipolar transistor, while its h or y parameter representation is an example of the latter technique.

2) A collection of algorithms, for automating the solution process for the problems represented by the models.

These algorithms are the sets of rules in which the mathematical methods used to solve the problems are embodied. An example of such an algorithm is the Runge-Kutta method of solving ordinary differential equations. The algorithms are coded into the computer programs for solving the models.

3) The system program. This program allows the analyst to have free and rapid access to the algorithms, and allows him to enter the parameters of the problem and obtain the results of the analysis in a manner and language familiar to him.

11.1 MATHEMATICAL REQUIREMENTS

All of the models which are developed to analyze the power processing system can be classified into a relatively small number of types according to their mathematical structure, and to some extent the physical nature of the phenomena they model. The largest class of models encountered in power processors is lumped parameter networks. Included in the class of lumped parameter networks are ordinary electrical circuits and many kinds of mechanical, acoustical and thermal systems. These systems are represented by ordinary differential equations. Lumped parameter networks are of two kinds, linear and nonlinear. This distinction is made because of the differences in analytical techniques often employed in treating the two kinds. General nonlinear techniques, which are essentially special techniques for linearizing nonlinear equations, work

for solving linear networks, but not conversely. There is a subclass of lumped parameter network models that is very important in power processing system analysis. This subclass consists of network elements which themselves are n-port networks which are completely characterized by their terminal characteristics. Such a generalization of the lumped parameter network is important to perform analysis on a system block diagram level.

The other large class of models are those governed by partial differential equations. These are representative of distributed systems, such as generally encountered in heat transfer mechanisms, certain electromechanical interactions (as induction machines), most acoustic phenomena, and most phenomena involving elasticity, wave propagation and vibrations in continuous media. The most critical application of these models in power processing systems will be to the thermal analysis.

The third type of model is a Boolean model of the binary type logic functions applicable to problems of the switching and control functions of some power processing systems.

Probabilistic models arise in reliability studies of the equipment.

Recently, there has been a great deal of development of computer programs for analyzing lumped parameter networks. These differ widely in the complexity of problems they can solve. There are two basic kinds of programs. The most general kind solves the problem in the time domain usually using the state variable approach. These programs are usually adapted to nonlinear networks by changing the parameter at each of the computational time increments according to the particular nonlinear constituient relationship involved, treating the problem as a linear one at each time increment. The other basic type of program performs a frequency domain analysis of linear, time invariant systems.

The network solving programs are divided into two parts. The first part generates the differential equations (or the Laplace transforms of the equations, in the case of frequency domain analysis)

from the network topology and the branch constituient relations. The other part is the algorithm for solving the differential equations.

The kinds of distributed parameter problems encountered in power processing system analysis are fairly limited to those of the following forms:

Diffusion and heat transfer: $$\alpha^2 \nabla^2 \phi = \frac{\partial \phi}{\partial t}$$

Wave propagation and dispersion: $$\frac{\partial^2 \phi}{\partial t^2} = V^2 \nabla^2 \phi + \xi(\bar{x}, t)$$

These are classical equations in physics and engineering, and techniques for solving them on a computer have been studied extensively.

Much effort has been expended toward automating logic design and analysis, and some of that work is quite applicable to analyzing the binary control sections of power processing systems. Breuer has compiled an extensive bibliography on the subject.*

11.2 INPUT - OUTPUT REQUIREMENTS

As a practical matter, the system programs and input-output techniques developed for this kind of analysis are an integral part of the program which implements the particular mathematical method adopted (e.g., state variable analysis in the time domain). The distinction is made between the two programming levels, input-output control programs and equation solving programs, because they are fundamentally separable. Decisions as to how each level is mechanized in practice are based on quite different considerations. Nevertheless, the close interaction required between the two levels compels them to be integrated in any actual computing system.

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* Bibliography I, Reference 123.

The sophistication of the control program depends largely on the extent to which the evaluation process is to be automated. At the simplest level of the automation process, we have the engineer using the computer as a calculating machine. The engineer decides what is to be evaluated and chooses the way to decompose and model the system, then picks an appropriate analysis program and puts it on the computer, which performs the calculations for him. A catalog would be provided containing lists of performance specifications to be evaluated, modeling techniques and procedures and analysis programs available. The control portion of the computer-aided evaluation program would then consist of the above mentioned catalog and user instructions for the analysis programs.

The minimum level of input-output sophistication for the analysis programs should be such that all information required to run the analysis program except the specification of the model and its parameters be generated by the control portion of the program. This would include provisions internal to the program for determining a computational time increment, for example. The user should have only to concern himself with the details of the problem statement and model, not with the exigencies of the computing process.

The engineer would still be faced with the task of interpreting the results of the analysis and of assaying the system as being of good design or not.

In evaluating a power processing system, it is desirable to compute various performance indices. Examples are line and load regulation, ripple, efficiency, transistor junction temperature versus ambient temperature, load and input voltage, component operation within specifications, probability of second breakdown under various operating conditions, losses in magnetic structures, mean time before failure, and the sensitivity of these factors to changes in component values. The next step in the control program's sophistication might be to plan it to output these indices directly after being given only the relevant model parameters. The control program could, for example, in calculating transistor junction temperature rise under worst case conditions, call for the relevant algorithm to analyze both the thermal model and the electrical model (which interact), taking the necessary results from each analysis and outputting only the desired temperature rise.

The capacity for such operation would require the control program to be able to call upon a number of analysis programs and provide them with the required data, and must be able to handle the interaction between various programs, such as electrical and thermal analysis.

The highest level of automation would have the operator feed information contained on block diagrams and schematic diagrams along with component values, characteristics and limitations, and structural data to the control program. This program would then perform the task of completing the modeling and deciding on the computational program appropriate for each stage of the analysis and putting it into operation.

Such a control program must be able to identify a model by the type of mathematical method used to solve it. It must be able to handle a block diagram type analysis, and it must be able to accept input and produce output in engineering terms. The computer must be able to call for specific experiments on a system prototype to aid the analysis or verify the results.

11.3 SURVEY OF COMPUTER AIDED DESIGN PROGRAMS

At this point, a survey of work on computer-aided design is appropriate. Most of the efforts applicable to power processing systems have dealt with lumped parameter networks. The researchers have proceeded by taking an analysis technique which is suitable for computer analysis and powerful enough to handle the desired class of networks and outfitting it with a control program and input-output devices which meet their requirements.

NET-1 was developed by A. F. Malmberg, et al., at the Los Alamos Scientific Laboratory of the University of California (1964). It is a network analysis program which does both dc steady state and transient analysis of networks containing linear time invariant resistors (up to 400), capacitors (400), and inductors(400), including mutual coupling, and also containing junction diodes (40) and junction transistors (40), signal sources (63), and fixed voltage sources (63). This program can determine the effect of varying circuit parameters.

Parameters of transistors and diodes are stored in an internal library by device JEDEC type number. Transistors and diodes are the only nonlinear devices admitted by NET-1. This program operates in a batch mode only and uses a time domain method of analysis. Output is in tabular form. There is an advanced version of NET, NET-2, which has all of the features of NET-1 and, in addition, can perform variational analyses and Monte Carlo analysis and has provision for graphical output.

ECAP is an Electronic Circuit Analysis Program written by G. R. Hogsett of I. B. M. Corporation (1965) and exists in versions for the I. B. M. 1620 and SYSTEM/360. It is a collection of three programs to perform dc analysis, ac analysis and transient analysis. The dc analysis program admits linear resistors, fixed independent voltage and current sources, and dependent current sources. The ac analysis is performed in the frequency domain and admits linear time invariant R, L, C's, mutual inductances, independent sinusoidal sources and dependent current sources. The transient analysis program admits linear R, L, C's (no mutual inductances), fixed or time varying independent sources, dependent current sources and switches. Nonlinearities are treated in the transient analysis program by switching branch parameter values as functions of branch voltage or current. The 1620 version can handle 20 nodes and 60 branches. The SYSTEM/360 version can handle up to 50 nodes and 200 branches. Output is in tabular form.

More recent work in this area has produced some outstanding results. On-line circuit design, a technique which uses time sharing computers, allowing the engineer to interact with the computer continuously as if he were the only user. Significant progress has been made, resulting in programs such as AEDNET and CIRCAL, both developed at M. I. T. AEDNET simulates networks whose elements are nonlinear, time-varying resistors; capacitors; inductors; and dependent and independent sources. The nonlinearities may be specified either by a table or by an analytical expression. The input-output is through either a teletypewriter console or oscilloscope display. Using the oscilloscope display data about planar networks is entered as a schematic diagram drawn on the oscilloscope face with a light pen. The output is either tabular, or as graphs of voltage or current versus time, or one variable versus another. AEDNET has the capacity to nest networks. That is, a network may be specified and then later, imbedded

in a larger network. In this way, equivalent circuits of devices may be entered and identified and used as elements of other circuits without having to redraw the model each time the device (e.g., a transistor) is used. The program permits study of parameter variations. CIRCAL retains all of the features of AEDNET and, in addition, has been refined by adding several features and expanding the class of networks it can solve. Most particularly, from the point of view of power processing system analysis, the latest version of CIRCAL admits network with other dynamical elements than inductors and capacitors and, also, has provisions for block diagram analysis.

11.4 REQUIRED DEVELOPMENTS IN COMPUTER AIDED DESIGN PROGRAMS

This list of computer-aided design programs is representative of the few hundred batch programs and the few time sharing systems now available, using more than thirty methods of solution. It is found from a study of these programs that most of the analytical techniques necessary to analyze power processing systems are already embodied in various computer programs. To make computer-aided evaluation of power processing systems practical, the size of networks that general purpose systems such as CIRCAL (CIRCAL is presently limited to networks with 20 nodes and 50 branches) can handle must be increased. Capability for general block diagram analysis must be expanded. The need for an on-line time sharing system is seen to vary inversely with the degree of automation employed. The more human supervision and intervention is required in the evaluation process, the more essential is the fast man-machine interaction afforded by on-line facilities.

In adapting these computer facilities, more study of the analytical requirements of power processing systems is needed. From this study will come ways of partitioning the system and organizing the analysis so that a supervisory program can be written which will coordinate and direct the process, calling on different analytical techniques as needed. Usable models which account for the non-ideal behavior of devices and materials used in power processing systems must be obtained. Ways of predicting reliability, making maximum use of both theoretical and experimental evidence, must be developed and worked into the program.

Once developed, the computer-aided design analysis of power processing systems can be adapted to other types of equipment with a resultant increase in quality of equipment in the field.

12. ANALYSIS OF A TYPICAL POWER PROCESSOR

In the previous chapters, we have described a procedure whereby power systems may be successively partitioned into smaller sections until blocks at the circuit level are reached. In this chapter, we shall apply this procedure and some of the analysis techniques previously described to an analysis of a specific power processor. We should note that we are attempting only an analysis and not an evaluation. An evaluation must include a comparison of actual behavior with desired behavior together with some value judgements based on appropriate criteria. However, an understanding of the operation of a system is essential if an evaluation must be made. The following pages will describe only the operation of a specific power processor.

The unit we shall consider here is the U. S. Army PP4125 ( )/U battery charger, which is shown in Figure 12.1. The charger is designed to work from a nominal 28 vdc prime source and to charge 6 volt and 12 volt batteries at a preselected current in one of three charging modes.

The first step in the analysis of this power processor is to identify the basic power converter(s) and the auxiliary circuitry. Referring to the schematic in Figure 12.2, we see that the circuitry on the extreme bottom and left of the schematic in some manner serves to ultimately control the relay K4. This relay in turn controls the connection of the circuitry in the upper right part of Figure 12.2 to the prime power input and the device output. This latter portion of the circuit is that part which performs the actual power conversion of the unit and is, therefore, a basic power converter of the PP4125. The remaining circuitry serves solely to connect (via K4) the basic power converter between the source and load at certain times and this can be classified as auxiliary circuitry. This partitioning is illustrated in Figure 12.3.

Each of these sections may be further divided into distinct, functional blocks. Such a division into separate circuit blocks is shown in Figure 12.4. Each section shown here is seen to be a portion of the entire circuit which may be analyzed independently of the

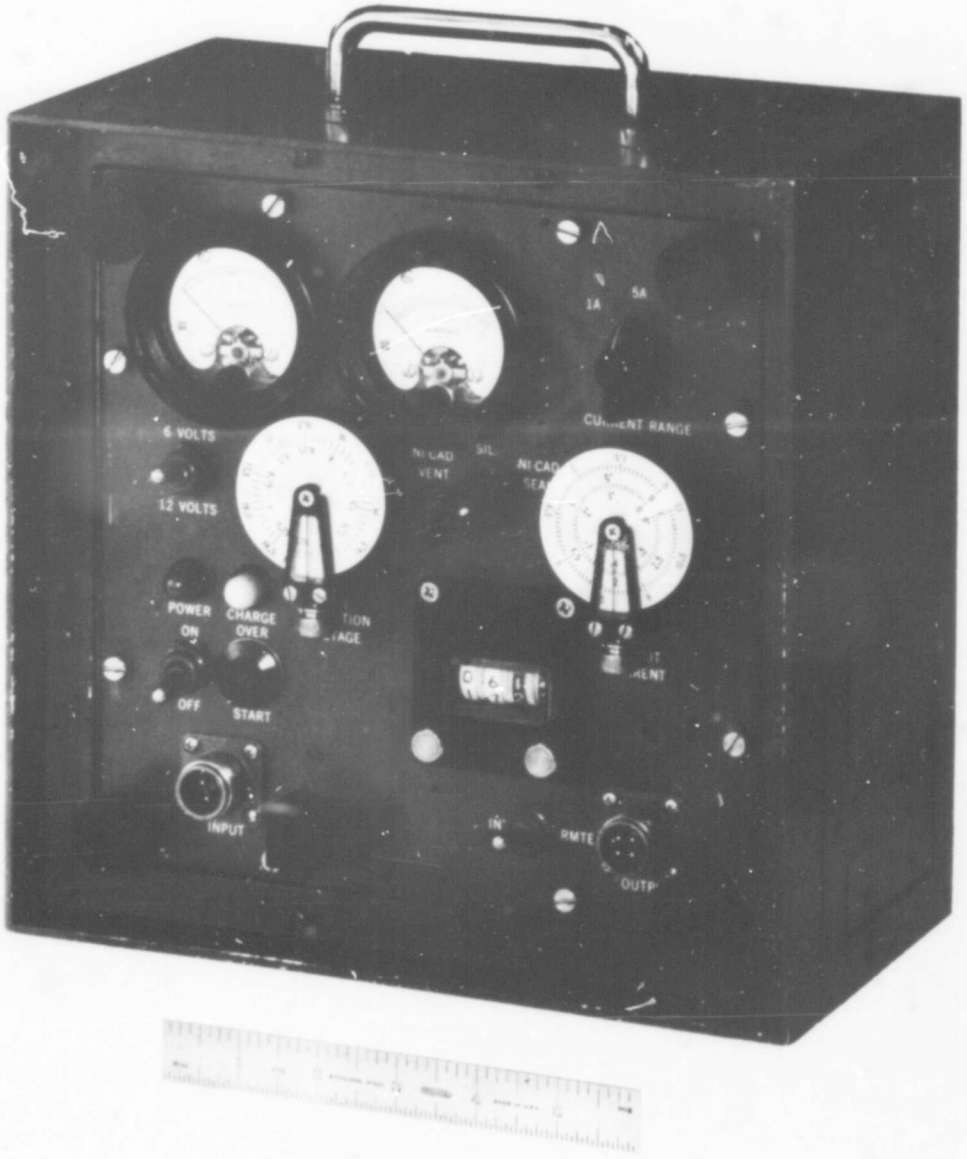


FIGURE 12.1

U. S. ARMY PP4125 ( )/U BATTERY CHARGER

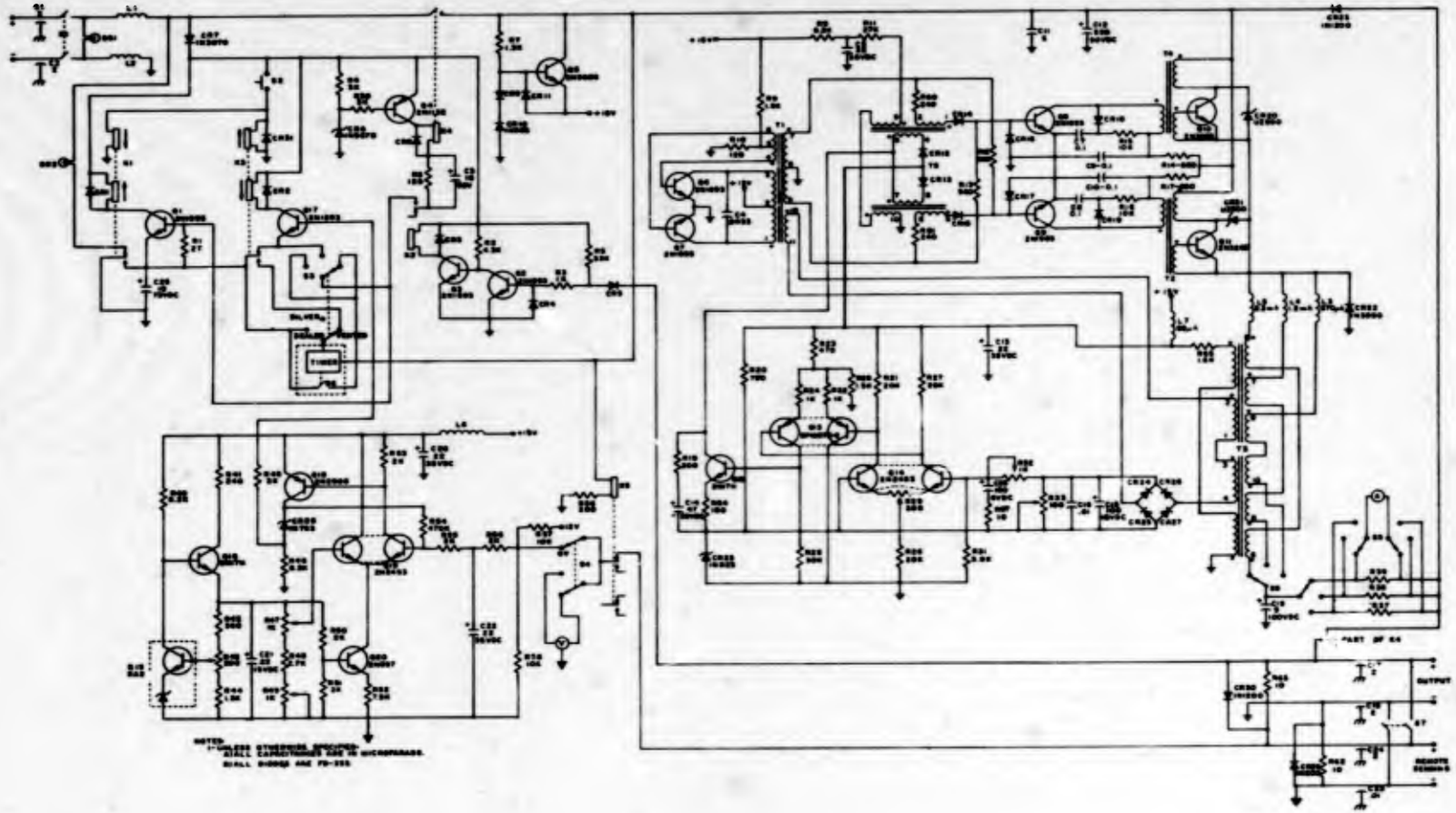


FIGURE 12. 2

SCHEMATIC OF PP4125 ( )/U BATTERY CHARGER

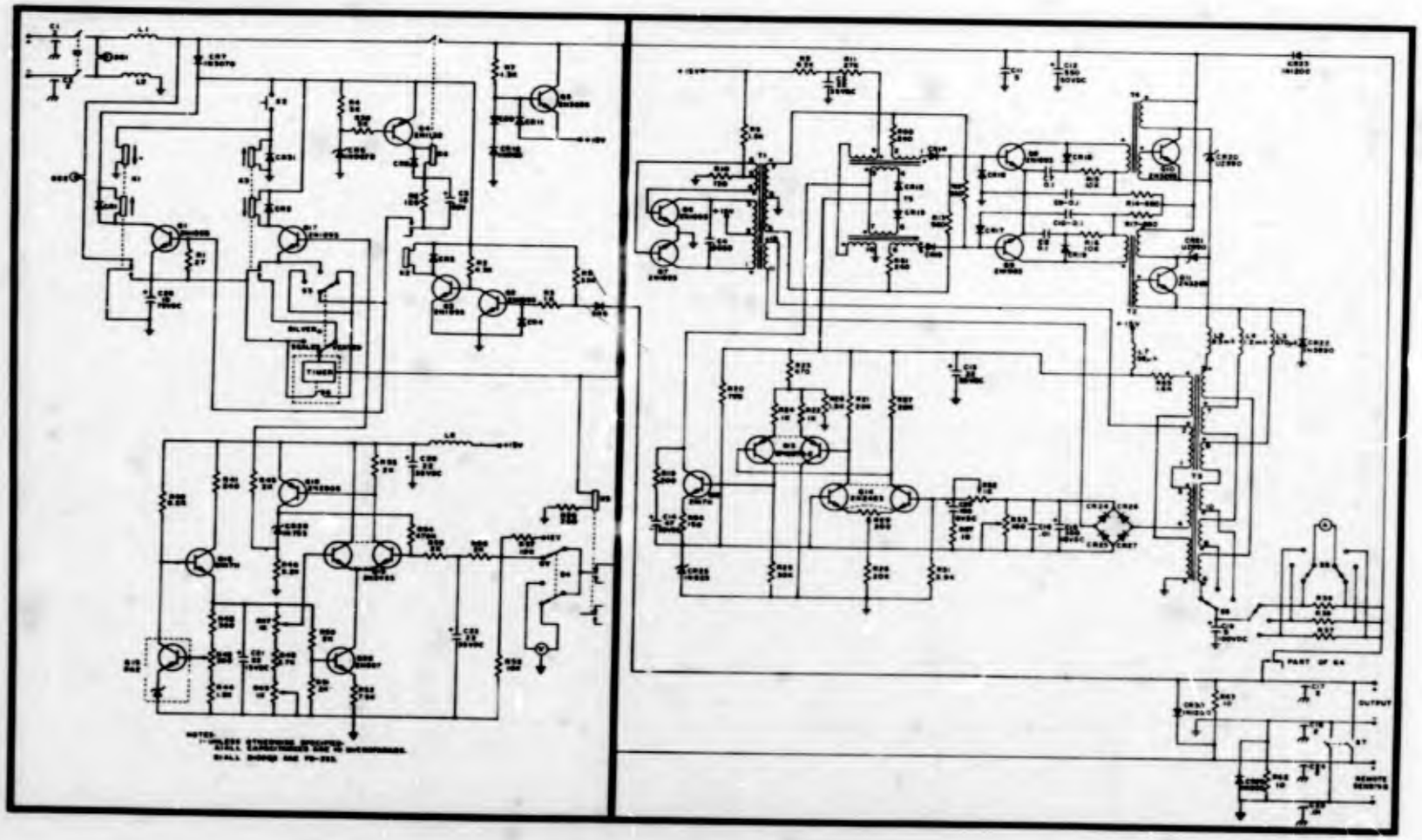


FIGURE 12.3

SCHEMATIC SHOWING BASIC POWER CONVERTER AND AUXILIARY CIRCUITRY

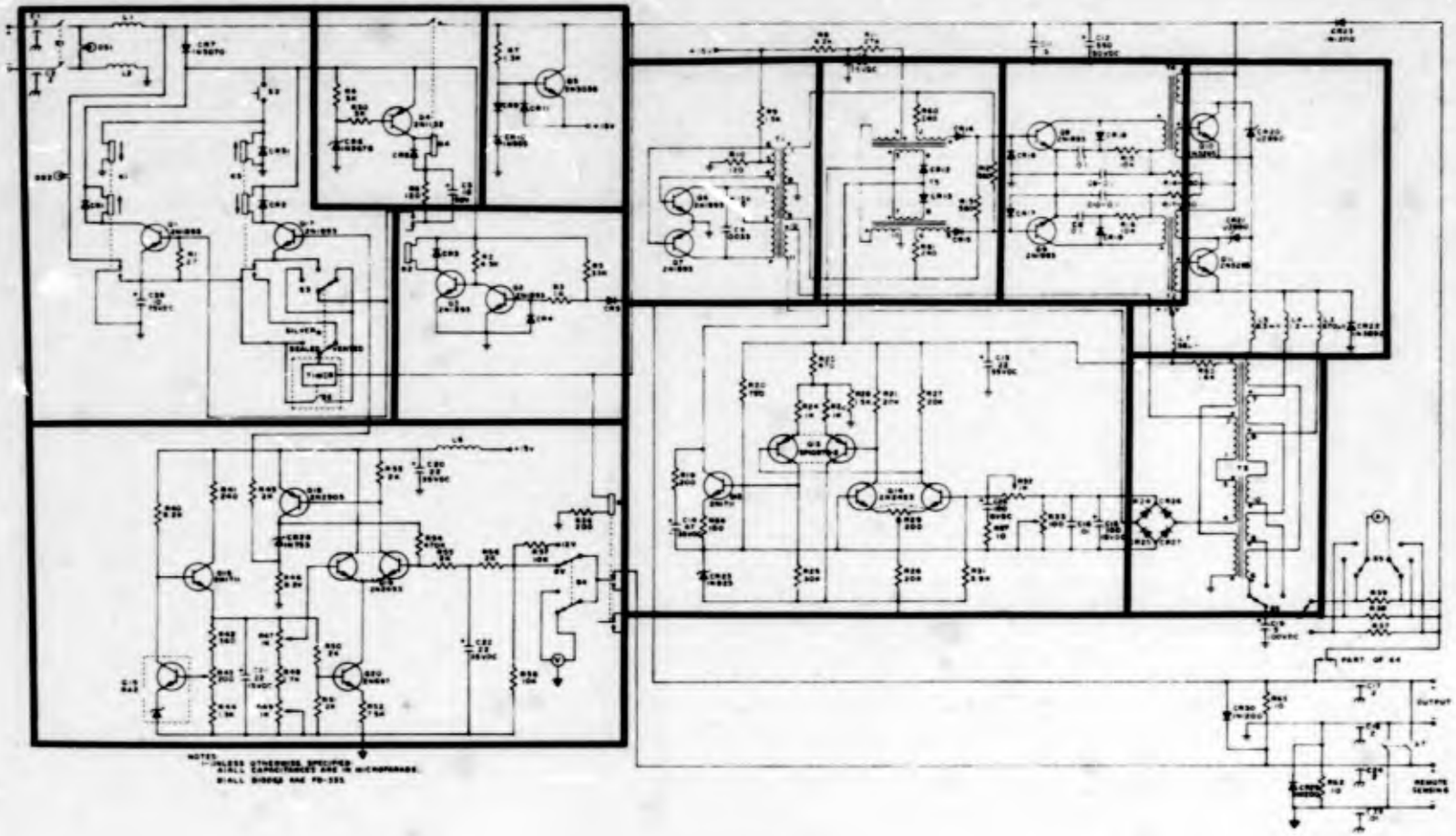


FIGURE 12.4

SCHEMATIC SHOWING CIRCUIT BLOCKS

other sections. These sections are shown here for reference and will be justified later after an appropriate analysis.

The partitioning shown in Figure 12.4 has divided the system into blocks which are simple enough to allow a feasible and meaningful circuit analysis. We shall determine the characteristics of each of these blocks separately and then use these derived characteristics to determine the terminal properties of the entire system. A flow chart illustrating the analysis procedure is shown in Figure 12.5. Note that partitioning is performed at various levels until the circuit level is reached. Analysis techniques are then utilized to determine the properties of the various levels starting at the circuit level and ending at the system level.

The device and component models we shall use in this example will be quite simple and idealized. Some of the models and values used in the following analysis have been deduced from measurements made on the unit since some of the required information was not initially available. Wherever possible, this information is shown in Figure 12.2. In order to simplify our analysis, we shall assume that transistor speed limitations are not important, that they have high beta, and that base emitter voltages may be neglected except as specifically noted in the analysis. The nonlinear magnetic elements will be modeled by ideal square loop B-H characteristics. Although some of these assumptions may not seem realistic, the results obtained by using them are sufficiently accurate to reflect the nature of the circuits in the battery charger and these results are borne out by actual circuit operation. The latter statement is the key to the modeling process since we need only use a model sufficiently realistic to predict device behavior to the desired accuracy.

12.1 AUXILIARY CIRCUITRY

Auxiliary Regulator

Having identified the various circuit blocks, let us proceed with an analysis of the auxiliary circuitry. We shall consider the auxiliary regulator first. This circuit, shown in Figure 12.6, consists of a

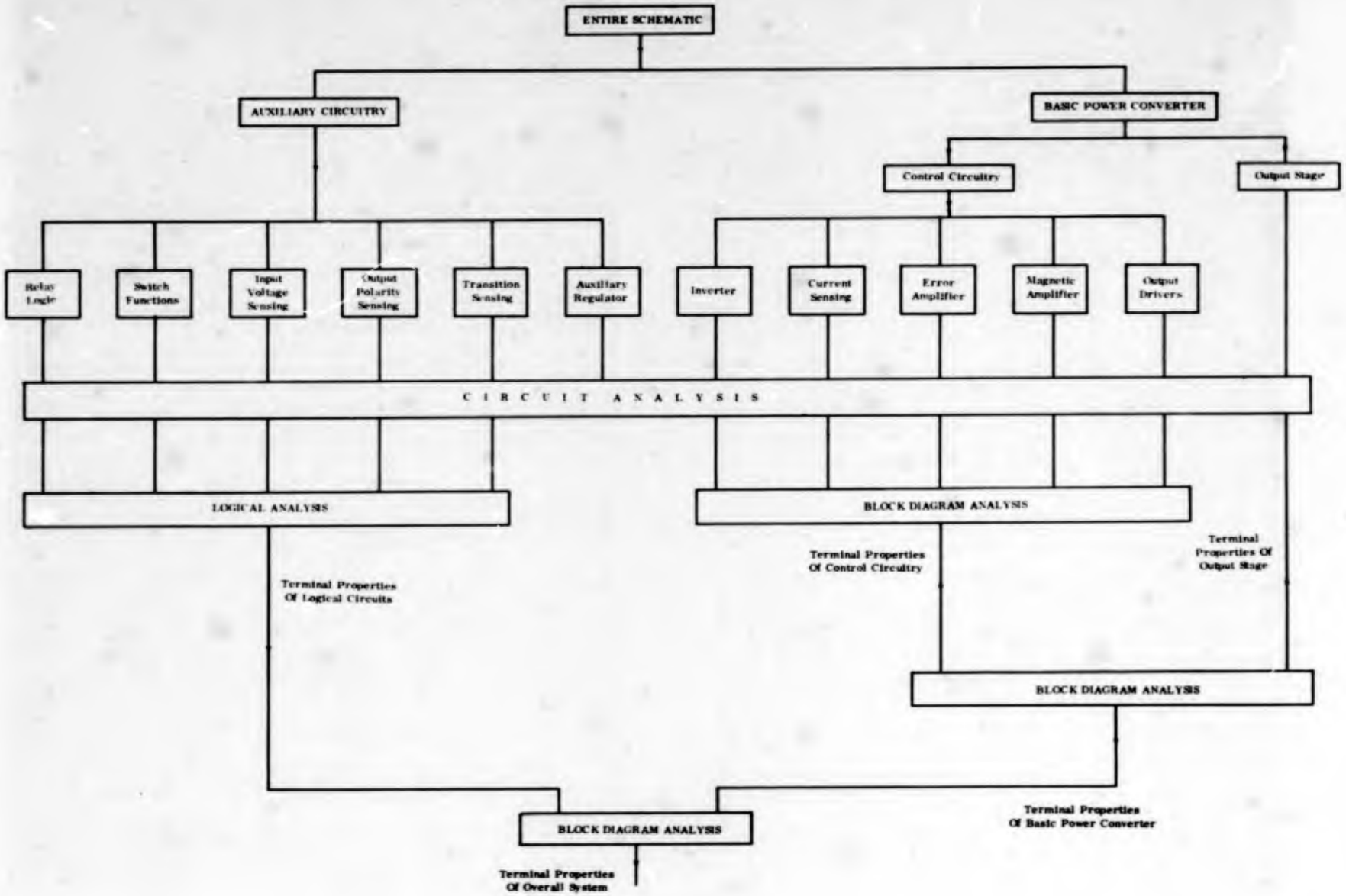


FIGURE 12.5

ANALYSIS FLOW CHART

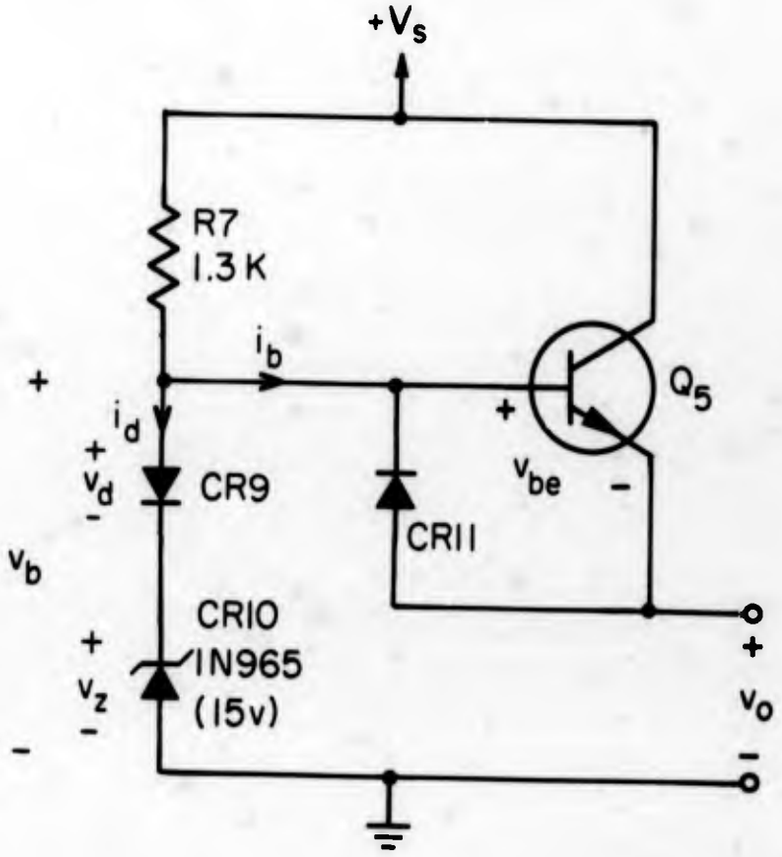


FIGURE 12.6

AUXILIARY REGULATOR

voltage reference and an emitter follower. For the moment we shall assume that the supply V_s is greater than 15 volts, so that the voltage at the base, v_b, is given by

$$v_b = v_z + v_d$$

where v_z is the zener voltage (15 volts nominally) and v_d is the forward drop in diode CR9. The output voltage v_o is given by

$$v_o = v_b - v_{be} = v_z + (v_d - v_{be}) \qquad (12.1)$$

where v_{be} is the base-emitter voltage of Q5. To a first order approximation, $v_d \simeq v_{be}$, so that

$$v_o \simeq v_z \qquad (12.2)$$

From Eqn. 12.1 we see that any change in the quantity $(v_d - v_{be})$ will appear as a change in the output voltage v_o. Assuming essentially constant loading on the auxiliary regulator, changes in v_{be} will be due mainly to temperature variations. The diode voltage v_d may change due to temperature variations or diode current variations. The diode current is given approximately by

$$i_d \simeq \frac{v_s - 15}{1300}$$

The current i_d can change by a factor of 2.4 maximum for the specified input range (22-32 volts). At room temperature, this will produce a maximum diode voltage change of approximately 22 mv. The zener has a nominal impedance at these current levels of approximately 20 ohms. Therefore, a variation in line voltage from 22 to 32 volts will cause a zener voltage change of approximately 200 mv, which is seen to be the dominant error term. Small errors may also be produced by temperature variations between diode CR9 and transistor Q5 due to

their different power dissipations, but any such changes should be in the millivolt region and will be small compared with the zener temperature drift. Accounting for various errors, the auxiliary regulator should provide 15 vdc at approximately 2% regulation for line and temperature variations.

Transition Voltage Sensing

The transition voltage sensing circuit is shown in Figure 12.7. By inspection, we see that it consists of two parts - a voltage reference and a comparator. The entire circuit works from the internally regulated 15 vdc line.

Let us consider the simplified reference amplifier, shown in Figure 12.8, with the feedback removed. Q15 is a reference device with an integral zener diode. The device starts to conduct when the base voltage exceeds 7 volts (nominal). Thus, if v_i is less than 7 volts, Q15 is cut off and $v_o \simeq 15$ volts. As v_i increases past 7 volts, Q15 begins to conduct, producing a drop in the collector voltage and a corresponding decrease in v_o. For simplicity, we shall assume an infinite gain in Q15 which gives the $v_i - v_o$ relation shown in Figure 12.9. The resistive feedback divider places another constraint on v_i and v_o. Again, referring to Figure 12.8, we have the feedback network constraint

$$v_i = av_o, \quad 0.7 \leq a \leq 0.8 \tag{12.3}$$

where a = 0.7 when the wiper of R43 is toward R44 and a = 0.8 when the wiper of R43 is toward R42. This relation is also plotted in Figure 12.9 for the two extreme values of a. When the feedback loop is closed, as it is in the circuit, both of the above constraints must be satisfied. Therefore, the output voltage may be found from the point of intersection of the two plots. As the wiper of R43 is moved, we see that the nominal range of v_o is given by

$$8.75 \leq v_o \leq 10 \text{ volts (set by R43).} \tag{12.4}$$

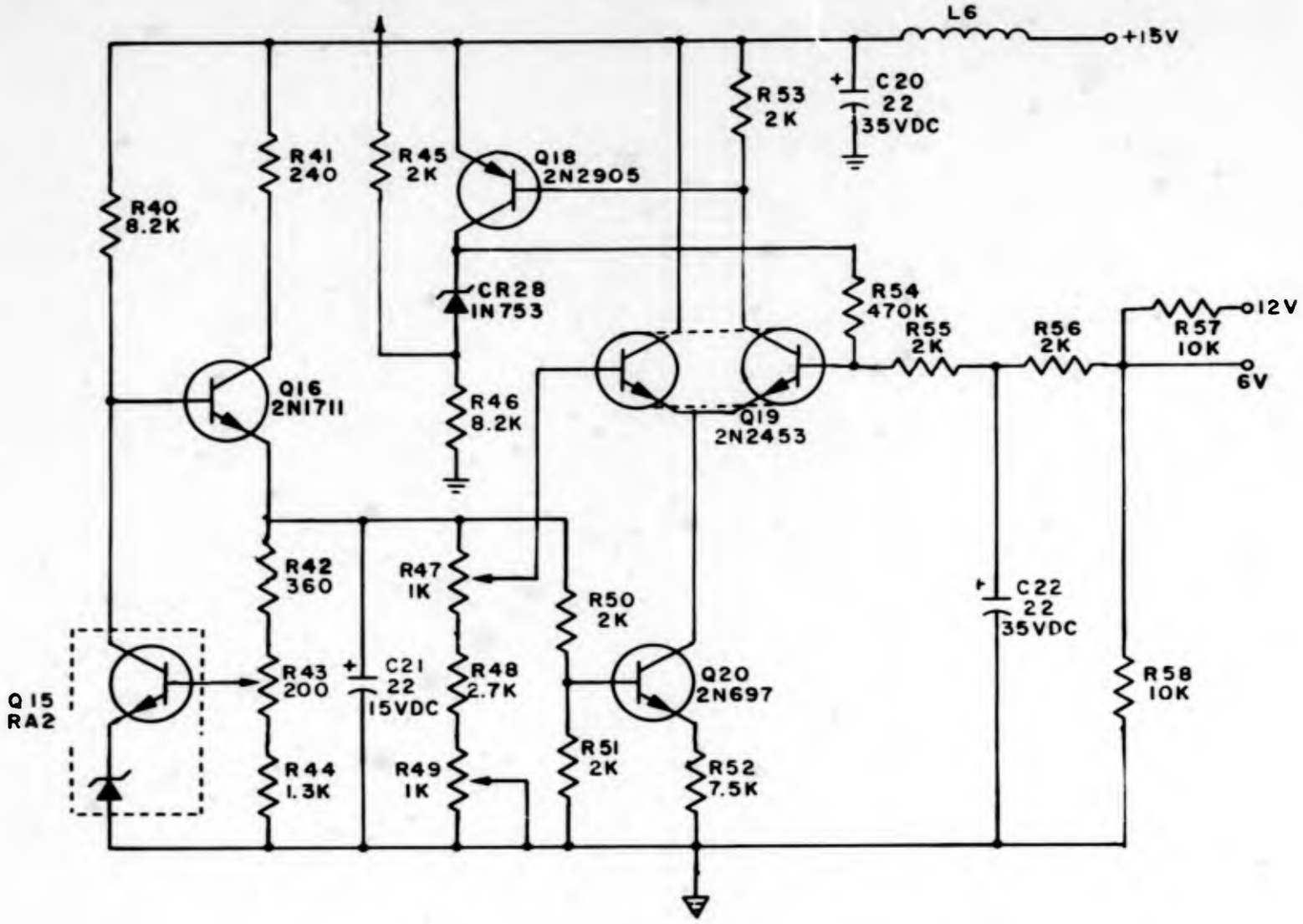


FIGURE 12.7

TRANSITION VOLTAGE SENSING SCHEMATIC

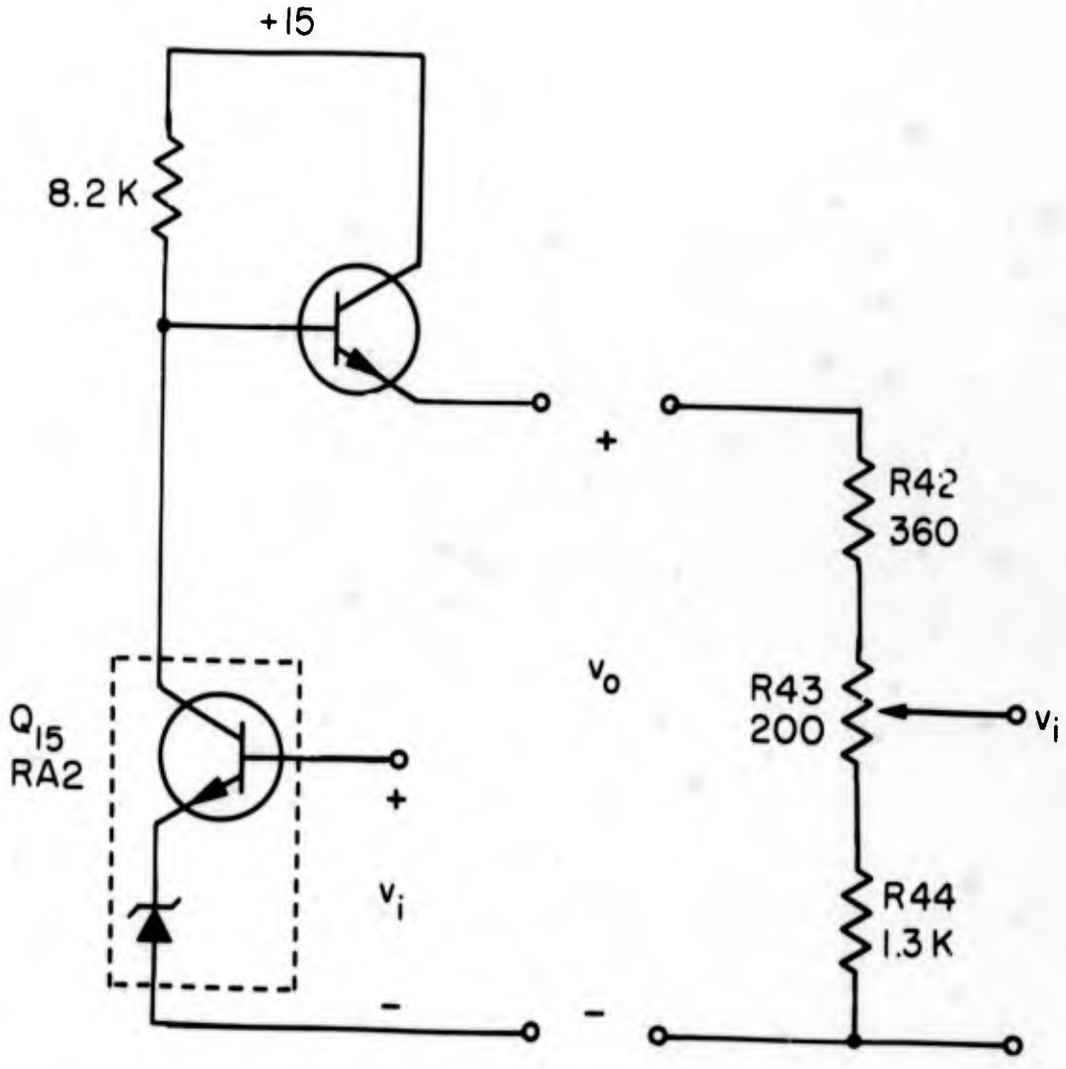


FIGURE 12.8

REFERENCE AMPLIFIER WITH FEEDBACK REMOVED

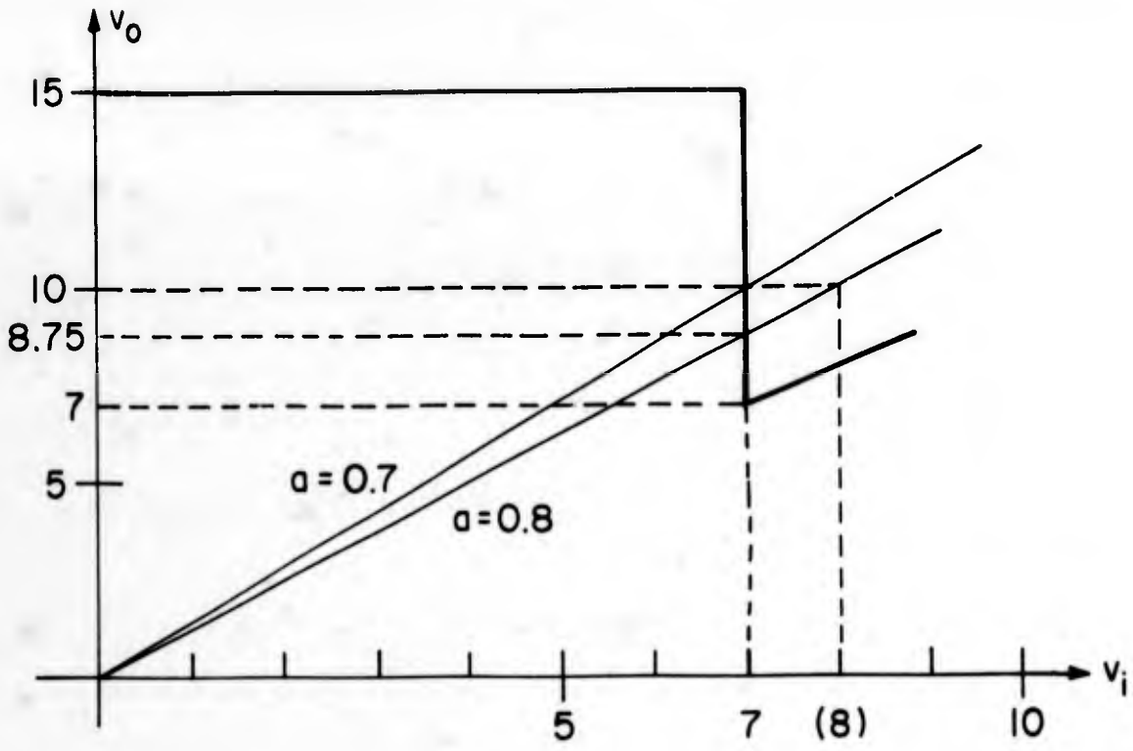


FIGURE 12.9

REFERENCE AMPLIFIER TRANSFER AND FEEDBACK CHARACTERISTICS

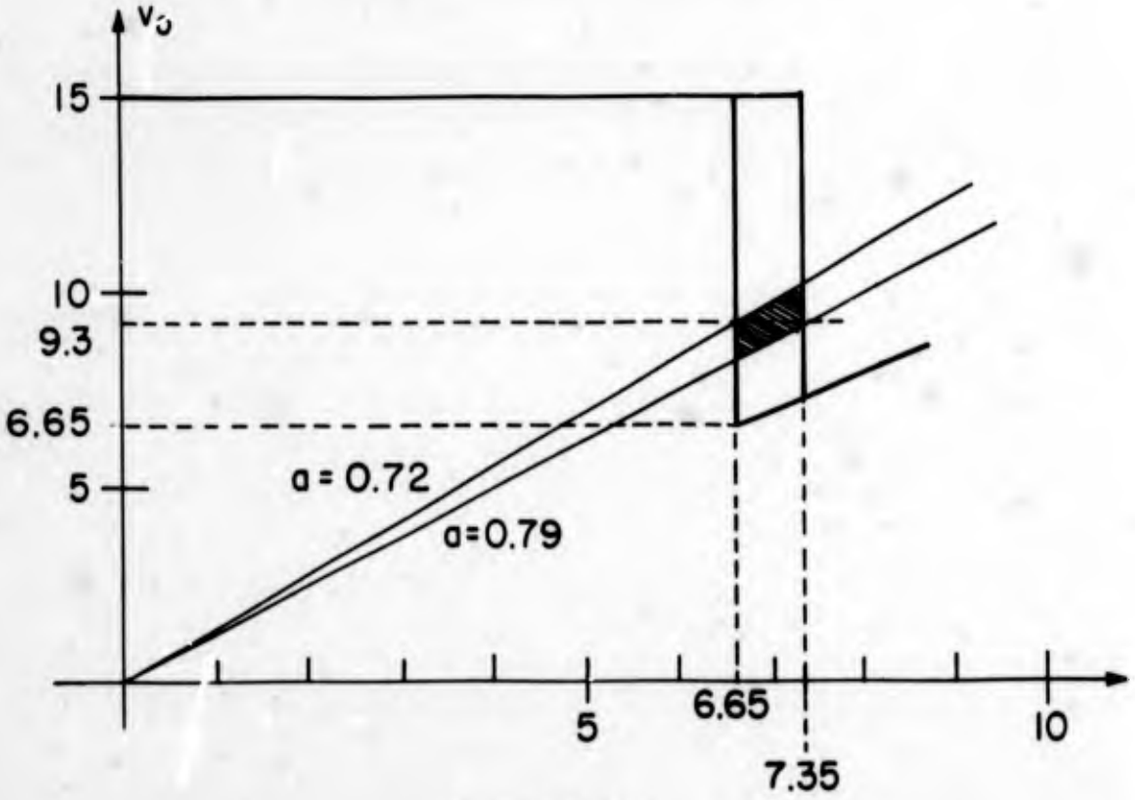


FIGURE 12.10

REFERENCE AMPLIFIER TRANSFER AND FEEDBACK CHARACTERISTICS WITH TOLERANCES

If we account for possible tolerances in the resistive divider (5%) and the reference voltage of Q15 (5%), we find that the coefficient $\underline{a}$ in Eqn. 12.3 can be guaranteed to lie in the range

$$0.72 \leq a \leq 0.79. \tag{12.5}$$

Figure 12.10 shows the possible output voltage range v_o which can be observed when accounting for various component tolerances. We see that the output v_o can always be set to 9.3 volts but that guaranteeing a different value requires tighter component tolerances. Although the probability is quite small that all tolerances will be such to yield this case, the problem may be entirely eliminated by allowing a larger range of adjustment, perhaps by using a 500 ohm pot for R43 instead of the present 200 ohms.

The actual value of the transition voltage is selected by the wiper of R47, a front panel control which forms part of a resistive voltage divider from the regulated output v_o of Q16. As we shall see, the desired voltage range at the wiper of R47 should be from 6.75 volts to 9.25 volts. From Figure 12.7, we see that the maximum value of voltage at this wiper occurs when the wiper is toward the emitter of Q16, and that this voltage will be the regulated reference voltage v_o determined above. Thus, R43 must be set to provide 9.25 volts at the emitter of Q16 and it is with this setting in mind that an increased adjustment range with R43 is desired.

A voltage of 6.75 volts is desired at the wiper of R47 when this wiper is toward R48. This requires

$$\frac{R48 + R49}{R47 + R48 + R49} = \frac{6.75}{9.25} \tag{12.6}$$

which gives

$$R48 + R49 = 2.7k. \tag{12.7}$$

R48 is presently a 2.7k fixed resistor which leaves almost no room for component tolerances. In the device tested here, the 1k ohm trimmer R49 was set to approximately 50 ohms. A value of R48 which is

within tolerance but above the nominal 2.7k ohm value could make it impossible to accurately set the lower threshold. If R48 is lowered to 2.2k ohms, then the 1k ohm trimmer R49 would provide a ± 500 ohms allowance about the nominal 2.7k ohm value and should not present a calibration problem.

Now let us consider the comparator circuit shown as a simplified schematic in Figure 12.11. Using the indicated nomenclature, we see that for $e < V_r$, the right side of Q19 and, hence, Q18 are both cut off. If we also have $e < 6.2$ volts, then the zener diode CR28 will not conduct and we have

$$v_1 = e, \quad e < 6.2 < V_r. \tag{12.8}$$

For $6.2 < e < V_r$, the zener will conduct current and maintain an essentially constant voltage. In this region, we then have

$$v_1 = 6.2 + \frac{2}{472}(e - 6.2)$$

$$= 6.2 + .04\,(e - 6.2), \qquad 6.2 < e < V_r. \tag{12.9}$$

For $e > V_r$, the right side of Q19 will conduct and, assuming a large gain, Q18 will saturate for all $e > V_r$. Thus,

$$v_1 = 15, \quad e = V_r. \tag{12.10}$$

The $e - v_1$ relation described by Eqns. 12.8 and 12.10 is plotted in Figure 12.12. This is the forward transfer constraint on e and v_1.

There is another constraint on e and v_1 dictated by the feedback network consisting of R54, R_a and R_s. When the voltage range selector switch (S4) is in the 6 volt position, the charger sensing line is connected to the junction of R57 and R58, yielding $R_s = 0$ and $v_s = v_b$, where v_b is the voltage to be sensed. For this case, we may write

$$e = \frac{470}{474} v_b + \frac{4}{474} v_1. \tag{12.11}$$

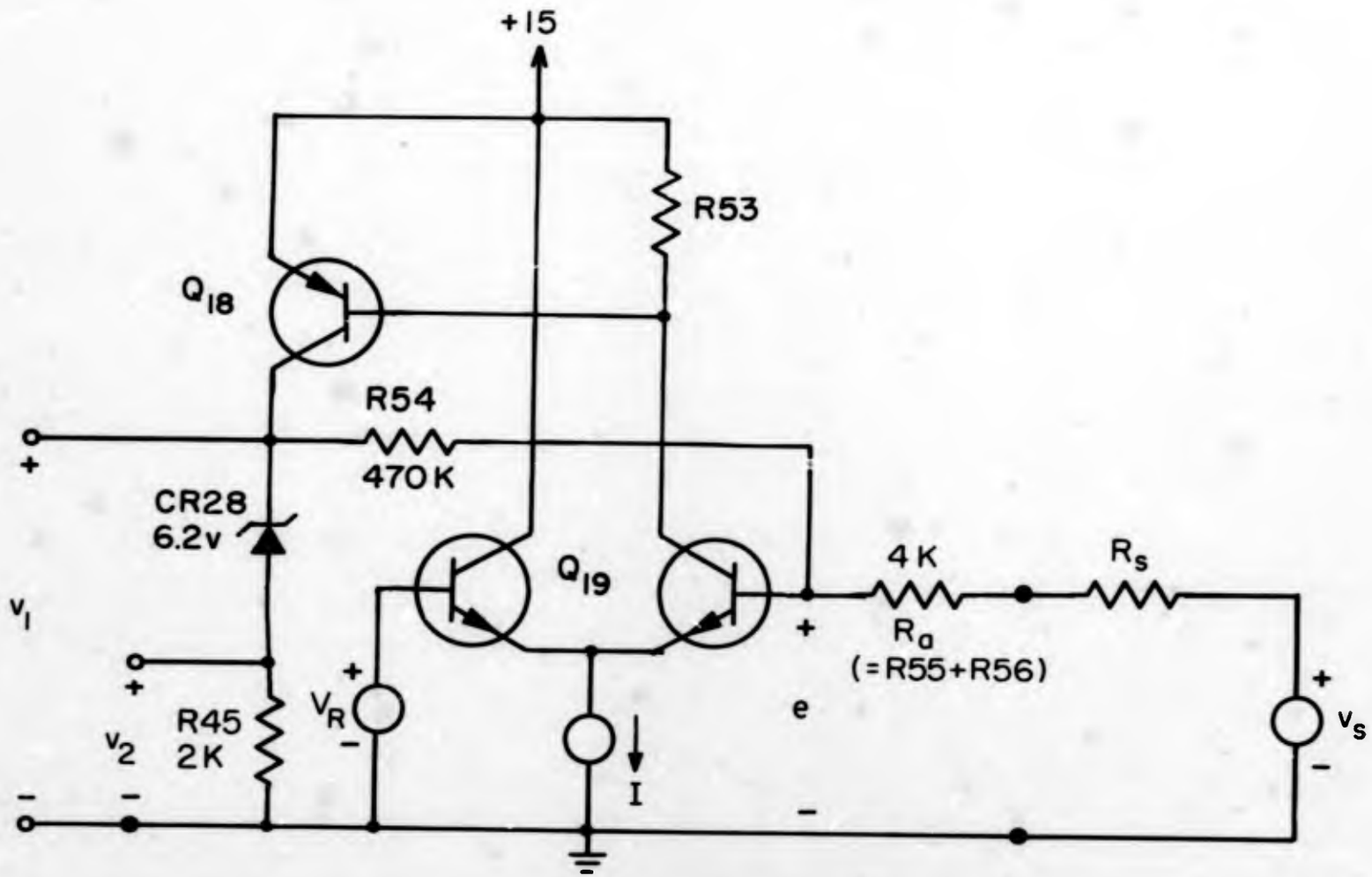


FIGURE 12.11

SIMPLIFIED SCHEMATIC OF THE TRANSITION VOLTAGE COMPARATOR

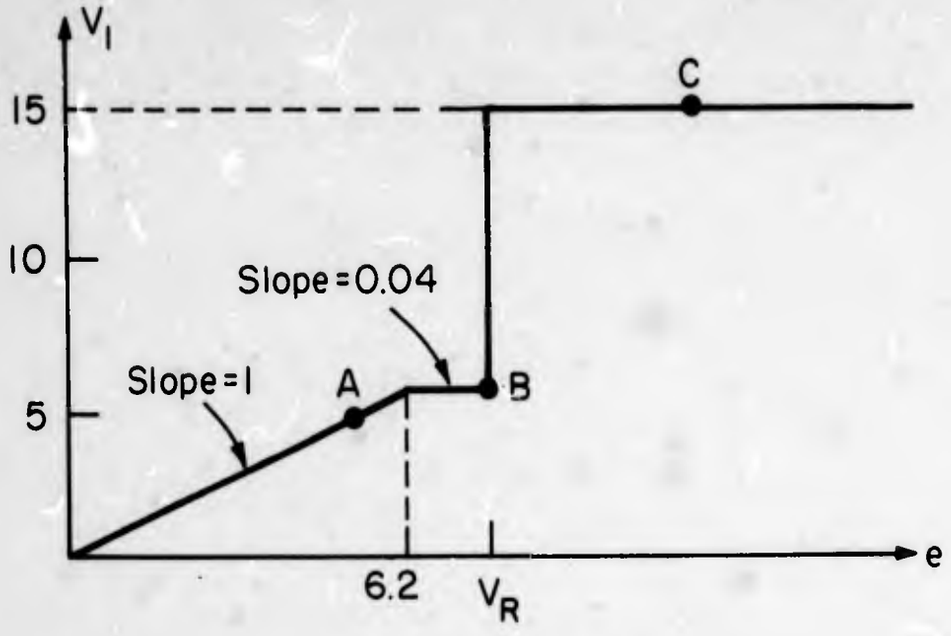


FIGURE 12.12

TRANSITION VOLTAGE COMPARATOR TRANSFER CHARACTERISTIC

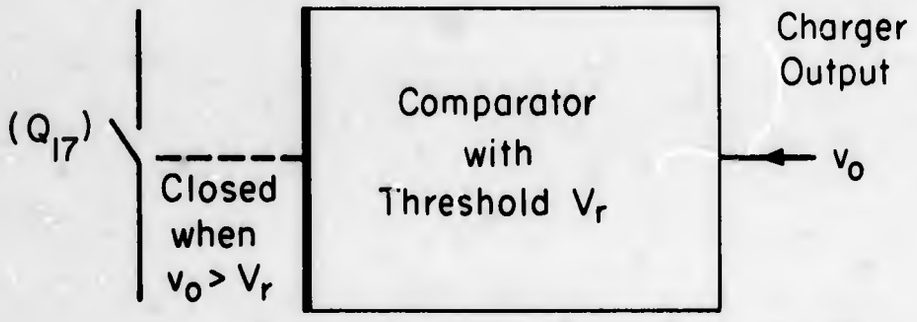


FIGURE 12.13

BLOCK DIAGRAM OF TRANSITION VOLTAGE SENSING CIRCUIT

When the voltage range selector is in the 12 volt position, the voltage to be sensed, v_b, is connected to the top of a resistive divider formed by R57 and R58 (shown in Figure 12.7). The values of R_s and v_s, the Thevenin parameters as seen looking back from R56, are then given by R_s = 5k ohms and $v_s = \frac{1}{2}v_b$. We then have

$$e = \frac{470}{479}\left(\tfrac{1}{2}v_b\right) + \frac{9}{479}v_1. \qquad (12.12)$$

For the moment, we shall assume that the voltage range switch is in the 6 volt position so that Eqn. 12.11 must be satisfied. Given a value of v_b, we may find e and v_1 from Eqn. 12.11 and the v_1 - e constraint shown in Figure 12.12. The relation in Eqn. 12.11 is illustrated in Figure 12.12 for three different values of v_b. For $v_b < 6$, the intersection occurs at a point A to the left of $e = V_r$. As v_b increases, the point of intersection moves toward point B, where $e = V_r$ and $v_1 \simeq 6.2$. A further increase in v_b forces the point of intersection to C, where $v_1 = 15$v. The critical value of v_b is that which corresponds to point B. Solving for this value, we obtain

$$v_b = 1.008V_r - 0.051 \qquad \text{(6 volt range)}. \qquad (12.13)$$

Similarly, we may obtain the result

$$v_b = 2(1.034V_r - 0.228) \qquad \text{(12 volt range)}. \qquad (12.14)$$

The expression in Eqn. 12.14 is not exactly twice that in Eqn. 12.13, but the error due to this factor should not exceed about 15 mv.

Now, referring to Figures 12.11 and 12.12, we see that v_2 will be zero until v_b reaches its critical value, at which time v_2 jumps to the value (15 - 6.2) or 8.8 volts. This then supplies base drive to Q17 (in Figure 12.2) through R45. Thus, we may model the transition voltage sensing circuit as a switch which is closed when the charger output voltage exceeds a preset value, as shown in Figure 12.13.

Output Polarity Sensing

Let us consider the circuit shown in Figure 12.14. We see that relay coil D2 can operate its associated contacts only if the input voltage v_i is a sufficiently positive value and Q3 is saturated. For Q3 to be saturated, Q2 must be off. If CR5 were absent, v_i could provide base drive to Q2, turning Q2 on. In order to keep Q2 off, the clamping diode CR5 must see a zero or negative value of v_o, the voltage at the charger output terminals. If we assume that the coil requires a minimum of 18 volts, we then have for the conditions that the coil is energized,

$$\left.\begin{aligned} v_i &> 18 \\ v_o &< 0 \end{aligned}\right\} \qquad (12.15)$$

From the contact wiring shown in Figure 12.14, we see that the circuit may be modeled as a single switch controlled by a logical combination of v_i and v_o and independent of any other circuit variables.

Input Voltage Sensing

The input voltage sensing circuit is shown in Figure 12.15. For $v_i < 0$, CR7 is open and Q4 is cut off. For $0 < v_i < 18$, CR6 is open and there is no voltage across R4, so that Q4 remains cut off. For $v_i > 18$, CR6 conducts and maintains a drop of 18 volts. This provides a voltage $(v_i - 18)$ across R4 which, in turn, provides base drive to Q4 through R30. Thus, Q4 acts as a switch which is open for $v_i < 18$ and closed when $v_i > 18$.

Mode Switch and Relay Logic

The PP4125 is designed to have three operating modes, selectable by means of a front panel switch. Here we shall consider only

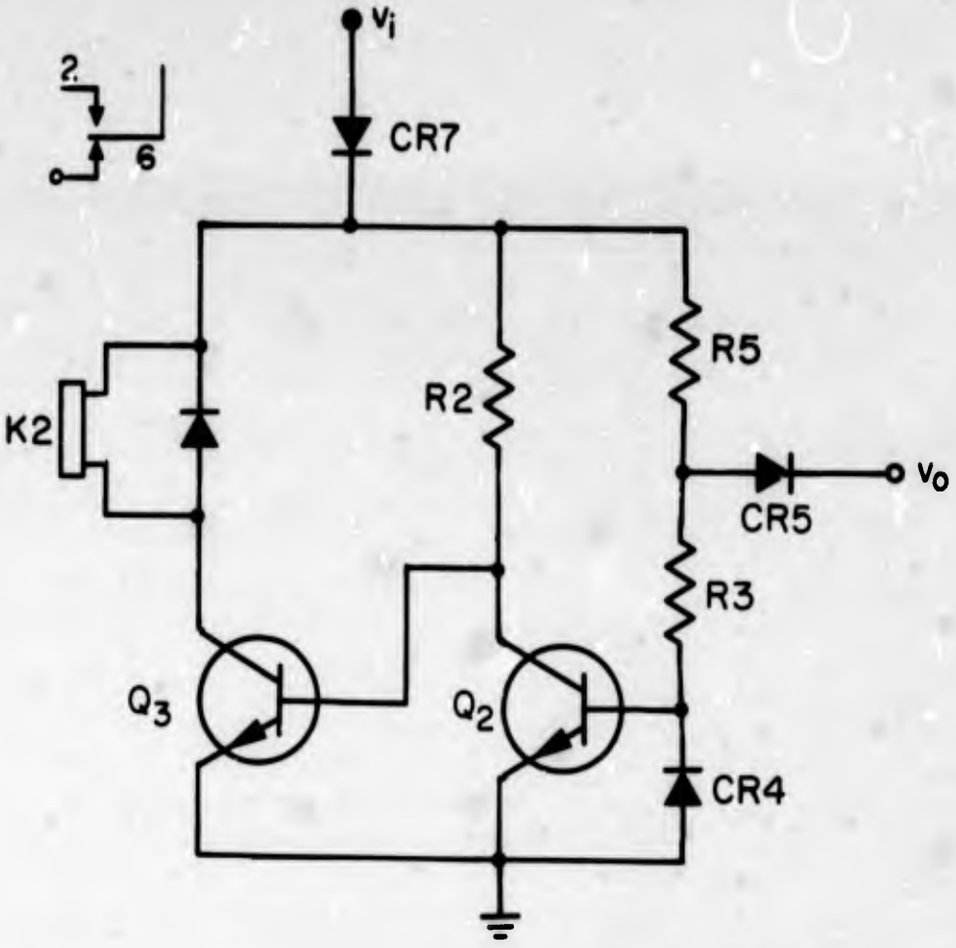


FIGURE 12.14 SCHEMATIC OF POLARITY SENSING CIRCUIT

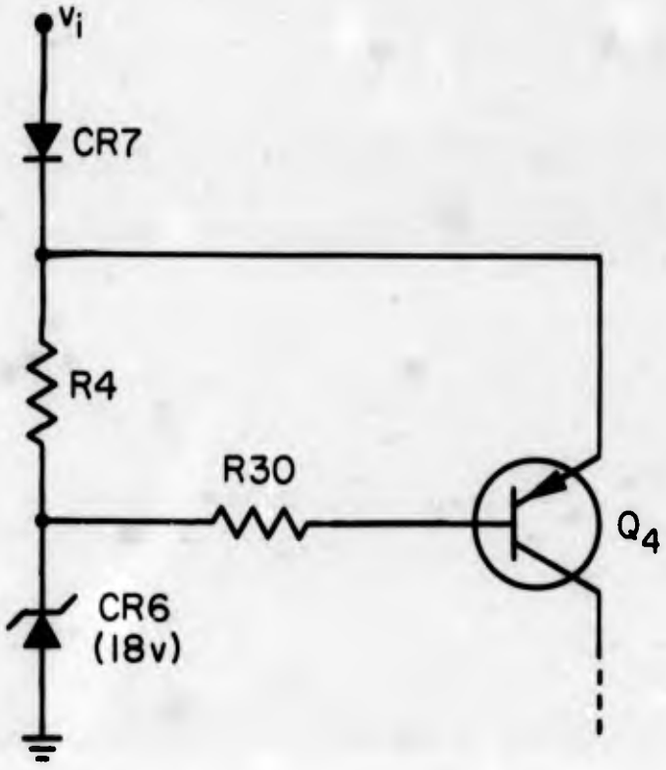


FIGURE 12.15 SCHEMATIC OF INPUT VOLTAGE SENSING CIRCUIT

one of these modes in detail since the remaining two modes can be treated in a similar manner.

The schematic for the entire switch and relay logic circuit is shown in Figure 12.16. Assuming that the mode switch is in its middle position, the SILVER mode, we may simplify this schematic somewhat as shown in Figure 12.17. The switches I, P and M are those operated by the input voltage sensing, output voltage polarity sensing and transition circuits respectively. S is the momentary contact START switch and L is the CHARGE OVER light. K1 and K3 are latching relays. An arrow by each coil shows the direction the contacts are thrown when that coil is excited.

The relay logic equations will be sequential in nature due to the time delay between coil excitation and contact response. We shall assume that an unspecified delay time Δt is sufficient to allow contact movement of all relays and sufficient excitation to all coils. For any relay we denote a coil by K and a contact by C. A logical "1" will denote a closed contact as indicated in Figure 12.17 or an excited coil. We shall assume that coil excitation is instantaneous with applied voltage and that all delays are lumped in the contact response. Thus, for the nonlatching relays, we have the logical expressions

$$C4\,(t + \Delta t) = K4(t) \tag{12.16}$$

$$C2\,(t + \Delta t) = \overline{K2}(t) \quad \text{(i.e., relevant contacts closed with no excitation)} \tag{12.17}$$

The logic describing the latching relays is more complicated due to their inherent memory. The desired expressions are easily obtained from a truth table, such as the one in Figure 12.18, defining the relay operation. Here we have defined the coil A as that which closes the contact C and coil B as that which opens the contact C. If neither coil is excited, the contact remains in its previous state (lines 1 and 2 in Figure 12.18). For example, in line 4, the contact C is closed and the coil B is excited at time t. The excitation on this coil causes the contact C to open at time $t + \Delta t$ as indicated. In line 3, the contact is already open when B is excited so that no change is initiated. In lines 7 and 8 we have assumed that no change in the contact state results if both coils are excited simultaneously. The logical expression

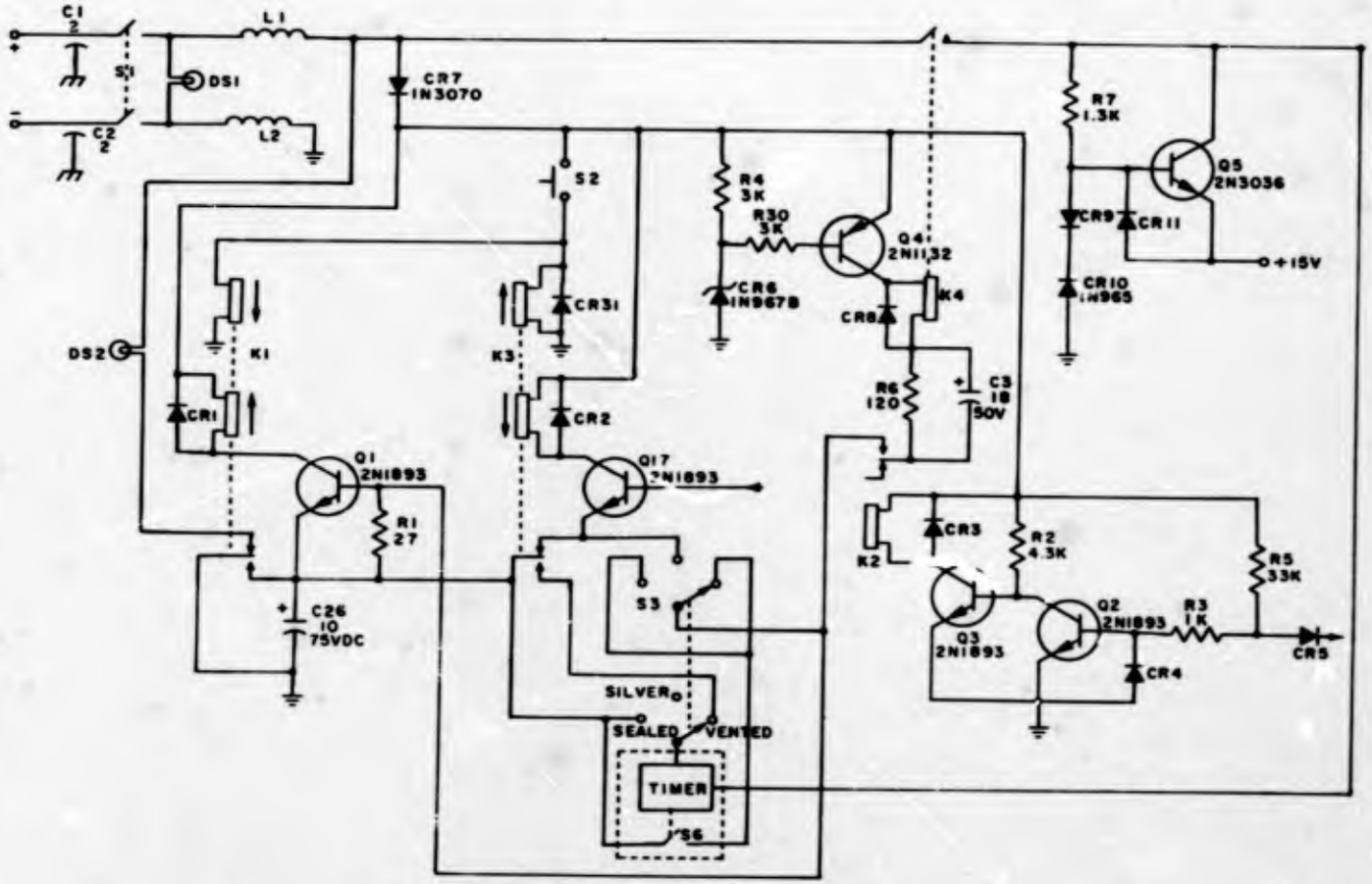


FIGURE 12.16

SWITCH AND RELAY LOGIC

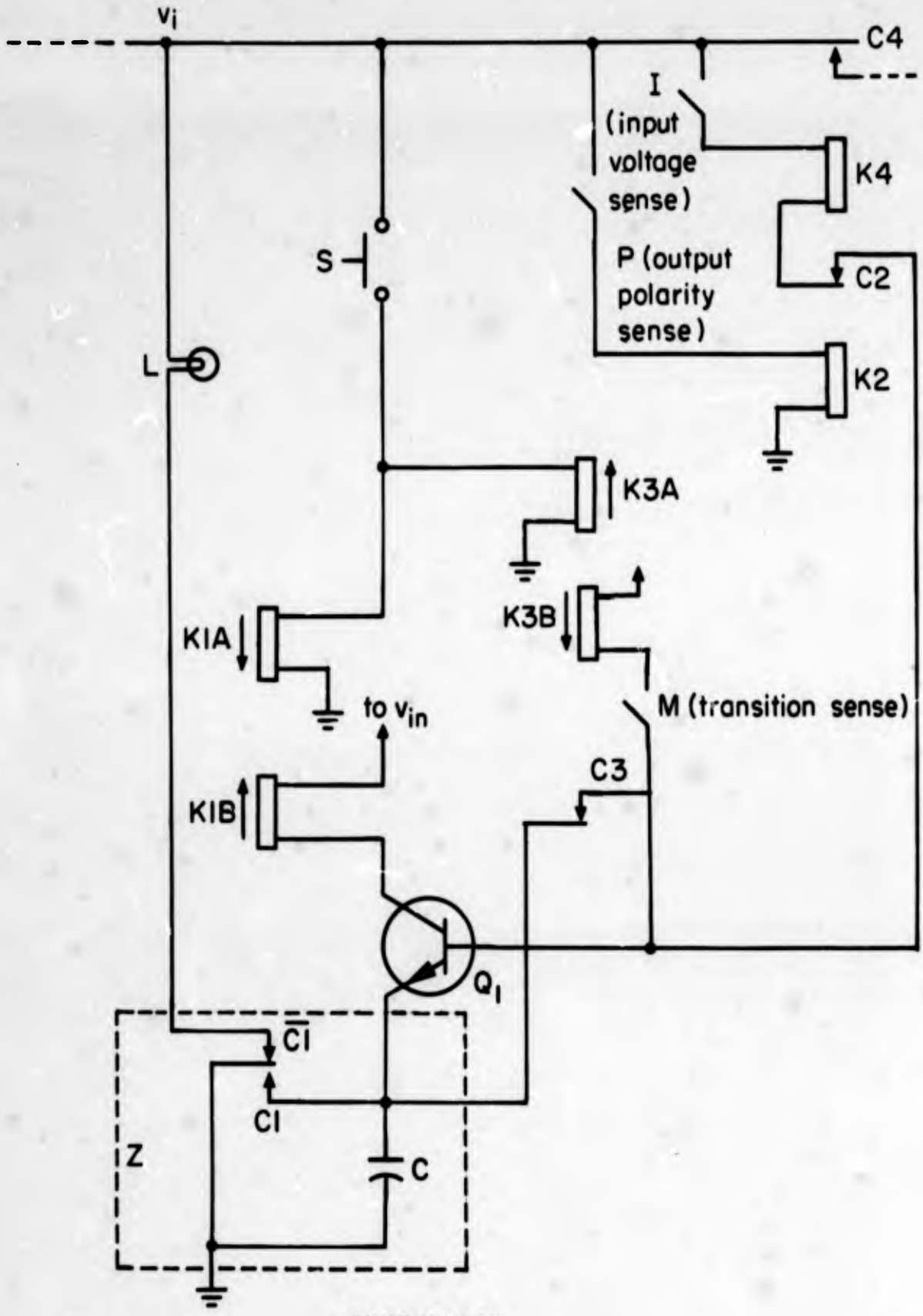


FIGURE 12.17

SIMPLIFIED LOGIC SCHEMATIC FOR THE SILVER CHARGING MODE

	State at Time t			State at Time t + Δt
	Coils		Contact	Contact
	A(t) (set)	B(t) (reset)	C(t)	C (t + Δt)
1	0	0	0	0
2	0	0	1	1
3	0	1	0	0
4	0	1	1	0
5	1	0	0	1
6	1	0	1	1
7	1	1	0	0
8	1	1	1	1

Logical Expression:

$$C(t + \Delta t) = C(t) \cdot [A(t) + \bar{B}(t)] + A(t) \cdot \bar{B}(t)$$

FIGURE 12.18

LATCHING RELAY TRUTH TABLE

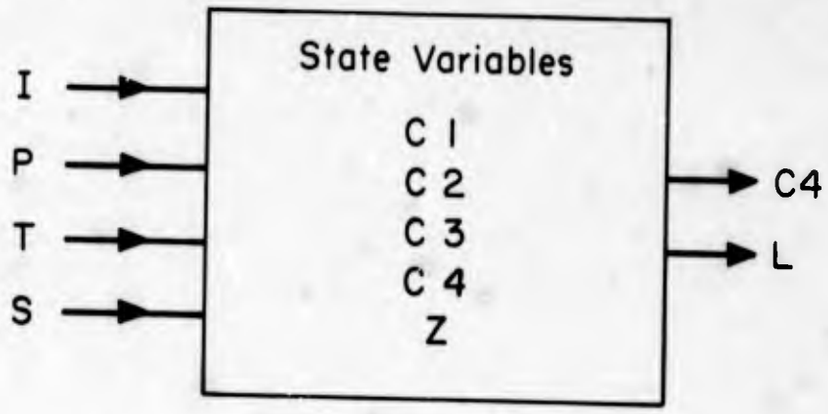


FIGURE 12.19

STATE MODEL OF LOGIC

defining this truth table is given at the bottom of Figure 12.18. In terms of the relay variables of Figure 12.17, we may write

$$C1\,(t + \Delta t) = C1(t) \cdot [K1A(t) + \overline{K1B}(t)] + K1A(t) \cdot \overline{K1B}(t) \tag{12.18}$$

$$C3\,(t + \Delta t) = C3(t) \cdot [K3A(t) + \overline{K3B}(t)] + K3A(t) \cdot K3B(t). \tag{12.19}$$

From the discussion of circuitry preceding this section, we may write for the logical state of the switch I(Q4)

$$I = \begin{cases} 0, \text{ when } v_i < 18 \\ 1, \text{ when } v_i > 18. \end{cases} \tag{12.20}$$

From Eqn. 12.15 we have for the output polarity switch P(Q3)

$$P = \begin{cases} 0, \text{ when } v_o > 0 \\ 1, \text{ when } v_o < 0. \end{cases} \tag{12.21}$$

Here we shall define a variable T by

$$T = \begin{cases} 0, \text{ when } v_o < V_r \\ 1, \text{ when } v_o > V_r \end{cases} \tag{12.22}$$

so that T indicates whether the preset transition voltage has been reached. With reference to Figure 12.2, we see that the transition sensing circuit derives its power from a point after the contact C4. Thus, this contact must be closed in order for the transition circuit to operate. Thus, we may write for M,

$$M(t) = T(t) \cdot C4(t). \tag{12.23}$$

Before we proceed to write the equations relating the various switches and relays, the function of the capacitor C at the emitter of Q1 should be explained. Its purpose is to provide, in effect, a delay in the relay characteristic and ensures proper operation. If C1 was previously closed and is then opened at time t, the capacitor C provides a path from the emitter of Q1 to ground for a short time later (assumed to be one Δt interval here). Thus, the transmission through the capacitor may be thought of as the C1 transmission function delayed by Δt. Denoting the transmission from the emitter of Q1 to ground by Z as shown in Figure 12.17, we effectively have

$$Z(t) = C1(t) + C1(t - \Delta t). \tag{12.24}$$

Now we may write the logical equations relating the switch and relay states. Since I is essentially an indication of the presence of sufficient supply voltage, which we assume is necessary to operate all relay coils, we shall use I as the input power variable and, therefore, will appear in all relay expressions. Thus, the coil K2 excitation state may be written

$$K2(t) = P(t) \cdot I(t). \tag{12.25}$$

Tracing the transmission path for K4, we obtain

$$K4(t) = I(t) \cdot C2(t) \cdot C3(t) \cdot Z(t). \tag{12.26}$$

Two of the latching coil expressions are given by

$$K1A(t) = S(t) \cdot I(t)$$

$$K3A(t) = S(t) \cdot I(t) \tag{12.27}$$

For the coil K3B, we have

$$K3B(t) = M(t) \cdot C3(t) \cdot Z(t) \cdot I(t) \tag{12.28}$$

The coil K1B can be excited only when Q1 is conducting, and we have

$$K1B(t) = Q1(t) \cdot Z(t) \cdot I(t). \tag{12.29}$$

Transistor Q1 will be on only when it has base drive. For such drive to occur, we see from Figure 12.17 that C3 must be open so that the base emitter junction is not shorted, and base current must be supplied through either of the paths containing coils K3B or K4. Thus, we have

$$Q1(t) = \overline{C3}(t) \cdot [C2(t) \cdot I(t) + M(t)].$$

Combining this with Eqn. 12.29, we obtain

$$K1B(t) = I(t) \cdot Z(t) \cdot \overline{C3}(t) \cdot [C2(t) + M(t)]. \qquad (12.30)$$

Finally, the CHARGE OVER lamp L is described by

$$L(t) = \overline{C1}(t) \cdot I(t) \qquad (12.31)$$

Equations 12.16 - 12.31 describe the logical operation of the charger when the mode switch is in the SILVER mode. At the beginning of this chapter we observed that the function of the auxiliary circuitry was to connect the main power converter between the source and load via operation of relay K4. Thus, it is the state of the contact C4 that we are concerned with. We may model this logic system by a discrete time system with four inputs, I, S, T and P, two outputs C4 and L, and state variables C1, C2, C3, C4 and Z as shown in Figure 12.19. The inputs are the variables external to the system and are defined as follows:

$$I = \begin{cases} 0 \text{ - insufficient input voltage} \\ 1 \text{ - sufficient input voltage for operation} \end{cases}$$

$$P = \begin{cases} 0 \text{ - proper polarity at output} \\ 1 \text{ - improper polarity at output} \end{cases}$$

$$S = \begin{cases} 0 \text{ - START switch open} \\ 1 \text{ - START switch depressed (closed)} \end{cases}$$

$$T = \begin{cases} 0 \text{ - output voltage less than transition voltage setting} \\ 1 \text{ - output voltage greater than transition voltage setting} \end{cases} \qquad (12.32)$$

The outputs of the system are C4 and L, which are defined by

$$C4 = \begin{cases} 0 \text{ - main power converter disconnected} \\ 1 \text{ - main power converter connected} \end{cases}$$

$$L = \begin{cases} 0 \text{ - no CHARGE OVER indication} \\ 1 \text{ - CHARGE OVER indicated.} \end{cases} \qquad (12.33)$$

The state variables C1 - C4 and Z are the states of the relay contacts and the capacitor C26 at the emitter of Q1. We shall consider time increments of Δt and we shall use the notation $X_n = X(n \cdot \Delta t)$ where X is a logical variable. We can determine the state equations from Eqns. 12.16 - 12.31 by eliminating the coil variables and the auxiliary variables previously defined. This yields the logical state equations

$$C1_{n+1} = (C1_n + S_n \cdot I_n)(C3_n + Z_n + \overline{C2}_n \cdot \overline{T}_n + \overline{C2}_n \cdot \overline{C4}_n) + C1_n(S_n + \overline{I}_n)$$

$$C2_{n+1} = \overline{P}_n + \overline{I}_n$$

$$C3_{n+1} = (C3_n + S_n \cdot I_n)(\overline{C3}_n + \overline{Z}_n + \overline{T}_n + \overline{C4}_n) + C3_n \cdot (S_n + \overline{I}_n)$$

$$C4_{n+1} = I_n \cdot Z_n \cdot C2_n \cdot C3_n$$

$$Z_{n+1} = C1_n + S_n \cdot I_n(C3_n + \overline{Z}_n + \overline{C2}_n \cdot \overline{T}_n + \overline{C2}_n \cdot \overline{C4}_n) \qquad (12.34)$$

and the output equations

$$C4_{n+1} = C4_{n+1}$$

$$L_{n+1} = \overline{C1}_{n+1} \cdot I_{n+1} \cdot \qquad (12.35)$$

Equations 12.34 and 12.35 describe the behavior of the relay logic when the charge mode switch is in the SILVER mode.

The operation in a typical case may be studied by selecting a set of input values and an initial set of states and then using Eqns. 12.34 and 12.35 to observe the charger behavior. A table such as that shown in Figure 12.20 is useful in such a case. Here a time sequence of input values is shown on the left side of the chart. We may determine the operation of the unit from this input sequence once we choose an initial state. An arbitrary set of values for the state variables C1 - C4 and Z at the interval corresponding to n = 0 was selected and these are shown on the first line in Figure 12.20. Once these state values are fixed, we can then determine the entire time history of the state variables from the initial state and the input time history. Thus, from the values of the input and state variables at n = 0, we may find the state values at n = 1 from Eqn. 12.34. Eqn. 12.35 then allows us to calculate the values of the output variables. Since the time history of the input is given and we now know the state n = 1, we may compute the state and output for n = 2. This process can be continued for any input sequence.

As long as no input power is applied (I = 0), we see that the system reaches a stable state as shown for n = 2. Here the CHARGE OVER lamp is off (L = 0) and the main power converter is disconnected from the source and load (C4 = 0). We should point out that such a stable state can exist indefinitely if the inputs remain fixed. This is merely to point out that the "time" unit n is mainly a sequencing index, and that perhaps hours or days may elapse before the next n unit is initiated. At n = 3 power of proper polarity and magnitude is applied to the unit (I = 1). At n = 6, we see that the system has reached a stable state at which the main power converter is disconnected (C4 = 0) and CHARGE OVER lamp is illuminated (L = 1).

After some time, we now assume that the START switch is momentarily depressed (S = 1 at n = 7). We observe that after two changes in state the system reaches a stable state at n = 9. For this state, the main power converter is connected between the source and the load (C4 = 1) and the CHARGE OVER lamp is dark (L = 0). The unit will remain in this state, which is its charging state, until there is a change in one or more logical inputs.

Time	Inputs				State Variables					Outputs
n	I	T	S	P	C1	Z	C2	C3	C4	L
0	0	0	0	0	1	1	0	0	1	0
1	0	0	0	0	1	1	1	0	0	0
2	0	0	0	0	1	1	1	0	0	0
3	1	0	0	0	1	1	1	0	0	0
4	1	0	0	0	0	1	1	0	0	1
5	1	0	0	0	0	0	1	0	0	1
6	1	0	0	0	0	0	1	0	0	1
7	1	0	1	0	0	0	1	0	0	1
8	1	0	0	0	1	1	1	1	0	0
9	1	0	0	0	1	1	1	1	1	0
10	1	0	0	0	1	1	1	1	1	0
11	0	0	0	0	1	1	1	1	1	0
12	0	0	0	0	1	1	1	1	0	0
13	0	0	0	0	1	1	1	1	0	0
14	1	0	0	0	1	1	1	1	0	0
15	1	0	0	0	1	1	1	1	1	0
16	1	0	0	0	1	1	1	1	1	0
17	1	1	0	0	1	1	1	1	1	0
18	1	1	0	0	1	1	1	0	1	0
19	1	1	0	0	0	1	1	0	0	1
20	1	1	0	0	0	0	1	0	0	1
21	1	0	0	0	0	0	1	0	0	1
22	1	0	0	0	0	0	1	0	0	1
23	1	0	0	0	0	0	1	0	0	1
24	1	0	0	0	0	0	1	0	0	1

FIGURE 12.20

STATE TABLE FOR RELAY LOGIC

At n = 11, the input power is interrupted which causes C4 to change to its zero state, disconnecting the main power converter and halting the charging operation. When power resumes at n = 14, we see that C4 closes, which allows the charge operation to resume.

At some time, we have assumed that the output voltage exceeds the preset transition voltage (T = 1 at b = 17). The chart shows us that a sequence of states is followed until n = 20, at which point the state remains constant. In this state, the main power converter is disconnected (C4 = 0) and the CHARGE OVER lamp is illuminated (L = 1).

Figure 12.20 and the preceding discussion show that in the SILVER charging mode, a charging cycle is initiated by supplying input power and depressing the START switch. The charging cycle continues, stopping and automatically resuming if power is interrupted, until the output voltage reaches the preset value of transition voltage, at which time the charge is stopped and the CHARGE OVER lamp is illuminated.

The above process may be carried out for any input sequence, although it should be clear that the labor involved in an exhaustive study would be quite tedious. Further, the results presented here are valid only when the mode switch is in the SILVER mode. In the other modes, the state equations will be different and some new state variables may need to be introduced. An alternative procedure would be to include the mode switch is a general state formulation, thus incorporating its position and movements automatically. The penalty paid for this generalization, as is usually the case, is an increase in the complexity of the state formulation.

Alternately, we may readily obtain all the information shown in Figure 12.20 from a state transition diagram of the relay logic similar to the one illustrated in Figure 10.45. Such a diagram, valid for the SILVER mode, is shown in Figure 12.21. This transition chart contains all the information shown in Figure 12.20 and it allows an easy determination of the presence of some simple, undesirable modes. For instance, there is no state in which the system can be locked into a "chatter" condition due to the logical design. This approach to sequential analysis can be quite useful when operating sequences under abnormal conditions are important. This

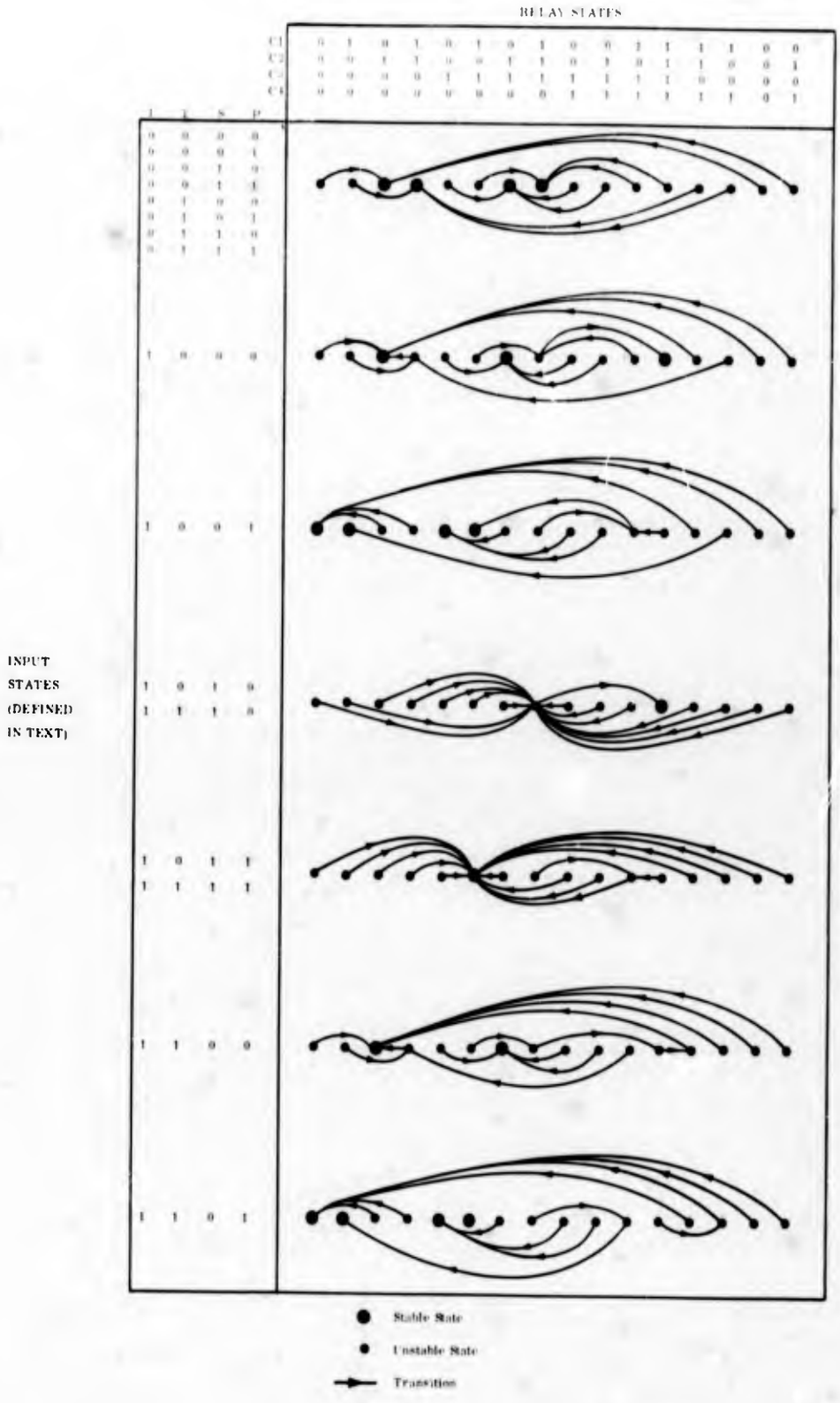


FIGURE 12.21

STATE TRANSITION DIAGRAM

approach is readily mechanized on a computer, as is the input sequence method, which can be an excellent aid in complex system analysis.

12.2 BASIC POWER CONVERTER

The basic power converter can be partitioned into two sections as shown in Figure 12.22 - a basic output stage and control circuitry. The output stage consists of transistors Q10, Q11 and diode CR22, which are the switches, transformer T3 and inductors L3, L4 and L5 and capacitor C19, which form the output filter. We can see that the form of the output stage is fixed but that the inductor and transformer windings are changed by the current range selector switch. In this section, we shall consider only one current range - the 5 ampere range.

Output Stage

An inspection of Figure 12.22 reveals that the output stage is the chopper output stage discussed in Chapter 5. An equivalent for this output stage is illustrated in Figure 12.23. Here C is the capacitor C19 in the unit and R_s and L are equivalent parameters determined by experimental measurements on a unit. The measured equivalent R_s of 0.2 ohms is much greater than the equivalent diode resistance or saturation resistance of the output transistors so that these latter terms will be neglected here.

If we include the control system in the model, we may construct a quasi-static model of the entire basic power converter as shown in Figure 12.24. Here we consider the input voltage V_s to be a constant function of time. The main object of the analysis will be to characterize the V_o-D relation of the output stage, which we can do at the present, and to characterize the D - (controlled output variable) relation of the control system. At this point however, we shall leave the output stage in the form shown in Figure 12.24 and return to this model after a consideration of the control system.

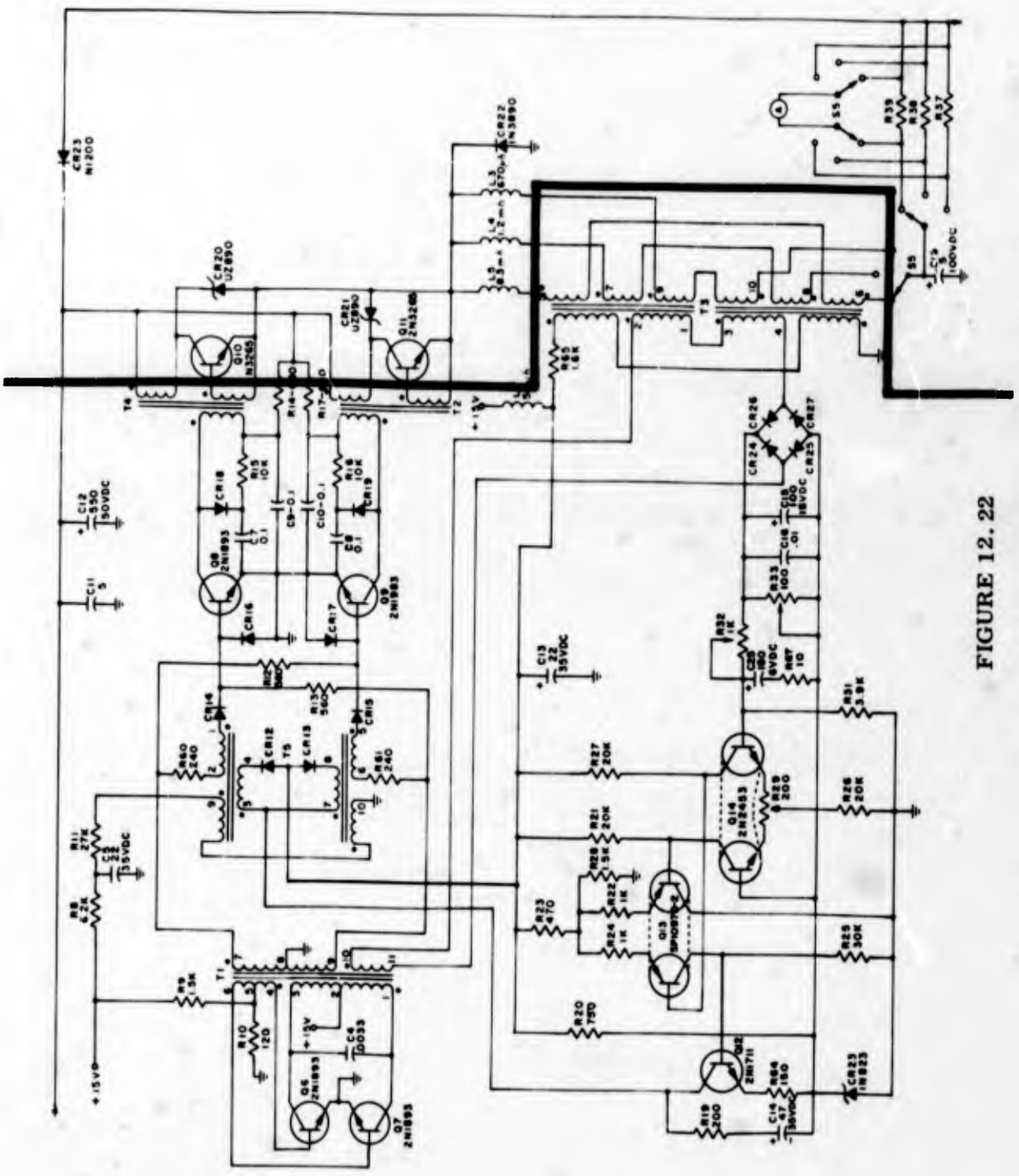
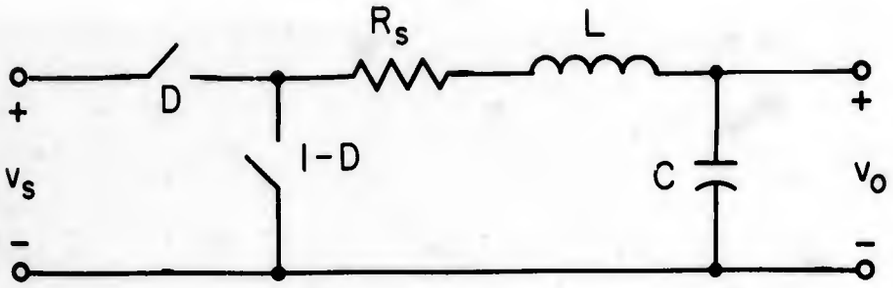


FIGURE 12. 22

BASIC POWER CONVERTER



$R_s = 0.2\ \Omega$

$L = 1.3$ mh

$C = 5\ \mu f$

FIGURE 12.23

OUTPUT STAGE EQUIVALENT

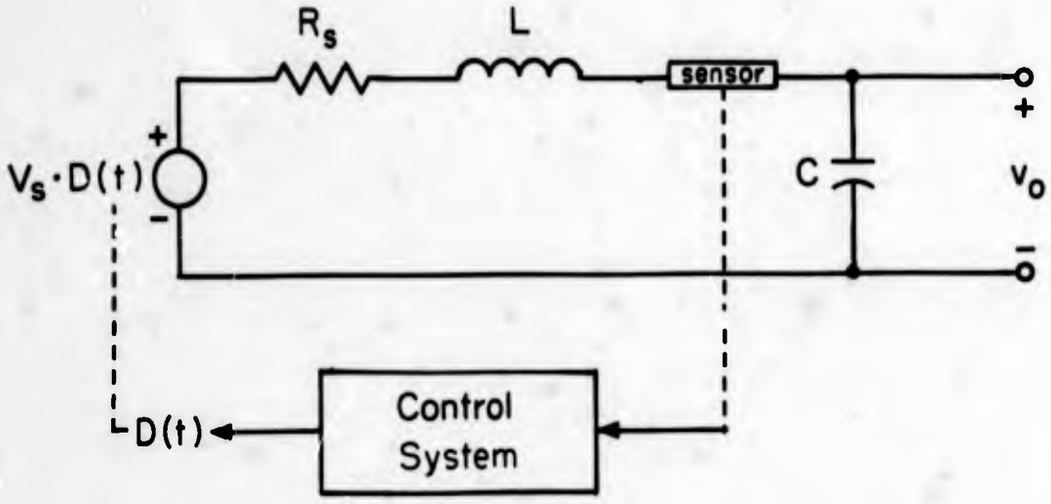


FIGURE 12.24

QUASI-STATIC MODEL

Control System

The circuit blocks comprising the control system for the charger are shown in Figure 12.4. We shall now consider these circuits so that we may characterize a model of the control system.

Inverter

The inverter circuit used in the PP4125 is one that is frequently encountered and has been treated extensively in the literature. A good reference is Royer's original paper.* The specific magnetic properties of the core used in the inverter were not available and were not measured. As is evident from Figure 12.22, we need only be concerned with the inverter as it is seen from its output windings on T1. Such a characterization was made from measurements on a working unit, which yields the model shown in Figure 12.25. The inverter frequency should be essentially as stable as the 15 vdc line and the temperature stability of the core saturation flux.

Current Sensing

Now we shall consider the operation of transformer T3. A simplified circuit of the current sensing circuit is shown in Figure 12.26. Here $v_b(t)$ is square wave excitation derived from winding 10 - 11 on transformer T1 and N is the network consisting of the diode bridge CR24 - CR27 and the associated filter. Winding 11-12 is the winding excited through R65 and winding 7 - 8 is the output winding of interest when the charger is set to the 5 ampere current range (the other output windings are open-circuited by S5).

We shall make the following assumptions at this point. We assume that the currents I_o, the output current, and I_b, the current in winding 11-12 supplied through R65, are independent of any constraints due to T3. Therefore, we may assume that windings 7 - 8

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* Bibliography III, Reference 136

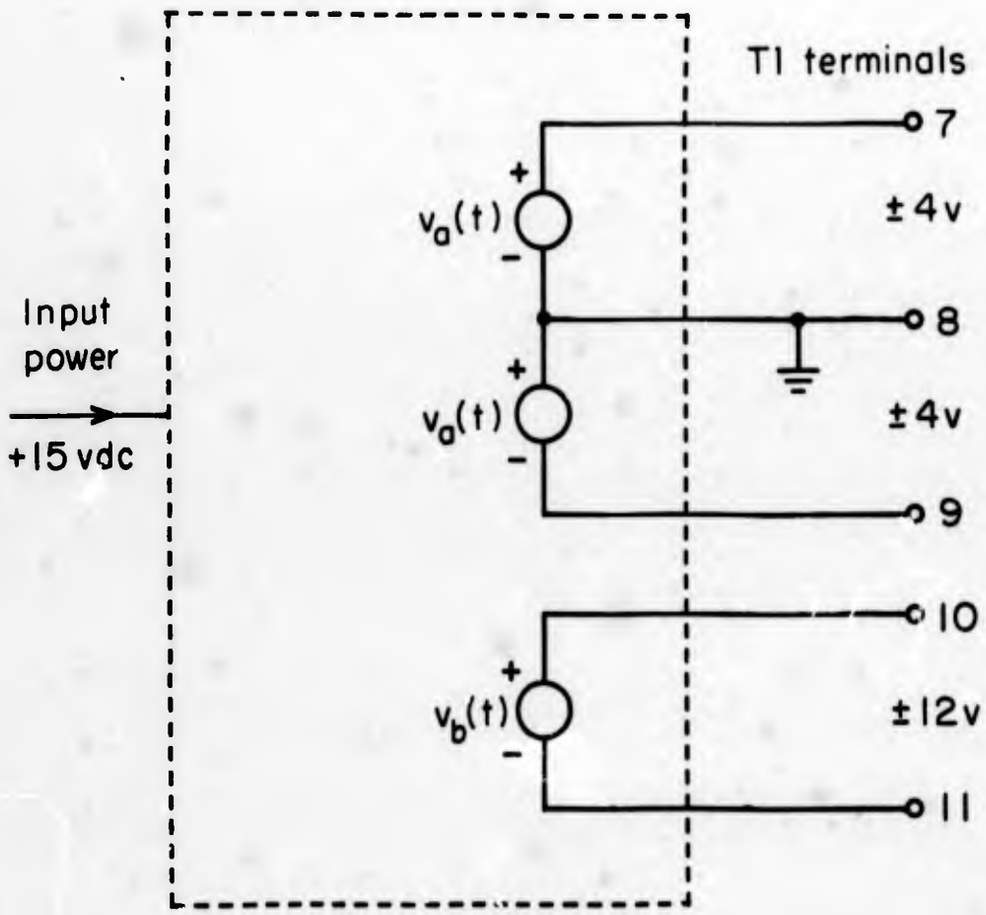


FIGURE 12.25

TERMINAL MODEL OF INVERTER

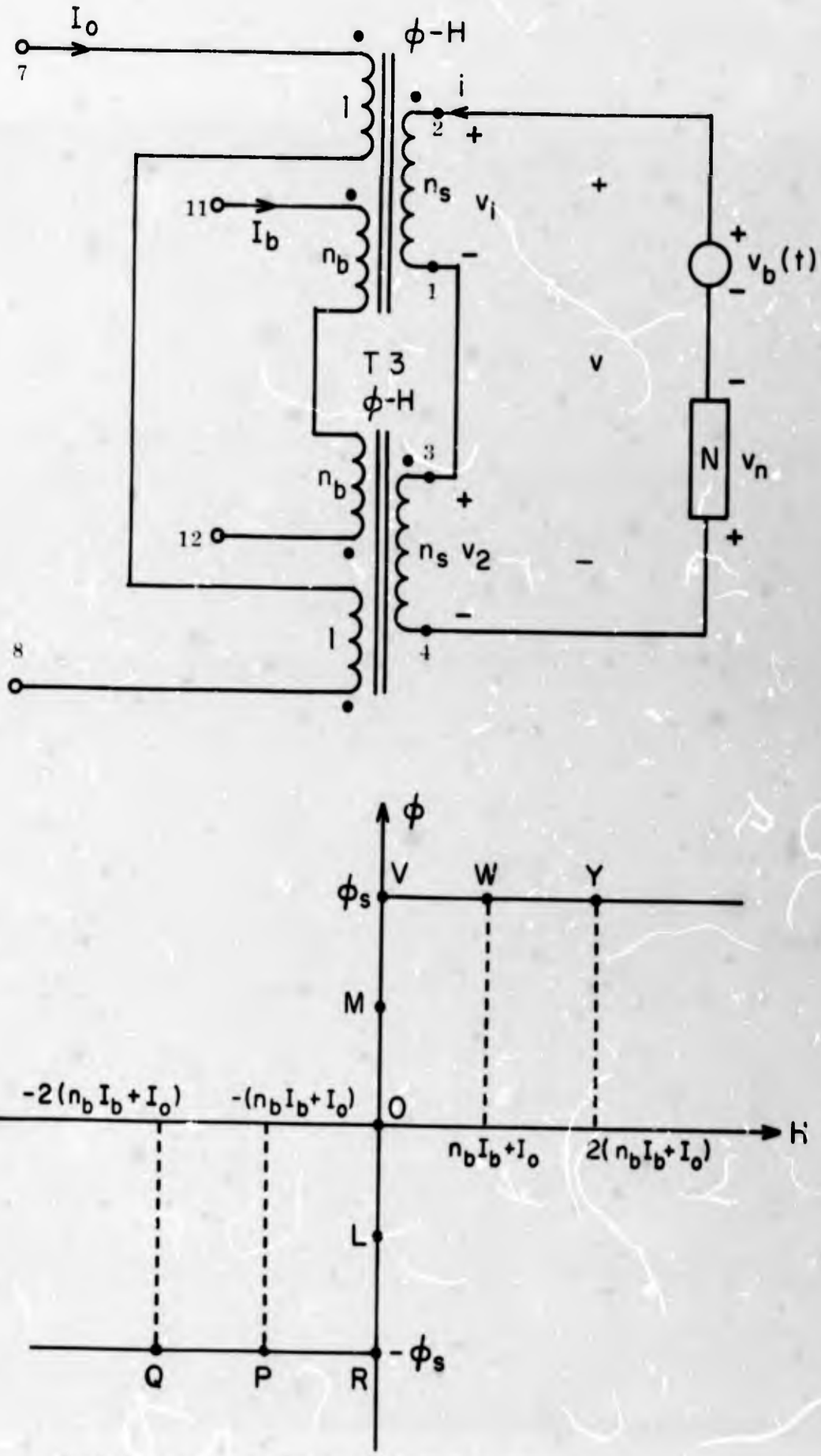


FIGURE 12.26 CURRENT SENSING TRANSFORMER

and 11-12 are connected to current sources I_o and I_b respectively as far as operation of T3 is concerned. We also take each core of T3 to have the square ϕ-H characteristic shown in Figure 12.26 with saturation flux ϕ_s.

The terminal characteristics of an m-winding magnetic element, as shown in Figure 12.27, with flux $\phi = \phi(H)$ and turns per winding of $n_1, n_2, \ldots n_m$ are described by

$$\left.\begin{aligned} H &= n_1 i_1 + n_2 i_2 + \ldots + n_m i_m \\ \phi &= \phi(H) \\ v_1 &= n_1 \frac{d\phi}{dt} \\ v_2 &= n_2 \frac{d\phi}{dt} \\ &\vdots \\ v_m &= n_m \frac{d\phi}{dt} \end{aligned}\right\} \qquad (12.36)$$

or, if we wish, by the set of m equations

$$v_k = n_k \frac{d}{dt}\left[\phi\left(\sum_{j=1}^{m} n_j i_j\right)\right], \qquad k = 1, 2, \ldots m \qquad (12.37)$$

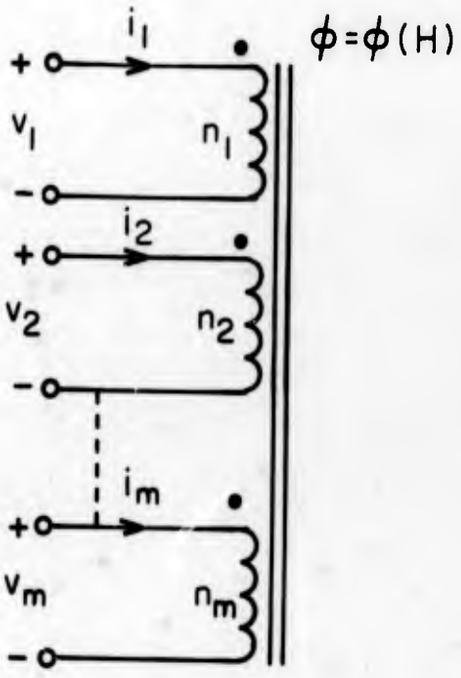


FIGURE 12.27

M-WINDING MAGNETIC ELEMENT

For the circuit in Figure 12.26, we then have, with the given sign conventions,

$$\left.\begin{aligned} H_1 &= n_s i + n_b I_b + I_o \\ H_2 &= n_s i - n_b I_b - I_o \end{aligned}\right\} \tag{12.38}$$

$$\left.\begin{aligned} \phi_k &= \begin{cases} \phi_s, & H_k > 0 \\ -\phi_s, & H < 0 \end{cases} \\ H_k &= 0, \qquad -\phi_s < \phi_k < \phi_s \end{aligned}\right\} \tag{12.39}$$

$$\left.\begin{aligned} v_1 &= n_s \frac{d\phi_1}{dt} \\ v_2 &= n_s \frac{d\phi_2}{dt} \end{aligned}\right\} \tag{12.40}$$

We shall assume that $I_o > 0$, $I_b > 0$, that $v_b(t)$ starts at $t = 0$ as shown in Figure 12.28 and that $i(t) = 0$ for $t < 0$. Then, we have for $t < 0$,

$$\left.\begin{aligned} &H_1 = n_b I_b + I_o > 0, \\ &\phi_1 = +\phi_s, \\ &H_2 = -(n_b I_b + I_o) < 0, \\ &\phi_2 = -\phi_s, \\ &v_1 = v_2 = 0. \end{aligned}\right\} \tag{12.41}$$

Note that

$$H_1 - H_2 = 2(n_b I_b + I_o) > 0 \tag{12.42}$$

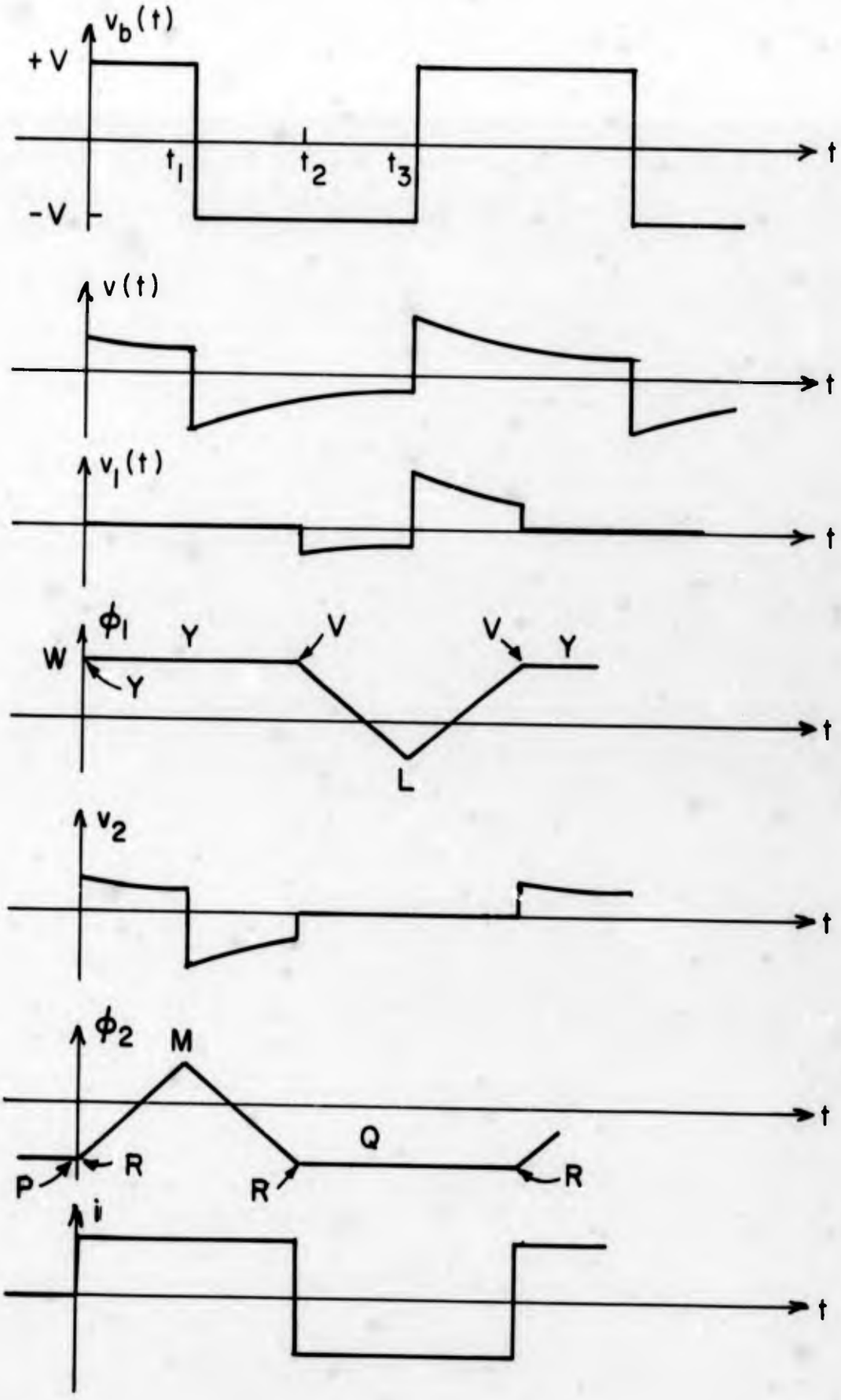


FIGURE 12.28

WAVEFORMS IN CURRENT-SENSING CIRCUIT

if $I_b > 0$ and $I_o > 0$. This means that the state of both cores, which can be represented by two points on the ϕ-H characteristic, are such that the state of core 1 is always $2(n_b I_b + I_o)$ to the right of the point representing the state of core 2. Thus, for the conditions given in Eqn. 12.41, we have core 1 at the point W and core 2 at the point P. In the following analysis, the core states corresponding to various points in the time plots in Figure 12.28 will be given by the appropriate letter on the time plots.

At $t = 0$, v_b jumps to +V(12 volts). Here we assume that $|v_n| < |v_b|$ so that $v(t) > 0$ when $v_b(t) > 0$ and $v(t) < 0$ when $v_b(t) < 0$. Therefore, we must have

$$v = v_1 + v_2 = n_s \frac{d}{dt}\left[\phi_1 + \phi_2\right] > 0. \tag{12.43}$$

It follows from Eqn. 12.43 that $(\phi_1 + \phi_2)$ must be increasing since its derivative is positive. Since $\phi_1 = +\phi_s$, it cannot be increasing so that ϕ_2 must begin to increase from $-\phi_s$. From Eqn. 12.39 we see that $H_2 = 0$. Now, using Eqn. 12.38 and Eqn. 12.39, we obtain

$$H_2 = n_s i - n_b I_b - I_o = 0$$

or

$$i = \frac{1}{n_s}(n_b I_b + I_o), \qquad 0 < t < t_1 \tag{12.44}$$

and

$$H_1 = n_s i + n_n I_b + I_o = 2(n_b I_b + I_o) > 0, \tag{12.45}$$

so that

$$\phi_1 = \phi_s, \quad v_1 = n_s \frac{d\phi_1}{dt} = 0, \tag{12.46}$$

$$v_2(t) = v(t),$$

$$\phi_2 = \frac{1}{n_s} \int_0^t v_2(\tau) d\tau. \tag{12.47}$$

These conditions are illustrated in Figure 12.28, with the state of each core at $t = 0^+$ being given on the ϕ-plots. Thus, core 1 remains at the point Y in Figure 12.26 and core 2 moves up the ϕ-axis from point R.

At time t_1, $v_b(t)$ switches to -V and we assume that v(t) also jumps to some negative value as shown. Now we have the constraint

$$v = n_s \frac{d}{dt}\left[\phi_1 + \phi_2\right] < 0 \tag{12.48}$$

so that $(\phi_1 + \phi_2)$ must be decreasing. If either ϕ_1 or ϕ_2 is changing with time, then from Eqn. 12.39 the corresponding H must be zero. Therefore, the remaining H must be nonzero and the corresponding ϕ must be constant. If we assume that ϕ_1 is decreasing, then we have

$$H_1 = 0,$$

$$H_2 = -2(n_b I_b + I_o),$$

$$\phi_2 = -\phi_s.$$

Note that this condition necessitates an instantaneous jump in ϕ_2, which, from Eqn. 12.48 would produce an infinite voltage. Since the voltage v is finite, this cannot be the case. Hence, it must be that ϕ_2 is

decreasing. The corresponding conditions are then

$$\left.\begin{aligned} H_2 &= 0, \\ H_1 &= 2(n_b I_b + I_o), \\ \phi_1 &= \phi_s \\ \phi_2 &= \frac{1}{n_s}\int_0^t v(\tau)d\tau, \\ i &= \frac{1}{n_s}(n_b I_b + I_o). \end{aligned}\right\} \qquad (12.49)$$

Thus v_1 remains zero and v_2 follows v(t) while ϕ_2 is decreasing.

At $t = t_2$, $\phi_2(t)$ reaches $-\phi_s$ and cannot decrease further, so that it cannot maintain a negative derivative. From Eqn. 12.48 we know that either ϕ_1 or ϕ_2 must be decreasing while v(t) is negative. It follows that ϕ_1 must then begin to decrease after $t = t_3$, which in turn necessitates that $H_1 = 0$ by Eqn. 12.39. Eqn. 12.42 then implies that $H_1 < 0$, $\phi_2 < -\phi_s$ and $v_2 = 0$. Thus for $t > t_2$, we have

$$\left.\begin{aligned} v_1 &= v = n_s\frac{d\phi_1}{dt} < 0, \\ H_1 &= 0, \\ i &= -\frac{1}{n_s}(n_b I_b + I_o), \\ H_2 &= -2(n_b I_b + I_o), \\ \phi_2 &= -\phi_s, \\ v_2 &= 0. \end{aligned}\right\} \qquad (12.50)$$

These conditions are also shown in Figure 12.28.

When $t = t_3$, $v_b(t)$ switches to +V and v(t) jumps to a positive value. We may observe that the conditions here are identical to those at $t = t_2$ but with the roles of each core reversed and the sign of v(t) reversed. Hence the continuation of the plots in Figure 12.28 is easily accomplished as shown.

From Eqns. 12.44, 12.49 and 12.50 we see that the current i in the secondary windings of T3 is a zero average square wave with a peak value of $\frac{1}{n_s}(n_b I_b + I_o)$ and a period equal to that of the inverter output $v_b(t)$. Note from the preceding analysis that this peak value is independent of the saturation flux ϕ_s of the cores, the peak value of $v_b(t)$, and the frequency of $v_b(t)$ as long as the basic operation of the circuit is not affected.

The network N illustrated in Figure 12.26 is a full-wave bridge rectifier and filter consisting of CR24 - CR27, R33, C15 and C16. Since the operation of transformer T3 places a current constraint on the winding in series with the rectifier network N, the rectifier "sees" a current source drive. Thus, the rectifier output is not affected by the diode voltage drops. Looking back into the diode bridge, we then see a current source which is the rectified current i in Figure 12.28.

The assumption most likely not realized in practice is that of an ideal limiting core characteristic with zero hysteresis along the H-axis. If the above analysis is carried out assuming a core characteristic such as that illustrated in Figure 12.29, we find that the average rectified output current i remains equal to $\frac{1}{n_s}[n_b I_b + I_o]$ as long as the condition

$$n_b I_b + I_o > H_c \qquad (12.51)$$

is satisfied. Hence, the excitation currents I_b and I_o must be such that their induced H would be outside the square hysteresis portion of the core characteristic. Since the PP4125 current ranges are calibrated down to zero amperes, we see that the bias current I_b

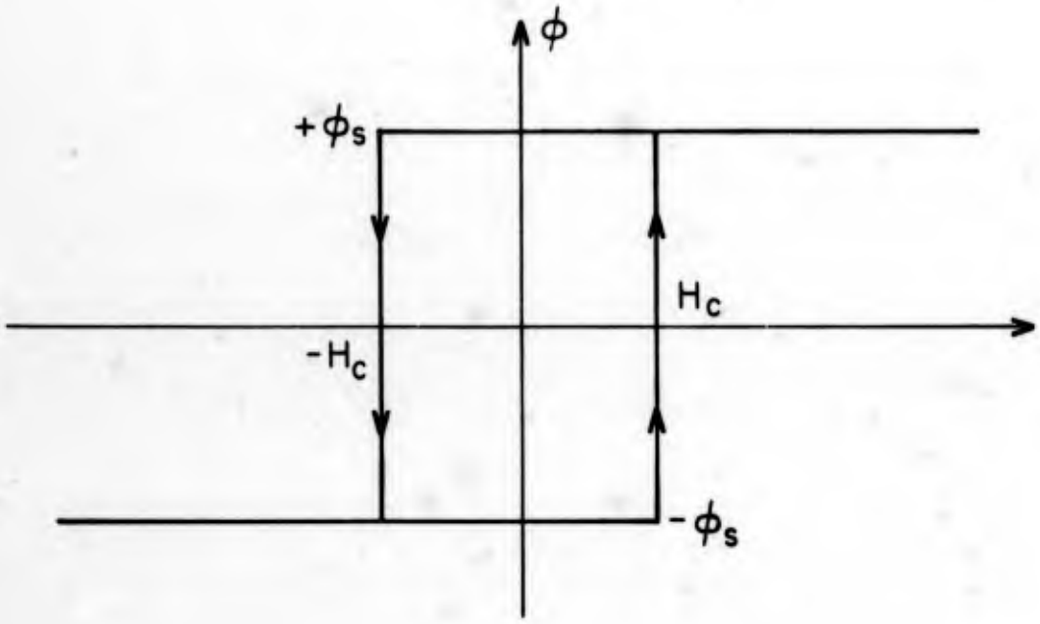


FIGURE 12.29

SATURATING CORE WITH HYSTERESIS

is necessary to satisfy Eqn. 12.51 for any output current $I_o \geq 0$, and, in fact, we may write

$$n_b I_b > H_c.$$

This bias current then permits proper operation of the current sensing over the desired output current range. Experiments made on the charger show that the turns ratios n_b and n_s on the 5 ampere range are given by

$$1:n_b:n_s = 1:59:59$$

or

$$n_b = n_s = 59.$$

The bias current I_b is approximately 9 ma, so that the output current of the bridge rectifier is then

$$i_b = \frac{1}{59} I_o + I_b$$

or

$$i_b(\text{ma}) = 17\, I_o\,(\text{amperes}) + 9. \qquad (12.52)$$

An incremental model of the current sensing circuit which gives the incremental voltage input v_i to the differential amplifier Q14 is shown in Figure 12.30. A static model which is useful in determining operating points is shown in Figure 12.31. We shall return to these models later.

Output Switch Drivers

Transistors Q8 and Q9 together with their associated circuitry provide the necessary drive to switch the output transistors Q10 and

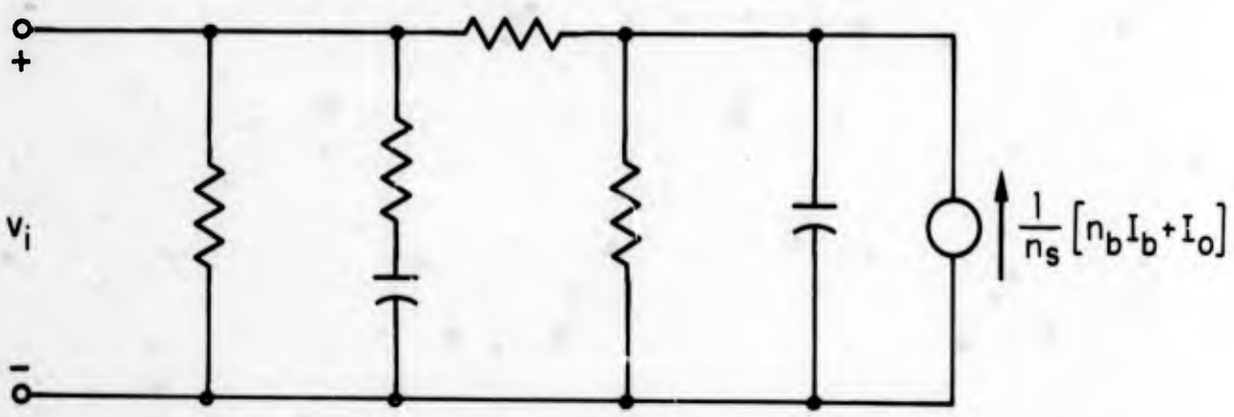


FIGURE 12.30

INCREMENTAL CURRENT SENSING MODEL

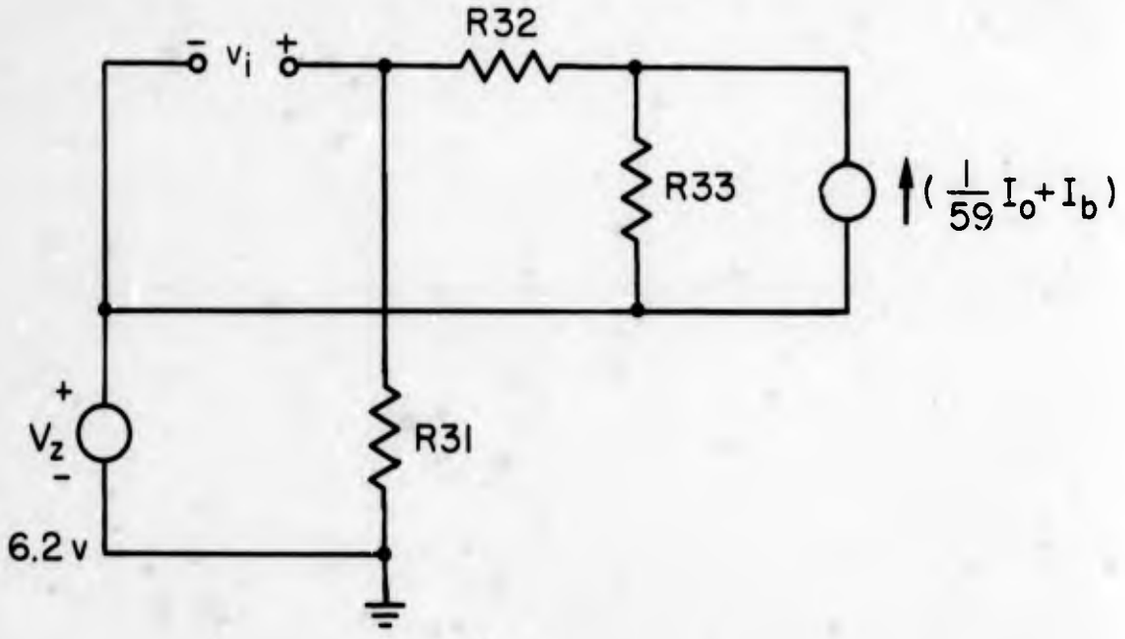


FIGURE 12.31

STATIC CURRENT SENSING MODEL

Q11. Since the two circuits are independent of one another and identical, we shall consider the operation of only one of the driver circuits.

We may note that the driver transformers T2 and T4 must be linearly operated since saturable operation would result in an uncontrolled turnoff of the output transistors. Since these transformers are linear, the output transistor base-emitter diode reflects in the primary as another diode, with voltage levels determined by the turns ratio. For the driver transformers used in the PP4125, this base-emitter drop reflects approximately as a 10 volt drop across the primary, so that the primary can be modeled as "seeing" a diode with a 10 volt barrier potential, as shown in Figure 12.32. Here L represents the finite magnetizing inductance of T4. The remaining portions of the circuit are identical to the actual schematic with the exception of driver transistor Q8, which has been modeled by the switch S.

We shall assume that S is opened and closed with given periods T_{off} and T_{on} as shown in Figure 12.33. A qualitative description of the circuit operation can be given once we assume initial states for the capacitor voltages and inductor current. At $t = 0^+$, these are shown in Figure 12.33 as V, I and V_r.

Before continuing, let us note some of the characteristics of the circuit in Figure 12.32. The time constant of C7 and R15 is one millisecond, which is much longer than the period of the switch S (which we observe runs at the inverter frequency by looking back through the magnetic amplifier). Thus, C7 cannot charge or discharge significantly through R15 in one switching period. Second, the resonant frequency of C9 and L is calculated to be much lower than the actual switching frequency, so that the variables associated with these elements will be small pieces of sinusoids, which we may assume are approximately linear ramps. With these points in mind, the waveforms in Figure 12.33 may now be sketched.

At $t = 0$, switch S is closed, grounding the lower end of the inductor L. For this condition, we have

$$L\frac{di_L}{dt} = v_L = v_c > 0$$

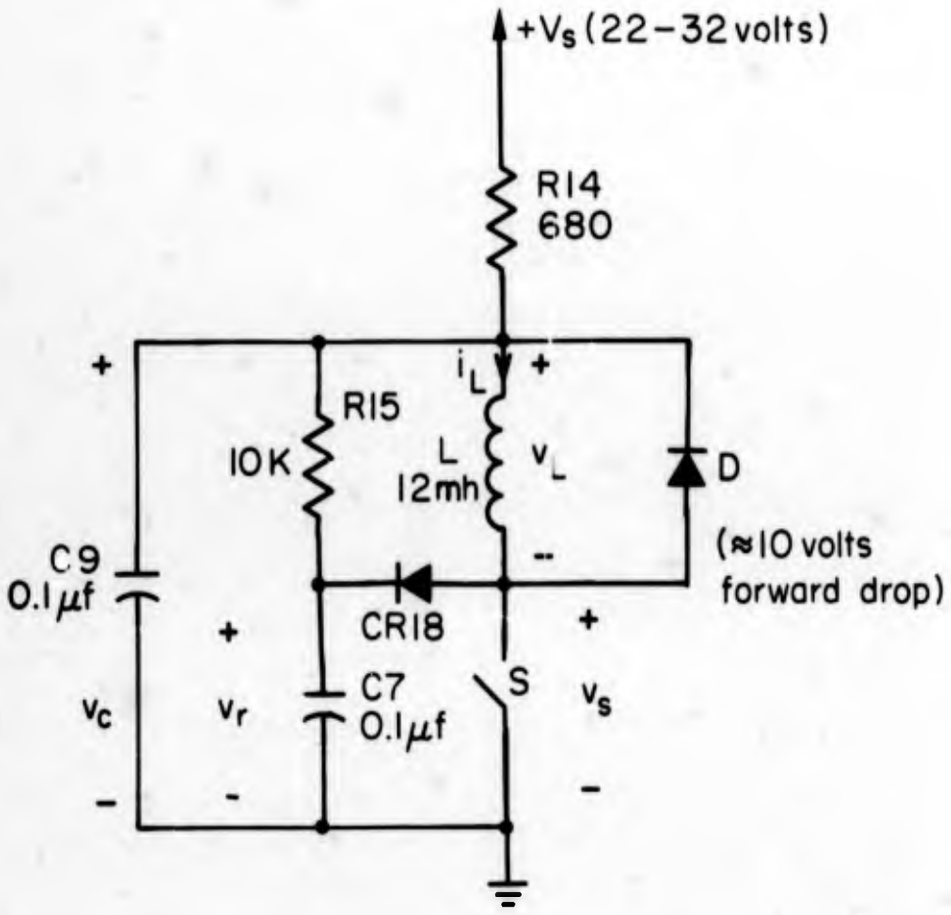


FIGURE 12.32

IDEALIZED MODEL OF DRIVER CIRCUIT

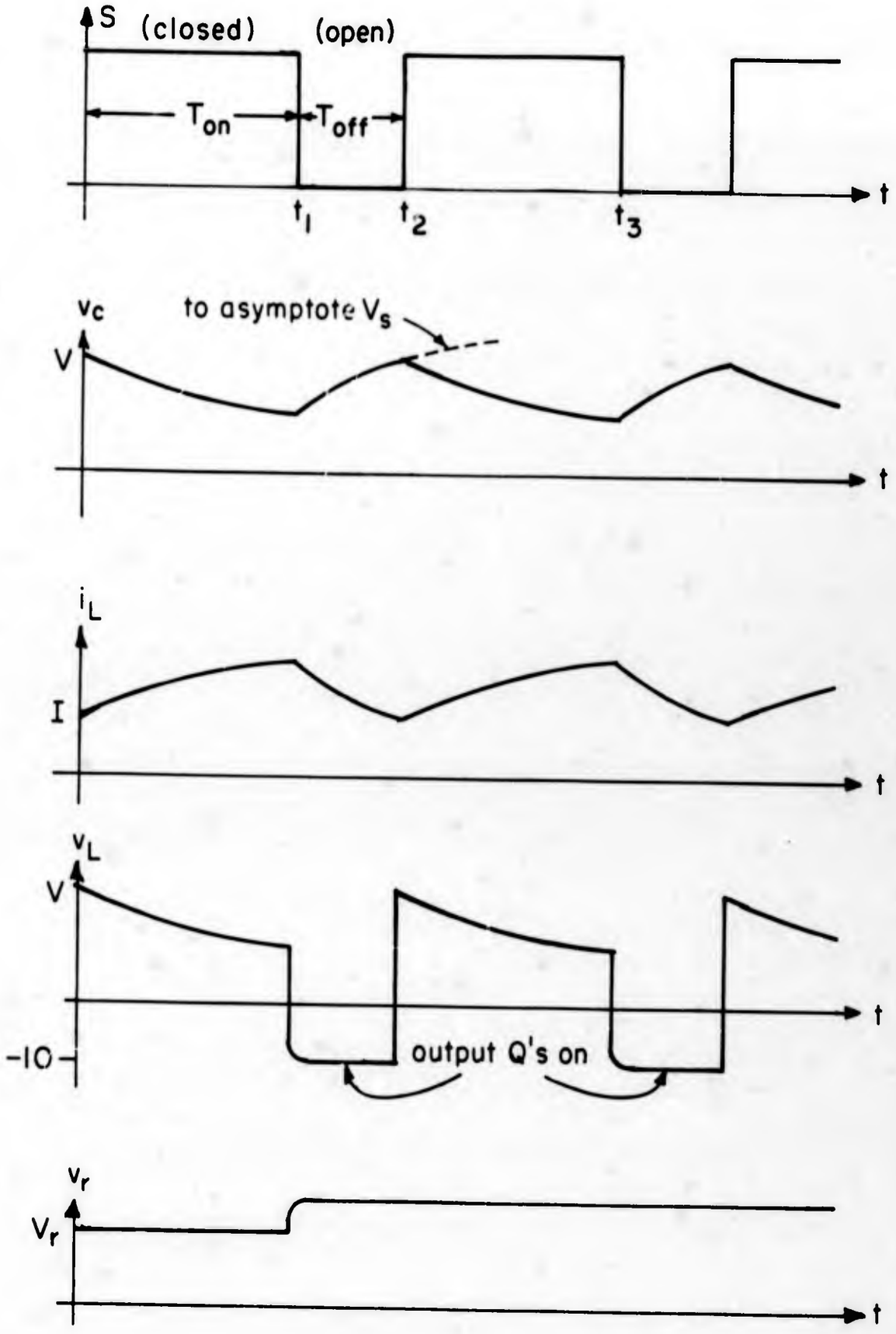


FIGURE 12.33

WAVEFORMS IN DRIVER CIRCUIT

so that i_L is increasing. Diode CR18 is reverse biased so that v_r, which can then discharge only through R15, remains essentially constant. For the moment, we shall assume that v_c is decreasing, so that the variables then continue as shown in Figure 12.33 until time t_1. During this interval, the equivalent diode D is reverse biased. Since this is the reflected base-emitter junction of the output transistor Q10, this transistor remains off during the "on" time of S.

At $t = t_1$, switch S is opened. Since i_L cannot change instantaneously, it must flow into diode CR18 or the diode D. Since D has an equivalent conducting drop of approximately 10 volts, we see from Figure 12.32 that D will conduct if $v_r - v_c > 10$ and that CR18 will conduct if $v_r - v_c < 10$. The situation illustrated shows the latter case. Here the current in L will charge C7 as shown until $v_r = v_c + 10$, at which point diode D will begin to conduct and maintain a constant 10 volt drop. During this time $v_L = -10$ and i_L is decreasing as shown while v_c charges toward V_s through R14. At this point, we should note that D does not stop conducting if i_L goes to zero or goes negative, the reason being that until now, we have neglected the feedback drive winding in the collector of the output transistor Q10. A careful study of the reflected v-i characteristic as seen at the primary of T4 will show that the current through the equivalent D can go both positive and to a certain degree negative. This feedback action keeps Q10 on until time t_2.

At $t = t_2$, S again closes and we have the constraint $v_L = v_c > 0$, so that D is forced into cutoff. This, of course, corresponds to the turnoff of the output transistor Q10. At this time, we have a situation similar to the one at $t = 0$, except the "initial" values of the cycle may now be different from those at $t = 0$.

In steady-state operation, each waveform in Figure 12.33 must be identical from cycle to cycle. If we equate the values at the end of a cycle to those at the beginning of a cycle, we can obtain the steady-state results.

In steady-state, the average value of v_L must be zero. If S is open for a fraction α of the time [i.e., the output transistor is on during this time], then we may observe that v_L and v_c have identical averages during T_{on} and that

$$\langle v_c \rangle = \frac{10\alpha}{1-\alpha} \tag{12.53}$$

where <> denotes time average. Knowing the average capacitor current is zero, we have

$$\langle i_L \rangle = \frac{1}{R14}\left[V_s - \frac{10\alpha}{1-\alpha}\right]. \tag{12.54}$$

From previous arguments, we also have

$$\langle v_r \rangle = 10 + \langle v_c \rangle.$$

The major conditions which must be satisfied in the design deal with the driver transformers T2 and T4. These must have sufficient volt-second capability on the windings so they do not saturate and the energy stored in the magnetizing inductance L at time t_1 in Figure 12.33 must be sufficient to start the turn-on feedback drive of the output transistors.

We see that an on-off drive to the driver transistors effects the switching of the output transistors, with the output transistors in the "on" state when the drivers are cut off and vice versa.

Magnetic Amplifier/Modulator

We shall now consider the operation of the modulator circuit and transformer T5. By inspection, we may make the following observations about the circuit:

1) Windings 1-2 and 5-6 "see" a pair of diodes looking into the base circuits of the driver transistors Q8 and Q9, so

that we may assume these points are short circuits if we neglect the diode barrier potentials.

2) Resistors R12 and R13 are connected between a voltage source (winding 7 - 9 of the inverter transformer) and the base circuits of the driver transistors. Since the latter are essentially short circuits, R12 and R13 will have no effect on the operation of T5.

3) Since the average voltage across winding 9 - 10 must be zero, we have the voltage across C5, which will be essentially constant, given by

$$v_{c5} = \frac{27}{27 + 6.2} \cdot 15 = 12 \text{ volts.} \qquad (12.55)$$

4) The turns ratios of T5 are such that the impedance seen at windings 3 - 4 and 7 - 8 is high compared with 200 ohms (R19), so we shall assume that the collector of Q12 is a voltage source as seen by T5. Thus, windings 3 - 4 and 7 - 8 can be modeled as seeing a voltage source with a value given by the difference between the collector voltage of Q12 and the +15 volt supply.

With these points in mind, we may construct a model of T5 and the relevant circuitry as shown in Figure 12.34. The turns ratios shown and the ϕ-H characteristic of the cores were determined from laboratory measurements. The voltages v_1 and v_2 are given by

$$v_1 = \frac{d\phi_1}{dt}, \quad v_2 = \frac{d\phi_2}{dt}. \qquad (12.56)$$

The source $v_a(t)$ is a model of the inverter winding 7 - 8 - 9 and the source V is the voltage between the collector of Q12 and the +15 volt supply.

Before proceeding further, let us note from Figure 12.34 that CR12 constrains v_1 by

$$5.5\, v_1 \leq V$$

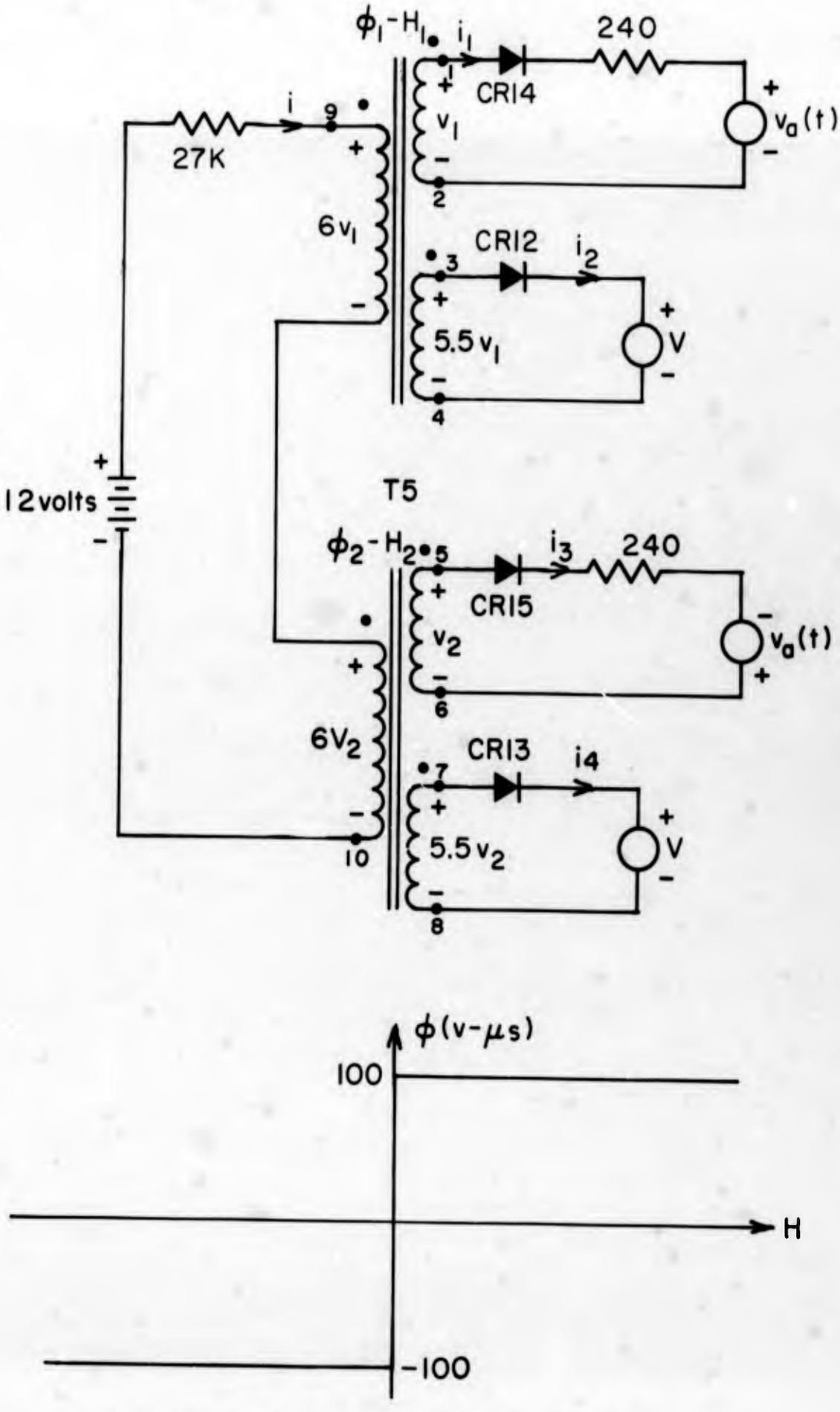


FIGURE 12.34 MODEL OF MAGNETIC AMPLIFIER

and by taking time averages, we obtain

$$5.5 \langle v_1 \rangle \leq V.$$

In steady-state operation, the average voltage across any winding must be zero. Therefore, since $\langle v_1 \rangle = 0$, we have the result that V must be positive in steady-state operation, i.e., the collector of Q12 is always above the +15 volt bus.

We may write the equations describing the cores as

$$H_1 = 6i - i_1 - 5.5i_2 \tag{12.57}$$

$$H_2 = 6i - i_3 - 5.5i_4 \tag{12.58}$$

$$\phi_k = \begin{cases} +100(v-\mu s), & H_k > 0 \\ -100(v-\mu s), & H_k < 0, \end{cases} \tag{12.59}$$

$$H_k = 0, \qquad -100 < \phi_k < +100. \tag{12.60}$$

The constraints placed by the circuitry external to T5 can be written as follows, where currents are understood to be in milliamperes:

$$6v_1 + 6v_2 + 27i = 12 \tag{12.61}$$

$$\left.\begin{array}{ll} v_1 = .25i_1 + v_a, & i_1 > 0 \\ i_1 = 0, & v_1 < v_a \end{array}\right\} \tag{12.62}$$

$$\left.\begin{array}{ll} v_1 = .18V, & i_2 > 0 \\ i_2 = 0, & v_1 < .18V \end{array}\right\} \tag{12.63}$$

$$\left.\begin{array}{ll} v_2 = .25i_3 - v_a, & i_3 > 0 \\ i_3 = 0, & v_2 < -v_a \end{array}\right\} \tag{12.64}$$

$$\left.\begin{array}{ll} v_2 = .18V & i_4 > 0 \\ i_4 = 0 & v_2 < .18V \end{array}\right\}. \qquad (12.65)$$

Given $v_a(t)$ and V, we shall use the method of assumed states to find a consistent solution to the above equations. This consists of specifying the initial state of the cores (the fluxes ϕ_1 and ϕ_2 here) and assuming certain conditions about the variables. The correct assumptions will be consistent with <u>all</u> of the above equations. Since we also desire a steady-state solution, at any time, we require the state of each variable in the network to be identical to its value at the corresponding time in the previous period. In the present case, due to the symmetry of the situation, we need only follow the waveforms for one-half cycle, at which time the roles of symmetric variables should be reversed. For example, if the inverter output $v_a(t)$ has a period T, we require that

$$\left.\begin{array}{l} \phi_1(t + \frac{T}{2}) = \phi_2(t) \\ \phi_2(t + \frac{T}{2}) = \phi_1(t) \end{array}\right\} \qquad (12.66)$$

with similar equations relating the variable pairs $v_1 - v_2$, $i_1 - i_3$, and $i_2 - i_4$.

When using the method of assumed states, a number of incorrect states may be tried before one that is consistent with all the network constraints is found. In the following work, the trial assumptions which turned out to be incorrect (and there were some) will not be recorded. Only those which yield the correct solution will appear here.

We shall start out analysis by assuming that core 1 is saturated in the negative direction and that core 2 has a nonsaturating flux of ϕ. At $t = 0$, $v_a(t)$ switches to +4 volts. If the equivalent source $V < 22$ (which laboratory observations confirm), then Eqn. 12.63 tells us that $v_1 < 4$ volts. Thus, with $v_a = 4$ and $v_1 < 4$, we have $i_1 = 0$. From Figure 12.34, we may expect that $i_3 > 0$ with v_a positive and

that $v_2 < 0$. With this assumption, we have from Eqn. 12.65 that $i_4 = 0$. Since we have assumed that ϕ_2 is not at saturation, we have $H_2 = 0$. The remaining assumption to be made concerns core 1. We shall assume that $v_1 > 0$, since ϕ_1 can only increase, and $H_1 = 0$. This leads us to believe that $i_2 \neq 0$. Listing these assumptions, we have

$$\left.\begin{aligned} &i_1 = 0, \\ &i_2 > 0, \\ &v_1 > 0, \\ &v_2 < 0, \\ &i_4 = 0, \\ &H_1 = 0 = H_2. \end{aligned}\right\} \qquad (12.67)$$

Equations 12.57 - 12.65 then become

$$6i = 5.5i_2,$$

$$6i = i_3,$$

$$6v_1 + 6v_2 + 27i = 12,$$

$$v_1 = .18V,$$

$$v_2 = .25i_3 - 4,$$

These have the solutions

$$\left.\begin{aligned} v_1 &= .18V, \\ v_2 &= -(2.5 + .045V), \\ i &= 1 - .03V, \\ i_1 &= 0 = i_4, \\ i_2 &= 1.1 - .033V, \\ i_3 &= 6 - .18V \end{aligned}\right\} \quad 0 < t < t_1 \qquad (12.68)$$

which are consistent with Eqn. 12.67. We also have ϕ_1 and ϕ_2 given by

$$\phi_k = \phi_k(0) + \int_0^t v_k dt$$

so that v_1 and v_2 are the slopes of ϕ_1 and ϕ_2 respectively. The plots of ϕ_1, ϕ_2, v_1 and v_2 are shown in Figure 12.35.

At $t = t_1$, we assume that core 2 saturates so that $\phi_2 = -100$, $v_2 = 0$, and $H_2 < 0$. With $v_2 = 0$, we may write, noting that core 1 is not saturated,

$$\left.\begin{aligned} i_4 &= 0, \\ i_3 &= \frac{4}{.25} = 16, \\ i_1 &= 0, \\ H_1 &= 0, \\ H_2 &< 0. \end{aligned}\right\} \qquad (12.69)$$

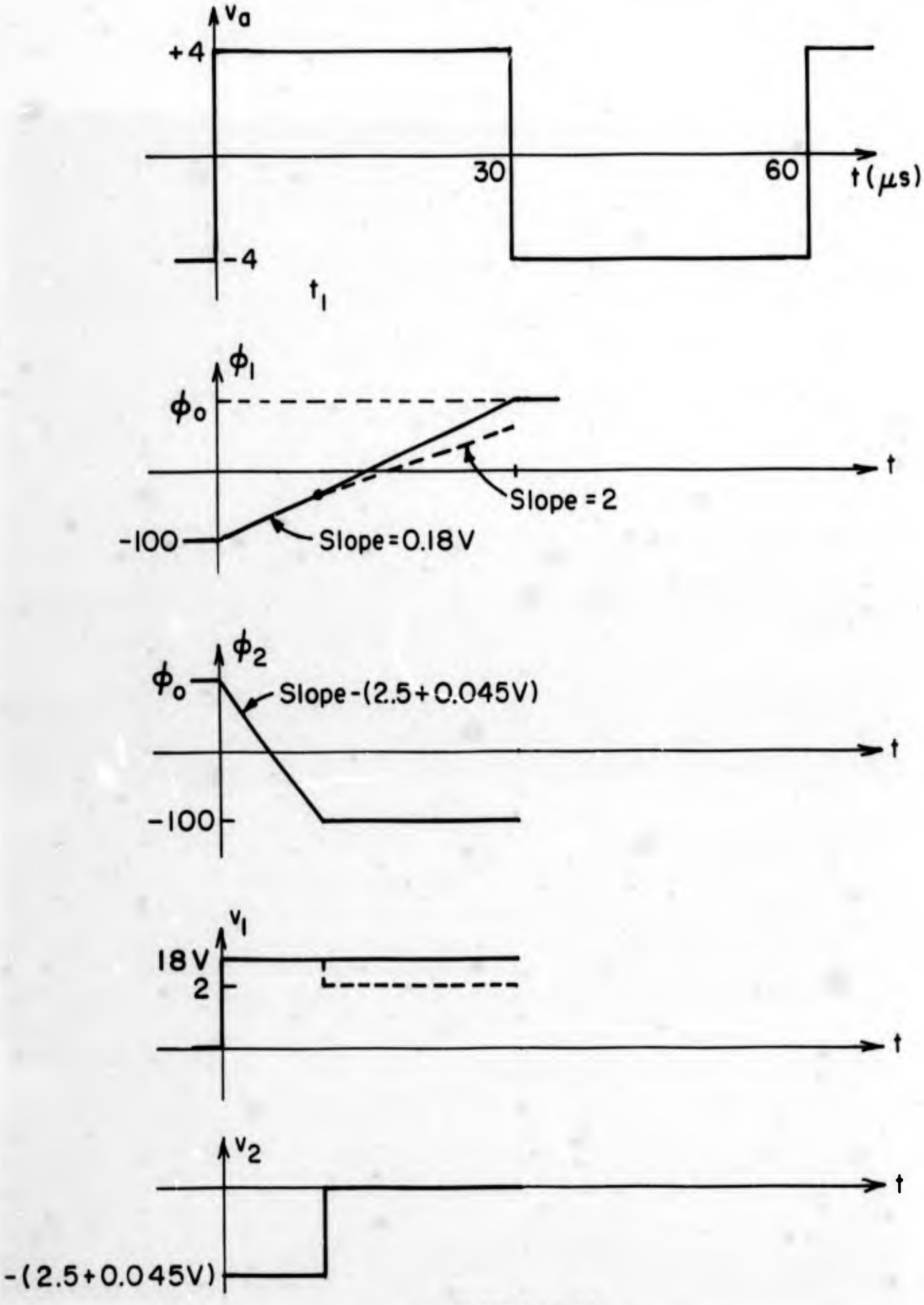


FIGURE 12.35

WAVEFORMS IN MAGNETIC AMPLIFIER

We must make another assumption here concerning v_1 and i_2. Since v_a is still positive, i_1 remains zero. However, we may assume that either $5.5v_1 = V$ and $i_2 > 0$ or that $5.5v_1 < V$ and $i_2 = 0$. If Eqns. 12.57 - 12.65 are solved with either of these assumptions, a consistent solution can be found, but only for certain values of V. These two sets of solutions are

$$\left.\begin{aligned} &i = 0.45 - 0.04V, \\ &i_1 = 0 = i_4, \\ &i_2 = 0.5 - 0.044V, \\ &i_3 = 16, \\ &v_3 = 0.18V, \\ &v_2 = 0. \end{aligned}\right\} \quad \begin{aligned} &t_1 < t < 30\ \mu s \\ &V \leq 11.1 \text{ volts} \end{aligned} \qquad (12.70)$$

$$\left.\begin{aligned} &i = 0, \\ &i_1 = i_2 = i_4 = 0, \\ &i_3 = 16, \\ &v_1 = 2, \\ &v_2 = 0. \end{aligned}\right\} \quad \begin{aligned} &t_1 < t < 30\ \mu s \\ &V \geq 11.1 \text{ volts} \end{aligned} \qquad (12.71)$$

One of these solutions will be valid until $t = 30\ \mu s$, when $v_a(t)$ reverses sign.

Since we desire the steady-state solution, the symmetry of the circuit requires that at $t = T = 30\ \mu s$, the states of the two cores be reversed from those at $t = 0$. We see from Figure 12.35 that

$\phi_2(T) = \phi_1(0)$. We also require that $\phi_1(T) = \phi_2(0) = \phi_o$. Equating the changes in the flux in each core, we have for $V < 11.1$,

$$(2.5 + .045V)t_1 = (.18V)\ 30,$$

or

$$t_1 = \frac{5.4V}{2.5 + .045V}\ \mu s, \qquad V \leq 11.1 \tag{12.72}$$

and for $V \geq 11.1$,

$$(2.5 + .045V)t_1 = (0.18V)t_1 + 2\cdot(30 - t_1),$$

or

$$t_1 = \frac{60}{4.5 - 0.135V}\ \mu s, \qquad V \geq 11.1. \tag{12.73}$$

The drive current i_{b1} to transistor Q8 is the sum of two components - the current i_1 above and the current in resistor R13. Similarly, the drive current i_{b2} to Q9 is the sum of i_3 and the current in R12. These components are shown in Figure 12.36.

From the analysis of the drive circuits, we know that an output transistor will be conducting when the corresponding driver transistor is cut off. We can see from Figure 12.36 that the "off" times of the drivers alternate, so that one of the output transistors will be conducting when either of the drivers is cut off. There are two observations which can be made at this point. One is that the output transistors <u>do not</u> operate in parallel, but alternate instead. Second, the output stage duty cycle D is given by that fraction of the time that at least one output transistor is conducting. From Figure 12.36, we see that

$$D = \frac{t_1\ (\mu s)}{30\ \mu s}. \tag{12.74}$$

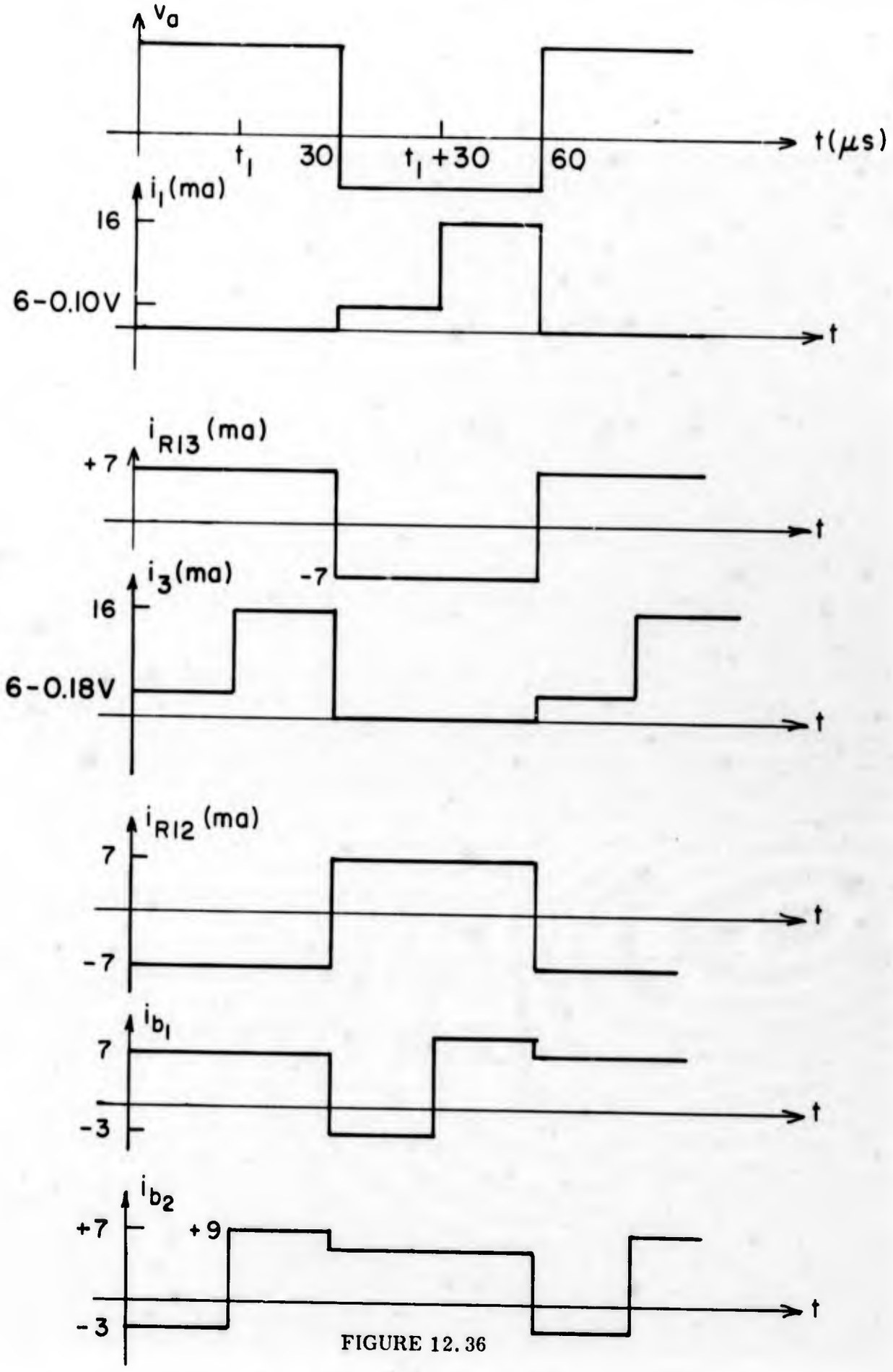


FIGURE 12.36

DRIVE CURRENT WAVEFORMS

Using Eqns. 12.72 and 12.73, we then obtain for the magnetic amplifier/ modulator control characteristic

$$D \simeq \begin{cases} \dfrac{4V}{55 + V}, & 0 < V < 11 \\ \dfrac{15}{33 - V}, & 11 < V < 18, \end{cases} \qquad (12.75)$$

which is depicted in Figure 12.37.

The two modes of operation which are predicted by Eqn. 12.75 are observed in practice, although the quantitative agreement is not very accurate. However, the fact that a dual mode nature is predicted and observed lends credence to the validity of the qualitative description. The lack of numerical agreement is most likely a result of the crude models used. Better quantitative results would require more detailed and practical models.

The question we may ask here is whether this dual mode operation is detrimental to operation, and if it is, whether the design can be modified to eliminate the problem. The predicted change in incremental gain across the boundary of the two regions is approximately 40%. The actual characteristic, shown in Figure 12.38, exhibits a negative slope in the middle region of the characteristic. Again, this is probably due to the nonideal nature of the core characteristic. The particular unit tested did not seem to be adversely affected by this nonlinear characteristic, but more information concerning component tolerances would be needed to ensure proper operation.

The dynamic characteristics of the magnetic modulator are not easily found analytically due to the quite nonlinear behavior of the circuit. For this analysis, the dynamic modulator characteristics were determined by a number of laboratory experiments. The results of these tests are shown in Figures 12.39 and 12.40. The large signal response of the modulator is shown in Figure 12.39. Here we can see that for an excitation frequency of 300 Hz, the response, although nonlinear, is essentially instantaneous. The exposure was made so that the instantaneous duty cycle is the envelope of the lower trace. The small signal response of the modulator to a 200 Hz input

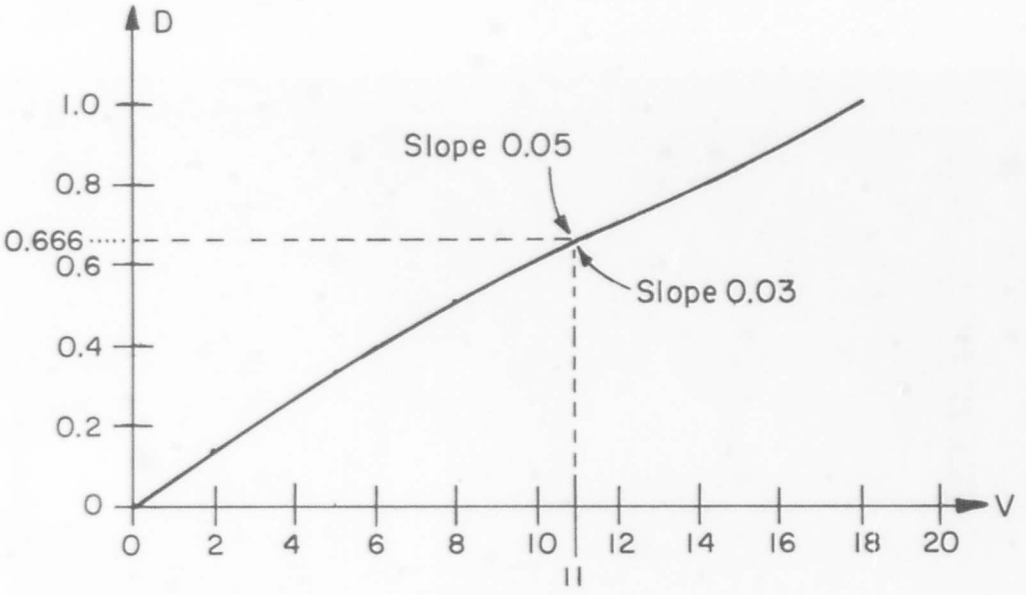
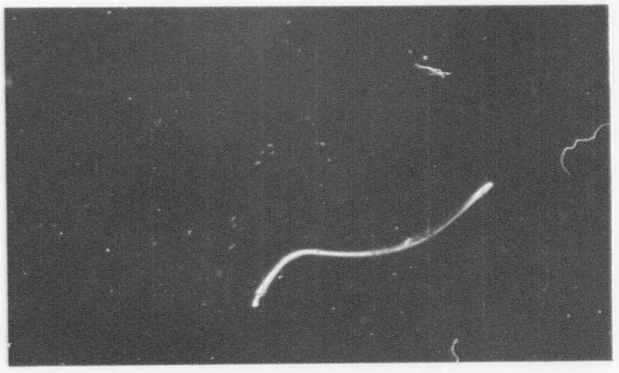


FIGURE 12.37

PREDICTED STATIC CONTROL CHARACTERISTIC



HORIZONTAL:

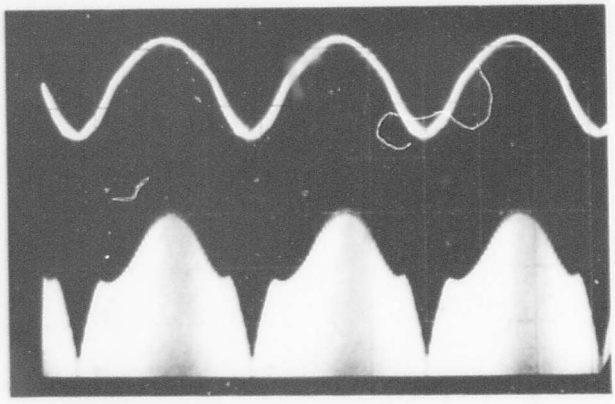
Control Voltage
4 volts/cm

VERTICAL:

Duty Cycle
0.2/cm

FIGURE 12.38

OBSERVED STATIC CONTROL CHARACTERISTIC



UPPER TRACE:

Control Voltage
10 volts/cm

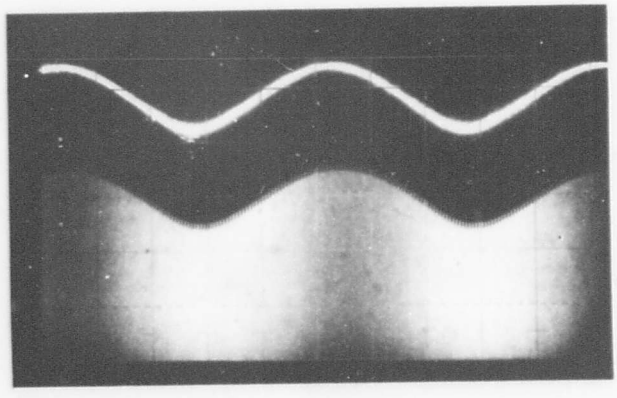
LOWER TRACE:

Duty Cycle 0.2/cm

HORIZONTAL: 1 ms/cm

FIGURE 12.39

LARGE-SIGNAL DYNAMIC CHARACTERISTIC OF MAGNETIC MODULATOR



UPPER TRACE:

Control Voltage
5 volts/cm

LOWER TRACE:

Duty Cycle 0.2/cm

HORIZONTAL: 1 ms/cm

FIGURE 12.40

SMALL-SIGNAL DYNAMIC CHARACTERISTIC OF MAGNETIC MODULATOR

is shown in Figure 12.40. Here we see that the system is incrementally linear and that no phase shift is exhibited at the test frequency. Since very low frequency cutoff filters are used previous to the magnetic amplifier, we may assume that it can be described, both statically and dynamically, by the control relation in Figures 12.37 and 12.38.

The remaining characteristic we should like to know is the v-i characteristic of the magnetic modulator as seen at the collector of Q12. Eqns. 12.68, 12.70 and 12.71 predict that the average terminal current at the collector of Q12 will be constant independent of the control voltage V. In the device tested, the input characteristic had a 25K ohm incremental impedance and not infinite impedance. An equivalent circuit of the magnetic amplifier, including R19 and C14, as seen by the collector of Q12 is shown in Figure 12.41. The duty cycle is then a function of the terminal voltage as previously derived.

Error Amplifier

The control signal for the modulator is supplied from the amplifier consisting of Q12, Q13, Q14 and the associated circuitry. We observe that it is a two stage differential amplifier followed by a single-ended output stage as shown in Figure 12.42.

A simplified model of this circuit is shown in Figure 12.43. The approximations which have been made here are:

1) The 20K emitter resistor, R26, has been replaced by a current source of 280 μa, the current being determined from the operating point set by CR23.

2) Resistors R_a and R_b include R29 and also the equivalent emitter resistance of Q14. At the existing operating point, we have $R_a + R_b = 560$ ohms. Since the potentiometer R29 has a value of 200 ohms, R_a and R_b are also constrainted by $180 < R_a < 380$, $180 < R_b < 380$.

3) Resistors R23 and R24 have been replaced by a Thevenin equivalent so that Q13 effectively "sees" an 11.4 volt source behind 370 ohms as shown.

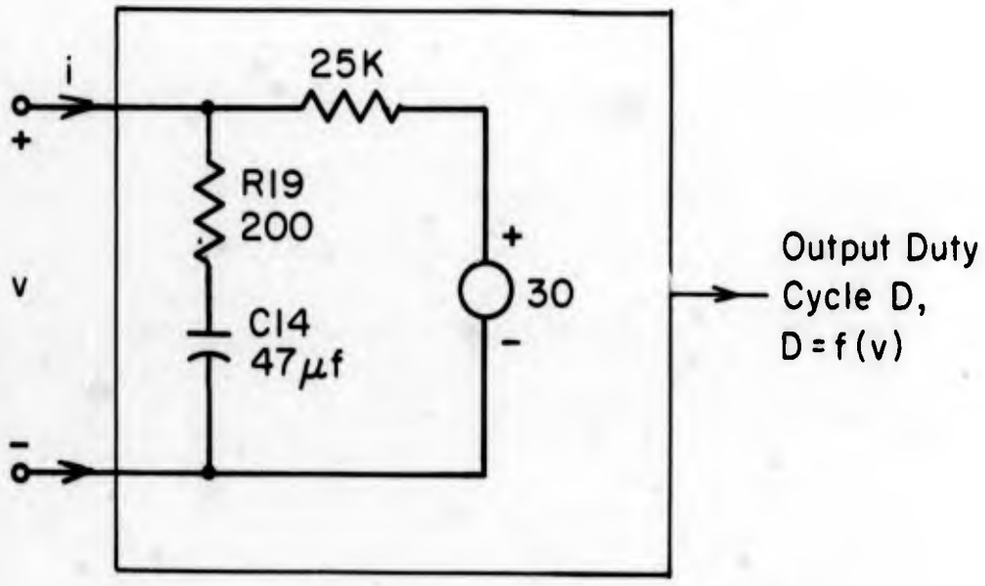


FIGURE 12.41

EQUIVALENT MODEL OF MAGNETIC AMPLIFIER INPUT

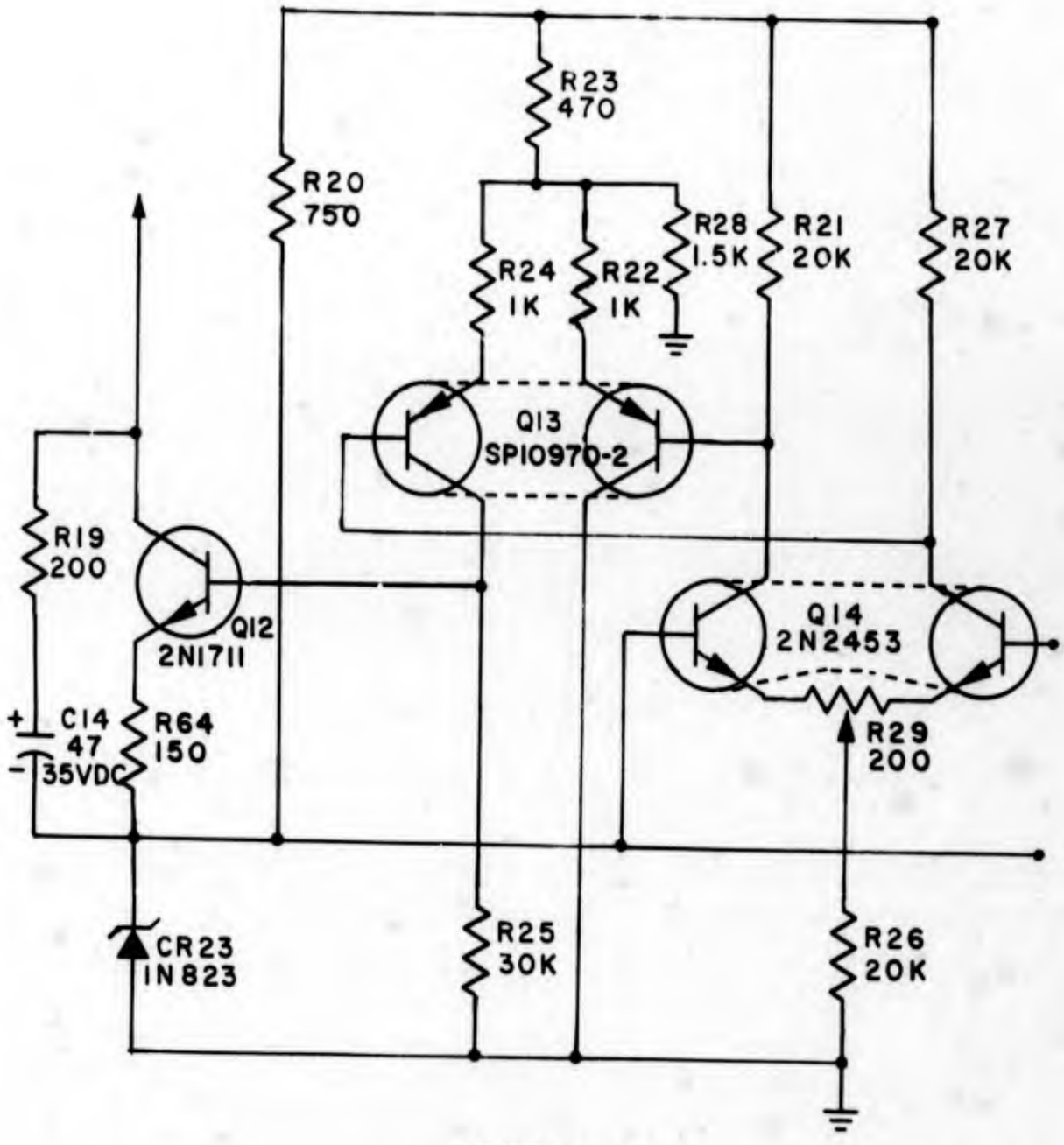


FIGURE 12.42

ERROR AMPLIFIER

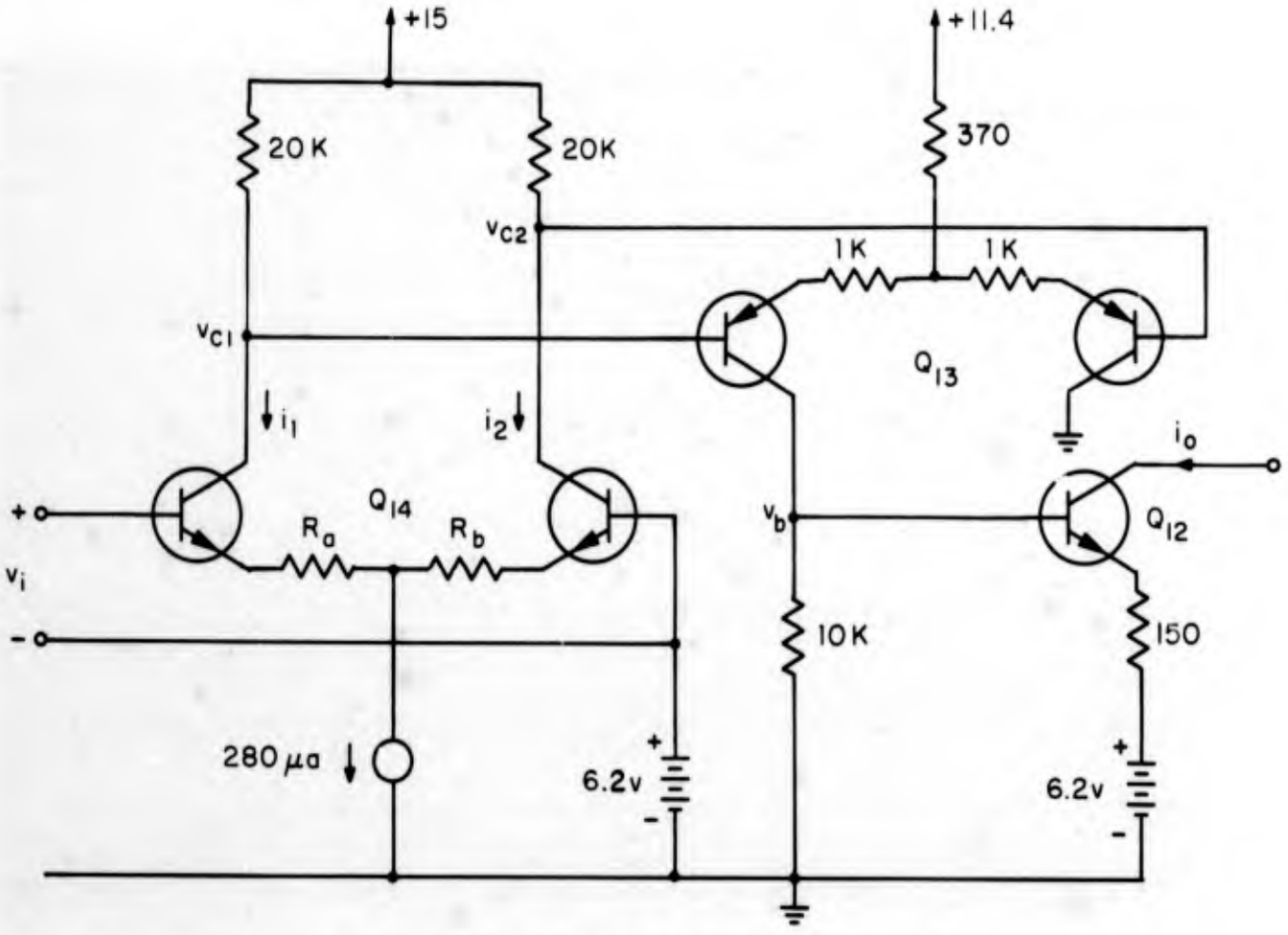


FIGURE 12.43 SIMPLIFIED MODEL OF ERROR AMPLIFIER

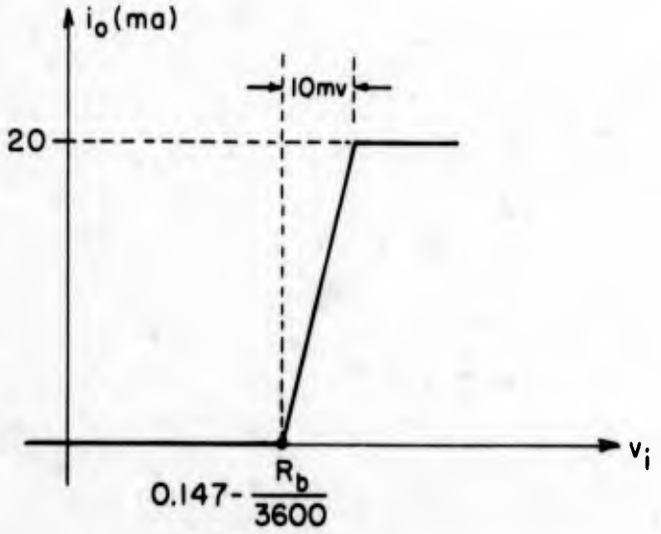


FIGURE 12.44 TRANSFER CHARACTERISTIC OF ERROR AMPLIFIER

4) With the specified gain for a 2N1711, the emitter resistor R64 reflects into the base of Q12 as approximately 15K ohms. Combined with R25, this results in an equivalent collector load for Q13 of approximately 10K ohms. We may now treat Q12 as if it had an infinite input impedance, since the effect of its finite impedance is modeled in the Q13 collector load.

With reference to Figure 12.43, we see that if $i_1 = i_2 = 140\ \mu a$, then $v_{c1} = v_{c2} = 12.2$ volts. Also, for any i_1 and i_2, we have $\frac{1}{2}(v_{c1} + v_{c2}) = 12.2$ since $(i_1 + i_2)$ is constant. Thus, either v_{c1} or v_{c2} will be above 12.2 volts, which we then see will always keep one half of Q13 cut off since its effective emitter supply is only 11.4 volts. The conditions of interest are those for which the left half of Q13 will be cut off, so that Q13 acts like a single transistor with a 1370 ohm emitter resistor. Now, we write the second constraint on the currents i_1 and i_2 - the Kirchoff voltage equation around v_i and the emitter of Q14. Assuming the base-emitter voltages cancel, we have

$$R_a i - R_b i_2 = v_i \tag{12.76}$$

and again

$$i_1 + i_2 = 0.280 \text{ ma} \tag{12.77}$$

$$R_a + R_b = 560. \tag{12.78}$$

These yield

$$i_1(\text{ma}) = 1.8 v_i + \frac{R_b(\Omega)}{2000} \tag{12.79}$$

which, in turn, gives the result

$$v_{c1} = 15 - 36 v_i - \frac{R_b}{100} \tag{12.80}$$

The desired transfer characteristic is the transfer admittance $\frac{i_o}{v_i}$. Allowing 0.7 volts as the base-emitter drop of Q12, we see that Q12 will be cut off if $v_b < 6.9$. The condition that $v_b > 6.9$ corresponds to the conditions $v_{c1} < 9.7$. When $v_{c1} < 9.3$, then Q13 will will be saturated and $v_b \simeq 10$. Thus, the equivalent region at the input is

$$0.157 - \frac{R_b}{3600} > v_i > 0.147 - \frac{R_b}{3600} . \tag{12.81}$$

Since

$$i_o(ma) = 6.7\,(v_b - 6.9), \tag{12.82}$$

we may write

$$i_o(ma) = \begin{cases} 0, & v_i < 0.147 - \frac{R_b}{3600} \\ 2000\left[v_i - \left(0.147 - \frac{R_b}{3600}\right)\right], & 0.147 - \frac{R_b}{3600} < v_i < 0.157 - \frac{R_b}{3600} \\ 20, & v_i > 0.157 - \frac{R_b}{3600} \end{cases} \tag{12.83}$$

This relation is plotted in Figure 12.44.

Now let us consider the static current sensing model shown in Figure 12.31. The differential input voltage v_i determined from this model is

$$v_i = \frac{R31 \cdot R33 \cdot \left[\frac{1}{59}\, I_o + I_b\right] - (R32 + R33)V_z}{R31 + R32 + R33} \tag{12.84}$$

This result together with Eqns. 12.75, 12.83 and the model in Figure 12.41 contains sufficient information to allow us to derive the static modulator duty cycle D versus output current I_o characteristic. This result has the general form shown in Figure 12.45. The distance I_a is given by the functional form

$$I_a = a\frac{R32}{R33} + \frac{b}{R33} + cR_b \qquad (12.85)$$

where a, b and c are constants. Resistor R32 sets the desired output current, so we can see that R33 alters the scale factor associated with the R32 setting. Given a value of R33 which yields the correct scale factor, R_b, which is actually part of the "balance" potentiometer R29, can be set to yield the desired offset when R32 is set at the zero ampere output position. The nominal setting for R33 is approximately 33 ohms, and we shall use this value in the following work. With this value, I_a is given approximately by

$$I_a \text{ (amperes)} = 3 \cdot R_{32}(k\Omega) \qquad (12.86)$$

for the 5A current range.

12.3 TERMINAL PROPERTIES OF THE BASIC POWER CONVERTER

The chopper output stage used here has a quasi-static equivalent source v_e given by $v_e = V_s \cdot D$ as shown in Figure 12.46. We may construct a static model of the basic power converter as shown in Figure 12.47. Using the characteristics in Figures 12.45 and 12.46, we derive an equivalent model in the active region as shown in Figure 12.48. The load regulation characteristics can be deduced from this model and also the static operating point for any given load. The approximate incremental output impedance ranges over 44 - 64K ohm, depending on the value of the source voltage V_s.

We can construct a small signal dynamic model by using the dynamic models determined above in the analyses of the current sensing,

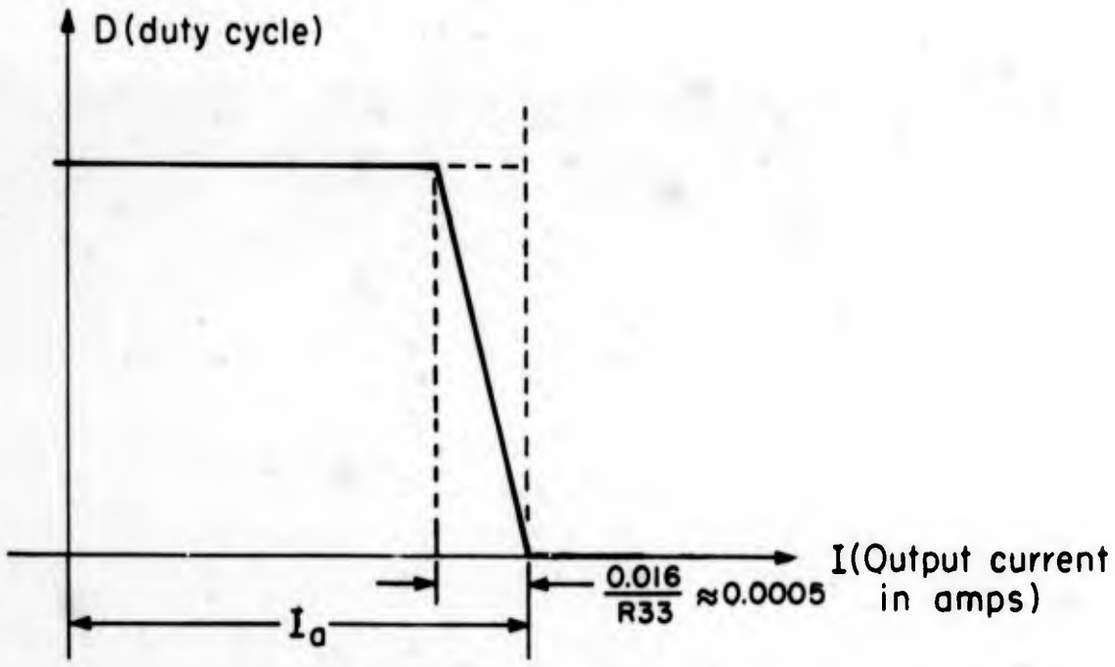


FIGURE 12.45

STATIC CONTROL CHARACTERISTIC

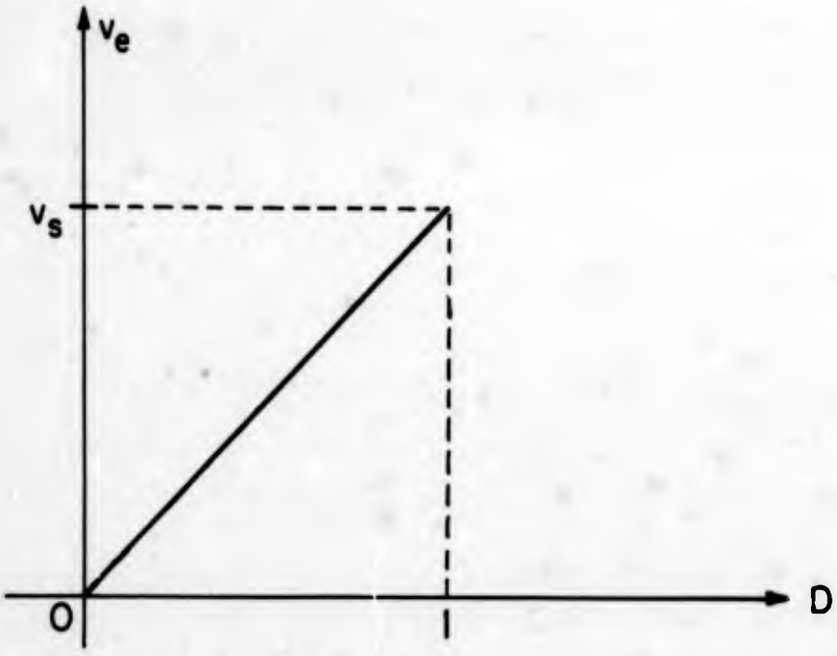


FIGURE 12.46

QUASI-STATIC CHOPPER CHARACTERISTIC

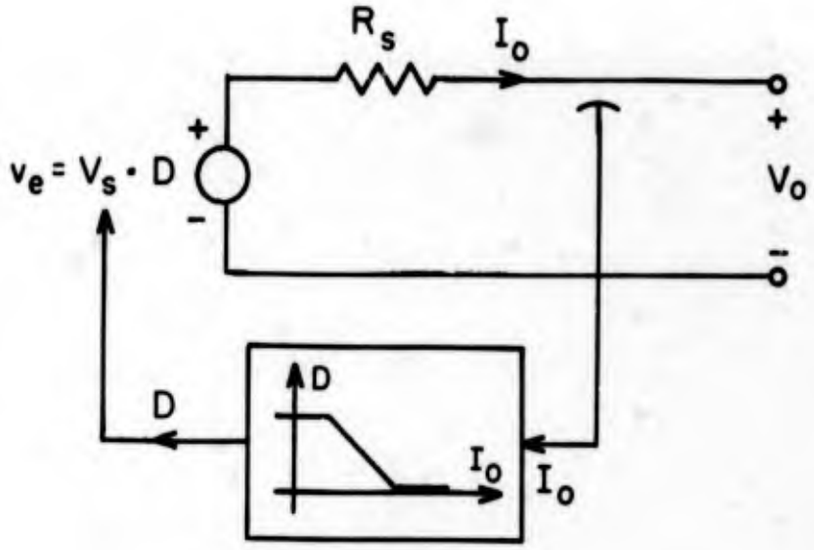


FIGURE 12.47

STATIC MODEL OF THE BASIC POWER CONVERTER

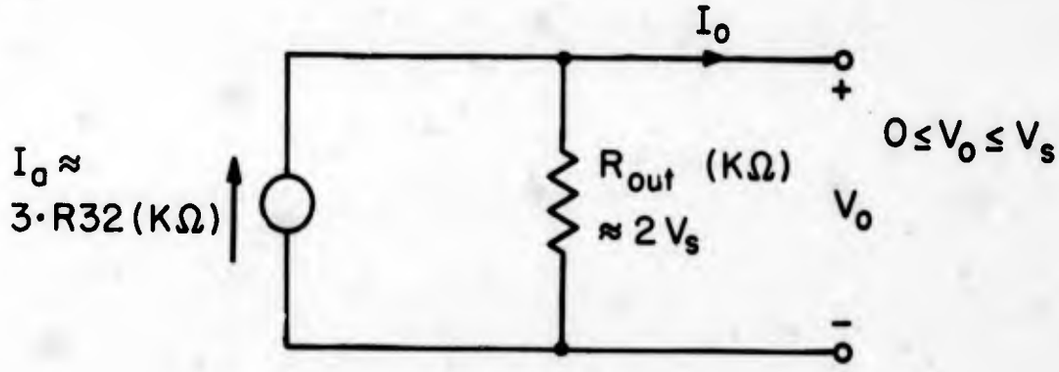


FIGURE 12.48

STATIC EQUIVALENT

the magnetic amplifier and the output stage. Putting these together, we obtain the model shown in Figure 12.49. In this model, the current sensing has been placed to the left of the output R_s-L elements rather than to the right, where it actually is in the device with no change in behavior since it still senses the current in the series R_s-L. The parameter R is the value of the current set resistor R32, which we see may affect the dynamic behavior of the system. The constant A is the slope of the D-V characteristic in Figure 12.37 at the particular dc operating point of interest. As the operating point changes, A may vary from 0.007 to 0.1 and we shall consider this range in our analysis where necessary.

That part of the network to the left of aa' in Figure 12.49 can be replaced by a Thevenin equivalent network. In this case, since there is no independent source, the equivalent model will be a linear impedance as shown in Figure 12.50, where

$$\frac{V_1}{I}(s) = Z_o(s). \tag{12.87}$$

If we let H(s) denote the transfer impedance function from I to V_e in Figure 12.49, then

$$H(s) = \frac{V_e}{I_1}$$

Since $V_1 = V_e$, we have from Eqn. 12.87 that

$$Z_o(s) = H(s) \tag{12.88}$$

so the output impedance as seen looking back from aa' is just the transfer function of the feedback loop. One observation we may make immediately is that the stability of the system should be independent of the loop gain, since the gain acts only to scale the resulting impedance. Stability of this model will be determined solely by the pole-zero pattern of the feedback transfer H(s).

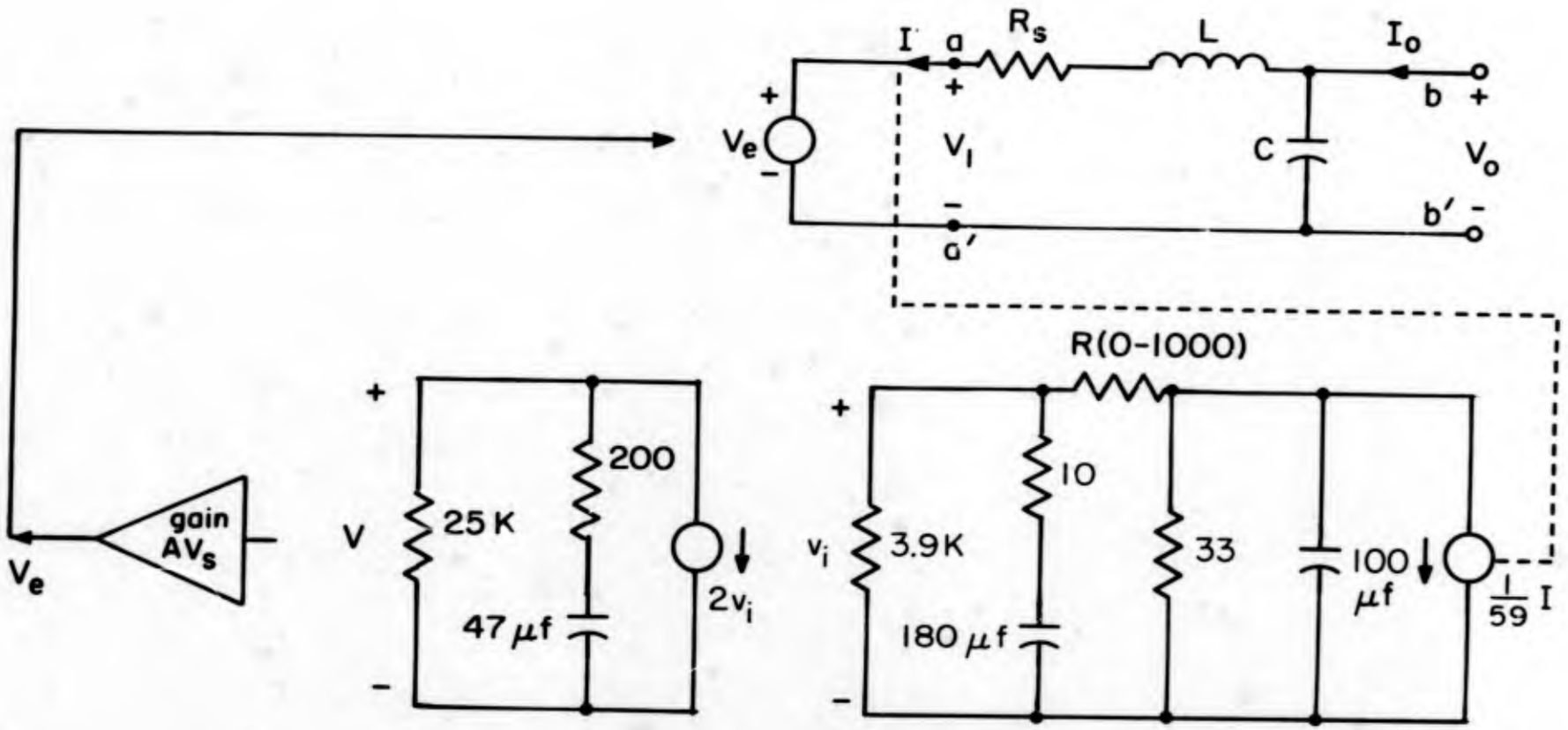


FIGURE 12.49

SMALL SIGNAL DYNAMIC MODEL OF THE BASIC POWER CONVERTER

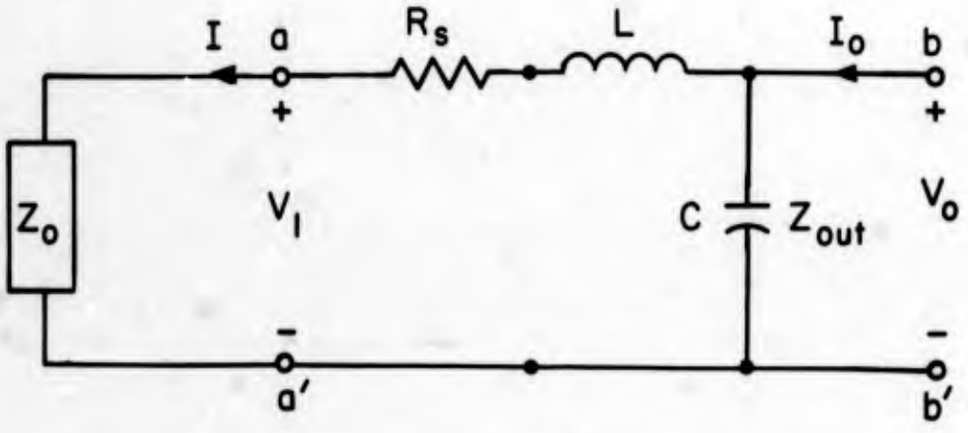


FIGURE 12.50

EQUIVALENT DYNAMIC MODEL OF THE BASIC POWER CONVERTER

The calculated impedance looking back from aa' is given by

$$Z_o(s) = K \frac{(s + 557)(s + 100)}{(s + 0.8)\,[.007(R + 0.1)s^2 + (2.11R + 1.3)s + 3R + 118]}$$

where K is a positive constant whose magnitude we have just seen will not affect the stability of the system. As was shown in Chapter 10, the system will be unconditionally stable if the impedance $Z_o(s)$ is passive. If we perform a test for passive character on Eqn. 12.89, we find that $Z_o(s)$ is passive for $R < 50$ ohms (approximately) and active for $R > 50$ ohms. Therefore, the system is potentially unstable for the condition $R > 50$, even though <u>all</u> of the poles of $Z_o(s)$ remain in the left half-plane for the entire range of R (0-1000 ohms). This range of R corresponds to an output current setting greater than 1/20 of full-scale current, full-scale current being 3 amperes on the 5 ampere range.

Tests on the unit with battery or resistive loads showed no signs of instability. However, a certain class of inductive loads did cause oscillations, some of which were severe enough to cause the polarity and run relays to operate, which resulted in a relaxation mode of oscillation.

The calculated region of potential instability is most likely not quantitatively accurate, although such a region obviously exists. One factor affecting our results is the presence of the series resistance R_s in Figure 12.49. Since we can only make measurements at the V_o-I_o port, the fact that the system is potentially unstable for certain frequencies means that

$$R_s + \mathrm{Re}[Z_o(j\omega)] < 0 \qquad (12.90)$$

for some range of ω.

Some insight into the nature of the problem can be gained by considering the behavior of the output impedance $Z_{out}(s)$ (at the battery charger terminals) in the s-plane away from the $j\omega$-axis. Figure 12.51 shows a possible real part of the output impedance for

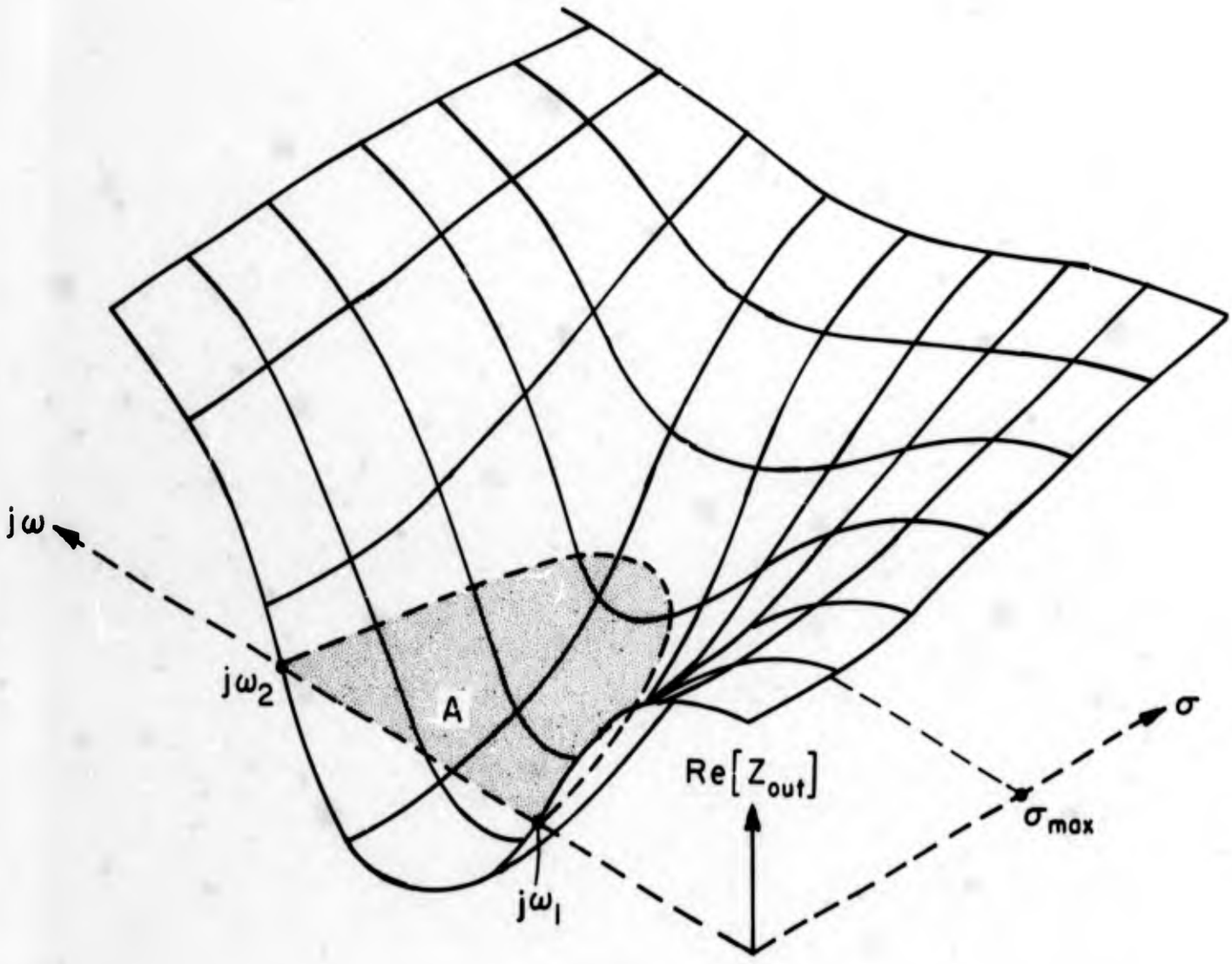


FIGURE 12.51

REAL PART OF $Z_{OUT}(S)$

first-quadrant values of the complex frequency s. We can see that for some region in the right half-plane, $Re[Z_{out}(s)] < 0$.

If an impedance $Z_L(s)$ is connected to a device with output impedance $Z_{out}(s)$, the resulting system will have natural frequencies at those points in the s-plane where

$$Z_L(s) + Z_{out}(s) = 0,$$

or

$$Z_L(s) = -Z_{out}(s). \tag{12.91}$$

The system will be unstable for a given passive $Z_L(s)$ if there are any right half-plane solutions to Eqn. 12.91. Since $Re[Z_L(s)] > 0$ for all values of s in the right half-plane (since $Z_L(s)$ is passive), right half-plane solutions to Eqn. 12.91 can exist only if $Re[Z_{out}(s)] < 0$ in some region of the right half-plane, such as the $Re[Z_{out}(s)]$ depicted in Figure 12.51.

Since there is no restriction on the sign of the imaginary part of a passive impedance in the right half-plane, we can always construct a $Z_L(s)$ which will satisfy Eqn. 12.91 for any one frequency in the region A in Figure 12.51. In general, this $Z_L(s)$ may need an imaginary part and a positive real part. If the imaginary or reactive component of $Z_{out}(s)$ is given by the sketch in Figure 12.52, where $Im[Z_{out}(s)] > 0$ for $Re[s] > 0$, then Eqn. 12.91 cannot be satisfied in the right half-plane by a purely resistive load $Z_L(s)$. Note that we can <u>always</u> find a reactive $Z_L(s)$ which will make the system unstable (a natural frequency in region A) though the system will be stable for any resistive load. Thus, unconditional stability is not guaranteed by stability with any resistive load.

If the imaginary part of $Z_{out}(s)$ happens to look like the surface

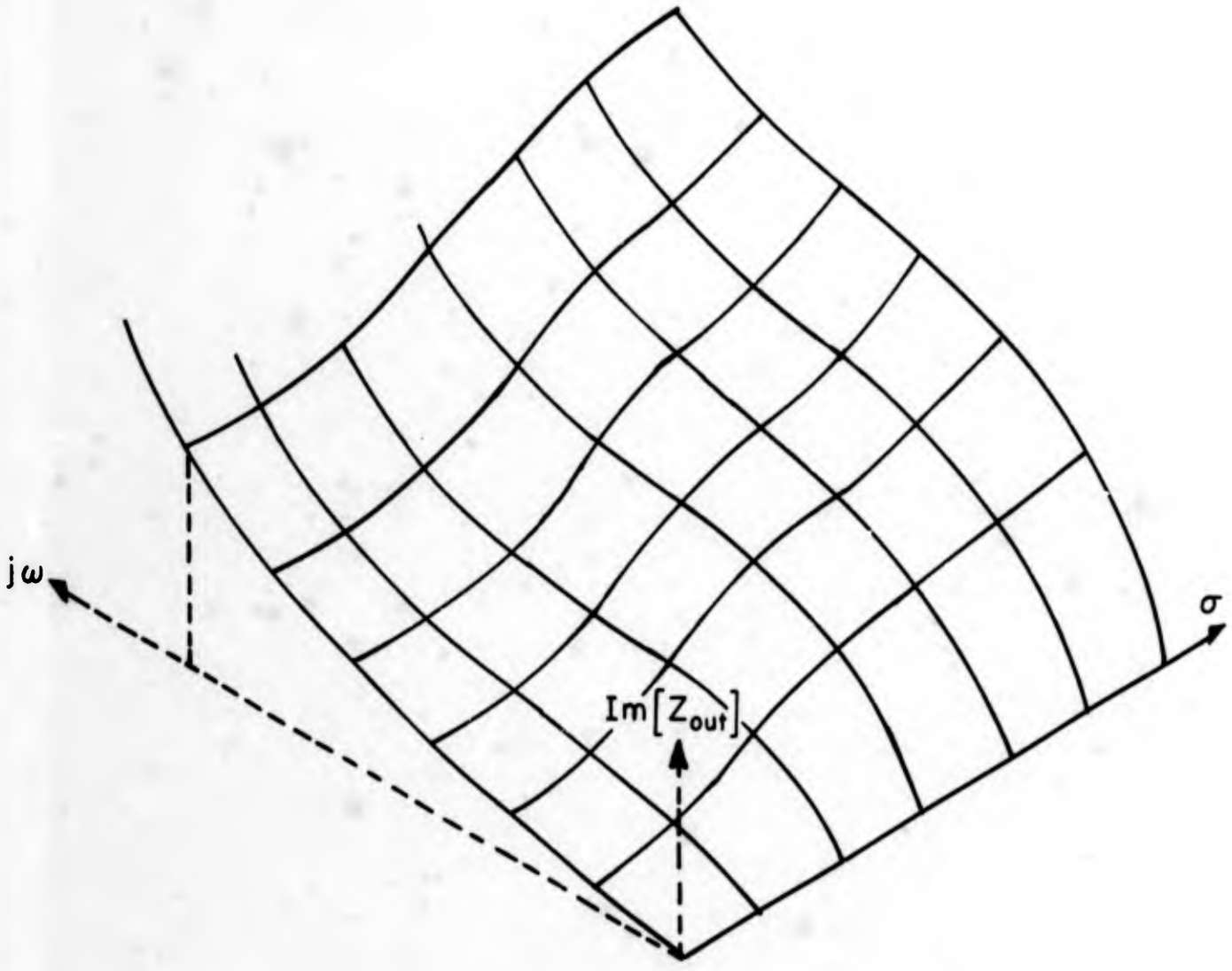


FIGURE 12.52

POSSIBLE IMAGINARY PART OF Z_{OUT} (S)

in Figure 12.53, then we see that the system will be unstable for some purely resistive loads. This we notice from the fact that a positive resistive load $Z_L(s)$ can satisfy Eqn. 12.91 for values of s which lie on the segment PQ in Figure 12.53. With these observations, we may state that a system will be unconditionally stable if

$$\mathrm{Re}[Z_{out}(s)] \geq 0 \text{ when } \mathrm{Re}[s] \geq 0 \tag{12.92}$$

and stable with resistive loads if

$$\mathrm{Im}[Z_{out}(s)] \neq 0 \text{ whenever } \mathrm{Re}[s] \geq 0,\ \mathrm{Re}[Z_o(s)] < 0. \tag{12.93}$$

The latter condition just states that a system will be stable with resistive loads if the output impedance $Z_{out}(s)$ is never pure negative-real anywhere in the right half-plane.

12.4 TERMINAL PROPERTIES OF THE POWER PROCESSOR

The terminal properties of the charger will depend on both the properties of the basic power converter and the auxiliary circuitry. For the charging mode just analyzed, the charger is a two terminal pair device with a power converter connected between the terminal pairs at times determined by the auxiliary circuitry. Aside from the normal operation of the charger which, in the SILVER mode, charges at a fixed current until the output voltage exceeds a preset threshold, the presence of auxiliary circuitry allows modes of oscillation which would not exist if only the basic power converter were in the charger.

In the preceding sections, we observed that the basic power converter is unstable when certain passive loads are connected to it. Some of the resulting oscillations, observed at the output terminals, may be severe enough to cause the polarity sensing circuit in the charger to change state, which in turn will disconnect the basic power converter from the charger output terminals. Since this polarity reversal is due to the basic power converter, the fault indication is relieved soon after the basic power converter is disconnected, and

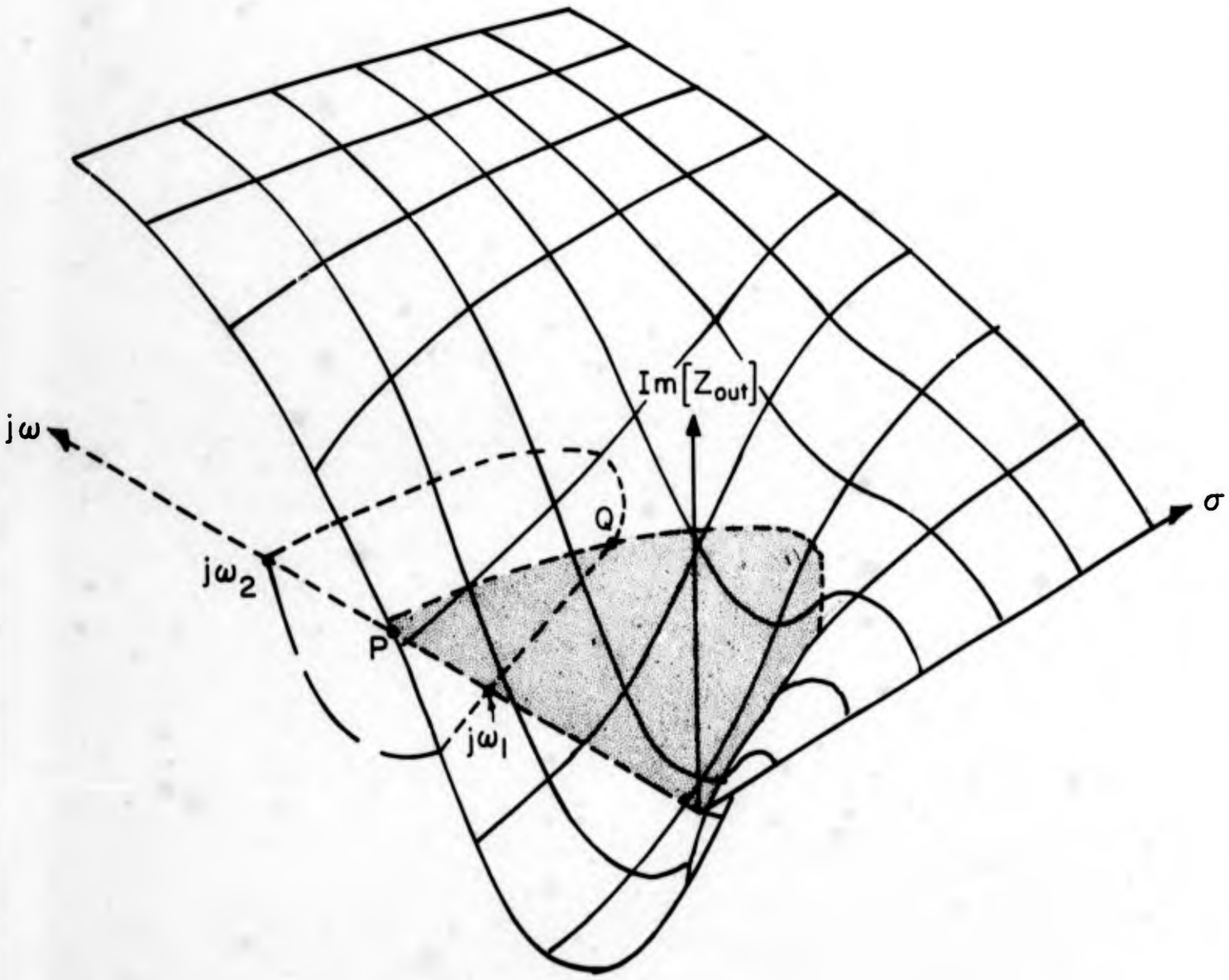


FIGURE 12.53

POSSIBLE IMAGINARY PART OF Z_{OUT} (S)

the auxiliary circuitry will again connect the basic power converter to the charger output. This cycle will continue indefinitely if the same loading condition persists.

This example serves to show the interaction among the various parts of a simple power system and especially the possible introduction of undesirable modes in certain parts of the system. In this case, we see that the auxiliary circuitry, which as a block performs well, can be included in an unstable loop due to instabilities in the remaining part of the system.

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13 ABSTRACT

A study of theoretical techniques applicable to the analysis and design of modern power processing equipment is presented. An organizational structure is developed which defines a meaningful partitioning of a power system into component blocks at various levels. Considerations relevant to the various levels of this structure both at the block diagram and circuit level, are treated. These areas include discussions of device models, dc power output stages and basic power converter limitations. A survey of current computer programs applicable to the analysis and design of electrical equipment is presented. Brief treatments of some mathematical techniques, including Hilbert transforms, describing functions, phase-plane analysis and stability criteria are given. The above theoretical tools are applied to the analysis of a practical power processor, and predicted characteristics compared with those observed in the laboratory. Bibliographies are provided for three areas; power processors, mathematical methods and computer aided design.

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