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RESEARCH AND DEVELOPMENT OF HIGH SPEED PROCESSOR ARRAYS

Prepared by
Philco-Ford Corporation
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FIRST INTERIM REPORT
January 1969

RESEARCH AND DEVELOPMENT
OF
HIGH SPEED PROCESSOR ARRAYS

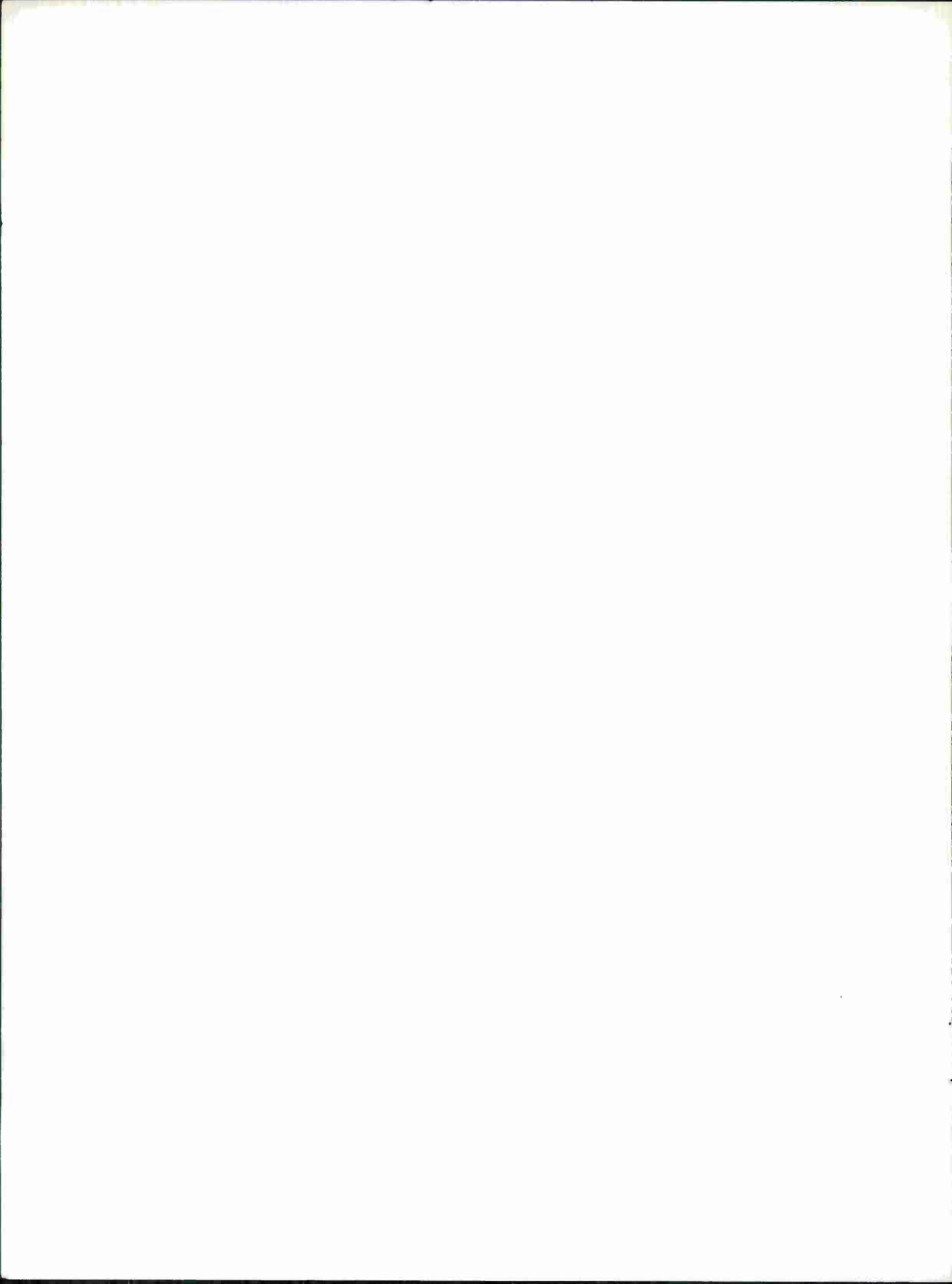
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For
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ABSTRACT

A research and development program directed toward the development of high density, high performance, complex digital arrays and their application in high speed system feasibility studies is under way.

The design effort included establishment of layout design rules and the design of the basic high speed ECL gate which will be employed in the processor arrays. Computer aid is being employed to generate photomask designs.

Development of high yield microcircuit and multilevel interconnection techniques has continued.

A microcircuit study vehicle, to be used in studying the thermal aspects of packaging high density arrays has been designed and fabricated.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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I - INTRODUCTION

1.1 PROGRAM OBJECTIVE

The objective of this program is the continued development of high density, high performance, complex digital arrays and their application in high speed system feasibility studies.

1.2 AREAS OF INVESTIGATION

During the past few years, Philco-Ford has directed research and development efforts toward the establishment of device, micro-circuit, and large-scale array technologies which can be applied in high speed complex data processing systems. This has been accomplished in part on previous programs subcontracted to Philco-Ford by MIT Lincoln Laboratory, under the primary sponsorship of the United States Air Force. During the present program, development of these technologies will continue. In addition, specific two- and three-level arrays will be designed and fabricated for application in feasibility studies of a high speed central processor. Program efforts will also include the continued investigation of multichip assembly techniques which are compatible with high speed systems.

The principal responsibility of Philco-Ford is the fabrication and preliminary testing of the designed devices,

microcircuits and arrays. In addition, Philco-Ford will serve as technology consultants by specifying component, microcircuit and array design rules.

II - PROGRAM DEVELOPMENTS

2.1 INTRODUCTION

The program effort for this first quarter has been concentrated in the following areas:

1. Establishment of a set of layout rules to be implemented by Lincoln Laboratory in designing the high speed array layouts.
2. Design of the basic microcircuit gate which will be used in the high speed processor arrays.
3. Continued development of high yield microcircuit and multilevel interconnection techniques.
4. Design and fabrication of a "Thermal Chip" to be used in studying the thermal aspects of packaging high density arrays.

2.2 LAYOUT DESIGN RULES

Lincoln Laboratory is performing the microcircuit and array layout designs, utilizing the computer aided layout capability which was developed and demonstrated during the previous program (see Final Summary Report, "R & D of the Technologies Required to Design Ultra High-Speed Computer Systems"). During this quarter,

a complete set of layout design rules for high-speed, high-density two- and three-level arrays has been established and documented.

Some key design features are:

1. The narrowest linewidths are to be 0.1 mil.
2. The narrowest line-to-line spacings are to be 0.1 mil.
3. Isolation linewidths are to be 0.2 mil.
4. First-level vias are to be 0.4 mil x 0.4 mil.
5. Second-level vias are to be 0.6 mil x 0.6 mil.

These design rules are consistent with high performance and high-yield processing and are based, in part, on modifications of rules evaluated during the previous program. They were also based, in part, on evaluations of transistor-resistor data obtained from test chips which were fabricated during this period. The test chip, referred to as the SPX-1, is shown in Figure 1.

2.3 DESIGN OF BASIC GATE

The choice of the basic gate for potential use in future complex chip designs was narrowed down to the two ECL circuit designs shown in Figure 2. Both of these gates are being designed onto a microcircuit test chip. The final choice of the basic gate will be based on static and transient analyses, and a speed-power

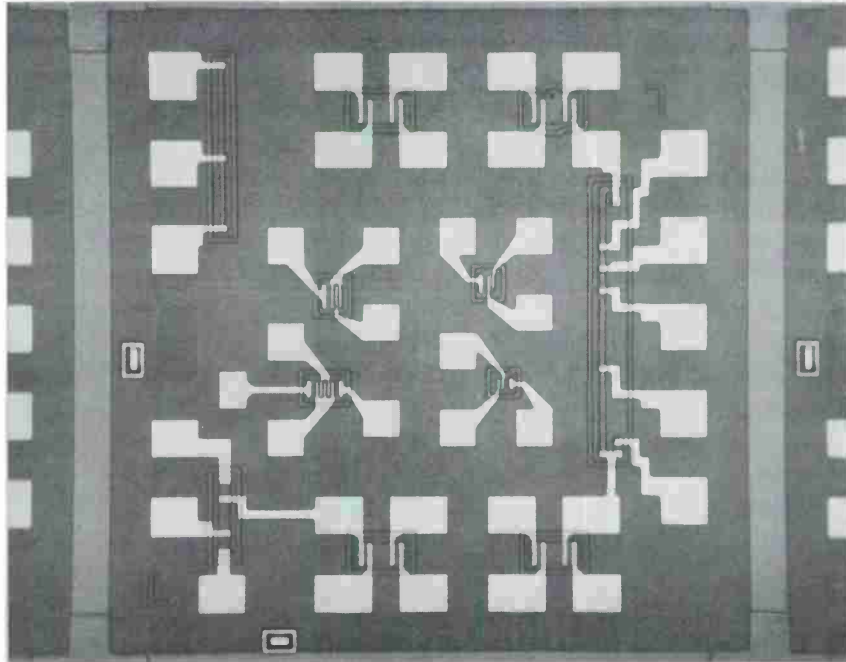
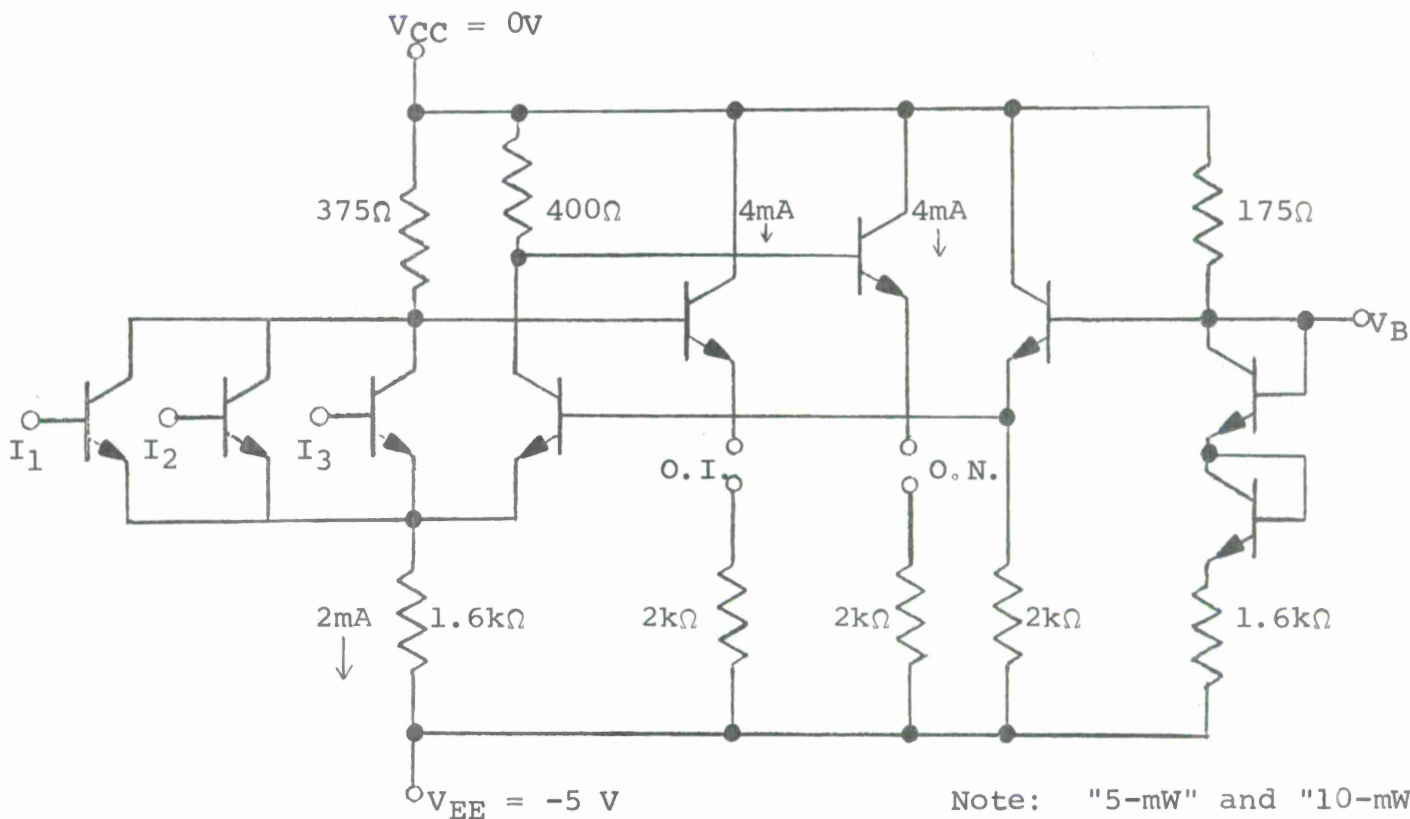
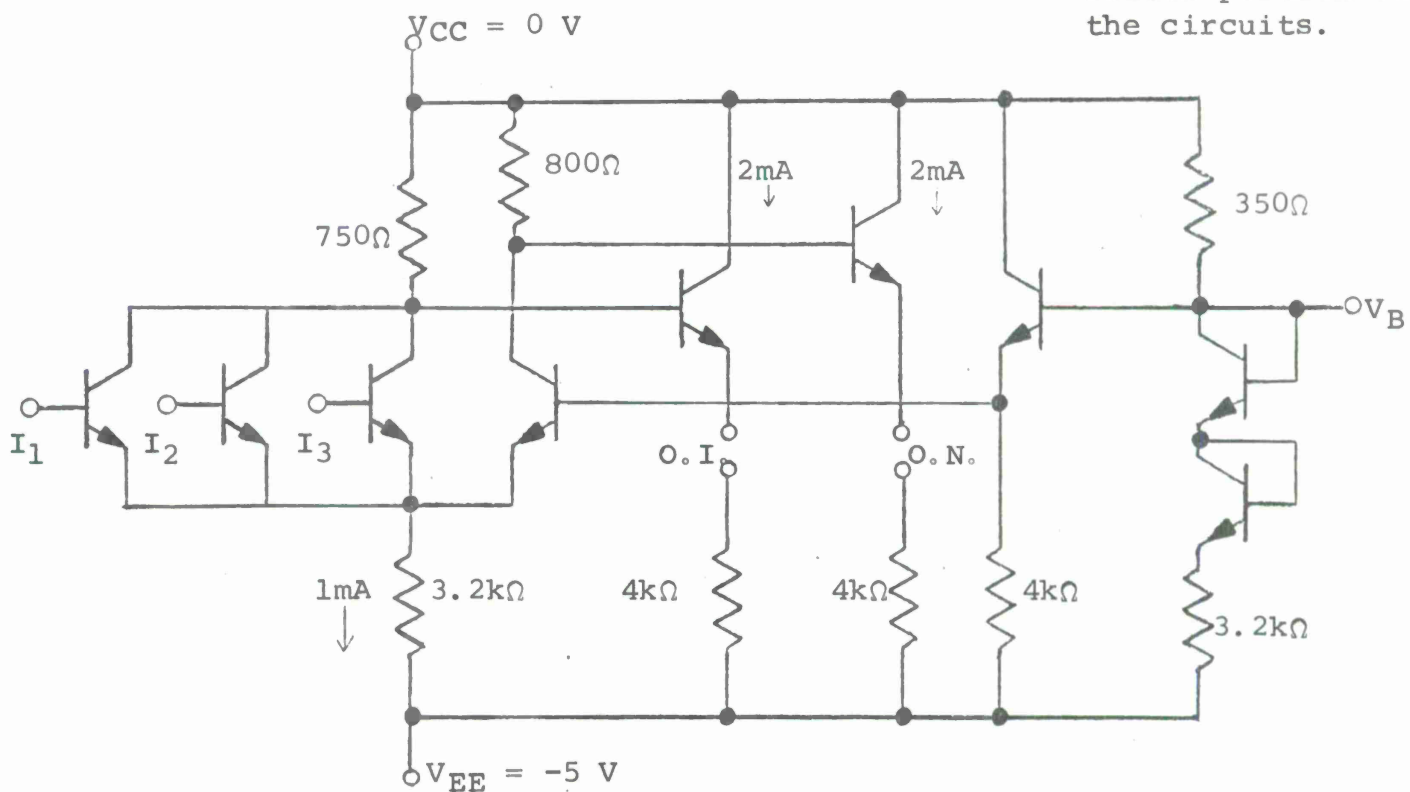


Figure 1. Photomicrograph of high speed test chip containing 0.1-mil geometry transistors, small-geometry resistors, and test patterns for device diffusion sheet resistance.



a. 10-mW ECL gate design.

Note: "5-mW" and "10-mW" specify the average power dissipation in the current switch portion of the circuits.



b. 5-mW ECL gate design.

Figure 2. Schematic diagrams of 5-mW and 10-mW high-speed ECL gate designs.

comparison to be made on fabricated versions of these microcircuit gates during the next quarter.

The microcircuit test chip, to be referred to as the SMX14, will contain groups of 5-mW and 10-mW gates, which will be evaluated for propagation delay time, τ_{pd} . The gates are interconnected in the manner illustrated schematically in Figure 3. The average τ_{pd} of a single array gate = $\frac{\tau_{pd}(\text{chain}) - \tau_{pd}(\text{Ref})}{4}$

Test transistors and test resistors will be included on the chip. These can be interconnected to simulate the gates and reference circuits for D-C analysis purposes. The test chip, which will have two levels of interconnections, will also contain a via test vehicle consisting of ten serially connected vias for evaluating the new two-level design rules.

2.4 HIGH YIELD MICROCIRCUIT ARRAY FABRICATION TECHNOLOGY

During the previous program, a capability for consistently fabricating high speed microcircuit transistors at greater than 90% yield was developed and demonstrated. On specific array wafers, yields in excess of 98% were obtained. During this program, efforts are being directed toward additional fabrication process improvements affecting the performance, yield, and reliability of small-area microcircuit arrays. Technology refinements related to fine-line photoengraving, uniform shallow-junction diffusion, thin epitaxial layer growth, and "defect-free" silicon

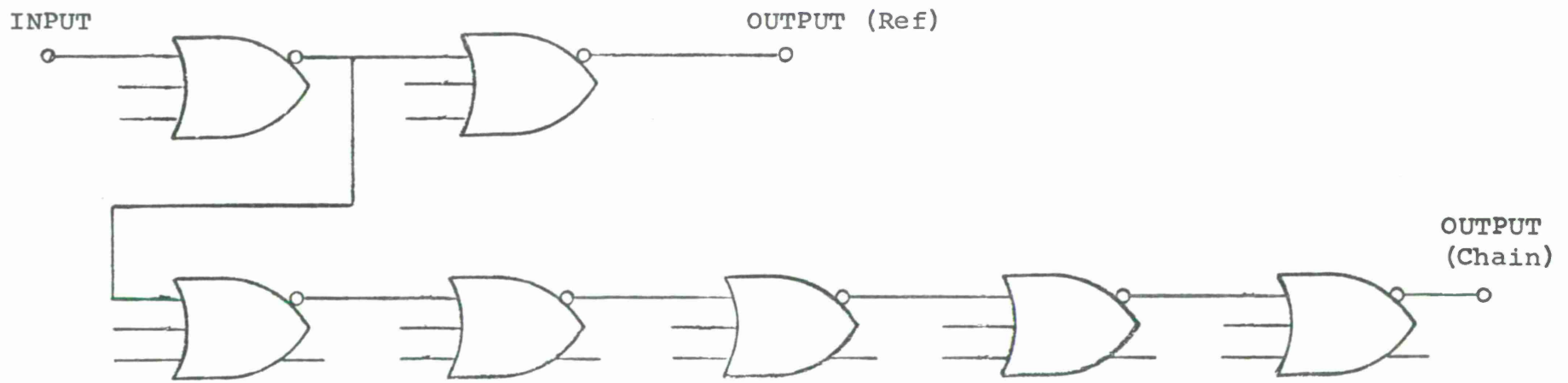


Figure 3. Schematic diagram illustrating the technique employed to measure propagation delay time on SMX14 ECL gates.

wafer processing are being continued. Transistor yields in excess of 97% are required to fabricate the processor arrays which will have gate complexities of 50 to 80 gates.

2.5 THERMAL CHIP

The packaging of arrays possessing high component densities presents problems in thermal management. During this first quarter, a special thermal test chip has been designed and fabricated. The Thermal Chip is a 100- x 100-mil chip consisting of a matrix of heating resistors and an array of sensing resistors dispersed throughout the chip. The Thermal Chip microcircuit will provide quantitative thermal data on packaged microcircuits. This technique for study of thermal properties will be used to supplement infrared scanning techniques currently being used for this purpose. Figure 4 is a photomicrograph of the Thermal Chip.

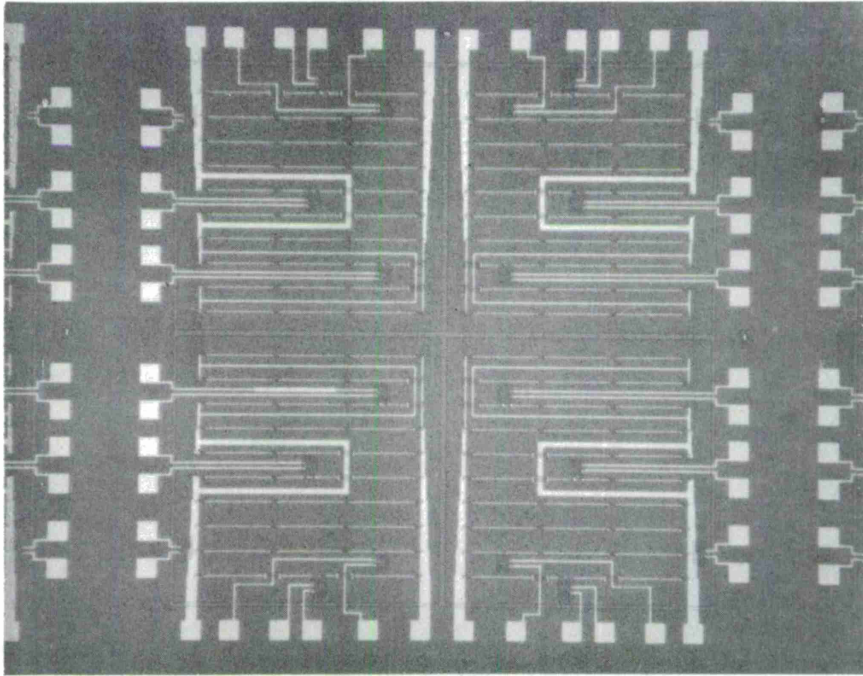


Figure 4. Photomicrograph of Thermal Chip.

III - FUTURE PLANS

Future work on this program will include:

1. Continued development of high-yield fabrication technologies for high speed arrays.
2. Fabrication and evaluation of SMX14 microcircuit test chip.
3. Selection of the basic microcircuit gate for future high speed processor array designs.
4. Design and fabrication of specific subfunction array chips for the high speed processor. These arrays, which will employ a maximum of three levels of interconnections, will include:
 - a. A 256-bit Read Only Memory chip,
 - b. A 4-bit Adder chip,
 - c. An 8-bit Register chip.
5. Design and fabrication of a multilevel test chip which will be used to test the effectiveness of present three-level array design rules and at the same time optimize future design rules.
6. Continued investigation of multichip assembly techniques.
7. Continued investigation of the thermal properties of single and multichip enclosures using the Thermal Chip as a study vehicle.

IV - DELIVERIES

During this interim, 60 packaged SPX-1 test chips were delivered to the Lincoln Laboratory.

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