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FINAL TECHNICAL REPORT
AIRBORNE FREQUENCY SYNTHESIZER
MODULE

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FINAL TECHNICAL REPORT
AIRBORNE FREQUENCY SYNTHESIZER MODULE

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Prepared by

Sylvania Electronic Systems Eastern Division
Sylvania Electronic Systems
An Operating Group of Sylvania Electric Products, Inc.
100 First Avenue, Waltham, Mass. 02154

Prepared By C. Onthank
C. Onthank
Project Manager

Approved By D. Newcombe
D. Newcombe
Radio Frequency
Laboratory Manager

For

Massachusetts Institute of Technology
Lincoln Laboratory
Lexington 73, Mass. .

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ABSTRACT

This report covers work performed from August, 1966 to September, 1967 on the design, development and fabrication of ten (10) Frequency Synthesizers. The program included analysis, circuit design, hybrid microcircuit development and the mechanical and electrical design required for an equipment design.

The results obtained during the program are discussed in detail. Included is a description of the Frequency Synthesizer Module, a discussion of the electrical and mechanical design and the results of the electrical performance of the Frequency Synthesizer.

**Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office**

1.0 INTRODUCTION

Sylvania was contracted by Lincoln Laboratory under an Air Force Prime Contract No. AF 19 (628)-5167 to design, develop, fabricate, test and deliver ten (10) production modules of a Frequency Synthesizer.

Hybrid Microcircuit Technology was used throughout the design of the Synthesizer. The program was accomplished in three (3) phases as follows:

Phase I: Design, Development and Breadboarding

Phase II: Airborne Packaging

Phase III: Production and Delivery of Ten (10) Units

The purpose of the required design study was to optimize circuit design for the application of Hybrid Microcircuit Technology and to determine the physical performance and projected unit cost of a developed package.

Subsequent to the award of the subcontract to Sylvania Electronics Systems - East (SES-E), a document entitled "Specification For An Airborne Frequency Synthesizer Module" dated 18 May 1966 was supplied by Lincoln Laboratory. This specification included two major sections, a basic performance specification and a suggested design approach. The technical approach to accomplish the program of objectives were described in Subcontractor's "Proposal for Design, Development and Fabrication of a Frequency Synthesizer for Lincoln Laboratory" dated 13 June 1966.

This document was incorporated by reference as part of the scope of work providing the basic, though tentative, functional design of the Frequency Synthesizer under development.

The implementation of the various microcircuits was examined in detail during the development stages, with the objective of developing a design approach which would provide the functional capability within the volume and environmental constraints while maximizing reliability and minimizing unit cost in production.

The desired packaging of the Synthesizer was as a single module under the general requirements of MIL-E-19600. Overall module size is 94 cubic inches.

The Synthesizer was designed to meet MIL-E-5400 Class 1 for aircraft electronic equipment.

Section 2.0 gives a detailed description of the synthesizer. The section is broken down to wafer and component level so as to detail the design and approach.

Section 3.0 summarizes the synthesizer specifications in three (3) categories: electrical, mechanical, and environmental.

Section 4.0 summarizes the design, development and test programs. The intent is to give the reader a complete description of the final design configuration and a summary of how and why this design was chosen and how and why the design differs from the original concept. The section concentrates on critical design areas, design consideration problems and performance obtained in the meeting of the specification. It has a subsection on "Promising Avenues Toward Improvements".

2.0 FREQUENCY SYNTHESIZER MODULE SYSTEM DESCRIPTION

The block diagram of the frequency synthesizer module is shown in Figure 2-1. The module consists of three components: the component frequency generator assembly, the control word buffer, and the mix-divide module assembly.

Assembly Name	Wafer Type	Wafer Description	Sylvania Drawing Number
Component Freq. Generator	X	Freq. Multiplier, Mixer	00-470602
	Y	102.4 KHz Generator	00-470582
	D	Buffer Amplifiers, Divide-by-Three	00-470633
Control Word Buffer	(Assembled directly to Multi-layer Board)		00-470662
Mix-Divide Assembly	A, B	Mix-Divide; A, B	00-470574, Sheet 1
	A	Mix-Divide; A	00-470574, Sheet 2
	B	Mix-Divide; B	00-470574, Sheet 3
	C	C Wafer (Output Buffer)	00-467981, Sheets 1 & 2

The purpose of the frequency synthesizer module is to generate approximately 1,000,000 discrete frequencies in the range of 7.6 to 8.4 MHz. The discrete frequencies are spaced 0.78125 Hz apart. The generated frequencies are derived from an accurate 1 MHz external reference. The frequency selected is controlled by 20 external digital lines. The digital signal is stored in the control word buffer in response to an external command. Upon receiving the external command, the frequency synthesizer module will settle at the new desired frequency within 20 microseconds.

The Component Frequency Generator produces 4 frequencies required by the mix and divide modules to synthesize the one million frequencies. These 4 frequencies are generated from the external 1 MHz reference by a process of frequency multiplication, mixing and filtering.

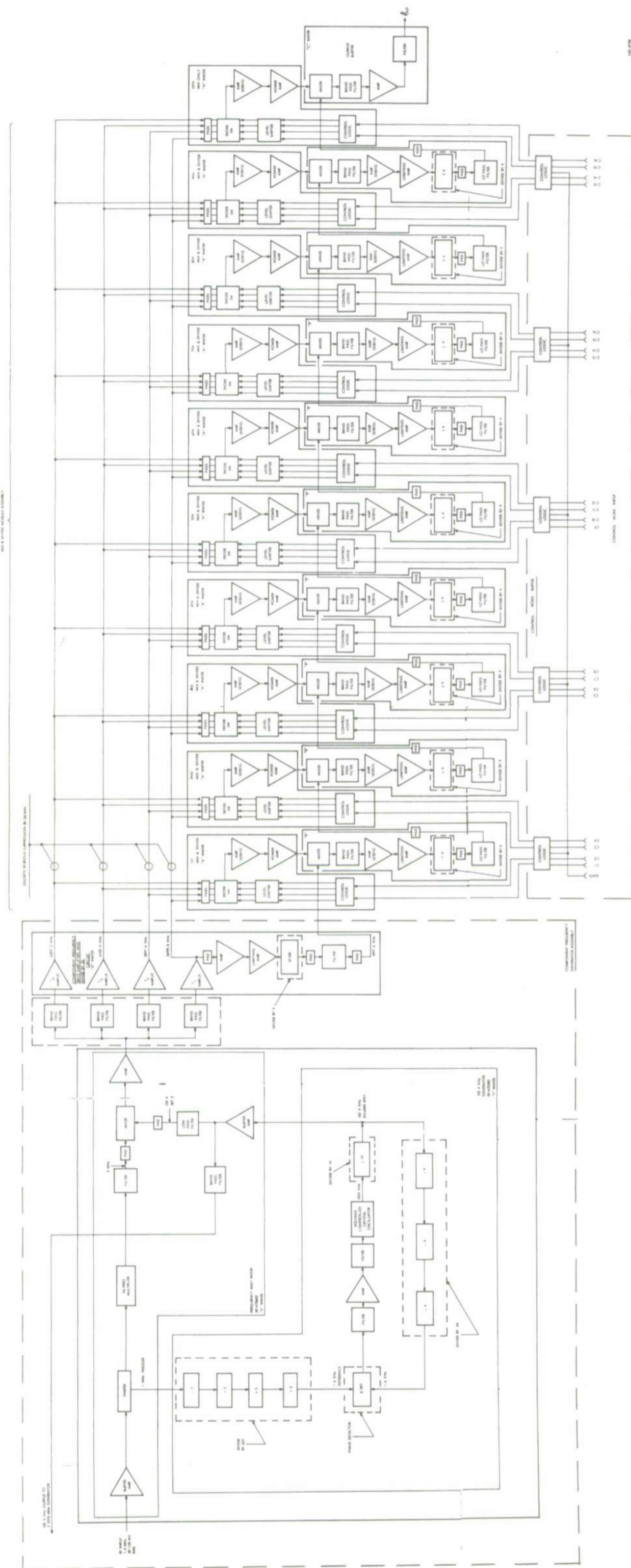


Figure 2.1 Frequency Synthesizer Block Diagram

Ten (10) mix-and-divide modules are required to generate the one million output frequencies. The first Mix-and-Divide module generates four steps of 0.78125 Hz. The second mix-and-divide module provides four steps of 3.125 Hz. Each successive mix-and-divide module generates steps of four times the previous value, with the last mix-and-divide module providing four steps of 204.8 KHz.

The lowest frequency generated by the frequency synthesizer module is 7.5904 MHz. This frequency is generated in response to a control word of 20 0's corresponding to a binary number 0. When the control word buffer contains all 0's, only two frequencies are selected from the component frequency generator - 5692.8 KHz and 1897.6 KHz. The sum of the two input frequencies to the mixer is the desired 7.5904 MHz. This is separated from the difference frequency out of the mixer by a bandpass filter. In the first 9 mix-and-divide modules, the 7.5904 MHz signal is divided by 4 to recover the original 1,897.6 KHz. In the last mix-and-divide module, the divide by 4 is not performed, and the output is 7.5904 MHz.

When the control word buffer contains a binary 1, the first mix-and-divide module selects a frequency of 5897.6 KHz. This frequency is exactly 204.8 KHz higher than the previous selected frequency. This delta frequency is divided by 4 in nine mix-and-divide modules. This division by 4^9 results in the desired incremental step of 0.78125 Hz at the output of the frequency synthesizer module.

The estimated power budget breakdown for the frequency synthesizer module is shown in Table 2-1.

TABLE 2-1	
POWER BUDGET	
SUPPLY VOLTAGE	POWER
+15V	8.9W
-15V	3.7W
+5V	<u>3.0W</u>
	15.6W
Total power dissipation 15.6 watts	

In the design of the synthesizer, the spurious requirements of 60 db over the band and 80 db individual spurious level have been considered. Subsections 2.1.4, 2.1.5, 2.3.2 and 2.3.4 should be referred to for detailed discussion.

2.1 COMPONENT FREQUENCY GENERATOR

The component frequency generator produces 4 output frequencies required by the mix-and-divide modules to generate the one million output frequencies. Four of the frequencies from the component frequency generator are produced by mixing a 6-MHz signal with the first and third harmonics of the 102.4 KHz frequency.

The 6 MHz frequency is generated by a frequency multiplier which multiplies the 1 MHz external reference frequency. The 102.4 KHz signal is generated by a VCXO in a phase lock loop. The output of the 102.4 KHz VCO oscillator is limited and filtered to produce the harmonics to drive the balance mixer which generates the output frequencies of the component frequency synthesizer.

The four frequencies produced by the balanced mixer are filtered by extremely narrow, sharp-skirted crystal bandpass filters and are then amplified by a component frequency drive amplifier which contains a power divider to drive 10 RF switches for each output frequency. An 1897.6 KHz signal is generated by the divide by 3 module and is filtered and attenuated to drive the input of the first mix-and-divide module.

2.1.1 Input Buffer

The input buffer consists of a two-stage amplifier. The first stage is a high-gain video amplifier. The second stage is a saturated inverter. The two stages are required to amplify the approximate 70 mv input level to an output square wave of 0 to 3 volts. The square wave is required to drive the x 6 multiplier and the divide by 625 section of the 102.4 KHz generator. The gain of the input buffer is sufficient to produce a saturated square wave output over the required input range of $-10 \text{ dbm} \pm 5 \text{ dbm}$. The input buffer has a voltage gain of approximately 100. The input buffer also serves to isolate the input signal line from frequencies generated within the component frequency generator.

2.1.2 102.4 KHz Generator

The frequency 102.4 KHz is generated by a VCXO in a phase lock loop.

The 1 MHz external signal is divided by 625 using 4 integrated divide by 5 modules. The output of this divide by 625 is a 1600 Hz signal. This is fed into one input of a flip-flop phase detector. The other input to the flip-flop phase detector is generated by dividing the output of the 102.4 KHz voltage control oscillator by an integrated $\div 10$ followed by a 6-stage binary divider. The output of the phase detector is filtered to produce a DC level which is fed into the control input of the 102.4 KHz VCO to control the frequency, which equals 1 MHz multiplied by 64 and divided by 625.

The phase detector consists of a single R-S flip-flop which is an AC-coupled set-reset flip-flop with independent set and reset inputs.

The 102.4 KHz voltage-controlled oscillator is crystal-controlled with a pair of varactor capacitors to pull the oscillator to the exact required frequency in response to an external DC input.

The divide by 64 circuit uses 3 divide-by-four integrated circuits in a conventional binary divider chain.

The filter at the output of the phase detector is an RC filter which stores the DC level corresponding to the phase difference between the divide by 625 chain and the divide by 64 chain. The filter is followed by an operational amplifier to drive the varactors.

2.1.3 x6 Frequency Multiplier

The x6 multiplier is used to generate a 6-MHz sine wave output to the balanced mixer at 50 ohms. The x6 multiplier is driven by a low impedance 1 MHz square wave from the "input buffer". The 1 MHz square wave is first converted to 3 MHz by a symmetrical hard limiter followed by a three pole band pass filter. The 3 MHz output of the tripler stage is then doubled in a transformer-coupled full wave diode circuit. The 6 MHz output from the diode doubler circuit is filtered and used to drive the 50 ohm input to the balanced mixer.

2.1.3 Balanced Mixer

The balanced mixer employs a Sylvania matched diode quad unit, a bridge circuit within a TO-46 case, and three toroid transformers in a Ruthroff configuration to provide good balance operation.

This balanced mixer approach is used to minimize the signal feed through between any two terminals. The isolation between the input terminals will be in the order of 40 db. At the output terminal, the sum and difference of the input signals, plus the associated mixer harmonic frequencies and the two input signals, will be present; an advantage of this circuit is that undesired input frequencies are suppressed by a minimum of 25 db and other undesired mixing products a minimum of 40 db with respect to the sum or difference frequencies.

In the component frequency generator frequency module, the required frequencies are selected by the appropriate crystal filters described in Para. 2.1.5 to obtain the required harmonic and spurious frequency rejection.

2.1.5 Bandpass Filters

The desired output from the balanced mixer consists of four frequencies: 6307.2 KHz, 6102.4 KHz, 5897.6 KHz and 5692.8 KHz. These signals are fed into a crystal filter assembly. Each filter passes its desired frequency and rejects the other three, as well as the 6 MHz input to the balanced mixer which will also appear at the output of the mixer.

The undesired signals appearing at the output of each filter are at least 80 db down to obtain desired spectral purity. (Unless a sufficient amount of rejection is obtained, the undesired signals will appear at the input of the balanced mixer and generate spurious signals at the output above the minimum requirement.)

A filter which will meet the above requirements must have a maximum 80 db bandwidth of 200 KHz. This requirement is dictated by the 6102.4 KHz and the 5897.6 KHz filters which must also reject the 6 MHz signal appearing at the input to the filters. A relatively simple four-pole crystal network and matching transformers are used to meet the design goal of 80 db rejection of undesired signals. The filters are packaged as one filter assembly with one input and four outputs. The latter approach was chosen since it simplifies overall packaging problems, is smaller in size and has fewer external interconnections. Because of the relative simplicity of the filter, the complete filter assembly is packaged in less than 6 cubic inches.

2:1.6 Component Frequency Drive Amps and Divide by Three

The component frequency driver amplifiers are two stage feedback amplifiers connected as a voltage source. They employ a PNP-NPN pair with transformer output.

The divide by 3 circuit generates 1897.6 KHz from the 5692.8 KHz output of the balanced mixer. The divide by 3 is performed by two integrated flip-flops connected as a binary counter with feedback which resets the counter to 1 when a count of 3 is reached.

2.2 CONTROL WORD BUFFER AND DECODERS

The control word buffer consists of 5 Sylvania 4-bit integrated storage registers. These registers store the external control word when the control line goes to zero. Interface requirements for control word buffer (0's and 1's) are standard Sylvania SUHL levels.

2.3 MIX-AND-DIVIDE MODULES (Wafer Pairs: 9 A/B and 1 A/C)

Each mix-and-divide module consists of a 4:1 RF switch, an RF amplifier, a double balanced mixer, a bandpass filter, a divide by four circuit and a low pass filter. Nine such modules are required to generate the one million output frequencies. The tenth module differs in that no frequency division occurs.

Each module mixes one of four frequencies spaced 204.8 KHz apart with the 2 MHz ± 102.4 KHz output of the previous module. The desired mixing frequency is determined by the settings of the control word buffer flip-flops.

The output of the mixer contains sum and difference frequencies (i.e., 4 MHz and 8 MHz). The sum frequency is selected by a bandpass filter and is amplified and limited to produce a square wave suitable for driving a binary divide by four stage. The square wave output of the divider stage (approximately 2 MHz) is filtered to remove the higher harmonics.

2.3.1 RF Switch

The RF switches used in the mix-and-divide module employ two Sylvania high-speed RF switch diodes in a back-to-back configuration to provide 80 db of isolation required to meet the spurious output requirements. Each switch is driven directly from decoding gates which decode the output of the control word buffer.

2.3.2 RF Amplifier

The RF amplifier provides approximately 30 db of gain at the output of the RF switch to compensate for the loss of the switch and to supply sufficient power to drive the balanced mixer.

2.3.3 Balanced Mixer

The balanced mixer used in the mix-and-divide module is identical to the configuration described in 2.1.4. The mixer is used to generate the sum of the 2 MHz + 102.4 KHz signal from the previous mix-and-divide module with one of the four frequencies from the RF switch (i.e., 6 MHz + 102.4 KHz and 6 MHz + 307.2 KHz).

2.3.4 Bandpass Filter

The bandpass filter is used to pass frequencies between 7.5 MHz to 8.5 MHz.

The bandpass of the filter has a center frequency of 8 MHz, a 3 db bandwidth of 800 KHz and a 60 db bandwidth of 4.7 MHz. The bandpass filter is a Butterworth, four-pole inductive-coupled network using powdered iron toroids. This filter network has a 2 db insertion loss. The input and output impedances of the network are 50 ohms. Sixty db of rejection is provided at 6.4 MHz (the highest mixer frequency). Since the mixer provides 24 db of rejection, the 6 MHz is at least 84 db down at the output of the synthesizer, due to direct transmission.

2.3.5 Divide by 4 Circuit

The divide by 4 circuitry of the mix-and-divide modules incorporates two stages of integrated flip-flops connected as a straight binary divider. The integrated circuits are preceded by a buffer amplifier consisting of a video amplifier followed by a saturating switch driver to convert the output of the bandpass filter from a sine-wave to a symmetrical 3 volts square wave required to drive the integrated circuit flip-flops.

2.3.6 Low Pass Filter

The low pass filter is used to remove the square wave harmonic components generated in the divider circuit.

The low pass filter rejects frequencies at 4 MHz and higher at 48 db down and will pass frequencies at 2 MHz and lower at a ripple to 2 db. The filter network is a modified Chebyshev with the input and output impedance at 50 ohms.

2.3.7 Output Buffer

The output buffer employs a video amplifier followed by a limiter circuit. The output level is -5 dbm, nominal.

2.4 MECHANICAL DESIGN

The basic design objectives were to utilize the latest construction techniques for increasing reliability, making equipment easier to maintain and to reduce overall cost. State-of-the-art techniques in microelectronics and packaging were employed, within the limits of MIL-E-5400H Class I equipment, to accomplish the above objectives. The frequency synthesizer design line dimensions are 3" wide, $4\frac{1}{2}$ " high, 7" long occupying a volume of $94\frac{1}{2}$ cubic inches.

The system contains 23 microcircuits of 6 different layouts. The circuits are of a thick-film hybrid type employing alumina substrates, integrated circuits and discrete microminature components.

Twenty-one of these microcircuits are mounted to and interconnected by a 5 layer multi-layer printed circuit board. The multi-layer board combines printed wiring and stripline fabrication techniques to accomplish both RF and DC transmission. The RF transmission lines are sandwiched between two ground planes minimizing radiation and cross-talk. Plated-through holes are used to bring the signals and voltages to the surfaces of the multi-layer board.

Compartmented covers, each one accommodating one of two microcircuits were used to secure the circuits to the mother-board and to provide the required shielding between microcircuits.

Interconnection of the microcircuits to the multi-layer board is accomplished by using flying leads on the microcircuits. The leads are inserted through clearance holes and protrude to the far side of the multi-layer board where they are bent over and soldered to a plated-through hole. This eliminates the need for connectors and facilitates maintenance. The weight of the entire package is $5\frac{1}{2}$ pounds.

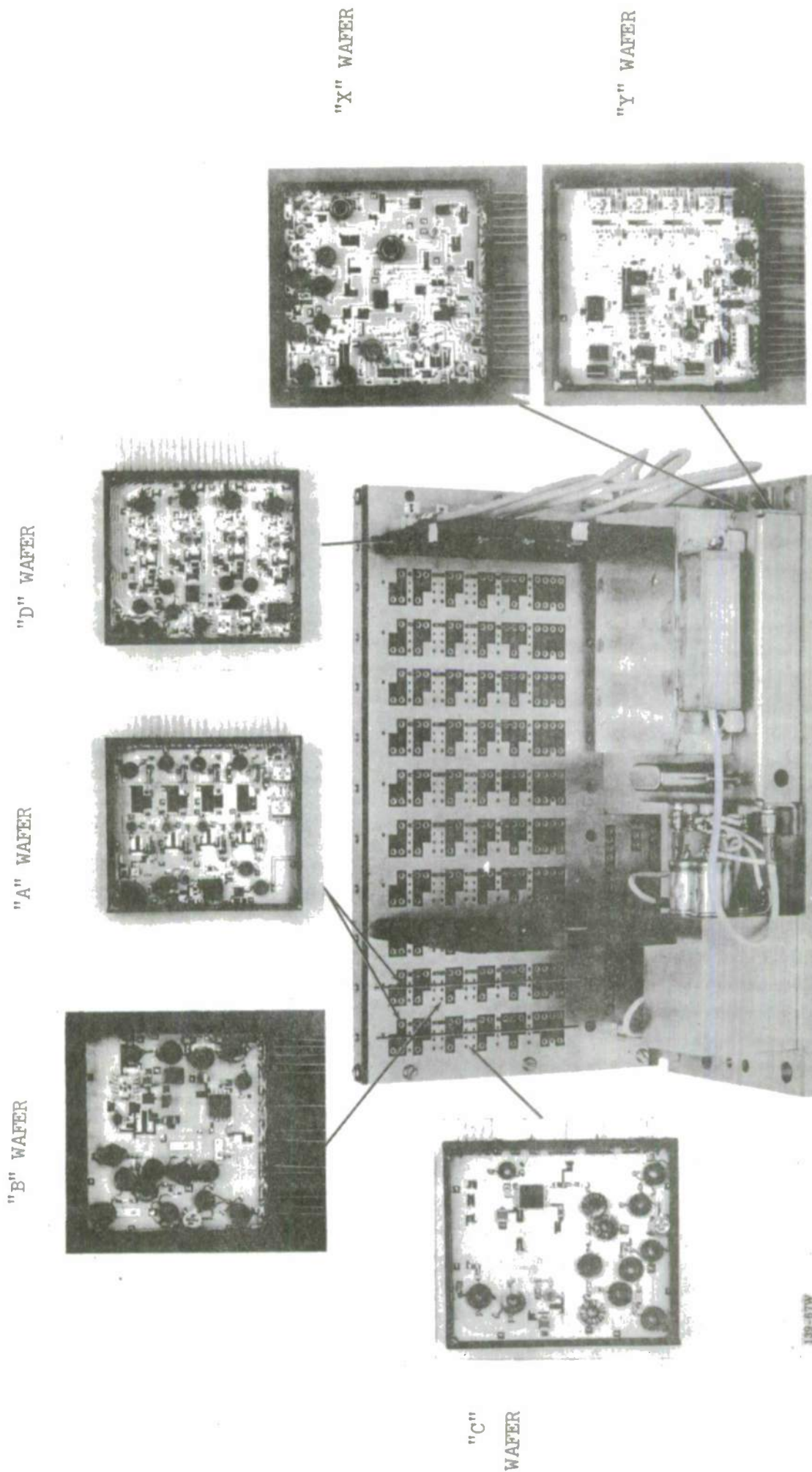


Figure 2.2 Frequency Synthesizer Unit

2.5 ELECTROMAGNETIC INTERFERENCE DESIGN

The frequency synthesizer module has been designed to the general environmental requirements of MIL-E-5400. Since the module is not expected to operate as an independent unit, it was designed for incorporation into a major assembly from which it derives secondary power and control command signals. As a sub-assembly it is not designed to meet the full requirements of any Military EMI Specification. However, due to the severe operational performance requirements imposed upon the frequency synthesizer, the design incorporates judicious measures to minimize crosstalk, intermodulation, spurious response and interference emanations--both conducted and radiated. To achieve high performance within its compact size, circuit isolation is obtained by the application of power line de-coupling at each microcircuit card and at the multi-layer board. In addition, 70 db RF filters are in series with the module DC input lines. Each microcircuit card has a ground plane covering one surface. This provides isolation between cards and reduces radiation. Each card is enclosed within an individual brass cover which is grounded to the base plate of the module. RF interconnection between microcircuits are achieved by printed wiring sandwiched between two ground planes of the multi-layered mother-board. All other RF interconnections are by shielded cable. The crystal filter and crystal oscillator are in separate metallic enclosures. An RF-tight cover is fitted over the entire assembly and is secured to the base plate.

The frequency synthesizer has been tested and passed the limits of MIL-I-6181.

3.0 SPECIFICATIONS - 8 MHz FREQUENCY SYNTHESIZER

3.1 Electrical

Center Frequency	8 MHz
Number of Selectable Frequencies	2^{20}
Total Bandwidth	(Approximately) 800 kHz
Input Control	20 binary bits plus 1 control level
Frequency Increments	0.78125 Hz
Spectral Purity	60 db spurious in 100 Hz band \geq 100 Hz from carrier
Switching Time	20 μ sec
Output Specifications	-5 \pm 3 dbm into 50 ohms load
Input Reference Frequency	1.0 MHz (nominal)
Input Reference Frequency Accuracy	1 part in 10^7 (present design will tolerate specification of 5 parts in 10^6)

Input Reference Source Impedance	50 ohms
Input Reference Level	-10 <u>+5</u> dbm
Non-harmonically Related Spurious Contamination of Reference Frequency Input Line	-70 db below input reference signal

3.2 Mechanical

Size	4½ x 3 x 7
Volume	94.5 cu. in.
Weight	5.5 lbs.

Power

15 watts	+15	8.9w
	-15	3.0w
	+ 5	<u>3.7w</u>
Regulated to 1%	TOTAL	15.6w

3.3 Environmental

Built to meet requirement of MIL-E-5400, Class 1.

4.0 CRITICAL PERFORMANCE AREAS

4.1 Spectral Purity

4.1.1 Definitions

The primary requirement with respect to spectral purity was to suppress both in magnitude and number all discrete spurious spectral lines. For all practical purposes, such spurious lines were the dominant contaminants threatening both aspects of the spectral purity requirement. This requirement is repeated here for reference:

1. "For any selected output frequency, with the digital control word held fixed, the total power in the frequency band from 7.5 to 8.5 MHz, excluding a 10 Hz band centered on the output frequency, should be at least 40 db (60 db design goal) below the output power in a 10 Hz band centered on the output frequency.
2. For any selected output frequency, with the digital control word fixed, the power in any 100 Hz band centered 1 KHz or more away from the output frequency should be at least 60 db (80 db design goal) below the output power in a 100 Hz band centered on the output frequency.

4.1.2 Design Considerations

4.1.2.1 Random Noise

As indicated above, the contribution of non-discrete contamination, assuming a reasonable noise figure in the "C" wafer amplifier, would be negligible (about 35 db below the indicated allowable total noise power). Consequently, the present design was not sensitive to noise figures.

4.1.2.2 Discrete Spurious

4.1.2.2.1 Mixer Design

The direct synthesis approach, employing an iterative mix/divide (frequency translate/frequency divide) structure, requires the selection of a mixer frequency ratio, and a range in that ratio, which avoids generation of low-order, in-band spurious products, and then a doubly-balanced mixer to attenuate higher-order products which unavoidably do lie in-band.

4.1.2.2.2 Filter Design

Certain frequencies are inherently strong in the mixer output. Particularly so are the sum and difference frequencies, and the "local oscillator" or switching drive frequency. The primary frequency response requirement of the band-pass filter following each mixer is the attenuation of these and other troublesome frequencies.

The primary frequency response requirement of the low-pass filter following each frequency divide-by-four circuit is the attenuation of the harmonics of the fundamental output frequency.

In the component frequency generator, the primary frequency response characteristic of the filtering (RC) between the phase detector output (SF-30) and the VCXO is the attenuation of the sampling frequency sufficiently to avoid excessive FM sidebands of the VCXO output (which would be in-band spurious passing through the XTAL comb filter).

4.1.2.2.3 Isolation and De-coupling

There exist many opportunities for cross-talk and mutual contamination of signal points and signal paths in a synthesizer. The problem is compounded by three considerations:

- a. The importance of minimizing such crosstalk.
- b. The fact that a very large number of discrete frequencies normally occur throughout the synthesizer in normal operation.
- c. The need for miniaturizing the synthesizer, thus placing these potential communicants in close proximity.

4.1.3 Problem Areas

The types of problems experienced in obtaining satisfactory signal purity in the synthesizer output may be grouped under three headings:

1. Crosstalk, or undesirable propagation of primary signal frequencies, so as to directly contaminate other primary signal frequencies. The contaminated and the contaminating signals may be related "laterally" (such as mutual contamination between component frequencies), or "sequential" (such as coupling of a "signal" frequency from one mix-and-divide assembly (module) to an earlier or later mix-and-divide module).
2. Mixer product frequencies, generated as immediately in-band spurious, and processed by the remaining portion of the synthesizer mix-and-divide chain as would be legitimate sidebands of the "signal under process".
3. Particular frequencies inherently generated as by-products of certain operations, further interacting in non-linear devices so as to produce, ultimately, in-band spurious signals.

4.1.3.1 Crosstalk, Isolation Problems

These problems arise predominantly from the need for compactness of packaging.

4.1.3.1.1 Component Frequency Crosstalk

Since the mode of operation of the synthesizer involves successive selection and processing of one or another of four nearly equal basic component frequencies, it is apparent that if, at any point in the chain, the intended component frequency becomes contaminated with one or more of the three un-intended component frequencies, spurious sidebands will result. It turns out that the majority of such possible occurrences result in in-band sidebands being generated and propagated. Such propagation is accompanied by improvement in signal to spurious sideband ratio of 12 db at each frequency-division point encountered.

The component frequencies are generated in a common circuit ("X" wafer), and are separated in the crystal band-pass filter assembly.

The first subsequent opportunity for recombination, or crosstalk, occurs in the "D" wafer, where each of the component frequencies is amplified (in power) and re-presented to one of four parallel pairs of printed conductors buried inside the mother-

board. Signals are extracted as required from these "transmission lines" into each of 10 "A" wafers spaced along the length of the motherboard. One and only one of the four component frequencies is accepted into each "A" wafer, the choices being independent of one another, and uniquely defined by the ultimate frequency required from the synthesizer.

Excessive crosstalk of component frequencies, one to another, was encountered, attributable to inadequate isolation on the "D" wafer, the motherboard, and the "A" wafers.

4.1.3.1.1.1 "D" Wafer Crosstalk of Component Frequencies

It was found that magnetic coupling from the output of one amplifier to the input of the adjacent one was producing excessive crosstalk, (about 60 db down). It was found possible to reduce this contamination by orienting the output lead pair (transformer-coupled) so as to produce a net magnetic coupling of zero, leaving only residual resistive and capacitive coupling. This was a workable solution because it was possible to insure permanency of adjustment of each lead position with a bead of epoxy.

Also, the "D" wafer, as with all other wafer types, was completely potted with a transparent jelly-like encapsulant. (Sylgard #182). This latter coupling "resistive" was primarily due to the finite conductor and node resistances characteristic of thick-film techniques. The layout had already provided individual ground returns for the four amplifier circuits, but coupling was provided from one "ground" circuit to another "ground" circuit by power supply by-pass capacitors. The net coupling was reduced, therefore, by decreasing the by-pass capacitors.

The resultant crosstalk of component frequencies at the "D" wafer output, with no "A" wafers loading the motherboard "transmission lines", but with equivalent local loading provided by discrete resistors, was characteristically 70 db down.

4.1.3.1.1.2 Motherboard-Induced Crosstalk of Component Frequencies

As the next step in the study of crosstalk, the four individual, local load resistors at the output terminals of the "D" wafer (mounted to the motherboard) were replaced by four sets of nine resistors each, mounted to the motherboard at the terminal pairs ultimately intended to connect to the input leads of the first nine of ten "A" wafers. These resistor values corresponded to the (loaded) input impedance of the "A" wafers. It was found that the crosstalk increased, due now to the added magnetic coupling incurred on the motherboard.

The solution was to adjust the "D" wafer compensating loops (discussed above) with the "D" wafer mounted to the motherboard, with a compromise simulated load resistor set of 12 (three resistors distributed the length of the motherboard. The crosstalk was by this means brought to a suppression level of 65 to 70 db, with worst-case loading (corresponding to all of the first nine "A" wafers calling for the same component frequency).

4.1.3.1.1.3 "A" Wafer-Induced Crosstalk of Component Frequencies

The amount of crosstalk measured on the signal distribution buses with a full complement of "A" wafers mounted to the motherboard was markedly increased over that observed with the simulating resistor load. The increase in crosstalk was still greater when the complement of "B" wafers was mounted to the motherboard. This was due to the fact that each mixer (L.O.) drive circuit included the motherboard "ground" etch, since the mixer and its driver were mounted on different wafers ("B" and "A" wafers, respectively), each mounted by leads to the common motherboard. Thus, since the input component frequency buses and the mixer drive circuits were both grounded to the motherboard, component frequency cross-contamination was produced.

This situation was corrected by completely floating each of the four component frequency lines requiring the replacement on each "A" wafer of the input shunt inductors by bifilar transformers. Finally it was noted that to obtain minimum crosstalk, the turns distribution around the toroidal cores of each of these transformers was adjusted to be uniform.

The incorporation of the indicated changes (Sections 4.1.3.1.1.1 through 4.1.3.1.1.3) resulted in the attainment of a 65 to 70 db suppression of adjacent-line crosstalk.

4.1.3.1.2 Other Crosstalk Problem Areas

4.1.3.1.2.1 Need for Care in Avoiding Leakage of High Level Signals, in General

It is extremely important in a synthesizer of this type to confine stray fields and define ground paths. One becomes convinced of this, for example, upon realizing that the output of a divide-by-four circuit whose input signal frequency (f_s) is accompanied by a spurious signal (f_N), will contain spurious at a great number of frequencies $\left[\frac{n}{4}f_s \pm f_N \right]$. Such a prolific family of spurious frequencies has an excellent chance of either immediately including or subsequently producing an in-band spurious product. This is just one example of how spurious products can and do result in "indirect" ways.

4.1.3.1.2.2 Stray Mixer Currents

The problem here arose from the fact that each mixer had not been mounted on the same wafer as its drive circuit, and that the communicating link between them involved a motherboard, and did not, due to space problems, involve coaxial fittings. The problem was particularly troublesome through allowing mutual contamination of component frequencies. (See Section 4.1.3.1.1.3 above), but also was found to contaminate the output of the "C" wafer which essentially constitutes the synthesizer output. The cure for this particular manifestation was to shield the active

circuitry and the output network of the "C" wafer from the mixer and bandpass filter, in order to better define ground paths on the wafer. The same problem occurred on the "B" wafers, but here it was adequate to separate ground areas on the "B" wafer, one area for the mixer circuit, the other area for the remainder of the circuitry. Also, ground conductances were augmented by adding a silver strap between key points on the ground structure.

4.1.3.1.2.3 Imperfect Shield Wall Between "A" and "B" and Between "A" and "C" Wafers

Another mechanism existed to allow mixer L.O. frequencies access to bypass the succeeding bandpass filter. This resulted from the coincidence of three unhappy occurrences:

1. The high level circuitry handling to L.O. (mixer drive) frequency on an "A" wafer was located near the edge of the wafer away from the motherboard.
2. The low level input circuitry to the corresponding "B" (or "C") wafer occupied the same part of that wafer.
3. The shield wall separating each A/B or A/C wafer pair was soldered to the wafer-pair cover only at intermittent "points" in this area.

Soldering the shield wall continuously along its length removed this source of contamination.

4.1.3.1.2.4 "D" Wafer - Ground Impedance Problem

The harmonics of the divide-by-three output frequency were found to be contaminating the component frequency outputs of the "D" wafer. This was traced to the existence of over two ohms of resistance accumulating in the ground return conductor from one corner of the wafer to one diagonally opposite, where the wafer ground lead was attached. This crosstalk was brought to an acceptable magnitude by adding a short silver strap from the remote corner to the immediate rear face (1 "square" of resistance), already grounded.

4.1.3.1.2.5 Leakage of Harmonics of "2 MHz" Divide-by-Four Output Frequency to Succeeding Mixer Input

This problem, again attributable to ground path coupling, was only significant at the "C" wafer where it was solved by the addition of a series-tuned filter at the mixer input.

4.1.3.1.2.6 Contamination of Input (Reference Frequency) Line by Component Frequencies

In order to bring the level of this contamination to within specification (70 db) it was necessary both to augment the ground conductors connecting the X/Y wafer pair assembly to the component frequency generator assembly and to insert another series-tuned filter in the input path.

4.1.3.2 Mixer Products, Spurious, In-band

In the present design there exist two pairs of mixer-generated frequencies which, in general, constitute higher-order in-band spurious signals. These are as follows:

$$\text{4th order pair: } \begin{cases} 2\omega - 2\alpha \\ 4\alpha \end{cases}$$

$$\text{8th order pair: } \begin{cases} 3\omega - 5\alpha \\ -\omega + 7\alpha \end{cases}$$

where ω \equiv mixer L.O. frequency

and α \equiv ± 4 output frequency (mixer input "signal" frequency)

The fourth order pair, although of relatively low order, involves only even multiples of the parent frequencies and, since the design is a doubly-balanced mixer (Ruthroff transformers), the suppression of this pair is good. The eighth order pair is inherently good because of the high order. In order to assure adequate margin in meeting the signal "purity" requirement, however, it was necessary to take certain measures, determined experimentally. They were as follows:

1. It was found that, with this particular mixer configuration and type of diode quad, a current source L.O. drive provided improved suppression of spurious.
2. Not surprisingly, some padding was required between the mixer output and the input to the bandpass filter. A shunt resistor of 51 ohms was satisfactory.
3. Improved limiting was required on the "C" wafer to provide the expected advantage afforded by a "hard limiter" in removing equivalent spurious amplitude modulation produced by the presence of a single spurious spectral line.

4.1.4 Performance Attained

The output spectral purity (signal to individual discrete spurious ratio) attained in these synthesizers was

$$S/N \geq 61 \text{ db} \quad [\text{worst-case selection of frequency}]$$

and

$$65 \leq S/N \leq 75 \text{ db} \quad [\text{typical-case selection of frequency}]$$

The specification required a minimum of 60 db.

4.1.5 Promising Avenues toward Future Improvement

Experience gained to date suggest that the following design changes would contribute to a synthesizer of yet higher spectral purity.

4.1.5.1 "D" Wafer Changes

4.1.5.1.1 Magnetic Coupling Reduction

Presently the input and output lead pairs for each component frequency are connected to the pad areas on the motherboard through separate holes and, in doing so, form a loop. It is felt that by twisting each pair, input and output, and passing each such pair (eight in all) through individual holes in the motherboard, the magnetic cross-coupling would be reduced greatly, and the need for "compensating loops" on the "D" wafer would be avoided.

4.1.5.2 Motherboard Changes

4.1.5.2.1. Increased Shielding

It would be advisable to fill in ground etch as much as possible on each level of the multi-layer motherboard. It is further suggested that printed-through grounds be employed "in profusion", to achieve redundancy in shielding, particularly adjacent to critical signal conductors buried within the motherboard.

4.1.5.2.2 Reduction of Magnetic Coupling

It would be advisable to transpose periodically the printed conductors of each component frequency line pair so as to simulate twisted pair and thus reduce greatly the magnetic coupling induced on the motherboard. It is suggested that care be taken to stagger transposition periods (distances between cross-overs) from line to line.

4.1.5.3 Wafer Changes ("A", "B", "C" Wafers)

4.1.5.3.1 General - All wafers should be individually shielded in their separate enclosures or envelopes, each mounted separately to the motherboard. Each such envelope should be sealed electrically by soldering a cover plate over the wafer.

4.1.5.3.2 "A" Wafer Changes

4.1.5.3.2.1 Ceramic Wafers

Care must be taken in the laying-down of conductor paths to take advantage of lower achievable conductor and node resistance and to allow erection of electrostatic shield walls between diode switches.

4.1.5.3.2.2 Relocation of Mixer

Include the mixer on the "A" wafer to avoid unnecessary crosstalk arising from involving an extensive ground return path for the mixer drive current.

4.1.5.3.2.3 Improved Mixer

Use a more highly balanced mixer (purchase from a vendor with this capability in a suitably small package).

4.1.5.3.2.4 Transformer Coupling

Transformer-couple the outputs of the diode R.F. switches to further control ground impedance-induced crosstalk.

4.1.5.3.3 "B" and "C" Wafer Changes

4.1.5.3.3.1 Increased Gain

Increase sensitivity by adding gain, avoiding limiting in any feedback amplifiers. The addition of linear gain, followed by a hard limiter, will allow more padding to be inserted between the mixer and the band-pass filter, and will insure realization of optimum improvement in signal/noise in traversing the wafer.

4.2 Phase Settling Time ("Switching Time")

4.2.1 Definition:

The specification requires that, upon a frequency change command involving all of the 15 most significant bits (and no others), the output phase of the synthesizer be (and stay thereafter) within $(45/16)$ electrical degrees of steady state value, after a maximum elapsed time of 20 microseconds.

4.2.2 Design Considerations

The main design consideration with respect to this transient response requirement was the assumption that the total delay would approximate the sums of the delays of the (10) individual band-pass filters required in the synthesis chain of mix-and-divide modules. Using envelope delay of the filters as a measure of this transient requirement, the design employed suggested an overall settling time of about 15 microseconds would be attained.

4.2.3 Problem Areas and Their Status

4.2.3.1 General

The switching time actually attained (≤ 24 microseconds) was quite often in excess of the maximum specified. Invariably, this would occur when calling for a change to a synthesizer frequency requiring the selection of the highest of the four component frequencies (f_4) at the majority of the "A" wafers.

Per this report, it cannot be reported that this problem has been solved. Certain areas have been studied, in whole or in part, and certain other areas remain to be examined in the search for the reason for this phenomenon.

4.2.3.2 Inadequate dynamic range of "B" Wafer

Since the calling for a change in frequency results in a transient superposition of two waveforms of similar frequency, one decaying and one growing, the sum waveform at each consecutive filter output may be expected to undergo a "pseudo-null", on a transient basis. If there is inadequate gain interposed between the filter and the divide-by-four circuit, the divide-by-four circuit will cease triggering temporarily until the "null" period has passed.

The gain of the feedback (I.C.) amplifier on the "B" wafer was increased slightly, increasing the margin of overdrive under steady-state sinusoidal signal conditions from about 5 db to perhaps 10 db. (This was done by grounding both pins 1 and 2 of the SE-501G flatpack.) No improve-

ment was seen (but the change in circuit has been retained). It may be worthwhile in future work to try a greater gain margin (say 20 db).

4.2.3.3 Component Frequency Line Transients

Tests run at Lincoln Laboratory (M.I.T.) suggested some correlation between transients seen to occur on the component frequency lines and the occasion of the worst-case settling time measurements. Future work should pursue this. If the current transient delivered to the supply (component frequency) lines due to "A" wafer R.F. switch action should prove contributory to the problem, a higher input impedance to the "A" wafer would be worthwhile trying for effect, to reduce this transient in current.

4.2.3.4 Limiting in Feedback Amplifier

The amplifier on the "B" wafer can limit during an additive transient condition. A limiting feedback amplifier such as this might produce erratic phase behavior at the divide-by-four input. A better choice would be a linear amplifier followed by a hard limiter.

4.2.3.5 Filter Design/Topology

It is possible that a filter design of different topology might be less given to delay of the type defined herein although theory, in terms of "envelope delay", does not suggest this. An experimental comparison would be interesting, but costly.

CONCLUSIONS

A synthesizer of the same design, as that discussed here, but incorporating the refinements suggested in sections 4.1.5 and 4.2.3, may be expected to exhibit spurious suppression greater than 85 db and switching time on the order of 10 (ten) microseconds.

Current component availability suggests the feasibility of direct synthesis in the 30 to 50 MHz region using this basic design approach. The advantage of scaling the center frequency in this manner is an approximate inverse reduction in switching time. In the case of a 50 MHz synthesizer, a switching time of approximately 2 (two) microseconds may be achieved, adequately short for very high data rate systems.

This type of synthesizer is inherently limited to a maximum of about 0.1 for the ratio of tuning range to center frequency. Any application requiring a higher ratio can be accommodated by an appropriate combination of frequency multiplication and/or translation subsequent to the direct synthesis. It should be noted, however, that switching speed cannot be reduced by such manipulations and that spectral purity is sacrificed by frequency multiplication after synthesis.

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