ESD-TR-67-356

MTR-362

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DESIGN CONSIDERATIONS FOR FORWARD ERROR CONTROL EQUIPMENT FOR HF RADIO

AUGUST 1967

K. Brayer

Prepared for
AEROSPACE INSTRUMENTATION
PROGRAM OFFICE
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Massachusetts

Project 705B
Prepared by
THE MITRE CORPORATION
Bedford, Massachusetts
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FOREWORD

This report was prepared by the Range Communications Planning and Technology Subdepartment of The MITRE Corporation, Bedford, Massachusetts, under Contract AF 19(628)-5165. The work was directed by the Development Engineering Division under the Aerospace Instrumentation Program Office, Air Force Electronics Systems Division, Laurence G. Hanscom Field, Bedford, Massachusetts. Captain J. J. Centofanti served as the Air Force Project Monitor for this program, identifiable as ESD (ESSI) Project 5932, Range Digital Data Transmission Improvement.

REVIEW AND APPROVAL

Publication of this technical report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

C. H. Horrigan

for OTIS R. HILL, Colonel, USAF
Director of Aerospace Instrumentation

ABSTRACT

The National Range Division (NRD) presently operates high-speed (2400 bits/sec) HF communication links to transmit data back to the Cape Kennedy complex from down range stations such as Ascension Island. Due to the high error rates normally experienced on these HF channels, error correction must be implemented to improve communication. This report deals with the design of an error controller within the constraints of the NRD communications environment.

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INTRODUCTION

To improve communication of digital data on NRD HF circuits, using high-speed modems, it is necessary to add some form of error control to the communications circuits involved. Two such forms of error control are forward error correcting codes, and retransmission methods. This paper deals with the design aspects of forward error control equipment (FEDAC) on the High Frequency radio circuits of the National Range Division (NRD). However, the approach is general and can be used in the design of similar systems for other users.

SECTION II

MODEM DESCRIPTION

The HF modem in use by the NRD is the Philco AN/USC-12. This modem uses twelve information tones to achieve a maximum data rate of 2400 bits/sec. Each tone is keyed at 100 symbols per second (2 bits/symbol) resulting in a 10 millisecond PSK keying interval. The phase-keyed tones are spaced 200 Hz apart in a range from 700 Hz to 2900 Hz. A variety of data rate input options is provided to make the modem versatile from an operational standpoint. The minimum data rate input is 300 bits/sec on any one of eight parallel inputs. All combinations of input data rates of 300, 600, 1200, and 2400 bits/sec are possible provided that the total does not exceed 2400 bits/sec. The data used to evaluate the performance of codes in this paper is error pattern data collected with the AN/USC-12 on a link between Antigua Island and Cape Kennedy and the data previously collected with the Kineplex TE-216 modem, and described in Reference 1.

SECTION III

CONSTRAINTS ON FEDAC CODER DESIGN

As in the case of any equipment design, there are certain restrictions placed upon the designer. The first and most obvious restrictions in this design are that the FEDAC (Forward Error Detection and Correction Equipment) must interface with the modems and must act effectively on the error patterns which result from transmissions with the modem.

MODEM INTERFACE REQUIREMENT

The requirement that the FEDAC interface with the modem constrains the output of the FEDAC to one or more channels of data at 300, 600, 1200, or 2400 bits/sec such that the total is not greater than 2400 bits/sec (for the modems presently considered). Furthermore, since all National Range Division sources have been standardized to single serial data rates of 75×2^m bits/sec (m=1, 2, . . .), the output rate of 2400 bits/sec is eliminated if the input rate is 2400 bits/sec. The above restriction is a function of maximum modem data rate and will be changed by the use of 4800 and 9600 bit/sec modems.

DELAY REQUIREMENT

An additional restriction is that of system delay. It has been specified that the coder must have the capability of operating with no more than 110-millisecond delay in one mode and with as much as a 5-second delay in another mode. Additionally, the information must at all times be transmitted without delay.

CONSTRAINTS ON CODE SELECTION

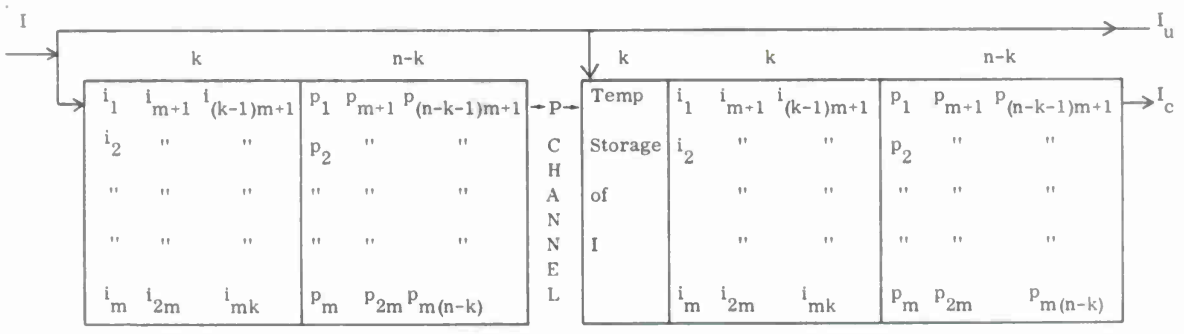
In addition to the requirement that the error correcting code should correct the greatest possible number of errors in digital transmission on the medium, the interface and system delay requirements place initial restrictions on code choice. The interface requirement restricts the allowable code rates (fraction of a total code word which is source information).

The usable code rates are restricted to those code rates compatible with the input and output data rates. For this analysis codes of rate 1/4, 1/2, and 3/4 shall be chosen. The 1/4 rate codes which contain the least information per code word (most redundancy) naturally have the greatest error correction capability. The 3/4 rate codes have the least error correction capability. By choosing these three rates it will be possible to investigate the relationship of redundancy and error correction performance on the digital error patterns.

Additionally, it is required that information and parity (redundancy) from the output of the coder be placed on separate channels of the modem such that if a receive decoder fails, it can be disconnected and the unprotected information will still be available without delay. In order to meet these restrictions it is required that the input to the coder at half rate be 300, 600, or 1200 bits/sec on one channel with output of 300, 600, and 1200 bits/sec each on two channels, one information and the other parity. If the Philco modem is used, the output can be on two separate channels of information and parity. If one channel is needed the Philco modem has, internal to it, the capability of channel multiplexing. If the Kineplex modem is used and one channel is needed, the information and parity must be pre-multiplexed.

PROPOSED IMPLEMENTATION

An implementation which meets the requirements stated is presented below. The technique used is randomized (interleaved) coding. The digital data is read in from the source and transferred as described in Figure 1.



m = randomizer length.

I_u is real time unprotected information.

I_c is delayed corrected information.

Code has n total bits, k information bits, and n-k parity bits.

Figure 1. Interleaver Configuration

The information bits available to the encoder are identified as I_{ji} where j identifies an interval of mk consecutive input bits and i identifies a bit within the interval ($i = 1, 2, \ldots mk$). Similarly, parity bits are identified p_{jr} where r identifies a bit within the interval ($r = 1, 2, \ldots m(n - k)$). In the 1/2 rate mode, data is transmitted in two streams with the bit correspondence (reading from right to left) given on the following page.

$$
\begin{array}{ccccccc}
i_{j+1,1} & i_{j,mk} & \cdots\ i_{j,m+2} & i_{j,m+1} & i_{j,m} & i_{j,2} & i_{j,1} \\
p_{j,1} & p_{j-1,mk} & \cdots\ p_{j-1,m+2} & p_{j-1,m+1} & p_{j-1,m} & p_{j-1,2} & p_{j-1,1}
\end{array}
$$

When a multiplexed output is necessary, the parity stream is delayed 1/2 bit at the information rate and the two streams are multiplexed onto a single stream at twice the information rate.

In the 1/4 rate mode two streams one information and one parity, are generated internally. Reading from right to left they are structured as given below:

$$
\begin{array}{cccccccccccc}
i_{j+1,1} & & & i_{j,mk} & \cdots\ i_{j,3} & & i_{j,2} & & & & & i_{j,1} \\
p_{j,1} & p_{j-1,m(n-k)} & p_{j-1,m(n-k)-1} & p_{j-1,m(n-k)-2} & \cdots\ p_{j-1,7} & p_{j-1,6} & p_{j-1,5} & p_{j-1,4} & p_{j-1,3} & p_{j-1,2} & p_{j-1,1}
\end{array}
$$

If there is more than one output stream the information stream is one such stream and the internal parity stream is broken into three output streams all at the information data rate. The bits which are encoded together (using the column notation of Figure 1) are:

$$
\begin{array}{ccccc}
i_{(k-1)m+1+s} & \cdots & i_{2m+1+s}\ i_{m+1+s} & i_{1+s} & \\
 & & & & s = 0, 1, \ldots m-1 \\
p_{(n-k-1)m+1+s} & \cdots & p_{2m+1+s}\ p_{m+1+s} & p_{1+s} &
\end{array}
$$

The actual system can be constructed either as a double subscripted storage system or as storage along a line. If the decoder fails, it can be removed from the circuit and the information (unprotected) is directly available. The delay of the system is the time it takes to receive the necessary information and parity plus any decoding time. At the maximum channel speed of 2400 bits/sec, logic is available such that decoding can take place at speeds higher than the data rate, thus eliminating decoding time from consideration. The

delay time is seen to be 2 mk bit times since it requires m x (k) to receive the information and m x k additional bit times to receive the parity, the total is 2 mk at all rates.

As stated previously, the delay must be no more that 5 seconds or 6000 bits at 1200 bits/sec. Therefore, it is required that $2\ mk \leq 6000$ bits. In the case of a 110 millisecond delay for the same situation

$$2\ mk \leq 132 \text{ bits}$$

In general, if R is the source data rate, then for

maximum delay	$2\ mk \leq 5 \times R$
110 ms delay	$2\ mk \leq 0.1 \times R$

A summary of the restrictions on 2 mk is presented below.

Total Source Data Rate	Maximum Delay	110 ms Delay
300 bits/sec	$2\ mk \leq 1500$	$2\ mk \leq 33$
600 bits/sec	$2\ mk \leq 3000$	$2\ mk \leq 66$
1200 bits/sec	$2\ mk \leq 6000$	$2\ mk \leq 132$

To obtain maximum error correction, it is necessary to test numerous codes (values of n) and randomizers (values of m) against the actual data, rather than arbitrarily selecting codes. Prior to finding the combination of code and randomization (m) which gives the best combined performance, it is possible to make some statements about these values. The randomizing parameter has previously been shown to be best if it is a prime number. [1] The reason for this is that errors tend to occur periodically in the measured channels. If m is the same as this periodicity, the tendency is to lump all the errors in a few code words and thus fail to correct most of the errors. To protect against all values of periodicity (none of which are prime) a prime number is chosen.

Additionally, the decoder must have the capability to output the received uncorrected information if it detects a number of errors beyond its error correction capability. The primary reason for this is if there are excessive errors, the received error vector may be close to some code vector such that the distance from the decoded vector to the error vector is less than the distance from the actual source code vector to the error vector. In this case, it is well known that the output information may have more errors than the received incorrect information. The decoder has generated errors. It might be argued that these additional bit errors are unimportant since most sources transmit on a message basis and not a bit basis, and if a message is in error, it does not matter how many errors it has. Examination of the randomization method, however, indicates that the n information bits encoded together are separated each from the next by (m - 1) bits. Thus, if the decoder generates new errors, they will be separated by (m - 1) bits and, if a message is less than m bits long, new message errors are generated. As an example, if a code can correct three errors in a 24-bit block with 12 information bits, and four errors occur, a correction failure will generate new errors. Suppose the new number of errors is six and the source uses a 12-bit message and m = 12. The output of the decoder will contain six 12-bit words all in error. However, if the information received at the decoder is output, only three words are in error. The code must have the capability of correcting errors and detecting at least e + 1 errors so that the received information bits can be output, without correction, thus reducing message error generation.

SECTION IV

PLANNED EVALUATION OF CODES

The NRD is presently using 12-tone PSK Philco modems for HF transmission. However, the selected codes shall be evaluated for performance against data collected with both modems previously described. We shall use the data previously described [2, 3, 4] and data collected in December of 1966 using the Philco modem in one-way transmission from Antigua to Cape Kennedy.

Since the errors in the channel occur in bursts and since delay is permitted, there is an initial designer's choice between using long symbol codes or short random error correcting binary codes and a randomizing device. It is difficult to meet the requirement of no delay in information transmission with symbol codes, and there is no continuously variable delay capability as will be shown for binary codes with randomizers. For the purposes of this study, it has been decided to use random error correcting binary codes with randomization. The randomizer selected is the same one discussed in Section III. This randomizer has been demonstrated to be the best one* for the types of error patterns observed. A set of short block codes** has been selected for examination in conjunction with interleaving. These codes are described by the form (n, k, e) where k is the number of information bits, n is the total of information and parity bits, and e is the number of correctable errors. The codes are shown in Table I.

---

* The improvement data is correct only for interleaver lengths where $|m - rp|$ is a maximum, where p is the periodicity of errors (16 for TE-216, 12 for Philco AN/USC-12) and r is a non-negative integer.

** The (24, 6, 4) is a block code. The (24, 18, 1) is a Hamming code and other codes are modified BCH codes and the Modified Golay Code.

Table I

Codes to be Evaluated

1/4 rate	1/2 rate	3/4 rate
	(8,4,1)	
(16,4,3)	(16,8,2)	
(24,6,4)	(24,12,3)	(24,18,1)
	(32,16,3)	(32,24,1)

The performance of these codes in terms of improvement factor (uncoded error rate/decoded error rate) on data collected with the TE-216 modem is presented in Figures 2 through 4. [1]

For a given amount of interleaving, the best code gives the greatest improvement. Of the 1/2 and 3/4 rate codes the (24, 12, 3) and (24, 18, 1) perform best on both test samples 309 and 339. Of the 1/4 rate codes, the (24, 6, 4) gives superior performance to the (16, 4, 3) but the (16, 4, 3) is more easily implemented in terms of the delay requirement.* Based upon this performance the (24, 12, 3) code has been chosen for consideration along with the (16, 4, 3), and the (24, 18, 1)* as codes for evaluation with the AN/USC-12 data. As with the Kineplex data, typical AN/USC-12 data has been selected for evaluation. The consecutive error and gap distributions of this data are presented in Table II and Figure 5. Using previously developed evaluation techniques [1] it is clear that we have one test run with random and periodic

* The (16, 4, 3) and (24, 18, 1) codes have been chosen because they are easily implemented cyclic codes. The (24, 6, 4) code is a block code which must be constructed by storage of a code book and decoded by table lookup. The size of the table for the (24, 6, 4) is $2^k \cdot 2^{n-k} = 2^6 \cdot 2^{18}$, over ten-million elements and is impractical to construct. The (16, 4, 3) code is a modified (15, 5, 3) code and has available one bit for error detection and one for synchronization. The (24, 18, 1) is a single error correcting, double error detecting Hamming Code.

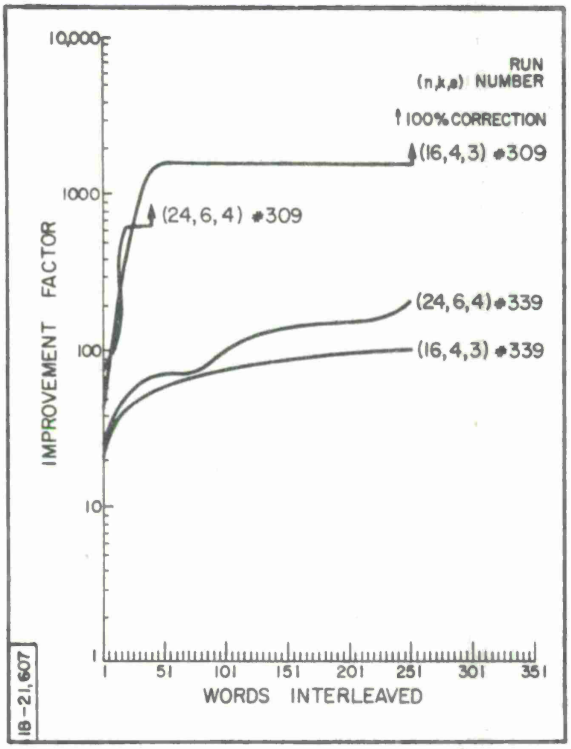


Figure 2. Kineplex Data, 1/4 Rate Codes

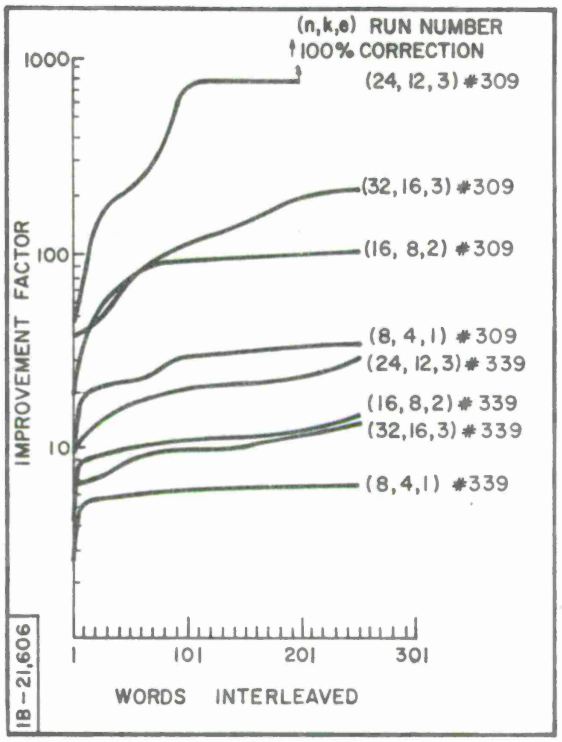


Figure 3. Kineplex Data, 1/2 Rate Codes

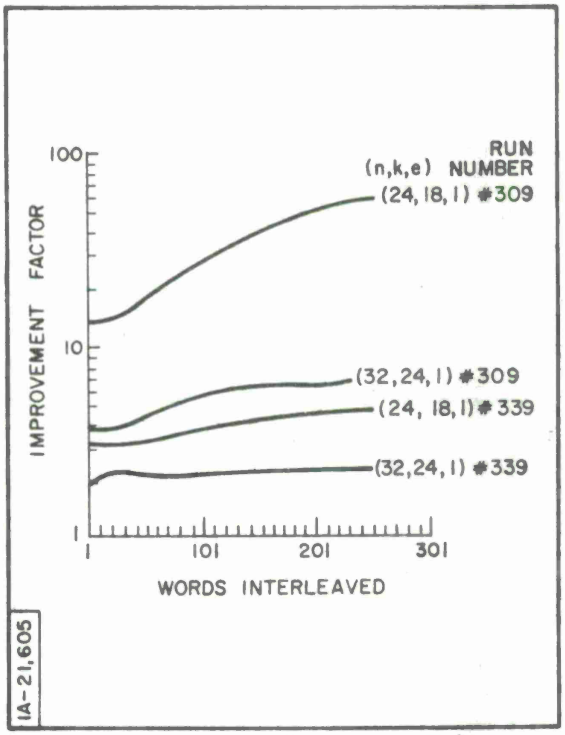


Figure 4. Kineplex Data, 3/4 Rate Codes

errors (Run 12) and one run with short high density bursts (Run 24). The performance of the codes with these two runs is presented in Figure 6. As expected in the run with bursts, the improvement increases with interleaving. However, in the test run which is near random to start with, interleaving serves only to re-order the errors into bursts. Additional interleaving randomizes these bursts and regains the error correction. The output message error rates for this data are presented in Figure 7. The figure demonstrates that the use of interleaving in the random environment has actually increased the output message error rate for some values of m. A summary of the results to this point is contained in Table III.

Considering the results on the restricted set of test runs a number of points become apparent. Examination of the improvement curves indicates that improvement increases rapidly with delay up to approximately 89 words of interleaving. Beyond that point the few errors which remain are difficult to correct through the interleaving technique. Furthermore for $m > 247$ improvement becomes virtually independent of delay with the result that equipment complexity is increased with no benefit to the communications system. It is also apparent from Figure 7 that extreme care must be exercised in the actual operation of FEDAC equipment because of possible channel degradation.

At the beginning of this study it was decided to examine 3/4, 1/2, and 1/4 rate codes. This class was further reduced in size when it was determined that at 300 bit/sec, and with no interleaving, the maximum delay permitted is 33 bits. As a result of the performance of the evaluated 3/4 rate codes, it is evident that the improvement gain does not justify their implementation.

As a final evaluation of the expected performance of these codes the codes were evaluated against more than 5 hours of data collected with the

TE-216 modem and more than 15 hours of data collected with the AN/USC-12. The gross error rate results are presented in Table IV, and the total channel performance is presented in Figures 8 and 9. The interval lengths were chosen according to the code rate (e.g., a 10-minute uncoded channel interval after decoding by a 1/2 rate code is a 5-minute interval decoded channel). From these figures the observation can be made that, through the use of the previously described interleaved codes, it is possible to take a poor channel and create an excellent communications channel.

Table II

Distribution of Consecutive Errors

Consecutive Errors	Run 12	Run 24
1	34,511	252
2	460	53
3	7	--
	--	--
Total Errors	35,452	358

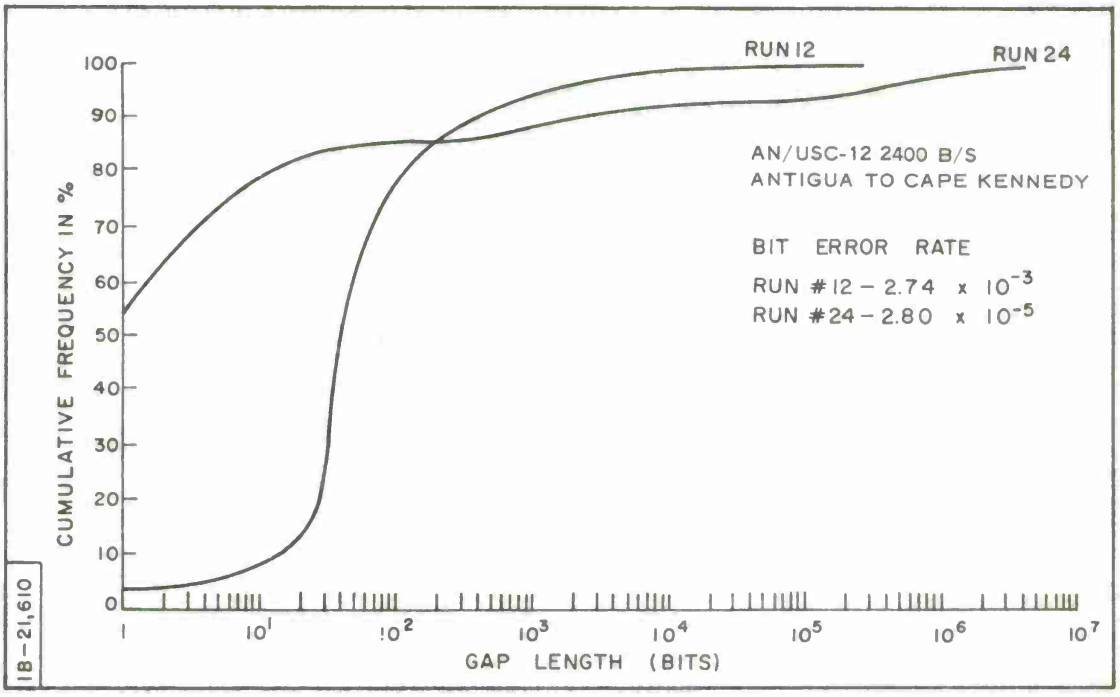


Figure 5. Distribution of Error Free Intervals

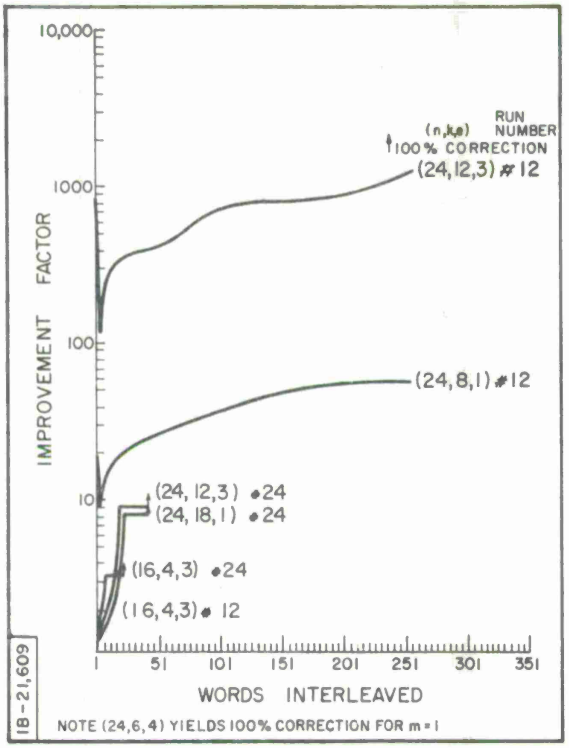


Figure 6. Improvement Factor for AN/USC-12 Data

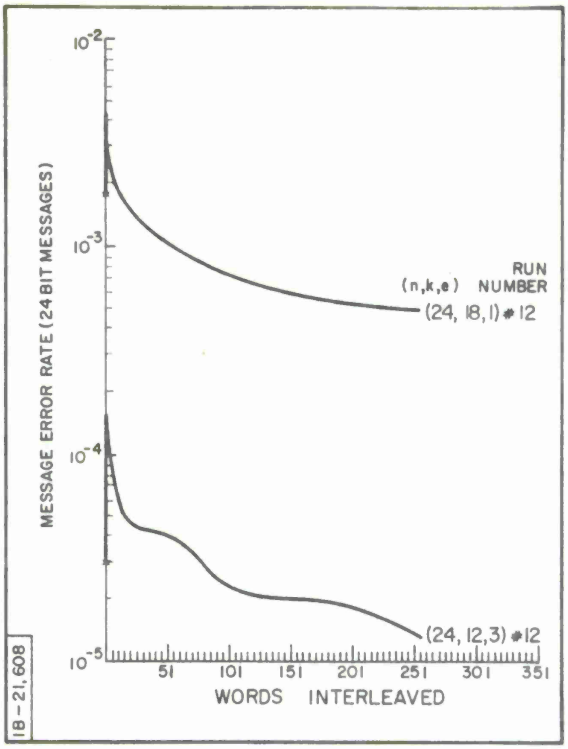


Figure 7. Effect of Interleaving on Message Error Rates in a Near Random Case

Table III

Summary of Code Performance

Test Run Number (BER)	Error Pattern Type	Code	Improvement Factor
309 (4.3×10^{-3})	Low Density Bursts and Periodic Errors	(16, 4, 3)	Infinity
		(24, 12, 3)	"
		(24, 18, 1)	60
339 (1.2×10^{-2})	Low Density Bursts	(16, 4, 3)	80
		(24, 12, 3)	30
		(24, 18, 1)	5
12 (2.7×10^{-3})	Near Random Errors	(16, 4, 3)	Infinity
		(24, 12, 3)	1000
		(24, 18, 1)	80
24 (2.8×10^{-5})	High Density Short Bursts	(16, 4, 3)	Infinity
		(24, 12, 3)	"
		(24, 18, 1)	"

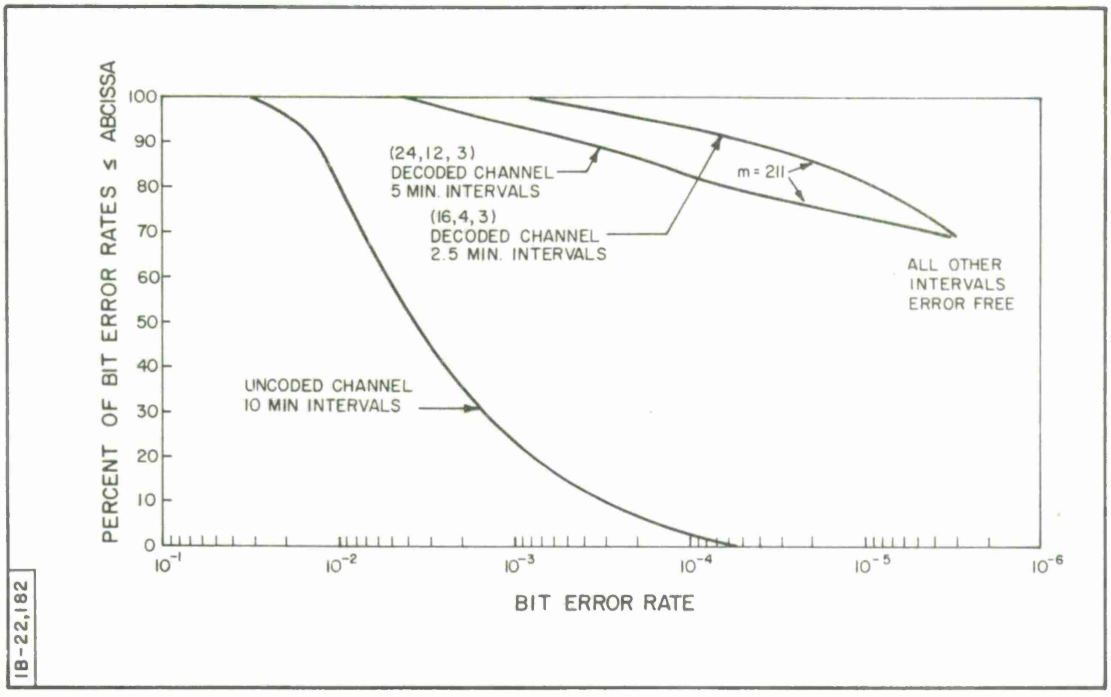


Figure 8. Cumulative Performance in TE-216 Channel

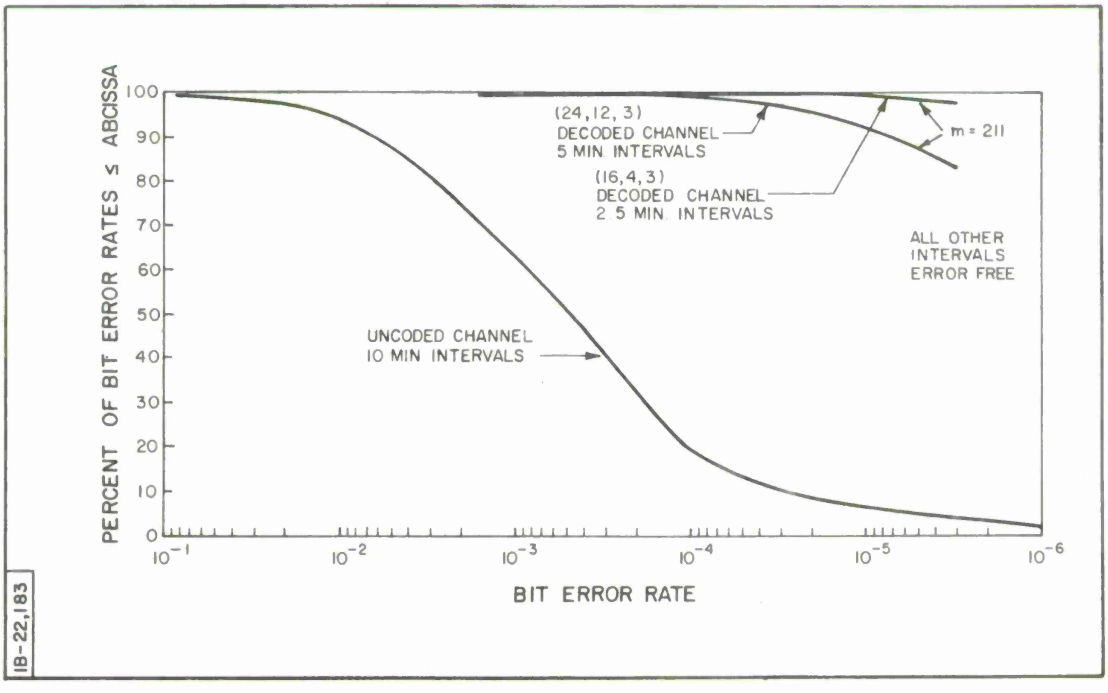


Figure 9. Cumulative Performance in AN/USC-12 Channel

Table IV

Code Performance on Large Data Samples

Modem	TE-216	AN/USC-12
Channel Data Rate	2400 bits/sec	2400 bits/sec
Total Bits	4.8×10^{7}	1.4×10^{8}
Total Errors	2.6×10^{5}	2.5×10^{5}
Error Rate	5.4×10^{-3}	1.7×10^{-3}
Output Error Rate (24, 12, 3) Code m = 211	9.3×10^{-5}	4.7×10^{-6}
Output Error Rate (16, 4, 3) Code m = 211	1.6×10^{-5}	2.1×10^{-6}

SECTION V

CONCLUSIONS

In this paper the restrictions presented by the NRD communications environment have been used to develop a forward acting error controller which will correct the error patterns observed in the HF channels of the NRD. It has been demonstrated that the code selection is actually restricted by other system requirements and in fact is the last thing which can generally be selected. Based upon this analysis, it is recommended that the (24, 12, 3), and (16, 4, 3), cyclic codes be used to give error correction on NRD channels. The maximum interleaver length consistent with less than five seconds delay at 1200 bits/sec information should be 247 words, and the 110 ms delay mode, at 1200 bits/sec, can be accomplished with five words.

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4. K. Brayer, "Error Patterns Measured on Transequatorial HF Communications Links", ESD-TR-67-99, April 1967.

Unclassified

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1 ORIGINATING ACTIVITY *(Corporate author)*

The MITRE Corporation
Bedford, Massachusetts

2a. REPORT SECURITY CLASSIFICATION

Unclassified

2b. GROUP

3 REPORT TITLE

Design Considerations for Forward Error Control Equipment for HF Radio

4 DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

N/A

5. AUTHOR(S) *(First name, middle initial, last name)*

BRAYER, Kenneth

6 REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
August 1967	24	4

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
AF 19(628)-5165	ESD-TR-67-356
b. PROJECT NO. 705B	
c.	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)* MTR-362
d.	

10. DISTRIBUTION STATEMENT

This document has been approved for public release and sale; its distribution is unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Aerospace Instrumentation Program Office, Electronic Systems Division, L. G. Hanscom Field, Bedford, Mass.

13. ABSTRACT

The National Range Division (NRD) presently operates high-speed (2400 bits/sec) HF communication links to transmit data back to the Cape Kennedy complex from down range stations such as Ascension Island. Due to the high error rates normally experienced on these HF channels, error correction must be implemented to improve communication. This report deals with the design of an error controller within the constraints of the NRD communications environment.

DD FORM 1 NOV 65 1473

Unclassified

Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
SYSTEMS AND MECHANISMS						
Data Transmission Systems						
Multichannel Radio Systems						
Voice Communication (HF) Systems						
INFORMATION THEORY						
Coding						
MATHEMATICS						
Statistical Analysis, HF Error Locations						
Statistical Distributions, HF Error Locations						
Statistical Data, HF Error Locations						