NRL Report 6584

A Digital Magnetic Tape System for Recording Radar Data

P. L. Watkins, J. M. Goodman, and A. M. Knopp

Search Radar Branch
Radar Division

July 24, 1967

NAVAL RESEARCH LABORATORY
Washington, D.C.

42

CONTENTS

ABSTRACT

A versatile multichannel medium-speed data system for recording radar data on magnetic tape directly in digital-computer format was designed for use with the Randle Cliff Radar facility at the Naval Research Laboratory's Chesapeake Bay Division, and it is currently installed and operating there.

Input data to the system can be analog voltages, which are internally digitized, or digital codes. Timing and reference data are internally generated. The system operates with three simultaneous data scanning rates: (a) basic (radar pulse repetition frequency), (b) submultiple, and (c) a multiple of the basic. Both the sequence and the amount of data sampled at each rate is patchboard-controlled.

Any basic scan rate from 6 pulses per second to 3 kilo-pulses per second can be generated, depending on the volume of data. Data are recorded as sequential seven-bit characters at constant density, without intermediate storage, over the full range of trigger rates, through the choice of six tape speeds.

Selected portions of the data can be monitored by an on-line printer and lamp display, during recording. Further checks can be made during playback of recorded tapes.

The system has developed into an unusually successful preoperational monitoring device for itself and for nearly the complete radar system, in addition to being a versatile and dependable recording system.

PROBLEM STATUS

The work reported is an introduction to only a portion of a much more comprehensive and continuing project. This is an interim report.

AUTHORIZATION

NRL Problem R02-05
Projects ONR RF 001-02-41-4001
and ARPA Order 32-60, Amendment 7

Manuscript submitted April 25, 1967.

A DIGITAL MAGNETIC TAPE SYSTEM FOR RECORDING RADAR DATA

INTRODUCTION

A previous report* describes a space-research radar system associated with a 150-ft paraboloidal-reflector antenna, now known as the Randle Cliff Radar (RCR) facility, located at the Naval Research Laboratory's Chesapeake Bay Division. A section of that report describes the digital data recording system which was then being designed. Subsequently, the system was constructed and installed at the radar site by the Systems Engineering Laboratories, Inc.,† Fort Lauderdale, Florida. The data system (Fig. 1) became operational in September 1962. Since that time it has been used successfully to record radar data for numerous experiments and measurements.

Since the data format allows direct entry of the tape into a high-speed electronic digital computer (CDC 3800, NRL NAREC, or IBM 7090), research and measurement procedures are greatly facilitated. Computer programs have been written for various kinds of data processing, and laborious manual processing is thereby eliminated. The system has proven to be versatile and reliable. This report describes the detailed design of the system, its modes of operation, and its versatility.

The choice of a method for recording radar data depended on various factors, primarily on the quantity of data to be recorded and the data reduction methods available. In the past, manual, photographic, and paper recording devices and methods were all satisfactory. However, the present-day requirement to analyze large quantities of data in as short a time as possible requires the use of higher density recording media, such as magnetic tape. With magnetic tape the data could be recorded in either analog or digital form.

When the digital method for recording radar data was initially chosen, similar systems had not been designed; thus, few guidelines were available. Analog magnetic tape recordings did not lend themselves readily to analysis without further processing. Moreover, analog recorders suitable for predetection, or video recordings, were new and costly. Thus, the choice of digital magnetic tape recordings was indicated; furthermore, the digital computer, which has superseded most other means of analyzing data at high speeds, was becoming readily available and more versatile. The digital-tape method possessed other advantages such as: (a) compactness (large amounts of data can be stored in a small space), (b) maintenance of accuracy in storage (that is, little deterioration of the stored data), (c) resolution adjustable to the accuracy of the measurement, and (d) flexibility in processing the data.

Subsequently, experience has demonstrated that a combination of digital and analog magnetic-tape recordings is most desirable and that photographic and paper-chart recordings provide readily available visual aids to data analyses. Predetection i-f or postdetection video recordings of the receiver output during the entire interpulse period provides a permanent record of all available signal information which can later be

*"A VHF-UHF Missile and Space-Research Radar with a 150-Foot Steerable Antenna," L.V. Blake, editor, NRL Report 5801, Aug. 27, 1962.
†Contract NONR-3717(00)(X) dated 2 January 1962.

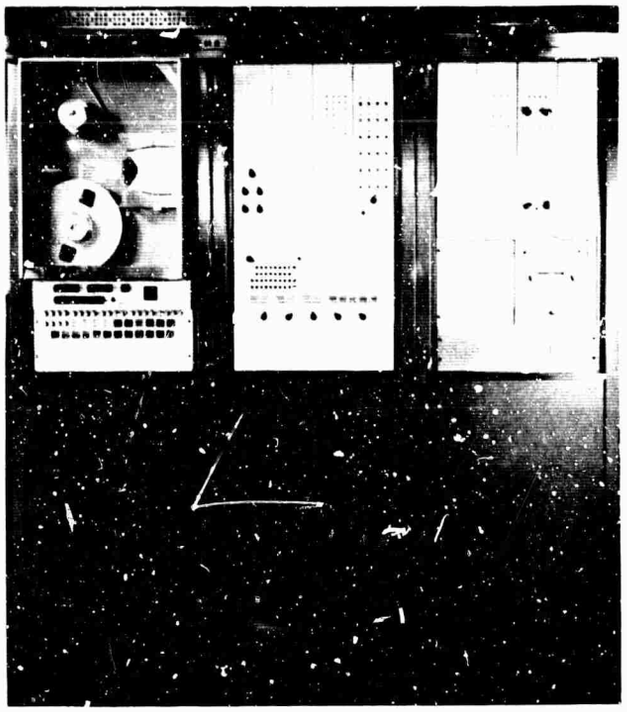

Fig. 1 - Digital data recording system installed at the Randle Cliff Radar facility at the Chesapeake Bay Division of NRL. The left cabinet contains the magnetic tape recorder/reproducer and a radar range digitizer (not described in this report). The center cabinet contains the linearizer, digital multiplexer, sequencer, and analog/digital converter plus the main system display and control panel. The right cabinet contains the analog multiplexer, the data search and selected readout, and the format generator.

translated to digital form. Simultaneous digital recording obtains specific signal information and all other related data necessary for immediate or later analysis.

The major features which were desired and achieved for this recording system are: (a) it must accept many channels of information, (b) it must have a variety of recording rates, (c) it must operate normally at two sampling rates simultaneously, i.e., fast and slow data rates, with the fast data rate capable of being increased for observing special effects on a limited number of inputs, (d) its data groups must be long enough to provide adequate statistical sampling, (e) it must be capable of recording in computer format without transcribing or processing, (f) it must be capable of handling data of different precisions, i.e., the number of significant digits it can record must be variable within limits, (g) it must be capable of readily changing format, such as length and sequence, (h) it must contain adequate checking features, such as on-line monitoring during recording and during playback, (i) it must operate without large and costly intermediate storage devices (instead, it may have a variety of recording rates for various input rates), (j) it must use the magnetic-tape recording medium efficiently in order to provide for lower tape speeds for a slower input data rate, and (k) it must be adaptable to expansion.

Subsequent to the design of this system, the cost and size of high-speed memory devices have been drastically reduced. Also, incremental tape recorders have been developed which can accept low-speed intermittent data rates. Data recording systems of more recent design incorporate one or both of these devices when a wide range of data rates must be accepted. However, the data-rate versatility of this system was achieved without either of them.

In the system obtained, data are recorded usually in a straight binary code on magnetic tape in a modified International Business Machine (IBM) format compatible for direct entry into the IBM 704, 709, or 7090, NRL's Naval Research Computer (NAREC), or the newly leased CDC 3800. The system operates in record or playback mode at several speeds. It has facilities for producing a printed record and driving low-speed analog output displays, and with slight modifications it could have facilities for producing punched cards or tape.

DEFINITIONS

In the description of the data system, some special terms will be used. Their definitions follow.

A frame is a complete scan of data, usually within one pulse-repetition-frequency (prf) period. However, in some cases a prf-countdown is used, so that out of n prf periods the data from only one are recorded, and data from (n - 1) are not recorded. In these cases the frame time for the one recorded period may extend over the entire n prf periods. In any case, the frame consists of the totality of data recorded during the frame time.

The reference time for a frame is a pulse derived from the echo range gate in the electronic tracking unit of the radar. Thus the radar echo, and not the transmitter pulse, provides the reference. If the transmitter pulse were used the echo data existing at the start of the frame would be that of the preceding pulse, and recording difficulties would arise. However, using the echo as reference causes the timing stability of the frame rate to be affected by target motion. The instability thus engendered is, for the worst expected case of a 25,000 mph (escape velocity) target, about one part in 10^4.

Data to be recorded can be grouped in two categories called fast and slow data. Fast data are those which occur or change with every transmitter pulse. Examples are target-echo pulse amplitudes, target range, antenna pointing angles, and the like. These data are recorded in each frame. Slow data are those which do not change appreciably during one prf period but which can or do change enough over a longer period to warrant being recorded. An individual slow-data quantity (e.g., transmitter power, calibrating-signal-generator power) may be recorded once every 8, 16, or 32 frames, but some slow-data quantities are recorded on every frame. The slow data may also be referred to as subcommutated data.

The frame rate for the recordings on magnetic tape depends only upon the prf, because a fixed density of pulses or bits per inch on the tape is prescribed by the computer. When a normal prf of 100 pulses per second (pps) is chosen for the radar, the maximum frame length is 10,000 μsec.

If the frame time is divided into 120 segments, the time of each segment will be 83.3 μsec. The data in these segments are called characters. A character is a group of seven parallel bits or pulses entered simultaneously across the width of the tape.

The maximum number of characters per frame is 120. Although arbitrarily chosen, this number is based on two requirements: (a) 120 is divisible by both six and eight

(which are the numbers of characters in computer words) and (b) many inputs are necessary. If data could be represented by two characters, the system would have the capability of recording 60 different data or input channels during each frame.

Zero characters refer to two conditions: a data zero condition is caused when the data has a zero value, or when nonconsecutive sampling pulses are used within a frame. An automatic zero condition occurs between the end of frame and start of next frame, when the frame rate is not exactly synchronous with the radar prf. For a data zero condition there may be frame, channel, and parity bits. For the automatic zero condition only a parity bit will be recorded.

An input channel is a particular data source.

A data group is the assembly of information from a data source into either two, four, or six consecutive characters. For frame rate data it is equivalent to a tape channel.

A tape channel is a group of characters on the tape — usually from one particular data source but sometimes from more than one source or from the same data source sampled more than once during a given interval or frame. (The latter may be referred to as supercommutation.) The tape channel consists of two, four, or six characters and is equivalent to a primary format channel.

The primary format is the assignment of data to tape channels and words within a frame.

A basic scan represents one pass through the primary format. The basic scan rate is equivalent to the frame rate.

The subcommutation format is the assignment of data to the subcommutated tape channels within each frame of the subcommutation cycle. The subcommutation cycle consists of 8, 16, or 32 consecutive frames, after which the sampling of the data is repeated.

The supercommutation format is the assignment of data to the supercommutated tape channels within the frame. Two data groups may be sampled twice within the frame or one data group may be sampled up to four times within the frame.

The arrangement number refer to a particular sequence in which data is sampled.

A character rate is the transfer rate of data onto magnetic tape, which is variable to maintain a constant character density of 200 bits/in. (bpi) at tape speeds of 120 in./sec (ips), 60 ips, 30 ips, 15 ips, 7-1/2 ips, and 3-3/4 ips. Therefore, the character rates are, respectively, 24 kc/sec, 12 kc/sec, 6 kc/sec, 3 kc/sec, 1.5 kc/sec, and 750 c/sec.

The word rate is the rate at which words, selectable as either six or eight characters, are recorded. Since there are six possible recording character rates, and two possible character groupings in a word, there are twelve different word rates depending on tape speed and format.

A complete record will group together a number of frames of data, arbitrarily chosen to be between 16 and 512 frames. This grouping is called a block of data.

A file is a group of consecutive blocks recorded from the same test and using the same format.

Standard computer format for the IBM 700 or 7000 series and the NRL NAREC or CDC 3800 requires the use of seven-track 1/2-in. magnetic tape in the proper coding and density. The correct bit-density is 200 pulses per inch of tape.

A track is a row of pulses or bits entered serially along the length of the tape.

For the proper coding, the choice lay between a straight-binary code and a binary-coded decimal (BCD) code. The former was chosen because it was the most efficient for computer processing; also, it provided greater precision and used less tape space. Because computers operate only in the binary mode, the BCD would have to be translated to binary; thus, the machine time required to extract and prepare data for computation was determined to be considerably greater than that used for straight binary directly. One limitation to binary is that visual displays of real quantities require translation to be meaningful.

The format finally used is a modified IBM format that is directly acceptable, however. This format is composed of four data tracks, two synchronization or identification tracks, and one lateral-parity track. The format description designation (Fig. 2) gives a more graphic representation of the variety of possible data that can be recorded in a frame of data, and it shows the relative location of these data on the magnetic tape. It indicates those data items that are subcommutated or supercommutated and their respective frame-number locations. The format designation allows one to reconstruct a format without identifying the information of any particular entry. For example, the format designation of 6-43-96-3, S4-44-2, and M4-2-1 represent the primary, subcommutation, and supercommutation formats, respectively. The primary format indicates (a) a word length of six characters, (b) 43 tape primary data channels, (c) 96 characters per frame, and (d) the third arrangement of primary data. The subcommutation format numbers indicate (a) four primary data channels subcommutated, (b) 44 data groups subcommutated and (c) the second arrangement of subcommutated data. The supercommutation format numbers indicate (a) four primary data channels supercommutated, (b) two data groups supercommutated, and (c) the first arrangement of supercommutated data.

On the layout of the format (Fig. 2) it can be seen that time data has been assigned to the first six-character word location and has been designated as channel 1 for the first two-character group and channel 2 for the remaining four-character group. Channel 3 has been assigned to subcommutated data with the items recorded in each frame listed under tape channel 3 of the subcommutation format. Note also that range data in word 4 has been grouped similar to the time data, i.e., a two-character channel 8 is followed by a four-character channel 9. These represented the high and low-order bits, respectively, of the digital range data sampled by sample pulse numbers 10, 11, and 12.

The vertical and horizontal vhf sum signals are sampled as channels 10 and 11. The notation for these channels, L-A and L-B, indicate that these data groups are linearized by functions A and B respectively. The vertical sum data is a supercommutated data group and is sampled again as tape channel 41 in the 16th word. Tape channel 16 in word 7 has been assigned to the elevation error signal with the notation "OS" indicating that an offset has been added to the signal after digitizing.

Referring to the subcommutation format again, it is noted that in tape channel 3 frame numbers 11 through 16 carry an N.U. (not used) designation. This indicates that no data groups have been assigned to these locations. The same is true for frame numbers 10 through 16 under tape channels 24 and 28. This illustrates that not all of the 64 possible subcommutated locations have to be used. Therefore, 10 groups are sampled in channel 3, 16 groups in channel 7, and 9 groups each in channels 24 and 28, respectively, making 44 groups which should agree with the subcommutated channel count registered in frame 9 of tape channel 28.

Format locations labeled N.S. (not significant) indicate that a data position has been sampled, but the data source connected to the position is not significant.

GENERAL EQUIPMENT DESCRIPTION

Recording System

The data recording equipment accepts inputs from various data sources within the radar system and assembles the data in a format directly compatible for subsequent digital computer processing. Additionally, there is an on-line visual-display facility for monitoring the data while recording and during playback of the recorded tape. The system consists of eight major subsystems which are assembled from standard off-the-shelf modular circuits or instruments. It is shown in Fig. 3 in block form.

Program Sequencer — All the timing pulses for the recording modes are generated in a program sequencer. By distributing sampling pulses through a patchboard, any of the data sources can be sampled at various times within the recording cycle. The primary data recording cycle starts with an external trigger pulse, and the length of the basic recording cycle is variable in time up to the total time interval between trigger pulses. The sequencer may also operate from other internal triggers and provide a countdown of the trigger rate, where the recording time interval for the desired number of channels exceeds the time interval between trigger pulses. A subcommutated and a supercommutated recording cycle are also generated for sampling data sources at less than or higher than the basic scan rate. Internal timing is crystal controlled and is subdivided to provide a choice of basic recording rates and to control various external operations. A relative time count and a slow-data channel count are generated within the sequencer unit.

Analog Multiplexers — The analog signal voltages enter the system through the analog multiplexing unit. Sixty-four analog input positions are provided for either normal, slow, or super scan-rate data in four groups of 16 inputs each. They are divided into four groups to provide the necessary isolation between inputs. Each multiplexer position can handle either a unipolar or a bipolar signal variation. An internal precision reference supply is used for calibration and multiplexer testing operations. The outputs of the four input multiplexers feed a secondary multiplexer whose output bus contains the serialized analog data which has been sampled from the patchboard.

Analog-to-Digital Converter and Linearizer — The voltage amplitudes are converted initially to nine bits in straight binary code, sequentially, in an analog-to-digital (A/D) converter representing the full range of input voltage variation. Digital offsets are introduced in a linearizer unit to adjust bipolar signal variations to the same code range as the unipolar signals. Also, selected converter outputs can be linearized according to four separate correction functions, as determined by the patchboard program. All the converter outputs pass through the linearizer whether offsets or corrections are applied or not. The linearizer output is eight data bits in parallel plus an overscale indication bit.

Digital Multiplexer — A digital multiplexer receives the output of the linearizer together with internally generated counter outputs, manually switched data, and externally-generated digital data. The sampling order for all data is controlled by the patchboard program in groups of two, four, or six character tape channels. The output of the digital multiplexer is a sequential pulse train of four data bits in parallel, and a channel marker bit.

Format Generator — A format generator combines the five multiplexer outputs with frame synchronizations and parity checkmarks to form the seven-bit recorded tape character. Channel, frame, and block detection-circuits are included to drive their respective counters during both record and playback modes.

The generation of automatic zeros between frames and the tape gaps between blocks and files are also controlled within the format generator. A system start-stop mode-selector controls the system counters and the tape transport in four recording modes

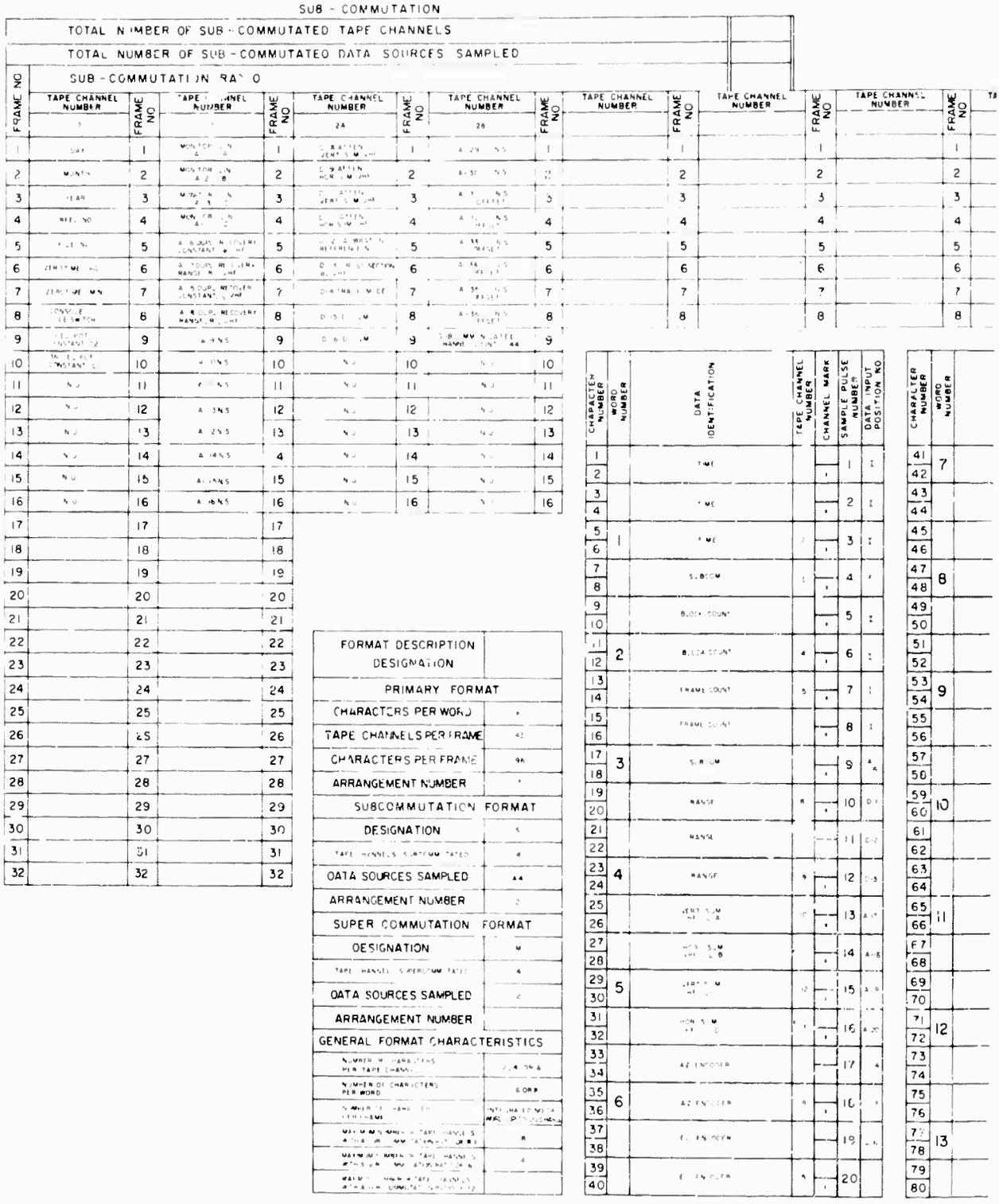

Fig. 2 - Format description, which shows the location of all data s on magnetic tape. A new format sheet is made out and a designat sequence or amount of data recorded is changed.

A

ATION	
ANNELS	
URCES SAMPLED	

FRAME NO	TAPE CHANNEL NUMBER 28	FRAME NO	TAPE CHANNEL NUMBER	FRAME NO	TAPE CHANNEL NUMBER	FRAME NO	TAPE CHANNEL NUMBER	FRAME NO	TAPE CHANNEL NUMBER	FRAME NO
1	A-29 NS	1		1		1		1		1
2	A-30 NS	2		2		2		2		2
3	A-31 NS OFFSET	3		3		3		3		3
4	A-32 NS OFFSET	4		4		4		4		4
5	A-33 NS OFFSET	5		5		5		5		5
6	A-34 NS OFFSET	6		S		6		6		6
7	A-35 NS OFFSET	7		7		7		7		7
8	A-36 NS OFFSET	8		8		8		8		8
9	SUBCOMMUTATED CHANNEL COUNT (AA)	9								
10	NU	10								
11	NU	11								
12	NU	12								
13	NU	13								
14	N	14								
15	NU	15								
16	NU	16								

ABBREVIATIONS	
N S	= NOT SIGNIFICANT (SAMPLED)
N U	= NOT USED (NOT SAMPLED)
•	= CHANNEL MARK LOCATION
A	= ANALOG DATA
D	= DIGITAL DATA
F	= FIXED DATA
I	= INTERNAL DATA
L	= LINEARIZED (FUNCTIONS A, B, C, D)
OS	= OFFSET

DESCRIPTION SIGNATION	
RIMARY FORMAT	
RS PER WORD	6
NELS PER FRAME	41
RS PER FRAME	94
MENT NUMBER	[illegible]
MMUTATION FORMAT	
GNATION	[illegible]
[illegible]	[illegible]
CES SAMPLED	AA
MENT NUMBER	[illegible]
OMMUTATION FORMAT	
NATION	[illegible]
[illegible]	[illegible]
RCES SAMPLED	[illegible]
MENT NUMBER	
RMAT CHARACTERISTICS	
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	
[illegible]	

CHARACTER NUMBER	WORD NUMBER	DATA IDENTIFICATION	TAPE CHANNEL NUMBER	CHANNEL MARK	SAMPLE PULSE NUMBER	DATA INPUT POSITION NO
1 / 2		TIME		•	1	[illegible]
3 / 4		TIME		•	2	[illegible]
5 / 6	1	TIME	[illegible]	•	3	[illegible]
7 / 8		SUBCOM	[illegible]	•	4	[illegible]
9 / 10		BLOCK COUNT		•	5	[illegible]
11 / 12	2	BLOCK COUNT	[illegible]	•	6	[illegible]
13 / 14		FRAME COUNT	[illegible]	•	7	[illegible]
15 / 16		FRAME COUNT	[illegible]	•	8	[illegible]
17 / 18	3	[illegible]	[illegible]	•	9	[illegible]
19 / 20		RANGE	[illegible]	•	10	[illegible]
21 / 22		[illegible]			11	[illegible]
23 / 24	4	RANGE	[illegible]	•	12	[illegible]
25 / 26		[illegible]		•	13	[illegible]
27 / 28		[illegible]	[illegible]	•	14	[illegible]
29 / 30	5	[illegible]		•	15	[illegible]
31 / 32		[illegible]	[illegible]	•	16	[illegible]
33 / 34		[illegible]			17	[illegible]
35 / 36	6	[illegible]	[illegible]	•	18	[illegible]
37 / 38		[illegible]			19	[illegible]
39 / 40		[illegible]	[illegible]	•	20	

CHARACTER NUMBER	WORD NUMBER	DATA IDENTIFICATION	TAPE CHANNEL NUMBER	CHANNEL MARK	SAMPLE PULSE NUMBER	DATA INPUT POSITION NO
41 / 42	7	[illegible]	[illegible]	•	21	[illegible]
43 / 44		[illegible]	[illegible]	•	22	A 22
45 / 46		[illegible]	[illegible]	•	23	[illegible]
47 / 48	8	[illegible]	[illegible]	•	24	[illegible]
49 / 50		[illegible]	[illegible]	•	25	[illegible]
51 / 52		[illegible]	[illegible]	•	26	[illegible]
53 / 54	9	[illegible]	[illegible]	•	27	[illegible]
55 / 56		[illegible]	[illegible]	•	28	A 28
57 / 58		[illegible]	[illegible]	•	29	[illegible]
59 / 60	10	[illegible]	[illegible]	•	30	[illegible]
61 / 62		[illegible]	[illegible]	•	31	[illegible]
63 / 64		[illegible]	[illegible]		32	[illegible]
65 / 66	11	[illegible]	[illegible]	•	33	[illegible]
67 / 68		[illegible]	[illegible]	•	34	[illegible]
69 / 70		[illegible]	[illegible]	•	35	[illegible]
71 / 72	12	[illegible]	[illegible]	•	36	[illegible]
73 / 74		[illegible]	[illegible]	•	37	[illegible]
75 / 76		[illegible]	[illegible]	•	38	[illegible]
77 / 78	13	[illegible]	[illegible]	•	39	[illegible]
79 / 80		[illegible]	[illegible]	•	41	[illegible]

CHARACTER NUMBER	WORD NUMBER	DATA IDENTIFICATION	TAPE CHANNEL NUMBER	CHANNEL MARK	SAMPLE PULSE NUMBER	DATA INPUT POSITION NO
81 / 82		ANALOG NS	[illegible]	•	41	[illegible]
83 / 84	14	[illegible]	[illegible]	•	42	[illegible]
85 / 86		ANALOG NS	[illegible]	•	43	[illegible]
87 / 88		ANALOG NS	[illegible]	•	44	[illegible]
89 / 90	15	ANALOG NS	[illegible]	•	45	[illegible]
91 / 92		[illegible]	[illegible]	•	46	[illegible]
93 / 94		[illegible]	[illegible]		47	[illegible]
95 / 96	16	[illegible]	[illegible]	•	48	[illegible]
97 / 98					49	
99 / 100					50	
101 / 102					51	
103 / 104					52	
105 / 106					53	
107 / 108					54	
109 / 110					55	
111 / 112					56	
113 / 114					57	
115 / 116					58	
117 / 118					59	
119 / 120					60	

- Format description, which shows the location of all data sampled and recorded gnetic tape. A new format sheet is made out and a designation assigned when the nce or amount of data recorded is changed.

B

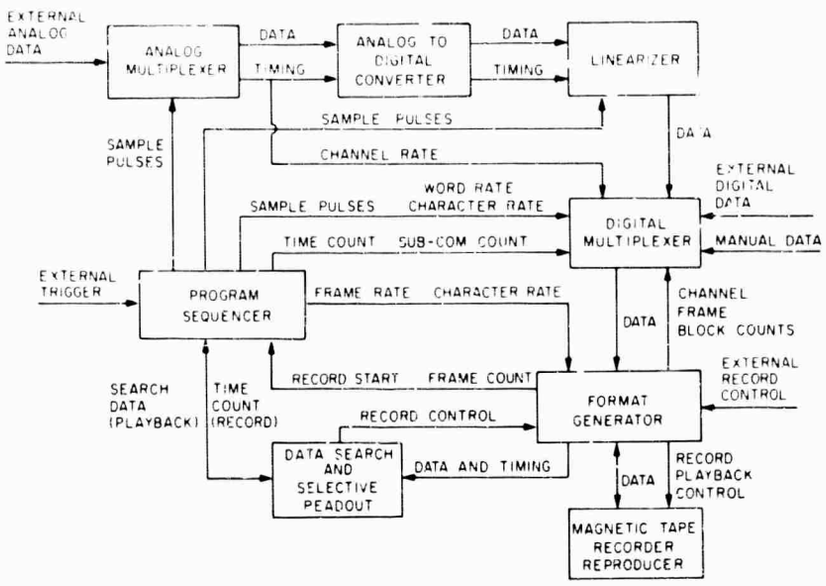

Fig. 3 - Data recording system functional block diagram. The system accepts both analog and digital inputs and generates magnetic tapes for direct computer entry. It also has playback and monitoring facilities.

and two playback modes. During playback the parity generators serve as parity checkers.

Data Search and Readout — During both record and playback operations, a certain portion of the data may be selected for visual display and printing. Additionally, during playback the tape may be searched for particular time or other data-value locations to control the printout and visual displays. All selective data readout operations are controlled separately from the sequencer patchboard which controls the tape format.

Tape Transport — The tape transport has a rapid start and stop time and complete facilities for recording and playback at six speeds. Recordings are made in seven-track IBM- compatible NRZ (non-return to zero) format. The transport can be controlled separately from the rest of the recording system in the local-control mode in both speed, direction of travel, and timing of start-stop operations. In the automatic-control mode the transport start-stop and speed-selection commands are generated in the data recording system. Provisions are included to prevent the writing-over or erasure of previously recorded data when switching from automatic to local control or from record to playback mode.

Digest of System Capability

The eight subsystems which comprise the data system are all solid-state devices. An outline of the pertinent features of each unit is given below.

Program Sequencer –

1. Four triggering modes for generating a primary scan or frame of data: (a) radar trigger, (b) internal oscillator, (c) continuous cycle, and (d) manual.

2. Trigger rate countdown in integral submultiples up to 15:1 for generating data scans at less than the external trigger rate.

3. Six crystal-controlled character rates from 750 pps to 24 kc/sec for maintaining constant character density on the tape at each recording speed.

4. Patchboard control of all data sampling operations: (a) variable data sequencing, (b) adjustable frame length in integral computer word groups up to 120 characters per frame, (c) data grouping as two, four, or six character channels within six or eight character words, (d) subcommutated sampling control at 1/8, 1/16, or 1/32 of the basic frame rate of up to eight channels, (e) supercommutated sampling control of up to four channels at two, three, or four times the basic frame rate, (f) index marking at end of each channel and at beginning and end of frames, and (g) quick program changing through removable prewired patchboards.

5. PRF or frame trigger rates acceptable up to 200 pps for full 120-character frames. Higher trigger rates acceptable for shorter frames. Maximum trigger rate for one-word frame is four kc/sec.

6. Six-bit counter for subcommutated data channels.

7. Twenty-four-bit relative time counter operating in 0.01, 0.001 or 0.0001 second crystal-controlled increments for monitoring and recording frame triggering time interval.

8. Outputs available for external equipment: Time rate, character rate, frame rate, and up to four sample pulses at frame rate, subcommutated rate, or supercommutated rate.

9. Input terminals available for external control: frame rate, time rate, character rate, and time counter start and stop.

Analog Multiplexer –

1. Sixty-four input positions for either bipolar (-10 to +10 volt) or unipolar (0 to +20 volt) signals.

2. Fifty-μsec aperture-time for analog gates at all recording speeds.

3. Less than 10 mv offset to signal source.

4. Separate sampling sequence control for each multiplexer position from sequencer patchboard.

5. Combined linearity and long-term stability are within ±0.2%.

6. 60 dB isolation between multiplexer positions if signal source impedance is 4000 ohms or less.

7. Output buffer amplifier for voltage level and impedance matching to A/D converter.

8. Internal stable reference-voltage source for calibration and testing of multiplexer gates.

9. Other input voltage ranges can be accepted by replacement of output buffer amplifier.

Analog to Digital Converter –

1. 30-kc/sec conversion rate for nine-bit binary code (eight bits plus sign).

2. Bipolar signals converted to code range from -128 to +127, corresponding to multiplexer input range from -10 to +10 volts.

3. Unipolar signals converted to code range from 0 to +255, corresponding to multiplexer input range from 0 to +20 volts.

4. Isolated analog, digital, and chassis grounds.

5. Conversion starts on command signal from analog multiplexer.

6. End-conversion pulse generated after each coding operation.

7. Internal stable reference voltage.

Linearizer –

1. Bipolar output codes from A/D converter converted to unipolar code range (0 to 255) by adding offset code of 128.

2. 0 to 255 code range divided into 16 equal segments.

3. Four separate 16-segment correction functions with two-to-one scale factor for each function.

4. Correction factors from 0 to ±15 in steps of one, or 0 to ±30 in steps of two may be added to each coded analog signal segment.

5. Out-of-limit signal generated for corrected output codes which are negative or greater than +255.

6. Analog channel and function selection for linearizing and bipolar offsetting are controlled from sequencer patchboard.

Digital Multiplexer –

1. All data-input positions consist of up to eight data bits plus a special code mark bit: (a) 16 external digital-input positions of nine bits each, (b) 10 manual code-input positions of nine bits each, (c) nine input positions for sampling internal counters, and (d) one input position of nine bits from linearizer.

2. Logic levels are zero and -6 volts.

3. Sampling of each input position is controlled by the patchboard program.

4. End-of-sample pulses generated for the external digital input channels.

5. All sampled data sources converted to sequential five-bit characters. Each character consists of four data bits and a marker bit indicating the end of the channel in even character positions, and out-of-limits or other special code in odd character positions.

Format Generator –

1. Flow of data and control signals are controlled to and from the tape recorder during record and playback.

2. Lateral and longitudinal parity generated in record modes. Parity checked in playback modes.

3. Channel and frame marks detected for separating channels within words, and frames within blocks.

4. Six-bit channel count and nine-bit frame count generated from detected marks.

5. Block length control in multiples of 16 frames up to 512 frames per block.

6. Block and file gaps generated.

7. Block gap detected and 12-bit block count generated.

8. Four recording modes (continuous, time monitor, calibrate, and remote) and two playback modes (continuous and data search).

9. Recording of automatic zeros controlled between end of one frame and beginning of next to maintain continuous character rate on tape during the block.

10. Seven-line pulse data converted to NRZ format for recording, and skew compensation is provided on playback.

Data Search and Selected Readout –

1. Up to four channels or 12 characters selected for display and/or printout from selected frames during record or playback.

2. Octal or decimal code conversion of up to 16 bits provided for each selected channel.

3. Display/print rates selected in binary submultiples of the frame rate up to 128. Maximum print rate is five frames (lines) per sec.

4. Digital-to-analog (D/A) conversion of any two consecutive characters in one selected channel.

5. Channels located and counted where out-of-limits and special code marks are generated during the recording.

6. Channels located and counted where parity errors are detected during playback.

7. Data readouts and error displays controlled during playback when the data value in a selected channel falls between preset values. This is the playback search mode.

Tape Recorder Reproducer

1. Six recording and playback speeds: 120, 60, 30, 15, 7.5, and 3-3/4 ips.

2. Start and stop times of 3 msec or less.

3. Seven-track NRZ (nonreturn to zero) recording on 1/2-in. magnetic tape.

4. Recording density – 200 characters in.

5. IBM or NARTB reel sizes up to 10-1/2-in. diameter may be used.

6. Protection against tape erasure during tape advance, rewind, and playback operations.

7. Transport start-stop and speed selection from either system or manual control.

8. Load-point and end-of-tape sensors.

9. Tape speed tolerance ±2% at all speeds.

10. Dual record-playback heads. Head dimensions and tolerances compatible with IBM format.

DETAILED EQUIPMENT DESCRIPTION

Program Sequencer

Operations of the program sequencer (Fig. 4) are generated and controlled by seven circuits. These are (a) the trigger mode control, (b) the crystal oscillators and frequency dividers, (c) the time counter-register, (d) the sample-pulse distributor, (e) the program patchboard, (f) the subcommutation control gates, and (g) the supercommutation control gates.

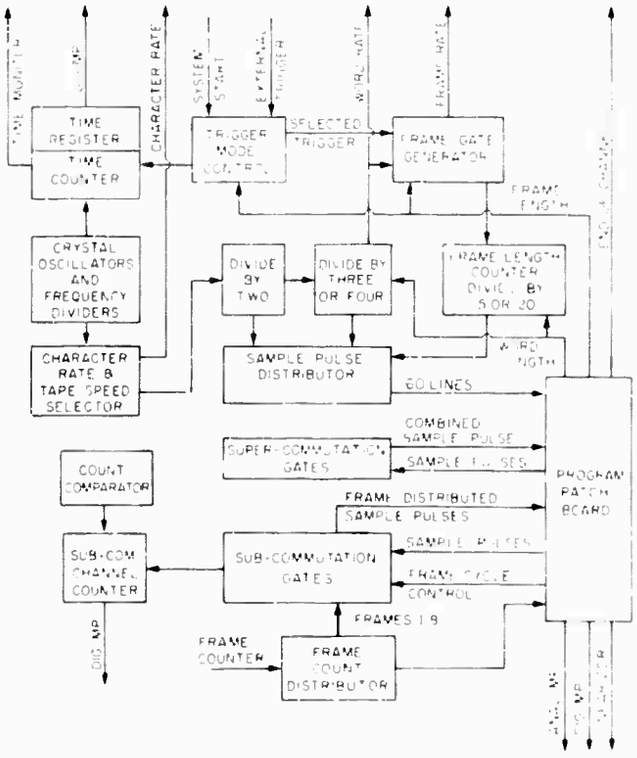

Fig. 4 - Program sequencer, which generates all timing pulses used in the system. Data sampling pulses are generated and distributed through a patchboard for sampling at either basic, subcommutated, or supercommutated rates in variable sequence. Relative time and subcommutated channel counters are included in the unit.

The trigger mode control can select one of four triggering options: (a) prf, (b) oscillator, (c) continuous, and (d) manual. After receipt of a system start signal from the format generator, the trigger mode control determines the basic recording cycle of the system. In the normal prf mode the system is triggered by the range-gate pulse of the radar, whose rate is virtually equal to the basic radar trigger rate. During system test operations the output from a variable-rate internal oscillator (oscillator mode) is used as a system trigger The frequency of this oscillator is adjustable from 10 to 1000 pps and is part of the trigger mode control circuit. The system may also be triggered in a continuous cycle mode, where a pulse occurring at the end of a frame is used to trigger the next frame. A manual triggering mode may be selected which will allow a single frame to be generated each time a pushbutton is actuated. This mode is designed primarily for test purposes.

The selected trigger is fed to a trigger countdown circuit, where any integral countdown of the source trigger rate may be selected to trigger the system. This mode of operation is used when the recording time for the desired number of channels within a frame exceeds the interval between trigger pulses. Although the trigger countdown is used chiefly when the system is being triggered from the range-gate pulse, it can also be used when triggering from the internal oscillator or in the continuous cycle mode.

The system clock and timing pulses are derived from separate, nonsynchronized, but highly stable 1-Mc/sec and 192-kc/sec crystal oscillators. Each oscillator is fed to frequency divider chains where precisely timed submultiples of these frequencies are obtained, for internal and external programming. Either a 10-kc/sec, 1-kc/sec, or 100-c/sec pulse train is used as a time rate input to the time counter-register. Either a 24-kc/sec character rate or any binary submultiple down to 750 c/sec may be selected as input to the sample-pulse distributor circuit. The system character rate pulses for use in other portions of the system are delayed one-half of a character time from that entering the sample pulse distributor.

The time counter may be started or stopped locally or by external signals, and counts in selected increments up to its 24-bit capacity. The counter may be reset and preset to any desired value locally. Upon the next selected time incrementing pulse (10 kc/sec, 1 kc/sec, or 100 c/sec) after receipt of the system trigger pulse from the trigger mode control, the contents of the time counter are transferred to a 24-stage register where the time count is stored until the next system trigger pulse. The time register output may be recorded at any time during the frame while the time counter continues to accumulate the selected pulse increments. The time counter output is also monitored by the system start-and-stop control circuitry in the format generator.

The sample pulse distributor circuit operates from the selected system trigger rate and character rate pulses. The character rate pulses are fed to a 2:1 countdown circuit followed by a divide-by-three or divide-by-four circuit. These are the sample-pulse generator and word-generator circuits, respectively. A frame is started by the frame gate generator with the first pulse from the word generator after receipt of a pulse from the trigger mode selector. The word rate pulses are then gated through to a frame length counter which divides by either 15 or 20 depending on whether the word generator divides the sample pulse rate by four or three. This is controlled by a word length connection from the patchboard. The outputs from all stages of the sample pulse rate generator, the word generator, and the frame length counter are combined into a decoding matrix in the sample pulse distribution to provide up to 60 sequential pulses on parallel lines within a frame. The duration of each of these pulses is equal to twice the interval between character rate pulses. The number of sample pulses in the frame can be preset to any multiple of three or four (six or eight characters) by designating a particular sample pulse as the end-of-frame pulse. At this time the frame gate generator and frame length counter are reset, and the outputs from the 60-line matrix are terminated until the next frame is started. When the frame is terminated and the frame gate

generator is reset, automatic zero words consisting of only parity marks are recorded under control of the format generator. These will consist of integral multiples of six or eight characters to fill in the time between the end of a frame and the start of the next frame.

If the trigger pulse from the trigger mode control occurs before the programmed frame is complete, the frame is terminated at the end of the current word cycle and the next frame will commence at the beginning of the next word. In this case there would be no zero words between frames. The programmed frame time should be kept shorter than the interval between trigger pulses so that over a block period the average trigger pulse interval will equal the frame time plus the average zero word time.

All of the 60 line outputs of the sample pulse distributor are routed to the patchboard. These pulses are brought to two different areas for selecting either analog multiplexer inputs or digital multiplexer inputs. The analog multiplexer sample pulses are advanced one sample pulse time ahead of the corresponding digital multiplexer sample pulses. This is to allow for the analog input processing delay in multiplexing, digitizing, bipolar offsetting, and linearizing. All of these operations are controlled by the analog multiplexer sample pulses. The digital multiplexer sample pulses are used to sample all internal or external digital data in two character groups. These sample pulses are also used for inserting channel marks at selected locations so that digital data may be grouped as either two, four, or six character channels by using one, two, or three successive sample pulses for the data and using the last sample pulse of the group for the channel mark.

The word rate and the frame length are also controlled from the patchboard. The word rate selection controls the word generator and the frame length counter and also inserts an automatic channel mark at the end of the word group. The sample pulse used for frame length must coincide with the end of a channel and a word group. The two remaining functions controlled from the patchboard are subcommutation and supercommutation and use either analog or digital sample pulses.

The subcommutation program distributes the sample pulses to selected analog or digital data over eight, sixteen, or thirty-two frames. Up to eight sample pulses in a frame may be allotted to the subcommutation program when using an eight-frame cycle. This number is reduced to four sample pulses in a 16-frame cycle and to two in a 32-frame cycle, so that in each case there are 64 possible sample pulse locations. Since each sample pulse spaces only two character times, two or three adjacent sample pulses must be used for sampling four or six character digital data in the subcommutation program. The number of sample pulses subcommutated remains the same in every frame regardless of the number of characters in the data source, to maintain the same number of characters and channels in each frame. Both analog and digital data may be multiplexed into the same primary channel locations through the program patchboard, with each data sample occurring in different frames. This has been done in tape channel 28 of the format (Fig. 2) where the subcommutated channel count is multiplexed with eight other analog data groups.

The subcommutation of the sample pulses is controlled by 64 AND gates arranged in an eight-by-eight group to allow access by eight sample pulse lines and eight frame lines. One input to each group of eight gates is enabled by the eight successive frame line outputs from the three low-order stages of the frame counter. Another input to each of the 64 gates is patch-connected to either an analog or digital sample pulse, of which up to eight may be used in an eight-frame program. Analog and digital sample pulses must be separately patched because of the two-character time-delay difference between correspondingly numbered sample pulses.

For a 16-frame subcommutation program, the output of the fourth stage of the frame counter is patched to the gates such that adjacent rows are enabled sequentially from frames one to eight and nine to sixteen, respectively. In this case the gates effectively assume a four-by-16 pattern, and only four basic sample pulses can be distributed. In the case of a 32-frame program the fifth stage output of the frame counter is also patched in to generate a two-by-32 sample pulse-frame pattern in which the 32 frames are arranged in four adjacent rows of eight frames each.

It is noted that in any of the three arrangements it is only necessary to connect a sample pulse line to the gates which are used to sample data at the multiplexers. Hence, any of the sample pulse locations within the subcommutation cycle can be omitted. All the sample pulse outputs from the activated gates are routed to the desired multiplexer positions and are also OR-gated together to advance a subcommutated channel counter. Before each recycle of the subcommutated sequence count is compared to a preset number as a check on the sampling of the desired number of channels. In the case of adjacent sample pulses being used to form a four-character or six-character channel, only one pulse is formed in the OR-gating process ahead of the counter. Hence, the counter recognizes channels only, and not individual sample pulses.

The supercommutation control circuit consists of four separate four-input OR gates for combining from one to four sample pulses on each line. Each of the four output lines may be used to sample either an analog or digital multiplexer position. Here analog and digital sample pulses must be confined to separate OR gates.

Analog Multiplexer

The analog multiplexer for which a block diagram is shown in Fig. 5 contains 64 input positions which may be sampled in the order and at the rates determined by the sequencer patchboard. The multiplexer is divided into four groups of 16 inputs each followed by a four-input secondary multiplexer. Each multiplexer position contains a matched pair of transistors driven by a gating transistor, through an isolation transformer, to present a high impedance during its off time and a low impedance during its on time. Each of the input signals must remain constant in amplitude during the first 50 μsec of the sample pulse-time, which, of course, varies with the selected character rate in the sequencer.

Any of the analog input positions may be used for unipolar signals in the range of 0 to +20 volts or bipolar signals in the ±10-volt range. However, there are only provisions for offsetting 24 bipolar signals from the patchboard. For internal check purposes all of the analog input lines may be switched to calibrated voltage levels from the reference supply which furnishes minimum, midscale, and maximum voltages for linearity checking in both unipolar and bipolar ranges. Also, the reference voltages may be connected continually to individual multiplexer input positions for long-term stability checking. Isolation between multiplexer positions may be checked by connecting maximum and minimum reference voltages to adjacent positions within a primary 16-input group.

The sample pulse lines from the patchboard are fed simultaneously to the selected primary multiplexer positions and to four 16-input OR gates. The outputs from these gates are delayed a fixed amount to allow for analog switch settling time in the primary multiplexer, after which the secondary multiplexer is gated. The output of this multiplexer is fed to a buffer amplifier to match the amplitude and impedance level of the voltage-varying pulse train to that of the A/D converter. The reference supply furnishes the operating voltages for the buffer amplifier. The pulse trains used to gate the secondary multiplexer are further OR-gated and delayed to initiate each conversion cycle in the A/D converter. The original OR-gated sample pulse train is also passed through a

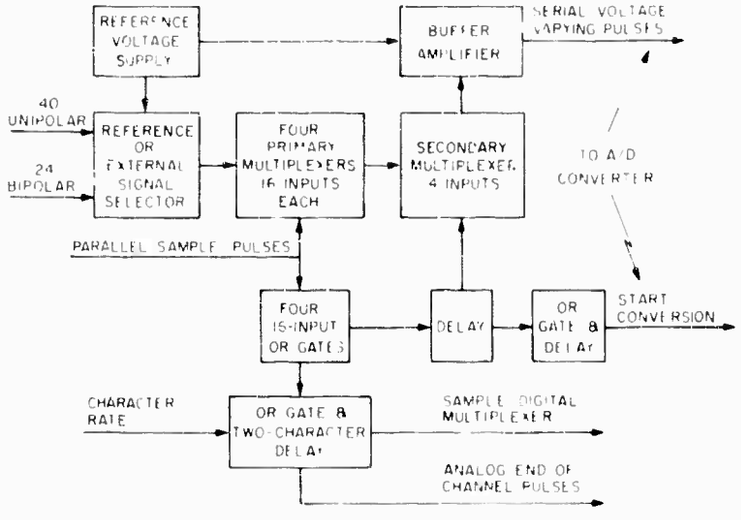

Fig. 5 - Analog multiplexer having 64 input positions which are sampled in a programmable sequence and converted to a serialized pulse train. Multiplexing is accomplished in two stages to maintain interchannel isolation.

delay equal to two character times to furnish synchronized sample pulses for the digitized analog data at the digital multiplexer. An end-of-channel pulse is also generated with every second character-rate input pulse, if an analog sample pulse is also present.

Analog-To-Digital Converter

The A/D converter, shown in a block diagram (Fig. 6), accepts the voltage-varying pulse train representing the multiplexed analog data. The output of the converter is a nine-bit parallel code equivalent to quantized voltage levels from -20 to +20 volts, although the actual input voltage has been reduced by the analog buffer amplifier to the range of the internal reference voltage (±8.4 volts) of the converter.

The converter operates on the principle of successive comparisons of the input signal voltage with internally generated precision voltage steps. The input signal is assumed to remain constant during the conversion period, which is about 33 μsec (11 bit-times at 3 μsec per bit). The conversion starts on an external command signal from the analog multiplexer and proceeds to digitize at a bit rate of 333 kc/sec obtained by a 3:1 countdown from the 1-Mc/sec crystal oscillator. This corresponds to a voltage digitizing rate of 30 kc/sec.

At the start of conversion the highest-order bit position is set in the register by the sequence counter. A half-scale voltage level is generated by the digital-to-analog (D/A) decoder. If the input signal exceeds the generated voltage, the register bit position remains set and the next lower register position is set by the sequence counter so that a three-fourths-scale voltage is then generated. A comparison is again made, and if the input signal is smaller, the second register position is reset, after which the third position is set in the register. At the end of nine of these conversion steps the digitizing is completed, and the end-of-conversion signal is generated, thereby initiating the offset and linearization process.

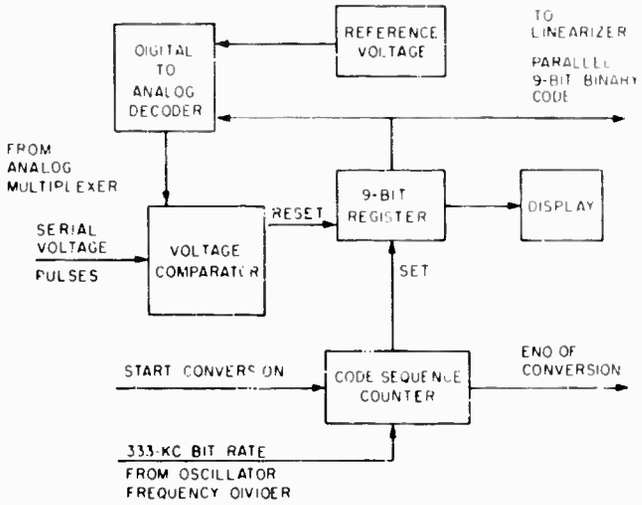

Fig. 6 Analog-to-digital converter which digitizes input voltage levels to form a nine-bit binary code by comparing the input signal to sequentially generated precise voltage levels. Conversion is accomplished in eleven steps or 33 μsec.

The coded outputs for unipolar signals will have a range of values between 256 and 511, whereas bipolar signals will have a range of values between 128 and 383.

Linearizer

The linearizer (Fig. 7) performs two distinct operations on selected analog inputs. One operation is to introduce a positive offset to bipolar input signals to shift them into the same code range as the unipolar signals. The other operation is to introduce small-scale positive or negative corrections to selected analog signals at discrete amplitude levels within four separate groups.

The output from the A/D converter is fed to the nine-bit linearizer input-counter. The end-of-conversion signal then gates in the bipolar offset bit, which has a weight of +128. Since the full range of bipolar signals in nine-bit code would have original values between 128 and 383, the insertion of a bit in the eighth stage of the counter causes the code range to fall between 256 and 511, corresponding to the unipolar signal range. There is capacity for offsetting up to 24 signals by patchboard connections of the desired analog sample pulses.

From this point on, the most significant bit in the input counter is ignored so that the effective code range is now 0 to +255. The four most significant bits of this code are gated to the segment selector by a delayed end-conversion signal to insure that the counter has assumed a steady state after offsetting. The segment selector decodes the four-bit input into sixteen equal zones.

The sixteen-segment lines are gated with four separate, function select lines which carry the serialized analog sample pulses as selected on the patchboard and combined into four 60-input OR gates. This gating selects one of 64 possible five-bit correction

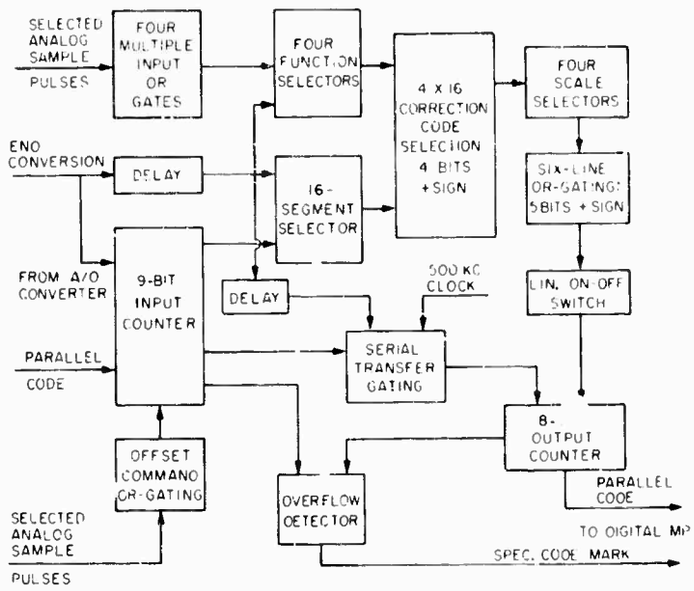

Fig. 7 - Linearizer, which converts bipolar codes from A/D converter to unipolar range and applies a four-bit correction to selected channels within sixteen segments from minimum to maximum code. Four correction patterns may be selected with either a fine or coarse scale. Overscale and underscale indication is provided.

codes at each selected sample pulse time. These correction codes are set up on a switch bank, as determined by calibration tests, and represent four bits plus sign within each of the 16 segments and four functions. Each of the four functions may be scaled, depending on whether a fine or a coarse correction to the data is desired. The fine-scale correction corresponds to ±15 in steps of one, whereas the coarse correction corresponds to ±30 in steps of two.

The outputs of the four scale selectors are OR-gated together and enter the eight-bit counter through the linearizer ON-OFF switch. Fine-scale corrections are entered into the four low-order bit-positions of the counter, and coarse corrections are entered into the second through the fifth low-order positions. Negative corrections are entered in eight bit complementary form, i.e., a correction of -12 sets the counter to 255 minus 12 or 243.

After the corrections are entered, the original code from the input counter is gated in sequentially to corresponding stages of the output counter. The sequencing allows the carries to proceed down the counter before the next bit is gated in. When subtracting, the carry from the highest-order bit-position is added into the low-order stage to obtain the correct result.

Values which exceed the limits of the output or input counter are detected by the counter overflow circuitry. In the output counter an overflow is detected by the presence of a carry from the last stage when adding, or the absence of a carry from the last stage, when subtracting. In the input counter the range of allowable values, after the code and the offset are added, is 256 to 511, which is equivalent to 0 to 255 when the ninth bit is

ignored. Thus, a carry beyond the ninth stage is a positive overflow, and the absence of the ninth bit in the original nine-bit code is a negative overflow condition.

Both the outputs from the overflow detector and the output counter are fed to the digital multiplexer. The total processing time for analog data through multiplexing, digitizing, offsetting, and linearizing is about 90 μsec, which is slightly longer than one sample pulse time or two character times at the highest character rate.

Digital Multiplexer

The digital multiplexer, shown in block form (Fig. 8), performs a parallel-to-serial conversion from the various internal and external data sources to form sequential characters of five parallel bits each. It consists of 36-sample pulse-input AND gates followed by ning 36-input OR gates, two five-bit parallel-character AND gates, and a five-bit output OR gate. Each of the sample pulse gates represents up to nine bits in parallel for the linearizer, manual, or external digital data inputs, or up to eight bits in parallel for the internal counters. The sampling time of each of these 36-input data-groups is determined by the patchboard program. These data groups are composed of the following: (a) 16 external digital inputs, nine bits each, (b) ten manual inputs, nine bits each, (c) one linearizer input, nine bits, (d) three relative time inputs, eight bits each, (e) two block number inputs, eight bits and four bits, (f) two frame number inputs, eight bits and two bits, (g) one channel number input, six bits, and (h) one subcommutated channel number input, six bits.

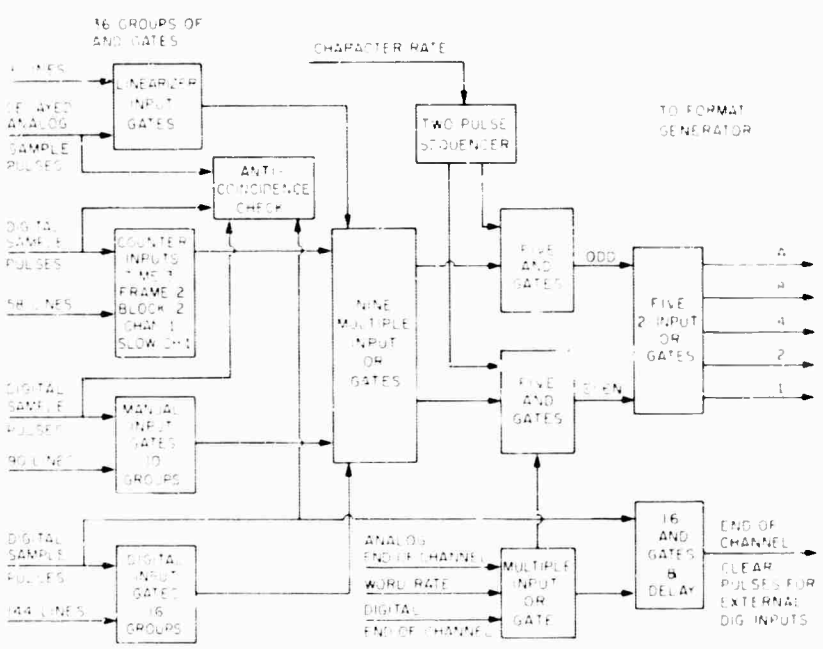

Fig. 8 - Digital multiplexer, which converts thirty-six parallel input data groups of up to nine bits each into serial five-bit data characters

The output from these 36 sample-pulse gates are combined into nine 36-input OR gates representing eight data bits and a special code mark when the latter is generated. The four high-order bits with the special mark feed five parallel AND gates, and the four low-order bits with the OR-gated end-of-channel marks feed five other AND gates in parallel. The end-of-channel marks are generated after each analog sample in the analog multiplexer, at the end of each word cycle in the sequencer, and at other selected sample pulse positions as determined from the patchboard.

The high-order positions are gated every odd character-time, and the low-order positions are gated every even character-time by the character-rate sequencing circuit. It is noted that these character-rate pulses occur one-half character-time after the leading edge and one-half character-time before the trailing edge of the sample pulse gates, respectively. The outputs from the two sets of AND gates are combined as odd and even characters in the five two-input OR gates at the multiplexer output.

It is noted that the linearizer sampling pulses are derived by the OR-gated analog multiplexer sample pulses delayed two character-times. This puts the combined analog sample pulses in phase with correspondingly numbered digital sample pulses. All of the sample pulses at the input of the digital multiplexer are also entered into an anticoincidence check circuit to insure that the same sample pulse is not used to sample more than one data group.

Any of the input data groups may be sampled at the frame rate, the supercommutated rate, or the subcommutated rate within the numerical limitation of the sample pulses generated at each rate in the sequencer. The time count and the subcommutated channel count are generated in the sequencer, whereas the block, frame, and channel counts are generated in the format generator. The relative positions of the character-rate pulses and the sample pulses insure that none of the counters are changing state at the time the two sets of five AND gates are interrogated.

The manual data are coded by nine banks of nine switches located internally and one bank of nine switches located externally. These data are usually multiplexed with the other slowly varying data and sampled at the subcommutated rate. The nine switches in each group correspond to eight data bits and a special code mark.

External digital data enter as 16 nine-bit groups composed of eight data bits and the special code mark which may signify negative quantities, nonbinary codes, or changing data value during the sample time. The precise meaning of each of these marks, of course, depends on how it is generated by each of the external equipments. After each external digital group is sampled, a clearing pulse is generated by AND-gating the separate sample pulses with the output of the end-of-channel mark OR gate and delaying the resultant pulse. Any of the direct digital inputs may be sampled as two, four, or six character channels by patch connection of adjacent sample pulses and using the last sample pulse in the group also to generate a channel mark. The sampling rate for each input may be at any of the three rates generated in the sequencer.

Format Generator

The format generator shown in Fig. 9 receives timing signals from the sequencer and data outputs from the digital multiplexer to generate the input and control signals for the tape recorder. Most of the circuitry in this part of the system functions during both record and playback modes. The format generator consists of three seven-bit buffer registers, various tape-mark generating and detecting circuits, the record/playback buffer control, and the system start-stop control.

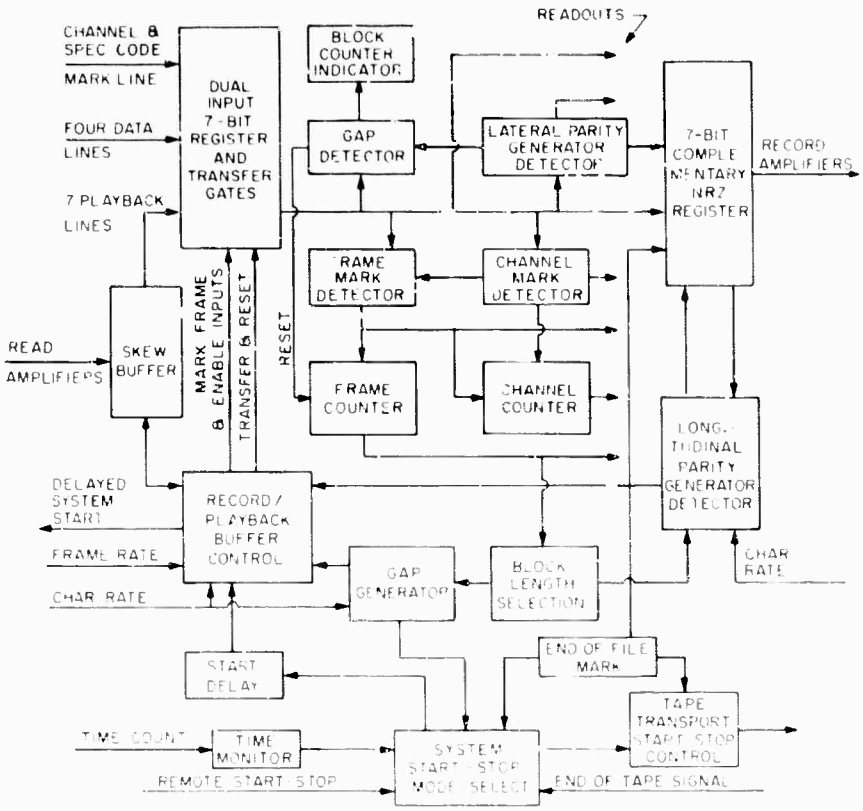

Fig. 9 - Format generator, which controls flow of data and timing pulses to and from tape transport. Various tape marks and gaps are generated and detected during record and playback modes. Counters are provided for the various format subdivisions.

The data registers consist of a dual-input seven-bit register followed by transfer gates and a seven-bit complementary register to convert pulse data to NRZ format to drive the record amplifiers. Five of the inputs to the input register are fed directly from the data line and channel-mark line outputs of the digital multiplexer. Another input is a start-of-frame mark and an end-of-frame mark, generated in the record/playback control circuit from the leading and trailing edges of the frame-gate, which is received from the sequencer. The seventh register position is not used during record modes. Each register position has another set of seven input gates which are fed from a skew buffer during playback modes.

The record input-gates are inhibited by the record/playback buffer control except during the frame scan, as determined by the sequencer. The register output transfer-gates are also inhibited at this time and during tape-gap intervals. While both inhibits are removed, the data passes through the register along with the channel and frame marks. These six outputs are examined by the lateral parity generator, and a seventh bit is generated if there is an even number of ones in the other six outputs. No parity bit is generated if there is an odd number of ones in the other six positions. The parity bit is generated during the storage time in the register between input gating and transfer gating by a network of exclusive OR gates. This time is controlled in the record/playback control circuit by delaying the input character-rate signal from the sequencer and is equal to about 12 μsec.

When only the register input gates are inhibited, the parity generator will always generate a one-bit, since no data will enter the register. This corresponds to the automatic zero period of the recording intervals which exist between the frame scan periods and at the start of each block of data. When the output transfer-gates are also inhibited, both the register and the parity-generator data-flow are blocked. This corresponds to gap periods of the recording intervals which exist between blocks.

The transfer-gate interrogation pulses, which occur near the end of each character-rate time, transfer the register and parity generator outputs to the seven-stage complementary register. One-bits reverse the state of the respective register positions, but zero-bits leave the register states unchanged. At the end of each interrogation pulse a reset pulse is generated for the six register stages and the parity generator. This occurs prior to the start of the next character time. The complementary register output drives the tape record amplifiers.

The outputs from the transfer gates are continually monitored by channel, frame, and block-detecting circuits. These circuits operate in the same manner during both record and playback. The outputs of these circuits drive the channel, frame, and block counters, respectively.

The channel-mark detector monitors the fifth or A-track register-output which contains both special code marks at the start of some channels and end-of-channel marks at the end of all channels. The detector separates these marker pulses by dividing the transfer-gate interrogation pulses into odd and even character times and gating them with the channel-track output pulses. Two outputs are then generated as special code marks and end-of-channel marks which are used in the selected data readout portion of the system. The end-of-channel pulses are used to advance the six-stage channel counter. The output of this counter is fed to the digital multiplexer and the selected data readout.

The frame mark detector monitors the sixth or B-track output, which contains a pulse at the start and end of each frame. The frame-track output is gated with the end-of-channel mark detector output to separate start-of-frame marks and end-of-frame marks. Both detected frame marks are used in the selected readout unit, and the end-of-frame marks are also used to advance the frame counter and reset the channel counter. The frame counter consists of ten stages, and its output is available for sampling at the digital multiplexer and is also used in the selected data readout unit. The five low-order stages of the frame counter are used in the subcommutation control portion of the sequencer for the slow-data sampling program.

The gap detector OR-gates the outputs of all six lines from the register and the parity generator line. After each end-of-frame signal is detected, the output of the OR gate is interrogated. Absence of an output pulse signifies a gap, whereas the presence of a pulse signifies only an intermediate frame within the block. This circuit is reset with the next detected start-of-frame pulse and operates the same during both record and playback. The gap detector output triggers a 12-stage block counter and resets the frame counter. There is a continuous display of the block-counter output, and it is also fed to the digital multiplexer unit.

The duration of each block may be set to any multiple of 16 frames up to 512, the maximum capacity of the frame counter, by the block-length selection-circuit. When the state of the frame counter is coincident with the selected block-length code, the longitudinal parity-generator circuit counts four character rate pulses while the register transfer gates are inhibited through the record/playback control. At the fourth character time the complementary NRZ register is reset to form the longitudinal parity mark.

The end-of-block signal also allows the gap generator to start counting character-rate pulses and inhibits the register transfer-gates through the record/playback control. This gap period lasts for 154 character times, equivalent to 3/4 in. on the tape after the longitudinal parity mark. At a character count of 64 during the gap generator-time, a system stop-command is generated for the start-stop mode selector circuit. This count-delay allows for the tape distance traveled in stopping and starting the tape recorder within the 90 remaining character-times during the gap period.

The system start-stop mode control circuit allows selection of four recording modes. These are the local start and stop pushbuttons, the time monitor circuit, calibrate control, and remote start-stop commands. In the first mode the recording time lasts for integral block intervals between the time that the start and stop switches are closed. In the time monitor mode, preselected times to start and stop the recording are made. The start and stop selection gates then generate output pulses when the relative time counter in the sequencer reaches the preselected times. In the calibrate mode, single blocks are recorded each time the manual start switch is closed. The system stops automatically after each block. In the remote record mode, the recording interval is controlled by externally generated signals.

The timing of a typical recording cycle is shown in Fig. 10. The receipt of a system start signal starts the tape transport, provided an end-of-tape condition is not sensed from the tape recorder. After a variable delay time, depending on the selected tape speed, to allow the recorder to assume uniform speed, the inhibit is removed from the system frame trigger control circuit in the sequencer. This inhibit line is fed through the record/playback control. If a trigger pulse had not been received during the last word time, the recording will commence with automatic zero. This will continue until the trigger pulse is received, and the trigger pulse will then generate a frame-rate signal in the sequencer. The receipt of the frame-rate signal by the record/playback control will then remove the inhibit from the register input gates (and terminate the automatic zero period). The frame-rate pulse starts with the next complete word cycle after the trigger pulse. It is noted that the character-rate and the word-rate generator in the sequencer unit operate continually in all recording modes, independent of frame and channel gating time. However, the inhibit signal will be removed from the register gates prior to the receipt of any input data from the digital multiplexer at the start of each frame, due to system character-rate delay-time.

The system stop recording sequence requires a stop command signal from the gap generator and a stop-enable signal from the selected start-stop control source. It is noted that all recordings are made in complete block units, so that all generated stop signals do not take effect until after the block gap time has commenced. The stop signal is generated when the gap generator reaches a count of 64 or when about one-half of the gap time has elapsed. This allows for the tape transport stop and start distance within the gap period. If a start command is received before the stop command is executed after the end of the block, the transport will not stop during the gap, since the transport start-stop control circuit stores only the last signal generated by the start-stop mode selector.

The end-of-file mark is recorded after the last desired block of data has been generated. This signal is generated manually after the system has stopped, and it consists of a single character of ones in the four data-bit positions followed by a longitudinal parity character after a 3-1/2-in. gap from the last block. The register input and output gates are inhibited during this time through the record buffer control circuit, just as in other tape-gap periods. The transport control is turned on ahead for sufficient time to generate the 3-1/2-in. gap before the mark is entered in the NRZ register for recording.

On playback, the read amplifiers in the tape recorder convert the tape saturation level changes to pulse voltages representing one-bits in each of the seven tracks. The

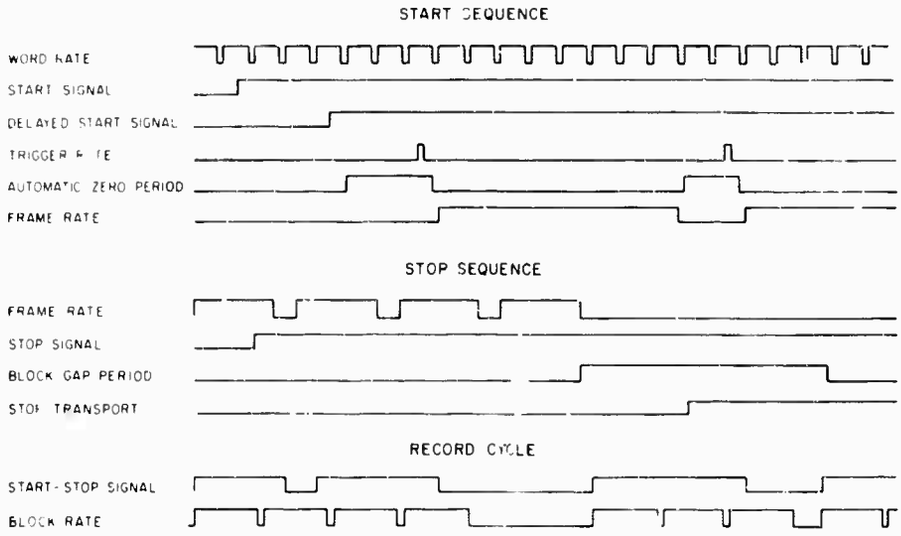

Fig. 10 - Timing diagram showing the relationship of the trigger pulse and the start and stop signals to the generated frame and block rate

pulse voltages from each track are read into the skew-buffer which holds the pulses for a fixed length of time after the initial pulse within a character-time is received. A playback clock-rate is generated by combining the outputs from all seven lines in an OR gate and generating a delay from the trailing edge of the OR gate output in the playback buffer control.

The skew buffer's seven outputs enter the output register continually through one set of the dual input gates when the system is in the playback mode. The record input gates are continually inhibited in the playback mode by the buffer control circuit. The generated playback clock reads the data out of the register through the output transfer gates and simultaneously resets the skew buffer prior to arrival of the next character from the read amplifiers.

When in the playback mode, the lateral parity generator generates a parity bit in the same manner as in the record mode, through a set of cascaded exclusive OR gates. The generated bit is then compared with the recorded bit each character-time. An output line is pulsed whenever the generated and recorded parity bits are different. This line feeds the selected data readout unit. The channel, frame, and block detectors and their counters function the same during playback as in record modes. The gap generator operation is also the same. That is, the gap generator starts counting character-rate pulses at the end of the selected block length and when the gap period has been detected. However, the gap generator is not used to control the inhibit on the register, as in recording, but is merely used to control the tape transport stop-command time. The seven-bit complementary register acts as a one's counter for each bit on the playback, to regenerate the longitudinal parity character after the block. The playback parity mark is compared with the recorded mark for error detection.

Selected Data Search and Readout

The data search and readout unit block diagram is shown in Fig. 11. This unit monitors and displays selected portions of the data from the format generator during both

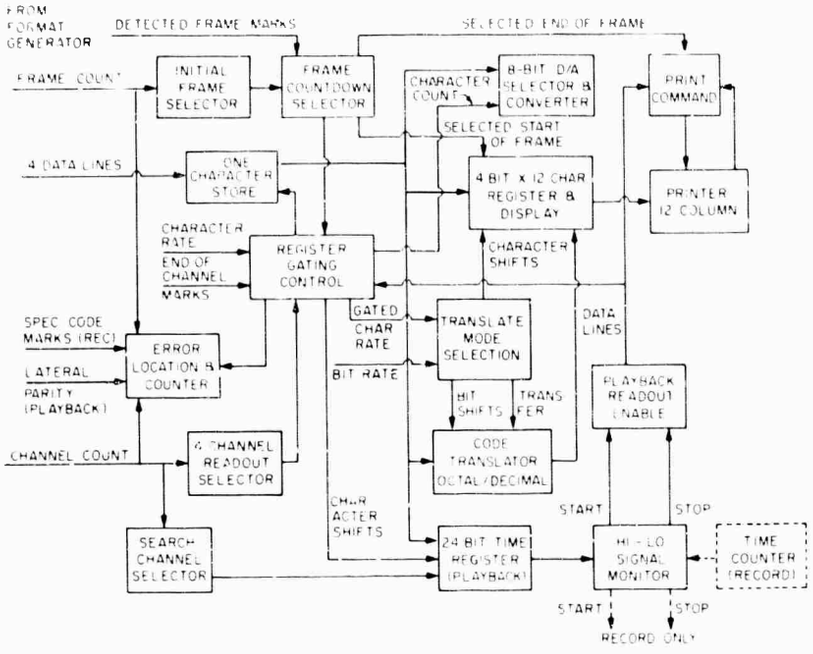

Fig. 11 - Data search and selective readout, which provides visual display and printout of up to four selected channels during record and playback. One channel may be selected for digital-to-analog conversion. Overscale or parity error indications are provided. A signal monitor can control record and playback periods.

record and playback modes. Up to four channels or 12 four-bit characters may be selected at reduced frame rates for panel display and tabular printing. The frame-rate selection is limited by the line speed of the printer. One of the selected channels may be converted to an analog voltage in an eight-bit D/A converter. There is also an error display and counter which monitors special code marks during record and lateral parity errors during playback. While in the playback mode the data readout and error display may be limited to regions where the data value in a selected channel lies between preset limits. The other feature of the readout unit is a code translator which converts input codes of up to 16 bits to four-bit code characters acceptable to the printer. Straight binary is converted to BCD, and other codes are converted to octal groups.

Channel selection is made by four banks of six switches each. The desired channel numbers are set in these switch banks. When the channel count reaches the set values, an enabling pulse is sent to the register gating control circuit. This circuit then starts counting character-rate pulses between end-of-channel mark inputs. The number of characters counted could be either two, four, or six for each channel selected. The outputs of the register gating circuit are delayed character-rate pulses and character counts, within each channel, to control the eventual gating of data into the various registers in the unit.

The gating of control pulses to the code translator and the 12-character (48-bit) register are limited by frame countdown selection, whereas the control pulses to the D/A register and the time register are gated through at the system frame rate. The frame selection is controlled on a cyclical basis by an initial frame selector and a frame countdown circuit. The preset initial frame code is compared with the contents of the

frame counter, and when the selected frame is reached, a pulse enters the countdown circuit which generates an output at a selected binary submultiple of the input rate. The duration of the frame countdown output pulse enables a portion of the register control circuit for one frame, since the pulse duration is controlled by the detected frame marks. Of course this selected frame gating applies only to the code translator and the 48-bit register which controls the data rate to the printer. If the initial frame selected were No. 18, and the frame countdown was selected as 32, the data frames displayed and printed would be Nos. 18, 50, 82, 114, etc., to the maximum number of frames within the block.

The four data lines from the format generator-register transfer gates are fed to a one-character storage register in the selected readout unit. The output of this one-character register is available to the D/A register, the 48-bit register, the code translator, and the relative time register (during playback only). The data are read into these registers at times determined by the register gate control circuit, after which the one-character storage register is reset, before the arrival of the next character.

The gating of the data into the 48-bit register and code translator is additionally controlled by the translate selector circuit. Data may be read into the 48-bit register in three ways for each of the four selected channels, depending on the code for the respective channels, and whether or not the data is to be printed. These three ways are direct loading, decimal grouping, and octal grouping.

In the direct loading mode each four-bit character enters the 48-bit register in its original form. The register is shifted one character position for each character in the selected channel. Since there are 12 character positions in the register, any combination of two, four, or six character channels up to four may be read out provided the total number of characters does not exceed 12. In this mode the code translator is not used, and data may be printed only if the code in each four-bit group does not exceed the 8-4-2-1 BCD equivalent of nine.

In the decimal mode of data grouping, straight binary codes of up to 16 bits may be translated to BCD code. Eight-bit channels (two characters) are translated to ten-bit BCD (three characters), and 16-bit channels (four characters) are translated to 19-bit BCD (five characters). Only the 16 most significant bits in 24-bit (six-character) channels are gated into the translator. This is accomplished by inhibiting shift pulses to the translator when the character count in the register gate control circuit reaches four. Four shift pulses are generated for the translator for each character in the channel selected for translation. Each bit from the one-character store is shifted in at a 192-kc/sec clock rate, so that the translation time is 48 kc/sec per character, allowing each character to be translated before arrival of the next character at the highest character rate.

After each shift pulse each four-bit character group is decoded, and where the code is five or more, a three is added prior to the next shift pulse. This is equivalent to adding a six whenever a carry is generated for the next character and compensates for the difference between the carry weights of 16 and 10 in binary and BCD codes, respectively.

While the code translation takes place, the data in the 48-bit register must be shifted down either three or five character-positions depending on whether a two-character or a four-character channel is being translated. The translated code is then parallel-transferred to the first three or five character positions in the 48-bit register.

In the octal mode the data is also fed to the translator for regrouping of the data bits before transfer to the 48-bit register. This mode is used when the original data code is not straight binary or 8-4-2-1 BCD and it is desired to print out the data. As the data are shifted through the translator register, every fourth bit-position is bypassed so that

all bit weights corresponding to eight in each BCD decade are left vacant. The character shifts generated in the translator selector circuit for the 48-bit register are the same for both decimal and octal translations, i.e., three character shifts are generated for two character inputs to the translator and five character shifts are generated for four character inputs to the translator.

The 48-bit register is reset with a selected start-of-frame pulse from the frame countdown selector, and the print command is generated for the line printer at the end of the selected frame, provided the previous print cycle has been completed.

For the D/A converter, the first of the four selected channels is gated in from the one-character storage register. Any two consecutive characters from two, four, or six character channels may be selected to enter the D/A converter eight-bit register. The code in the selected channel must be in straight binary code in order to produce a proportional output from the converter.

The channel and frame numbers are displayed for all channels, where special code marks have been generated either externally or internally. A count of the number of special code marks generated is also displayed. This gives the operator a check on the validity of the data being recorded. These displays may be set to indicate only the special code marks generated either in the channels and frames selected for printout or in all channels and frames.

All the above operations function during both record and playback, except that lateral parity errors rather than special code marks are displayed and counted on playback. Additionally, during playback a data search function is provided which controls the data readout to the code translator, 48-bit register, D/A converter, and the lateral parity error display. This is the case only if the playback search mode is selected, whereas in the regular playback mode, data readouts are continuous between start and stop of the tape transport.

The selection of a search channel number allows data to be gated to the time register in the sequencer unit from the one-character store. Shift pulses are supplied to the register from the gate control circuit after each character is read in. These shift pulses are continually supplied between all end-of-channel marks, but only those that occur during the selected search channel time have any effect.

Selected data limit values are preset in the high-low signal comparator which monitors the data in the time register. One limit is used to control the start of data readout by enabling the register gate control circuit and the print command circuit. The other preset data limit is used to stop data readout by inhibiting these circuits. Any two, four, or six character channel may be used for the search channel, and provisions are included for adjusting the resolution of the value comparison check. During record the value comparator is used to monitor the time counter to generate system start and stop commands for the format generator when the time monitor mode has been selected.

Magnetic Tape Recorder-Reproducer

The tape recorder-reproducer (Fig. 12) contains the magnetic tape transport, the recording and playback amplifiers, and the drive and control circuits for the transport.

The tape transport unit used with this system is a Potter Model 906II. It is provided with six operating speeds from 3-3/4 ips to 120 ips under both automatic or manual control. The automatic control signals are generated in the format generator and consist of a start-stop signal and a record/playback signal. The automatic speed selection is ganged with the character-rate selector switch in the sequencer. All recording operations

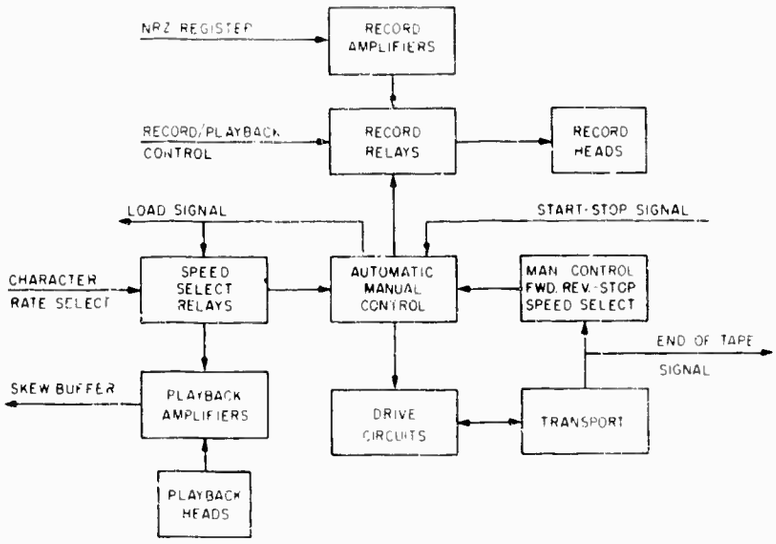

Fig. 12 - Tape transport, which operates at six speeds synchronized to system character rate. Tape recording and playback are always under system control while tape shuttling back and forth is always under manual control.

take place in the automatic mode. In the manual or local control mode the record heads are disconnected from the record amplifiers. This mode is used for advancing and rewinding the tape at high speed, independent of the automatic system speed selection. Also, the tape unit should be in the manual mode if it is desired to operate the rest of the data recording system without recording or playing back a tape.

The recording is made on seven-track, 1/2-in.-wide tape at a constant density of 200 characters/in. at all six operating speeds. The data lines to the record amplifiers are fed from the NRZ register in the format generator. The record amplifier outputs drive the record heads to positive or negative saturation level, which effectively writes over any previously recorded data. To prevent accidental erasure of a tape the record heads are disconnected through relays when in manual or playback modes of operation.

The transport is equipped with a dual head assembly with a gap separating the record and playback heads. The heads are designed for medium-density (200 characters/in.) record and playback at all six operating speeds. The playback head output drives the playback amplifiers, which are of the peak detecting type. The gain and time constant of the playback amplifiers must be increased at lower tape speeds, which is accomplished by a change of components through the speed selection relays. The playback amplifier output pulses feed the skew buffer circuit in the format generator.

The tape transport drive circuitry includes the reel-drive servo amplifiers and the capstan pinch-roller actuators. The output of the servo amplifiers are regulated by the tape tension arm positions on the transport which, in effect, control the speed of the upper and lower reel drive motors. The pinch-roller actuators are controlled from the start-stop signal. A forward start signal actuates the lower capstan pinch-roller, and the reverse start signal actuates the upper capstan pinch-roller. The start and stop time is less than 3 msec, although this is somewhat dependent on tape speed.

The capstans are driven by dual-speed hysteresis synchronous motors which maintain the tape speed regulation within ±2% at all speeds. The three pairs of tape speeds are obtained by a system of clutches and pulleys which couple the motors to the capstans. Isolation between the capstan pinch-rollers and the upper and lower reel drives is maintained by a vacuum buffer and three loops of slack tape on the tension arms. This insures smooth travel of the tape over the heads and reduces the inertia in the start-stop drive mechanism.

The transport assembly is also equipped with photoelectric end-of-tape sensors. These circuits detect the reflective markers that are positioned near the beginning and the end of a reel of tape. These are recognized as the load-point and end-of-tape markers, respectively. A stop signal is generated by the load-point marker when the tape is moving in the reverse direction and by the end-of-tape marker when the tape is moving in the forward direction. It is noted that, when operating in the automatic mode, the end-of-tape signal will not take effect until the end of a block, as determined in the format generator. This fact should be observed when generating long blocks of data, to prevent the tape from winding off the end of the reel.

A load switch is included with the automatic/manual control transfer circuit in order to advance the tape a fixed distance so that the load-point marker is positioned beyond the record head. This circuit compensates for the distance between the tape reflective mark sensor and the record head, which is about 4-1/4 in. The 120 ips speed is actuated when the load switch is closed, irrespective of the selected automatic or manual speed, so that a stop command is automatically generated a fixed time afterwards.

Operating Modes

For operating convenience most of the controls and status indicators associated with the sequencer, format generator, and portions of the data search and selected readout units have been assembled on a main-system control panel.

For most operations of a predictable duration the system is operated in the continuous-block recording mode. The intermittent-block recording modes are used for calibration purposes and tests of long duration in which the recording interval is determined by the automatic time monitor or a remote control unit. Intermittent modes are normally used, because excessive amounts of magnetic tape would generally be required in continuous-block recordings. Generally, the same format can be used in all three recording modes, although the data blocks should be confined to separate files. For each of these recording modes the number of frames within each block of the file should be the same. Also, within each frame, there should be the same number of characters and channels.

Special code marks and operating defects, such as short frames and data-track dropouts, can be detected by monitor lights on the system control panel during the recording modes. These defects can also be checked by playing back the recorded tape. Short frames can be detected by monitoring the recorded channel count, which should be the same in each frame. Track dropouts would be detected as parity errors in all channels in which data should have been recorded in the missing tracks, and also by the playback monitor lights for each track. The special code marks generated can only be detected during recording.

The format of Fig. 2 specifies the recording of radar video voltage amplitudes for two frequencies (vhf and uhf) and two polarizations (horizontal and vertical). These items are recorded in character numbers 25 through 32, inclusive. One range gate is used, that is, the data are sampled at one range interval only, as indicated in character numbers 19 through 24 inclusive. If multiple range gates were used, the resulting

additional echo-amplitude voltages could be recorded in any tape channel designated for analog data which are sampled but not active (N.S.). The remaining items that are being recorded are generally self-explanatory and are indicated on Fig. 2. When major changes in format are required, a patchboard panel is wired for each program. These prewired panels are then readily interchangeable in the system to generate magnetic tape files in a variety of formats.

SUMMARY AND CONCLUSIONS

The digital data recording system has proved to be a most versatile device. It not only accepts radar data and radar control signals to generate a magnetic tape in a form suitable for computer entry, but also is capable of (a) self-checking, (b) preoperational checkout of the radar, (c) continuous monitoring of the radar performance in real time, and (d) playback and selective readout of the recorded data.

These and other significant features of this system are applicable to any radar system. Most of the features have been incorporated into standard operations which have been used repeatedly in conjunction with the Randle Cliff Radar facility and various data-reduction programs. For example, by referring to the format (Fig. 2) each data channel, whether internal or external, can be verified prior to any operation. Each data channel may be selected for visual and printed display. If the value obtained for any selected data channel is not correct or is abnormal, then that data source can be investigated. As another example, a continuous real-time monitoring of all channels for out-of-limit values is displayed on a group of panel lights and identified by channel and frame number. As a further example, the radar pulse repetition frequency is also continuously monitored to detect a rate too high for the programmed frame length and tape speed. The exact prf can be measured by reading the elapsed time between selected frames on the printer.

The principal characteristics of the system are summarized below.

Input Data Capacity

Analog — 64 external bipolar and unipolar voltage positions or internal calibration voltage levels are multiplexed, digitized, and linearized with eight-bit-plus-sign resolution.

Digital — 144 external parallel input bit positions plus 136 bits of internally generated timing and reference data are multiplexed in either 8, 16, or 24 bit data groups plus a marker bit for each group.

Programmable Formats

Formats are readily interchangeable through prewired patchboards to permit data sampling in variable sequences with offset and linearizing functions selectable for analog data. Three data-sampling intervals may be selected for each analog or digital data group as follows.

Basic Scan — Up to 60 data groups.

Subcommutation Scan — Up to 64 data groups.

Supercommutation Scan — Up to four data groups

Variable Data Scanning Rates

The scanning rates are synchronized to the radar and are generated without the need for internal data storage.

Basic Scan Rate — Scan rates are continuously variable up to 200 full-length scans per second. Higher rates are allowable for programmed scans of fewer data groups. Automatic zeros are generated between the end of a data scan and the start of the next scan to maintain a continuous character rate within a data block.

Subcommutation Scan Rate — This may be set to either 1/8, 1/16, or 1/32 of the basic scanning rate.

Supercommutation Scan Rate — This may be set to 2, 3, or 4 times the basic scanning rate.

Block Length — The data block length is variable in multiples of 16 basic scans to be compatible with small-scale computers with limited memory capacity. Maximum block length is 512 data scans, with interblock gaps generated automatically.

Mode Flexibility

Flexibility of operating modes is obtainable through a 32:1 range of tape speeds. Tapes recorded at high speed may be played back at slower speeds for detailed verification and editing.

Record Modes — Continuous in single or multiple blocks under local, time monitor, or remote control.

Playback Modes — Continuous readout of all data or intermittent readout through automatic editing of a selected data group.

Data and System Performance Monitor

The data and system performance are monitored during real time or post recording.

Data Grouping — Up to four selected data groups may be read out on a digital printer at controlled intervals during record or playback. One data group may be converted to an analog voltage with variable resolution by bit selection to drive an external analog display or recorder.

Visual Lamp Displays - These displays are provided to indicate the status of input data and the internal operation of the data recording system as follows: (a) register indicators for comparison with printer data, (b) relative time and block number, (c) overscale indication for input data during record and parity error indication on playback are isolated by data group and scan number, (d) indication of digital multiplexer sampling, (e) record/playback amplifier outputs, (f) location of programming errors, and (g) overfrequency of input trigger rate for programmed scan.

Input/Output Compatibility

Compatibility with both input and output data and control devices is attained with little or no modification or interfacing.

Digital Encoders – Parallel outputs of digital encoding units are accepted directly. Serial encoder data requires only an external eight-bit storage buffer, regardless of the number of bits in the external digital word.

Ungated Radar Video – The ungated radar video may be sampled directly by programming the analog multiplexer gates to cover the desired range extent. This procedure eliminates the need for external analog storage units.

Control and Timing – Reference signals are available for synchronizing analog tape and chart recordings. Analog tape data may then be played back through the DDR system for generating the computer compatible tape, thus eliminating the need for special-purpose analog data processing equipment.

Remote Control – Use of remote control inputs for timing the data recording intervals allows long-term unattended automatic operation for recording intermittent data.

Remote Readout – Direct connections are available for driving remote slow speed digital readout units in parallel and in synchronism with the internal digital printer.

Long-Term Recording – Long-term continuous recording can be made possible through the addition of a second tape recorder to operate alternately with the existing recorder. This modification also allows direct readout of all data to a remote computer facility for real time data processing operations.

The wide range of operating characteristics and applications of the digital data recording system insures current and future utility even as the total radar system and its programs are expanded. It can be seen that the system is sufficiently flexible so that its usefulness depends, in large measure, on the skill and experience of the users.

DOCUMENT CONTROL DATA - R & D

Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified

1 ORIGINATING ACTIVITY (Corporate author)

Naval Research Laboratory
Washington, D.C. 20390

2a. REPORT SECURITY CLASSIFICATION

Unclassified

2b. GROUP

3 REPORT TITLE

A DIGITAL MAGNETIC TAPE SYSTEM FOR RECORDING RADAR DATA

4 DESCRIPTIVE NOTES (Type of report and inclusive dates)

An interim report; work on the project continues.

5 AUTHOR(S) (First name, middle initial, last name)

P. L. Watkins, J. M. Goodman, and A. M. Knopp

6 REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
July 24, 1967	38	1

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
NRL Problem R02-05 b. PROJECT NO Project ONR RF 001-02-41-4001 c. ARPA Order 32-60, Amendment 7 d	NRL Report 6584 9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

10 DISTRIBUTION STATEMENT

Distribution of this document is unlimited.

11 SUPPLEMENTARY NOTES	12 SPONSORING MILITARY ACTIVITY
	Department of the Navy (Office of Naval Research), Washington, D.C. 20360 and Advanced Research Projects Agency

13 ABSTRACT

A versatile multichannel medium-speed data system for recording radar data on magnetic tape directly in digital-computer format was designed for use with the Randle Cliff Radar facility at the Naval Research Laboratory's Chesapeake Bay Division, and it is currently installed and operating there.

Input data to the system can be analog voltages, which are internally digitized, or digital codes. Timing and reference data are internally generated. The system operates with three simultaneous data scanning rates: (a) basic (radar pulse repetition frequency), (b) submultiple, and (c) a multiple of the basic. Both the sequence and the amount of data sampled at each rate is patchboard-controlled.

Any basic scan rate from 6 pulses per second to 3 kilo-pulses per second can be generated, depending on the volume of data. Data are recorded as sequential seven-bit characters at constant density, without intermediate storage, over the full range of trigger rates, through the choice of six tape speeds.

Selected portions of the data can be monitored by an on-line printer and lamp display, during recording. Further checks can be made during playback of recorded tapes.

(over)

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Data system						
Digital sequencer						
A/D conversion						
Linearizer						
Format generation						
Data and search readout						
Recorder-reproducer						
Variable data canning rate						
Variable format recording						
Analog/digital multiplexing						

The system has developed into an unusually successful preoperational monitoring device for itself and for nearly the complete radar system, in addition to being a versatile and dependable recording system.