ELEVENTH INTERIM REPORT

R & D OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS

Covering the period

1 January to 31 March 1967

Prepared for

MIT, Lincoln Laboratory
P.O. Box 73
Lexington, Massachusetts 02173

Subcontract No. 295

Prime Contract No. AF 19(628)-5167

PHILCO-FORD CORPORATION
Microelectronics Division
Blue Bell, Pennsylvania • 19422

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Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

SECTION I - INTRODUCTION

1.1 SCOPE OF REPORT

This report describes the work performed during the third quarter of the research and development program, "R & D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems." The program is an extension of MIT Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(628)-5167). Preliminary work for this program was performed during the final months of the previous program, "R & D Program to Design and Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Time of 1 Nsec," which ended June 30, 1966.

1.2 PROGRAM OBJECTIVES

The principal objective of this program is the fabrication of ultrahigh-speed microcircuit arrays to establish the technological requirements for achieving very high-speed computer systems through the incorporation of increasing amounts of high-speed logic circuitry on a single monolithic silicon chip.

A second objective is to continue development of design principles and fabrication techniques for improving switching speeds of microcircuits, using simple circuit designs as test vehicles. Microcircuits of both unsaturating and saturating

types will be developed, with particular emphasis placed on optimizing the switching speed-power dissipation relationship.

1.3 AREA OF INVESTIGATION

The major task of this program is the investigation of the technological problems involved in designing, fabricating and testing various forms of small geometry, high speed complex bipolar arrays. The main benefit to be derived immediately from the array approach is performance; lower cost per logic function and improved reliability are additional benefits to be derived when the technology has sufficiently matured.

Higher speed system performance will be obtained through utilization of arrays by virtue of the reduced number of packages and interconnections which naturally result from incorporating more electronic functions into each silicon chip.

Increasing component chip densities, however, require multilevel metalization schemes. In this program we are employing aluminum and vapor deposited SiO_2 as our multilevel component materials. Two and three levels of metalization are being employed.

The first vehicles chosen for the array investigation were 3-, 9-, and 27-bit parity generators. The parity circuit arrays contain 58, 232, and 754 components, respectively, and require two (3 bits) or three (9 and 27 bits) levels of metalization. The logic form of the parity arrays is ECL.

The design phase for all three parity arrays was completed during the first quarter. Fabrication and evaluation began in the first quarter and will continue on through the fourth quarter.

The most fundamental array problem from the standpoint of fabrication is yield - yield at the microcircuit cell level and yield at the multilevel metalization level. One silicon defect or one insulation defect is sufficient to ruin an entire array. The yield problem is even more acute in high frequency arrays because of the added constraints of small geometries and shallow diffusion.

Evaluation and analysis of arrays, especially small geometry arrays, are other formidable problem areas. Special probing and testing apparatus are needed to evaluate the complex parity arrays. Analysis of failures is extremely difficult on the two larger size parity arrays. Strategic pin-to-pin analysis of the larger arrays, plus full analysis of the simpler 3-bit arrays, have been the main tools of analysis, in addition to test patterns which test such things as defect densities in the multilevel insulator structure.

Finally, the three levels of complexity which have been sampled in selecting the 3-, 9-, and 27-bit parity arrays should provide a good indication of the optimum chip size for small-geometry arrays.

Earlier program plans had called for investigations of high-speed saturated microcircuits only in simple microcircuit form. However, a high-speed RTL Memory Array has been chosen instead as the program vehicle for studying saturated microcircuits. Unlike the parity arrays, the RTL can be used and tested in sections so that it should be very useful as a microcircuit study vehicle.

1.3.2 High Performance Microcircuits

A secondary task of the program is to continue investigating the factors which determine performance and yield of small-geometry monolithic microcircuits, using simple microcircuit forms as vehicles.

In the last report we indicated that two new high-speed ECL microcircuit gate designs (SMX6 and SMX7) had been completed. During this period, a decision was made not to fabricate those designs but instead to replace them with two different designs, the SMX8 and the SMX9. The SMX8 is a very low power (0.1-mil geometry) design, calling for a maximum dissipation of 1 mW at propagation delays of 1 - 2 nanoseconds. The SMX9 is a micron geometry design which is expected to operate at or below 0.1 ns. Both designs differ fundamentally from the SMX6 and SMX7 in that they have the emitter follower inputs rather than emitter follower outputs, and as such should be intrinsically faster.

SECTION II - FACTUAL DATA

2.1 SUMMARY

As predicted in the previous report, fabrication of devices was temporarily delayed during this period because of the movement of laboratory facilities from the Lansdale plant to the Blue Bell installation. However, the new facilities have been fully functional for several weeks, and new arrays are being fabricated without delays. Wafers of each array type have been completed at the new facility. During the downtime, much effort was expended on evaluating previously fabricated arrays, examining some of the array problem areas, and designing the two new ECL microcircuits.

2.2 MICROCIRCUIT ARRAYS

2.2.1 Introduction

The parity circuit arrays are complex, high-speed computer-oriented microcircuits which derive their basic high speed capabilities from small-geometry components and shallow component diffusion.

Fundamentally, the 3-, 9-, and 27-bit arrays differ only in complexity, containing 8, 32, and 104 gates, respectively. Figure 1 gives a schematic of the 3-bit array. For a more

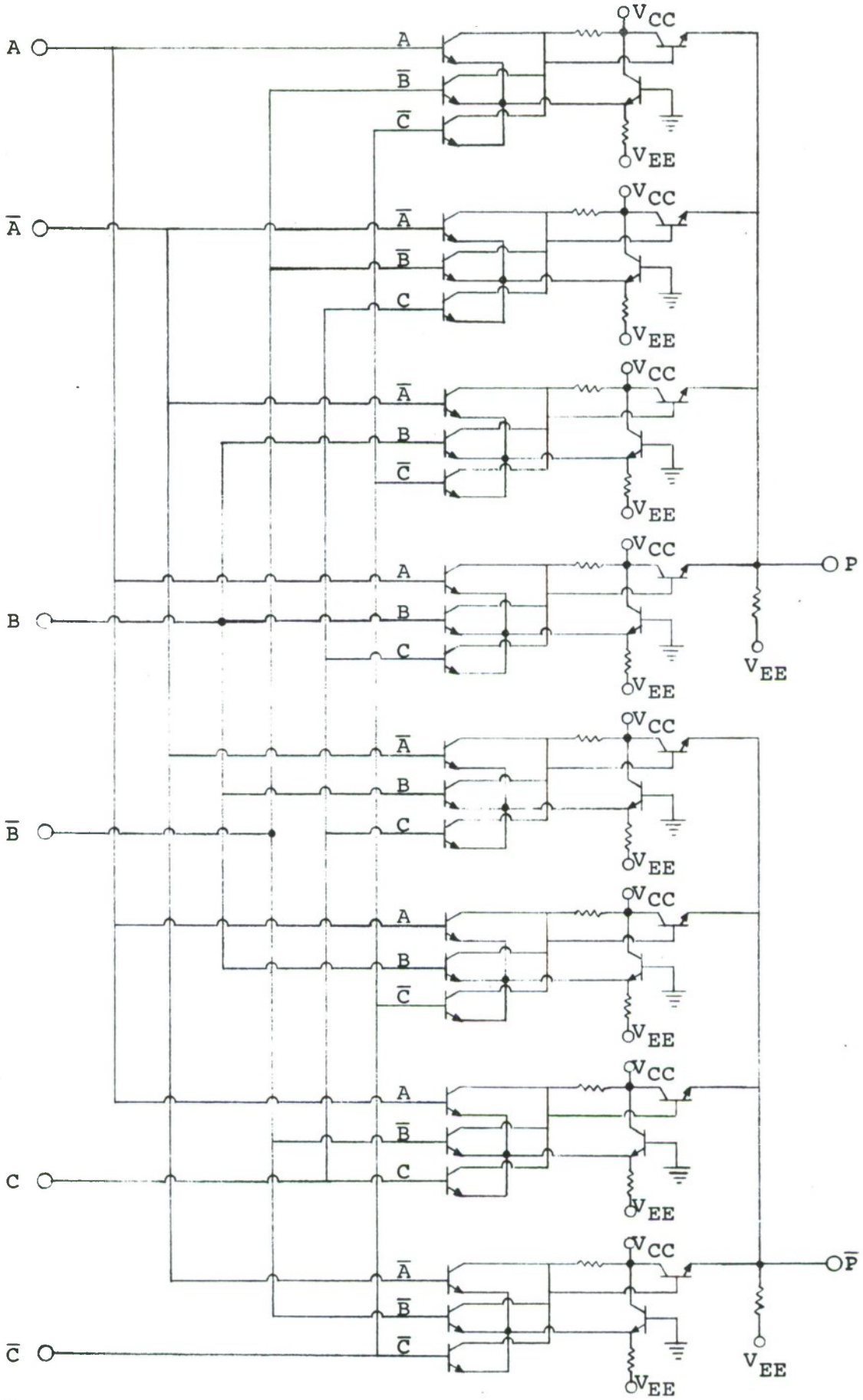

Figure 1. Schematic of 3-bit parity array circuit.

complete treatment of the circuitry of all three array types, as well as a description of the fundamental cell approach to fabricating the arrays, the reader is referred to the Ninth and Tenth Interim Reports.

2.2.2 Array Technology

The last report indicated that process changes at the microcircuit cell fabrication level as well as in multilevel metalization had resulted in an order of magnitude improvement in yields of 3-bit arrays. Device yield analyses and experiments on multilevel test structures indicate that processing is also proceeding at these improved levels at the new Blue Bell facility. Transistor yields of 80 - 90% are being obtained over random portions of wafers, with slightly higher yields being obtained in the prime area portions of wafers. Insulator pinhole levels are at about the same level reported last time.

2.2.3 Yield Analysis

To obtain some specific idea of what level of transistor yields are required to successfully fabricate arrays of the complexity of the 3-, 9-, and 27-bit arrays, a calculation was made to determine the transistor yield required to obtain one array per wafer of each of the various types. We calculated that the required transistor yields are

85% to obtain one 3-bit array per wafer (40 transistors)

97% to obtain one 9-bit array per wafer (160 transistors)

99.8% to obtain one 27-bit array per wafer (520 transistors).

While these requirements are difficult to meet on a wafer-to-wafer basis, they are not impossible, in view of the fact that wafers with a random transistor sampling yield of 95% have been made with the improved processes described in the previous report.

We also examined the extent to which parity array yields are predicted to be affected by interlevel metal shorts caused by pinholes in the multilevel insulating layers. Based on pinhole densities which are being obtained with our double-layer photoresist process, calculations predict that less than 7% of the 3-bit arrays are affected by pinholes. Less than 20% of the 9-bit arrays are similarly affected. The calculation has not yet been performed for the 27-bit array, but it is evident that a reduction in the present defect density is needed to improve chances of obtaining a 27-bit array.

2.2.4 3-Bit Arrays

Several wafers of 3-bit arrays were fabricated during this period, primarily to reevaluate the process as well as to investigate the merits of a new single thick layer photoresist system as a masking medium for insulator photoengraving. The transistor yields quoted above had been obtained from these wafers.

Evaluation of the photoresist system was not completely successful because of inadequacies discovered in the photomasks. Preliminary pinhole tests, however, showed marked improvements in the single layer resist system over the double layer resist process currently being used ($\geq$4 times reduction in pinhole densities). Improved photomasks have been obtained and a more complete evaluation of the new photoresist system is being made.

In the last quarter, we reported that 18 3-bit arrays were obtained from wafer 5 d. While analyzing the source of array opens on rejects from this wafer, we found that opens were in many cases created by an insulating film about 100 - 510 Å thick which existed between the two levels of aluminum. The exact nature of this film could not be determined, but we suspect that it was residual SiO_2 left behind due to uneven etching or incomplete resist removal. During the analysis, in which 6 - 10 volts were applied between terminals, 12 additional arrays were made functional by electrically rupturing the thin barrier. While this is not suggested as being a useful method of obtaining arrays, it does mean that at least 30 arrays on the wafer had 40 good transistors. This calculates out to be better than a 92% transistor yield.

2.2.5 9-Bit Arrays

Several 9-bit arrays which had been diffused using the "old" techniques were completed using the double-layer photoresist process. The yield of 9-bit arrays was zero. Moreover, the patterns and margins of failure indicated that the problem was principally one of transistor yield. This represented the last group of 9-bit arrays processed with the old diffusion methods and the results simply emphasize the significance to yield of the new processes.

It should be noted that on these wafers, we found a slight aluminum etch treatment prior to top aluminum evaporation to be beneficial in reducing contact resistance in interlevel metal contact regions.

2.2.6 27-Bit Arrays

One 27-bit array wafer was processed to completion, and although no functional arrays were obtained, it is important to point out that the margin of failure on a number of the arrays was quite small. Apparently the transistor yields within the arrays were extremely good. One chip failed only one test, and to the extent that we could analyze it, it appeared that the failure could have been caused by from one to four defective transistors. The complete arrays contains 520 transistors.

These results are encouraging and suggest that we are on the verge of fabricating a functional 27-bit array.

In the fourth quarter of this program, a large number of parity array wafers are scheduled for fabrication, especially the 9-bit and 27-bit arrays. To improve the chances of obtaining these arrays, larger (1-1/2" instead of 1-1/4") wafers are being processed. Lincoln Laboratory is sending a functional tester, developed especially for this program, to aid with die sorting as well as final testing.

2.2.7 RTL Memory Array

A tenth-mil geometry, 16-bit RTL Memory Array is being designed by Lincoln Laboratory (under guidance by this group) as a program vehicle for studying high-speed saturated arrays. The RTL array will be less complex than the 27-bit array, but more complex than the 9-bit, containing approximately 300 transistors, including driver transistors. The design is expected to be completed during this quarter.

2.3 NEW MICROCIRCUITS

Plans to fabricate the SMX6 and SMX7, two high-speed ECL microcircuit designs which were generated during the last quarter, were cancelled before photomasks were made of these designs. There were two reasons for the cancellation:

1. It was decided that higher speeds could be obtained if emitter follower input versions of the ECL gate were employed,
2. A change in program emphasis resulted in a desire to study one very high-speed circuit and one very low power circuit, instead of two similar high-speed circuits.

As a result, two new ECL designs, both emitter follower input types, were designed. The first, called the SMX8, emphasizes low power, being designed to operate at 1 mW at speeds anticipated to be between 1 and 2 nanoseconds. Significant features of the SMX8, which is shown schematically in Figure 2, include

1. The employment of transistors with 0.1 x 0.3 mil emitter geometries to obtain high speed at low currents. Transistors will operate at collector currents on the order of 0.1 to 0.2 mA;
2. The employment of multilevel metalization to minimize pad capacities and obtain low capacitance crossovers;
3. The employment of tantalum resistors on the second metalization level.

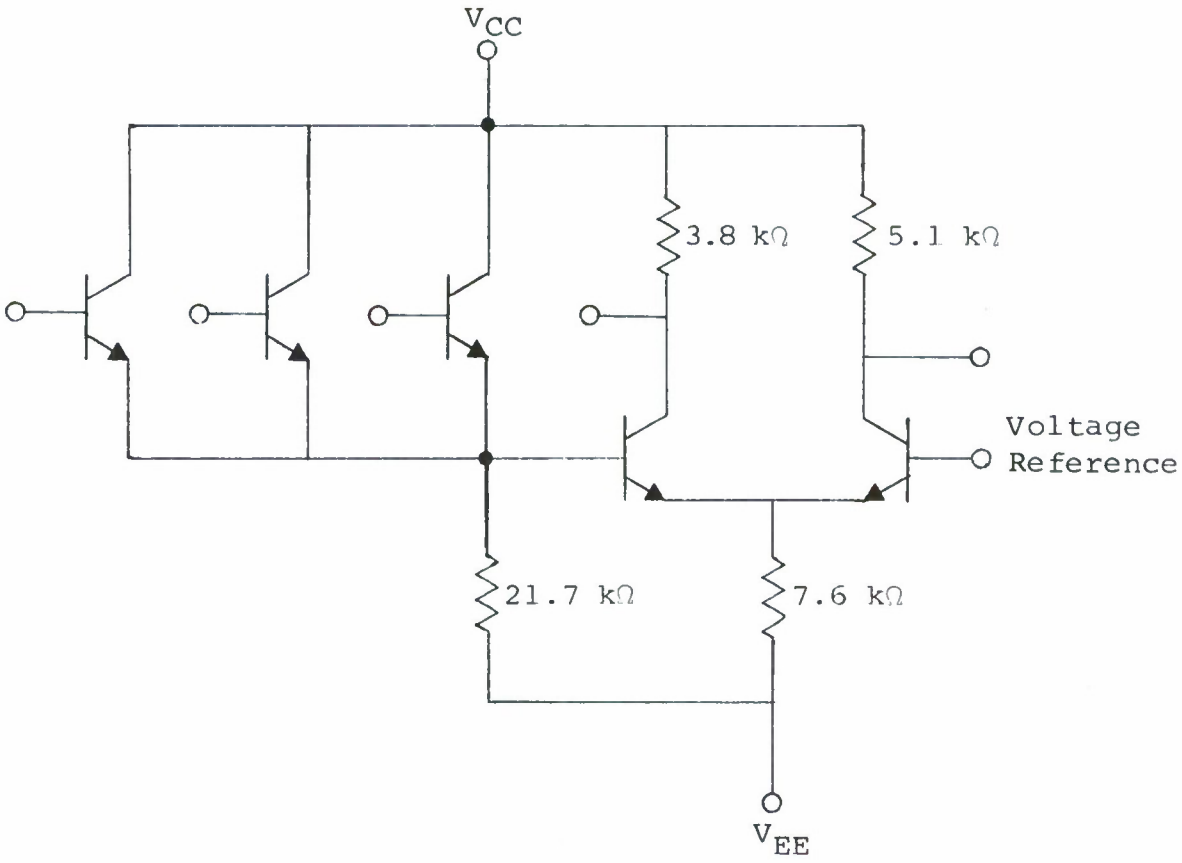

Figure 2. SMX8 low power ECL gate.

The second design, the SMX9, is a high-speed design, anticipated to operate at propagation delays on the order of 0.1 nanosecond with a power dissipation of 35-40 mW. Significant features of this microcircuit include

1. Employment of 0.05-mil geometry transistors,
2. Employment of multilevel metalization to minimize pad capacitances and effect low impedance crossovers.

Figure 3 shows the SMX9 schematically.

It is expected that samples of the low power microcircuits will be fabricated by the end of the fourth quarter. Special techniques are being developed to fabricate precision photomasks for the micron microcircuit. This may preclude complete fabrication of first samples during the next period.

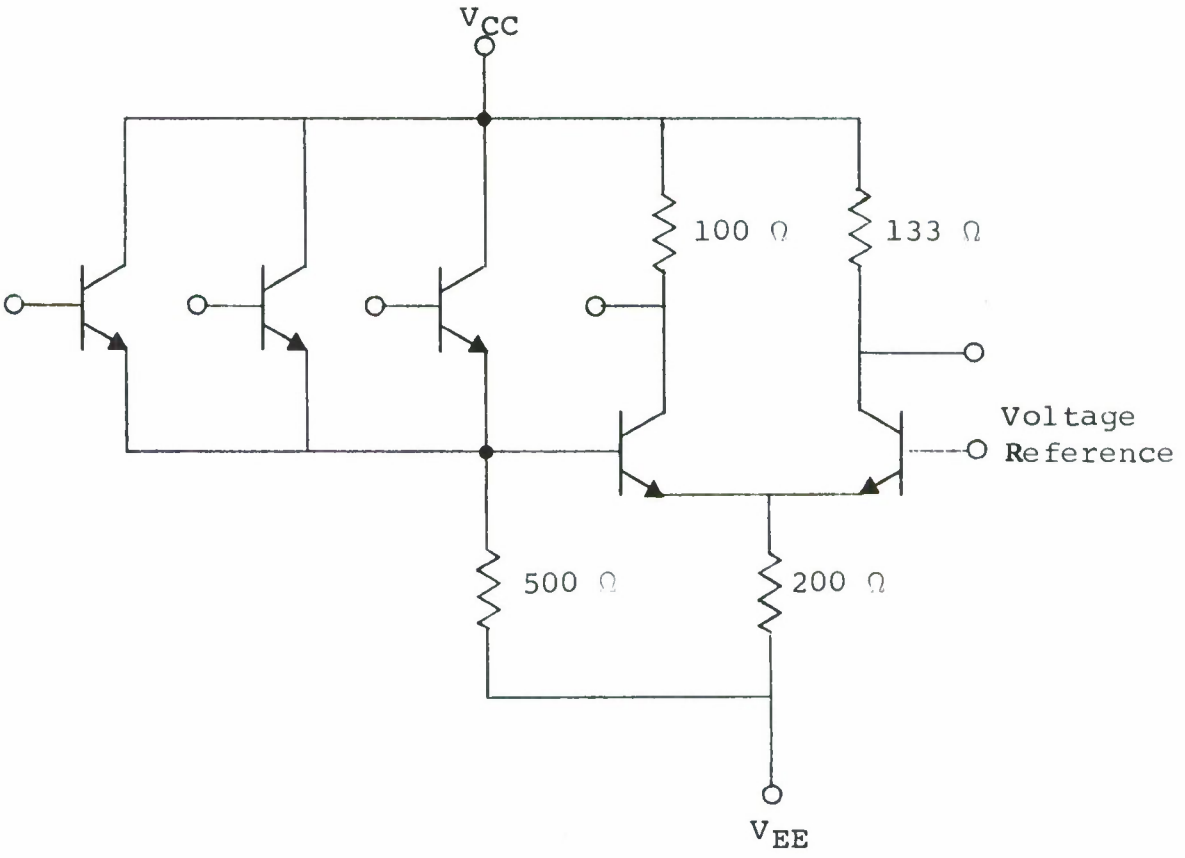

Figure 3. SMX9 high speed ECL gate.

SECTION III - SAMPLE DELIVERIES

During this period, the following samples were delivered to Lincoln Laboratory:

Ten (10) 3-bit parity arrays

Four (4) SX4 transistors.

SECTION IV - FUTURE PLANS

Program plans for the next quarter include the following tasks:

1. Continue to fabricate, but at an accelerated pace, 3-, 9-, and 27-bit arrays, with particular emphasis on the last two. Three-bit arrays will be used mainly to monitor the process and to monitor process improvements which might be tried;
2. Fabricate the SMX8, 1 mW microcircuit gate;
3. Generate photomasks for and fabricate the SMX9, 0.05-mil, 0.1-nanosecond gate.
4. Generate photomasks for and begin fabrication of the RTL array.

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13. ABSTRACT

A description is given of the work performed during the third quarter of the research and development program "R & D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems." The fabrication and evaluation phases of the 3-, 9-, and 27-bit parity arrays continued. The completed SMX6 and SMX7 high-speed ECL microcircuit gate designs were not fabricated but instead were replaced by two new designs, the SMX8 and SMX9.

14. KEY WORDS

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