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Final Report

RELIABILITY TEST PROGRAM OF ULTRASONIC FACE DOWN BONDING TECHNIQUE

Robert P. Moore
Univac Div. of Sperry Rand Corp.

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Air Force Systems Command
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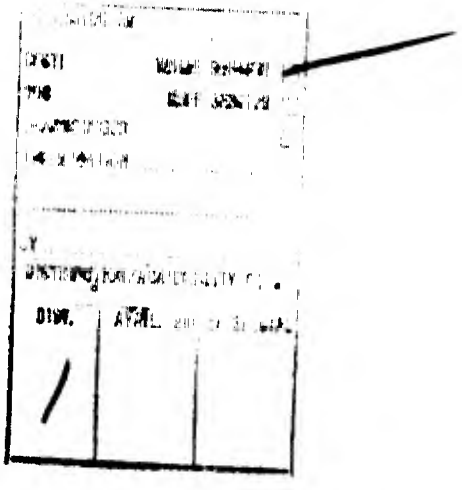

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FOREWORD

This final report was prepared by Robert P. Moore of Sperry Rand Corporation, Univac Division, Blue Bell, Pennsylvania, under Contract AF30(602)-3921, project number 5519, task number 551904. Reporting period covered was from 10 November 1965 to 31 January 1967. RADC project engineer is John E. McCormick (EMERM).

This technical report has been reviewed by the Foreign Disclosure Policy Office (EMLI) and the Office of Information (EMLS) and is releasable to the Clearinghouse for Federal Scientific and Technical Information.

This report has been reviewed and is approved.

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ABSTRACT

A study has been performed by the Univac Division to determine the overall reliability of its face-down-bonding process and to determine whether the bonding process damages the chip. The ultrasonic direct-bonding process was used to fabricate approximately 900 test samples for this study. Samples were subjected to the following tests: shear, mechanical shock, thermal shock, vibration, centrifuge, high-temperature storage, elevated-temperature back bias, step stress and comparison, and temperature and humidity. Defective units were examined for causes of failure. The test results indicate that the stresses applied during bonding do not affect circuit operation. The bond failure rate was high, but the distribution of failures suggests that this was due to inadequate substrate process control rather than inherent problems with face-down bonding. The substrate interconnect wires corroded in high-temperature and high-humidity ambients. Several potential solutions to this problem are suggested.

ILLUSTRATIONS

ILLUSTRATIONS

LIST OF TABLES

EVALUATION

The objectives of this program were to evaluate face down microelectronic interconnections made by ultrasonic techniques, and to determine how much, if any, damage was done to a silicon chip by the application of ultrasonic energy.

The tests used in this program are comparable to those used in evaluating integrated circuits packaged in hermetically sealed containers. The silicon chips and the bonds resisted the effects of these severe tests surprisingly well. The thin film aluminum deposited on both chip and substrate was attached to some degree during the high temperature and high humidity tests.

The tests conducted during this program have demonstrated that ultrasonic face down bonding, where the ultrasonic energy is applied diretly to the silicon chip, causes no apparent degradation to the electrical performance of a silison integrated circuit over a period of approximately one year and under extremely severe environmental stresses.

This ultrasonic face bonding technique appears to be the most economical and most reliable means for packaging and connecting integrated circuits at the chip level that we have investigated to date.

The results of this program have been compared with another all aluminum bonding technique involving thermal techniques (Diffusion Bonding Program). As stated above, ultrasonic bonds offer comparable reliability at lower cost.

A follow-on program will investigate (a) the amount of damage, if any, done to the glass or oxide coating covering an integrated circuit by ultrasonic energy; and (b) techniques for measuring mechanical stresses at the bond sites caused by thermal coefficient of expansion mismatches between silicon and substrate material.

John E. McCormick

JOHN E. McCORMICK
RADC Project Engineer

SECTION I

INTRODUCTION AND SUMMARY

1. OBJECTIVE

This volume is the final report of work performed under contract AF 30(602)-3921. The objective of this program was to investigate the effects of ultrasonic bonding on monolithic circuits. Life and environmental tests were performed to obtain reliability data and to determine whether the damage caused by the bonding process affects the operation of the monolithic circuits. Failure analysis was conducted to determine failure modes and to establish whether the failure was in the substrate, the silicon chip, or the bond.

2. BACKGROUND OF THE BONDING PROCESS

Several techniques for bonding integrated circuit chips directly to evaporated aluminum wiring have been described in recent literature.[1] Systems assembled by means of these techniques are theoretically more reliable than systems assembled from conventionally packaged integrated circuits because fewer bonds are required in the direct-bonding process. Three bonds are required per chip contact when the chips are packaged in cans or flat packs; two in the package and one to the external circuitry. Only one bond

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[1] Matcovich, T. J., Memory Systems for Microcircuits (Manufacturing Methods), Technical Documentary Report No. AFML-TDR-66-42, Wright-Patterson Air Force Base, Ohio, March 1966.

is required per contact when the direct-bonding technique is used. Improved reliability will be realized if the direct bond is at least comparable in reliability to the thermocompression bonds used in the can or flat pack and if the bonding process does not damage the chip.

A cross section through a bonded chip is shown in Figure 1. The aluminum wires are evaporated through masks onto the substrate. The wires are raised on pedestals at the contact location to allow ease in bonding and to provide clearance under the chip for substrate wiring.

Note that the pedestals have tapered sides. The taper is essential to ensure the electrical continuity of the evaporated conductor. This taper can be simply achieved by spacing the masks a few thousandths of an inch from the substrate during the evaporation process. Note also that the electrical contact is made directly to the evaporated wire and that the pedestal serves only to raise the wire at the contact point. A transparent substrate (glass) is used so that the chip may be viewed through the bottom of the substrate during the bonding process. This permits the chip lands and the substrate pedestals to be aligned visually.

The bonding process is shown schematically in Figure 2. The chip is lifted by means of a vacuum pickup and placed over the pedestals on the substrate. The chip is viewed through the substrate and is manipulated until the chip pads and substrate pedestals are aligned. The bonding tip in the transducer head is brought in contact with the back of the chip and a downward clamping force is applied to the chip. When ultrasonic energy is applied, a lateral "scrubbing" between the chip land area and the aluminum conductor over the pedestal takes place for a predetermined interval of time. The result is a molecular bond between each of the chip pads and the corresponding substrate wires.

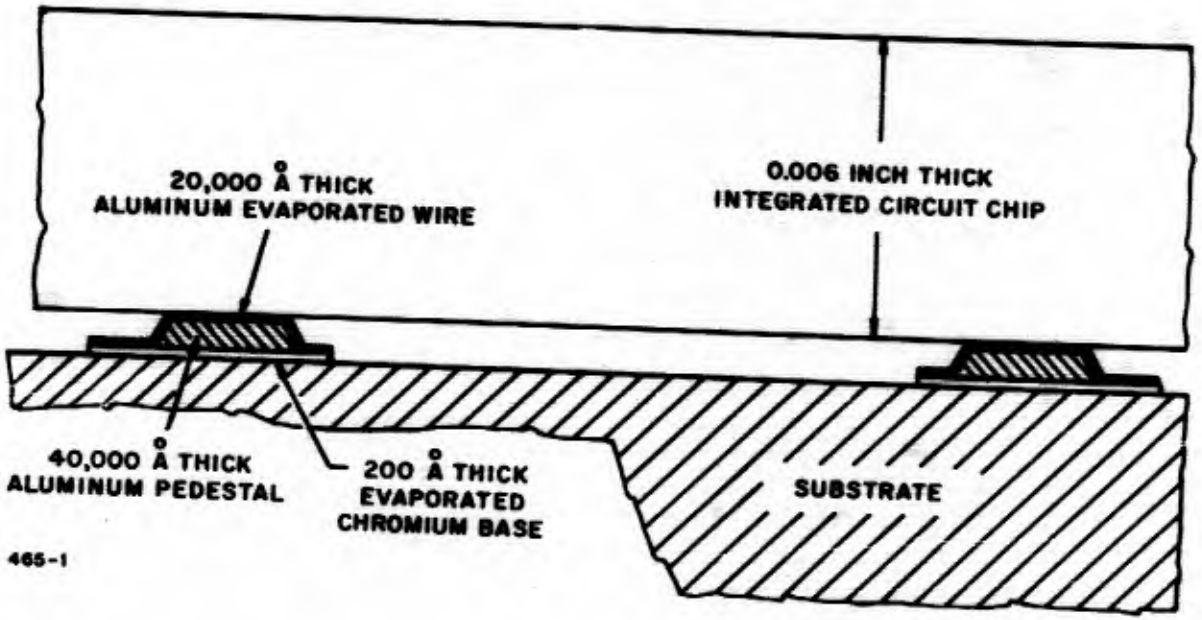


Figure 1. Cross Section Through Bonded Chip and Substrate

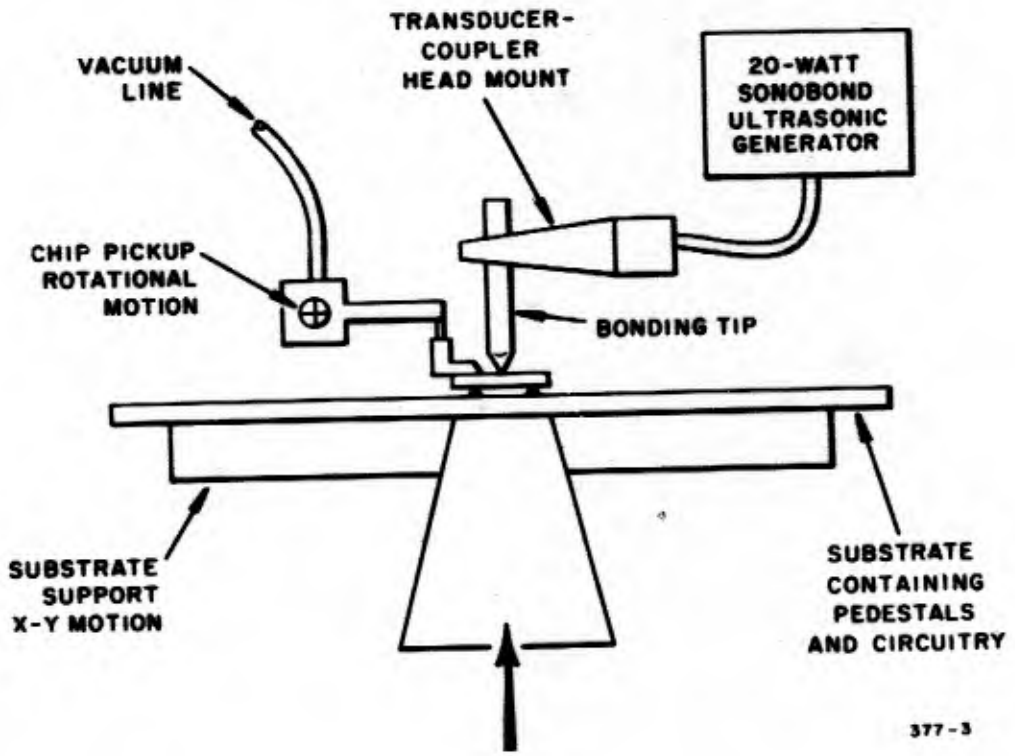


Figure 2. Schematic Diagram of Chip-Bonding Process

A bonded chip, viewed through the substrate, is shown in Figure 3. Figure 4 shows the pedestals and the wiring before bonding, and Figure 5 shows the chip on the pedestals after bonding. A mark made by the bonding tip is visible on the back of the chip (Figure 5) at the point of application of ultrasonic energy.

The bonds made by this process are mechanically strong and have low electrical resistance. Chips can be removed and replaced, if the bonding parameters are properly chosen. To accomplish this, the clamping force is reduced until the bond becomes the weakest point in the structure; when a shear force is applied the structure breaks cleanly at the bond. By proper choice of clamping force, bonds can be made sufficiently strong to pass vibration and shock tests, yet sufficiently weak to shear cleanly for replacement. The magnitude of clamping force will vary with pad and pedestal size and with the number of pedestals. Consequently, the appropriate magnitude has to be determined for each system.

3. SUMMARY

A study has been performed to determine the reliability of the direct bond and to determine whether the bonding process damages the chip. The ultrasonic direct-bonding process developed by the Univac Division was used to fabricate approximately 900 test samples for this study. Since the bonding process is in the early stages of development, the bond reliability data obtained in this study indicate areas requiring improvement rather than the maximum obtainable reliability for this type of bond. The data indicate that strong bonds can be made, but that a method must be developed to protect the aluminum interconnect wires from the corrosive effect of high humidity and temperature ambients. There was no indication of damage to the chip due to the bonding process.

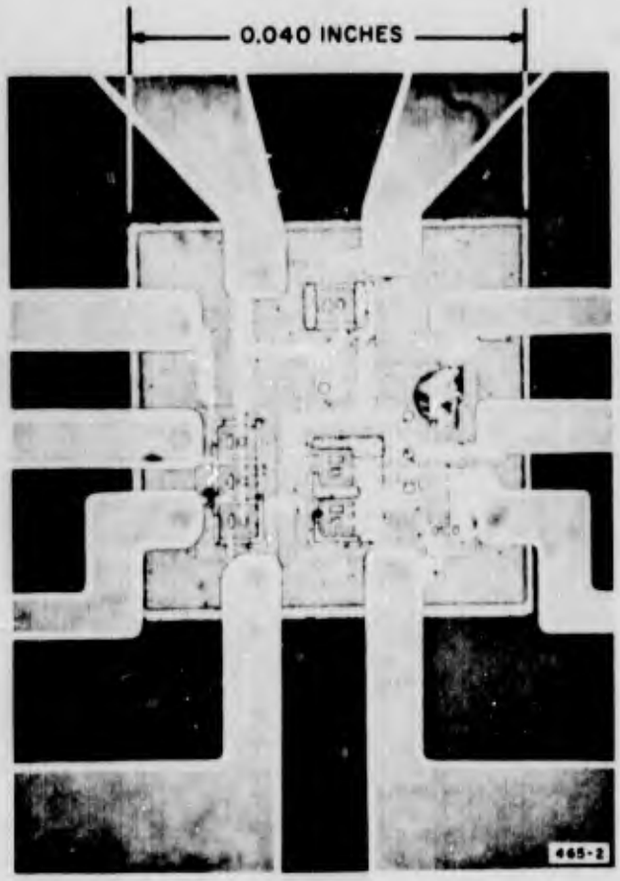


Figure 3. Photograph of Bonded Chip Viewed Through Substrate

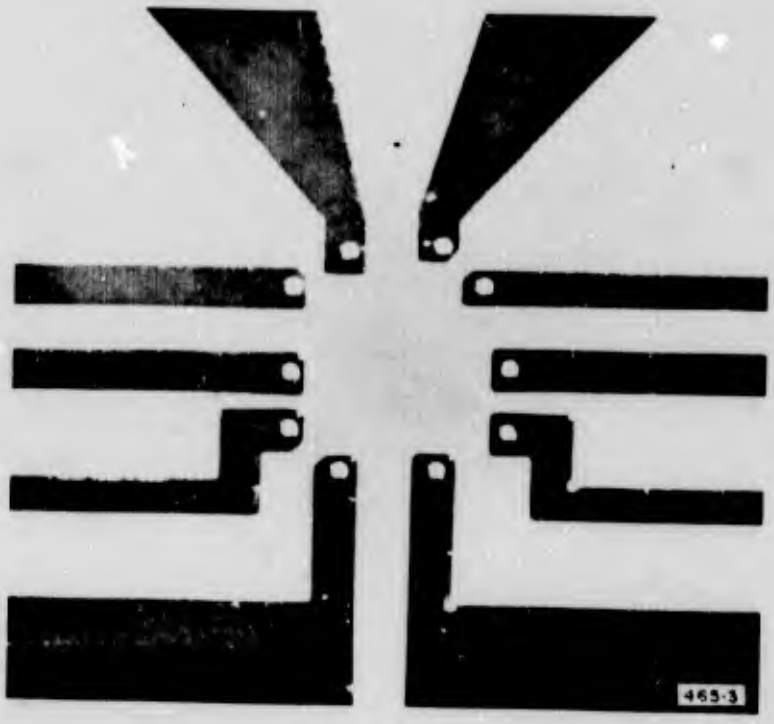


Figure 4. Photograph of Pedestals and Evaporated Wires

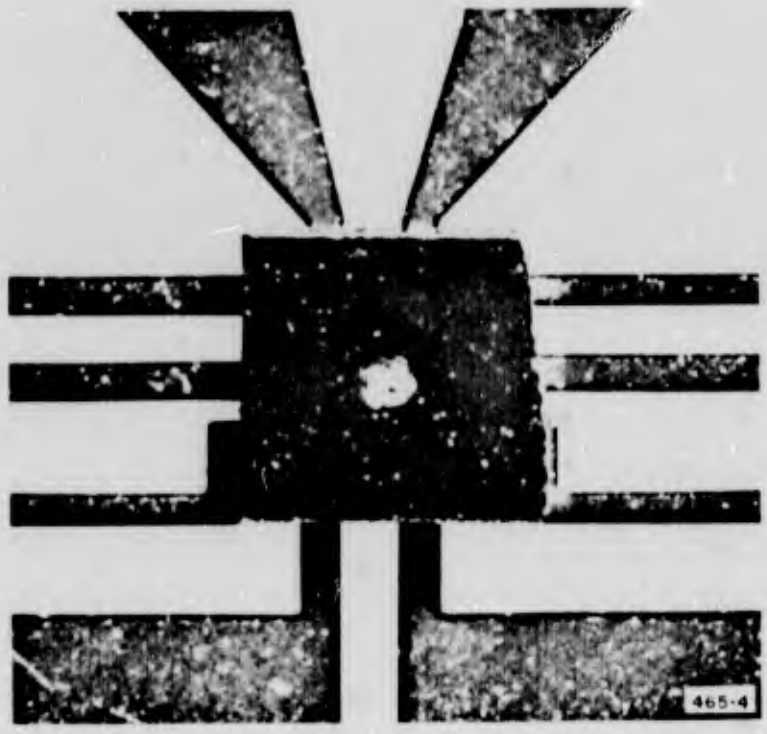


Figure 5. Bonded Chip, Showing Tool Mark

The details of the reliability study are presented in the following sections.

SECTION II

MATERIALS

1. SUBSTRATE

A transparent substrate (glass) was used to allow the chip to be viewed through the bottom of the substrate during bonding and to allow visual inspection of the wiring and chip after tests were performed. Corning type 7059 glass was chosen to match the thermal coefficients of expansion of the substrate and the silicon chip. The substrates were 1 inch wide, 1.54 inches long, and 0.031 inch thick. This size was chosen so the substrate would fit an available 30-pin printed-circuit-card socket used in the testing equipment.

2. INTEGRATED CIRCUIT CHIP

The chips used were 10-pad, glass-passivated Motorola type MC 306 gates, 40 mils square. A typical MC 306 chip is shown in Figure 6, along with the schematic drawing for the circuit.

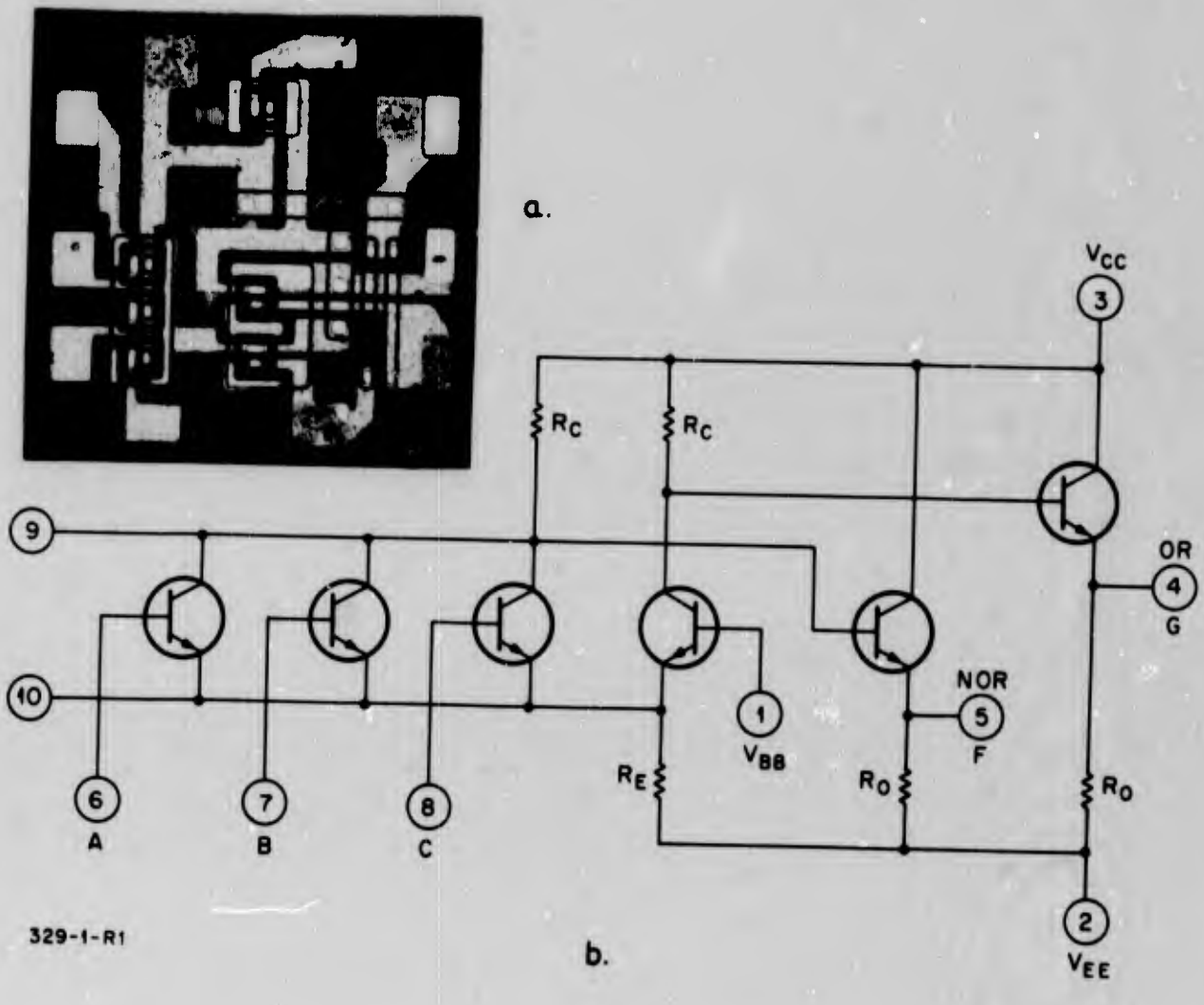


Figure 6a. Motorola MC 306 MECL Integrated Circuit Chip

Figure 6b. Schematic Diagram of Motorola MECL Logic Gate

SECTION III

SAMPLE PREPARATION

1. SUBSTRATE WIRING EVAPORATION

A typical substrate is shown in Figure 7. The aluminum pedestals and wires were evaporated on these substrates through electroformed nickel masks. The pedestal mask and the wiring mask are shown in Figure 8; the evaporation system in which the substrates were fabricated is shown in Figure 9.

The evaporation process is carried out in the following steps. First, a 200-Angstrom-thick layer of chromium is evaporated to improve the adhesion between the subsequently deposited aluminum layers and the glass. Next the pedestals are evaporated, then the interconnect wires. The 20,000-Angstrom-thick aluminum interconnect wires bring all the chip connections to convenient access points at the edge of the substrate. The pedestal diameter is nominally 0.0025 inch at the base. The diameter decreases during each evaporation because of the deposition of aluminum on the masks. The masks are cleaned after every fourth evaporation to limit the reduction in the pedestal diameter. The pedestals, made 40,000 Angstroms high for the first three evaporations, are made 60,000 Angstroms high on the fourth evaporation to compensate for the decrease in pedestal diameter. Measured values for the pedestal dimensions are shown in Table I, and actual views of the pedestals are shown in Figure 10. Since the reduction in pedestal size might affect the failure rate, the evaporation number for each sample was recorded.

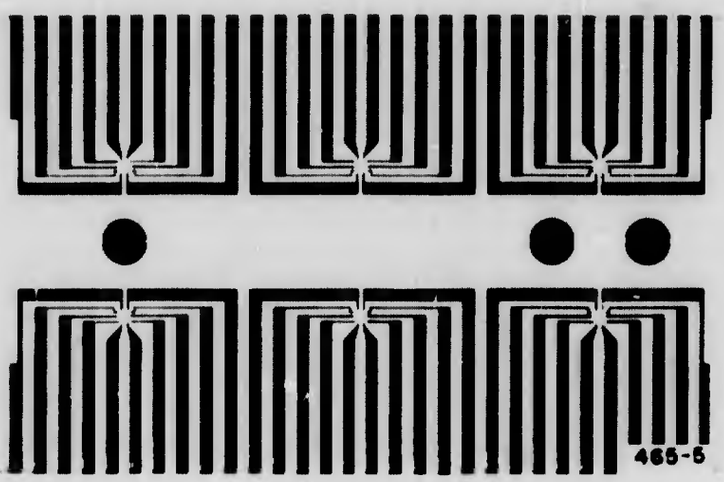


Figure 7. Photograph of Typical Substrate

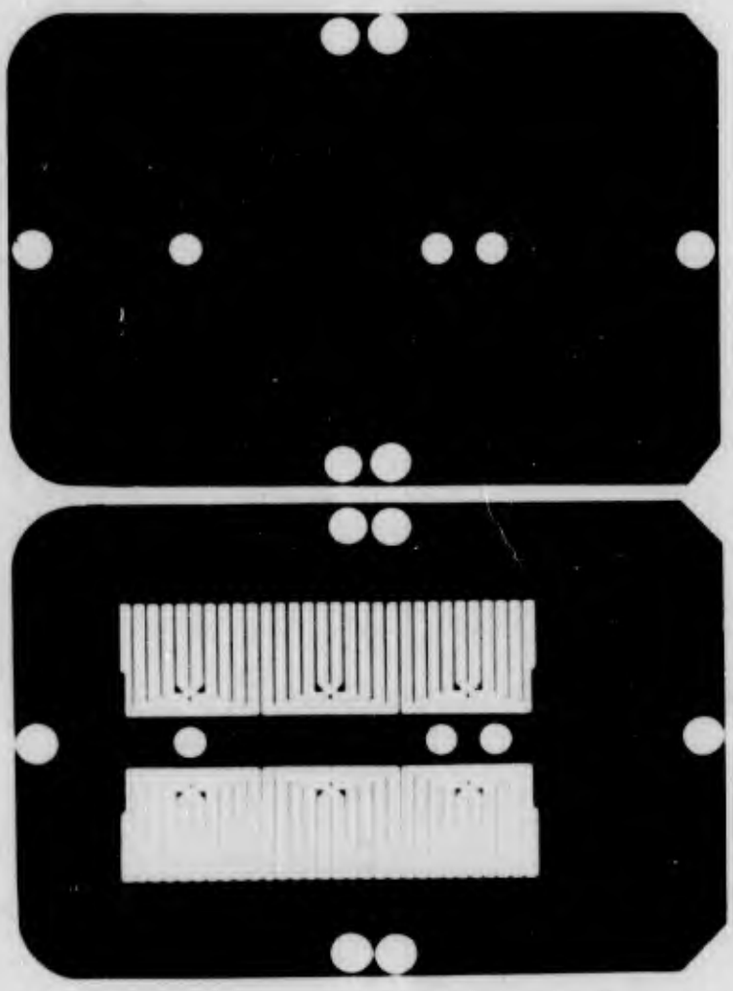


Figure 8. Pedestal and Wiring Evaporation Masks

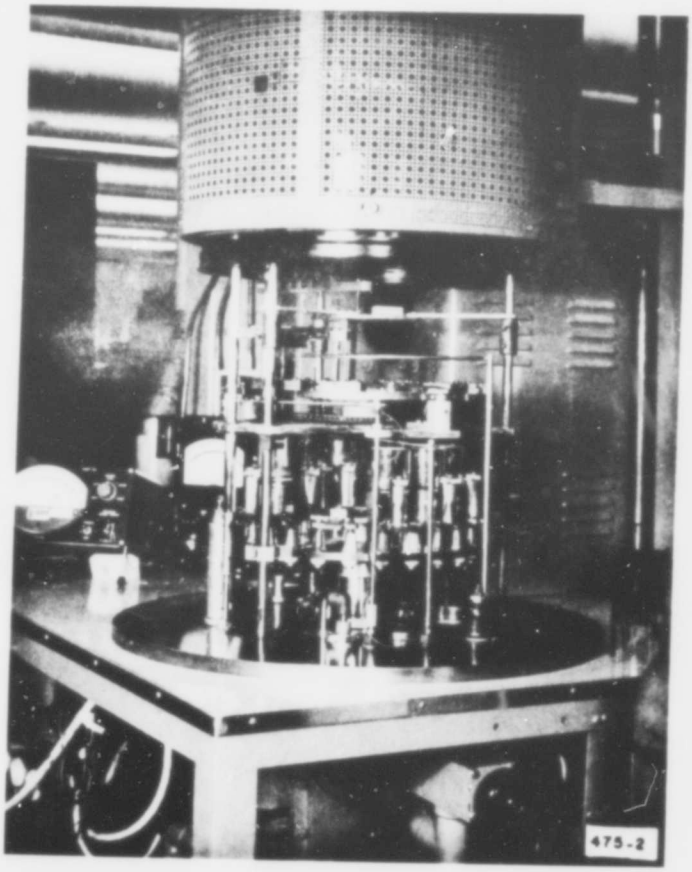


Figure 9. Evaporation System

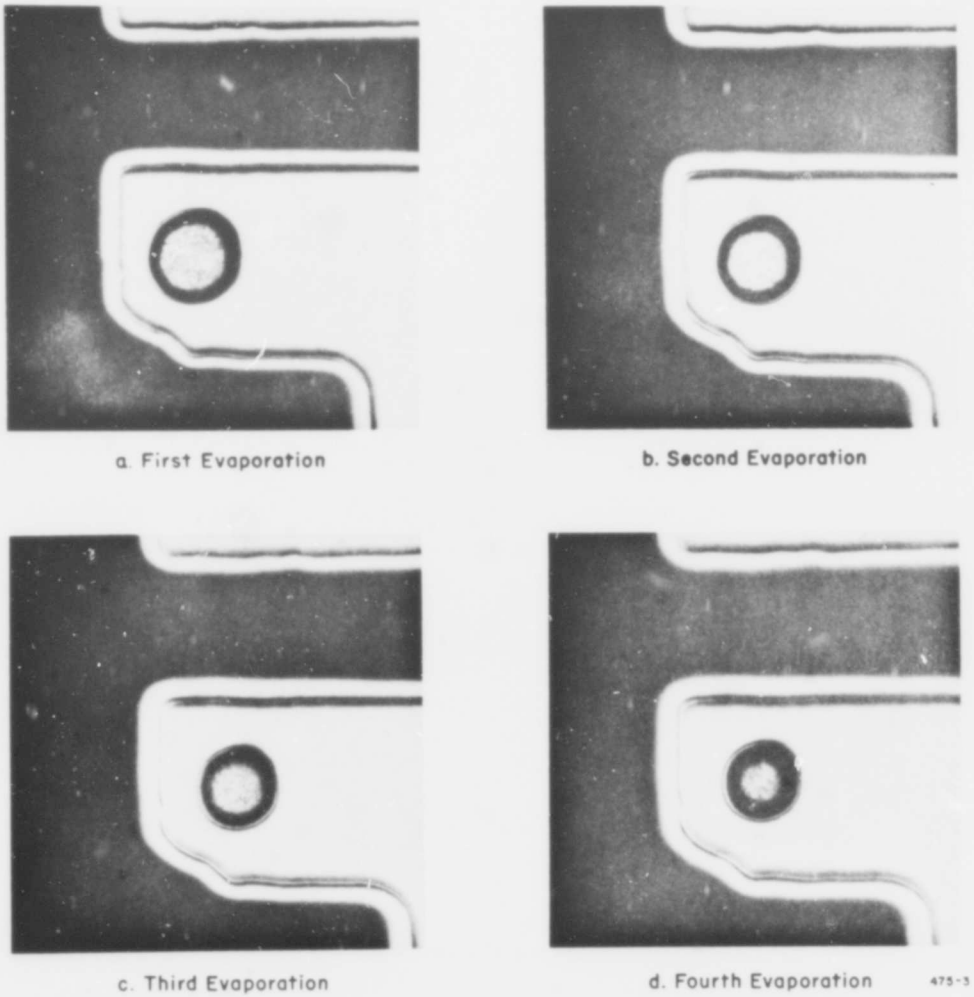


Figure 10. Photographs Showing Pedestal Variation in Successive Evaporations

TABLE I. Typical Pedestal Dimensions

Evaporation Number	Pedestal Base Diameter (inch)	Pedestal Plateau Diameter (inch)	Pedestal Height (Angstroms)
1	0.0025	0.0018	40,000
2	0.0024	0.0016	40,000
3	0.0022	0.0013	40,000
4	0.0020	0.0010	60,000

2. CHIP TESTING

Equipment developed by the Univac Division for performing d-c, a-c, and functional tests on integrated circuit chips was used to test all chips used in this program prior to bonding. The test equipment, shown schematically in Figure 11, consists of a test circuit board, a micromanipulator, a vacuum pickup, and viewing optics. A glass section of the test board contains aluminum pedestals used for the chip contacts. Connections are made to the external test circuitry by pressing the chip against the pedestals on the test card.

Pedestals are 40,000 Angstroms thick. The micromanipulator and the vacuum pickup are used to position the chip on the pedestals and to hold it there with sufficient force to ensure good contact. Pedestals are flash-coated with 200 Angstroms of chromium to minimize oxide formation and thereby to lower contact resistance. A vibrator, mounted on the vacuum pickup, is used when necessary to reduce contact resistance. A photograph of the tester is shown in Figure 12.

3. CHIP BONDING

Chips were face-down-bonded to the evaporated aluminum wires on the glass substrates. The chip pads were visually aligned with the pedestals

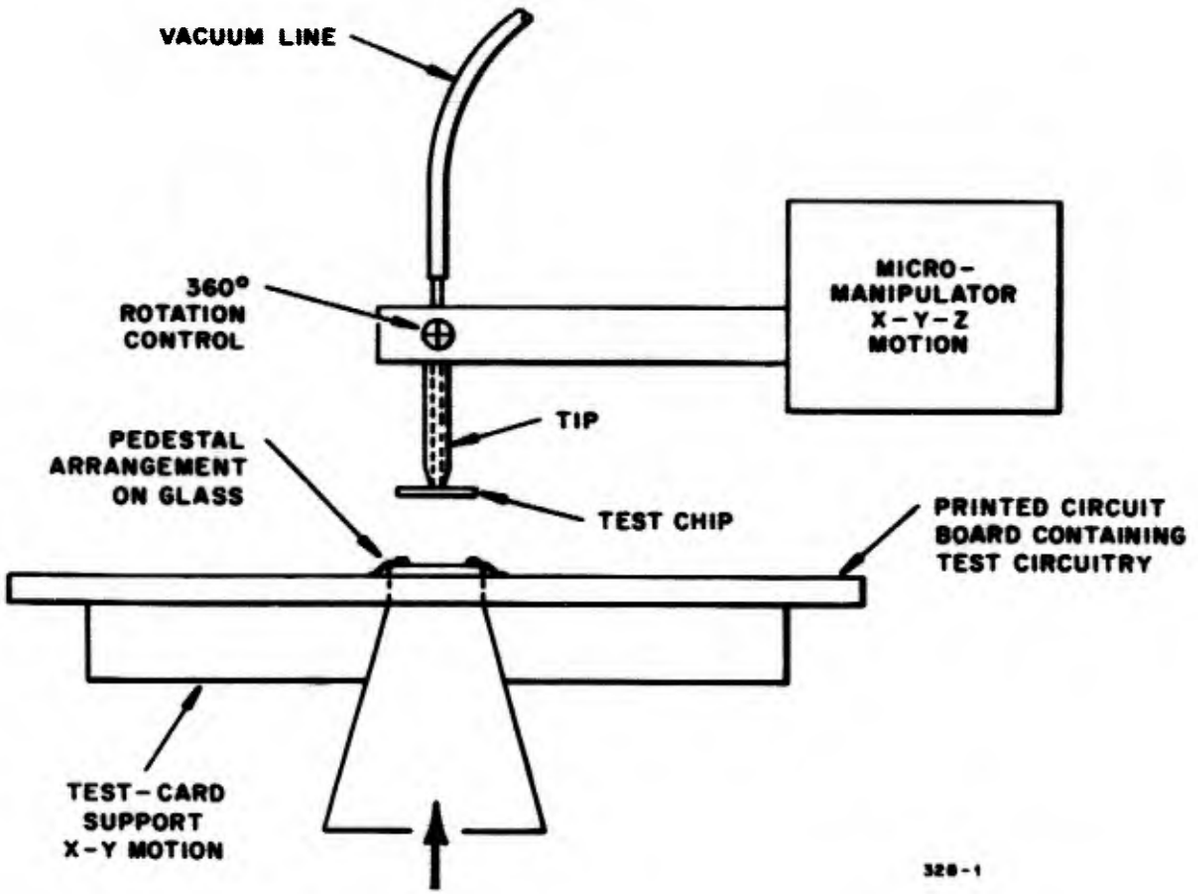


Figure 11. Schematic Diagram of Chip Tester

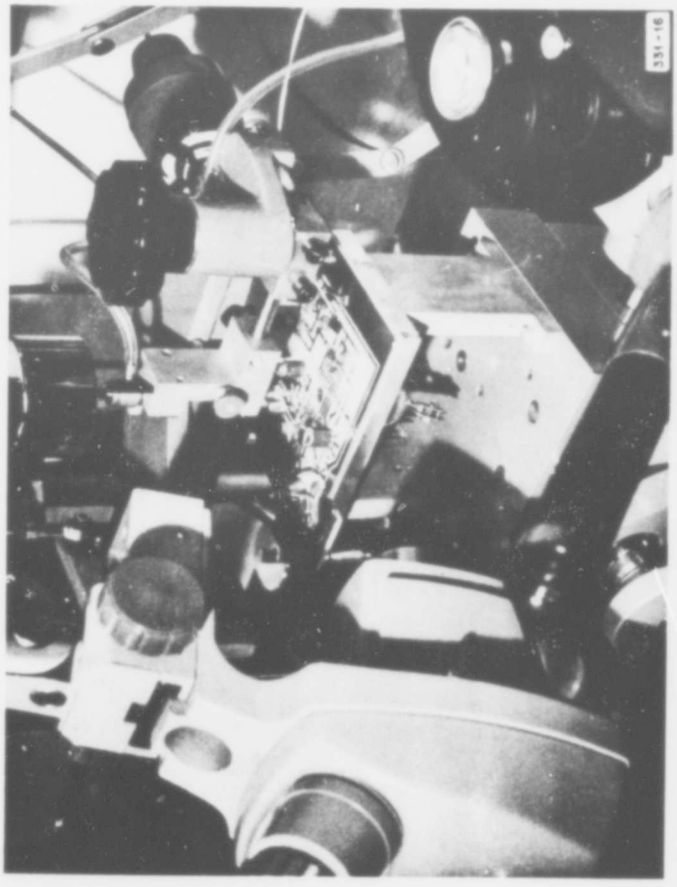


Figure 12. Chip Tester

on the substrate and were then clamped to the pedestal by the bonding tool. The energy transfer from the ultrasonic transducer to the chip is made by means of the tip. Four tip designs are shown in Figure 13. Good, reliable bonds are made when the truncated pyramid tip shown in Figure 13a is used, provided the chips are square. Energy is transferred along the chip edges; consequently, chips which have damaged or irregular edges do not bond well. Since this chip condition is common in chips which are obtained from scribed and broken wafers, and since this is the most general method of cutting wafers into chips, this tip has limited application. Good bonds are also made when the sharp-edged tip shown in Figure 13b is used. Problems arise from incorporating the vacuum pickup into the tip; consequently, the usefulness of this design depends on the specific application. Poor bonds are made when the sharp needle-point tip shown in Figure 13c is used. Frequently the chip is thrown out from under the bonding tool. Good bonds are made when the blunt needle-point tip shown in Figure 13d is used. This design was used on the bonding equipment used in this study. Clamping forces of 0.5 pound and 1.0 pound were used. A spring force gauge was used to calibrate the clamping force at the point of application. Ultrasonic bonding energy was obtained from a 20-watt Sonobond model W-260-TSL generator; the time setting on the generator was 2, and the power setting was 4. The face-down-bonding equipment is shown in Figure 14, and a close-up of the bonding tip and work area is shown in Figure 15.

4. TEST PLATES

A typical test plate is shown in Figure 16. All plates were functionally tested to ensure that the units were good before subjecting them to the environmental and life tests. Data were recorded of each plate for purposes of comparison with data obtained at the conclusion of the tests.

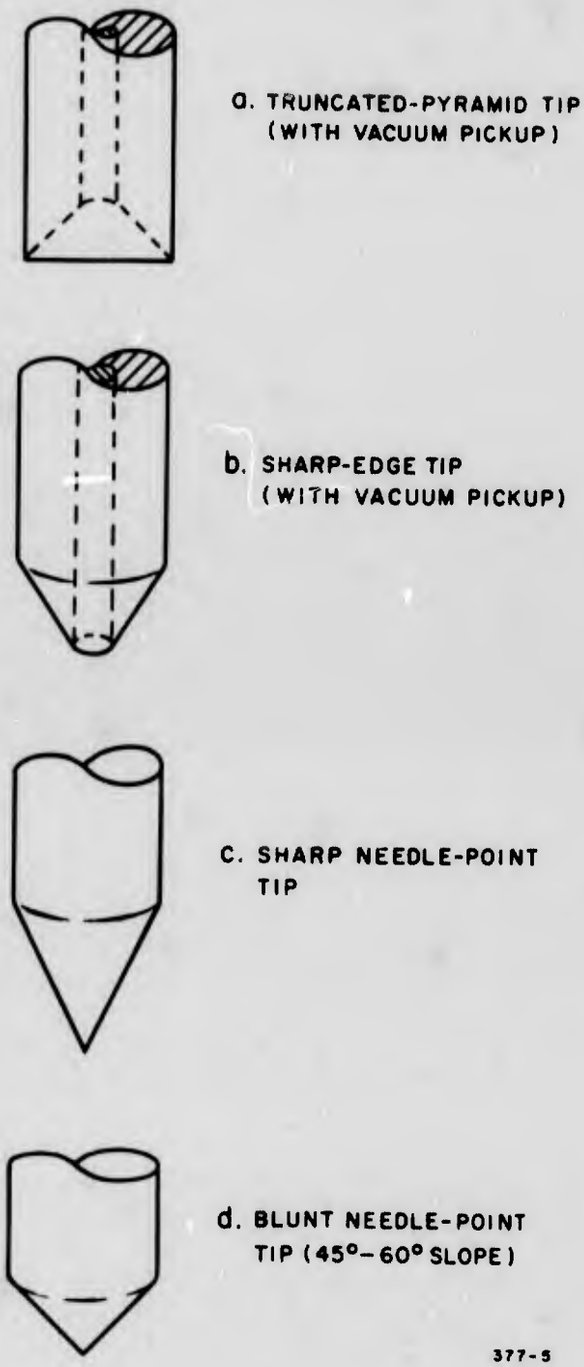


Figure 13. Bonding Tip Designs

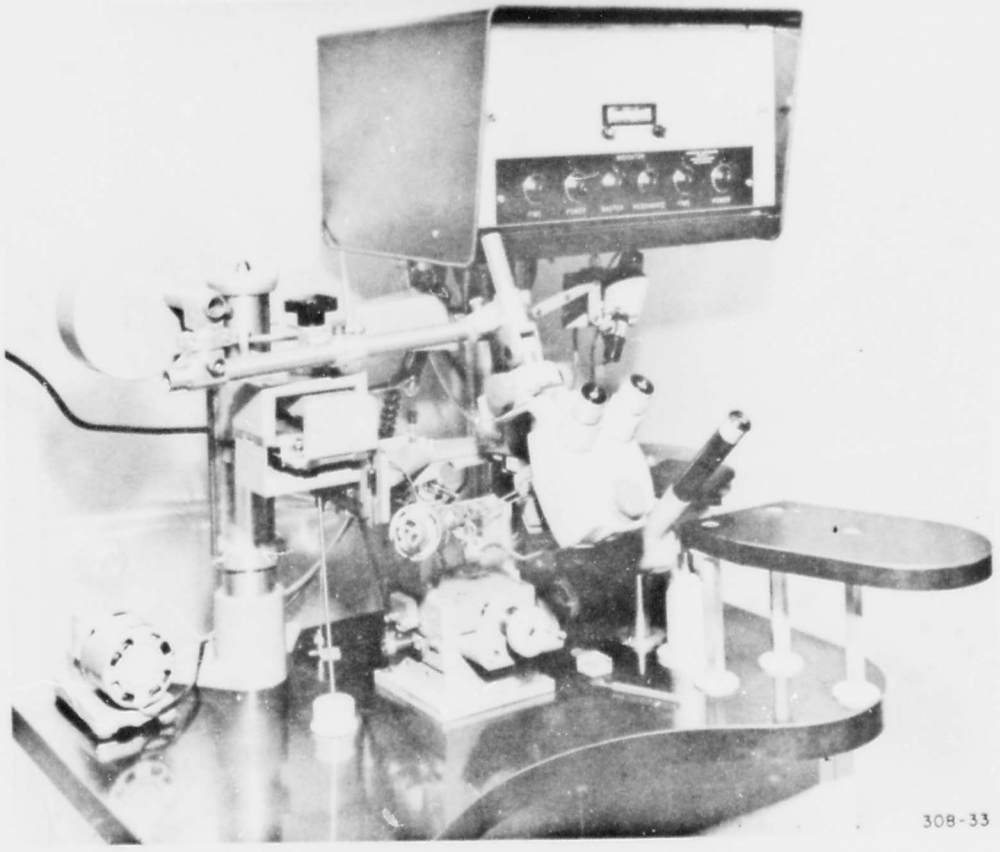


Figure 14. Ultrasonic Face-Down-Bonding Equipment

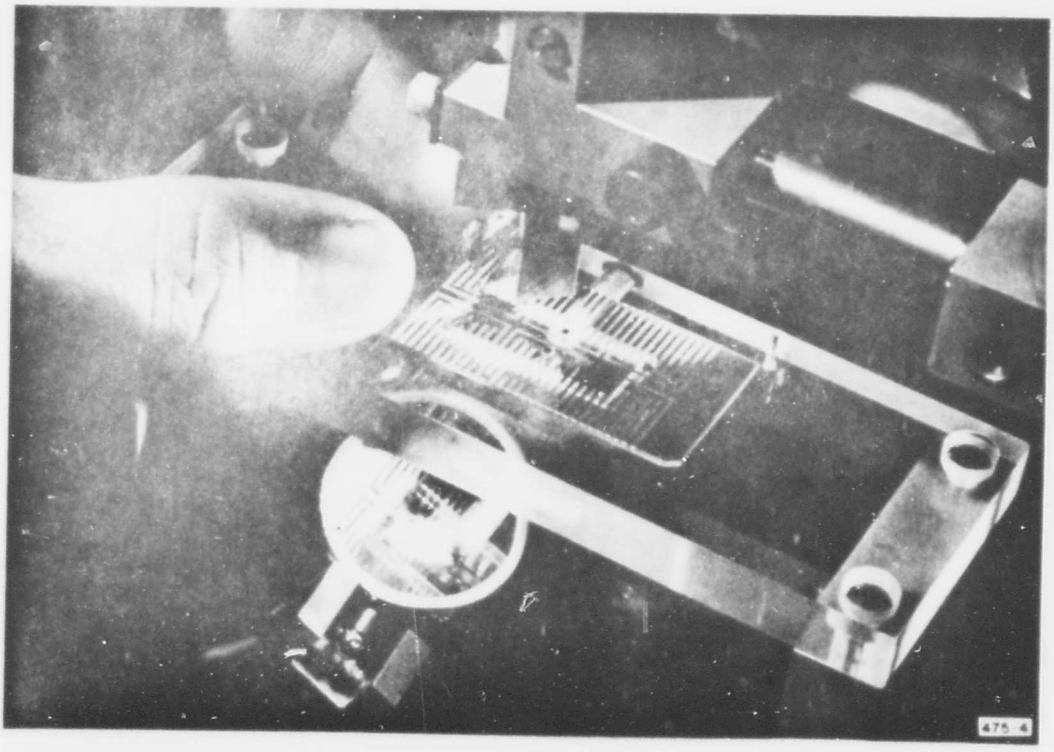


Figure 15. Close-up of Bonding Equipment

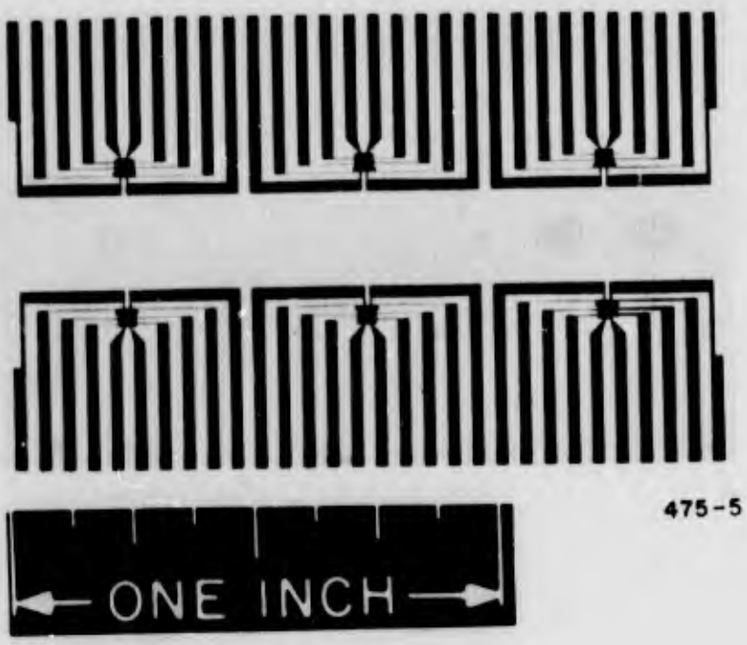


Figure 16. Typical Bonded Test Plate

Figure 17 shows the functional tester used, and Figure 18 shows the basic schematic drawing of the functional test circuit.

5. SAMPLE GROUPS

Three sample groups were used for each test. Group I samples were bonded at a 1-pound clamping force and were potted in silicone resin. Group II samples were bonded at a 1/2-pound clamping force and were potted in silicone resin. Group III samples were bonded at a 1/2-pound clamping force and were not potted. Chips bonded at a 1/2-pound clamping force were replaceable; those bonded at a 1-pound clamping force (Group I) were not. All chips were functionally tested before and after bonding.

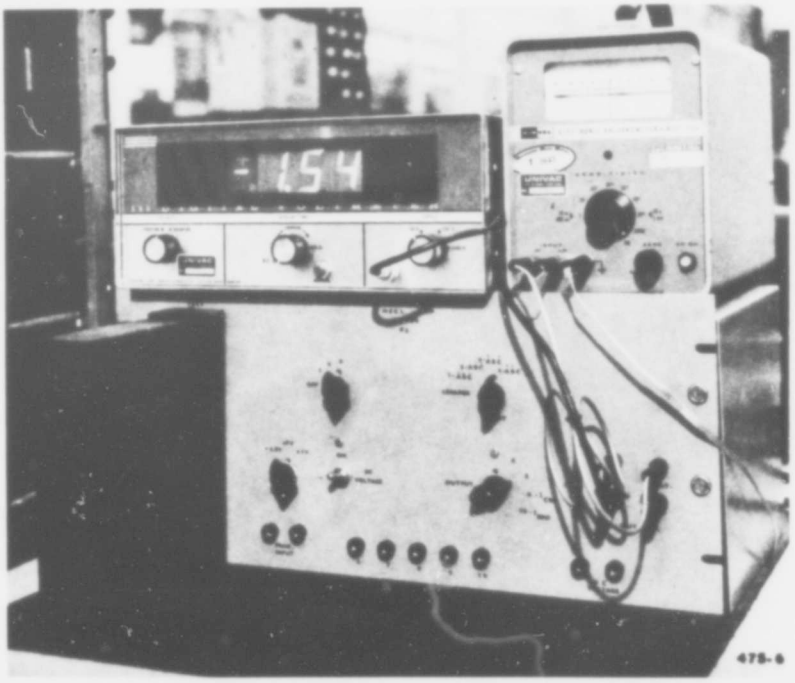
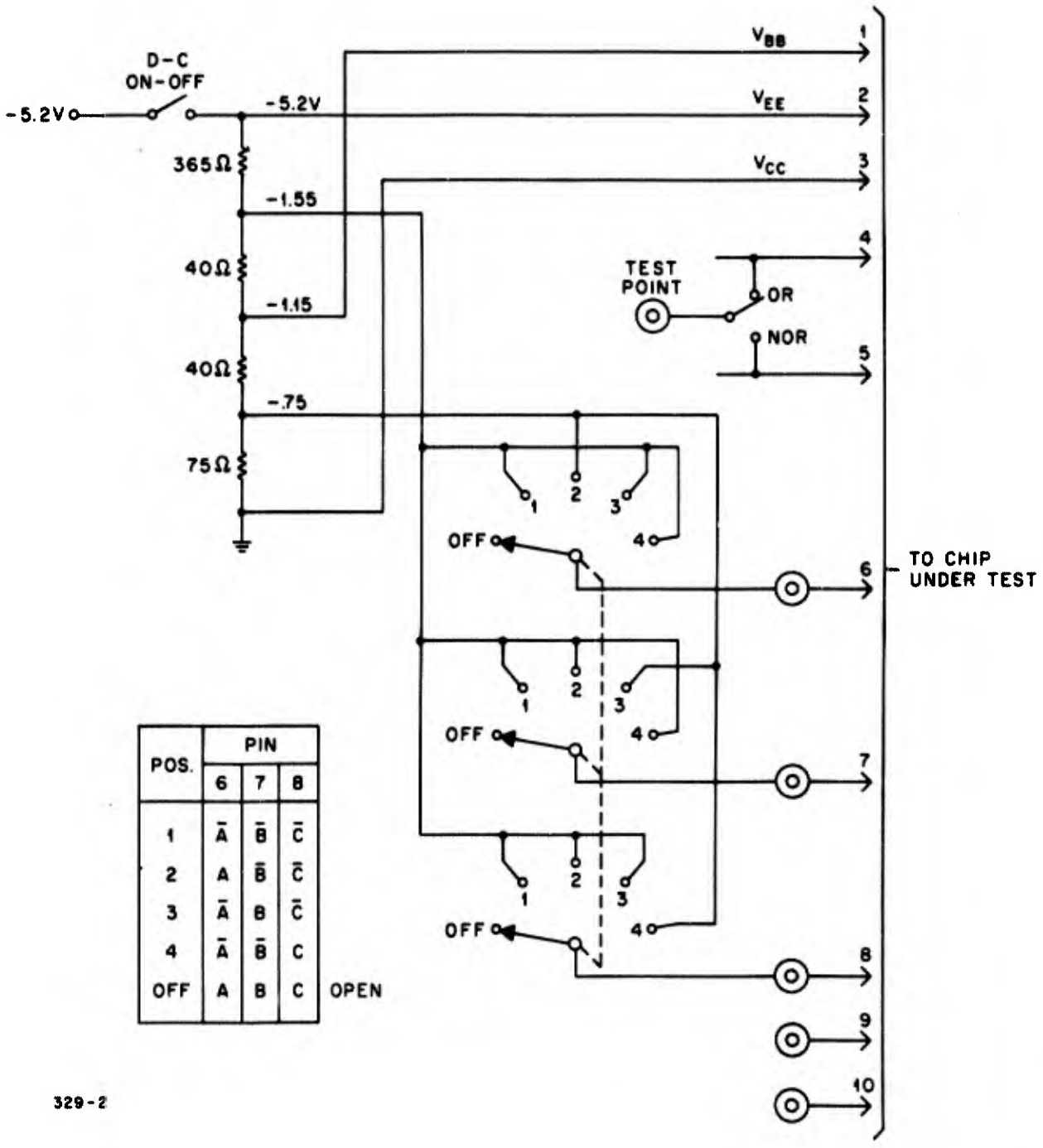


Figure 17. Functional Tester



POS.	PIN 6	PIN 7	PIN 8	
1	$\bar{A}$	$\bar{B}$	$\bar{C}$	
2	A	$\bar{B}$	$\bar{C}$	
3	$\bar{A}$	B	$\bar{C}$	
4	$\bar{A}$	$\bar{B}$	C	
OFF	A	B	C	OPEN

Figure 18. Basic Schematic Diagram of Functional Tester Shown in Figure 17

SECTION IV

TEST DESCRIPTION AND RESULTS

1. ENVIRONMENTAL TESTS

Sets of thirty or more test samples from each group were subjected to shear, vibration, mechanical shock, centrifugal stress, thermal shock, and temperature and humidity tests. These tests and results are described in this section.

a. SHEAR

For this test, 73 chips were bonded at a 1/2-pound clamping force and 71 at a 1-pound clamping force. Potted samples were not used. The chips were sheared by applying a force perpendicularly to one edge of each chip in a plane parallel to the substrate. The shear tester is shown in Figure 19. The force required to shear each chip is shown in Figure 20. The low, high, and average values are listed in Table II.

Table II. Shear Test Results

Clamping Force (pounds)	Shearing Force (grams)		
	Low	Average	High
1	200	291.9	400
1/2	140	234.4	355

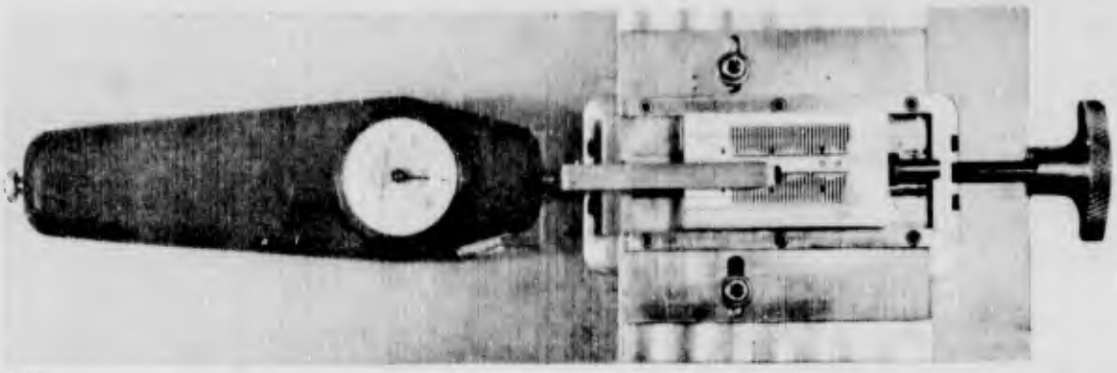


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Figure 19. Shear Tester

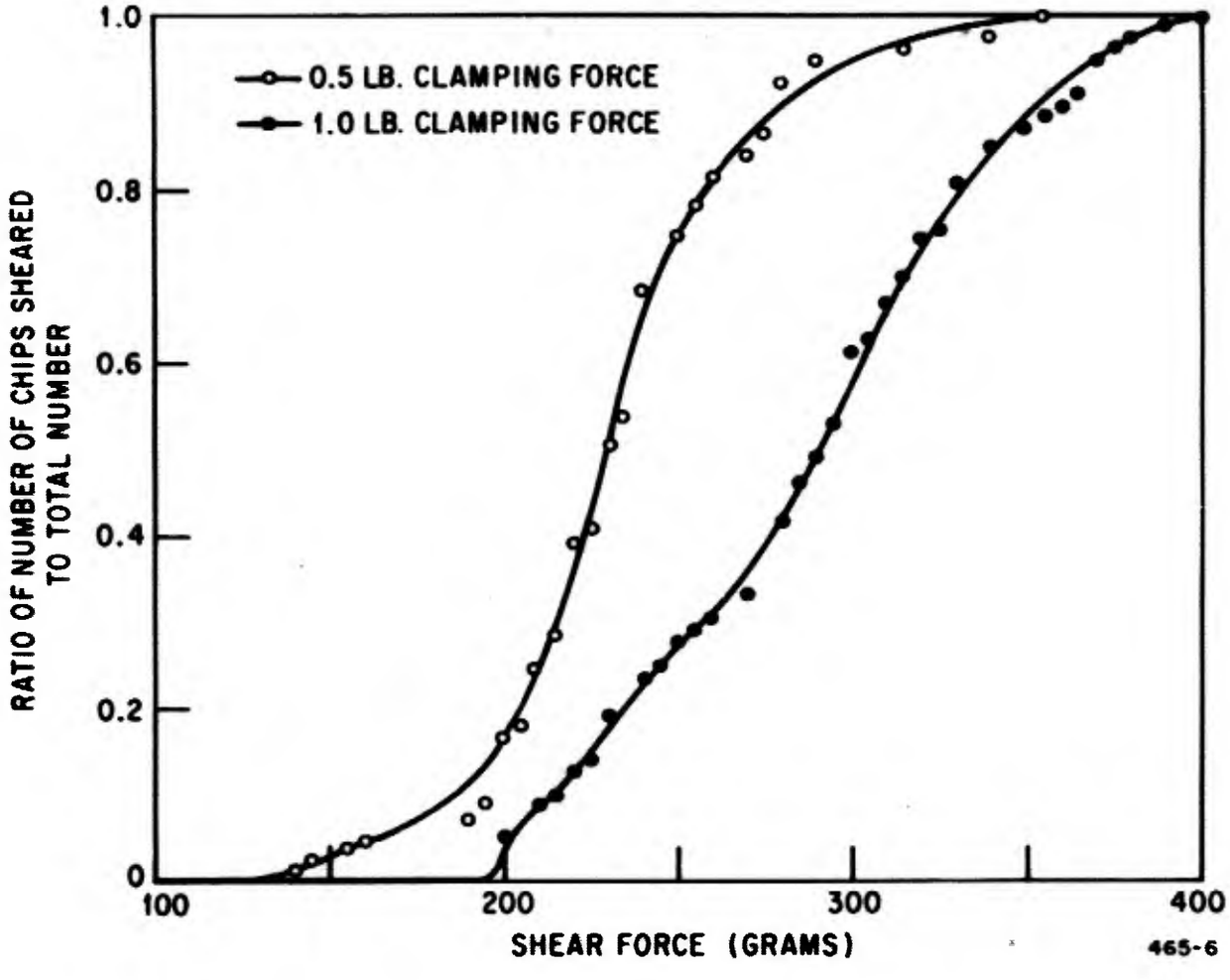


Figure 20. Bond Shear Strength Effect of Clamping Force

The bond strength can be expected to depend on the pedestal diameter and, therefore, on the evaporation number, as shown in Table I. Figures 21 and 22 show the data from Figure 20 plotted with evaporation number as a parameter. There appears to be no correlation between shear strength and pedestal diameter in these data.

b. VIBRATION

Thirty group I, 30 group II, and 31 group III bonded chips were subjected to the vibration test. Paraffin was used to attach the test substrates to aluminum plates mounted on the test equipment. The test equipment is shown in Figure 23, and the aluminum mounting plate and test substrates are shown in Figure 24.

The samples were vibrated over a frequency range of 100 to 2000 cycles per second; the frequency was varied logarithmically with time, and the range was covered in 4 minutes. The minimum peak acceleration was 20 G's. The test was repeated four times along three mutually perpendicular axes. The results of these tests are shown in Table III. All these chips, including those listed as failures, were electrically operable after the test; the failures were due to broken bonds.

Seven failures occurred, all in group I samples. Since these samples are bonded at a 1-pound clamping force, they should have stronger bonds than the group II and group III samples which were bonded at 1/2 pound force. Note, however, that in preparing these samples, six sets of pedestals are prepared simultaneously on a common substrate (Figure 7). Five of the failures in this test occurred on samples from a common substrate. This strongly suggests that the wiring or pedestals on this substrate were defective and that these failures should be attributed to inadequate process control.

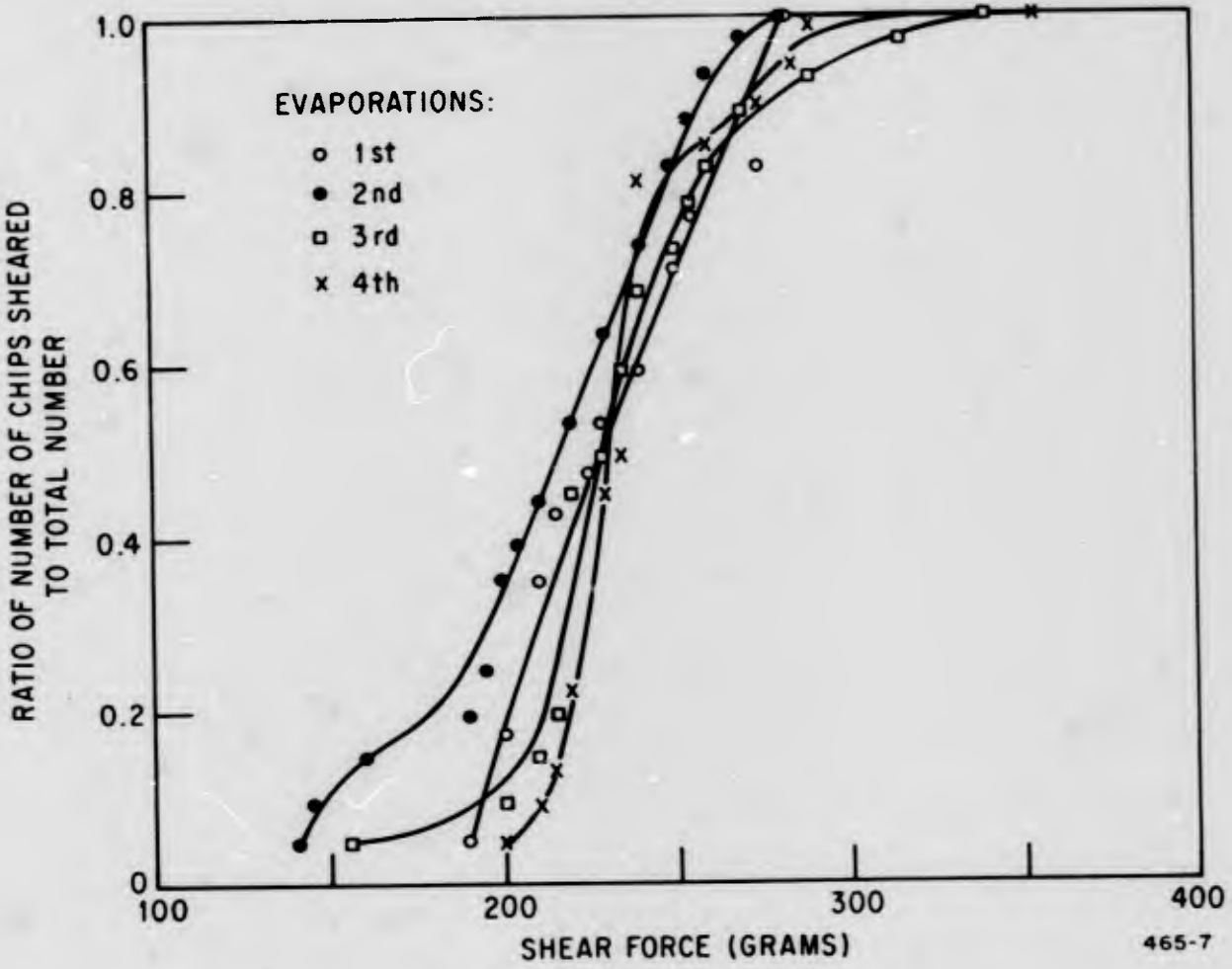


Figure 21. Bond Shear Strength Effect of Pedestal Size (0.5-pound Clamping Force)

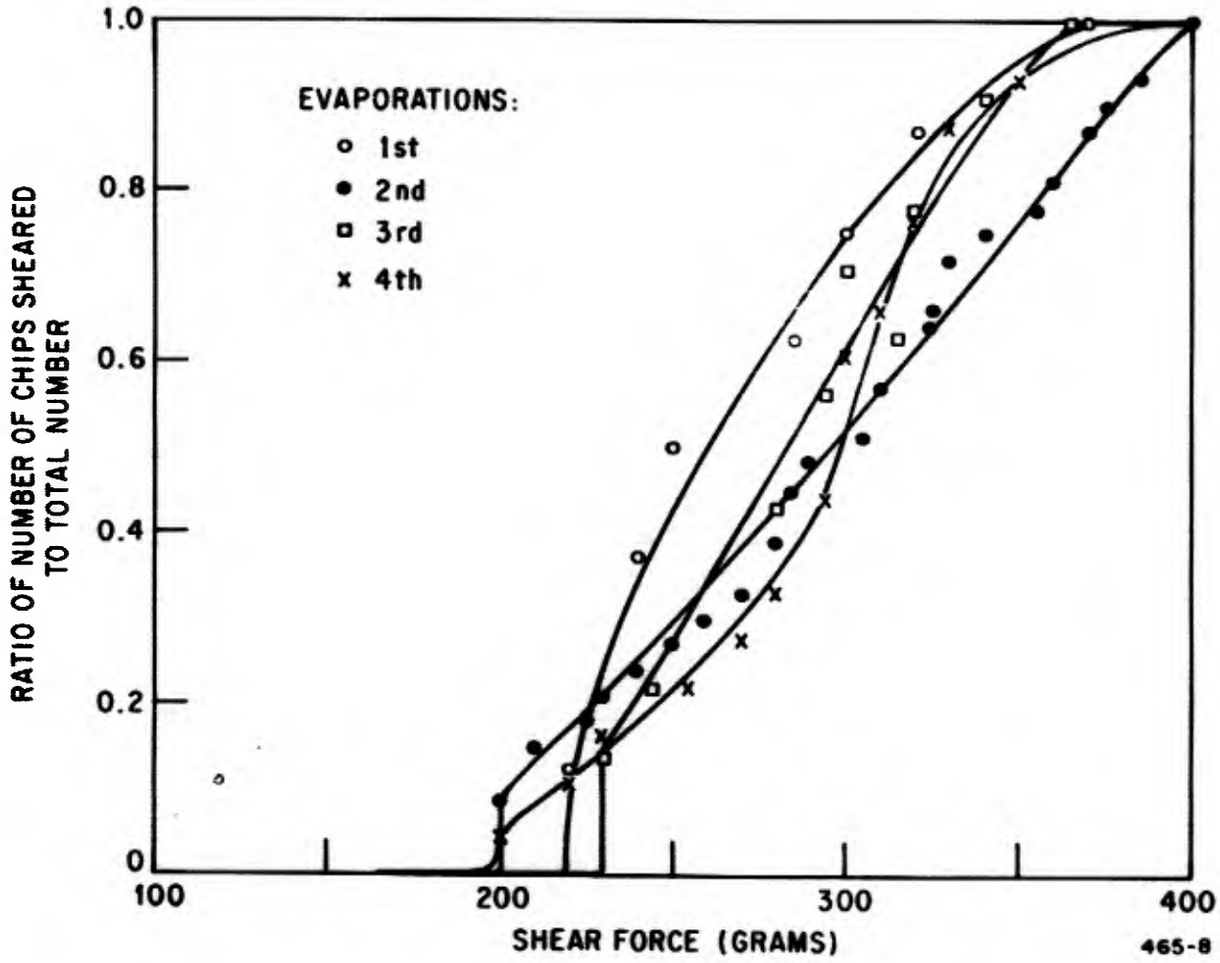


Figure 22. Bond Shear Strength Effect of Pedestal Size (1.0-pound Clamping Force)

Figure 23. Vibration Test Equipment

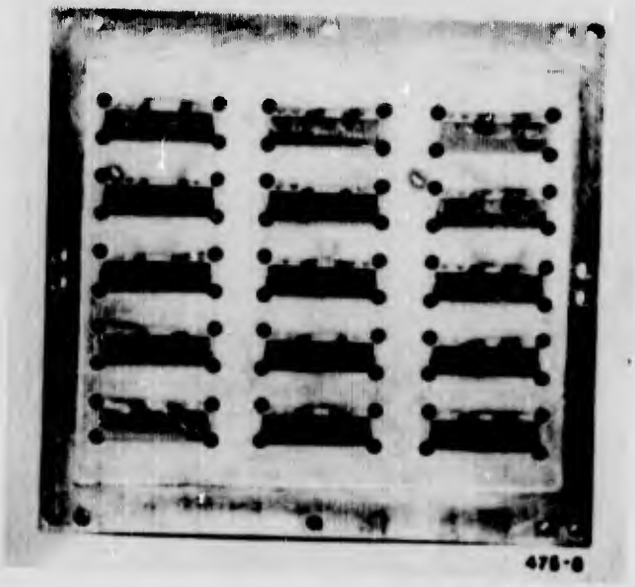


Figure 24. Vibration Test Mounting Plate

Table III. Vibration Test, Ratio of Number of Failures to Number of Samples

*Group	Evaporation Number				Total
	1	2	3	4	
I	0/9	[5]/6	0/6	[2]/9	7/30
II	0/3	0/6	0/12	0/9	0/30
III	0/12	0/10	0/3	0/6	0/31

[] indicates common substrate

c. MECHANICAL SHOCK

Thirty group I, 30 group II, and 30 group III bonded chips were subjected to the mechanical shock test. Paraffin was used to attach the substrates to aluminum plates mounted on the test equipment. The test equipment is shown in Figure 25, and the mounting plate is shown in Figure 26.

Each sample was subjected to five 80-G shocks in three mutually perpendicular directions. The duration of each shock was 4 milliseconds. The samples were then subjected to five 1500-G shocks in three mutually perpendicular directions. The duration of each shock was 0.9 millisecond. The results of these tests are shown in Table IV. All these chips, including those listed as failures, were electrically operable after the test; the failures were due to broken bonds.

Five chips had one lead bond fail, and two chips had several lead bonds fail as a result of this test. Five of these failures were potted chips that had been bonded at a 1/2-pound clamping force (group II). Again the grouping of failures on common substrates suggests the need for improved process control. The failures might also be associated with the

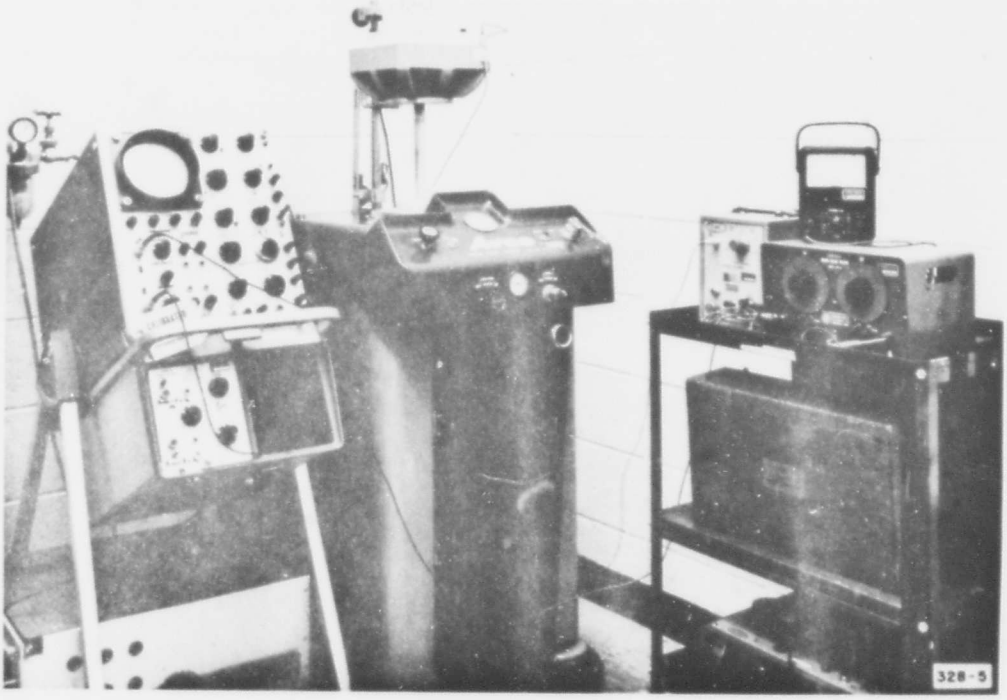


Figure 25. Mechanical Shock Test Equipment

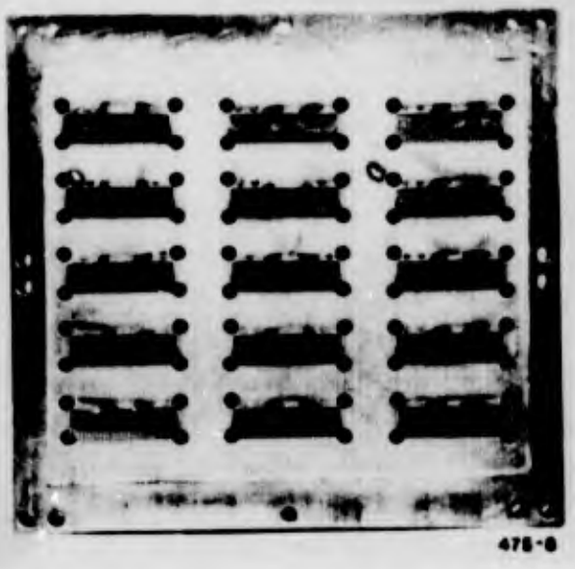


Figure 26. Mechanical Test Mounting Plate

use of the potting compound, since this is the only intended difference between group II and group III samples.

Table IV. Mechanical Shock, Ratio of Number of Failures to Number of Samples

Group	Evaporation Number				Total
	1	2	3	4	
I	0/0	0/9	1/15	0/6	1/30
II	0/0	0/0	[2]/12	[3]/18	5/30
III	0/9	0/6	0/9	1/6	1/30

[ ] indicates common substrate

d. CENTRIFUGAL STRESS

Thirty group I, 30 group II, and 30 group III samples were subjected to the centrifugal-stress test. The test equipment is shown in Figure 27. Paraffin was used to attach the samples to an aluminum plate mounted on the test equipment. The plates were mounted in a horizontal plane, and the samples were subjected to a 20,000-G stress for 1 minute. The results of these tests are shown in Table V.

Table V. Centrifugal Stress, Ratio of Number of Failures to Number of Samples

Group	Evaporation Number				Total
	1	2	3	4	
I	0/3	0/12	1/9	0/16	1/30
II	0/6	0/6	0/6	0/12	0/30
III	0/12	0/6	0/6	0/6	0/30

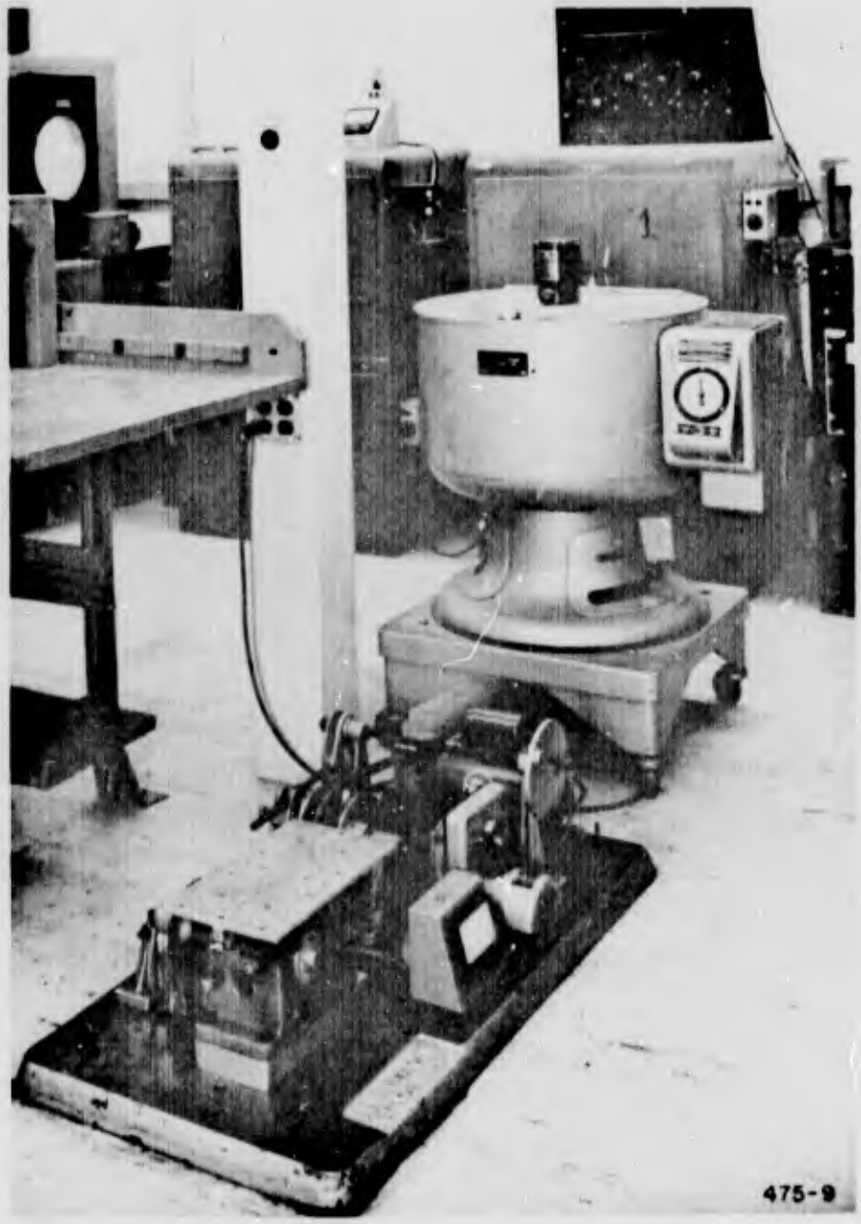


Figure 27. Centrifuge

All these chips, including the one listed as a failure, were electrically operable after the test; the single failure was due to a broken bond.

The plates were remounted in a vertical plane so that the mounted chips faced radially outward, and the test was repeated. Seven glass substrates came off the aluminum baseplate during the test, and the samples were destroyed. Repeated tests were performed on blank substrates in order to determine a suitable mounting arrangement for the vertical plane axis. Several methods were tried for mounting the plates; however, a method that ensured the safety of the plates was not obtainable, so the test was discontinued. The methods tried are shown in Figure 28, along with the damage incurred in the test. These methods included the use of paraffin (Figure 28a) and foam absorbers (Figure 28b). The actual damage is shown in Figure 28c. Note that the chip has remained bonded to its pedestals despite the shattering of the test-plate glass substrate.

e. THERMAL SHOCK

Thirty group I, 30 group II, and 30 group III samples were subjected to the thermal shock test. The test chamber is shown in Figure 29. The samples were placed in a chamber maintained at -55^{o}C for one-half hour, were removed and held at room temperature for 10 minutes, were placed in a chamber maintained at 85^{o}C for one-half hour, and then were removed and held at room temperature for 10 minutes. This cycle was repeated five times. The results of these tests are shown in Table VI. All these chips, including those listed as failures, were electrically operable after the test; the failures were due to broken bonds.

One lead bond failed on each of eight chips, and several lead bonds failed on two chips. Six of the failures were on chips bonded at a

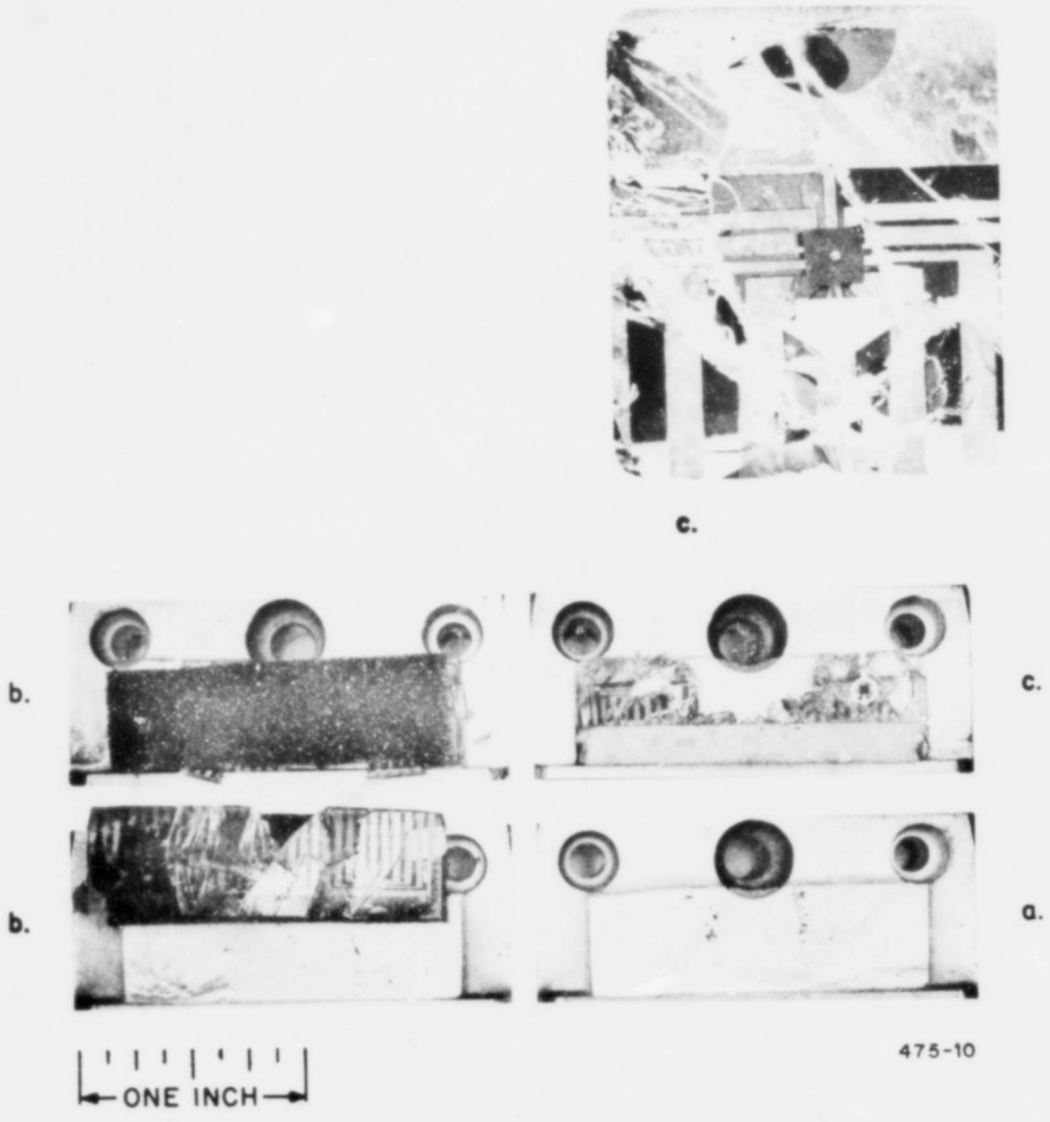


Figure 28. Centrifuge Mounting Fixture and Damage to Test Plates

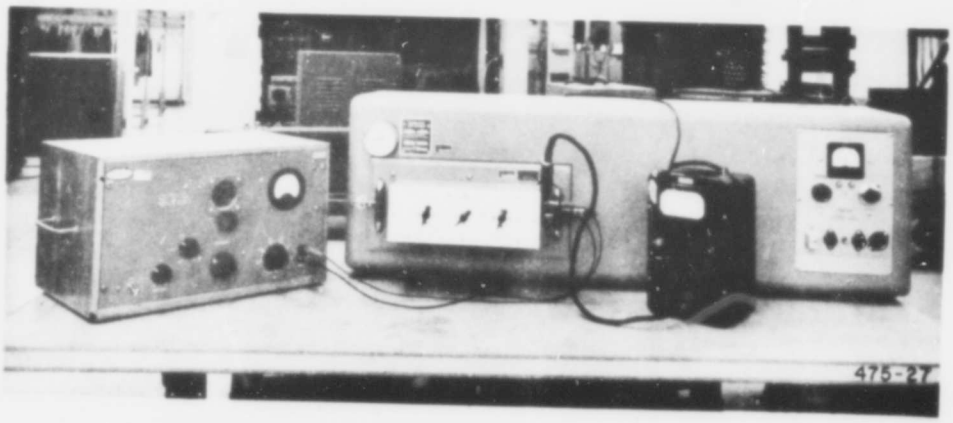


Figure 29. Thermal Shock Test Chamber

1-pound clamping force, then potted (group I); three were on chips bonded at a 1/2-pound clamping force and not potted (group III). Seven of the ten failures occurred on substrates prepared in the third and fourth evaporations.

Table VI. Thermal Shock, Ratio of Number of Failures to Number of Samples

Group	Evaporation Number				Total
	1	2	3	4	
I	1/3 *	1/3	[2]/15	2/9	6/30
II	0/9	0/6	1/9	0/6	1/30
III	1/9	0/9	0/3	2/9	3/30

[] indicates common substrate

The large proportion of failures on substrates prepared in the third and fourth evaporations suggests that bonds to these pedestals are poorer than those to larger pedestals; however, this conclusion is inconsistent with the shear-test data. Also, the reason why most of the failures occurred on the group I samples which were bonded with a stronger force is not known. These inconsistencies suggest inadequate process control.

The anticipated cause of failure in this test was bond failure due to the differential expansion of the substrate and the silicon chip. This may have occurred, even though the 7059 glass was chosen specifically to match thermal coefficients.

f. TEMPERATURE AND HUMIDITY

A total of 247 bonded chips were used in this test. These included 30 group I, 30 group II, and 30 group III chips prepared specifically for this test and 157 of the chips which survived the tests described under headings IV-1b through e. The samples were exposed to a 100°C, 95-percent-relative-humidity ambient for 20 hours and then to the

normal laboratory ambient for 4 hours. The test was carried out for a period of 40 weeks. Functional tests were made on the samples at the end of the 1st, 3rd, and 10th cycles, and then monthly thereafter for the remainder of the period. The test chamber is shown in Figure 30.

The results of this test are shown in Table VII.

Table VII. Temperature and Humidity,Ratio of Number of Failures to Number of Samples

Group	Evaporation Number				Total
	1	2	3	4	
I	10/20	3/13	12/24	7/14	32/71
II	1/15	3/18	3/26	5/27	12/86
III	4/29	3/25	5/15	3/21	15/90
Totals	15/64	9/56	20/65	15/62	59/247

Table VIII, which presents the ratio of failures to samples according to the history of the samples, is a further breakdown of the failure data in Table VII. Note that 32 of the total failures were from the group I samples (1-pound clamping force, potted) and that 16 of these were from the samples which had not undergone any previous environmental tests. Of these 16 failures, 13 occurred on only 3 substrates, suggesting defective substrate wiring. Consequently, these failures may be attributed to inadequate control.

The aluminum substrate wiring was severely corroded in this test, as shown in Figure 31, which shows photographs of actual failures. Even the potted units were damaged. The aluminum metalization on the chips was appreciably corroded; corrosion was observed in the pad areas as shown in Figure 32.

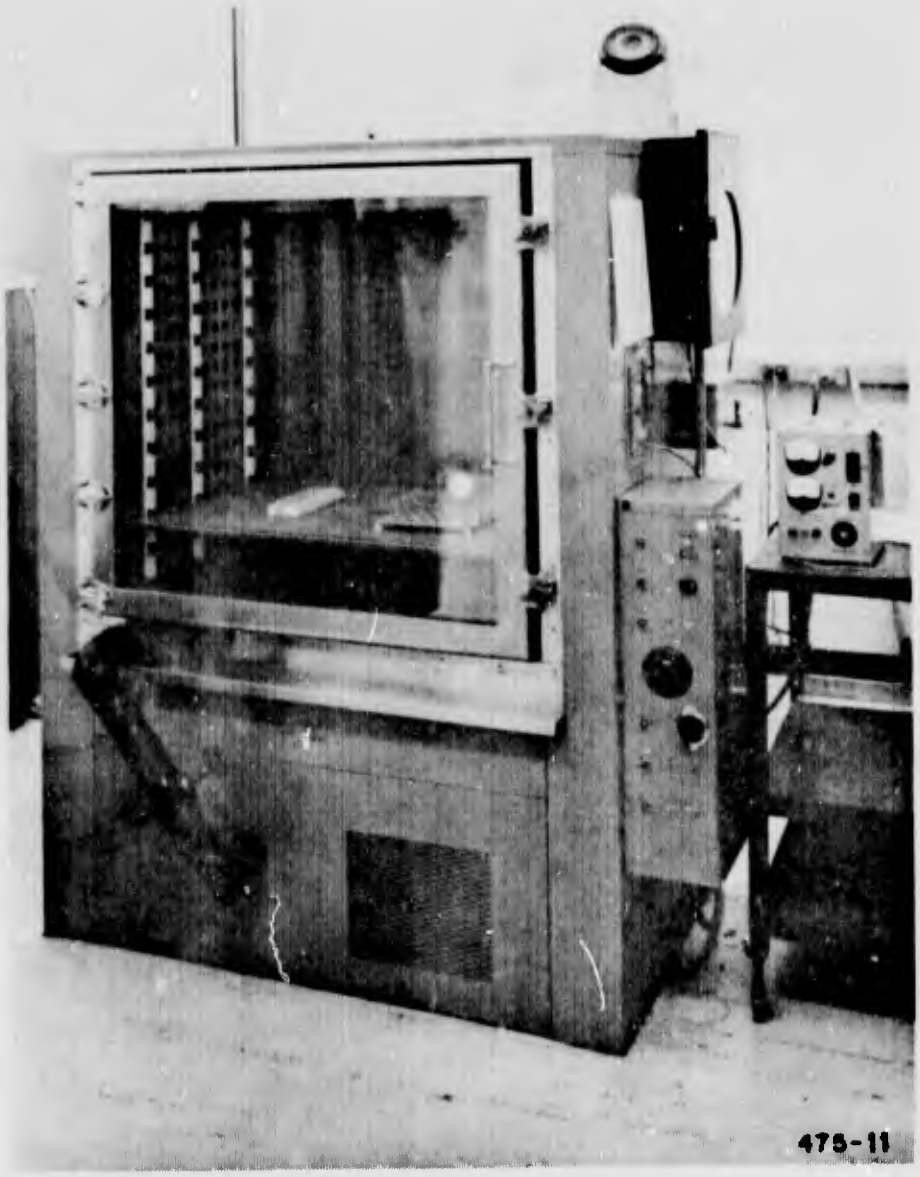


Figure 30. Temperature and Humidity Test Chamber

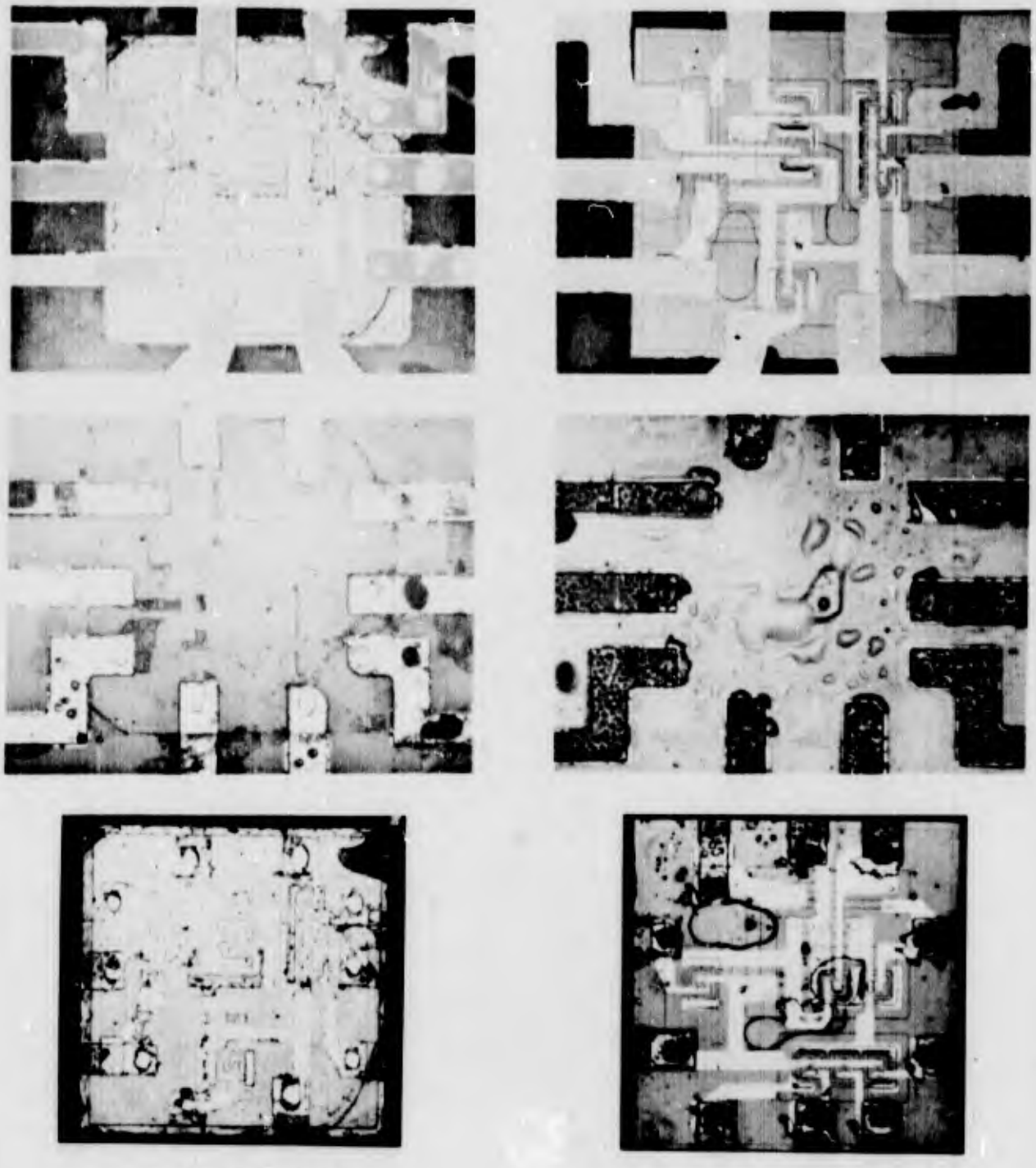
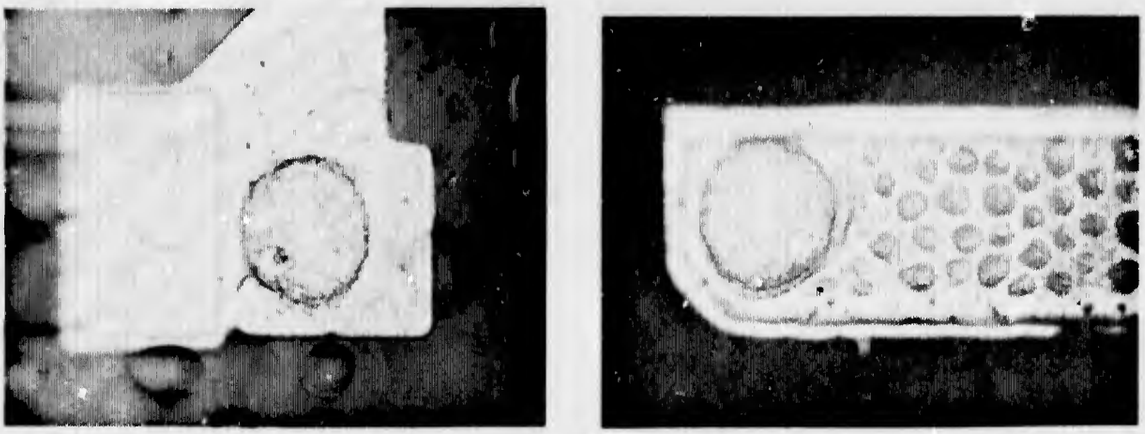


Figure 31. Temperature and Humidity Failures Showing Corrosion



a. Substrate Wiring Corrosion

b. Chip Pad Area Corrosion

475-13

Figure 32. Photographs Showing Corrosion of Evaporated Lines and Chip Pad Areas

Table VIII. Temperature and Humidity, Ratio of Number of Failures to Number of Samples, Showing Previous Chip Tests

Previous Test	Group	Evaporation Number				Total
		1	2	3	4	
(none)	I	(5)1/9	(2)/9	(3)/16	(5)/6	16/30
	II	0/6	0/9	0/6	1/9	1/30
	III	0/6	1/6	0/6	0/12	1/30
Vibration	I	1/6	1/1	0/0	0/3	2/10
	II	0/3	0/3	0/6	(2)/3	2/15
	III	0/6	0/4	1/3	0/3	1/16
Mechanical Shock	I	1/0	0/3	(2)(2)1/8	0/2	5/13
	II	0/0	0/0	1/6	1/6	2/12
	III	0/6	0/3	(3)/3	(3)/3	6/15
Centrifugal Stress	I	(2)/3	0/0	0/3	0/0	2/6
	II	0/3	0/3	0/3	1/6	1/15
	III	(2)/6	0/6	0/0	0/3	2/15
Thermal Shock	I	1/2	0/0	(3)1/7	(2)/3	7/12
	II	1/3	(3)/3	(2)/5	0/3	6/14
	III	(2)/5	(2)/6	1/3	0/0	5/14
Totals		15/64	9/56	20/65	15/62	59/247

( ) Indicates common substrate

A thorough examination of the failures was made. It was obvious that a major cause of failure was the corrosion of the aluminum on the substrates, although some failures were attributed to the corrosion of the metalization on the chip in the pad area. Samples were chosen from each failure group, cleaned, and then rebonded to new substrates. These samples tested functionally good, indicating no chip damage due to the bonding process.

The observed corrosion may be due to the formation of chromium-aluminum electrolytic cells, to the presence of organic contaminants, or to large numbers of pinholes in the aluminum. It was evident that when there was misalignment of the chromium and aluminum in the evaporation the wiring was severely corroded. The misalignment allowed the chromium to be

exposed (usually covered by the aluminum) and this could result in the formation of the chromium-aluminum cell mentioned above.

The corrosion only occurs when the sample is exposed both to high temperature and to high humidity. The substrate wiring did not corrode in the high-temperature storage test, and substrate wiring deposited under similar conditions has shown no signs of corrosion after exposure to 100-percent relative humidity at normal room temperature.

The test results clearly indicate that some method must be devised to prevent the substrate interconnect wiring from corroding. The corrosion of the metalization on the chip pad areas could have been induced by the substrate wiring corrosion. It was evident that the glass passivation prevented corrosion of the circuit metalization.

2. LIFE TESTS

Sets of 30 or more samples from each group were subjected to high-temperature storage, step-stress and comparison, and elevated-temperature back-bias tests. These tests and their results are described in the remainder of this section.

a. HIGH-TEMPERATURE STORAGE

Thirty group I, 30 group II, and 30 group III bonded chips were stored at 150°C for 1000 hours. All the samples were operable after this test, and no bond failures occurred. The test chamber used for this test is shown in Figure 33.

b. STEP-STRESS AND COMPARISON

Sixty group I, 60 group II, and 60 group III bonded chips were subjected to this test. The samples were operated at 100 percent of rated power (35 milliwatts) for 25 hours. Functional tests were then made on the samples. The power was then increased in 50-milliwatt steps. The time

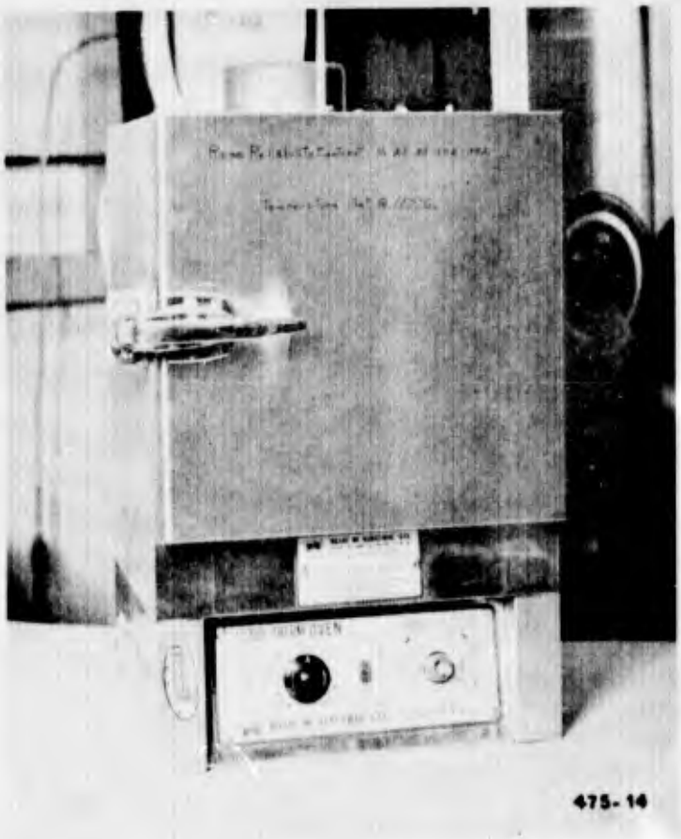


Figure 33. High-Temperature Storage Chamber

duration for each step was 25 hours. Functional tests were made on each sample after every step. The steps were continued until 50 percent of the samples failed. The step-stress and functional testing equipment used in this test is shown in Figure 34. Samples were inserted in 30-pin connectors mounted on a printed circuit board which contained the external load resistors necessary for the power steps. Sixty printed circuit cards, each containing three samples, were mounted in the test rack. For testing purposes, at the end of each step the cards were removed and inserted into the functional tester, where the testing was performed. The basic schematic for the power-dissipation step-stress test is shown in Figure 35.

The data obtained from this test is summarized in Table IX. Sixteen steps were required to obtain 50-percent failures of the 180 samples subjected to this test. The failures were spread rather evenly in the three groups, as shown in Table IX.

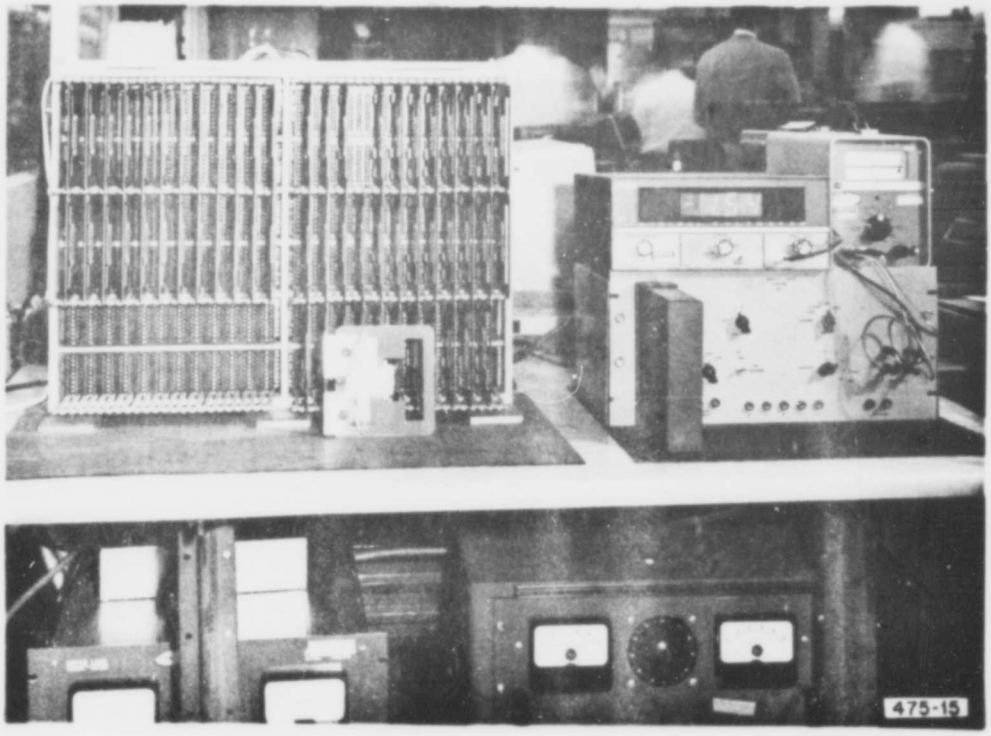


Figure 34. Step-Stress and Comparison Test Equipment

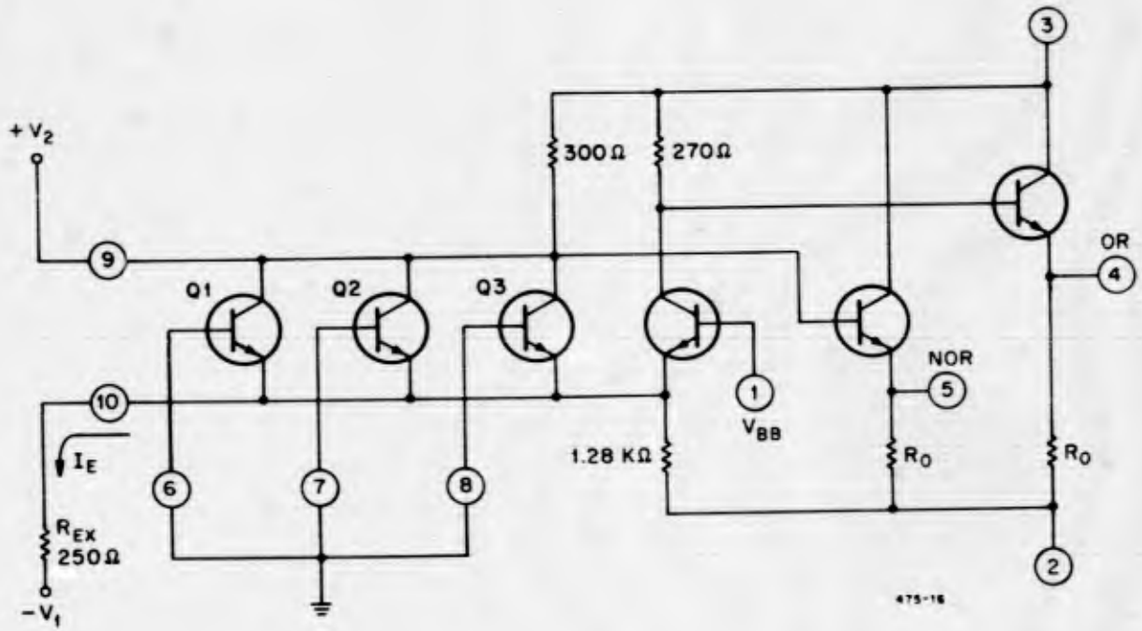


Figure 35. Basic Schematic of Step-Stress and Comparison Test

Table IX. Step-Stress and Comparison Failure Distribution in 180 Samples

Step	Milliwatt Level	Total Failures	Failures by Group		
			I	II	III
1	35	5	1	3	1
2	85	4	2	0	2
3	135	1	0	0	1
4	185	15	2	12*	1
5	235	2	2	0	0
6	285	0	0	0	0
7	335	7	2	0	5
8	385	6	2	1	3
9	435	6	2	2	2
10	485	10	3	1	6
11	535	6	0	1	5
12	585	6	1	4	1
13	635	5	1	3	1
14	685	4	2	0	2
15	735	11	8	0	3
16	785	18	9	2	7
Totals		106	37	29	40

*Unusually high number of failures is discussed in text.

On examination of the 106 failures, the following modes were noted:

Reason of Failure	Number of Failures
Pin No. 9 open only	56
Pin No. 3 open only	6
Pin No. 9 open plus one bond failure	35
Multiple bond failures	9

Under high magnification all the failures that showed an open pin No. 9 were of the same nature. The metalization on the chip which connects the pad associated with pin No. 9 to the rest of the chip circuitry is a very thin line, and the failure occurred on the chip, as shown in Figure 36.

As shown in the schematic of the test circuit, Figure 35, the three input transistors, Q_1, Q_2, and Q_3, of the current-mode logic circuit under test are connected in parallel. The emitters are connected and the collectors are connected by metalization on the chip; it was necessary to connect the bases (terminals 6, 7, and 8) externally. The cluster of parallel transistors is operated in the grounded-base configuration with the collectors returned to a positive supply voltage, V_2, and the emitters returned through a resistor, R_{ex}, to a negative supply voltage, V_1. The emitter voltage is about 0.8 volt and is essentially constant for varying levels of emitter current. Thus the collector-emitter voltage is

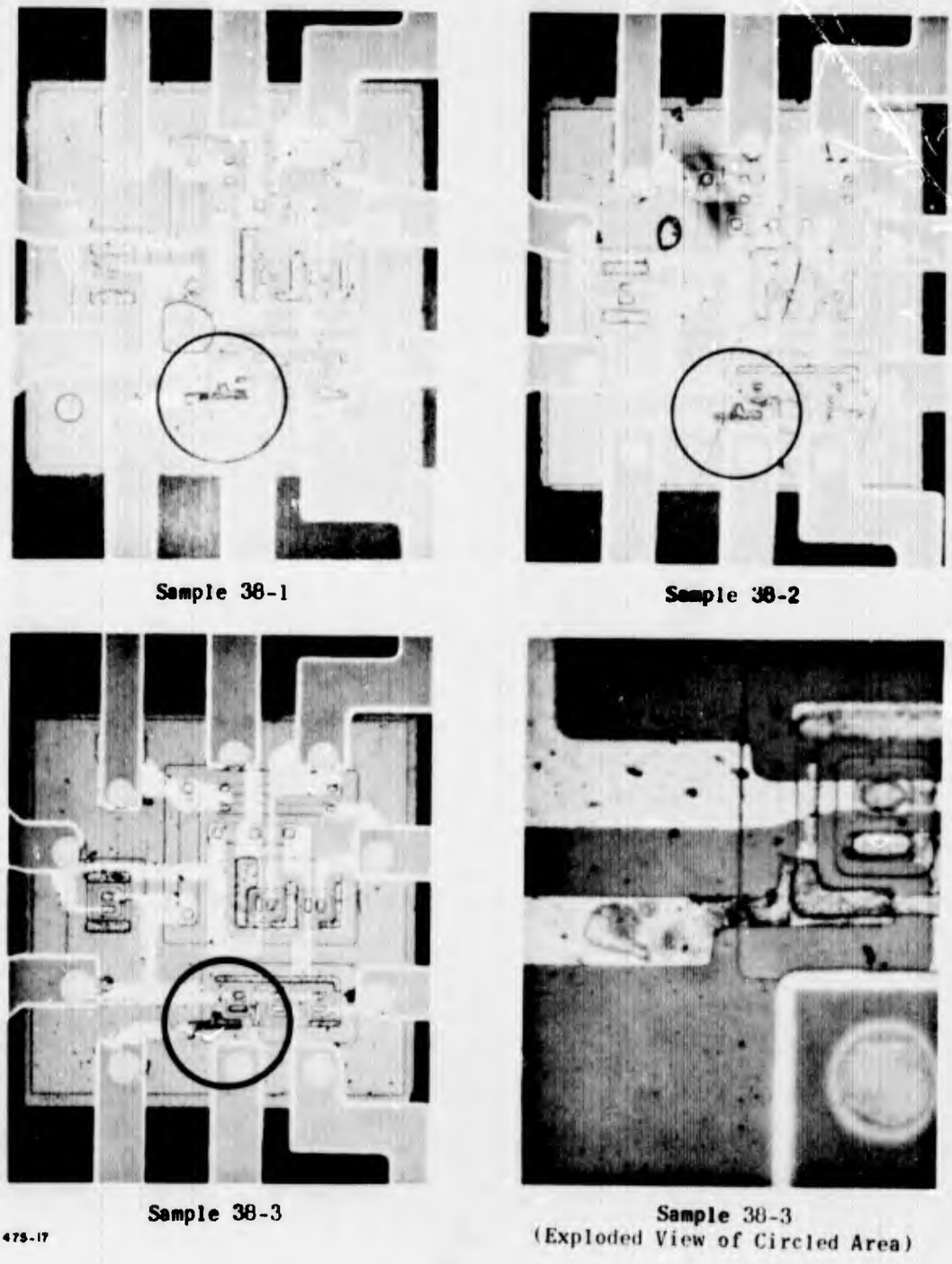


Figure 36. Photographs Showing Metalization Failure on Chip

$V_{ce} = V_2 + 0.8$. The emitter current is determined by the supply voltage, V_1, and the resistor, R_{ex}:

$$I_e = \frac{V_1 - 0.8}{R_{ex}}$$

The power dissipated is:

$$P = I_e(V_2 - V_1) = \frac{(V_2 - V_1)\ (V_1 - 0.8)}{R_{ex}}$$

The power level was controlled by adjusting V_1.

Because of the nature of the power dissipation circuitry, it was necessary to use pin No. 9 in a manner which is uncommon to the general use of this type of chip. The metalization on the chip was not meant to handle the load that this test put on it, and, therefore, it was very prone to failure.

From Table IX, it can be seen that 15 failures occurred at the 4th step (185 milliwatt level). On inspection of the samples and printed circuit cards, it was found that the external resistors associated with 10 of these samples were 50 ohms instead of the required 250 ohms. Consequently, the 10 samples failed sooner than they would have under normal loads. The samples involved are described in the following summary:

Level of Actual Failure	Level of Projected Failure	Samples	Reason Failed
85 mw	435 mw	1	Pin No. 9 metalization open
185 mw	926 mw	9	Pin No. 9 metalization open

As shown in the preceding summary, one sample with a 50-ohm load resistor failed at the 85-milliwatt level and nine samples with a 50-ohm load

resistor failed at the 185-milliwatt level. All these samples failed because the chip metalization opened at pin No. 9. The projected failure levels, computed by approximating a 250-ohm load, are given in the summary.

c. ELEVATED TEMPERATURE AND BACK-BIAS

A total of 244 bonded chips were used in this test. These included 30 group I, 30 group II, and 30 group III chips prepared specifically for this test, and 154 chips which survived the tests described under headings IV-1b through e. Maximum rated bias voltage was applied to the transistor collector and emitter junction of these chips while the chips were stored in a chamber maintained at a temperature of 125°C. The test chamber and automatic tester used for this test are shown in Figure 37. Samples, three on each test plate, were inserted in 30-pin printed circuit connectors which were mounted on printed circuit card racks in the test chamber. Insulated wires were brought out through the chamber and connected to the automatic tester. High-temperature solder was used to connect them to the printed circuit boards within the chamber. High-temperature tests were run on the standard 30-pin connectors. It was found that after an extended period of time at elevated temperatures, the body of the connector expanded and tension was relieved on the contacts, causing open circuits in the substrate-to-pin connection. An example of this expansion is shown in Figure 38.

To alleviate this problem, special connectors were used in the test chamber which were specified to withstand the conditions involved in the extended test.

The samples were tested at 24-hour intervals during the initial burn-in period, and weekly thereafter. The automatic chip tester was built for performing functional tests on the chips in the temperature chamber. The chips were automatically disconnected from the back-bias test and were

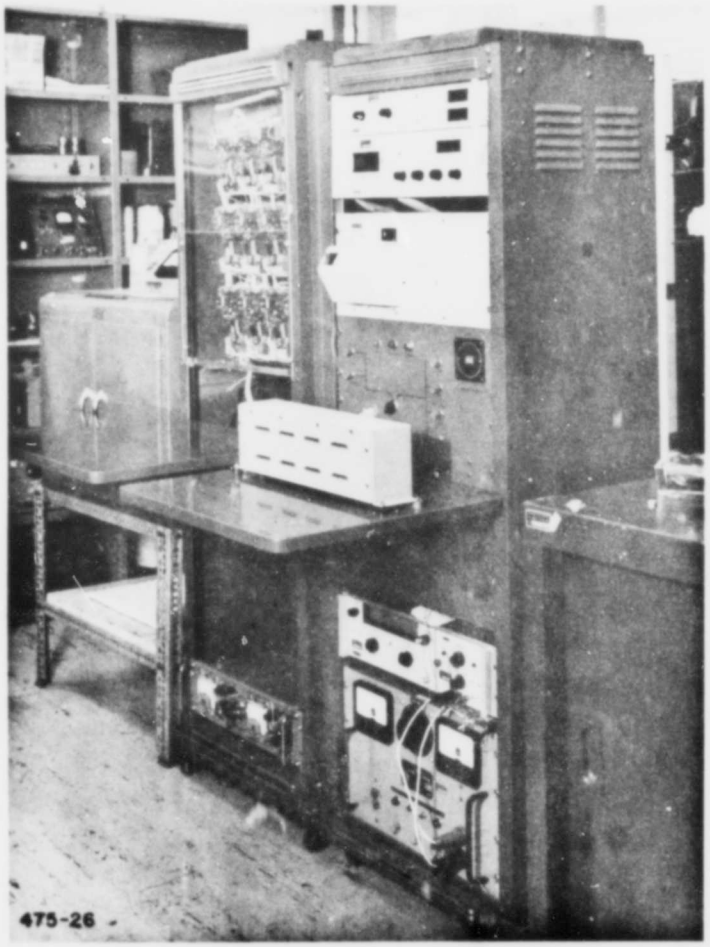
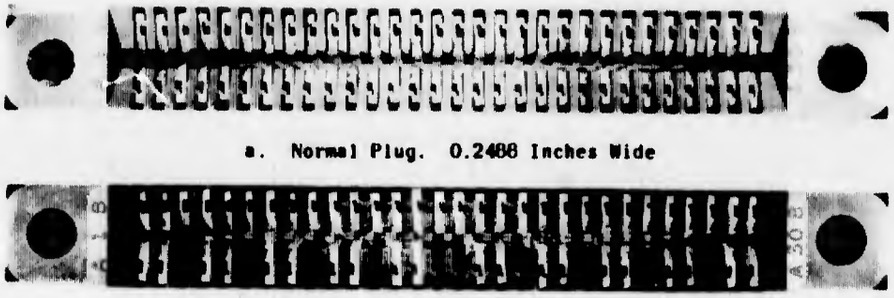


Figure 37. Elevated Temperature Back-Bias Test Chamber and Automatic Tester



a. Normal Plug. 0.2488 Inches Wide

b. Exposed at 150°C 72 Hours Showing Effect of Elevated Temperature. 0.2565 Inches Wide

475-19

Figure 38. Photograph Showing Damage to Standard Connector at Elevated Temperature

connected, one at a time, to a functional test circuit. Ten measurements were performed on each chip, limit comparisons were made to detect failures, and the data was printed on tape. Table X is a summarization of the data obtained from the 40-week test period.

Table X. Elevated-Temperature and Back-Bias Test Ratio of Number of Failures to Number of Samples

Group	Evaporation Number				Total
	1	2	3	4	
I	4/12	3/14	3/23	7/22	17/71
II	2/18	1/18	6/22	10/29	19/87
III	2/19	2/18	4/24	4/25	12/86
Totals	8/49	6/50	13/69	21/76	48/244

The failure data in Table X is further broken down in Table XI, which presents the ratio of failures to samples according to the history of the samples.

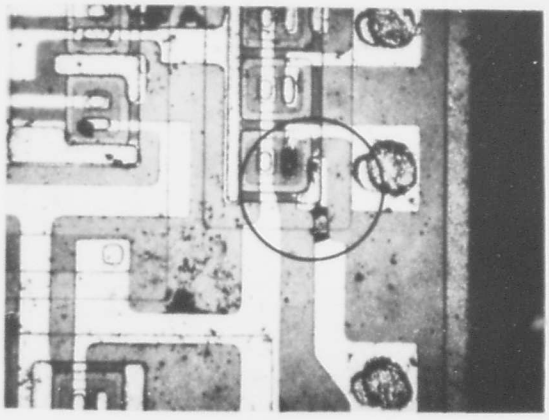
Table XI. Elevated Temperature and Back-Bias Test Ratio of Number of Failures to Number of Samples, Showing Previous Chip Tests

Previous Test	Group	Evaporation Number				Total
		1	2	3	4	
(none)	I	4/9	0/6	1/6	3/9	8/30
	II	1/9	0/9	1/6	2/6	4/30
	III	0/3	1/6	3/12	2/9	6/30
Vibration	I	0/3	0/0	1/5	1/3	2/11
	II	0/0	0/3	0/6	0/6	0/15
	III	0/6	1/6	0/0	1/3	2/15
Mechanical Shock	I	0/0	1/6	0/6	0/3	1/15
	II	0/0	0/0	1/4	0/8	1/12
	III	1/3	0/3	0/6	0/3	1/15
Centrifugal Stress	I	0/0	0/0	0/0	2/3	2/3
	II	1/3	0/3	2/3	5/6	8/15
	III	1/4	0/0	1/6	1/3	3/13
Thermal Shock	I	0/0	2/2	1/6	1/4	4/12
	II	0/6	1/3	2/3	3/3	6/15
	III	0/3	0/3	0/0	0/7	0/13
Totals		8/49	6/50	13/69	21/76	48/244

At the conclusion of the test period, the samples were tested individually in the functional tester. Forty-eight failures occurred in this test. Failures were examined under high magnification to determine the failure mode. Eight failures were associated with open bonds, two with poor substrate evaporation, and one was a catastrophic failure. The remaining failures, the predominant mode, were in the area of the three input transistors on the chip, as shown in Figure 39. Open metalization and high leakage were direct causes of failure. Discoloration of the chip due to local heating was another indication of the ruggedness of this test. The failures are listed and observations of failure modes noted in the following summary:

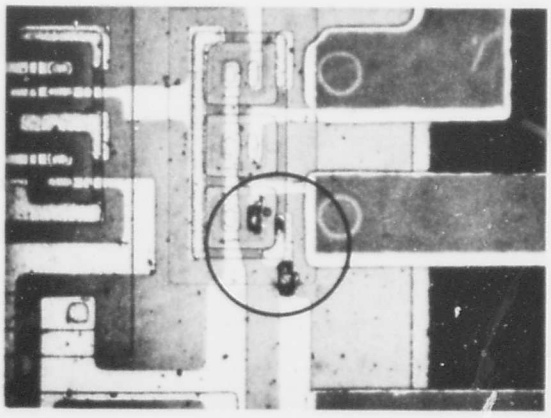
Number of Failures	Mode of Failure
25	Junction breakdown, metalization on chip bad, high leakage, and so forth
8	Chip metalization bad, in the input transistors and other areas
8	Open bonds, plus chip metalization bad
2	Poor substrate evaporation
2	Chip metalization bad, in the areas associated with back-bias
2	Chip metalization bad, in the areas not associated with back-bias
1	Catastrophic, chip burnt and substrate wiring
48	

Table XII gives an individual analysis of the 49 failures.



a. Sample 22-1 Open Metallization on Chip

475-21



b. Sample 35-1 Open Metallization on Chip

Figure 39. Elevated Temperature-Back Bias Test Failures

Table XII. Analysis of Each Failure, Elevated Temperature and Back-Bias Test

Sample Number	Failed at (Number of hours)	Remarks
44	0	Input transistors, metalization on chip bad
28	0	Input transistors, metalization on chip bad
76	0	Chip metalization bad, near pins 4, 5, and 7
175	0	Poor substrate evaporation
198	0	Open bonds, plus bad chip metalization
241	0	Chip metalization bad, near pin 1 and 8
2	24	Input transistors, metalization on chip bad
9	24	Input transistor, emitter-base short
72	24	Chip metalization bad, near pin 1
203	24	Open bonds, plus bad chip metalization
58	48	Input transistors, metalization on chip bad
232	312	Input transistors, metalization on chip bad
227	336	Chip metalization bad, near pins 1 and 8
223	480	Chip metalization bad, near pins 4 and 8
229	480	Input transistors, metalization on chip bad
224	584	Input transistors, metalization on chip bad
194	672	Open bonds, plus bad chip metalization
236	1008	Input transistor, high leakage
244	1176	Input transistors, metalization on chip bad
225	1344	Input transistors, metalization on chip bad
42	1680	Input transistor, high leakage
1	1848	Input transistors, metalization on chip bad
4	1848	Input transistors, metalization on chip bad
64	1848	Chip metalization bad, near pins 3 and 8

Table XII. Analysis of Each Failure, Elevated Temperature and Back-Bias Test (cont)

Sample Number	Failed at (Number of hours)	Remarks
188	2016	Input transistors, metalization on chip bad
246	2016	Input transistors, metalization on chip bad
16	2184	Chip metalization bad, near pins 1, 3, and 5
125	2352	Input transistors, metalization on chip bad
51	2520	Input transistor, high leakage
129	2520	Chip metalization bad, near pins 5 and 8
253	2520	Input transistors, metalization on chip bad
24	2856	Input transistors, metalization on chip bad
85	2856	Input transistors, metalization on chip bad
150	3192	Catastrophic failure, chip shorted and burnt, substrate wiring melted
147	5208	Input transistors, metalization on chip bad
69	5376	Chip metalization bad, near pin 3
226	5376	Input transistors, metalization on chip bad
233	5376	Input transistors, metalization on chip bad
195	5544	Open bonds, plus bad chip metalization
218	5544	Open bonds, plus bad chip metalization
62	6048	Chip metalization bad, near pins 4, 5, and 8
159	6384	Chip metalization bad, near pin 1
219	6384	Open bonds, plus bad chip metalization
92	6552	Poor substrate evaporation, plus metalization bad on chip

Table XII. Analysis of Each Failure, Elevated Temperature and Back-Bias Test (cont)

Sample Number	Failed at (Number of hours)	Remarks
6	6720	Chip metalization bad, near pins 4, 6, and 8
131	6720	Input transistors, metalization on chip bad
196	6720	Open bonds, plus bad chip metalization
197	6720	Open bonds, plus bad chip metalization

Because of the high number of junction breakdowns, channeling at the surface of the chip in the junction regions might be considered as a possible cause of failure. This channeling is known to exist in integrated circuits at extended periods of high temperature and back-bias, especially in uncased units.

The incremental failure rate, calculated from the data, is shown in Figure 40. The dotted line shows the values for the chips that failed, and the solid line shows the incremental failure rate at the 60-percent confidence level that would be obtained from the test if no failures occurred. The incremental failure rate obtained from this test decreases with time and follows the shape of the "no failure" curve rather closely.

The overall failure rate is defined as the number of failures in a given time interval, and was calculated as shown:

$$\text{Failure Rate} = \frac{\text{Number of Failures}}{\text{Total Operating Sample Hours}}$$

Number of Samples Tested 244

Number of Failures 48

Number of Units Completing Test 196

Test Period 6720 hours (40 weeks)

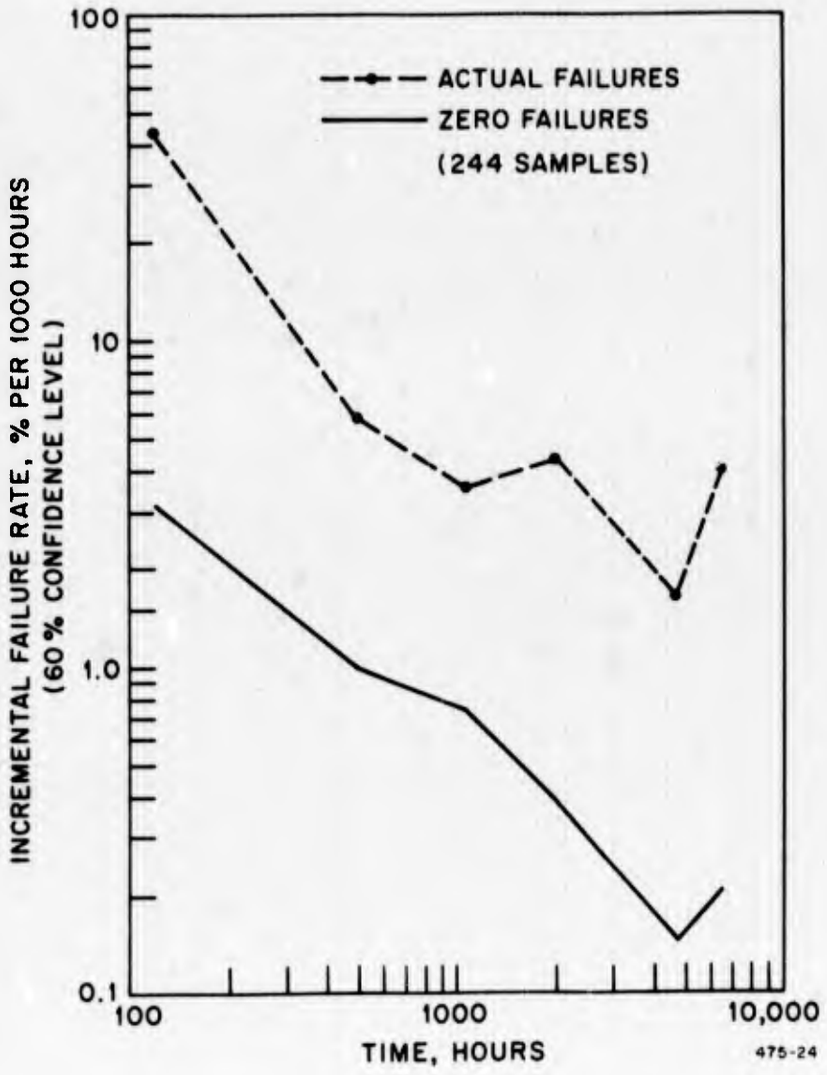


Figure 40. Elevated Temperature Back-Bias Test, Incremental Failure Rate

Total Operating Sample Hours 1,407,656

$$F_R = \frac{48}{1,407,656}$$

$F_R = 3.6 \times 10^{-5}$ 3.6 percent per 1000 hours

The failure rate was approximately 3.6 percent per thousand hours. Motorola reports a 0.082-percent failure rate per thousand hours for canned integrated circuits in normal operation at this temperature.[2] These failure rates cannot be compared directly, since the back-bias test is significantly more stringent. In addition, the samples were not hermetically sealed. The failures in this test appeared distributed with reasonable uniformity among the chips in groups I, II, and III.

The elevated temperature back-bias test was conducted to gather accelerated test data on the behavior of the chip surface. The chips used had a thin glass passivation layer over the surface, except at the bonding-pad locations. Potting the chips (groups I and II) did not provide any additional passivation. It is likely that the high rate of failure is due to the ruggedness of the test and the lack of hermetic sealing of the units, rather than to damage caused by the bonding process.

[2] Motorola Semiconductor Products Inc., Reliability Report on Motorola Monolithic, Digital Integrated Circuits, 1966

SECTION V

CONCLUSIONS AND RECOMMENDATIONS

1. CONCLUSIONS

At the initiation of the program, the main concern was that the face-down-bonding process might damage the chip. The mechanical damage to the back of the chip was obvious; the concern was over the potential damage to the circuit components and surface passivation layer. No damage was detected in the mechanical and thermal tests. The high rate of failure obtained in the elevated-temperature back-bias test was probably due to the rugged test conditions and to the fact that the samples were not hermetically sealed, rather than to damage caused by the bonding process.

The bond failure rate is high. The distribution of failures, Table XIII, indicates that the process controls were inadequate. The bonding process is still in the development stage and subsequent improvements can be expected.

The 1/2-pound-force bond did not have the shear strength of the 1-pound bond, but bonds made at either force withstood the thermal and mechanical tests equally well. This is significant, since the chip replacement feature, obtained when the 1/2-pound bonding force is used, is required to make the bonding process practical.

2. RECOMMENDATIONS

One problem which must be solved is the corrosion of the wiring in high-temperature and high-humidity ambients. Potential solutions include the

TABLE XIII. Overall Distribution of Failures

Test	Group	Failures/Number of Samples				Total
		Evaporation Number				
		1	2	3	4	
Vibration	I	0/9	5/6	0/6	2/9	7/30
	II	0/3	0/6	0/12	0/9	0/30
	III	0/12	0/10	0/3	0/6	0/31
Mechanical shock	I	0/0	0/9	1/15	0/6	1/30
	II	0/0	0/0	2/12	3/18	5/30
	III	0/9	0/6	0/9	1/6	1/30
Thermal shock	I	1/3	1/3	2/15	2/9	6/30
	II	0/9	0/6	1/9	0/6	1/30
	III	1/9	0/9	0/3	2/9	3/30
Centrifugal stress	I	0/3	0/12	1/9	0/6	1/30
	II	0/6	0/6	0/6	0/12	0/30
	III	0/12	0/6	0/6	0/6	0/30
Temperature and humidity	I	10/20	3/13	12/24	7/14	32/71
	II	1/15	3/18	3/26	5/27	12/86
	III	4/29	3/25	5/15	3/21	15/90
High temperature storage	I	0/24	0/6	0/0	0/0	0/30
	II	0/0	0/18	0/6	0/6	0/30
	III	0/0	0/0	0/12	0/18	0/30
Step-Stress	I	6/15	16/21	5/12	10/12	37/60
	II	10/21	13/21	5/15	1/3	29/60
	III	16/21	14/15	8/12	2/3	40/60
Elevated-temperature back-bias	I	4/12	3/14	3/23	7/22	17/71
	II	2/18	1/18	6/22	10/29	19/87
	III	2/19	2/18	4/24	4/25	12/86

overcoating of the substrate wiring with glass (as on the chip), the development of other protective potting materials, or the development of corrosion resistant, conductive alloys. If the main cause of corrosion is the electrolytic cell, elimination of the chromium underlayer may adequately solve the problem. It is apparent that some form of environmental protection, such as encapsulation or hermetic sealing, is required.

The face-down-bonding fabrication technique has many significant advantages, and these test results indicate that there are no unsurmountable problems in achieving a practical and reliable process.

APPENDIX

INTEGRATED CIRCUIT CHIP SAMPLE EXAMINATION

1. GENERAL

Aside from the requirements of this contract, a sample examination was made by the Rome Air Development Center. Thirty-two MC 306 MECL chips, selected at random from the purchased lot prior to testing, were forwarded to RADC for this purpose. Upon completion of the examination of the samples, the chips were returned to the Univac Division and were included in the vibration test. Some of these were also included in the temperature and humidity and elevated-temperature back-bias test.

The RADC sample examination report in its entirety is included in this appendix as follows:

2. ROME AIR DEVELOPMENT CENTER REPORT

a. MC 306, Three-Input Gate

(1) Thirty-two (32) unpackaged Motorola MC 306 three-input gate silicon chips were obtained from the Univac Division of Sperry Rand, Blue Bell, Pennsylvania for examination. This type of chip is used as the test circuit in the RADC sponsored contract AF 30(602)-3921, "Reliability Test Program of Ultrasonic Face Down Bonding Technique." The chip has nominal dimensions of 40 by 40 mils, with ten contact points.

(a) All circuits were submitted to visual inspection at 200X and several circuits were angle-lapped and stained for inspection of internal

circuit structure. Talysurf charts were made to investigate surface profile of the circuits.

(2) Visual inspection produced the following results:

(a) General Cleanliness of the Si Bars:

Two bars were found to be extensively covered with dirt, eight had some accumulation of dirt while the rest had a nominal amount of dirt, to be expected on bars which have been handled repeatedly.

(b) Metalization:

(i) Undercut Interconnect Pattern - none.

(ii) Scratches - all bars had at least several scratch marks across or along the interconnect pattern (see Figure 41, pictures of samples No. 1, 2, 3, 4, 11, 17, and 25), but none seemed to cut the metal lines completely. Twelve (12) bars had large amount of scratches and 2 bars were very badly scratched.

(iii) Voids, Opens, Excess Metal - damage due to scratches was not considered here. One bar had some excess metal left on at various parts of the circuit.

(iv) Other Damage to Metalization Pattern:

A slight mesh pattern was visible over all metalized areas. Possible cause—oxidation of the metal surface.

Nearly all land areas were damaged by probe points.

(c) Mask Registration and Line Resolution:

All diffusion masks were found to be very well aligned. There were some slight inconsequential shifts in metalization patterns. Several bars had somewhat undefined emitter and collector areas.

(d) Wafer Surface Damage:

Two bars showed some slight wafer surface damage under the oxide layer.

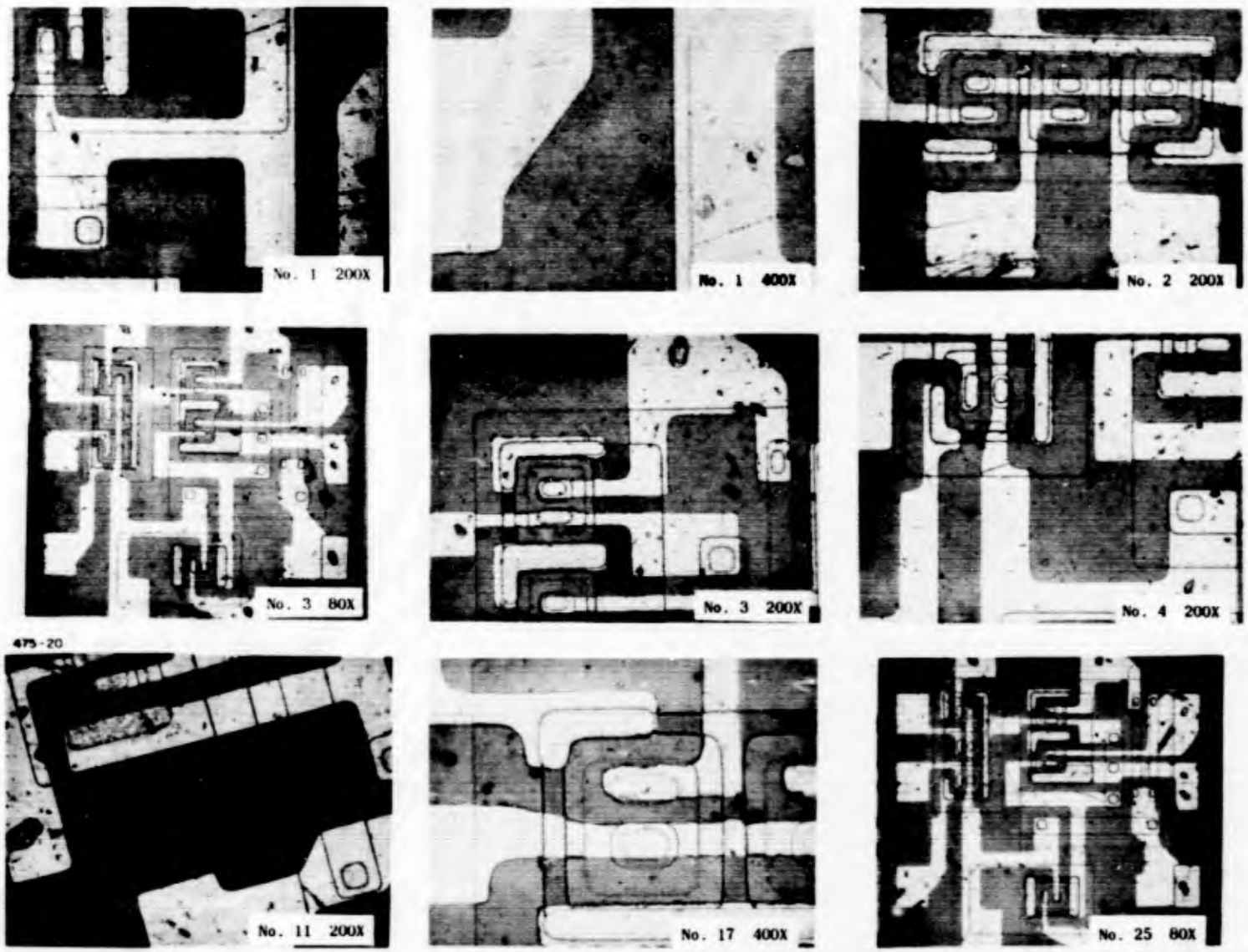
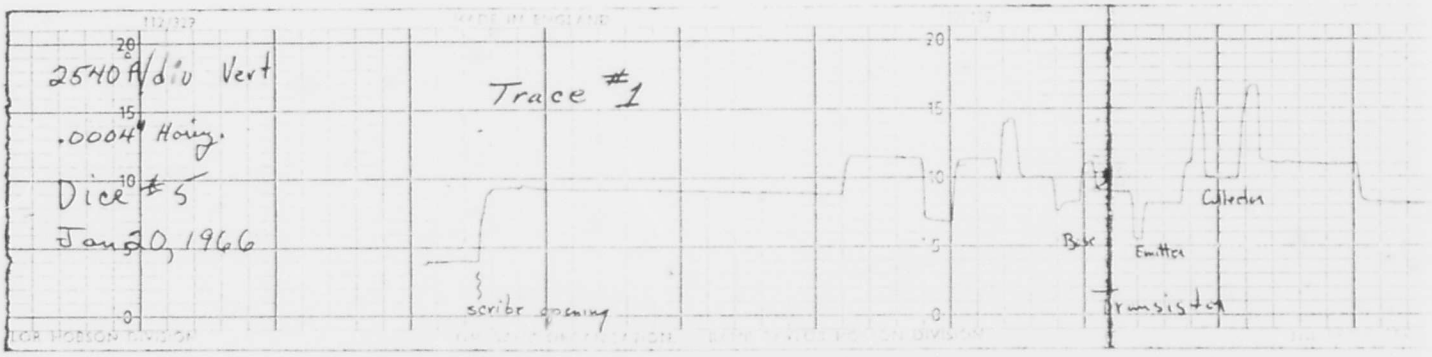


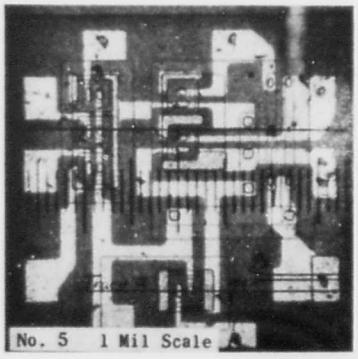
Figure 41. Rome Air Development Center Sample Examination

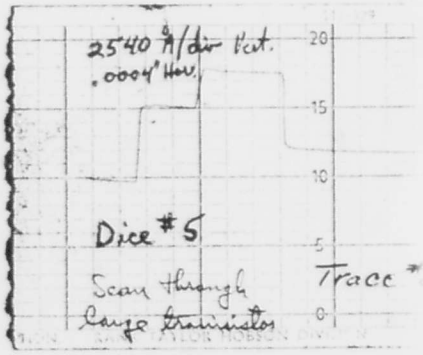
(3) Talysurf profilometer measurements were made of dice No. 5. (See Figure 42). The dice was oriented so that only one input transistor was profiled, in the interest of simplicity. As can be seen in the enlargement, the trace also showed a scratch over the bonding pad. Trace No. 2 depicts a large transistor. Areas of interest are marked on the recording. Aluminum overlap in the contact areas is not unusual. The profile also showed the thin glass passivating layer over the device, as indicated on the trace.

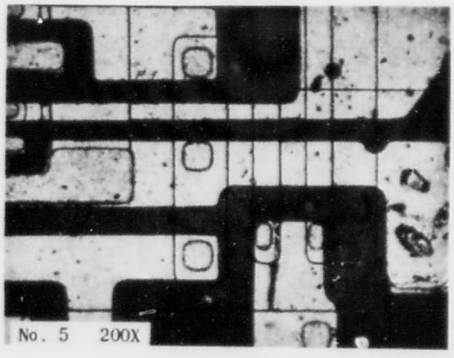
(4) Angle lapping. (See Figure 43.)

Heaviest oxide over nondiffused areas measured up to 16,000 Angstroms (Thallium light, used value of index of refraction ≅1.5). "Island" depth was measured to be in the 15 to 16.5 μ range, but since these depths were measured after prolonged starting cycles during which compensated areas also tend to stain, this depth could very well be larger. Resistor diffusion depth was found to be 2.7 μ, while the base collector junction depth was measured at ~3.0 μ level. Sample No. 31 after stripping of metal and silicon dioxide layers revealed a defect in the substrate at the edge of a resistor. Diffusion in this area as seen on subsequent photo micrographs extended through the device "island" into the substrate.

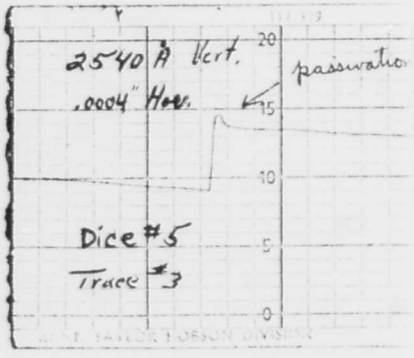








475-23



A

Figure

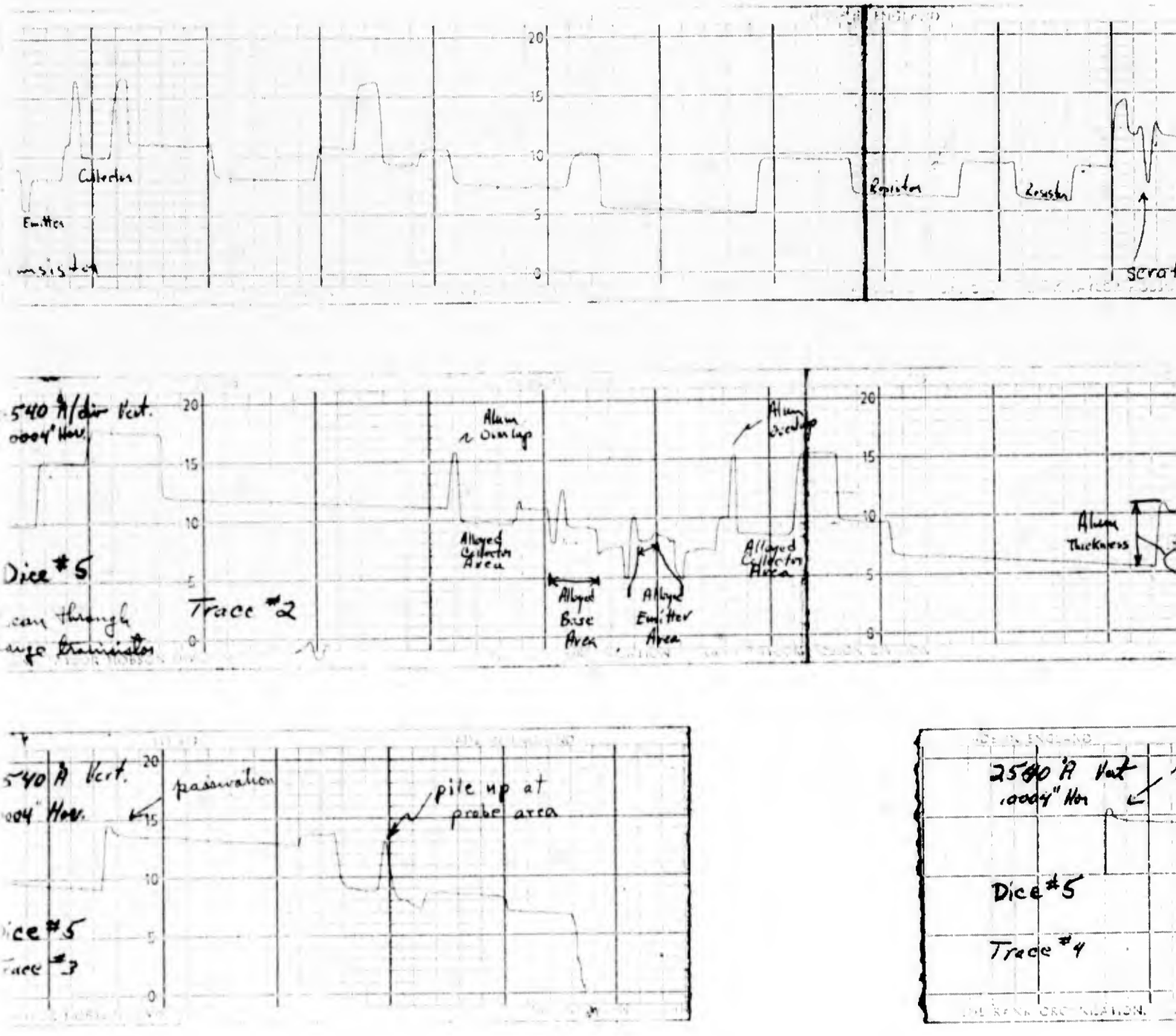
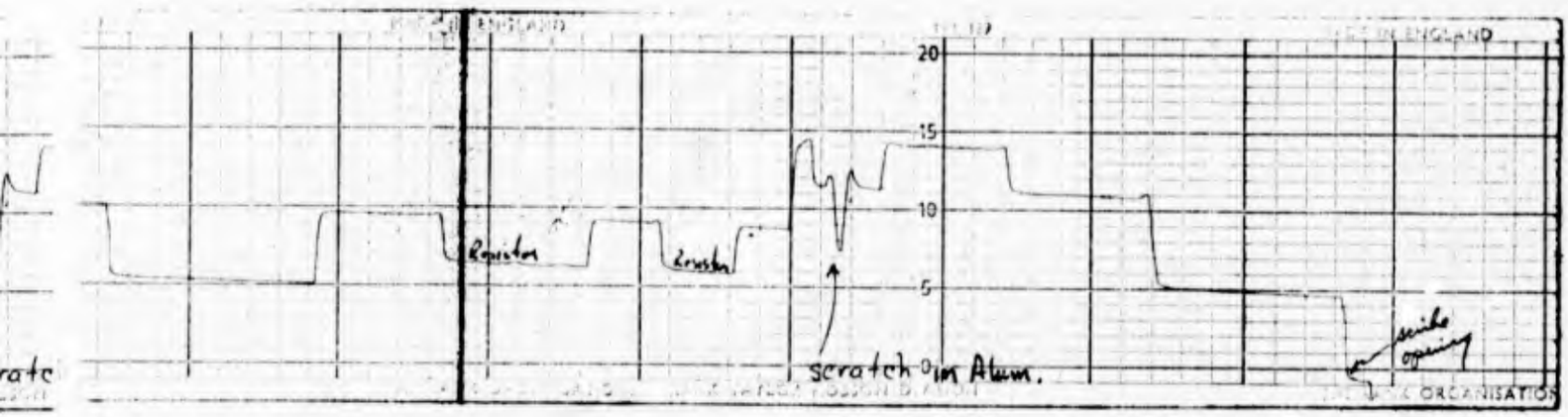
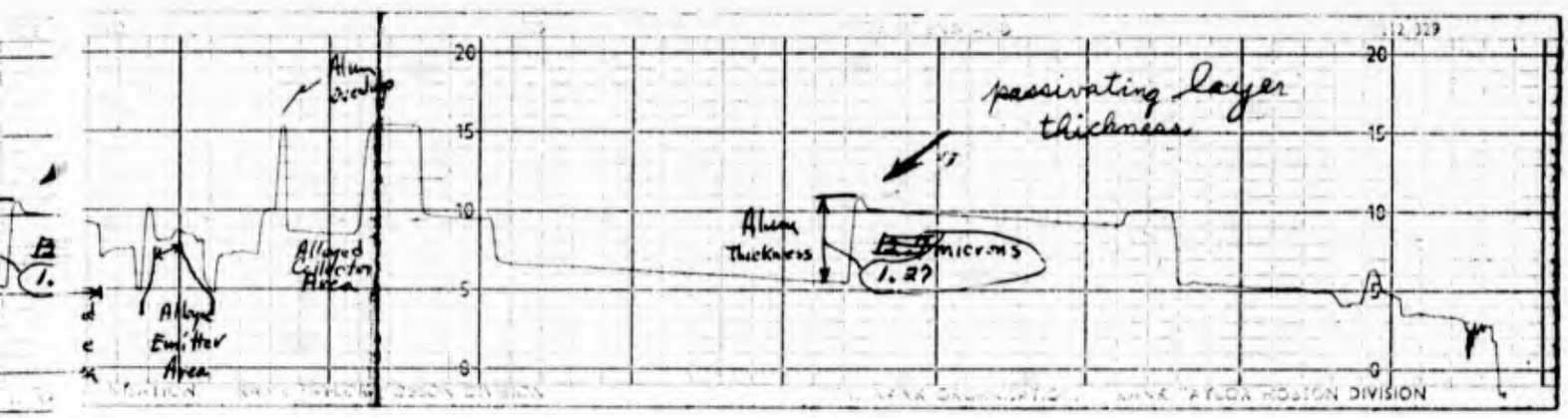
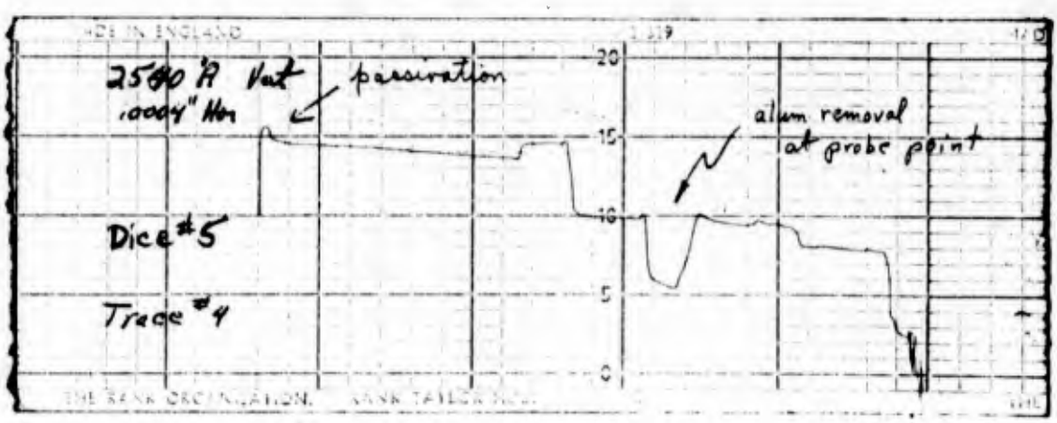


Figure 12. Rome Air Development Center Sample Examination







C

Sample Examination

No. 31 55X

No. 31 130X

No. 31 130X

No. 31 130X

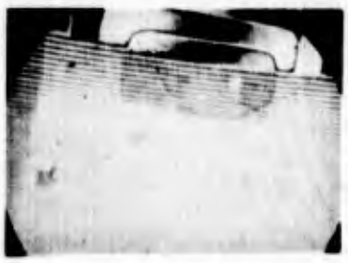
No. 31 130X
Resistor Diffusion Depth
~2.7μ

No. 31 130X
"Island" Depth
~16.5μ

475-22

No. 31 330X
Note Flaw in Resistor
Bar on the Left

No. 31 330X
Max. Oxide Thickness
~16000A



No. 31 330X
Base Diffusion Depth
~3.0μ

Figure 43. Rome Air Development Center Sample Examination

b. Examination after Testing.

(1) Visual inspection at 200X was repeated after the bars were bonded and life tested. This inspection was performed through the bar supporting glass substrate which in one case completely obscured the view of the bar.

The condition of the bar and interconnect pattern surfaces closely followed the grouping of the bars for life test purposes.

(a) Nearly all circuits which were submitted to temperature-humidity life test displayed extensive bar surface, surface protection film, and metallization pattern damage. No uniformity in this respect, however, was observed, as some glass substrates carried bars with very extensive, intermediate and no surface damage (Figure 44, Nos. 26, 27, 28). Ten of the sixteen circuits in this group displayed conditions indicating actual or potential shorting of the interconnect pattern (Figure 44, Nos. 3, 4, 6, 13).

(b) With exception to samples Nos. 19, 30, all circuits in the group which were submitted to temperature-back bias life test displayed very little or no damage to bar and interconnect pattern surfaces. The melted leads on sample No. 30 (Figure 45) were probably caused by the shorting of the bonding pads. The aluminum bridge between emitter and base contacts of the transistor in question was likely caused by the same effect, as the bridge was not present prior to bonding.

(c) Sample No. 19 displayed an extensive damage to the interconnect pattern (Figure 45). Similar damage was also observed on sample No. 1 (Figure 45). The nature and cause of this damage could not be determined by visual inspection.

c. Conclusion

Comparison of the results of the visual inspection before and after bonding except for few scratches within the interconnect pattern of some of the bars (Figure 41, Figure 44 - No. 17) did not reveal any significant damage to the bars which could be attributed to the bonding process (Figure 41, Figure 44 - Nos. 3, 4, 25).

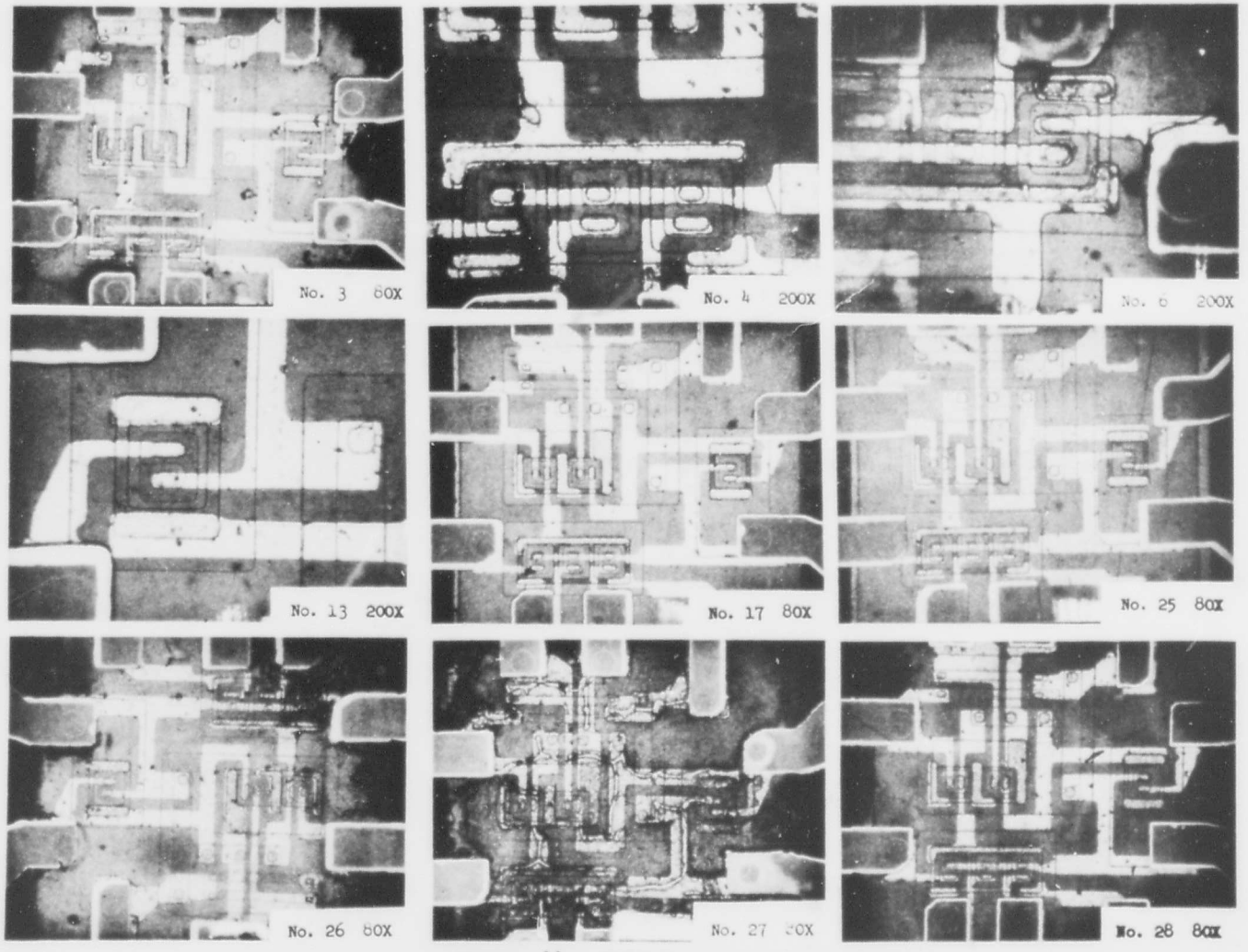


Figure 44. RADC Examination after Tests

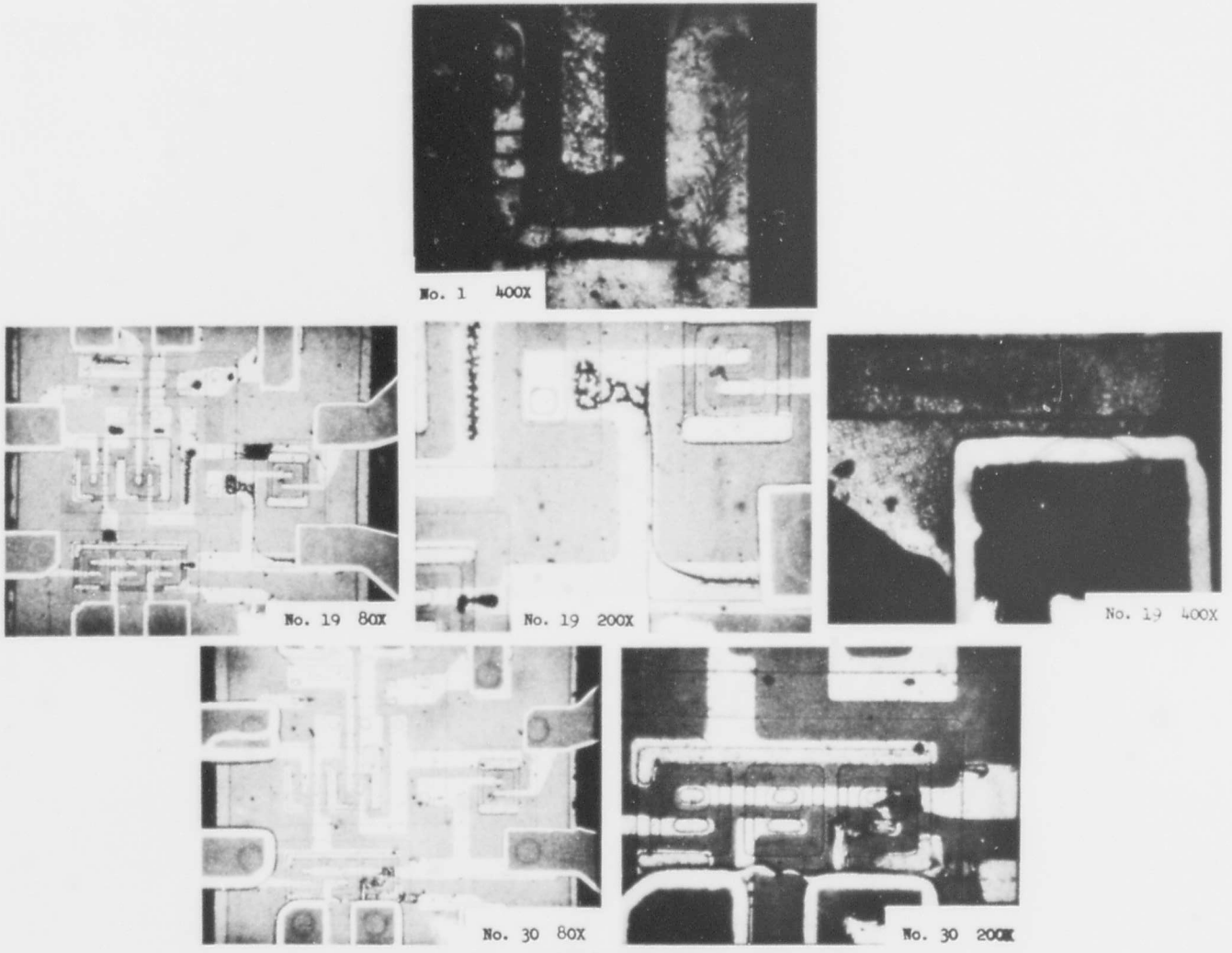


Figure 45. RADC Examination after Tests

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13 ABSTRACT

A study has been performed by the Univac Division to determine the overall reliability of its face-down-bonding process and to determine whether the bonding process damages the chip. The ultrasonic direct-bonding process was used to fabricate approximately 900 test samples for this study. Samples were subjected to the following tests: shear, mechanical shock, thermal shock, vibration, centrifuge, high-temperature storage, elevated-temperature back bias, step stress and comparison, and temperature and humidity. Defective units were examined for causes of failure. The test results indicate that the stresses applied during bonding do not affect circuit operation. The bond failure rate was high, but the distribution of failures suggests that this was due to inadequate substrate process control rather than inherent problems with face-down bonding. The substrate interconnect wires corroded in high-temperature and high-humidity ambients. Several potential solutions to this problem are suggested.

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14 KEY WORDS	LINK A		LINK B		LINK C	
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