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TENTH INTERIM REPORT

R & D OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS

Covering the period

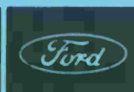
1 October to 31 December 1966

Prepared for

MIT, Lincoln Laboratory
P.O. Box 73
Lexington, Massachusetts 02173

Subcontract No. 295

Prime Contract No. AF 19(628)-5167



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SECTION I - INTRODUCTION

1.1 SCOPE OF REPORT

This report describes the work performed during the second quarter of the research and development program, "R & D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems." The report is titled "Tenth Interim Report" because the present program is actually an extension of Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(628)-4167), which began in July of 1964. The previous two one-year programs conducted under this subcontract were entitled "R & D Program to Design and Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Time of 1 Nsec," and "R & D of a New Class of NPN Silicon Transistor Switch Exhibiting UHF Capabilities."

1.2 PROGRAM OBJECTIVES

The main objective of this program is the fabrication of ultrahigh-speed microcircuit arrays to establish the technological requirements for achieving very high speed computer systems through the incorporation of increasing amounts of high-speed logic circuitry on a single monolithic silicon chip.

A second objective is to continue development of design principles and fabrication techniques for improving switching

speeds of microcircuits, using simple circuit designs as test vehicles. Microcircuits of both saturating and unsaturating types will be developed, with particular emphasis placed on obtaining optimum switching speed-power dissipation properties.

1.3 AREAS OF INVESTIGATION

1.3.1 High Speed Complex Bipolar Arrays

The major task of this program is the investigation of the technological problems involved in designing, fabricating, and testing various forms of small geometry, high-speed complex bipolar arrays. It was demonstrated on the previous programs that digital bipolar microcircuits which operate at propagation delay times of 0.2 - 0.4 nsec can be practically fabricated through the use of small component geometries (0.1 mil) and shallow junction devices ($\leq 0.5\ \mu$). (Basically, these techniques provide the low parasitic isolation capacitances and the high-speed transistor capability which are essential to high-speed microcircuit operation.) However, the high-speed potential of these microcircuits would never be fully realized in a conventional system environment because of the slowing effects of package parasitics and interwiring delays. The specific advantage of the small geometry-complex array is that it permits the basic high-speed capabilities of small geometry microcircuits to be translated to the system level by providing an environment with minimum delaying effects.

By fabricating and interconnecting larger repetitive portions of computer systems on single blocks of silicon in the form of arrays, the number of packages and the amount of interwiring in the computer will be reduced. This in turn will result in increased system speed and lower system cost.

One of the natural consequences of increasing microcircuit complexity is the need for a multilevel interconnection system on the chip. The interconnection system which was adopted for use in this program utilizes aluminum conductor layers and vapor deposited SiO_2 insulator layers.

The first vehicles chosen for the array investigation were 3-, 9-, and 27-bit parity generators. The parity circuit arrays contain 58, 232, and 754 components, respectively, and require two (3 bits) or three (9- and 27-bits) levels of metalization. The logic form of the parity arrays is ECL.

The design phase for all three parity array types was completed during the first quarter of this program. A brief summary is given in Section III. The fabrication and evaluation phases, begun during the first quarter, continued during the second quarter.

One of the fundamental problems encountered in bipolar array fabrication is yield. The number of arrays per wafer which an array process is capable of producing is strongly dependent upon

the device (transistors, diodes, resistors, etc.) yield which is characteristic of the microcircuit process, plus the number of defects introduced by the multilevel metalization process. Consequently, to produce arrays of a given complexity, the array process must not only be capable of a certain minimum device yield, but it must also introduce only minimal multilevel defects. The more complex the array, the more stringent the demands on device yield and multilevel defects.

In general, in small geometry arrays, the yield problems at the microcircuit and the multilevel metalization levels are acute, due to the added constraints of the small geometries involved. Therefore, a major subtask of this program is to attack the fundamental factors which affect yield at both of these levels so that functional arrays of the order of complexity of the 9-bit and 27-bit microcircuits can be fabricated and evaluated.

Another formidable array-related problem is encountered in the area of evaluation and analysis. Establishing failure modes on large complex arrays is, in many cases, virtually impossible. Generally, some sort of simple test vehicle is required. In this program, the simplest array, the 3-bit (40 transistors, 18 resistors) device serves as an excellent vehicle for studying processing problems. The 3-bit array is sufficiently complex to embody the problems which are common to the large arrays, yet simple enought to permit reasonable analysis.

Finally, small-geometry complex arrays impose special demands in the area of testing and packaging. The multiplicity of pads (23 and 59 for the 9- and 27-bit arrays, respectively) and the close pad spacings (center-to-center spacings are 5.1 mils on the 27-bit array) necessitate the development of both special multiprobe test fixtures for die sorting, and special packages. Inasmuch as the array technology is relatively new, these are not, in general, commercially available.

1.3.2 High Performance Microcircuits

A second, equally important, part of the program is to continue investigating the factors which determine the performance and yield of small geometry monolithic microcircuits, using simple microcircuit forms as vehicles.

Program plans for the first three quarters call for concentration on non-saturating type microcircuits, specifically ECL microcircuits, because this logic form has the most promising ultimate speed-power properties. Thus far, SMX2-design ECL gates (0.1-mil geometry) have been made which operated at average propagation delay times as low as 0.2 - 0.4 nsec while dissipating 60 mW. Subsequent analysis indicates that, with an optimized design, the ECL gate can be made to operate at 0.1 to 0.2 nsec delays, with only 40 mW average power dissipation. Micron geometry versions of the gate can be expected to operate even faster and at less power dissipation.

As part of this over-all effort, a computer analysis of the SMX4, a 0.1-mil ECL gate designed and fabricated during the latter part of the previous program, is being conducted by D. Eckl of Lincoln Laboratory. The computer program being employed is Net I.

During the latter part of this program, efforts will be focused on obtaining very high speed saturating circuits. This will require the development of unique techniques for reducing storage time, which at the present time limits saturating circuits from operating at subnanosecond speeds.

SECTION II - FACTUAL DATA

2.1 SUMMARY

During this second quarterly period, the following milestones were passed in the area of high-speed arrays:

1. New yield improving techniques have been developed and incorporated into the basic microcircuit processing and multilevel interconnection processing which we employ in fabricating the 0.1-mil geometry parity arrays.
2. An order of magnitude increase in yields of 3-bit arrays has resulted from incorporation of these new processing techniques.
3. 3-bit arrays have been fabricated which operated at 0.8 - 1 nanosecond speeds, while dissipating only 40 milliwatts (average gate dissipation is ≈5 mW).
4. Fabrication of the first 9-bit and 27-bit array wafers was completed.
5. Die sort equipment for testing all three array types was assembled.
6. Packages for all three array types were procured.

In the area of new microcircuits. two new ECL microcircuit designs, the SMX6 and SMX7, were completed. The SMX6. a new 0.1-mil version of the same basic ECL gate form employed by the SMX2 (see Figure 1), is expected to operate in the 0.1 - 0.2 nanosecond range, dissipating approximately 40 mW. The SMX7 is a micron version of the SMX6. It is expected to operate in the 25 - 100 picosecond range at less power than the SMX6.

During this period, substantial improvements were also made in our processing capability and in the performance of micron size transistors. SX4 transistors, employing 0.05-mil wide emitters and base contact stripes, were fabricated with significantly improved yields and with f_T as high as 9 GHz.

2.2 MICROCIRCUIT ARRAYS

2.2.1 Introduction

The parity circuit arrays are complex, high-speed computer oriented microcircuits. The basic array gate derives its high speed capability from small component geometries (minimum geometric size - 0.1 mil) and shallow component diffusions. Fundamentally, the 3-, 9-, and 27-bit arrays differ only in complexity. The 3-bit array contains 8 gates, while the 9- and 27-bit arrays contain 32 and 104 gates, respectively. Figure 2 is a schematic of the 3-bit array; Figure 3 is a logic diagram of the 9- and 27-bit arrays, wherein a single block represents the circuitry of one three-bit. All three array types require multilevel metalization.

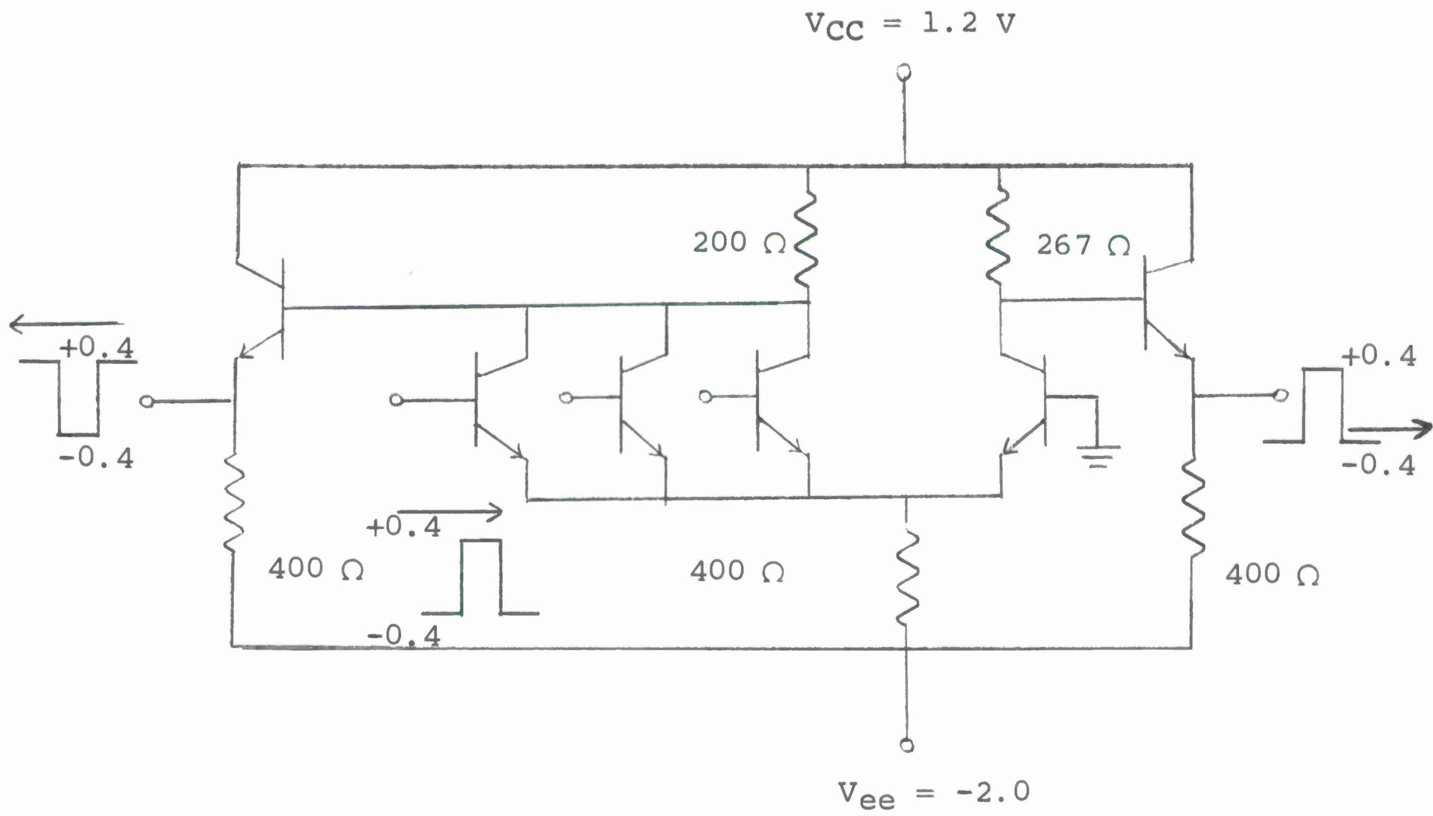


Figure 1. SMX6 microcircuit.

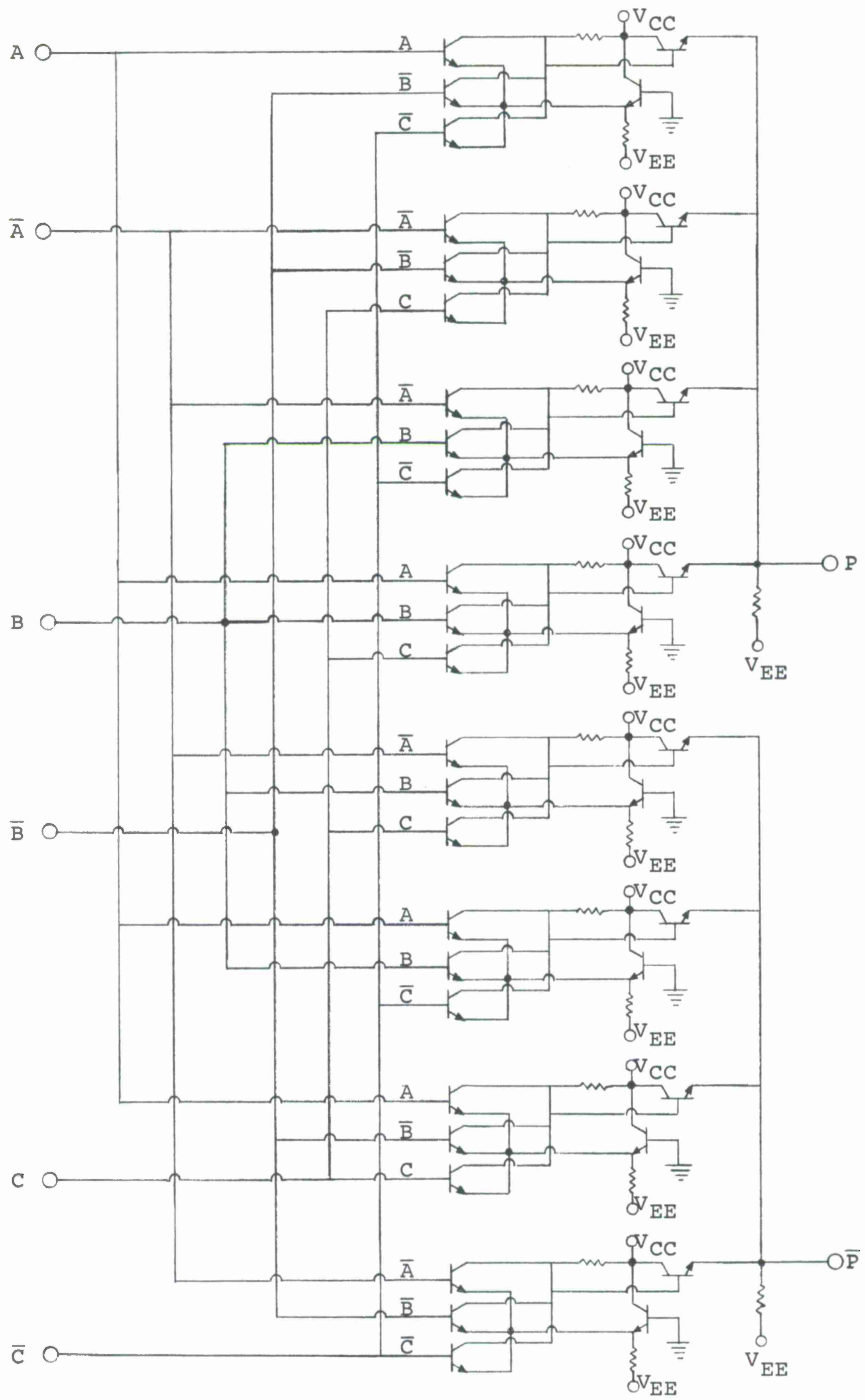


Figure 2. Schematic of 3-bit parity array circuit.

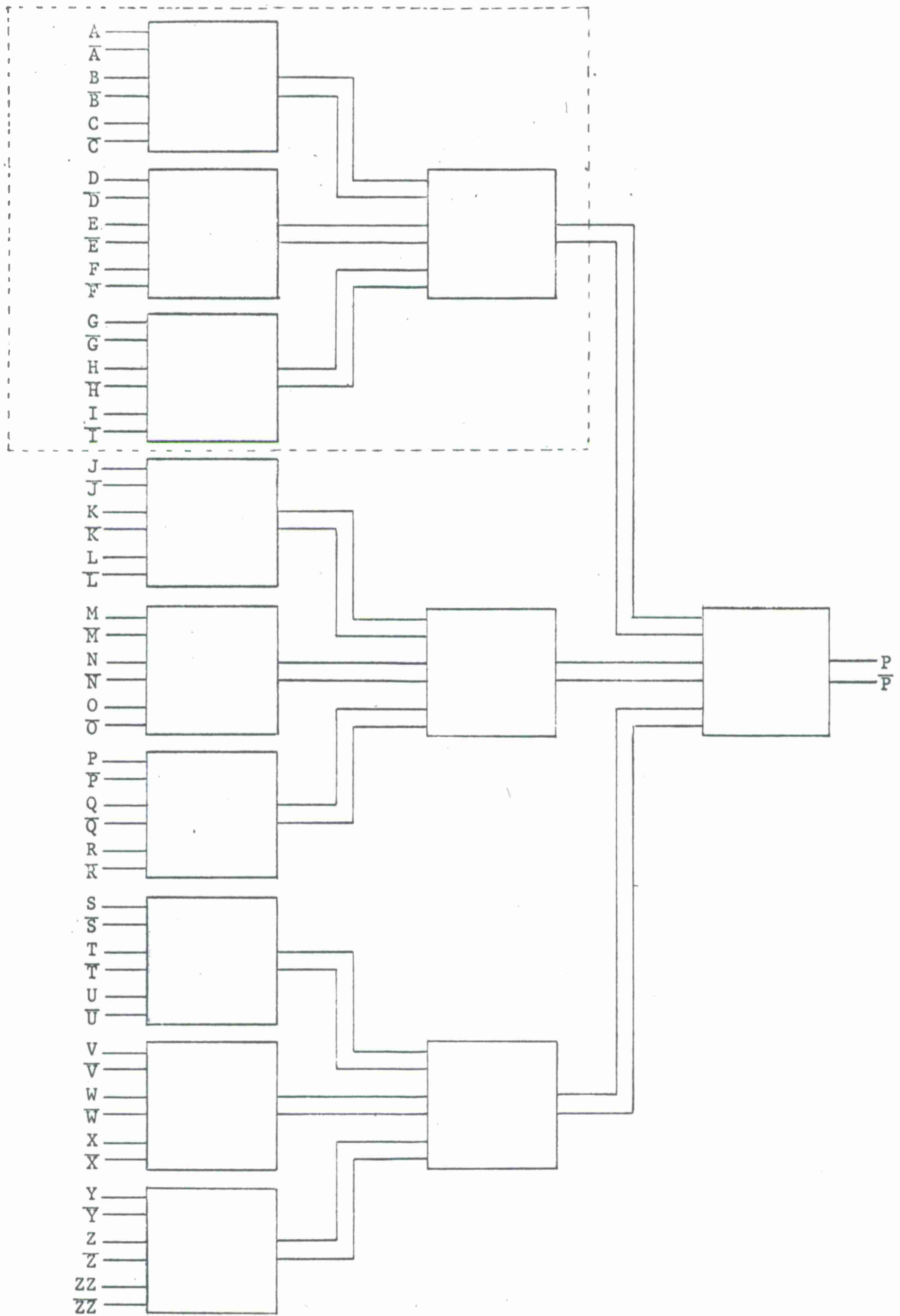


Figure 3. 27-bit parity circuit. (Portion enclosed by dashed line represents a 9-bit array.)

The over-all approach employed in these arrays is the commonly referred-to "cell approach." The cell approach involves

1. Generating a master wafer of 3-bit circuit cell patterns, complete with device metalization, and
2. Appropriately interconnecting these cells through multilevel metalization systems to form the completed 3-, 9-, and 27-bit arrays. The 3-bit array requires two levels of metalization, and the 9- and 27-bit arrays require three levels of metalization. Aluminum is used as the multilevel metal, while vapor deposited SiO_2 layers serve as the interlevel insulators. Figure 4 illustrates the basic cell pattern. Photographs of the completed arrays are presented in Figures 7, 8, and 9.

Fabrication of the 3-bit array actually deviates from the scheme presented above in that the first level metal pattern has been modified slightly to allow the 3-bit array to be fabricated with only two levels of metalization.

2.2.2 Array Technology

The main problem encountered thus far in fabricating the parity arrays has been yield. In the following text we will discuss the yield problems related to fabricating the array cells (the term "cell" meaning the array complete to the point of first

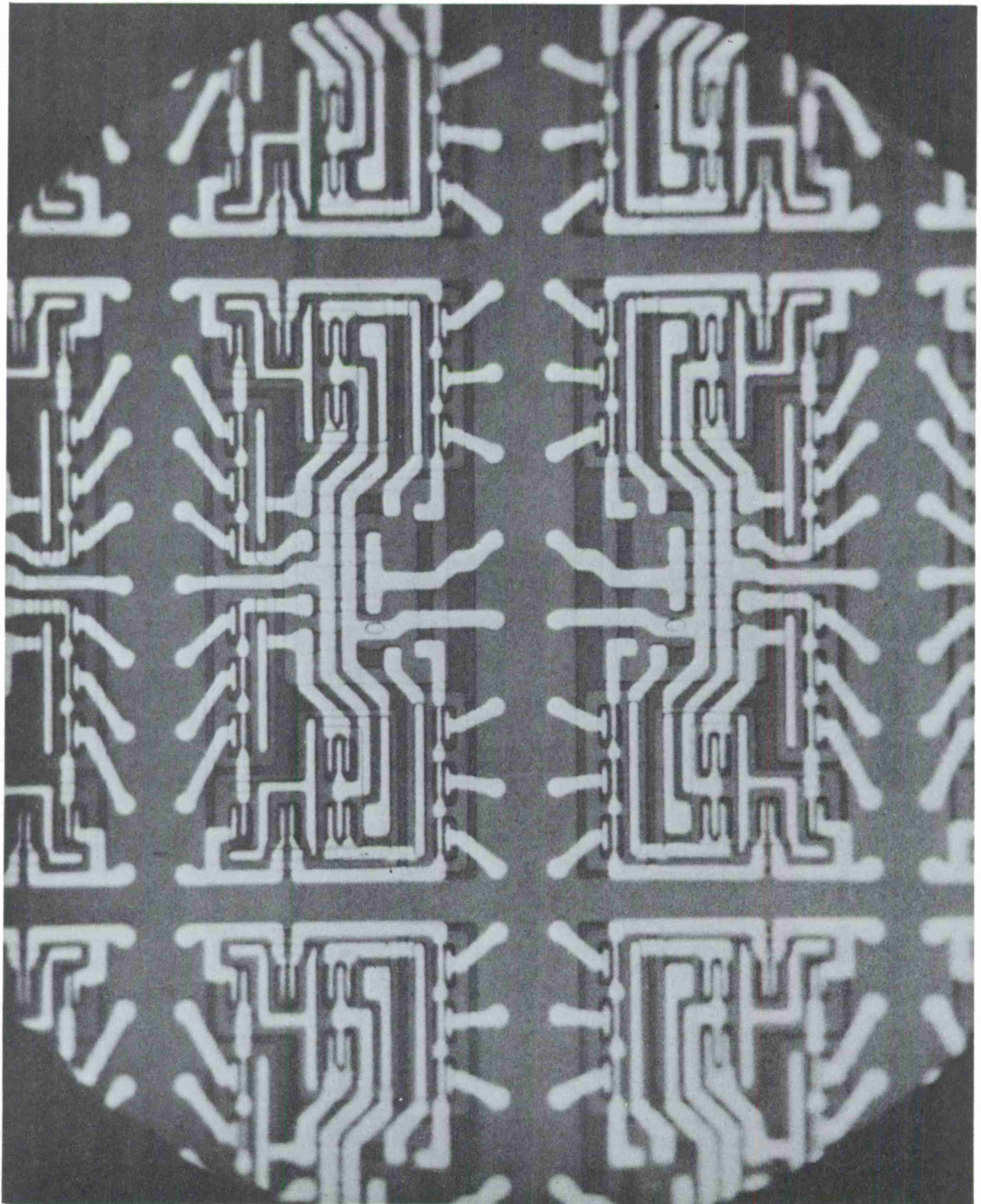


Figure 4. Basic cell pattern for parity arrays.

metalization) as well as yield problems related to fabricating the small geometry multilevel interconnection structures. We will also discuss process improvements which have substantially increased yield in both of these areas.

The two main failure modes which we have encountered in fabricating high-speed small geometry microcircuits are those of emitter-base and emitter-collector shorts and shunts. Both of these failure modes are natural outgrowths of the small geometries and narrow basewidths which are required in high-speed transistors. Unless these failures are minimized, the realization of arrays with complexities similar to that of the 27-bit parity checker will be virtually impossible.

During this past quarter, a concerted effort was made to minimize the causes of transistor E-to-B and E-to-C shorts and shunts. New process modifications which were introduced in photoengraving and diffusion were dramatically successful in reducing the incidence of these types of failures. On a recently fabricated wafer, transistor yields as high as 90% were achieved. Transistor yields previously obtained rarely exceeded the 60% level.

2.2.3 Yield Factors Related to Multilevel Interconnect Fabrication

The main yield problems which are encountered in fabricating multilevel interconnect structures are

1. High or infinite resistance interlevel connections, and
2. Interlevel shorts.

The principal causes of interlevel shorts are holes in the insulating layers between overlapping interconnection stripes. These pinholes can be defects formed during layer formation or holes generated during photoengraving. High resistance and electrically open interconnects are believed to be due to incomplete removal of insulator material in insulator feed-through cuts.

Early in this program, when low temperature (350°C) vapor deposited layers of SiO_2 were being evaluated as interlevel insulators, we determined that very few defects are generated in the SiO_2 layer during growth, provided that high standards of cleanliness are maintained. On early arrays, we further determined that the generation of pinholes during photoengraving was not a significant problem.

However, it subsequently became apparent that, when small area feed-through cuts are photoengraved (feed-through cuts in the parity arrays are 0.2-mil circles) in array structures, exposure times which are optimum for obtaining proper size cuts may not always be sufficient to produce a pinhole-free photoresist mask. This situation is somewhat similar to that

encountered in making small area device cuts, except that it is aggravated by the presence of aluminum pads beneath the insulator cut. The aluminum, because of its reflectivity, exaggerates the diffraction effects which occur at the photomask pattern edge, causing overexposure to occur much sooner. Thus, if a single-layer photoresist system is used, the problem remains of compromising pattern size and pinhole densities.

To resolve this dilemma, double coat-double etch photoengraving was adopted. Although this process requires an extra photomask and extra processing, the results justify the additional effort.

The double coat-double etch processing system developed was as follows:

1. Spin on and develop in the first layer of photoresist, the required pattern of 0.2-mil openings, using optimized resist thickness and exposure for obtaining proper size patterns,
2. Bake harden this layer,
3. Etch halfway through the insulator,
4. Spin on and develop in a second layer of photoresist a pattern of 0.5-mil circles which are concentric with the 0.2-mil circles. The exposure time for this layer can be appreciably longer because of the larger pattern size,

5. Bake harden this layer,

6. Etch completely through the insulator layer.

The philosophy behind this process is that by double coating we can minimize pinholes while at the same time, employing two different mask pattern sizes (the second of which is less critical to overexposure), we can obtain proper size small insulator cuts.

The success of this technique has been dramatic. Pinhole densities were reduced by an order of magnitude. While this represents a major improvement, additional refinements will be required to insure that pinholes are not a major yield problem on arrays as large as the 27-bit parity array (chip size: 90- x 85-mils).

The second major multilevel problem - high resistance and open interconnections - has been somewhat more difficult to analyze. Our present opinion is that, in our system, the opens occur due to incomplete removal of insulator material in some feedthrough regions, and that this results either from nonuniform etching or from incompletely opened photoresist patterns. Ordinarily, one would assume that extended etching would solve this problem, especially since the average etch rate of the aluminum layer beneath the insulator is one and one-half orders of

magnitude less than that of the insulator. However, extreme care must be exercised in over-etching the insulator because over-etching by even a short time (10-15 seconds) has been found to result in complete removal of the aluminum beneath certain insulator cuts in some cases.

2.2.4 3-Bit Parity Arrays

Thirteen packaged 3-bit parity arrays passed final test during the past three months. All functioned properly within the design limits at propagation delay times of 0.8 - 1.1 nanosecond, dissipating an average of 42 mW. Calculated on a per-gate basis, this amounts to an average dissipation of 5.3 mW per gate.

The propagation delay time of these arrays was about twice that of previous arrays because, as reported previously, resistor values were to be approximately doubled to reduce power dissipation. Figure 5 shows the basic array gate with the new resistor values.

Figure 6 illustrates the test method employed to measure the array propagation delay. All the barred inputs of the 3-bit array are D.C. coupled and driven by an appropriate pulse, while the unbarred inputs are D.C. coupled and driven by a complementary pulse from the drive circuit. Note that the drive circuit which supplies the complementary outputs is a high-speed SMX2 ECL

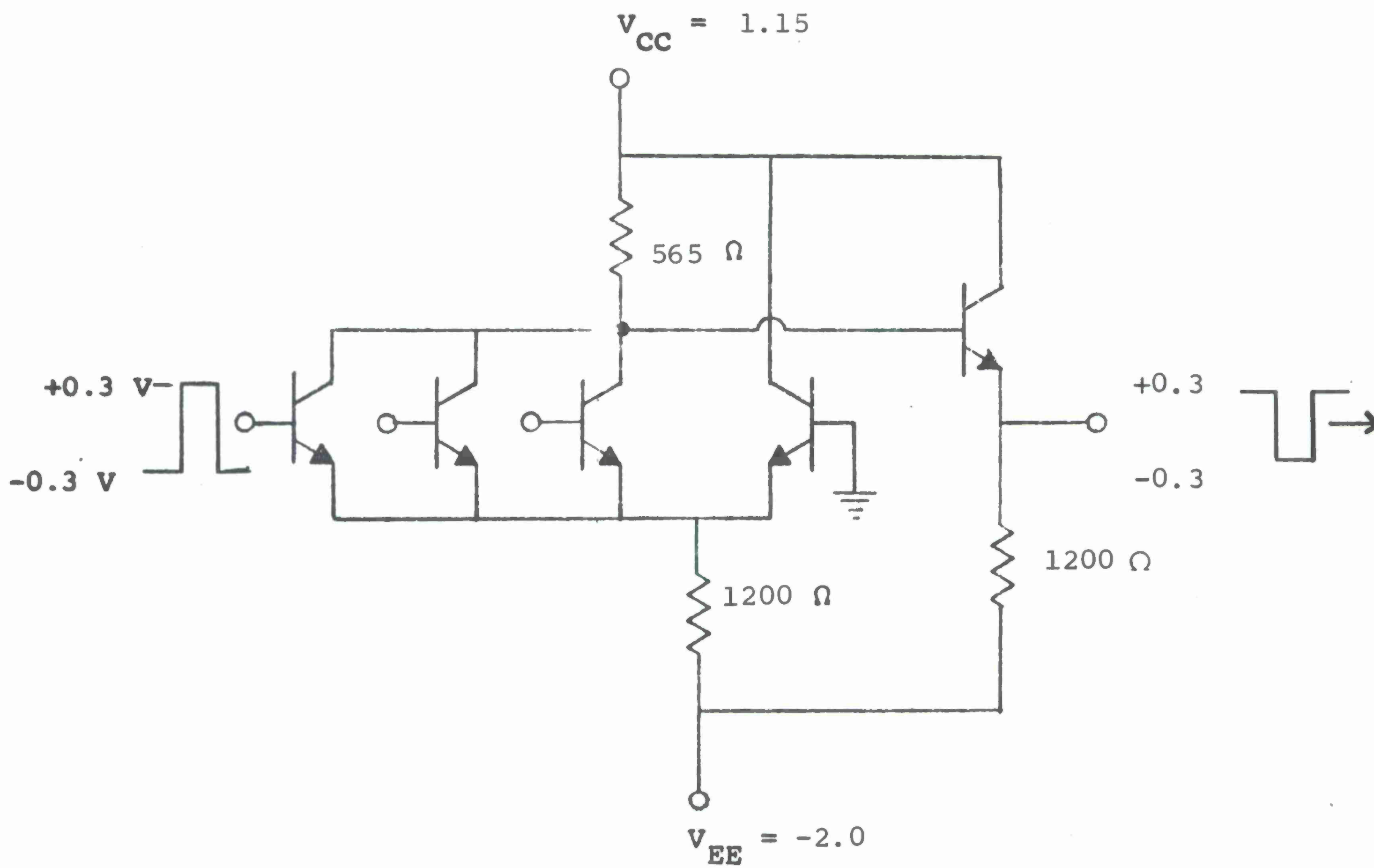
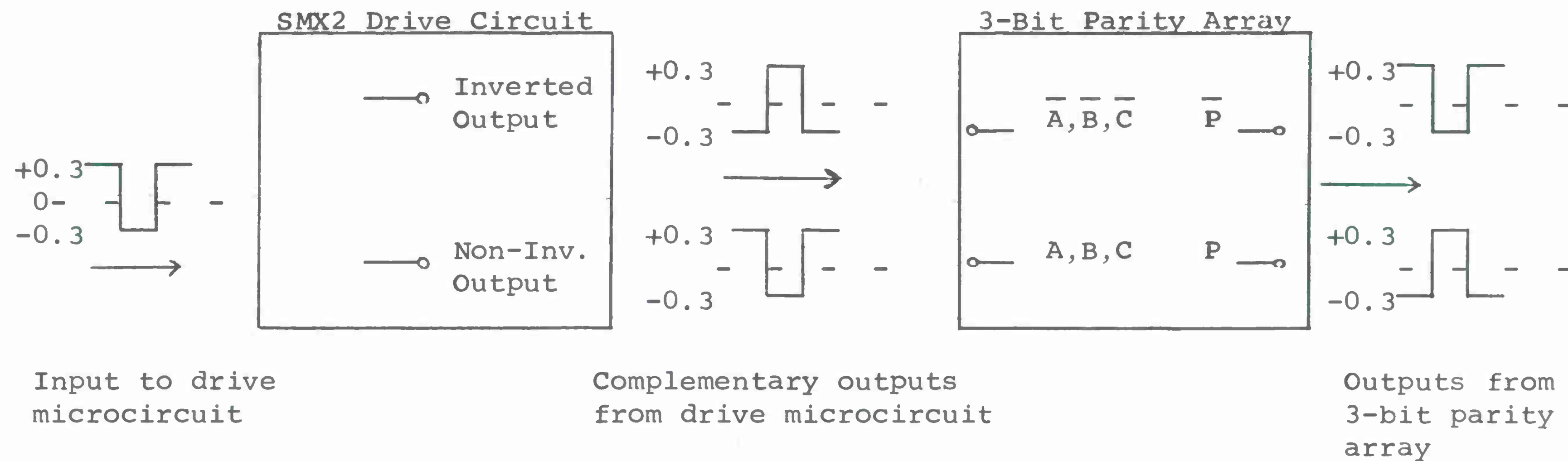


Figure 5. Basic 3-input gate for parity array.



Array #	Propagation Delays Through SMX2 Driver		Propagation Delays Through 3-Bit Arrays	
	Inv. Output	Non-Inv.	Output $\bar{P}$	Output P
1	----	----	1.10 ns	1.09 ns
8	----	----	1.11 ns	1.05 ns
11	----	----	1.07 ns	1.04 ns
14	0.63	0.75	1.05 ns	1.08 ns

Figure 6. (Top) Schematic illustrating test method employed to measure propagation delay time through 3-bit parity arrays.
(Bottom) Propagation delay data - 3-bit arrays - wafer SMX5-3-5d.

gate (τ_{pd} <0.4 sec). The table in Figure 6 illustrates propagation delay figures for four 3-bit arrays. Note also that the SMX2 drive circuit, while driving an fanout of 12, still operates at an average propagation delay of 0.7 nanosecond.

Six wafers of 3-bit arrays were evaluated during this period. Of these, only the last two were fabricated using the new improved techniques described in paragraph 2.2.2. All thirteen of the 3-bit arrays obtained came from these last two wafers. The major failure modes encountered in the first four wafers were device shorts and shunts (E-C and E-B), and inter-level metalization shorts due to insulator pinholes. Failure analyses conducted on the last two wafers (those made with the new process) indicated that the major yield problem still remaining was that of microcircuit opens, primarily attributable to incompletely etched-out insulator feedthrough cuts. Figure 7 is a photomicrograph of the 3-bit array.

Additional 3-bit arrays are in process. Future 3-bit arrays will be fabricated primarily to provide monitoring information on 9- and 27-bit arrays and to provide statistical data for the fabrication processes.

2.2.5 9-Bit Arrays

Several wafers of 9-bit arrays (Figure 8) were evaluated during this period. All were fabricated before the new process

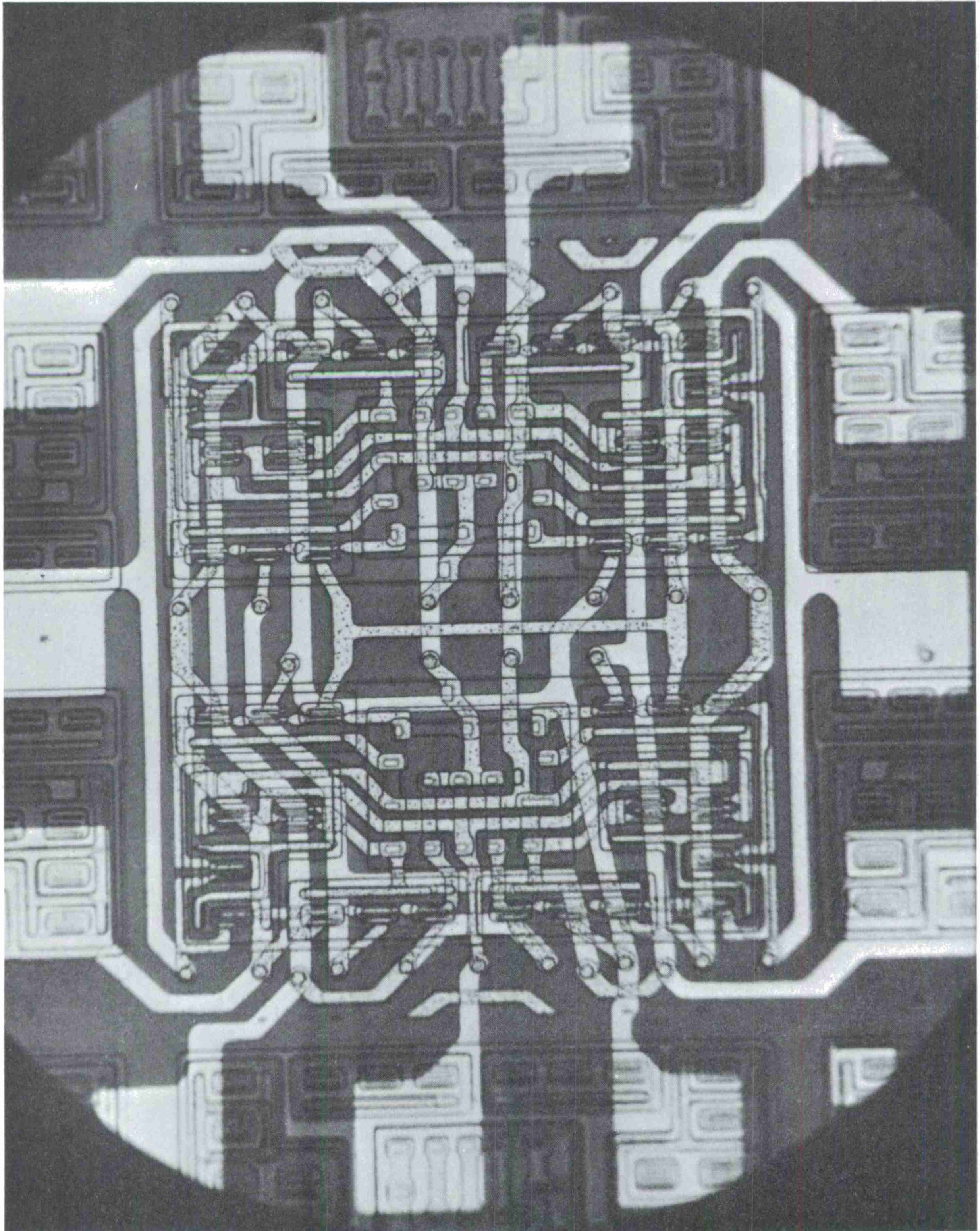


Figure 7. 3-bit parity microcircuit array.

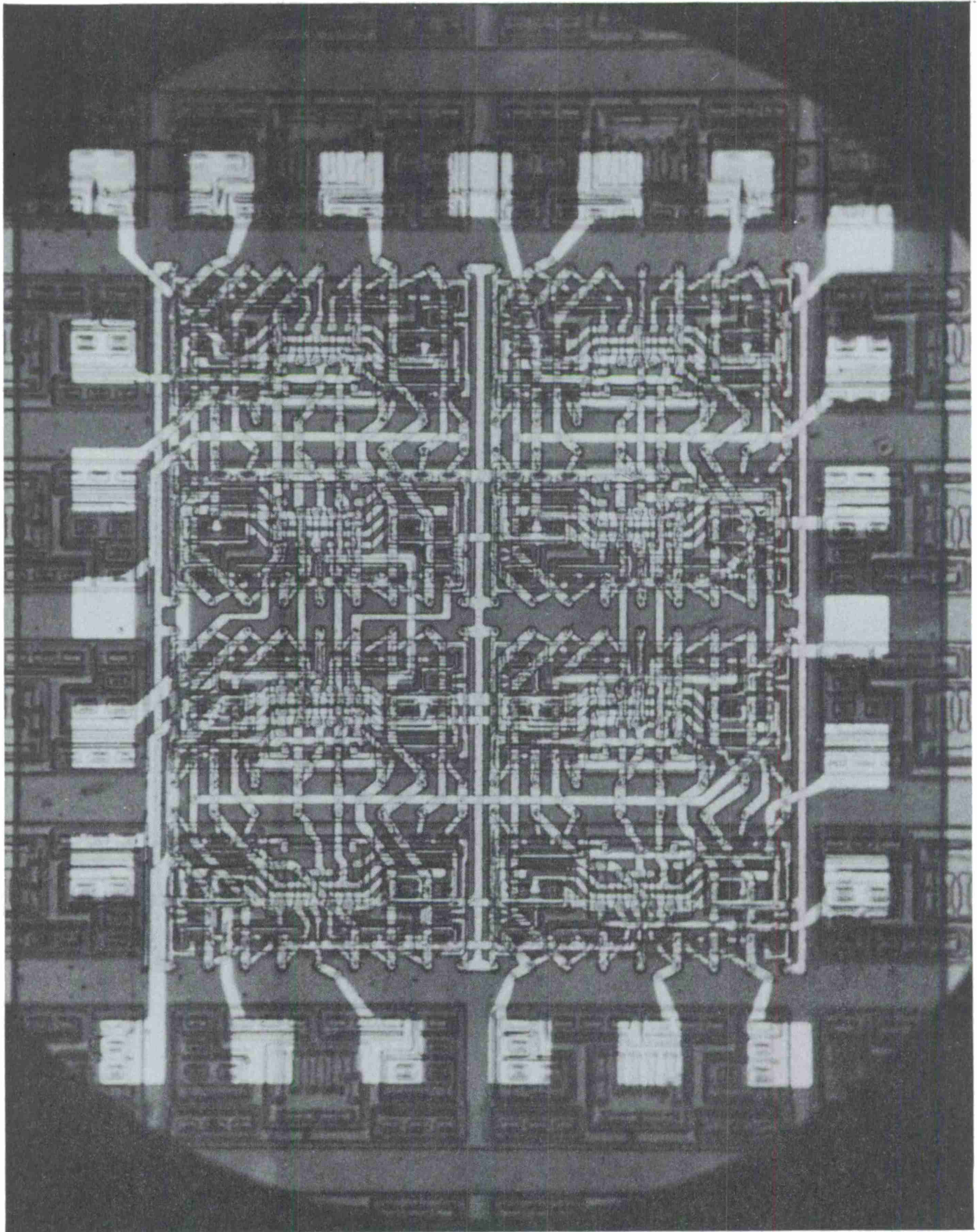


Figure 8. 9-bit array.

techniques were developed, and as a result yielded no useful arrays. There are indications that the failure mechanisms are the same as those on 3-bit arrays similarly fabricated.

Additional 9-bit arrays are in various stages of processing. During the coming period, 9-bit wafers will be completed utilizing some or all of the new techniques.

A special 23-point probe fixture, developed by Philco-Ford for die sorting the 9-bit arrays, has been put into operation and is performing well.

The 24-pin package selected for the 9-bit array was also developed by Philco-Ford.

2.2.6 27-Bit Arrays

Only one wafer of 27-bit arrays (Figure 9) was completed during this period. Although it was fabricated using the new processes, no functional arrays were obtained. This occurred mainly because the "anomalous aluminum etching" described in paragraph 2.2.3 was experienced on this wafer and the wafer had to be partially reprocessed.

Additional 27-bit array wafers will be forthcoming in the next period.

As was done for the 9-bit array, Philco Ford developed a special fixture for die sorting the 27-bit array. The fixture contains 59 fixed and accurately positioned spring-loaded probes. Probe center-to-center spacing is on the order of 5 mils.

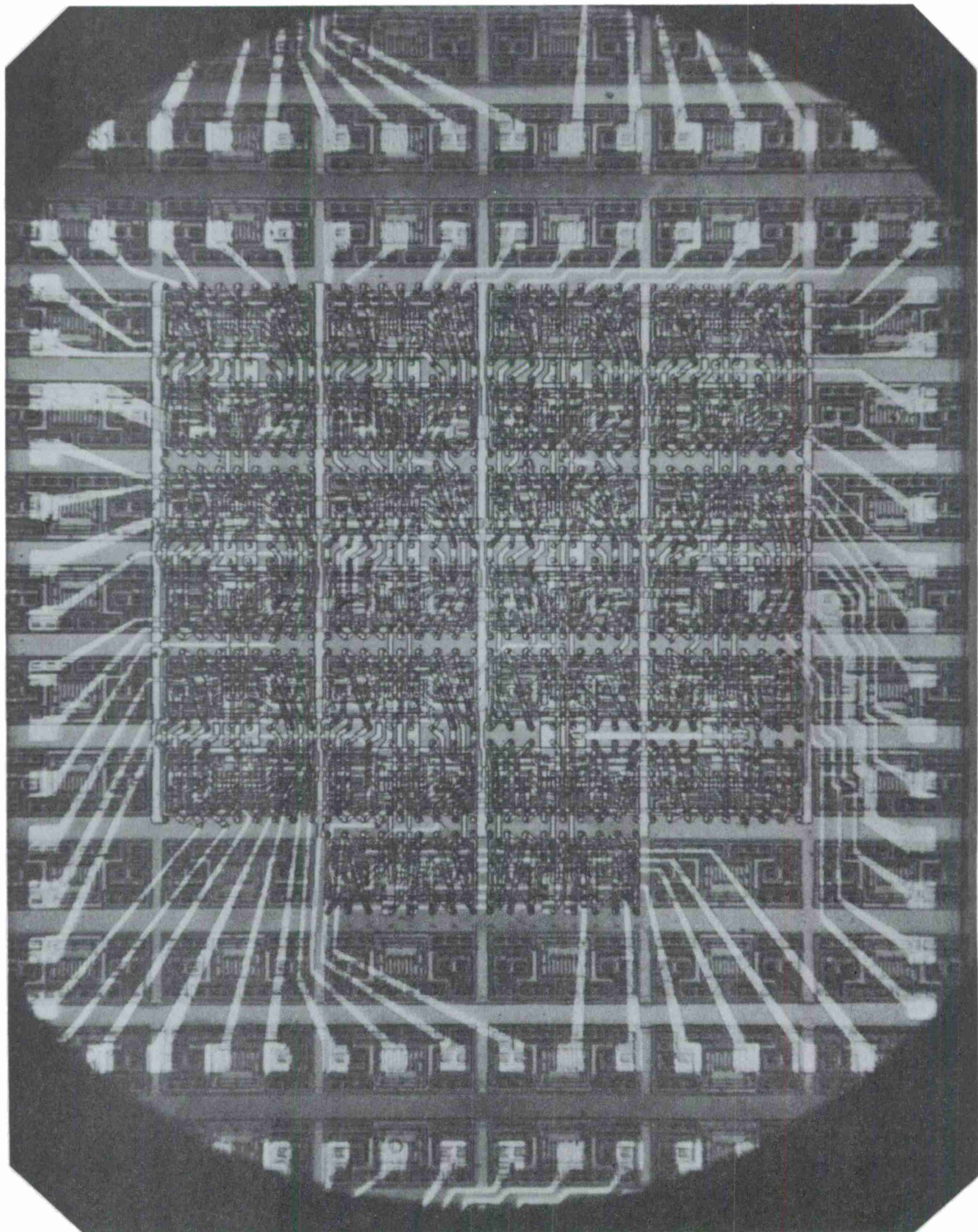


Figure 9. 27-bit array.

Finally, a special 60-pin package has been designed and is in the final stages of development.

The delivery of the semiautomatic tester, being built by Lincoln Laboratory for die sort and final D.C. testing of 3-, 9-, and 27-bit arrays, has been held back by delays in parts deliveries. However, the tester is expected to be completed and delivered shortly.

2.3 NEW MICROCIRCUITS

Two new high-speed microcircuit designs were completed during this period. The first is a new 0.1-mil geometry version of the same 3-input, complementary output ECL gate configuration (emitter follower output) previously employed for the SMX2. This, the SMX6 design, will feature transistors which are redesigned for optimum speed throughout their operating range, and resistors which are optimized for maximum microcircuit speeds (minimum RC delays) at reasonably low power dissipations. The anticipated performance levels are τ_{pd} = 0.1 - 0.2 nsec, P.D. = 40 mW.

In designing the SMX6, special emphasis was placed on incorporating design layout features which will insure the utmost in microcircuit yield without sacrificing performance.

The second design, the SMX7, basically a scaled-down version of the SMX6, will employ micron-size geometries. It is expected to operate at subnanosecond speeds and at less power than the SMX6.

As a preliminary to fabricating the SMX7, 0.05-mil geometry transistors (SX4) were fabricated in an attempt to improve processing techniques and to analyze further the speed properties of micron-size transistors. One significant result of this effort was the achievement of a transistor structure with the highest gain-bandwidth product yet reported. Device f_T's were typically in the range of 6 - 8 GHz at V_{CBO} = 4 - 6 V. One device had a gain-bandwidth product as high as 9 GHz. Figure 10 shows a plot of f_T vs I_C for the device, a multi-striped structure containing four 0.05- x 0.5-mil emitter stripes and five 0.05- x 0.5-mil base stripes.

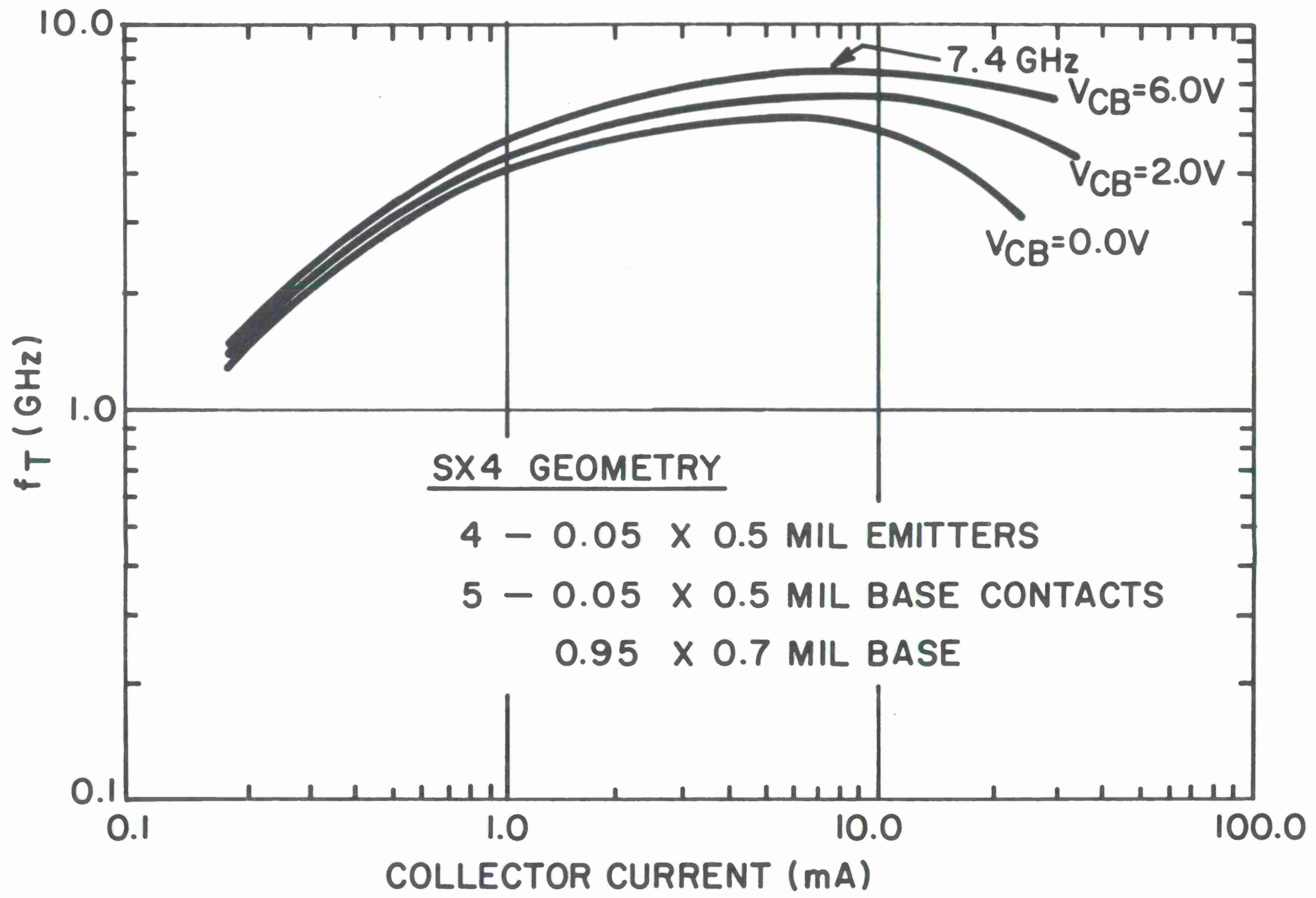


Figure 10. f_T vs I_C of SX4 transistor.

SECTION III - SAMPLE DELIVERIES

During this period, the following samples were delivered to Lincoln Laboratory:

Six	SMX4 Microcircuits
Thirty	SX4 Transistors
Eight	3-Bit Parity Arrays

SECTION IV - FUTURE PLANS

Program plans for the next quarter include the following items:

1. Continue fabrication and evaluation of 3-bit arrays. As indicated previously, this effort will be aimed mainly at monitoring the improvements in yield that future refinements in processing will produce.
2. Continue fabrication and evaluation of 9-bit arrays. Based on the improved yields obtained on recent 3-bit arrays, we expect that with slight additional refinements of the multilevel process, functional 9-bit arrays will be obtained in the next period.
3. Continue fabrication and evaluation of 27-bit arrays.
4. Generate the photomasks for the SMX6 and SMX7 designs, then fabricate and evaluate these microcircuits.

It is important to point out at this time that the fabrication of devices will be temporarily delayed during the next period due to a movement of facilities from the Lansdale plant to the Blue Bell installation. During the relocation, however, device assembly and evaluation will be virtually uninterrupted.

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13. ABSTRACT

A description is given of the work performed during the second quarter of the research and development program "R & D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems." The fabrication and evaluation phases of the 3-, 9-, and 27-bit parity arrays continued. In the area of new micro-circuits, two new ECL designs, the SMX6 and SMX7, were completed.

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