NINTH INTERIM REPORT

R & D OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH SPEED COMPUTER SYSTEMS

Covering the period

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SECTION I - INTRODUCTION

1.1 SCOPE OF REPORT

This report describes the work performed during the first three months of the research and development program, "R & D of the Technologies Required to Design and Fabricate Ultrahigh Speed Computer Systems." The program is an extension of MIT Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(628)-5167). Much of the preliminary work for this program was performed during the final months of the previous program, "R & D Program to Design and Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Time of 1 Nsec," which ended June 30, 1966.

1.2 PROGRAM OBJECTIVES

The principal objective of this program is the fabrication of ultrahigh-speed microcircuit arrays to establish the technological requirements for achieving very high-speed computer systems through the incorporation of increasing amounts of high-speed logic circuitry on a single monolithic silicon chip.

A second objective is to continue development of design principles and fabrication techniques for improving switching

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speeds of microcircuits, using simple circuit designs as test vehicles. Microcircuits of both unsaturating and saturating types will be developed, with particular emphasis placed on optimizing the switching speed-power dissipation relationship.

1.3 AREAS OF INVESTIGATION

The main program effort is concentrated on the investigation of the technological problems involved in designing, fabricating and testing various forms of small-geometry, high-speed, complex bipolar arrays. The first vehicles chosen for this study were 3-, 9-, and 27-bit versions of a computer (parity generator) circuit. These parity circuit arrays contain 58, 232, and 754 components, respectively, and require two (3-bit) and three (9- and 27-bit) levels of metalization. Preliminary work on the concepts and techniques for fabricating these ECL arrays was performed in the latter part of the previous program and was reported in the eighth quarterly summary report.

A secondary, but perhaps equally important, part of the program is to continue investigating the factors which determine the performance and yield of simple high-speed microcircuits. Typical of the types of microcircuits which are to be studied is the simple 3-input-complementary output SMX4 ECL gate, which was evaluated during the last quarter of

the previous program and during the first quarter of this program (see Microcircuit Development, subsection 2.2). This phase of the program will include work with 0.1-mil geometry microcircuits of both the saturating and non-saturating types, as well as microcircuit structures employing micron size transistor geometries.

The microcircuit transistors play a dominant role in determining ultimate microcircuit performance and yield. Therefore, efforts are constantly being made to improve the design and fabrication techniques involved in producing these components. The realization of nearly 100% transistor yield becomes a virtual necessity for successful fabrication of microcircuit arrays whose complexity is equivalent to or greater than the 27-bit parity circuit (520 transistors).

SECTION II - FACTUAL DATA

2.1 SUMMARY

During these first three months of the program, effort concentrated mainly on the parity circuit arrays. The first functional 3-bit parity arrays were fabricated. Fabrication of the 9-bit array began, and the composite drawings for the 27-bit parity array have been completed. None of the anticipated photomask equipment problems which could affect generation of small cuts over the large (90 by 85 mils) 27-bit array chip materialized. The main problem in producing these complex high-speed arrays is component yield.

In the area of new microcircuit designs, continued evaluation of the SMX4 ECL microcircuit gate revealed that this microcircuit design is not capable of the low tenth-nanosecond operation for which it was intended. The SMX4 appears to have a basic propagation delay limit on the order of 0.6 nsec. However, we feel that we understand the limiting factors. Thus, the redesigned version of the ECL gate planned for the next quarter should ultimately yield the desired 0.1 nanosecond (or less) propagation delay time.

2.2 MICROCIRCUIT DEVELOPMENT

2.2.1 SMX4

As discussed in the eighth quarterly summary report, preliminary evaluations of SMX4 microcircuits indicated that this microcircuit design would probably not be capable of the 0.1 - 0.2 nanosecond operation for which it was intended. Microcircuits from the first wafers to be fabricated were believed to be limited in speed (τ_{pd} = 0.65 - 0.75 nsec) largely because of the emitter capacitances of the gating and reference transistors. Even though the microcircuit transistors had peak f_T values of 3.0 to 3.5 GHz at V_{CB} = 1 V, the average f_T of these devices during turn-on and turn-off was considerably less because of the emitter transistor capacitance.

During this quarter we attempted to increase the average f_T during turn-on and turn-off by increasing the peak f_T of the SMX4 transistors. We fabricated SMX4 circuits which had peak f_T in the 3.5 to 3.8 GHz range. However, test results indicated that there was almost no improvement in microcircuit speed (τ_{pd} was still on the order of 0.65 to 0.7 nsec). These results and others, particularly those obtained on SMX2 microcircuits (τ_{pd} = 0.4 nsec), indicate that a redesign of the ECL microcircuit gate, incorporating smaller area gating and

reference transistors, will be necessary for the ultimate achievement of low tenth-nanosecond operation. We plan to redesign the ECL gate during the next quarter.

The SMX4 microcircuit, as originally designed, has high current drive capabilities and should be capable of high fan-out operation with little degradation in speed. Ring oscillator experiments on SMX4 microcircuits conducted by Lincoln Laboratory verified this capability. Increasing fanout from 1 to 5 was found to increase τ_{pd} by only 0.25 nsec, i.e., from 0.65 to 0.90 nsec. The fanout of 5 was simulated by adding four parallel networks of 1-pF capacitors and 7.5-k Ω resistors to each output terminal in the ring.

One of the circuit groups at Lincoln Laboratory recently requested a sample quantity of 25 SMX4 microcircuits for use in computer experiments. Nineteen of the requested 25 microcircuits have already been delivered. All had propagation delay times between 0.68 and 0.76 nanoseconds. Additional microcircuits for fulfilling the request are being final tested.

Unless specific requests are made for additional SMX4 microcircuits, all work on this microcircuit will terminate shortly.

2.3 MICROCIRCUIT ARRAYS

2.3.1 Introduction

The parity circuit arrays are highly complex, high-speed microcircuits which incorporate the basic small geometry and shallow diffusion technologies developed in part during the previous programs. Because of the component density, the parity arrays require multi-level interconnection systems. The over-all approach to fabricating these arrays involves

1. Generating a master wafer of "3-bit circuit cells," complete with device metalization, and
2. Appropriately interconnecting these cells through multi-level metalization systems to form the 3-, 9-, and 27-bit arrays. The 3-bit array requires two levels of metalization (counting device metalization as one level), while the 9- and 27-bit arrays require three levels of metalization. Aluminum is used as the multi-level metal, while vapor deposited SiO_2 layers serve as the interlevel insulators.

Developments on each of the arrays are reported in the following paragraphs.

2.3.2 3-Bit Parity Array

The first functional 3-bit parity array circuits were successfully fabricated during this period (see Figure 1.) Preliminary test results indicate that the average signal propagation delay through the 3-bit array, which contains 40 0.1-mil geometry transistors, 18 resistors, and two levels of metalization, is in the range of 0.5 nsec. This agrees well with propagation delay times obtained previously on the basic array gate (3 transistors and 3 resistors). The basic gate was obtained by using a special test metalization pattern to generate the single ECL gate from the array slice. The test pattern permits evaluation of transistors as well as of the basic gate, requiring only the conventional single level of metalization to do so.

As expected, the yield of 3-bit arrays obtained from the first four wafers process was low. Two of the four wafers were used to optimize the mechanics of forming the small-geometry, bilevel interconnection system. On the two succeeding wafers, one of which provided the functionally operative circuits, high circuit yield apparently was limited by the random E-B and E-C shorting common to simpler small geometry-shallow diffused microcircuits. Since the 3-bit parity circuit contains about seven times more transistors than any of the

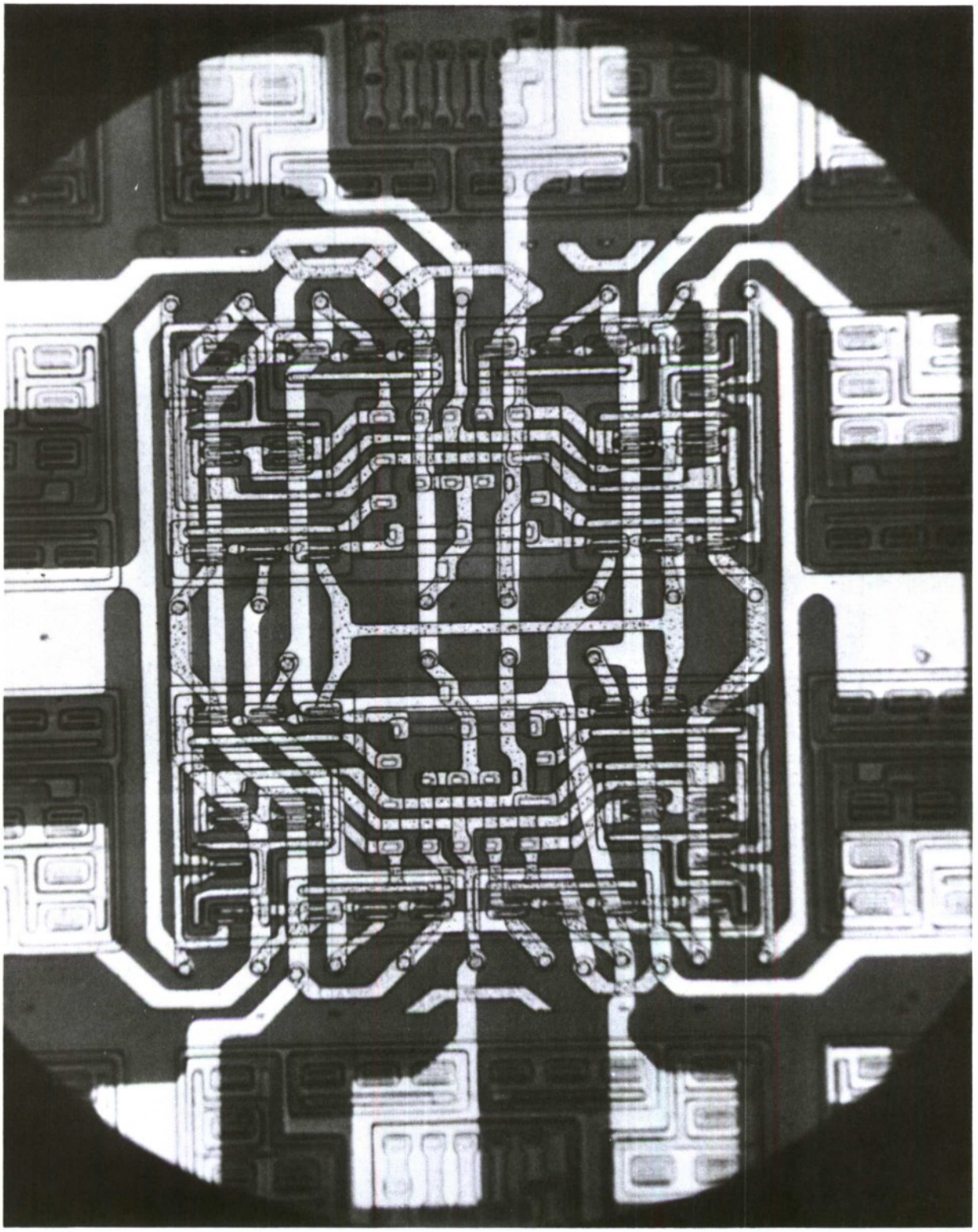

Figure 1. Three-bit parity microcircuit.

simpler microcircuits yet fabricated, it is to be expected that the E-B and E-C problem would more acutely affect yield. We are conducting experiments to determine the causes of E-B and E-C shorts.

Although direct analysis is somewhat difficult, it is important to note at this time that the array yields are relatively unaffected by defects in the vapor deposited SiO_2 layers.

Additional 3-bit wafers are in process. The first of these has been die sorted and is expected to yield functional arrays. The performance speed of these arrays is of particular interest because resistor values in the arrays have been increased to twice their original design values. This was done to significantly reduce power dissipation without appreciably degrading microcircuit speed. For proper operation of the 27-bit array, power dissipation must be kept on the order of 35 mW for the 3-bit array (with an eventual goal of 450 mW for the 27-bit array). The 3-bit arrays in this newer group should dissipate approximately 25-35 mW.

To aid in die sorting parity array wafers, Lincoln Laboratory is assembling a functional tester. This semiautomatic tester will be capable of completely testing 3-, 9-, and 27-bit arrays under a variety of programmable test conditions

and acceptance criteria. We expect delivery of the tester in about a month.

2.3.3 9-Bit Parity Arrays

The photomasks for the interconnection system of the 9-bit parity arrays have been delivered by the photolab, and fabrication of the first 9-bit array wafers is in progress. The first completed wafers are expected shortly.

Some registration difficulties were encountered between the first level metal mask patterns and the first insulator cut mask patterns. At first we thought that the registration accuracy (better than 0.1 mil) required between these two mask patterns would present difficulties, since the two photomasks were generated on grossly different stepping centers. (The first-level metalization pattern is stepped on 17- by 15-mil centers, whereas the first insulator pattern is stepped on 51- by 45-mil centers.) However, more detailed evaluation of the problem revealed that not only can close registration be obtained between mask patterns generated on grossly different stepping centers, but that the registration difficulty experienced with these particular photomasks originated in the contact printing process rather than in the stepping process. New insulator cut mask copies were made which register properly with the first-level metal mask patterns.

2.3.4 27-Bit Parity Arrays

The final layout design of the multi-level metalization system for the 27-bit parity array is complete and photomask generation is progressing.

Based on our previous experience with making small geometry photomask patterns, we were concerned over the feasibility of generating 0.2-mil diameter circular patterns over a 76-mil field. This requirement was dictated by the design of the first-level insulator cut mask for the 27-bit array. To establish the adequacy of the photomask equipment, a test pattern of 0.2-mil circles was designed and fabricated. Examination of the oxide cuts made with the test photomask indicated that there should be no pattern resolution or registration problems. The major problems in constructing this complex circuit will be obtaining 754 components in a 60 x 60 mil area at high yield, and establishing methods of analyzing those chips which do not meet performance requirements.

SECTION III - SAMPLE DELIVERIES

During this period, nineteen SMX4 microcircuits were delivered to Lincoln Laboratory.

SECTION IV - FUTURE PLANS

Program plans for the next three months include the following areas of effort:

1. Continued fabrication and evaluation of 3-bit arrays,
2. Fabrication and evaluation of 9-bit arrays,
3. Generation of the photomasks for the 27-bit arrays, followed by fabrication and evaluation of these arrays,
4. Design of a new high-speed, high-yield complementary output ECL gate (SMX6) microcircuit for operation at low- or sub-tenth nanosecond speeds. In addition, every effort will be made to incorporate design factors which will insure the utmost in microcircuit yield without sacrificing performance.
5. Preliminary design of a low-power, high-speed Micron Microcircuit. This microcircuit is intended for use in investigating the speed improvements obtainable at low power through utilizing transistors which have geometries on the order of a micron (0.04 mil),

6. Design of a very high speed saturating circuit (TTL).

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13. ABSTRACT

A description is given of the first three months of the research and development program "R & D of the Technologies Required to Design and Fabricate Ultrahigh Speed Computer Systems." The main program effort is concentrated on the investigation of the technological problems involved in the design, fabrication and testing of various forms of small-geometry, high-speed, complex bipolar arrays. The first functional 3-bit parity arrays were fabricated and fabrication of 9-bit arrays was begun. The composite drawings for a 27-bit parity array were completed. Evaluation of the SMX4 ECL microcircuit gate continued as part of the investigation of factors which determine the performance and yield of simple high-speed microcircuits.

14. KEY WORDS

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