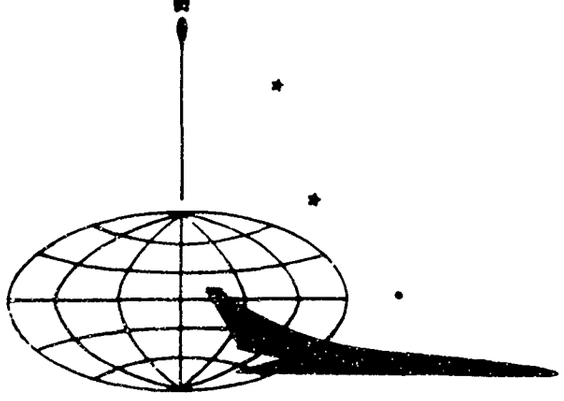
ATD Report 66-19 17 February 1966

Surveys of Soviet Scientific and Technical Literature

COMPUTER TECHNOLOGY

Compilation of Abstracts

Boris Doncov



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Surveys of Soviet Scientific and Technical Literature

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Compilation of Abstracts

ATD Work Assignment No. 81
(Report No. 5 in this series)

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FOREWORD

This is the fifth in a series of reports reviewing Soviet developments in computer technology. Abstracts contained in the report were selected from Soviet open-source literature recently available at the Aerospace Technology Division and the Library of Congress. Information not directly related to the assigned subject has been included because of its broad implications for study in this field. The 35 abstracts are arranged alphabetically by author within each of the following categories: components, design, applications, and associated systems. A recent review of two Soviet articles on homogeneous microelectronic structures is included in the Appendix. A bibliography is presented at the end of the report.

Full translations of some of the source materials used in this report may be available from other agencies or commercially. Interested readers may obtain translation data for individual sources by indicating source numbers from the bibliography list on the form attached at the end of this report and returning it to the Aerospace Technology Division.

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COMPUTER TECHNOLOGY

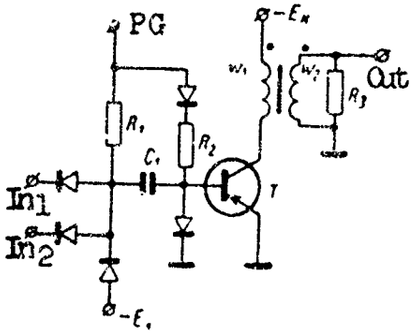
1. Components

Aslanova, M. S., and V. E. Khazanov. High-strength property of glass and quartz fibers at -196C (in liquid nitrogen). IN: Akademiya nauk SSSR. Doklady, v. 164, no. 6, 1965, 1277-1279.

Alkali-free aluminoborosilicate glass fibers with diameters d = 4—20 μ and quartz fibers (d = 10 μ) were subjected to tensile strength tests in free air at room temperature and at -196C in a humidity-free environment in which adsorption had been eliminated. The strength of glass fibers at -196C, as compared with the strength at room temperature, was 1.5—2 times greater (400—450 kg/mm^2). Maximum strength (800 kg/mm^2), was observed for 4—10-μ fibers. The average strength of quartz fibers increased 2.5—3 times under the same test conditions, and the maximum strength also reached 800 kg/mm^2. The strength of quartz fibers may be increased four times by fast extrusion; a maximum strength of 1000 kg/mm^2 at -196C was recorded. Decreasing the length of the quartz fibers (from 10 to 5 mm) increases the maximum strength by 30—40%.

Filippov, A. G. Transistorized dynamic inhibiting element with capacitive memory. IN: Fedotov, Ya. A., ed. Poluprovodnikovyye pribory i ikh primeneniye; sbornik statey, vyp. 13 (Collection of articles on semiconductor instruments and their utilization, no. 13). Moskva, Izd-vo Sovetskoye radio, 1965. 249-273.

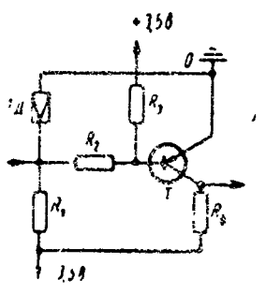
The proposed logic element, shown in the figure, performs the NOR operation with a multiple-input inhibitor stage, a delay stage, and an amplification stage. The number of inputs may be increased to 10—20 by including additional diodes. A ten input NOR element has performed successfully in laboratory tests. The pulse generator (PG) of bipolar pulses, together with R_1 and C_1, performs the required half-period delay. Since the stage is transformer coupled, it is impervious to temperature changes in the range of -60C to +60C. The circuit is also immune to bias variations of 30%. The ultimate speed capabilities of the NOR element are not given; however, the circuit operated at a clock frequency above 0.7 Mc when P414-P416 transistors were used.



Dynamic inhibiting element

Golovinskiy, L. V., and Ye. M. Sheremet. Evaluating drift failures in a tunnel diode switching stage. Izmeritel'naya tekhnika, no. 9, 1965, 4-6.

A tunnel diode-transistor switching stage, shown in the figure, was subjected to reliability analysis. The switching speed of the stage is limited only by the switching speed of the transistor; 50—100 nsec is cited. It was found that the circuit elements could be chosen in such a way that their drift of ±30—50% away from the nominal values would not affect the normal operation of the stage. Thus, the reliability of the stage would primarily depend on sudden failure of the elements. If both 0 and 1 inputs are present, the probability of the appearance of an output signal is 0.992. If degradation of input pulse shapes is taken into account, reliability of the circuit is 0.934.



Tunnel diode switching stage

Grezdov, G. I., and Yu. P. Kosmach. Development of control networks using cold-cathode tubes for adaptive mathematical machines. IN: Akademiya nauk UkrSSR. Institut kibernetiki. Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey; Trudy seminara po metodam matematicheskogo modelirovaniya i teorii elektricheskikh tsepey, vyp. 3 (Mathematical modelling and the theory of electrical circuits; transactions of a seminar on methods of mathematical modelling and the theory of electrical circuits, no. 3). Kiyev, Naukova dumka, 1965. 155-162.

Cold-cathode tubes are claimed to have advantages over electromechanical and semiconductor devices in the design of logic circuits for "adaptive mathematical models" which give out a solution of a problem with unknown variables subsequent to its analysis. The advantages over semiconductor circuits are claimed to be the ability of circuits with cold-cathode tubes, such as thyratrons, to give out a high voltage swing in a wide range of ambient temperatures and the possibility of separating input and output circuits.

Guzik, V. F., and O. D. Glukhov. Noiseproof flip-flop circuit with an operating frequency of 1 Mc. Izvestiya vysshikh uchebnykh zavedeniy. Elektromekhanika, no. 8, 1965, 863-873.

By addition of four D9B diodes, two resistors, and two capacitors with ±10% tolerance, the standard B1 module of the Ural-10 computer can be converted to a flip-flop with an operating frequency of 1 Mc. The flip-flop exhibits a high degree of reliability and noise immunity in a hostile environment.

The flip-flop has the following characteristics: output voltage swing, 5—6 v; output pulse rise time, 0.1 μsec; output pulse fall time, 0.15—0.5 μsec; bias voltage tolerance, ±10%; fan-out, 4; temperature range, -10C to +60C. During tests, the operation of the flip-flop was not affected by noise sources located at a distance of 1 m or less. The noise sources were: an operating MKU-48 relay, a 60—90-w soldering iron, an on-off switch of 500—600 w, and two 25-cm wire antennas connected directly to the load circuit of the flip-flop.

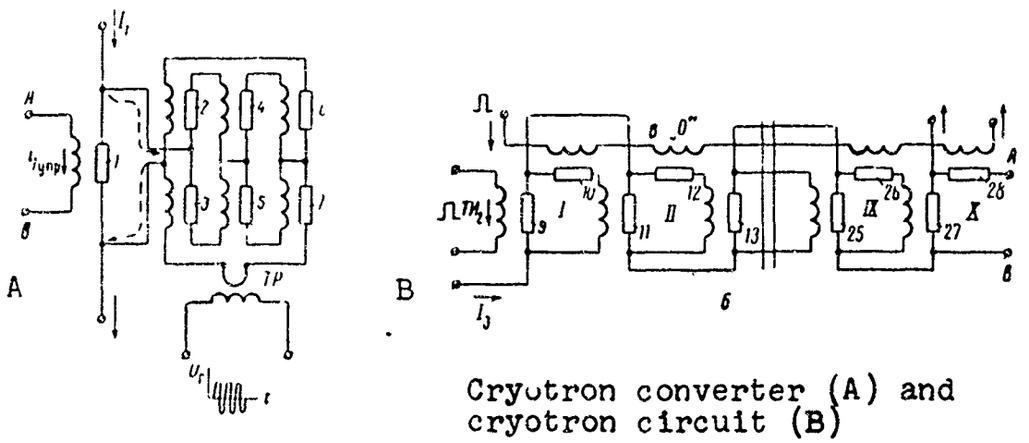
Kan, Ya. S., and V. A. Rakhubovskiy. Multiple-winding cryotron - a universal logic building block. Avtomatika i priborostroyeniye, no. 3, 1965, 33-34.

If an extra bias winding is added to a cryotron with multiple windings, the element may perform logical operations. Depending on the relative direction and the magnitude of the control and bias currents, the modified cryotron may perform OR, EXCLUSIVE OR, AND, NOR, and NAND operations. The last two are the most practicable. A 4-bit adder using 3-winding lead-tin cryotrons was constructed and tested at the Physicotechnical Institute, Academy of Sciences UkrSSR. Adder speed was increased by a factor of two over the normal. The cryotrons used had time constants of 250 μsec at an ambient temperature of 3.6K. The bias and control currents were 250 mamp ±20%.

Kan, Ya. S., and V. A. Rakhubovskiy. Use of a cryotron converter in the testing of cryotron circuits. Avtomatika i telemekhanika, v. 26, no. 10, 1965, 1884-1886.

A cryotron converter has been designed to measure the low difference in potentials during switching of a cryotron wire. The device (see figure) converts the d-c potential difference (10^{-5} v) into an ac voltage with an amplitude of 10^{-2} v, which can subsequently be amplified by conventional means.

The converter consists of a cryogenic oscillator (cryotrons 2-7) placed in parallel with the wire being tested (1). Current I_1 either passes through superconducting wire 1, shorting the oscillator input (no output), or upon application of control current to the cyrotron coil, is directed into cryotrons 2-7, giving rise to oscillations at the output. The amplitude and frequency of these oscillations depend on the magnitude of I_1 and the control current. The converter may be utilized in measurements of basic cryotron-cell time constants and other transient-response parameters of cryogenic circuits.



Cryotron converter (A) and cryotron circuit (B)

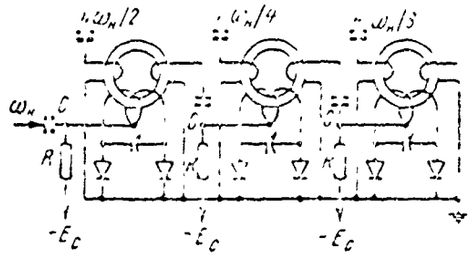
Kirenskiy, L. V., and N. S. Chistyakov. On some practical possibilities of using ferromagnetic tapes at ultrahigh frequencies. IN: Akademiya nauk SSSR. Doklady, v. 165, no. 1, 1965, 81-84.

The properties of ferromagnetic tapes for use in computer memories and uhf technology were tested at 3000 Mc under weak constant magnetic fields by the Institute of Physics, Siberian Branch, Academy of Sciences USSR (Krasnoyarsk). The uniaxially anisotropic permalloy tape samples (17% Fe, 80% Ni, 3% Mo) were prepared by thermal sputtering on a heated (200°) glass base, and the conditions for optimum control were established. If the magnetic field which does the switching is oriented in the easy direction and the intensity of the constant perpendicular field is appropriately chosen, the tape will switch by a shift of domain boundaries in one direction where variation of uhf susceptibility is absent and by rotation of the magnetic vector in another direction where uhf susceptibility varies. To increase the maximum operating frequency of ferromagnetic tapes, the skin depth may be increased if the tape is made of many alternating layers of ferromagnetic metal and silicon monoxide. Thus, a ten-layer tape, with each layer 1000 Å thick, has the same transmission factor as a single-layer tape 2000 Å thick.

Komolov, V. P. Parametron frequency divider circuits. IN: Moscow. Universitet. Vestnik, no. 5, 1965, 89-90.

The proposed parametron frequency divider shown in the figure effectively filters (to 30 db) undesirable pump frequency at the output, preserves parametric oscillations over a wide range of frequencies ($\Delta\omega_p/\omega_p \simeq 0.1$, where $\Delta\omega_p$ is the frequency band of mutual synchronization with the pump frequency), and maintains high efficiency (up to 90%).

The circuit was tested experimentally using a 4-Mc pump frequency and D813 reverse-biased (with -3 v) varactor diodes. The tuning of each stage was accomplished by varying the number of core windings. The output of the first and second divider stages contained undesirable signals which were 25 db down from the desired output. In the third stage, the signals were 30 db down. An attempt to increase the division by the addition of another stage without intermediate amplification proved unsuccessful.



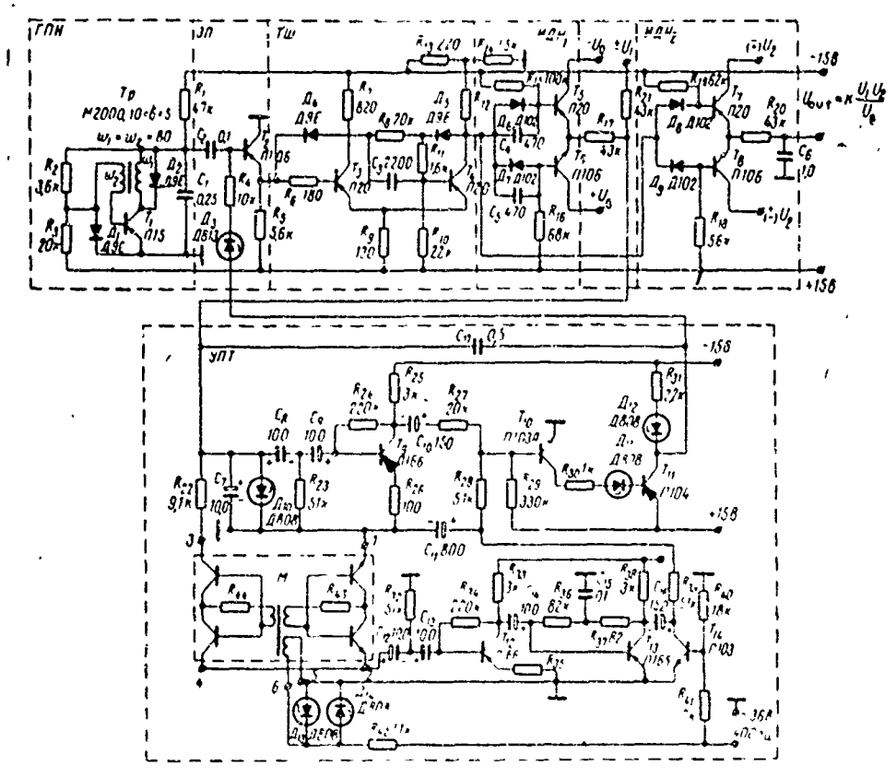
Parametron frequency divider

Petrov, B. K., V. B. Smolov, Yu. A. Tarasov, and Ye. P. Ugryumov. Transistorized precision pulse multiplier-divider. Avtomatika i telemekhanika, v. 26, no. 10, 1965, 1818-1823.

A circuit for multiplying or dividing two voltages is described (see figure). The output consists of a product U_2 and ratio U_1/U_0, which is a linear function of a duty factor of pulses appearing internally as an intermediate quantity in the multiplication-division process.

The circuit is made up of the following stages: sawtooth voltage generator (pulse repetition frequency, 8.5 kc), T_1; emitter follower, T_2; Schmidt trigger, T_3, T_4; clamp circuit, T_5, T_6; voltage divider, R_{21}, R_{17}; bipolar clamp circuit, T_7, T_8; and d-c voltage amplifier (gain, 20,000; zero drift, 0.4 mv) T_{9-14}.

The input voltages U_1, U_2 may be of either polarity in the voltage range from +4.5 to +6.6 v and are confined to the frequency bands from dc to 8.5 for U_1 and 10 cps for U_2. The errors which arise are ascribed to errors in the d-c amplifier, clamp circuits, and the presence of non-zero saturation voltages of the switching transistors. Measurements of relative normalized product error and rms error at +20 and +60C gave values of 0.075% and 0.006% at +20C and 0.125% and 0.01% at +60C.



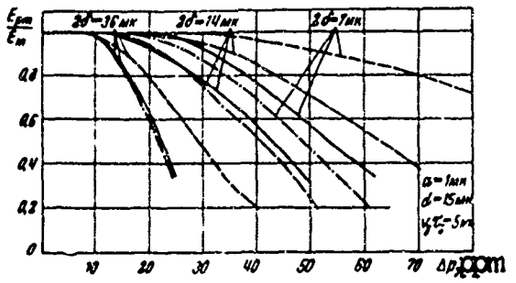
Multiplier-divider circuit

Viches, A. I. Characteristics of the density of magnetic recording of pulsed signals. Radiotekhnika, v. 20, no. 9, 1965, 63-71.

The variation of output signal amplitude of magnetic tape recorder units as a function of bit packing density is analyzed by linear approximation methods. It is established that the characteristic of the recording-reproducing channel depends on head design, spatial and spectral losses, and losses in the recording medium. The amplitude of signals which are directly proportional to induced voltage in the read-head winding show little relation to bit density, as contrasted to signals proportional to flux. The variation of output signals as a function of bit density is influenced more by head-to-surface distance than by recording layer thickness, and gap-length dimensions become important when the gap width is small.

The accompanying figure presents a roll-off curve for different gap width dimensions based on a recording system with a 79 NM permalloy head with gap length of 0.7 μ. Recording pulse duration was equal to the time constant of the

recording head. Pulse amplitude was such that the current in the head winding was equal to 0.3—0.4 of the saturation current. The product of surface velocity and head time constant was 0.4 μ.



Roll-off curve

2δ - Read head gap width (μ); a - head-to-surface distance in μ; d - recording layer thickness in μ.

——— Experimental results
– – – – Results obtained by approximation
-·-·- Results obtained by exact computer solutions

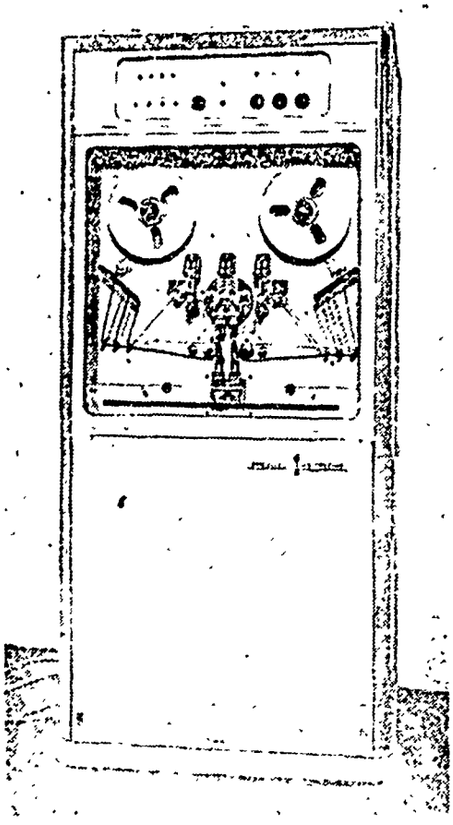
2. Design

Adas'ko, V. I. Amplifier for the photoelectric tape reader of the VNIIET-1 control computer. Priboros-troyeniye, no. 9, 1965, 23-25.

The photoelectric paper tape reader was developed at the All-Union Scientific Research Institute of Electromechanics and is capable of reading 17.5-mm punched tape at 250, 500, or 1000 characters per second. It has two modes of operation; with supply and takeup reels and without. Reel capacity is 500 m. The tape reader is mounted in a cabinet measuring 1500 x 700 x 350 mm. It operates in the start-stop mode and is very reliable. For example, the photodiode-transistor amplifiers are such that an unintended punched hole with a diameter 1/3 of that of the bonafide nole will be ignored by the reader. The reader has been in operation for more than two years.

Adas'ko, V. I., R. R. Pure, and A. N. Fedoseyev. Magnetic-tape transport mechanism for the memory unit of the VNIIEM-1 computer. Elektrotekhnika, no. 11, 1965, 40-42.

The All-Union Scientific Research Institute of Electro-mechanics has developed a tape-transport system for use as an auxiliary memory for the VNIIEM-1 computer. An external view of the system is shown in the figure. The transport system is capable of storing 15 x 10^6 bits on 360-m tape with a width of 12.7 mm. The read-write operation is performed by two separate magnetic heads. Each head has 7 tracks. Recording bit density is 10—12 bits/mm. The use of two heads allows the system to simultaneously record, read, control, and correct the incoming information. The error rate of the system is better than 1 bit in 10^8. The shielding of individual tracks is such that the signal tc noise ratio is 10:1. The start-stop mechanism allows the tape, moving at a speed of 1.8 m/sec, to be stopped in 3 msec and started in 5 msec. Tension arms together with an electronic damping system controlling an asynchronous motor evenly control the tape slack between the reels and capstans.



Tape-transport mechanism

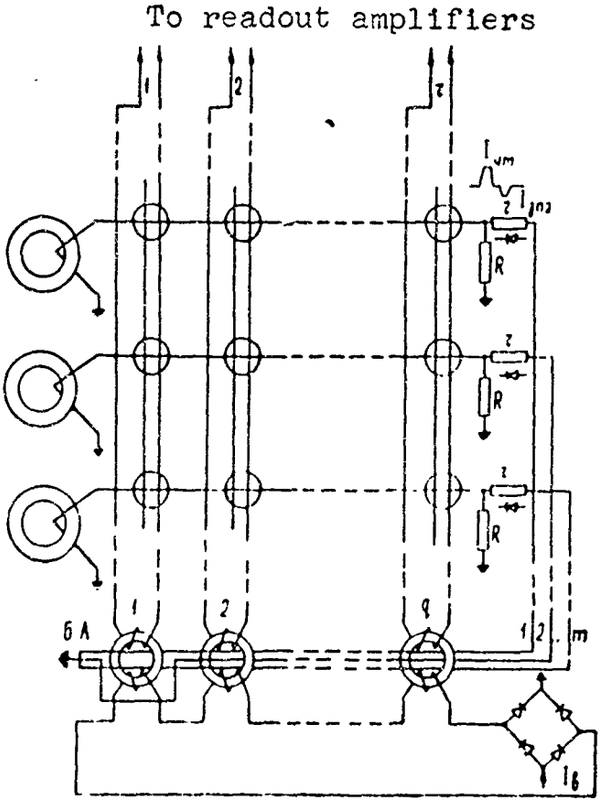
Ambrosovich, V. D., D. A. Kats, and V. Ye. Chernyshev. Permanent storage with four-coordinate selection. IN: Akademiya nauk SSSR. Avtomaticheskiye i teleinformatsionnyye sistemy (Automatic control and data transmission systems). Moskva, Izd-vo Nauka, 1965. 125-130.

To simplify the circuitry of address decoders associated with medium-capacity (10^4 words) permanent storage units of the wired-core type, it is necessary to resort to multicoordinate word selection. The authors describe a magnetic core storage unit using four-coordinate word selection with $N = \sqrt[4]{n}$ (where n is the number of addresses) outputs per each address decoder. A total of six decoders are used. Undesirable pulses due to partial core switching during the writing operation are not amplified by the read amplifiers. A coincidence gate allows the read amplifiers to act only during the read cycle.

Anishin, N. S. Fixed memory combined with working storage. Izvestiya vysshikh uchebnykh zavedeniy. Radiofizika, v. 8, no. 4, 1965, 842-843.

A combination working and permanent storage with one core per bit is described. The permanent storage is made up of q ferrite cores, each with one readout winding and m read windings, as shown in the figure. Each read winding also acts as one of m word address lines for the working storage. The address, thus, is common to both storages, so that the information read with a particular address may be from either.

To read out information from the working storage only, current I_B is applied to prevent flux reversal in one or all the q cores of the permanent storage. To read out the contents of the permanent storage only, current I_B is removed, and a pulse current (I_0) is sent on one of the address lines. This readout is nondestructive for the working storage. The working storage may be converted into permanent storage by replacing the resistors with diodes and connecting a current-limiting resistor r between points A and B. Point B is either grounded or made negative.

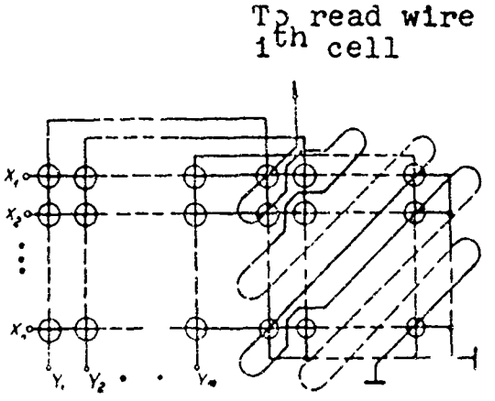


Combined storage

Anishin, N. S., and G. G. Rekus. Principles for combining working and permanent memory units. Izvestiya vysshikh uchebnykh zavedeniy. Priborostroyeniye, v. 8, no. 5, 1965, 68-71.

Address registers, decoders, read amplifiers, and in some cases output registers may be utilized in common by both working and permanent magnetic core memory units. For memory units with linear word selection, the permanent memory is integrated in the working storage by wired-core methods using one or two cores for each output bit (in the working storage, the compensating cores are laced according to a ones complement code) or one core for each output word.

For coincident-current type working storage, the permanent memory core wiring is done according to a ones complement code because of the peculiarity of the drive winding operation. Two or more permanent memories may be integrated into one working storage as long as the word address contains an additional indicator to avoid ambiguity. Integration for coincident-current type storage is shown in the figure. The cores of the $(r + 1)^{th}$ matrix containing permanently stored information are normally biased in one direction and are not affected by the read and write cycles of the working storage — $(r)^{th}$ matrix. To read the permanently stored information, zeroes must be written into every bit plane of the working storage and a half-select current applied simultaneously to the permanent memory cores.

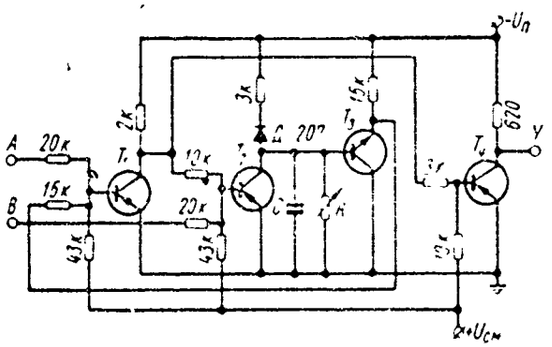


Arrangement of read lines in matrix-type memory unit

Blinder, M. I. Memory and time-delay logic elements. Priborostroyeniye, no. 9, 1965, 8-10.

Three semiconductor logic circuits which operate in ambient temperatures of 0—80C with bias voltage variation of +25% are described. The memory circuit, shown in the figure, follows the equation $Y = (AY) + \bar{B}$, where Y is the output, A is the set input, and B is the reset input. A parallel RC circuit allows this element to maintain its state even when the supply voltage is unregulated or completely removed for as long as 2 sec.

The other two circuits are three-transistor monostable multivibrators with a delay of $T_d = RC \ln 2$. One circuit delays the 0 to 1 transition and the other, the 1 to 0 transition. The maximum delay is 10 sec, and the error in the worst temperature and bias-variation environment does not exceed ±5%.



Memory logic element

U_n (supply voltage) = -6 v;
U_{om} (bias voltage) = +6 v.

Kochetov, A. Ye. Design of a magnetic-core decoder matr Priborostroyeniye, no. 8, 1965, 4-6.

An approximate design method for a magnetic-core addres decoder of the type used in the BESM and Kiev computers is described. Formulas are given for determining the required number of windings and the cross section of the core for a given switching current, signal-to-noise ratio, load resistance, mean toroidal radius, and switching time.

Komolov, V. P. Multistable parametrons. Avtomatika i telemekhanika, v. 26, no. 11, 1965, 2012-2018.

Single- and double-tuned, balanced and unbalanced parametrons with multiple stable states were tested to determine their suitability as high-speed computing elements in ternary computer systems and automatic control. The test results are shown in the table. The best results (highest number of stable states) were obtained by using low-loss matched Zener diode pairs (D808 - D813) and exact tank tuning by optimization of the number of parametron coil windings. Speed of switching from one stable state to another was increased twofold when the switching was effected by modulating the diode back bias rather than changing the pump signal amplitude.

Test results

№	A,B	n	f_p	f_0	Δf	$\Delta\varphi$	E	Ap	A_0	Φ	r	f_M	A_s	$\Delta\varphi_s$	m	M	D	σ	η	t
1		2	6	3	800	π	2	4	0,5	15	10	40	10^{-3}	25	1	20	DGTS 23	10^{-3}	2	1
		2	6	3	600	π	2	4	2	30	3	60	10^{-3}	30	1	40	813	10^{-1}	2	1
2	A	3	3	1	200	2π/3	4	5	1,5	14	12	10	10^{-3}	15	1	20	205	$3\cdot10^{-3}$	1	2
		4	4	1	120	π/2	5	7	1,5	12	12	10	—	—	1	20	205	$8\cdot10^{-3}$	1	2
		5	5	1	60	2π/5	5	10	1,5	10	15	6	—	—	1	20	205	$5\cdot10^{-3}$	1	2
	B	4	4	1	300	π/2	5	10	1	12	40	3	—	—	1	20	205	$2\cdot10^{-3}$	1	2
3	A	3	3	1	120	2π/3	1,5	4	1	25	10	10	—	—	1	30	813	$5\cdot10^{-3}$	2	2
		4	4	1	40	π/2	2	2	0,5	25	12	10	—	—	1	30	813	10^{-3}	2	2
	B	4	4	1	70	π/2	1,5	4	1	25	30	4	—	—	1	30	813	$2\cdot10^{-3}$	2	2
4	B	4	4	1	200	π/2	2;0	6	1,5	30	35	3	—	—	2	—	813	10^{-1}	4	2
		8	4	0,5	80	π/4	3;1;0	6	1,2	30	100	1	—	—	3	—	813	10^{-1}	6	3
5	A,B	6	3	0,5	100	π/3	5;0	6	0,8	25	45	2	—	—	2	—	205 813	10^{-3}	3	3
		8	4	0,5	30	π/4	5;0	10	0,5	25	50	2	—	—	2	—	205 813	$5\cdot10^{-3}$	3	3
		10	5	0,5	20	π/5	6;0	15	0,3	20	70	1	—	—	2	—	205 813	10^{-3}	3	3

1 - Single-tuned balanced parametron; 2 - double-tuned unbalanced parametron; 3 - double-tuned balanced parametron; 4, 5 - cascaded parametron stages.

A - Mutual synchronizing mode; B - serial activation mode; n - number of stable states; f_p - pump

frequency (Mc); f_o - operating frequency (Mc); Δf - synchronization band (kc); $\Delta\varphi$ - interval between stable phases (rad); E - diode back bias (v); A_p - pump signal amplitude (v); A_o - amplitude of carrier-frequency signal (v); Φ - pump signal attenuation (db); τ_r - oscillation envelope rise time (μsec); f_m - maximum switching frequency (kc); A_s - control signal amplitude (v); $\Delta\varphi s$ - control signal phase deviation (deg); m - minimum number of inputs; M - maximum number of inputs; D - diode type; σ - allowable rms magnitude of noise in 9-kc band (v); q - number of diodes; ℓ - number of tuned circuits.

Levinskiy, L. S., and A. N. Tsukhay. Construction methods for memory systems with a single write-in of repetitive information. Nauchno-tekhnicheskaya informatsiya, no. 7, 1965, 31-33.

A description is given of an associative memory system providing a single write-in of repetitive information without auxiliary programs. The storage is in the form of a pyramidal binary decoder which permits writing of N words, whose first m bits are similar, into m storage locations instead of N·m locations.

In addition to the main storage, the system contains read and write registers and an end-of-operation register. The memory elements store three values: 1, 0, and an "end-of-word" symbol. Both readout and write-in are accomplished by the coincidence of information and control pulses. The end-of-word symbol permits the use of words of variable length.

The memory unit is suitable for automatic computer translation systems, automatic written text recognition systems, and analysis of nuclear particles.

News in computer engineering. Nauka i tekhnika, no. 10, 1965, 15.

The ATE-80 digital computer with alphanumeric input/output was recently put into service at the Computing Center of the Directorate of Statistics of the Latvian SSR. The primary task of the computer is the preparation of a monthly composite picture of statistical indexes showing the degree of fulfillment of economic plans, growth rates, and manhour productivity for Riga and the rest of the Latvian republic.

The ATE-80 supersedes the much slower EV-80 computer. The new computer can store up to 1024 12-digit decimal numbers, and as a result of its simple organization, it is capable of solving problems requiring a large quantity of input data. Programs are introduced into the machine with the aid of perforating or tabulating units. Output may be either in the form of punched cards or tabulated alphanumeric information printed out with the speed of 150 or 300 characters per min.

Salum, Kh. Language for describing and modelling the operation of structural digital circuits (TsIMOD). IN: Akademiya nauk Estonskoy SSR. Seriya fiziko-matematicheskikh i tekhnicheskikh nauk, v. 14, no. 3, 1965, 464-471.

A new computer language — TsIMOD — has been developed to facilitate the computerized design of digital computers. The language is such that a new modelling program is not required for each different digital circuit design problem. The majority of the symbols are similar to those used in the ALGOL-60 language. The basic symbols are alphanumeric characters and other common symbols describing different micro-operations. The complete Cyrillic and Latin alphabets are utilized, with similar symbols separated by a number to avoid ambiguity. To illustrate the efficiency of TsIMOD, an example is cited in which an interpretational program for the M-20 computer utilized 2000 cells plus 200 working cells and constants. Storage of micro-operands, which vary the digital computer structure, utilized another 240 cells. The time for the execution of one command was 1.5 sec.

3. Applications

Bazilevich, F. V., and L. L. Orlinkov. An experiment in constructing a descriptor-type information retrieval system using superposed punch cards. Nauchno-tekhnicheskaya informatsiya, no. 9, 1965, 22-27.

An improved document retrieval system based on descriptor indexing and punch-card superposition is discussed. The system is conceived as a complement to the widely-used Universal Decimal Classification System (UDC) and is intended to avoid some of the latter's shortcomings. A specific claim is that the new system, using an address breakdown several orders greater than that of the UDC, could retrieve information equally as fast. The language is a combination of UDC plus a descriptor dictionary, and by using 20,000-entry punch cards, the necessary number of sub-groupings need not exceed 45.

Some trial storage has been accumulated from an existing card index, using the following groups: Resistors (1600 documents); Transformers (1700 documents); Electromagnetic Oscillators (5000 documents) and Amplifiers (10,000 documents). In addition to these entries, the system includes an address card file, a perforator, and a scanning device. Sample results of the trial system to date are as follows: response time to a broad generic request (1 or 2 descriptors only) yielding 100 documents, 42 min; response to a more specific request (6 or 7 descriptors) yielding 4 documents, 7—8 min. To illustrate the comparative improvement in retrieval, the authors point out that an existing card index of some 500,000 entries, with an annual turnover of 100,000 entries, requires a staff of 13 engineers, 6 technicians, and 7 assistants to process an average of 5 requests a day. With the new system, 50 requests a day could be handled by a team of 5 engineers and 5 assistants.

Ibragimov, I. I., K. G. Garayev, and F. Kh. Niyazov. Information processing of complex alphanumeric texts. Byulleten' tekhniko-ekonomicheskoy informatsii, no. 9, 1965, 42-44.

Two computer input/output units are described. The PUVVI-92 printer is capable of simultaneous transfer of information to the computer and hard-copy printing. It also prints the computer output. The printer has 31 Cyrillic and 13 Latin characters, 10 numbers, and 38 auxiliary characters. Printing speed is 8—9 characters per sec. Maximum number of characters per line is 160.

The second unit, the KSU, consists of tape perforator, alphanumeric printing unit, readout unit (capable of simultaneous readout from two tapes), and control panel. It can be used as a tape preparation unit for telegraph communication. The tape may be perforated according to 5-unit, binary-decimal, or octal codes. Fifty-five different characters can be printed at a speed of 10 characters per sec. The ambient temperature and humidity variations should not exceed +5—+50C and 65 ±15%.

Vaynshteyn-Kovalevskiy, G. Ye., A. A. Gordinskiy, L. M. Liberzon, and A. B. Rodov. Simulation of control systems with highly inertial objects on the Analog pneumatic computer. Priborostroyeniye, no. 11, 1965, 22-23.

The Analog pneumatic computer was developed by the Kharkov Teploavtomat Plant in cooperation with the All-Union Central Scientific Research Institute of Complex Automation. It is capable of solving ordinary differential equations and simulating control systems with time constants up to 20 min. The machine operates on a unified pneumatic signal (0.2 to 1 kg/cm^2) and consists of the following blocks: 1) a linear decision block with three integrators, four adders, and two setters, capable of solving differential equations up to the third order, including coefficients, in an interval of 10 to 1200 sec; 2) a delay block (delay time, 16—1200 sec); 3) a block of constant coefficients; 4) a block of nonlinearities for obtaining nonlinear functions of single argument; 5) a control and power supply block; and 6) a two-channel recording unit.

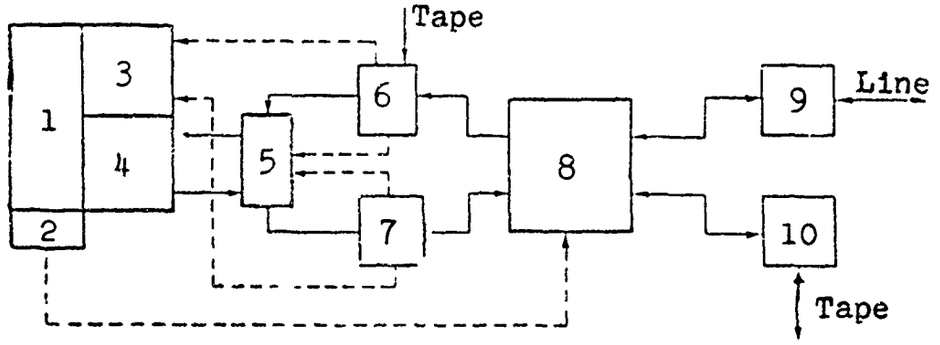
The accuracy of the Analog is 3—5% error for sixth-order differential equations with time constants up to 300 sec and 6—10% error with time constants of 300 to 1200 sec. The computer was used in optimization studies of a catalytic reactor. It was found to be very suitable.

Zaytsev, N. G., V. A. Lebedev, and A. B. Tyakhti. Interfacing of a telegraph channel with the Minsk-1 computer. IN: Akademiya nauk SSSR. Izvestiya. Tekhnicheskaya kibernetika, no. 5, 1965, 163-168.

Additional equipment designed to adapt the input-output unit of the Minsk-1 computer to slow-speed (50-baud) telegraphy is described. The Minsk-1 input format was previously confined to numerical characters, but may now be alphanumeric.

Translation from the telegraph code into the machine language and vice-versa is accomplished by programming methods. The information exchange between the telegraph subscriber and computer may be direct (in real time) or it may be stored on perforated tape as an intermediate step.

The interface block diagram is shown in the figure. It includes a tape reader-perforator (10), calling (dialing) unit (9), switching block (8), input and output blocks (6, 7), buffer register (5), and program-interrupt unit (3). The primary information flow is indicated by solid lines; broken lines indicate control signal paths. The computer control unit (2) determines whether the computer is to be linked with the telegraph channel or tape reader-perforator via the switching block. The buffer register performs serial to parallel conversion when the information flow is from the telegraph to the computer. The output unit causes the information output from the computer to flow into the buffer register, where it is converted from parallel to serial mode. The buffer storage and program-interrupt units serve to neutralize speed differences between the computer and the telegraph equipment. During output, the results of computation are sent to the slow-speed telegraph line, and between each character the computer returns to the main program in order to utilize the available time for other computations.



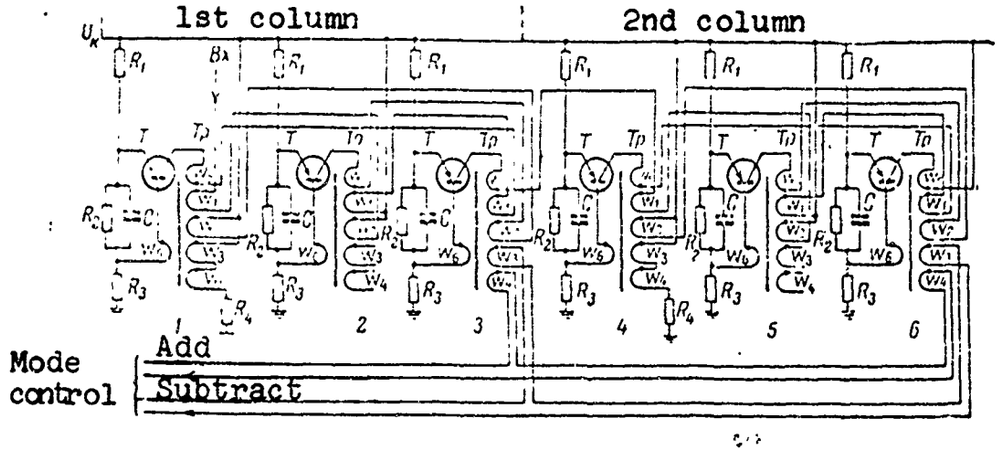
Computer-telegraph interface

1 - Computer; 2 - control unit; 3 - program-interrupt unit; 4 - buffer storage; 5 - buffer register; 6 - input block; 7 - output block; 8 - switching block; 9 - calling (dialing) unit; 10 - tape reader-perforator.

4. Associated Systems

Chistyakov, B. V. On a method of constructing a reversible binary counter with ferrite-transistor elements. Elektrosvyaz', no. 10, 1965, 77-79.

An improved reversible binary counter based on ferrite-transistor cells is described. It features a small number of circuit elements while providing high-speed operation, high reliability, and simplicity of reversal. Each binary column has three cells, consisting of a P-15 triode amplifier and a six-winding transformer on a type FT-5 square-loop ferrite core. A two-bit schematic is shown in the figure. Pulse timing diagrams for the addition and subtraction modes are given. Design data of a 5-digit counter are included. Built by the author, it has worked reliably at frequencies of up to 100 kc over an ambient temperature range of -40 to +50C with supply voltage variations of 20%. Author Certificate No. 167372 has been granted for this design (Byull. Izobr., no. 1, 1965).



Reversible counter

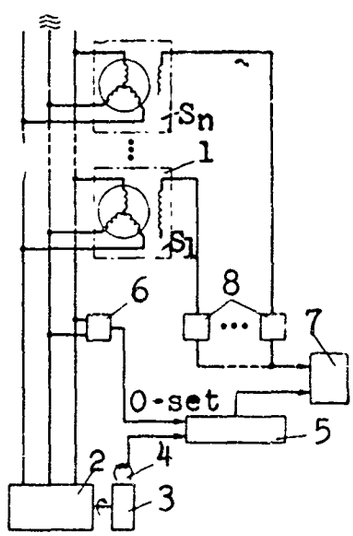
w_1 - Write; w_2 - inhibit; w_3, w_4 - magnetization level; w_5 - output; w_6 - base.

Glazov, M. N. Converter of voltage to shaft rotation angle and digital code. Izvestiya vysshikh uchebnykh zavedeniy. Priborostroyeniye, v. 8, no. 5, 1965, 75-79.

An experimental shaft encoder is described which is designed for analog-digital conversion in a feedback control circuit. The feedback signal is developed in the usual fashion by a stepped output motor, which positions the encoder shaft via a reducer. The experimental encoder used is a linear potentiometer with $\pm 160^\circ$ rotatability; encoder output is displayed on two decatron counters. For an error signal developed by the system within the limits of ± 250 mv, the statistical encoder error is not worse than 1%. Error threshold sensitivities of 10 mv and less are stated to be attainable, and satisfactory operation is maintained at power supply voltage and frequency deviations of $\pm 15\%$.

Gorokhov, L. P. Multichannel angle-code converter. Priborostroyeniye, no. 9, 1965, 29.

A multichannel angle-to-code converter is described. The converter (see figure) does not utilize the usual parallel-to-serial conversion nor a large quantity of pulse generators. Selsyns S_1, S_n are powered by generator 2. Pulse generator 3, driven by the power generator shaft, gives out a fixed number of pulses to sensor 4 for every 360° of rotation of the common shaft. The pulses from sensor 4 are applied to counter 5, which is reset by shaper 6 for each 180° change of phase of the generated voltage. Gate 7 allows shaper 8 in conjunction with the counter to enter the digital equivalent of an angle of turn of a selsyn into the computer. The system takes on an even simpler form if the computer memory consists of a magnetic drum; in this case, the drum rotation and power generator 2 are synchronized.

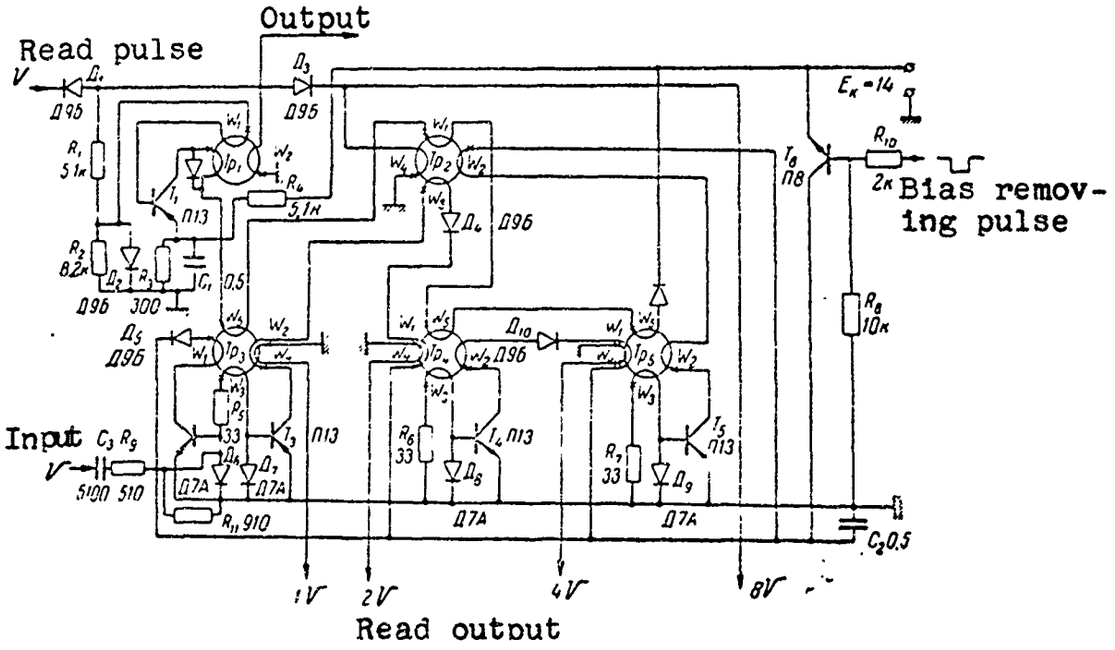


Multichannel converter

Granitskiy, L. V., A. F. Neyermolov, and V. Ye. Nosov. Decade counter with ferrite-transistor element. Geomagnetizm i aeronomiya, v. 5, no. 5, 1965, 958-960.

A decade counter with three ferrite-transistor flip-flops and one four-winding core with rectangular hysteresis loop is described. As seen from the figure, the Tp_2 core switches into the 1 state at the count of 8. The ninth and tenth pulses alternately switch the first flip-flop (Tp_3) into the 1 and 0 states. Winding W_2 of Tp_3 transmits this transition to core Tp_2 and switches it into the 0 state. The pulse emanating at this time from Tp_2 winding W_4 triggers the blocking generator (T_1 and Tp_1), which resets all the flip-flops.

The counter functions in the ambient temperature range of -30C to +55C. The bias voltage E_k may vary from 9 to 22 v without without affecting the operation of the counter. The limiting counting frequency is 30—50 kc under normal conditions and 25 kc at +55C. Reliability is increased by including 51-ohm resistors in the transistor collector circuits.



Decade counter with ferrite-transistor elements

Grebenshchikov, V. N., and V. O. Krichke. Register with analog-digital converter. Priborostroyeniye, no. 9, 1965, 10-12.

A description is given of a system capable of sensing negative slowly varying voltages between 0 and 15 v, converting them into a two-digit decimal number between 0 and 99 with an accuracy of 1%, and printing the results on the EUM-23 typewriter, all in 2 sec. The system uses relays to accomplish the logical functions needed in the comparison of the analog sample to the reference voltages. The conversion from binary to decimal numbers needed for the printout is also done by the same 16 relays. The system is comparatively slow but it has the advantage over other systems of the same type in that if one or more relays malfunctions or the comparator circuit fails, the typewriter will not print.

Karmazinskiy, A. N., and V. M. Nemchinov. Unitron counter. Izvestiya vysshikh uchebnykh zavedeniy. Radiotekhnika, v. 8, no. 4, 1965, 489-495.

An experimental direct coupled transistor logic counter using unitrons (field-effect transistors) is described. A block diagram is given in Fig. 1, and Fig. 2 is a schematic for two digits of a ring counter. In the absence of storage elements, the delay function in counting is provided by auxiliary trigger FET's (T_1^1, T_2^1 ... in Fig. 1). Tabulated results are given of the range of tolerance in circuit parameters for a counter operating at 18C and 40C. Operation was reliable over a 15% variation in supply voltage and a 10% variation in resistor values. Speed of operation was a limiting factor, being in this case only 25 kc. An advantage cited is the low power drain, due to the fact that in the unitron counter only two triggers are on at any given moment; the tested counter required only 40 mw.

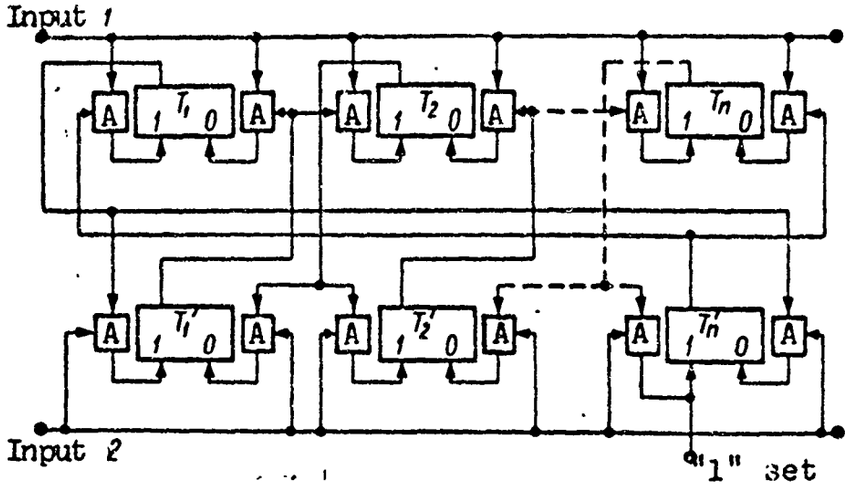


Fig. 1. Unitron ring counter

A - AND gates; T - triggers.

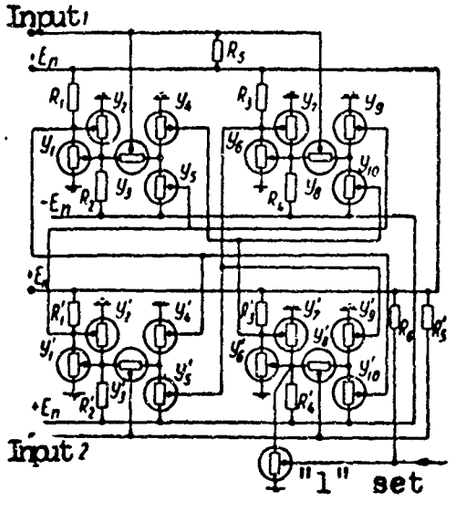


Fig. 2. Two digits of ring counter

Kneppo, P. L., A. A. Mozheyko, and V. F. Semenov. High-speed transistorized voltage-to-code converters. Priborostroyeniye, no. 8, 1965, 12-14.

A description is given of two analog-to-digital converters with ranges of 9.999 v and 10.2375 v and resolving capabilities of 1 mv and 2.5 mv, respectively. Conversion speeds are 3 μsec and 0.15 μsec; absolute error is $\pm(0.02\% U_X + 1)$ and $\pm(0.05\% U_X + 2.5)$, where U_X is the analog voltage to be converted.

Both models operate on the principle of successive comparisons. The 16 or 12 flip-flops (depending on the model) generate a voltage U_y, which is compared with U_x; the outcome of the comparison changes the flip-flop states, which in turn generate another U_y, which is again compared with U_x. The process continues until U_y does not differ from U_x by more than the lowest order binary digit or the sensitivity of the differential amplifier which is used as a comparator block. The differential amplifiers in the two models have a drift of 50 μv/C and 100 μv/C with common mode rejection capabilities of 50,000 and 10,000 (voltage ratio). The first converter is designed for operation in the temperature range of 15—35C, and the second, in the range of -20 to + 4C. Tolerable power line voltage unbalance is ±10% for both models.

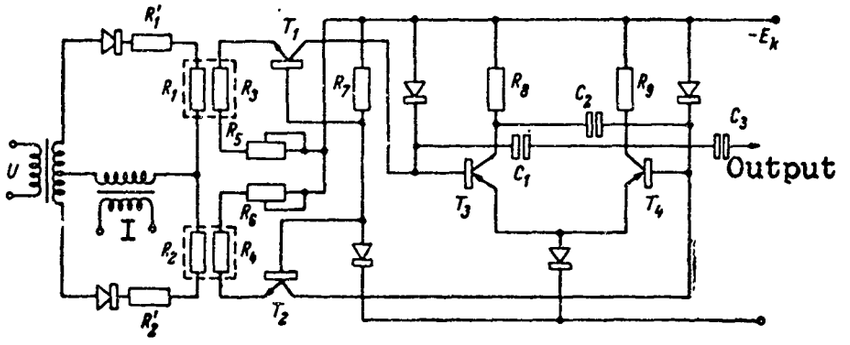
Levshteyn, M. I. Production technique for edge-punched cards. Reprodutsirovaniye dokumentov, no. 6, 1965, 39-41.

At present, there are only two main Soviet production centers for the manufacture of edge-punched cards: the All-Union Institute of Scientific and Technical Information, with a capacity of 10.5—11 million cards per year and the Central Bureau of Technical Information, with a capacity of 27 million cards per year. The printing and edge-punch coding of cards, whether by offset or with a flat press, do not allow the full utilization of the card for edge coding; only three edges are punched.

A new method suitable for coding and printing of abstracts on a card is described. The typesetting master after it has been used for printing an abstract is inserted into a metal frame with holes which are filled by special metal inserts. The position and type of inserts (3 types) correspond to the desired information coding. The time needed to compose one card is 2—3 minutes. This form is then mounted in a crucible machine and a blank card is edge-punched and typed simultaneously.

Shaposhnikov, R. D. Some features of information input and conversion in real time in centralized control systems. IN: Akademiya nauk SSSR. Avtomaticheskiye i teleinformatsionnyye sistemy (Automatic control and data transmission systems). Moskva, Izd-vo Nauka, 1965. 130-136.

A description is given of a converter operating in real time which converts the effective power of a single-phase source into a stream of pulses whose period is a linear function of the input power. The circuit (see figure) uses two transformers (one for voltage, U; the other for current, I), and two pairs of thermally coupled resistors working in conjunction with a current-controlled astable multivibrator. The characteristic of the thermally coupled resistors is such that their resistances vary as the square of the sum and difference of currents, which in turn depend on the measured power. The changing currents passing through T_1 and T_2 control the period of the astable multivibrator in a linear fashion.



Real-time converter

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Appendix: Homogeneous Microelectronic Structures for Computer Circuitry

SUMMARY: A new concept involving the utilization of homogeneous microelectronic computer elements (equistors) to perform logical and computing operations is reviewed. It is shown that the group of elements can, upon command, perform any logical operation. A comparison between this concept and that of the neuristor is made.

The recent trend in large-scale computer design is toward the greater capacity, reliability, and flexibility required by the increasing complexity of problems requiring computer solutions. Component miniaturization offers the most natural means of coping with these problems, and devices belonging to the microelectronic family have such inherent advantages as increased speed and reliability independent of the number of components. The latter makes it feasible to design systems using majority logic and redundancy methods [2].

On the other hand, miniaturization, though offering substantial benefits, is not without its problems, particularly with regard to wiring and interconnecting of integrated circuits. The size of the leads interconnecting individual modules cannot be reduced beyond a certain practical limit. Interconnections play a major role in signal attenuation, and in addition the reliability of overall systems is influenced by the reliability of connections. Such problems have prompted a search for methods which would fully exploit the advantages of microelectronic circuits while circumventing their disadvantages. One possibility is the use of homogeneous systems, which make use of different groupings of modules of a single type to perform any logical operation [2].

The homogeneity requirement has led to a re-examination of the accepted methods of synthesis of logical nets and has given rise to new methods, reflecting the special features of this type of system. Thus, the iterative circuit computer (ICC) has been proposed [3], employing a multilayer structure formed with single-type modules which upon external command may act as an accumulator, register, memory, or connecting line. In comparison with ordinary computers, the ICC achieves greater speed, simplicity of programming, and computing accuracy. It is capable of efficiently dealing with problems involving spatial relationships between variables. One drawback of the ICC is the complexity of the module structure, which requires external control.

Two other concepts — the neuristor [4;5] and the equistor [2;6] — utilizing the collective interaction of a group of elements with minimum outside control have also evolved. Systems based on these concepts behave similarly to biological systems, particularly, the nervous system.

The neuristor, a U. S. innovation, and the equistor, the result of Soviet efforts, have much in common with the action of the pulse-propagating portion of a neuron called the axon. The axon permits attenuation-free propagation of an ionic discharge wavefront moving at a "characteristic" velocity of 1—100 m/sec [5]. As the wavefront passes a given point, it causes the release or discharge of chemical potential energy in the form of separated ion concentrations stored at this point. Following the passage of a pulse, a refractory period of a few milliseconds occurs, during which the axon "heals" itself by restoring the discharged energy to some minimum level. Since the discharge can be initiated only when a certain level of stimulability has been exceeded, it is impossible to initiate a discharge wave during the refractory period.

Neuristors and equistors possess the following common properties, analogous to those of the nerve axon: 1) threshold stimulability, 2) attenuation-free propagation, 3) uniform velocity of propagation, and 4) a refractory period following the passage of a discharge past any point.

The equistor is a ramification of the neuristor concept and was developed by the Institute of Automation and Telemechanics of the Soviet Academy of Sciences. The system uses homogeneous elements to perform logical functions [2]. This system, unlike the neuristor networks, is able to perform all logical operations with a set of single-type stages, each composed of a flip-flop and associated gates with noncommutating interconnections between the stages.

The equistor networks are arranged in symmetric rectangular grids as shown in Fig. 1. The logic operations are effected by interaction between propagating pulses, i.e., by head-on collision or perpendicular crossing of the information streams. As in neuristor networks, the result of the interaction of two or more moving pulse streams may be mutual annihilation, mutual penetration, or inhibition of one such stream by the others and vice-versa.

The basic equistor cell may be in one of the two states: active ("1") or passive ("0"), depending on an external signal or a signal from an adjoining cell. In synchronous systems, the active state lasts for a time

interval equal to a whole number of clock pulses, after which the cell reverts to its initial passive state (following the refractory period), giving

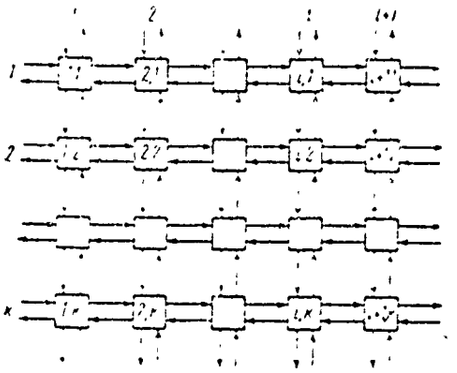

Fig. 1. Equistor network

out a signal to one or more neighboring cells. The refractory period and the velocity of pulse propagation are determined by the system clock rate. Since the cells are triggered into the active state only when the trigger signal exceeds a certain level and since pulse regeneration takes place in every cell, the properties which satisfy neuristors also hold for equistors.

The external control signals, applied only to information input cells, determine the direction of signal flow. The direction of signal flow from cell to cell for other types of cells is accomplished either by activation with outside pulses which have a particular phase relationship to the clock pulses or by sequential activation of two successive cells.

Fig. 1 illustrates cell operation. It is assumed that cell (i, k) is triggered in synchronism with the clock pulse. The cell remains in the active state for duration $t = a\tau$, where a is a whole number and τ is the clock-pulse duration. When a preset number of clock-pulse periods have elapsed, the cell will regress to the passive state. It may be triggered again only after the refractory period ($t_r = b\tau$, where b is a whole number) elapses. The time delay function is automatically realized as the pulse progresses from cell to cell in the equistor network structure.

The INHIBIT, NOT, and NOR operations can be performed with the equistor circuit under the following operating conditions: 1) The direction of signal flow is achieved by sequential activation of two

successive cells. 2) The entire cycle time for one cell lasts four clock periods (4 τ): activation time τ, active state ("1") 2 τ, and refractory period τ. 3) If two information streams intersecting at a particular cell location arrive simultaneously, they penetrate each other's paths without affecting one another. If, however, they arrive at different times, they are mutually inhibited.

In order to direct the information flow from cell $(i + 2, k + 2)$ in Fig. 2 to the right, external control pulses (dark dots) are applied in succession (staccato fashion at clock rate) to cells $(i + 2, k + 2)$ and $(i + 3, k + 2)$, after which the information progresses to cells $(i + 4, k + 2)$, $(i + 5, k + 2)$, etc. If it is desirable to branch out from cell $(i + 4, k + 2)$ downward, it is only necessary to apply a control pulse to cell $(i + 4, k + 3)$ τ seconds after cell $(i + 4, k + 2)$ is activated. All other directions are similarly accessible.

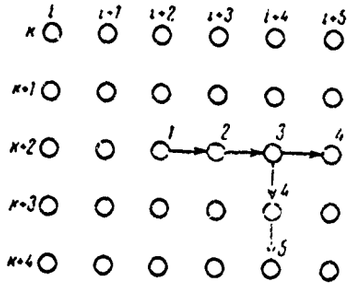

Fig. 2. Propagation direction control and branching

The INHIBIT operation is illustrated in Fig. 3. Information flow A, whose position for successive clock periods is indicated by a number next to a particular cell, arrives at cell $(i + 3, k + 2)$ two periods later than stream B, which at that same instant has already reached cell $(i + 5, k + 2)$. Since their arrival at cell $(i + 3, k + 2)$ is not synchronous, the signals are mutually inhibited, as shown by stream $A \cdot \bar{B}$ propagating upward and $\bar{A} \cdot B$ propagating to the right.

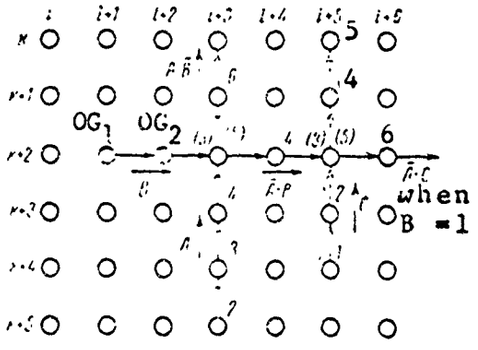

Fig. 3. Realization of INHIBIT, NOT, and NOR operations

For NOT and NOR operations, it is necessary to utilize one generators (OG), which are externally activated cells with strobing periods equal to 4 τ. If stream B in Fig. 3 is formed by two one generators placed as shown in cells $(i + 1, k + 2)$ and $(i + 2, k + 2)$, giving rise to signals (111...1) propagating to the

right, the signal at cell $(i + 4, k + 2)$ is $\bar{A} \cdot B$ $(B = 1)$, or $\bar{A}$; i.e., the NOT function is realized. If in addition a stream C is directed upward along column $(i + 5)$ with timing corresponding to the indicated numbers, then at cell $(i + 6, k + 2)$ the signal $\bar{A} \cdot \bar{C} = \overline{A + C}$ $(B = 1)$ is observed. Since this operation is a general NOR operation, all other logical operations may be similarly realized.

The ability of the signals to penetrate each other's paths if they arrive at a particular location simultaneously is characteristic for equistor structures and gives them operational flexibility. Memory elements may be made from 10 equistor units, 5 of them acting as one generators. Storage would be of the circulating type, circulating the stored bit in a rectangular path.

Another of the important features of equistor networks is that one and the same section of the homogeneous structure may be utilized to perform different operations, depending only on external control signals. Also, the same operation may be achieved by more than one method, and some complex logical operations are realized by more efficient methods than by dividing the operation into elementary logical steps.

Because of their characteristic homogeneous structure, equistor networks, unlike neuristors, lend themselves to easy application of redundancy methods at the block or even element level. The homogeneity of cells also makes it possible to apply adaptive principles. For example, a particular cell or an aggregate of cells may, if the situation warrants it, take over the functions of adjoining cells in case the latter fail to perform their assigned tasks. Neuristor networks on the other hand cannot readily be interchanged at the element level, since neuristors are not structurally homogeneous [4].

Neuristors, however, have less interconnections between basic junctions and blocks of junctions than equistors, which, in order to ensure operational flexibility, rely on control signals, which in most cases convert particular cells into one generators. The minimum number of control interconnections in equistor networks (grids) is one per each row and column. Control is accomplished by the selection of a particular cell and by appropriate signals converting the given cell into a one generator.

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