A SUMMARY OF SURFACE EFFECTS OF RADIATION
ON SEMICONDUCTOR DEVICES

by

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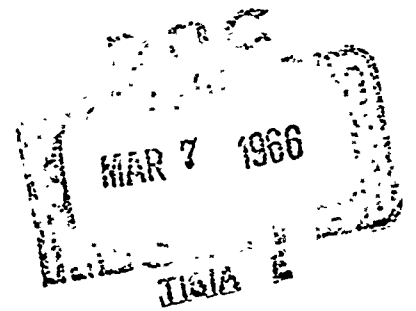
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ABSTRACT

A brief review of surface physics is given as background for the subsequent discussion on the role of surfaces in the behavior of semiconductor devices. The effects of channels and surface generation-recombination on p-n junctions and transistor characteristics are discussed.

The observed effects of ionizing radiation on nonpassivated, gas-filled transistors are interpreted in terms of a model in which ions formed in the gas ambient deposit charge on the device surface. The resultant surface charge buildup creates channels on the device surface which cause a decrease in h_{FE} and increase in I_{CBO}. Saturation, recovery, and the effects of dose rate and bias are also discussed.

Degradation of planar passivated transistors and other devices employing SiO_2 layers due to radiation is similar to that observed for nonpassivated devices. Surface charge buildup affects the device surface and leads to degradation. The bulk of experimental evidence points to accumulation of positive charge at the SiO_2-Si interface as the cause of degradation. Several possible means of charge buildup at the interface are discussed. However, the process responsible has not, as yet, been identified.

The direction of future experiments is discussed, particularly of those experiments which may yield information about the part played by radiation in positive charge accumulation at the SiO_2-Si interface.

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A SUMMARY OF SURFACE EFFECTS OF RADIATION ON SEMICONDUCTOR DEVICES

1. INTRODUCTION

When a semiconductor is exposed to nuclear radiation, two basically different effects may occur. First, the radiation will cause ionization through one of a number of electronic excitation processes. Second, if the radiation energy exceeds a threshold value (~0.5 - 500 keV, depending on the nature of the irradiating particle), some of the atoms in the semiconductor lattice will be displaced. If the semiconductor exposed to radiation is part of a device, the device characteristics will change; the changes depend on such factors as the nature and energy of the radiation, the materials and geometry of the device, and even the processes used in manufacturing the device. The changes in characteristics which occur when these effects take place in the bulk of a device have been investigated for some time and are quite well understood in terms of the usual physics of solids. However, effects can also occur at the surface of a device, giving rise to the so-called surface effects which have only more recently received attention and which are governed by the less well understood physics of surfaces.

The failure of the Telstar satellite in 1962 was explained in terms of surface damage to transistors in the command circuits, damage caused by radiation received during transit through the Van Allen belt.[1] From the experience gained in analyzing this failure, it is apparent that surface effects of radiation may often control the behavior of solid state devices subjected to nuclear radiation. In present-day semiconductor technology, the effects of radiation damage in the bulk have been reduced in transistors by using very shallow, diffused junctions. As a result, these devices are quite sensitive to surface conditions. Thus, a knowledge of surface effects is necessary if the decrease in sensitivity to bulk radiation effects is to be fully exploited.

The purpose of the present report is to present as unified and comprehensive a picture as possible of the work done to date on the surface effects of radiation on semiconductor devices. The task is somewhat hampered by the way in which much of the information on radiation effects is presented in the literature. Many authors do not distinguish between bulk and surface effects, and indeed in many experiments it is virtually impossible to do so. For this reason this report will be, for the most part, restricted to those experiments which deal specifically with surface effects.

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Some areas of the surface problem appear to be fairly well understood. The degradation process in nonpassivated devices in gaseous ambients has been satisfactorily explained in terms of surface channeling at exposed p-n junction surfaces. On the other hand, no such satisfactory picture has been published for planar transistors. The results at the moment are somewhat confused, contradictory, and incomplete. It is hoped that this summary may help to illuminate the problem and suggest paths for future studies.

A brief discussion of the present physical theory of surfaces, as required for an understanding of device degradation, will be given before starting a discussion of experimental results and specific models for radiation effects on surfaces since it is against this background that radiation effects must be explained. For a more complete discussion of surfaces, the reader is referred to articles by Many,[2] Watkins,[3] and Law.[4]

2. SURFACE PHYSICS

A. Surface Charges and Surface Potential

An atomically clean crystal surface, such as might be found upon cleaving a crystal, would show broken or dangling bonds associated with the surface atoms. If the bonds are covalent, then presumably each bond, which could hold two electrons, would be half-filled and therefore able to act as an acceptor state. If these acceptor states become filled, the crystal surface would then have a net negative charge. One might, therefore, expect to find a negative surface charge of $\sim 10^{15}$ electrons per cm^2, i.e., one excess electron per surface atom. If the crystal is a metal, the surface charge will be neutralized in a depth of a few angstrom units since metals have a high density of charge carriers. For a semiconductor, however, the much smaller concentration of charge carriers means that the effects of the surface charge will be present as far as $\sim 1\mu$ into the crystal. It should be noted that in this surface region the charge carriers will be holes regardless of the conductivity type of the bulk; i.e., the surface will always be p-type.

Such atomically clean surfaces have been achieved on both silicon and germanium, but they can only be maintained in a very clean vacuum. In any other ambient, the highly reactive surfaces of these semiconductors will readily adsorb several atomic layers from the ambient. These layers (usually oxide) will neutralize most of the surface states due to broken bonds. Some energy states will still exist at the crystal surface, however, either as a result of unsaturated lattice bonds or as a result of impurities or imperfections at the semiconductor surface. The density of these states is typically 10^{11} to 10^{12} per cm^2. These states, called

"fast" states, are in good electrical contact with the bulk material and have relaxation times of about 10^{-7} s. As a consequence, the fast surface states are often the controlling centers of minority carrier recombination and generation.

In addition to the states at the interface, states arise which are caused by ions in or on the surface of the film adsorbed on a semiconductor. These states may be sources or sinks for mobile carriers. Because of poor electrical contact between these states and the semiconductor, mobile carriers are exchanged slowly between the two, presumably by some tunneling process. These ionic states are called the "slow" surface states and have relaxation times from 10^{-3} seconds up to many minutes. Since the states may be positively or negatively charged, they can give rise to surface layers of either p- or n-type. Although little quantitative information is available, it is believed that the densities of slow states are of the order of 10^{12} to 10^{13} per cm^2.

Charges on a semiconductor surface trapped in either slow or fast states will attract or repel mobile charge carriers in the bulk region near the surface so as to neutralize the surface charge and shield the interior from their effects. The net result is a bending of the energy bands of the material in the surface region. The amount of bending of the bands is usually specified quantitatively by the surface potential, U_s. As shown in Figure 1, U_s is the difference between the Fermi level, E_F, and the intrinsic Fermi level, E_i, at the surface.

$$U_s = \left(E_F - E_i \right)_{x = 0}$$

Depending on the amount and direction of bending of the bands, one of three types of surface region will arise:

1. An exhaustion (or depletion) region is formed if the mobile carrier concentration is much less than the concentration of ionized impurities. For an n-type material this will occur if the bands bend up ($U_s < 0$) at the surface, making states for the electrons near the surface energetically less accessible. For a p-type material the bands must bend down to form an exhaustion region ($U_s > 0$).

2. An exhaustion layer may become an inversion layer if the bending of the bands is increased sufficiently. This case is illustrated in Figure 1 for an n-type material where the minority carriers dominate in the surface region. An inversion layer will, of course, have an exhaustion region behind it.

3. If for any reason the bands bend down for an n-type (or up for a p-type) semiconductor, excess majority carriers will collect in the surface region and an enrichment (enhancement or accumulation) layer will result.

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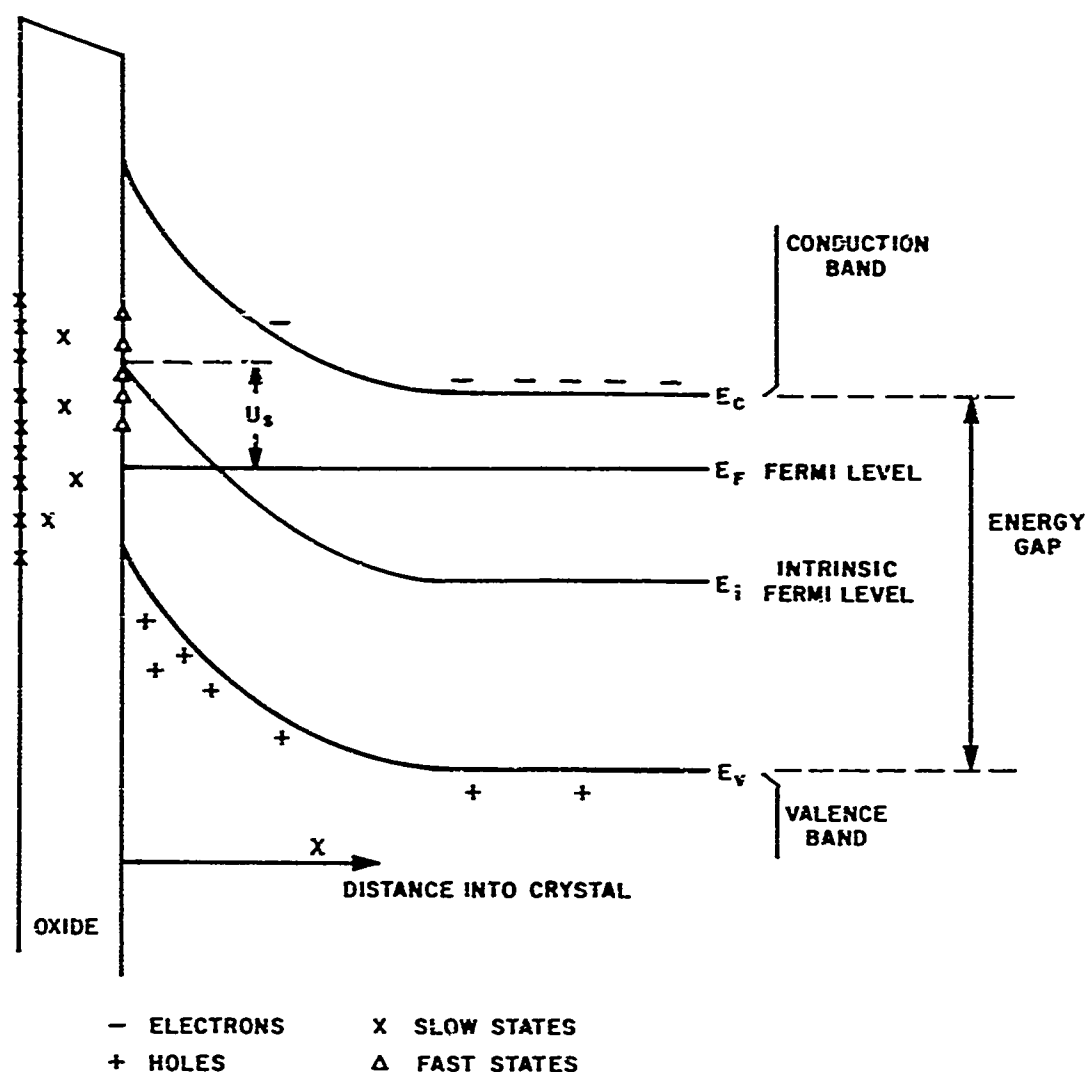
Figure 1. Band structure at the surface of a semiconductor

The three cases are illustrated for both n- and p-type materials in Figure 2.

It is apparent from the above discussion that the concentration of charge carriers and hence the conductivity of the surface layer of a semiconductor may differ considerably from the bulk values. In practice it is possible to obtain valuable information about surface effects by purposely changing the surface potential (and hence the bending of the bands) of a semiconductor and observing the resultant changes in surface conductivity.

B. Control of Surface Potential

The surface potential of a semiconductor is controlled through the charge in the surface states. In this regard the slow states are the more important since they are usually at least an order of magnitude more numerous than the fast states.

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Figure 2. Exhaustion, inversion, and enhancement surface layers
for n- and p-type semiconductors

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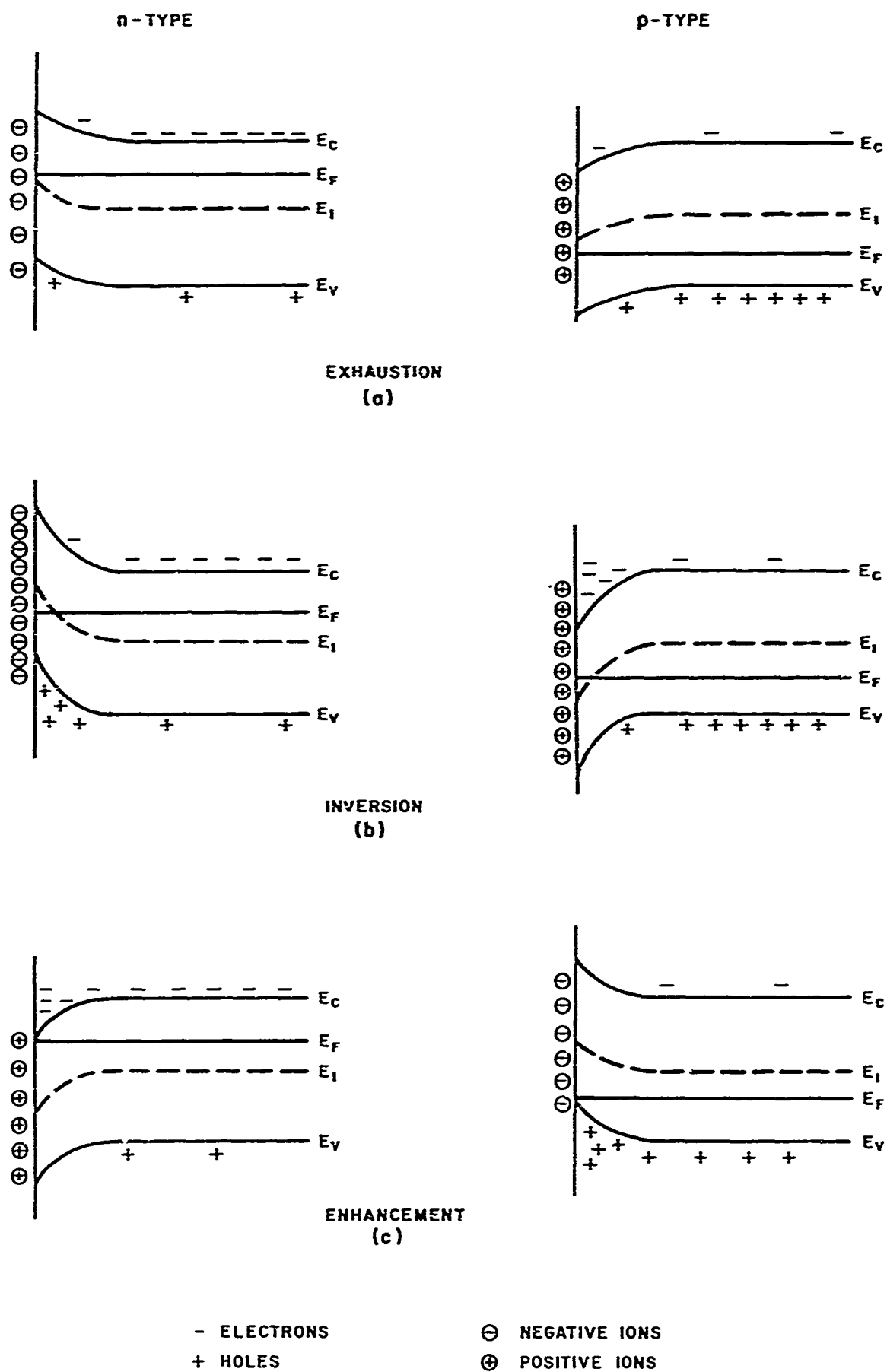There are two methods commonly used for controlling surface charge. In one method the charge is determined by the choice of ambient. For example, gaseous ambients such as oxygen or ozone have strong electron affinities and induce a negative charge on the surface which attracts to it mobile holes. Water vapor and ammonia, on the other hand, produce a positive surface charge, i.e., contribute donor states. Thus, by exposing a semiconductor to the appropriate ambient it is possible to produce, within reasonable limits, a desired surface potential.

The thermally grown SiO_2 layer on Si devices is a particular type of ambient widely used in device fabrication. This oxide stabilizes the surface by saturating the dangling bonds of the Si surface and by separating the Si from the slow states by the thickness of the oxide. This so-called passivation technique, although it does not completely isolate the semiconductor from the ambient, does reduce its sensitivity to ambient variations.

A second method of controlling surface potential is through the use of a field plate. As shown in Figure 3, a metal field plate is placed parallel to the semiconductor surface so as to form a capacitor between it and the semiconductor. The space between the field plate and the semiconductor is filled with some insulator such as SiO_2. The conductivity type of the semiconductor surface layer may be controlled by the applied potential. For example, if the field plate is positive with respect to the semiconductor, electrons will be attracted to and holes repelled from the surface, with the result that the surface layer tends to become more n-type. By the same argument, if the polarity of the potential is reversed, a tendency toward a p-type surface results. The field effect method of controlling surface conductivity is the operating principle of the metal-oxide-semiconductor field effect transistor (MOS-FET). In this device the conductivity of the base, and hence the source-to-drain current, is controlled by the gate (field plate) potential.
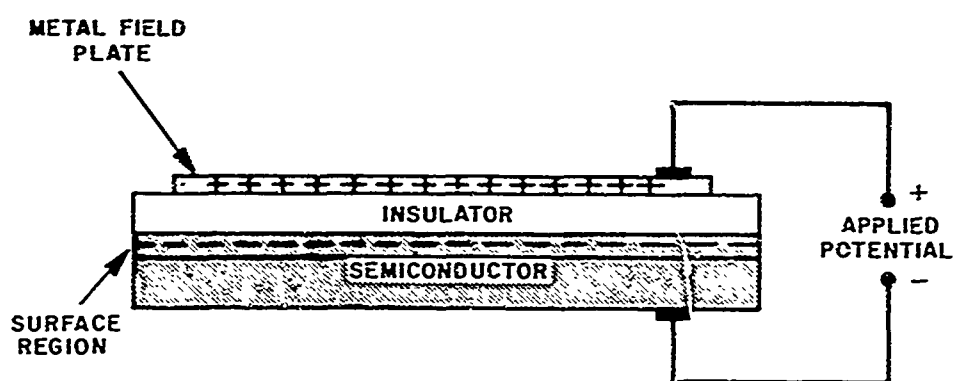

Figure 3. Field plate method of controlling surface potential

C. Surface Recombination Velocity

The fast states at a semiconductor surface are very important from a device standpoint since they act as recombination centers. These centers are relatively more important than bulk recombination centers since they have large capture cross sections and are present with an effectively higher density. As a consequence, within a few diffusion lengths of the surface, generation and recombination are controlled by the fast surface states. The activity of the surface states is measured by the surface recombination velocity, S. The particle current, J/q, of hole-electron pairs combining at the surface per cm^2 per s is proportional to the excess minority carrier density at the surface, Δn; i.e.,

$$J/q = S\Delta n$$

which defines S as the constant of proportionality. S has the dimensions of velocity. It is to be expected that S will change with variations in U_s, i.e., with variations in the surface charge. For S to be near maximum, the rate at which holes and electrons are captured by the fast states should be approximately equal. This condition is fulfilled when $E_F = E_i$ (assuming equal capture cross sections for the two carriers). As U_s changes in either direction from zero, the bands bend up or down causing the concentration of one type of carrier to increase and the other to decrease. The result in either case is a decrease in S. Figure 4 shows, as an illustration, the variation of S with surface potential, ϕ_s, for Ge surfaces as reported by Many.[5] It is apparent that changes in S of almost an order of magnitude are possible. The recombination velocity for Si surfaces has been found to be larger than that for Ge, but shows a similar dependence on U_s.[6]

D. Channeling

An important result of surface states which are sufficiently dense to produce an inversion layer at the surface is the effect known as channeling. Brown[7] discovered that the anomalous leakage current between the n-regions of an npn structure was the result of channels, i.e., inversion layers, formed across the p-region, which provided a conduction path of the same conductivity type as the end regions. Channel formation may occur at any p-n junction, generally on the low conductivity side of the junction. Channels have the effect of adding currents in parallel with the main junction currents. The times involved in channel formation indicate that the phenomenon is connected with the slow surface states. It will become apparent that channeling is the dominant surface effect for many semiconductor devices.
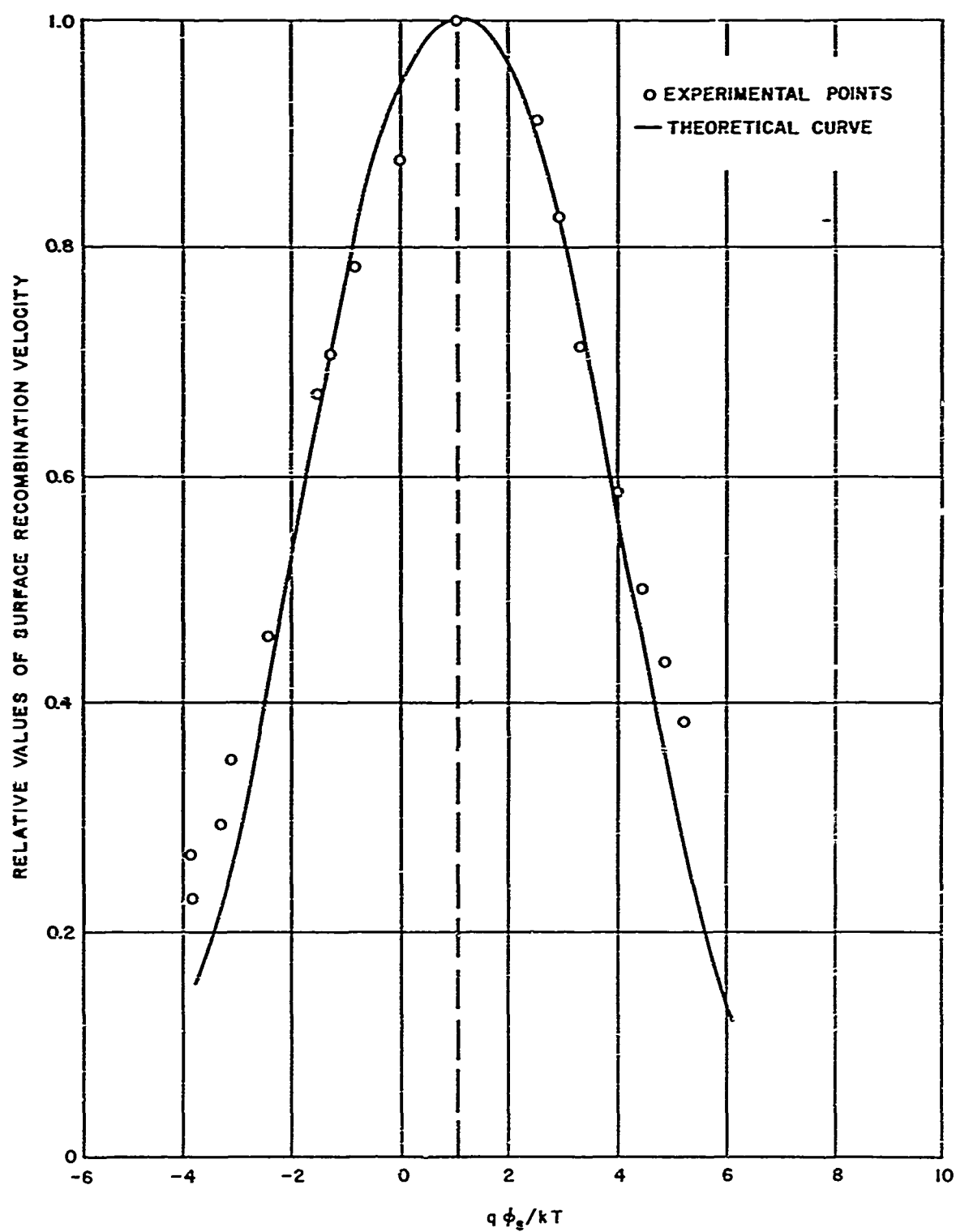
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Figure 4.   Variation of surface recombination velocity
with surface potential

3. EFFECTS OF SURFACES ON DEVICES

A. P-N Junction Reverse Characteristics

1. <u>Leakage Current.</u> The reverse leakage current of a p-n junction is the sum of several components. A bulk component arises from thermally generated minority carriers which are created within or diffuse to the space charge region and are swept across the junction by the reverse bias field. The surface near the junction is also a source of minority carriers and produces components of reverse current from the surface both outside and inside the junction space charge region.

If channeling is present when a diode is under reverse bias, the reverse current will be increased for two reasons. First, the channel increases the effective area of the junction and thereby increases the number of thermally generated minority carriers diffusing across the junction. Second, the increase in area takes place at the surface which, because of surface sites, has a high generation of carriers. A further result of the increased junction area is an increased junction capacity (which provides a convenient means of detecting the presence of channels).

2. <u>Breakdown.</u> The breakdown voltage of a reverse-biased junction is, in many cases, reduced below the value expected for bulk breakdown by surface conditions at the junction. Surface breakdown, like bulk breakdown, is an avalanche process and takes place at localized areas of the surface. It has been found that an inversion layer formed on the high resistivity side of a junction raises the breakdown voltage, while formation of an accumulation layer tends to lower it.

3. <u>1/f Noise.</u> Semiconductor devices often exhibit a noise whose spectral output is inversely proportional to frequency and which is referred to as 1/f noise. It is believed that this noise originates at the semiconductor surface; certainly it is very sensitive to surface conditions. According to McWhorter,[9] 1/f noise is the result of fluctuations in the charge in the slow states which cause corresponding changes in the semiconductor conductivity. Experimentally, it is known that 1/f noise increases when the semiconductor surface layer changes from accumulation to inversion. Atalla and his associates[9] have found that SiO_2 passivation significantly reduces 1/f noise.

B. P-N Junction Forward Characteristics

The effect of surface recombination and channel formation on p-n junction forward characteristics has been discussed by Sah.[10] The junction current can be divided into several components based on the location of carrier recombination-generation. The components are (see Figure 5):

1. Bulk recombination-generation current on either side of the junction

2. Transition region bulk recombination-generation

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For components 3, 4, and 5, m and I_s in the expression for I are functions of the surface potential; hence the diode forward characteristics depend, through this potential, on the surface charge. When channels are present at a junction, component 5 will usually dominate over components 3 and 4 and the surface part of the forward diode current will be determined by the channel values for m and I_s.

The efficiency with which a forward-biased p-n junction injects minority carriers into the more lightly doped side is an important quantity which is sensitive to the surface components of the forward current. If the component of minority carrier current caused by surface generation becomes large enough to be a significant portion of the total junction current, then the injection efficiency will decrease as a result.

C. Effects of Surface Recombination and Channeling on Junction Transistors

The effects of channeling and surface recombination on transistors are somewhat more complicated than for simple p-n junctions. As might be expected, I_{CBO} for the transistor behaves in a similar way to a diode-junction reverse current. I_{CBO} may also be increased by the formation of a channel across the base region so as to provide a leakage path from emitter to collector.

The current gain of a transistor is affected by both channel and surface recombination in the region of the emitter-base junction. The common emitter gain, $h_{FE} = (I_C - I_{CEO})/I_B$ is influenced through I_B. If the base transport factor (β) of a transistor is decreased because of increased surface recombination at the base surface, then I_B is increased to supply majority carriers for recombination. This recombination corresponds to an increase in a component of the emitter current with an exp (qV/mkT) dependence where m ~ 1. Generation-recombination at the surface of the emitter-base transition region lowers the emitter efficiency (γ) and also decreases h_{FE}. This corresponds to an increase in an emitter current component with an exp (qV/mkT) dependence with $1 < m < 2$. These effects of surface recombination and channeling on junction transistor characteristics have received experimental support from the work on Sah,[10] Kuper,[11] and Iwersen and his associates.[12] Kuper found that the base current, I_B, of diffused base Ge transistors was quite sensitive to surface traps at the surface of the emitter-space charge region. The effect of these traps on recombination could be increased by removing water from the surface oxide, resulting in an order of magnitude decrease in h_{FE}. The surface region of the emitter-base junction would thus appear to be the region which controls the common emitter current gain in Ge transistors.

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The gain degradation in Si transistors at low currents was investigated by Iwersen. Figure 6 shows a typical dependence obtained by Iwersen of I_C and I_B on V_{EB} for silicon npn transistors. The I_B characteristic has two components, an "ideal" one at high currents with $I_B \propto \exp(q\,V_{EB}/kT)$ and a "nonideal" one at low currents with $I_B \propto \exp(q\,V_{EB}/mkT)$ with $m \sim 2$. The latter component according to Sah's model could come from recombination in the emitter-base space charge region either in the bulk or at the surface. Iwersen used transistor-like structures with an additional electrode connected to the emitter with which they could shift the forward-biased part of the emitter away from the surface. Under these conditions the I_B characteristic showed the "ideal" behavior illustrated in Figure 6. Thus, the decrease in h_{FE} at low currents appears to arise from recombination at the surface of the emitter-base space charge region. The technique used by Iwersen to separate surface and bulk components is a very useful one and is currently being exploited in separate bulk and surface effects after irradiation as well.

Neither Kuper nor Iwersen discusses the effect of channels at the emitter-base junction. Sah, however, has investigated the effects of channels through the use of a special planar transistor which had a metal gate over the surface region of the emitter-base junction. A channel could be induced on the base surface by a suitable selection of gate potential, V_{GB}. Figure 7 shows the junction current, I_B, as a function of junction voltage, V_{EB}, for temperatures ranging from $-26°$ to $150°C$. The solid curves correspond to the absence of channels ($V_{GB} = -20V$) while the dashed curves are for the case of channels present ($V_{GB} = +20V$). It is apparent from Figure 7 that m is much larger (m $\sim$ 9 for channels as compared with m $\sim$ 1.4 for no channels) when channels are present. It is also apparent that I_B is much less temperature dependent when channels are present.

According to Sah, the surface recombination current is considerably higher on a bare surface than on an oxide-protected surface. Hence, we should expect to find a higher h_{FE} for protected devices. As predicted, Sah finds the gains for Si planar transistors are higher at all collector currents for oxide-protected devices than for the same devices after the oxide has been removed (however, the opposite effect has also been observed[13]).

4. SURFACE EFFECTS OF RADIATION ON NONPASSIVATED MATERIALS AND DEVICES

A. Introduction

There are two types of effects on the bulk of a semiconductor resulting from irradiation by energetic particles or photons. First, new defects are created which introduce additional energy levels in the energy gap of the semiconductor.
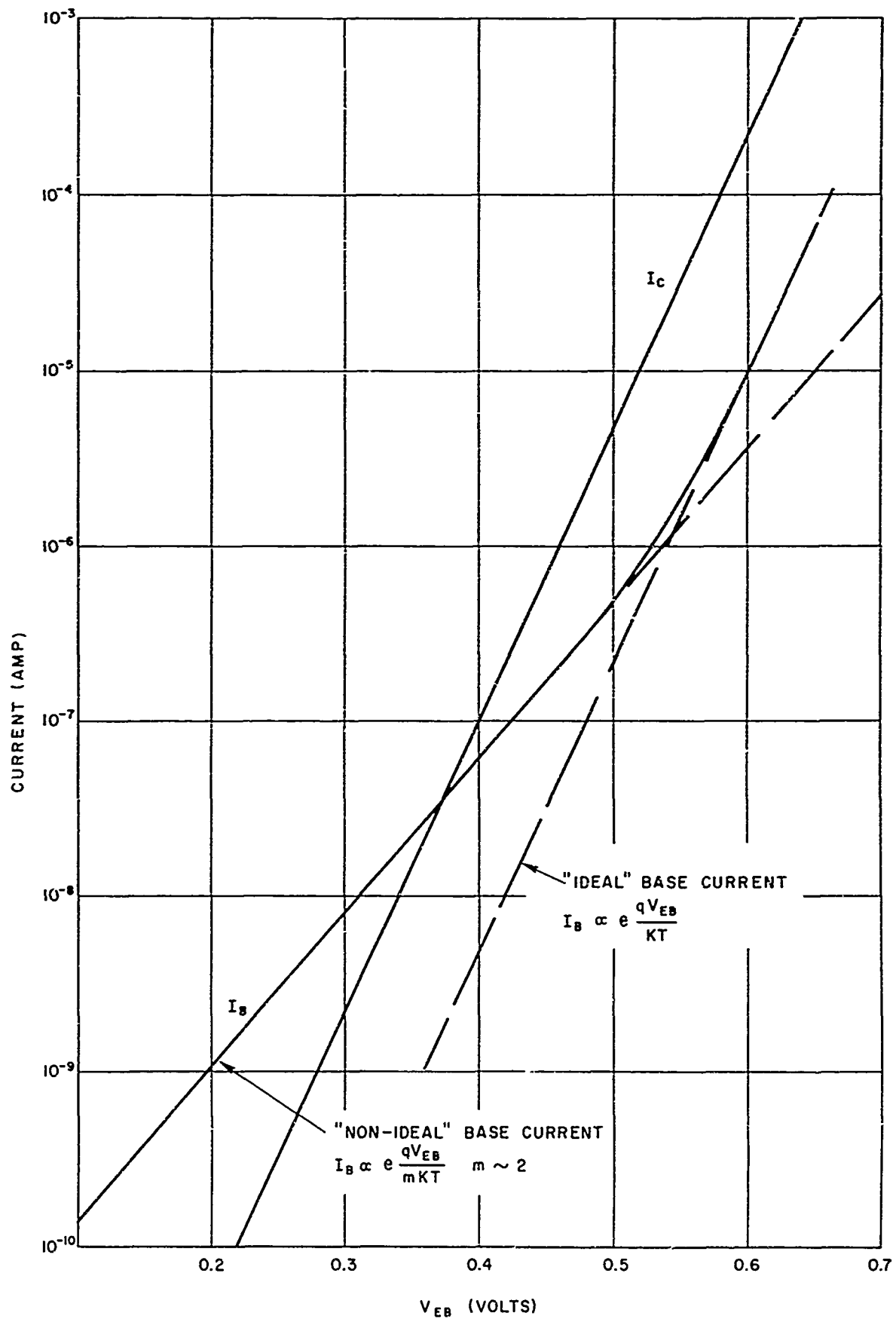
Figure 6. Typical I_C, I_B vs V_{EB} curves for Si npn transistors
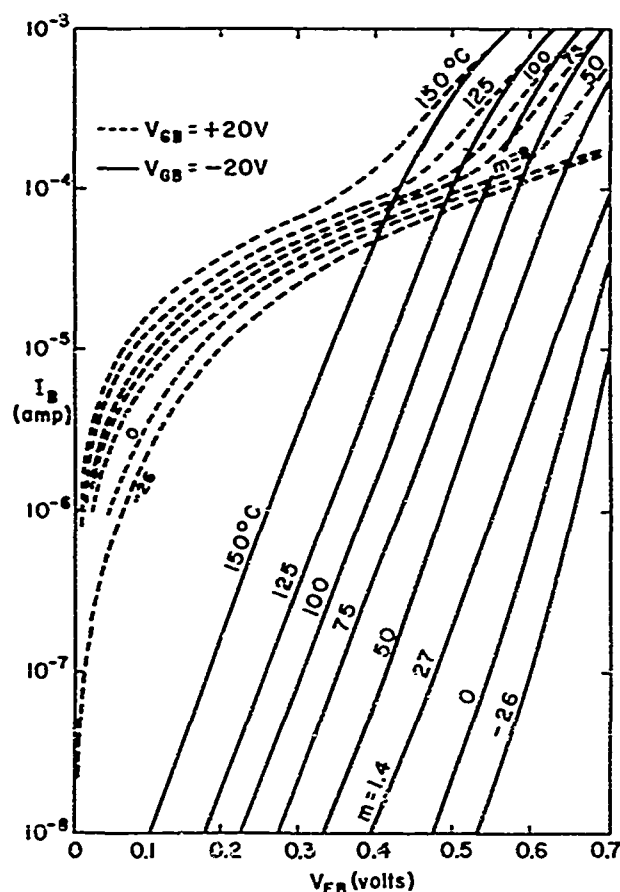
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Figure 7. Forward emitter characteristics for a surface channel (V_{GB} = +20V) and for no surface channel (V_{GB} = -20V)

Second, intense ionization is produced, most of which decays quickly, but a certain fraction of which may be trapped in rather long-lived excited states. The kind and number of defect states introduced into the bulk are very sensitive to the nature of the bombarding particle and its energy. On the other hand, the ionization produced in the bulk is presumably sensitive only to the total energy adsorbed.

The surface of a semiconductor is presumed to be a highly imperfect structure. Hence, it has been tacitly assumed that the radiation levels which significantly affect the number of bulk defect states could not similarly affect the number of surface defect states. This assumption may be invalid for the reasons discussed in the following paragraphs.

It is believed that the primary defects introduced by radiation are vacancies and interstitials. However, there is strong experimental evidence that these primary defects interact almost immediately with existing crystal defects. If they do not do so, there appears to be a strong likelihood that the vacancies and interstitials annihilate one another, i. e. , that frozen-in vacancies and interstitials per se do not exist. There is also strong experimental evidence indicating that existing defects in the semiconductor crystal may often be electrically inactive but become electrically active when attached to a primary radiation defect. Hence, the surface, with its high concentration of existing defects, may be a sink for primary radiation defects. The result of such an interaction could be a significant change in the number of impurity levels at the surface upon irradiation, i. e. , an increase in the density of fast states at the interface of the semiconductor and any adsorbed surface layer. In addition, the density of active (charged) slow states can be increased by purely electronic processes produced by ionizing radiation effects within or on the adsorbed surface layer. These changes in charge state of

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the surface defects can be very long-lived because of the weak electronic inter-action of these surface defects and the bulk of the semiconductor.

The evidence on nonpassivated devices tends to support the picture that the predominant effects of radiation on nonpassivated surfaces are changes in the charge in slow states rather than the creation of new defects. Hence, most experiments on surface effects have not concerned themselves with the nature of the ionizing particle but only with the energy absorbed (dose) at the surface. Most experiments have, therefore, been done with Co^{60} gamma rays as a matter of convenience, with a few investigations using energetic electrons. The possibility outlined above for the creation of additional defect states by the interaction of primary defects with existing defects and their dependence on the nature of the bombarding particle has not been adequately explored.

B. Effects of Radiation on Semiconductor Surfaces

There have been limited experimental studies on single crystal semiconductor samples of the effects of ionizing radiation on surface phenomena. Among the studies that could be cited is the work of Spear,[14,15] who investigated the effects of radiation on the photoconductive response in germanium down to energies of 0.5 eV, i.e., well below the absorption band edge. This response arises from deep-lying surface states. Irradiation with very low energy electrons (~ 5 keV) was found to quench this photoconductivity. Spear attributed this quenching to radiation-induced changes in the surface potential with the result that the surface became more n-type. Similar changes in surface potential of n-type Si were found by Spear for both 3 and 500 keV electron irradiation.

The effects of irradiation by Co^{60} gamma rays and energetic electrons on the surface recombination velocity in n-type Ge have been studied by Komatsubara.[16,17] He used alloyed p-n junctions with a nickel field plate on the opposite side of the Ge wafer from the alloyed junction. By using a wafer whose thickness was small compared to a diffusion length, he made the reverse current of the junction, I_s, proportional to the surface recombination velocity, ?. In this way he was able to obtain directly an oscilloscope presentation of the variation of recombination velocity with surface potential, E, using a 50-c/s ac voltage on the field plate. His results before and after various levels of γ bombardment are shown in Figure 8 and can be compared with the theoretical variation shown in Figure 4. There is obviously a considerable shift in the surface potential, which Komatsubara attributed to new fast surface states produced by the radiation.
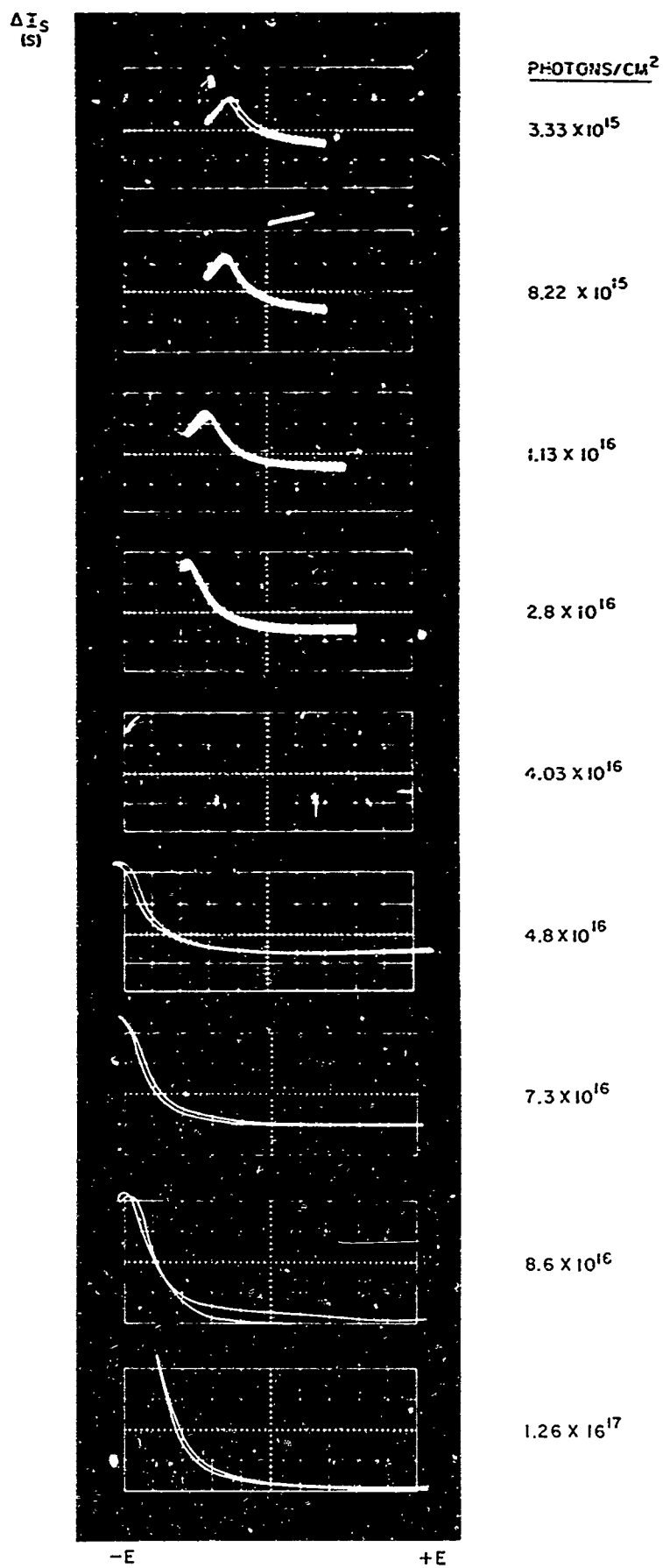
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Figure 8. Change of I_S vs E curves of 30 ohm-cm n-type Ge with radiation

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C. Effects of Ion Bombardment on P-Type Silicon Surfaces

Considerable experimental evidence (to be reviewed later) has established that many of the radiation effects on semiconductor devices can be traced to the ionization of the ambient by the radiation with subsequent migration of the ions to the semiconductor surface and resultant changes in the density of slow surface states.

In an attempt to discover more about the processes involved at the surface of an irradiated semiconductor device, Estrup[18] investigated the effects of ion bombardment on the surface conductivity of p-type Si. To do this he placed a slab of the material, into which n^+ regions had been diffused at either end, in a gaseous discharge. By a suitable selection of electrode potentials and gases he was able to bombard the Si surface with either electrons or positive ions. By measuring the current between the n^+ regions, Estrup determined whether n-type channels had been formed.

When the material was exposed to positive ions, a large increase in the current, I, through the sample was observed, indicating the formation of a highly conducting channel. Figure 9 shows the increase in current, ΔI, as a function of the total ion charge, Q, impinging on the surface for two ion currents, J_a and J_b $(J_a > J_b)$. Initially the rate of increase of I is very large, but it gradually diminishes until eventually I levels off, i.e., the surface effect saturates. The build up of surface charge was found to depend primarily on the ion current, the bulk material conductivity type, and the surface condition.

The surface effects of ions were found to be similar to those produced by chemical treatments except that the surface charge induced by the ions was unstable. The effects of positive ions could be counteracted by exposure to gases, such as O_2, which tend to produce a negative surface charge but were little affected by those, such as NH_3, which produce a positive surface charge.

At the termination of the discharge, the excess current recovered as shown in curve a of Figure 10. It was found that heating or exposure to ultraviolet radiation accelerated the recovery rate. Exposure to electrons caused an instantaneous decrease in I as shown by curves b and c, Figure 10.

Estrup proposed that the accumulation of surface charge results from two competing processes, a build up and a simultaneous decay of charge. The charge on the surface increases until the two processes reach equilibrium. The charge build up results from the impinging ions depositing charge in surface sites. From the details of the investigation, Estrup estimates that an impinging ion has about 10^{-4} chance of creating a charged surface site. These sites are presumably connected with some type of surface imperfection such as a chemical impurity, since
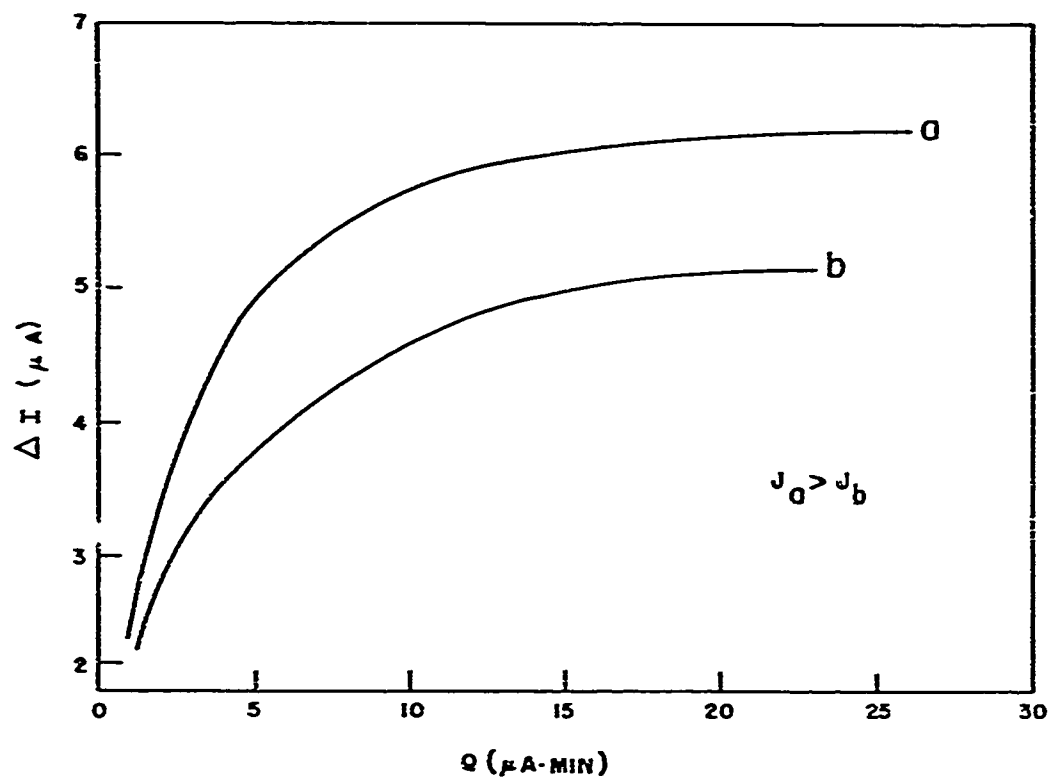
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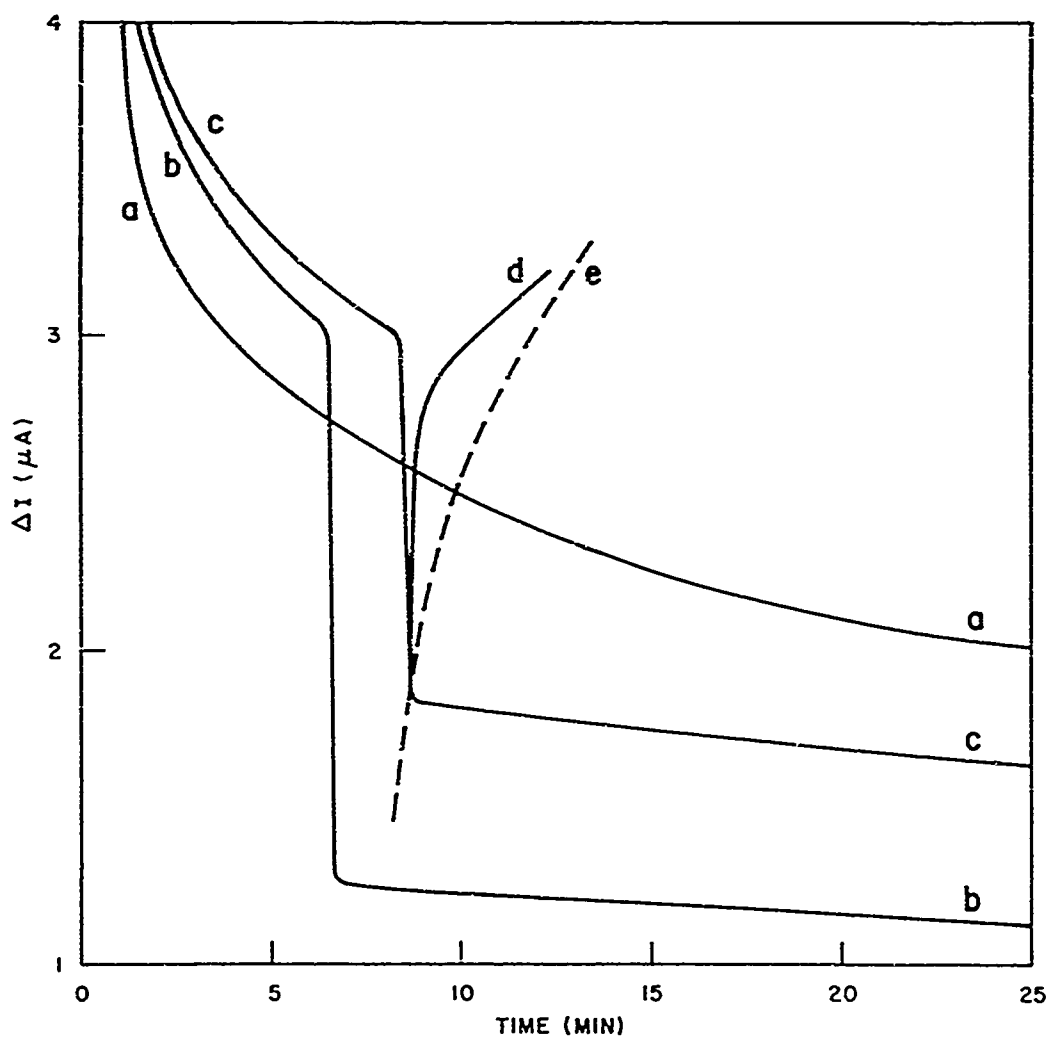Figure 9.   Current increase vs total ion charge reaching the Si surface

Figure 10.   Current increase as a function of time

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clean surfaces or surfaces with only a few layers of "pure" oxide do not show the surface effects. The decay of surface charge is apparently determined by the transport of electrons from the space charge layer to the surface. The transport of electrons, and hence the recovery process, is sensitive to heat, light, and exposure to bombarding electrons.

If a Si surface which had been "recovered" by exposure to electrons was subsequently exposed to positive ions, the current rapidly increased as indicated in curve d, Figure 10. The increase was found to be much more rapid than the normal increase indicated by curve e. Estrup explained this "memory" effect as resulting from a two-step decay process. A charged site decays to a neutral but active site and may remain in this condition for some time before decaying to a normal site. It is easier to charge these active sites than to charge originally the normal sites, and hence a surface once charged will "remember" its condition for a considerable length of time. This memory effect is quite important and is also seen in irradiated transistors.

D. General Effects of Radiation on Nonpassivated Devices

A discussion of radiation effects on semiconductor devices is complicated somewhat by the wide variety of responses found for various devices. Even two supposedly identical transistors may behave quite differently when exposed to radiation. When different manufacturing processes and different experimental procedures are added, the task of extracting a useful picture of the processes involved becomes more difficult. However, it is possible to make some rather broad statements about surface effects of radiation on devices. The predominant effect of irradiation appears to be the formation of channels on the device surfaces which lead to degradation of the device characteristics. The process by which such channels are formed is essentially that studied by Estrup and is due to ions produced in the ambient which diffuse or drift under the fields arising from junction reverse biasing to the semiconductor device surface.

Generally speaking, surface effects become noticeable at radiation doses $\sim 10^3$ rad (the rad is the unit of absorbed dose; 1 rad corresponds to 100 ergs/gm absorbed energy) as compared to $\sim 10^7$ rad for bulk effects and if the effects saturate they do so at doses of $\sim 10^7$ rad. (Saturation has been observed at doses as low as 10^3 - 10^4 rad, lightly doped particle detectors.[36]) The most radiation-sensitive parameters have been found to be the reverse-bias leakage current for diodes and I_{CBO} and h_{FE} for transistors. These parameters usually degrade when the device is exposed to radiation although in some isolated cases they have been observed to improve.

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For diodes the leakage currents may increase as much as several orders of magnitude and may or may not saturate. The collector leakage current, I_{CBO}, for transistors shows a similar behavior. Transistor gain, h_{FE}, generally decreases with dose and may, at sufficiently large doses, drop below unity. It is frequently found that the degraded characteristics show partial and sometimes complete recovery. Apparently, recovery is promoted by baking, forward biasing, and exposure to radiation without bias.

It is important to note that semiconductor devices operated at low injection levels, such as transistors used in low-level logic, are inherently more sensitive to surface conditions and hence are the most susceptible to surface effects due to radiation. Devices operated at high injection levels, on the other hand, are relatively less affected by surface effects of radiation.

E. Radiation Effects on Diodes

The amount of work done on nonpassivated diodes which may be discussed in terms of the surface effects of radiation is rather limited. Nevertheless, some interesting effects have been observed on diodes and deserve a discussion at this point.

Freyer[19] and Verrelli[20] have performed the most comprehensive experiments on the surface effects of ambient and radiation on diodes. Freyer subjected Ge diodes, both with and without encapsulation, to Co^{60} gamma irradiation. For the encapsulated devices he found an increase in reverse-bias leakage current during irradiation; he attributed this to bulk ionization which increased the bulk reverse current. To determine the effects of the ambient, he etched the surfaces of decapsulated devices and irradiated them in a controlled atmosphere. The results are indicated in Figure 11.

Two points are apparent from Figure 11. First, the magnitude of the reverse current, I, depends on the ambient, i. e., on the relative humidity. As seen in the figure, the reverse current decreases as the relative humidity increases from 0 percent (dry oxygen), passes through a minimum (10 to 35 percent relative humidity), and then increases steadily as the relative humidity approaches 100 percent. Second, at low values of the relative humidity the reverse current increases initially with voltage, reaches a peak at some critical voltage, then drops rapidly to a lower value and remains almost constant for further increases in voltage.

Similar results were also obtained by Verrelli under somewhat different experimental conditions, and thus confirm Freyer's observations to be the results of surface rather than procedural effects. Both Freyer and Verrelli explain their results as follows: A Ge diode surface is presumed to be covered with a few layers

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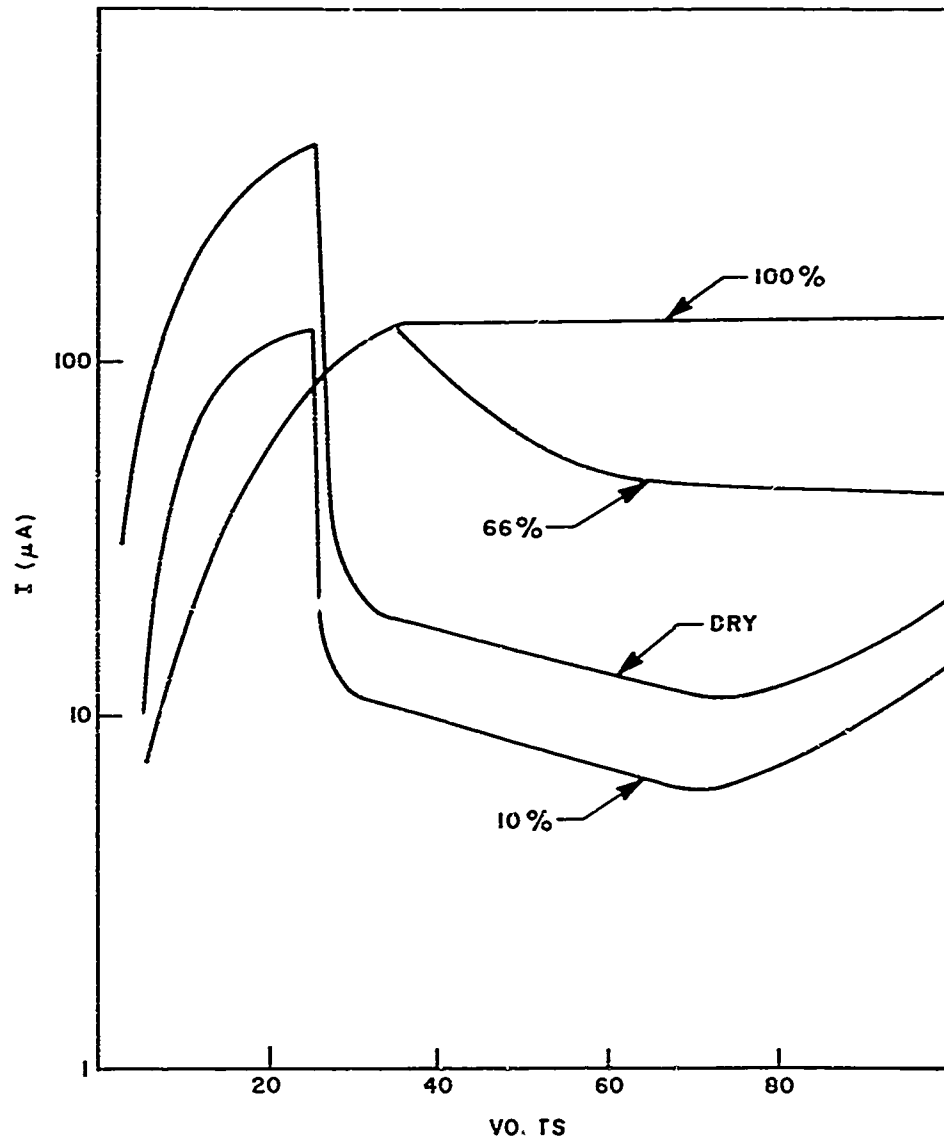
Figure 11. Reverse current-voltage characteristics in dry ambient
and 10, 66, and 100 percent relative humidity during irradiation

of oxide which give rise to slow acceptor surface states. In a dry ambient these
states are unoccupied, but irradiation causes ionization which supplies electrons
to the states. The resultant negative surface charge causes channel formation on
the n side of the diode with an accom, ·ying increase in reverse current. If the
relative humidity increases, moisture forms on the surface of the diode; this tends
to produce a positive surface charge and reduce channel formation and hence the
reverse current. As the relative humidity increases to 100 percent, the net sur-
face charge becomes positive because of further moisture collection and a channel
now forms on the p side of the junction. The result is an increase in the leakage
current.

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(a) INVERSION LAYER INDUCED BY
ADSORBED OXYGEN MOLECULES

(b) OXYGEN MOLECULES DESORBED
BY ELECTRIC FIELD

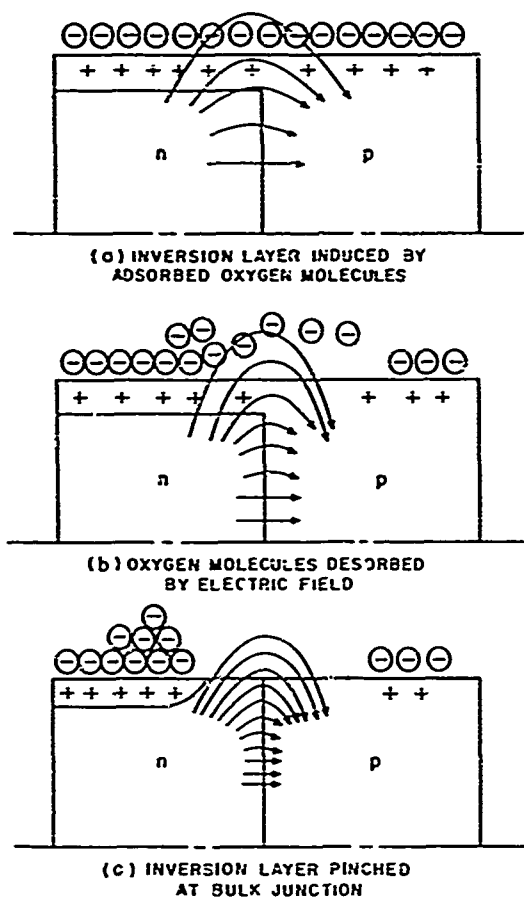(c) INVERSION LAYER PINCHED
AT BULK JUNCTION

Figure 12. Proposed model
for desorption

The peak in the reverse-bias I-V characteristics for dry ambients can be explained in terms of a different mechanism. Verrelli proposes the model shown in Figure 12. As the reverse-bias voltage is increased, the electric field at the surface near the junction increases and, at some critical value, becomes strong enough to cause desorption of the negative surface ions, Figure 12(b). With the surface charge removed, the inversion layer near the junction is removed and the channel is pinched off, Figure 12(c). The reverse current, of course, decreases substantially when the effect of the channel is removed.

Estrup[21] investigated the effects of electron and positive ion bombardment on reverse-biased, nonpassivated n^+ -p diodes. He found that bombardment with positive ions produced a reverse current-voltage characteristic similar to curve 1 of Figure 13. According to Buck,[22] this type of behavior results from inversion layer (i. e. channel) formation on the diode surface and the resultant effects on leakage current and breakdown described in Section 3A. A channel is to be expected here since the positive ions produce a positive surface charge which strongly affects the high resistivity side of the p-n junction, in this case the p side, and causes the formation of an inversion layer. A subsequent electron bombardment of sufficient duration should result in a negative surface charge and hence an accumulation layer on the p side. Buck predicts for this case a reverse current characteristic as shown by curve 2 of Figure 13. Estrup did, in fact, observe the predicted change in the characteristic when the diodes were irradiated with electrons. These observations are consistent with Estrup's findings discussed earlier and furthermore support the model for surface effects of radiation on transistors which will be described in the next section.
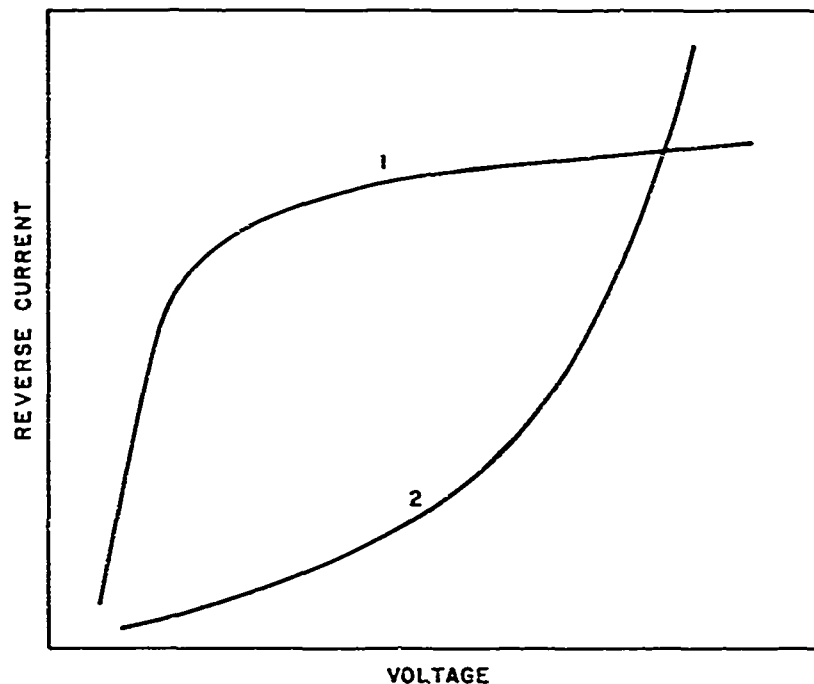
Figure 13. Schematic representation of diode
characteristics. Type 1 = inversion layer,
Type 2 = enhancement layer

F. Model for Nonpassivated Transistors with Gas Ambients

A model which qualitatively explains many of the experimental observations
of radiation effects on gas-encapsulated semiconductor devices has been developed
by Peck and his associates.[23] Their model describes the degradation of transistor
parameters in terms of the surface inversion layers and channels caused by ionized
ambient gas.

This model is best discussed by referring to a typical nonpassivated transis-
tor, as shown in Figure 14. The device itself is enclosed in a can and surrounded
by a gas. The basic process of degradation is explained as follows: Upon exposure
to radiation, the gas in the can becomes ionized, and the ions are attracted to the
device surface by the electric field created by the collector junction reverse bias
and by fields which may exist between the device and the can. As a result, the
surface becomes charged either by adsorption of the ions onto the surface or by the
process, proposed by Estrup,[18,19] of charge transfer from the ions to surface im-
purities already present. The surface charge layer thus created causes an inver-
sion layer in the region of the collector junction which leads to device degradation.

The model proposed by Peck can be elaborated to give a somewhat more de-
tailed description of degradation. Consider Figure 15, which shows channel
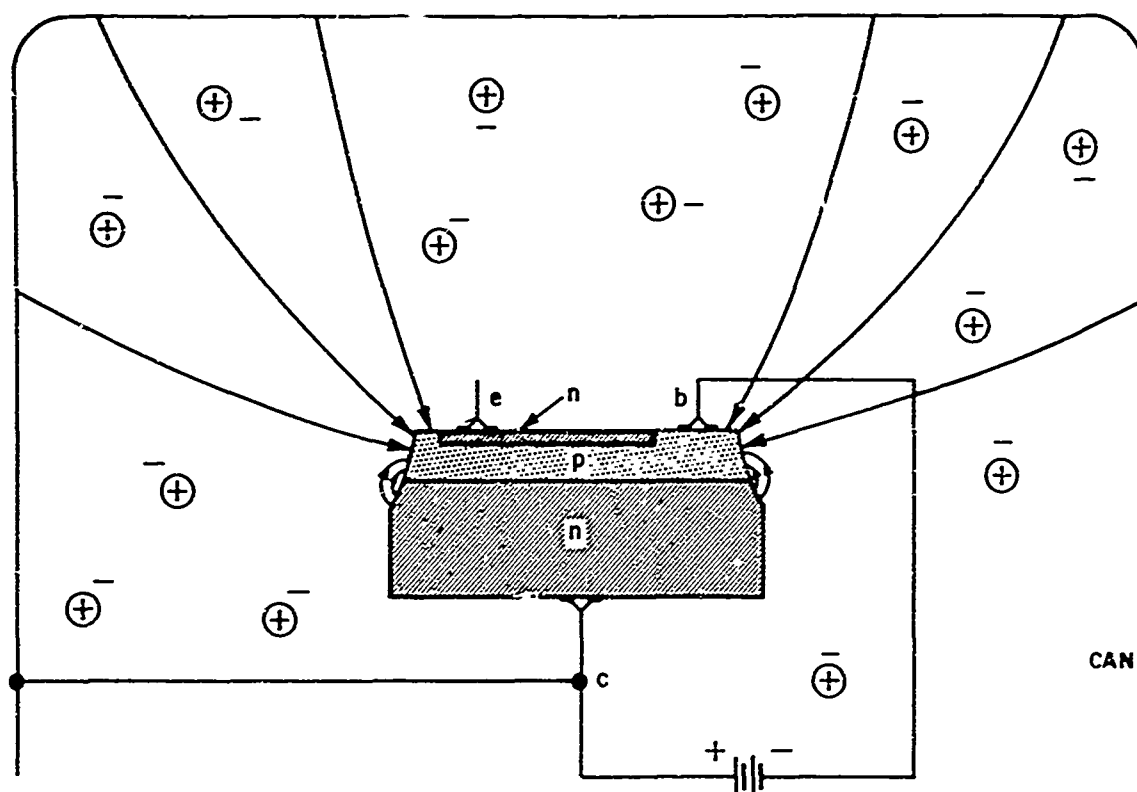
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Figure 14. Cross section of a typical nonpassivated transistor

formation on npn and pnp devices in more detail. For the npn device, Figure 15(a), the channel is shown extending part way from the collector to the emitter while the base surface near the emitter is depleted. Since, by design, the base width of a transistor is quite small, the change in the collector junction area due to the channel will not be sufficient to cause a large increase in I_{CBO}. However, the positive surface charge near the emitter will alter the surface potential and hence the surface recombination velocity may be increased. An increase in surface recombination requires an increased base current and hence causes a decrease in h_{FE}.

If the channel should extend across the entire base surface from the collector to the emitter, the surface recombination would be reduced (because the concentration of holes would be greatly reduced). However, a large increase in I_{CEO} would obviously result. Under these conditions, h_{FE} may actually appear to increase since the increase in I_{CEO} would appear as an increase in I_C without a corresponding increase in I_B.

As pointed out in Section 3B, changes in h_{FE} and I_{CEO} could also arise from changes in generation and recombination at the surface of the base or transition regions. For most devices, however, these effects are believed to be small compared to the effects resulting from channel formation.

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DEPLETED
REGION

e

ELECTRIC
FIELD

MINORITY CARRIERS
DIFFUSE TO SURFACE

CHANNEL

n

p

n

(a)

e

ELECTRIC
FIELD

p

n

CHANNEL

p

(b)
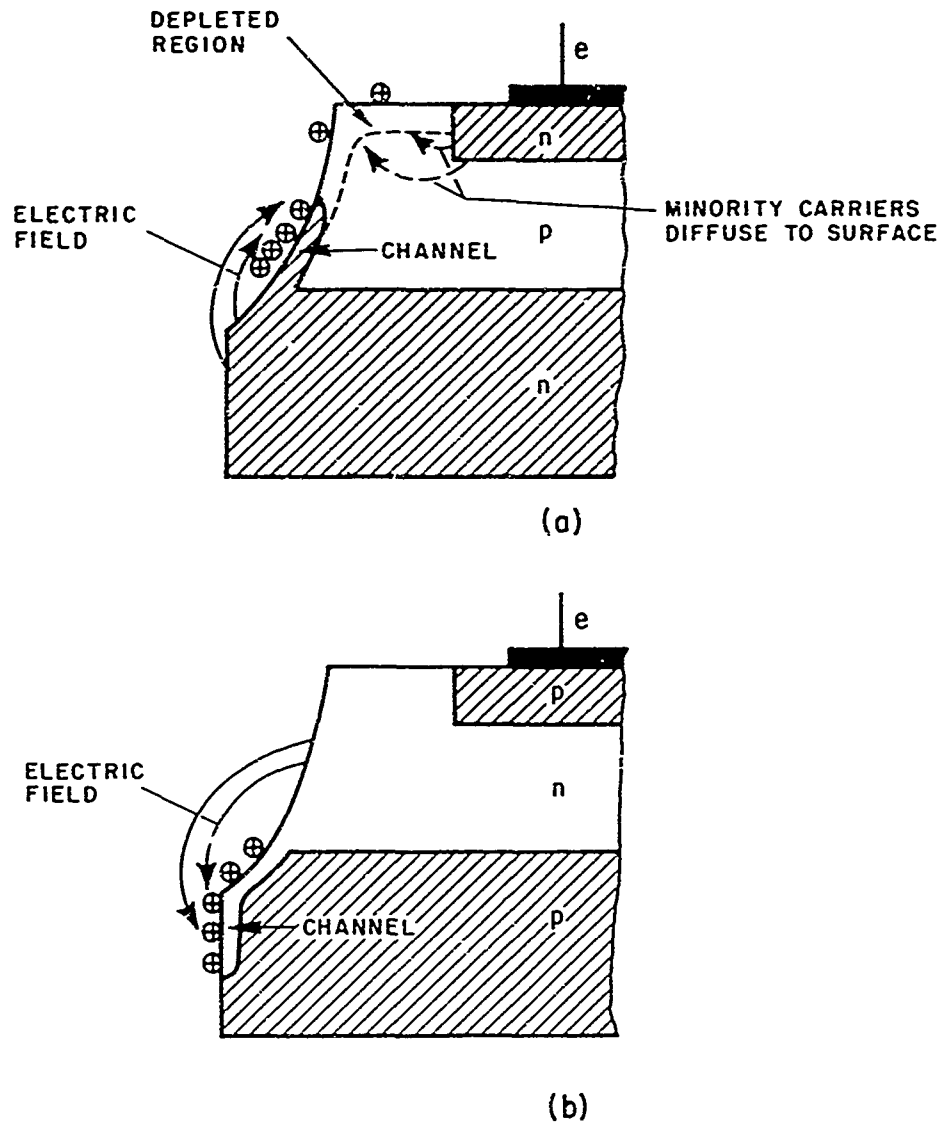
Figure 15.   Channel formation on (a) npn, (b) pnp transistors
by positive surface charge

For a pnp device, Figure 15(b), the positive surface charge will create a channel on the collector surface.   The area of such a channel may be quite large and cause a significant increase in I_{CBO} because of the increased area of the junction.   On the other hand, recombination at the base surface should be relatively unaffected and consequently h_{FE} should be comparatively stable.

It should be pointed out that the above predictions are necessarily of a general nature.   While irradiated devices will follow the general pattern of degradation, the detailed behavior of a specific device will depend upon such factors as the device geometry and surface treatment received during fabrication.
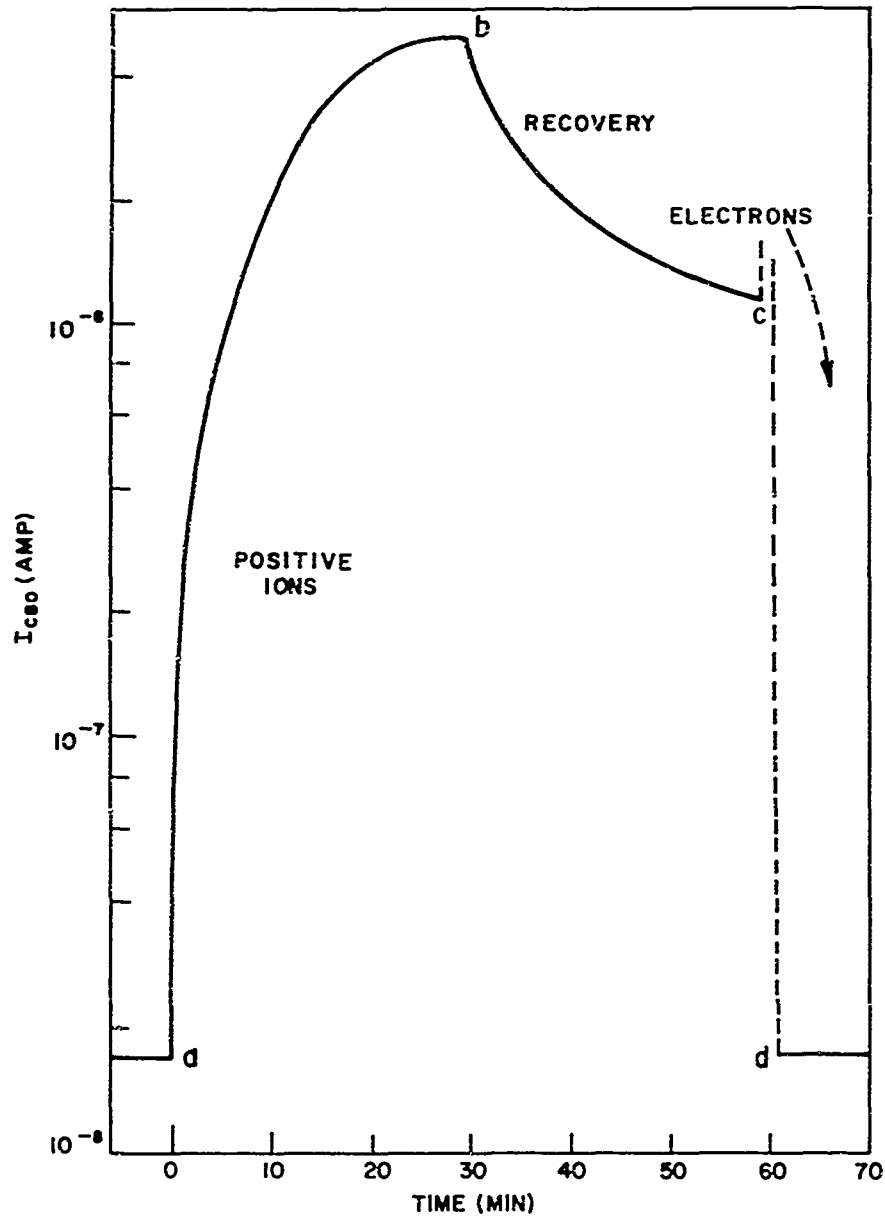
Figure 16. Normal effect of positive ions and electrons on transistor: a-b = discharge on, positive ions drawn to surface; b-c = discharge off; c-d = discharge on, electrons drawn to surface

Estrup[21] has verified the essential correctness of this model by a series of experiments on Si npn transistors in which he exposed the devices under reverse bias to positive ion and electron bombardment. The effect on I_{CBO} is shown in Figure 16. The positive ion bombardment starts at point a and continues to point b. During this time, I_{CBO} increases more than two orders of magnitude. According to the model, the ions deposit a positive surface charge on the p-type base of the transistor. This surface charge creates a channel from collector to emitter, which in turn causes the increase in I_{CBO}. From points b to c the device is under no

bombardment and a partial recovery is observed, presumably due to some neutralization of the positive surface charge. At c an electron bombardment begins and, as expected, the positive surface charge is rapidly neutralized, returning I_{CBO} to its original value.

G. Effects of Radiation on I_{CBO} of Nonpassivated Transistors

Figure 17 gives an indication of typical results obtained for I_{CBO} degradation of several transistor types.[24] It should be kept in mind that these curves are only indicative of results found for the types indicated and that the curve for a given device may depart markedly from the curve shown. Inspection of the curves reveals several important facts. As expected, Ge devices have higher initial reverse leakage currents than do Si devices and these currents remain higher, for most cases, up to quite large radiation doses. The magnitude of the I_{CBO} change depends on the device fabrication process (e. g., alloy vs diffused and epitaxial mesa vs mesa) and, most importantly, upon the ambient in the transistor can (e. g., gas-filled vs evacuated).

H. Dose Rate and Saturation Effects

It has been found that Ge pnp transistors show a saturation of I_{CBO} with increasing radiation dose.[25,26] Furthermore, it appears that the saturation value of I_{CBO} may be dose-rate dependent.[25] On the other hand, a decrease in I_{CBO} for two Ge npn devices has been reported.[26] The improvement appeared to be permanent with I_{CBO} decreasing to one-half its original value. Blair[27] has reported I_{CBO} measurements on a Ge mesa transistor which showed no signs of saturation up to a dose of 10^7 rad. The results for Si transistors are somewhat different from those for Ge in that there is usually no tendency for I_{CBO} to saturate with increasing dose.[26] Saturation has been observed in grease-filled Si transistors.[28]

On the basis of the proposed model, it is to be expected that as the total radiation dose received by a device increases, the number of ions formed in the ambient will also increase. As a result, the charge accumulated on the device surface and hence the degradation is expected to be, at least approximately, proportional to the total radiation dose. To some extent Peck[23] observes this dependence through a reciprocity of dose rate and time for dose rates not too different in magnitude, as shown in Figure 18. Reciprocity is also observed at dose rates as low as 5 rads/hr.

There are, however, reasons why the degradation should not necessarily follow this simple dependence on total dose. Devices do show recovery, so there must be some leakage process at the surface which counteracts charge accumulation.

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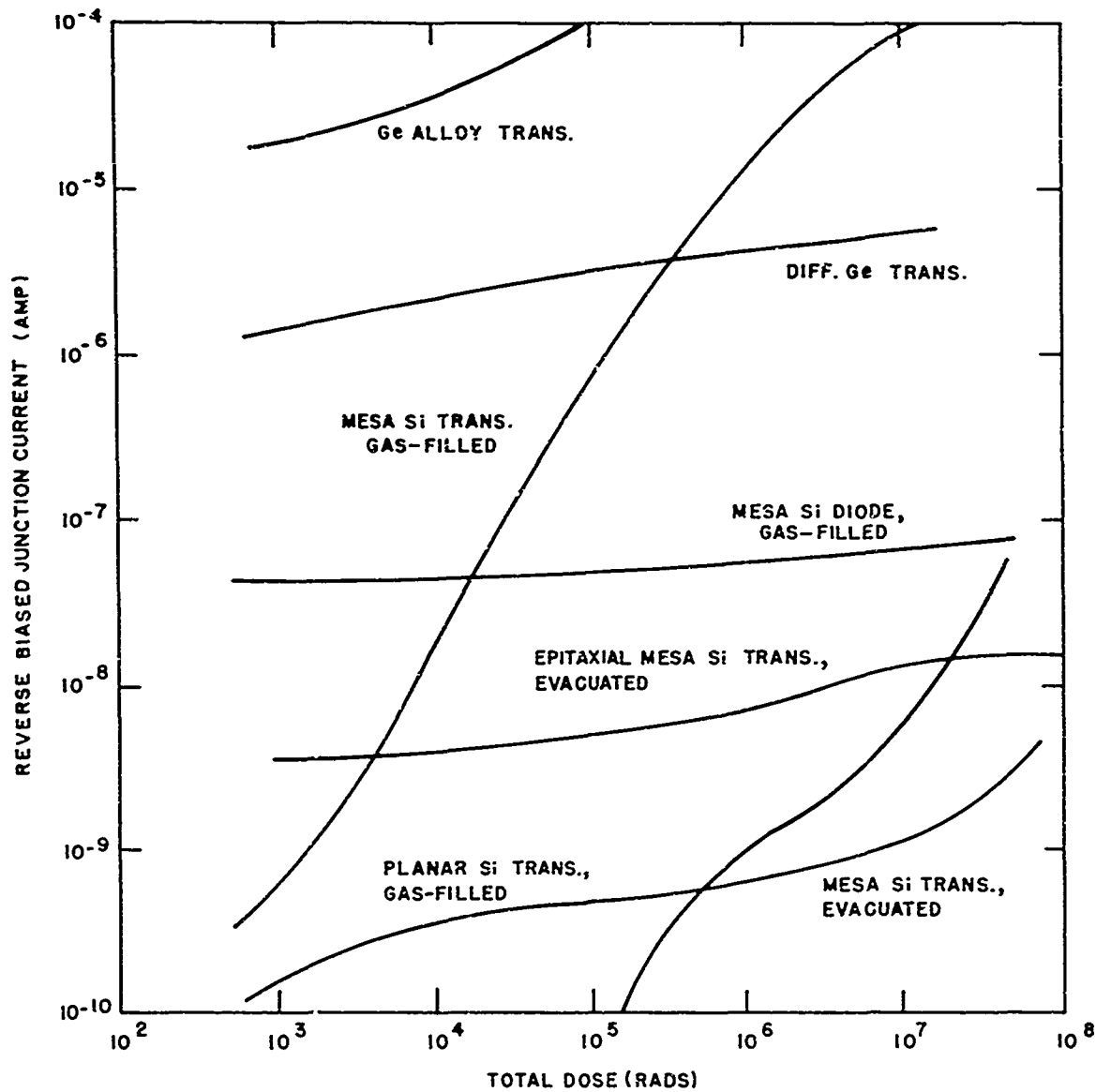
Figure 17.   Typical results for I_{CBO} degradation of several transistor types

Recovery, however, usually takes place at rather slow rates and it is likely that at all but very low dose rates such leakage processes are negligible.   At sufficiently high dose rates, on the other hand, it is possible that virtually all the ambient gas atoms are ionized and a further increase in dose rate will not cause a corresponding increase in the rate of degradation.

A saturation effect is also expected from the model discussed above.   There is a limit on the amount of charge which can be accumulated on the device surface, because of the limited number of slow states available or the electrostatic repulsion of additional incoming ions.   When this point is reached, the degradation will saturate.
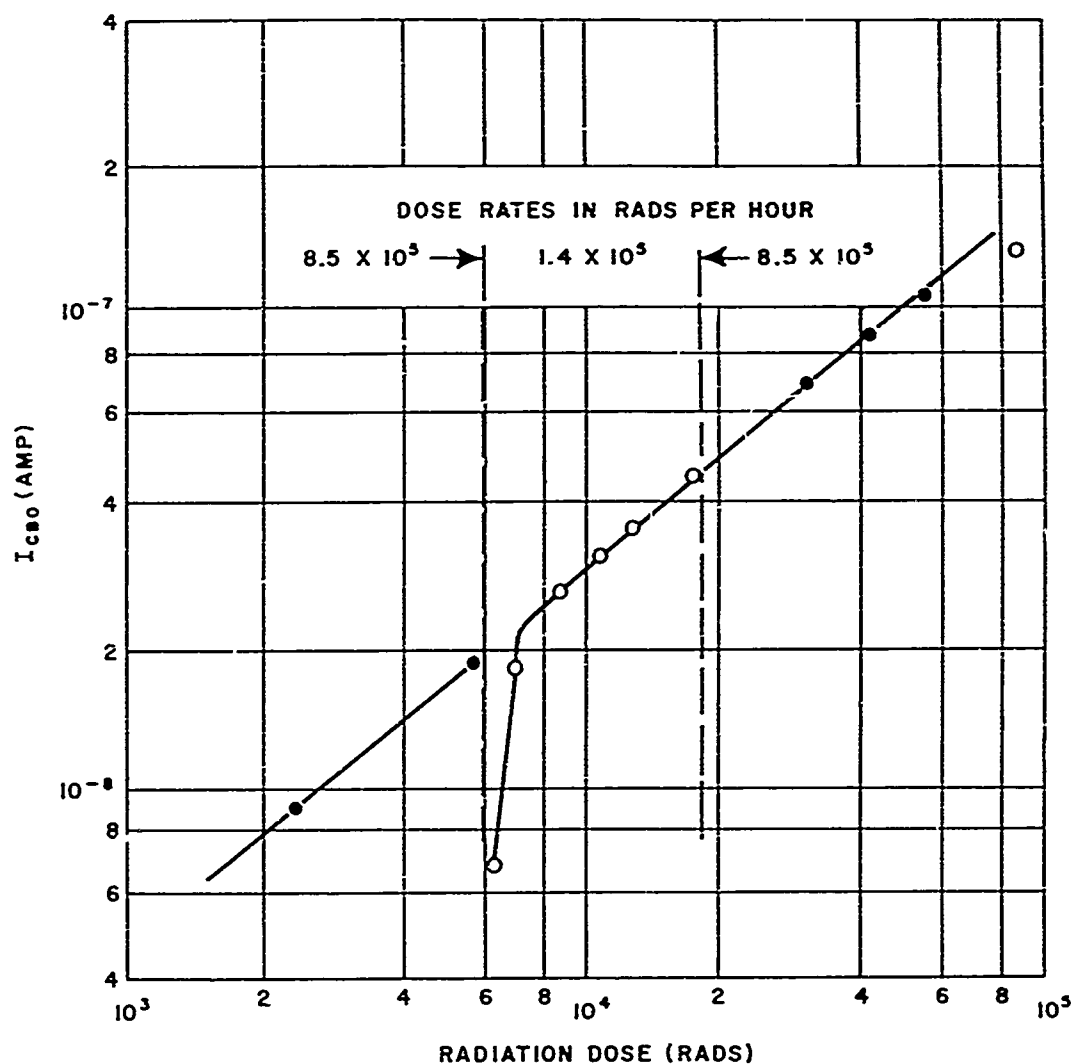
Figure 18. Reciprocity of dose rate and time
at two high radiation dose rate levels

Both dose rate and saturation effects are inherent in the model, but, at present, there are too many variables which could influence these effects to allow even qualitative predictions. It is impossible, for instance, to explain why Ge transistors (particularly pnp) show saturation of I_{CBO} while Si transistors, in general, do not.

I. Effect of Bias and Can Potential

Since the electric fields created by the collector junction bias are intimately involved in the degradation process, one should expect the increase in I_{CBO} to be strongly dependent on applied bias. Experimentally, it is generally found that non-passivated devices experience degradation only when subjected simultaneously to radiation and reverse bias on the collector junction. The necessity of the

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combination was pointed out by Peck and his associates.[23] Figure 19, which schematically illustrates their results, shows that separately neither bias nor irradiation produces degradation; in combination, however, severe I_{CBO} degradation is produced. The effect of bias voltage is further illustrated in Figure 20, which shows the increase in I_{CBO} with dose for various collector biases.[23] Also, it has been shown that if the bias voltage is raised while a device is under irradiation, the rate of increase of I_{CBO} will become larger.[29] If the bias voltage is subsequently returned to its original value, the rate of increase of I_{CBO} will be reduced to the corresponding value.
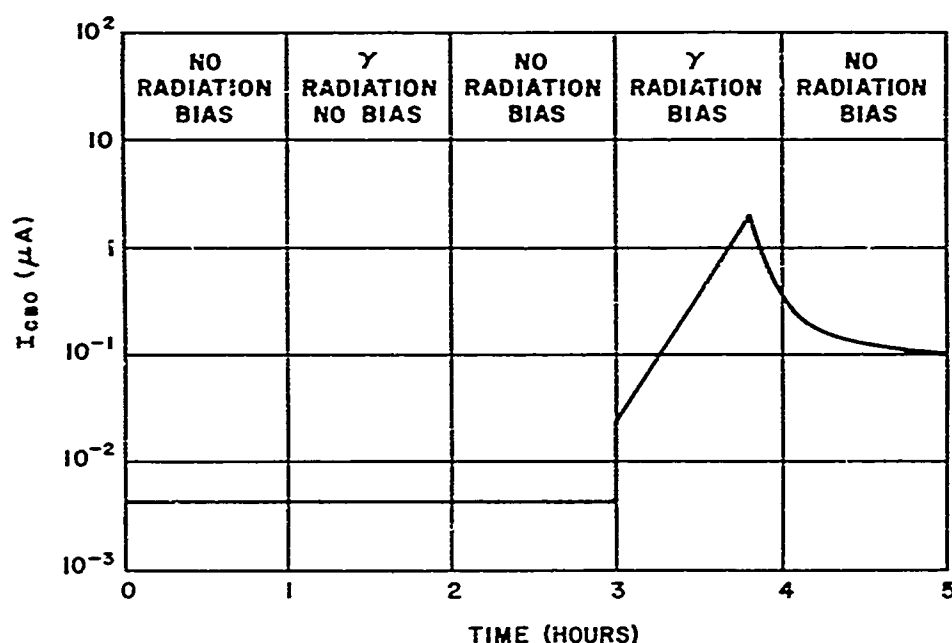
Figure 19. The response of I_{CBO} of a diffused Si transistor to either radiation or bias alone or to both together

Another electric field which might be expected to influence the behavior of an irradiated device is the field between the semiconductor and the encapsulating can. Results have been obtained by Peck[23] with a Ge transistor whose can-to-semiconductor potential was periodically reversed during irradiation. The increase in I_{CBO} was substantially enhanced when the can was positive with respect to the semiconductor. This result would seem to indicate that positive gaseous ions generated in the gas ambient were responsible for depositing charge on the device surface. This method of surface charge accumulation is in agreement with the model outlined above. Peck points out, however, that lack of reproducibility of results leaves this point open to question. Nevertheless, the can-to-semiconductor potential is important.
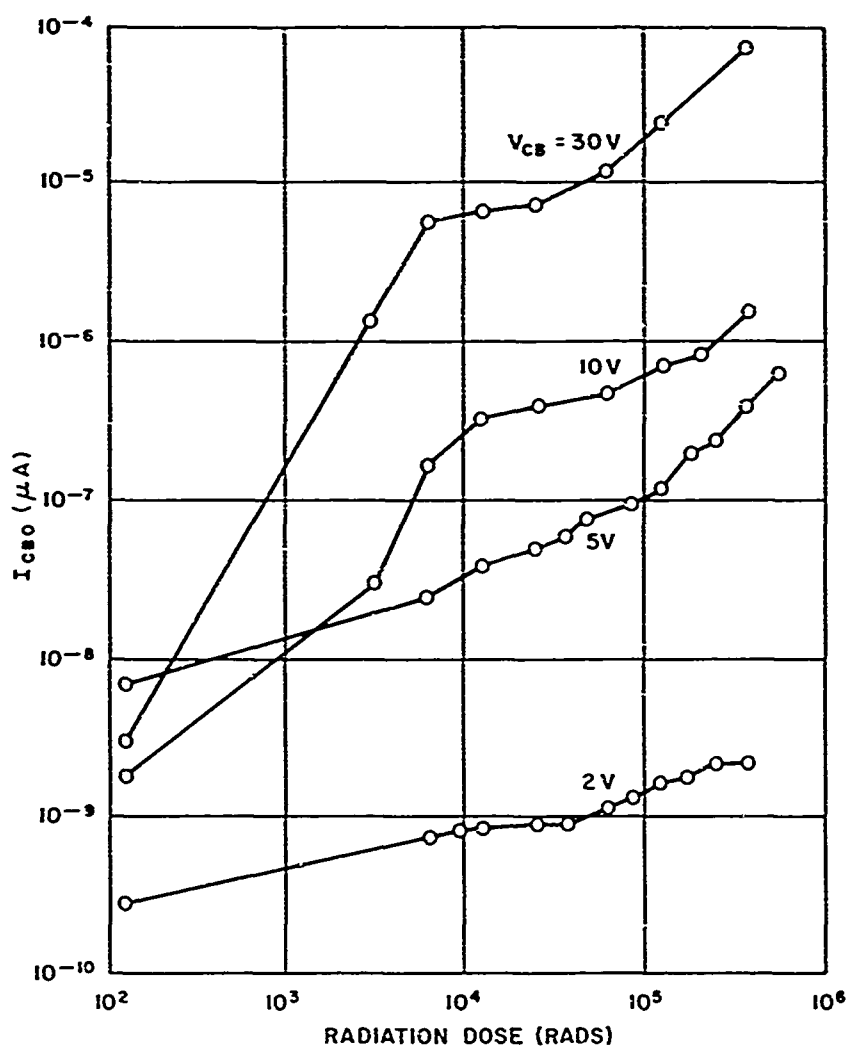
Figure 20. Dependence of I_{CBO} degradation
on collector bias

J. Recovery

From the model, one would expect a transistor to show recovery of I_{CBO} degradation under certain circumstances. Reducing the bias and hence the electric field at the junction should release the charge trapped on the surface and allow it to disperse. The presence of radiation with the bias removed should further enhance the recovery rate by providing electrons to help remove the positive surface charge.

Experimentally, the degraded I_{CBO} shows various rates and degrees of recovery depending on several factors. The effects of bias and radiation on recovery rate of gas-filled Si transistors, as reported by Blair,[27] are shown in Figure 21. In part A of the curve, the transistor has been removed from radiation but is still under bias. When the bias is removed (part B), the rate of recovery is increased,

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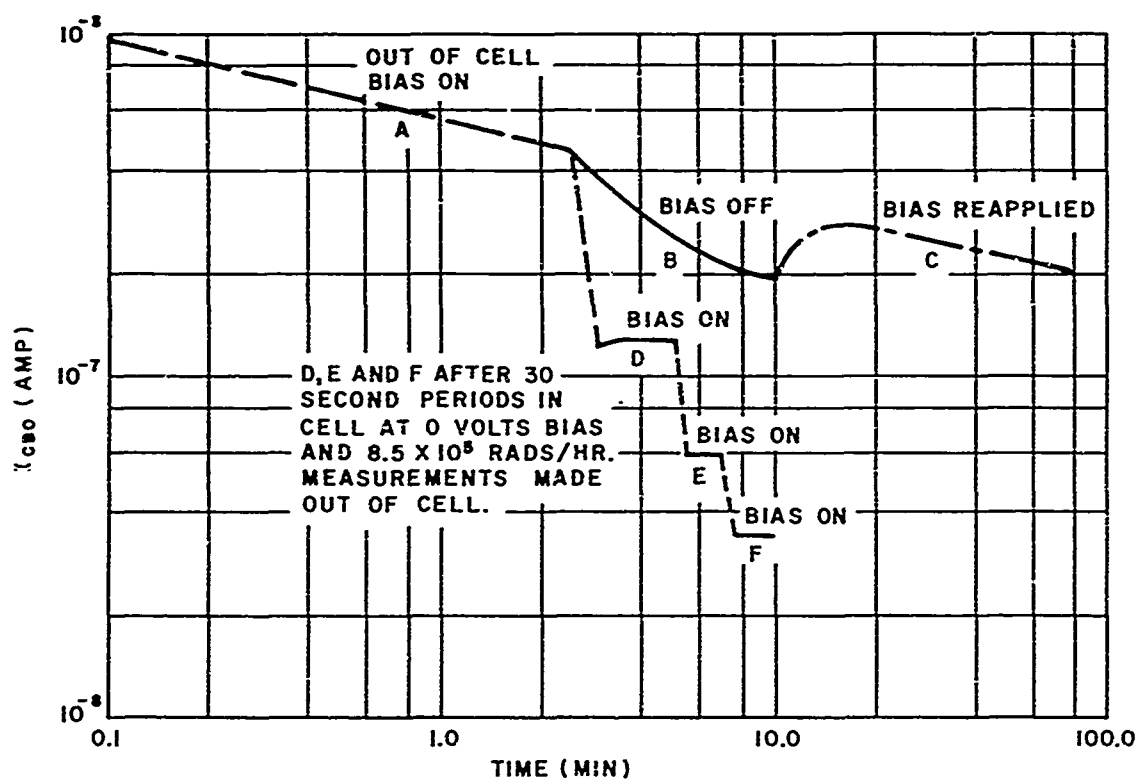
Figure 21. Influence of bias and radiation on I_{CBO} recovery

but upon reapplication of the bias (part C), the recovery rate is again reduced. The most rapid recovery is achieved (prior to parts D, E, and F), if the device is irradiated at 0 volt bias.

Although I_{CBO} usually appears to recover its original value after a sufficient length of time, it is found that subsequent, relatively small doses of radiation will bring I_{CBO} rapidly back to its previous high value. This so-called memory effect is illustrated in Figure 22 for a device irradiated after one month of shelf recovery time.[27] Apparently the recovery was only superficial and some part of the original damage was still present. Blair reports that even after an additional 15 months of aging the memory effect persisted. However, several authors report the memory effect can be eliminated if the devices are exposed to elevated temperature ($\gtrsim 100\,^{\circ}$C).

This memory effect is quite similar to that mentioned above in the work of Estrup for Si exposed to positive ion bombardment (see Figure 10). Estrup suggested that the effect was caused by a two-step discharge process which left the surface states in an "active" but uncharged condition for long periods of time before returning to the normal condition. Estrup offered no elaboration on the nature of these "active" states. However, the fact that the memory can be eliminated by

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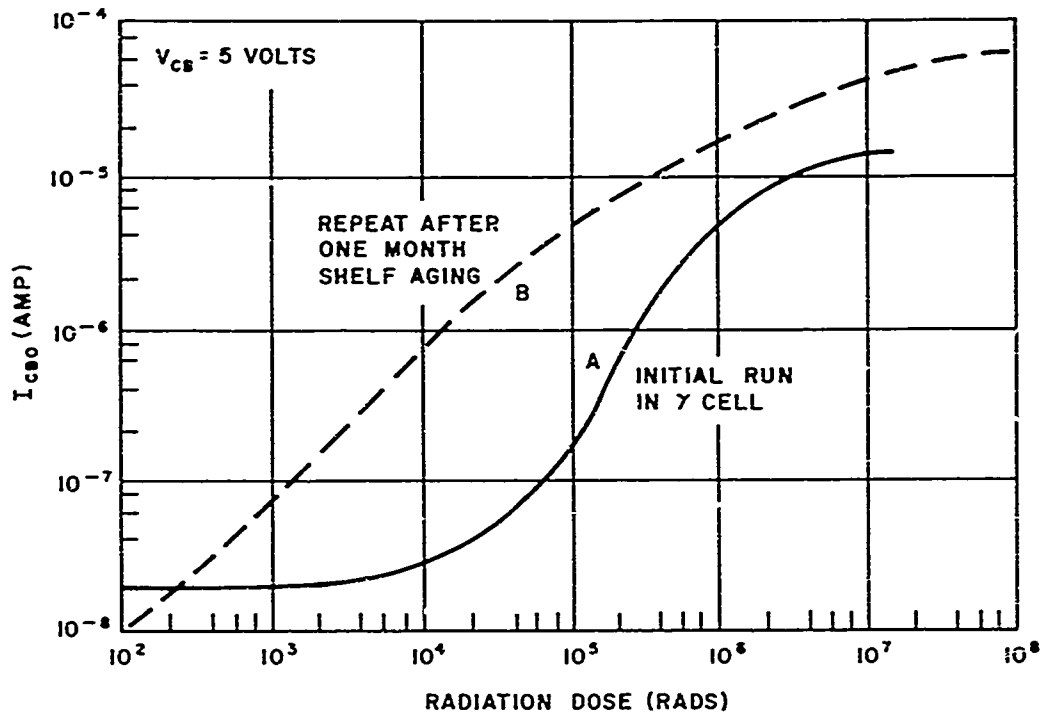
Figure 22. Si transistor "memory" of radiation after annealing
at room temperature

rather small increases in temperature would indicate that the cause of the effect is some small difference between "active" and normal states which anneals out easily.

K. Dependence of Surface Effects on Radiation Type

Since the primary effect of the radiation is the ionization of the gas in the transistor can, it would seem likely that the degradation should be independent of the type of radiation. Peck[23] has compared the effects of Co^{60} gamma rays and 18 MeV protons and finds that the radiation dose is significant, but he can discern no great difference between the effects of the two types of radiation.

L. Effects of Device Ambient

Many manufacturers attempt, for various reasons, to control the nature of the device ambient by using vacuum, various types of gases, or greases inside the can. These ambients, while in some cases performing the function of passivation, are not an integral part of the device surface and should not be confused with passivation techniques to be discussed later. Although the model discussed previously treated a gaseous ambient specifically, the same general approach should be applicable to other ambients.

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The model should be most easily extrapolated to the case of a vacuum ambient. One would expect a marked decrease in radiation sensitivity for this ambient since gaseous ions are no longer present to create a surface charge. Figure 23 shows a comparison between gas and vacuum ambients for two types of device.[23] As expected, the evacuated devices are less sensitive to radiation.
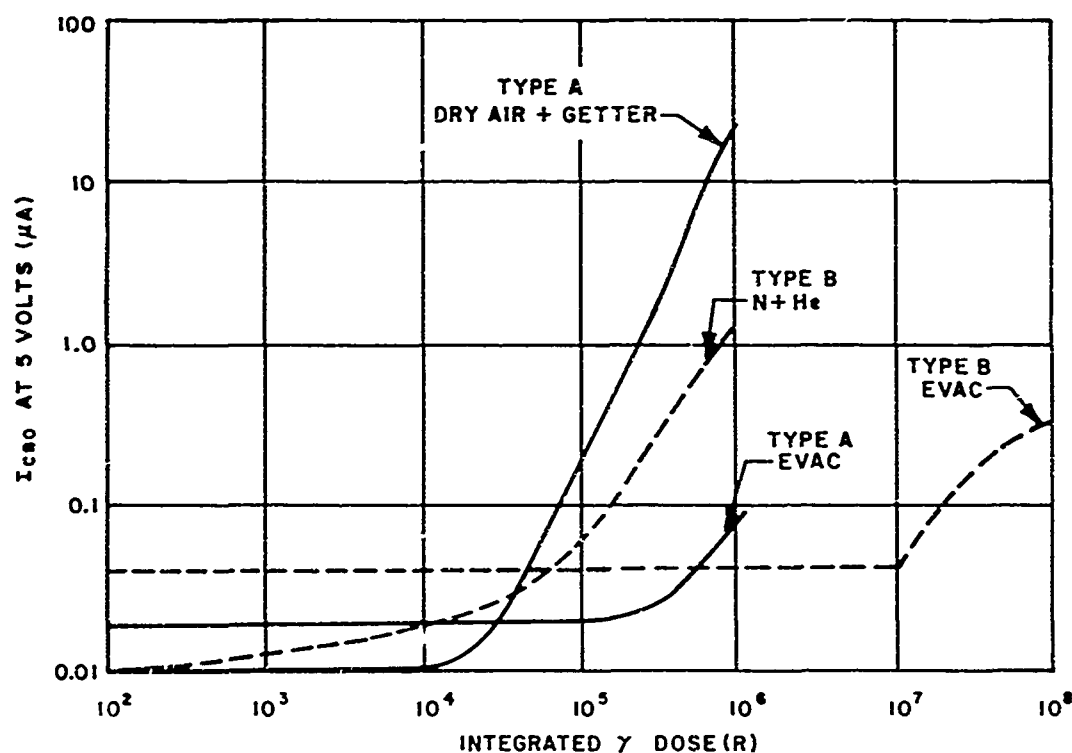
Figure 23. Radiation degradation of I_{CBO} of two types of diffused Si transistors, evacuated or with gas filling

The situation with grease-filled cans is somewhat more uncertain, and the simple model put forward above would require some refinement to account for the observations. Steele[25] reports that for Ge pnp alloy transistors the presence of silicone grease increases I_{CBO} degradation over values found for the same transistor without grease.

For Si grown junction npn transistors encapsulated in a silicone grease, on the other hand, I_{CBO} was found to saturate with dose, and the saturation value was significantly smaller with grease present. Infrared transmission studies of the grease from Ge devices before and after a 5×10^7 roentgen radiation dose showed that irradiation caused an increase of available hydrogen bonds which were presumably able to interact with the surface. The mechanism causing the change in

radiation sensitivity would thus appear to be a surface one, but the reason for the opposite effect on Ge and Si devices is not clear.

A saturation effect for I_{CBO} for silicone grease-filled Si alloy transistors has also been reported by Peck.[23] In fact, as shown in Figure 24, I_{CBO} decreases with dose after reaching a maximum. These devices, when exposed to short periods of high intensity radiation, showed only minor changes in I_{CBO}, but showed severe degradation in the periods subsequent to irradiation. These results might indicate production of ions in the grease which require time to migrate to the device surface.

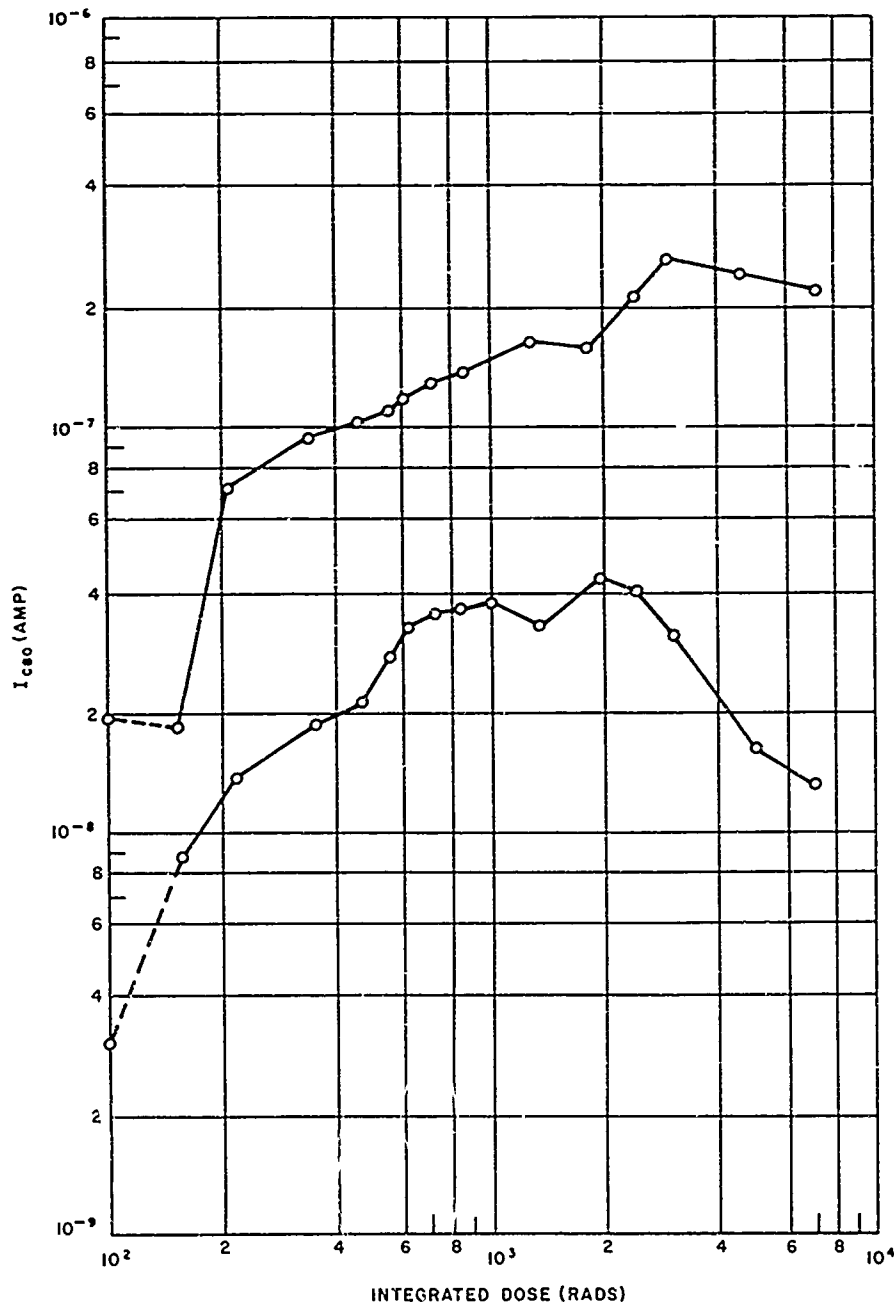Figure 24. Response of a grease-covered Si transistor under prolonged radiation at 5 rads/hr

35

It has been reported that silicone grease also decreased the radiation sensitivity of one type of Si grown junction transistor.[30] After a study of several types of transistors and various case fillings, however, no direct correlation was found between the presence or absence of grease and sensitivity to radiation.

M. Effects of Radiation on h_{FE}

As has been noted, the principal measurements of surface effects of radiation on nonpassivated transistors have emphasized I_{CBO} changes. Because the changes in other transistor parameters are much smaller, they have, to a large extent, been neglected. As will be seen later in the case of passivated transistors, changes in current gain and I_{CBO} are comparable, and studies of changes in other transistor parameters are more extensive. The effects of radiation on transistor parameters other than I_{CBO} have been studied by Zagorites and his associates.[26] They found for both npn and pnp Si devices a negligible change in h_{FE} for Co^{60} gamma doses up to 1.3×10^4 rads. For Ge devices, on the other hand, the changes in h_{FE} were quite large and somewhat erratic. Figure 25 shows the change of h_{FE} for three npn transistors. In each case the gain decreased by about a factor of two, although the authors claim h_{FE} for some other npn devices increased by the same factor. The changes in h_{FE} correlated strongly with changes in I_{CBO}, and Zagorites suggests that this is evidence for a common mechanism of degradation for h_{FE} and I_{CBO}. On the other hand, h_{FE} for pnp Ge transistors showed both increases and decreases, with no clear pattern emerging.

The effects of radiation on the collector family curves of some Si transistors have been studied by Blair.[27] His results are shown in Figure 26. A small 16 kc/s current has been superimposed on the base current steps to indicate the effects of radiation on the ac characteristics. For transistor number 50, a dose of 1.3×10^7 rads caused a small increase in I_{CBO} and a slight decrease in h_{FE}. The change in common emitter ac gain, h_{fe}, is also seen to be small. Transistor 44 is of the same type as 50 but showed a much larger increase in I_{CBO} for a dose of 10^7 rads. The amplified leakage current appears in the collector current and causes the apparent increase in h_{FE}.

For further comparison, the characteristics for a vacuum-encapsulated Si transistor are also shown in the figure. At a dose of 2.1×10^7 rads this device shows no increase in I_C at $I_B = 0$, and ac and dc gain decreases of about 20 percent. Of course, no general conclusions can be drawn from these curves but the type of degradation to be expected is well illustrated. The comparison of the curves for transistors 50 and 44 again emphasizes the variability of response between even two supposedly identical devices.

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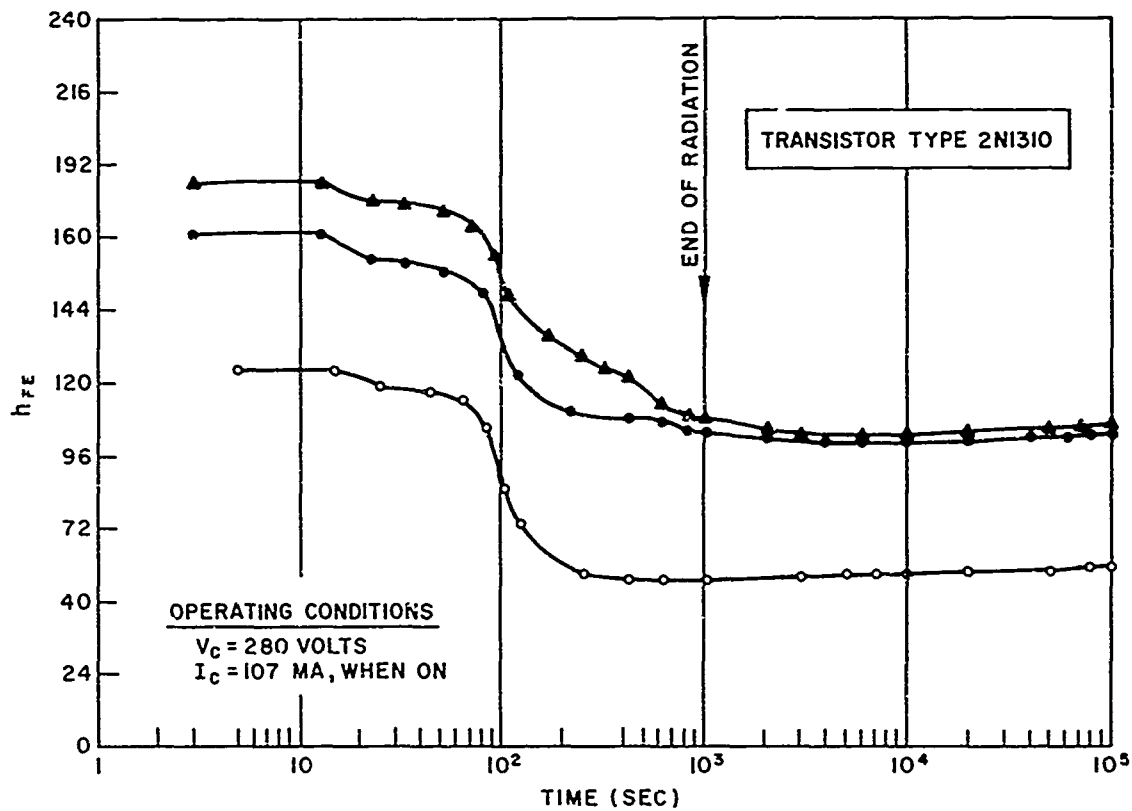
Figure 25. h_{FE} vs time for three npn transistors

N. Telstar Experiment

Perhaps the best known example of radiation-induced surface effects on semiconductor devices occurred when the command circuits of the Telstar satellite failed in November 1962.[1] After about four months of successful operation in orbit, the satellite gave indications of serious trouble in the command decoder, and within a few days the circuits failed completely. The maximum radiation dose rate ($\sim 10^3$ rads/hr) seen by the satellite was ~ 100 times greater than anticipated, probably as a result of a high-altitude nuclear explosion in July 1962. Several possible causes of the failure were considered and all except surface effects due to radiation on the transistors were ruled out because of lack of supporting evidence or correlation with the observed failure symptoms.

In an effort to discover more about the effects of ionizing radiation on the command circuits, circuits similar to those used in the satellite were cycled between high and low dose rate Co^{60} gamma radiation with the same period as that of the satellite in the radiation belts. The radiation-sensitive transistors in these circuits were nitrogen-encapsulated, diffused Si types. The transistors in the circuits showed the expected response to radiation, i. e. , I_{CBO} and h_{FE} degradation

37

Figure 26. Radiation effects on collector family curves of silicon mesa and epitaxial-vacuum transistor types; small 16-kc signal added to base current steps

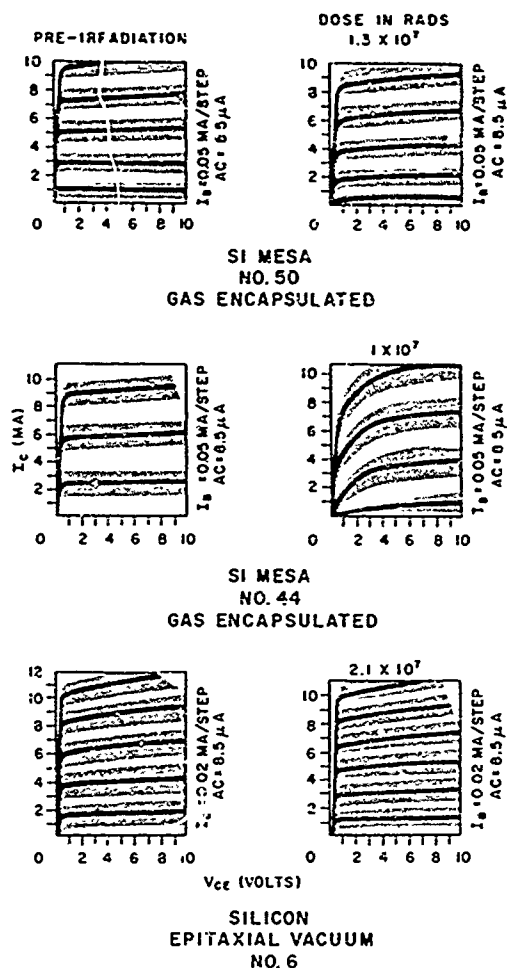at high dose rates followed by some recovery at low dose rates. The recovery was enhanced by reduction of bias, especially if the dose rate was high. A wide range of memory effects was also observed. Failure in one irradiated circuit was traced to h_{FE} degradation of one transistor, while failure in another circuit was attributed to an I_{CBO} increase.

After a careful analysis of these laboratory tests, attempts were made to rejuvenate the Telstar satellite circuits. Several unsuccessful attempts were made using various approaches. Finally, success was achieved with modified commands designed to circumvent one particular circuit which was assumed to have failed. The satellite then responded to subsequent commands and after some further manipulation the circuits were fully operational.

The exact reason for recovery is not known but was probably a combination of two effects. First, the dose rate seen by the satellite had decreased significantly from the value which first produced failure, with a consequent decrease in surface effects. Second, the suspected circuits were given a series of continuous commands. This manner of operation caused the normally off transistors (high V_{CE} and high rate of degradation) to have a decreased average bias voltage. Under these conditions, the surface degradation is decreased and recovery proceeds more rapidly.

O. Miscellaneous Nonpassivated Devices

1. Introduction. The discussion thus far has been limited to transistors and diodes. However, other semiconductor devices, not necessarily junction devices, are also sensitive to surface effects and are just as likely to be exposed to radiation. Unfortunately, there has been very little investigation of these devices, at least as far as surface effects of radiation are concerned.

2. _Solar Cells._ Solar cells will be exposed to radiation mainly in space applications, and studies of radiation effects on these devices have been made with these applications in mind.[31,32,33,34] Results obtained by Rosenzweig and others[34] indicate that the Si n/p cells presently used are most likely to degrade from bulk rather than surface radiation damage because most of the minority carrier generation in these devices takes place well below the surface. The importance of bulk damage is illustrated in Figure 27, which shows the percent quantum efficiency as a function of wavelength for an n/p Si solar cell after various doses of 1 MeV electrons. It is evident that the efficiency is most affected at the longer wavelengths, those at which carrier generation occurs well below the surface, i. e. , in the bulk damage region. It should be pointed out that similar optical studies could be quite useful for investigating surface effects in other semiconductor devices. In particular, they can be used to distinguish between surface and bulk effects as illustrated here for solar cells.

There has been recent interest in GaAs solar cells, since these devices approach Si solar cells in conversion efficiency and may, for some applications, be more radiation resistant.[31,35] Minority carrier generation near the surface is more important for GaAs solar cells, however, and it is possible that changes in surface recombination due to radiation are important on these devices.

3. _Radiation Detectors._ Radiation detectors in the form of specially designed reverse-biased diodes require stable surface properties to keep the noise level as low as possible. Detectors used in Telstar satellites used bare, etched, diffused p-n junctions inside a tight can back-filled with nitrogen containing a trace of oxygen. It was found necessary to add the trace of oxygen to stabilize the diodes against gradual increases in reverse current.

These detectors were tested for surface effects due to radiation by exposing them to 50 rads/hr gamma radiation while under intermittent reverse bias.[36] The devices showed a wide range of responses as observed in reverse current measurements. However, none of the devices showed serious permanent effects due to irradiation. In space, on the other hand, two detectors out of 18 did show significant surface-generated noise after several months of operation at radiation levels higher than expected.

Oxide-passivated surfaces in place of bare, etched surfaces have not been tested for these devices, but based on the experience with passivated transistors one might expect to find problems in the form of charge storage effects at the $Si-SiO_2$ interface.

4. _Metal-Semiconductor Junctions and Heterojunctions._ The region of the interface between two materials, such as a metal and a semiconductor, is obviously
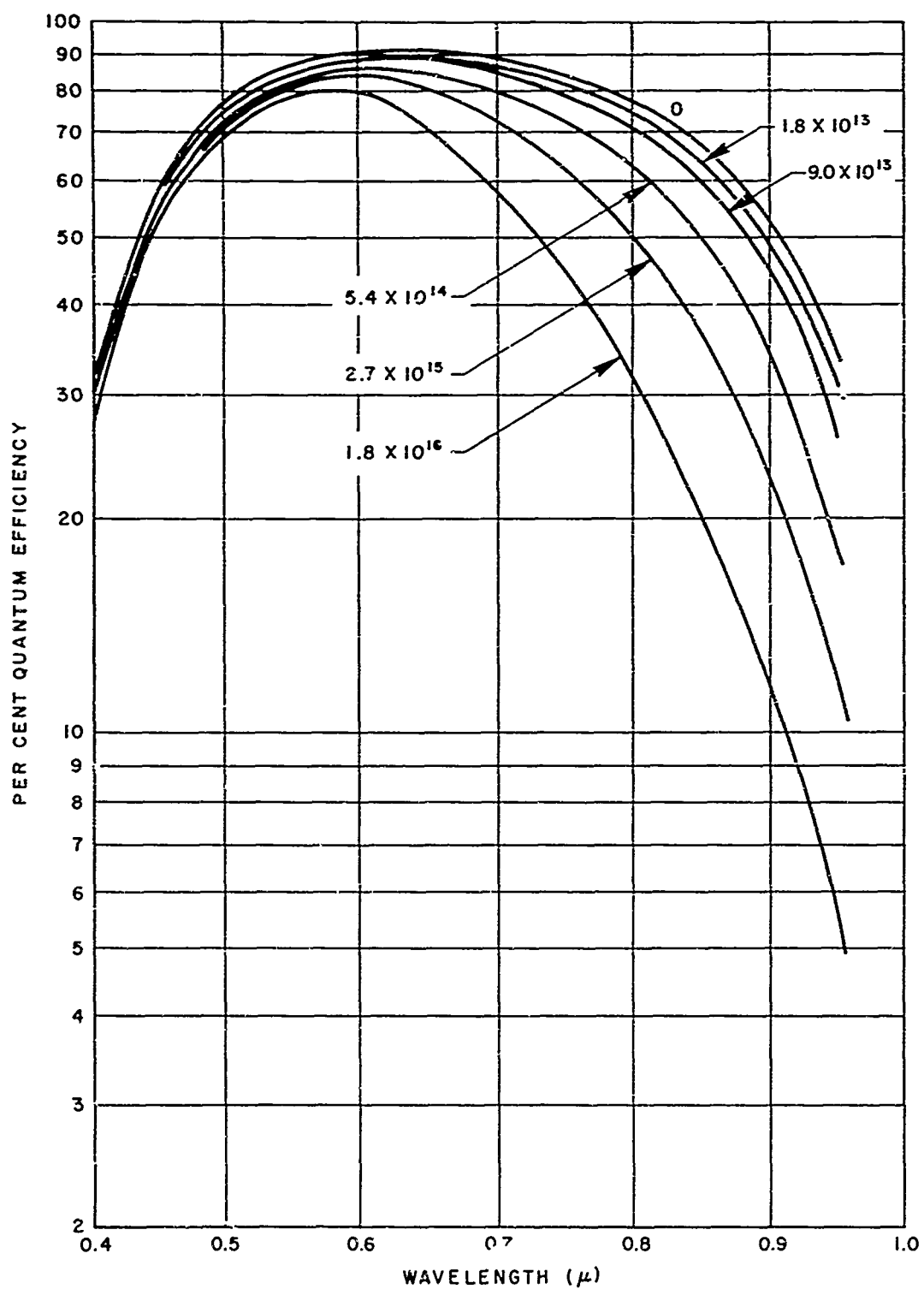
Figure 27. Percent quantum efficiency vs wavelength
after various levels of bombardment for n/p cells

not a true "bulk" region from a radiation effects point of view since it is a small region not typical of either material. Similarly, it is not a "surface" region in the usual sense of the word. Nevertheless, such interfaces are important and it is worthwhile here to broaden the definition of a surface to include interfaces and to discuss interfaces as they concern radiation effects.

It is difficult to predict what effect radiation will have on an interface region, since little is known about these regions and almost no experimental investigations have been carried out. However, it is known that, at metal-semiconductor junctions and heterojunctions, the crystallinity is either nonexistent or at least badly disturbed. As a result, these regions are likely to contain numerous trapping centers. Radiation may alter the number of these centers or the charge they contain, and hence may alter the characteristics of the device containing the interface.

There has been an indication that radiation does affect a metal-semiconductor interface.[37] The saturation current of an Ag surface barrier GaAs varactor was found to decrease 10 to 20 times after receiving a fast neutron dose of $10^{15}/cm^2$. Similar diffused GaAs varactors, on the other hand, showed the more typical increase in the saturation current. This increase is presumably caused by usual bulk effects. The unexpected decrease in saturation current of the surface barrier devices, however, is suspected to result from an increase in the barrier height of the interface. Such an increase could result from a change in the charge contained in the interface states as a result of irradiation.

Such radiation-induced changes in the metal-semiconductor barrier height could also affect the characteristics of commonplace p-n junction devices through their many metal-semiconductor junctions. However, no direct study of such effects has yet been made.

5. PASSIVATED DEVICES

A. Introduction

In recent years Si planar devices have assumed an increasing importance in the transistor industry. There are several advantages of planar devices over other device types such as alloy or mesa. One of these advantages is that the Si planar device lends itself naturally to an oxide surface passivation, which is quite effective in reducing the surface stability problems encountered in other types. At present only Si devices can be passivated by the oxide technique; there is yet no comparable passivation technique for Ge devices. The discussions in this section are understood, therefore, to apply to Si and Si devices.

As far as the effects of radiation on planar devices are concerned, it will be seen that the surface passivation layer itself plays a very important role. For this reason a short discussion of Si surface passivation and its effects on devices will be given to serve as a basis for the subsequent discussion of radiation effects.[38]

The electrical requirements of an ideal passivation material have been given by Young and Seraphim[39] as follows:

1. The semiconductor surface potential must not change significantly with time under the stress conditions that are encountered by the device.

2. The semiconductor surface potential should be optimum for the particular device under consideration.

3. In those types of devices.which require reasonably small values of the surface charge density and the surface recombination velocity, these characteristics should also be accomplished by the passivation.

The passivation used on planar devices is by no means perfect, but it does approach these ideals reasonably closely.

In practice, passivation of silicon devices is accomplished with a film of the oxide, SiO_2, which is thermally grown on the device surface. Because of the intimate contact between the oxide and semiconductor surface, this film stabilizes the surface and isolates it from the ambient. However, this type of passivation places the surface of the device in contact with a material which interacts in a complicated way with it and with the ambient. It has become apparent that if one is to understand the behavior of passivated devices one must understand the charge storage and transport mechanisms which occur in the thin layer of passivation material.

B. Silicon Dioxide as a Passivation Material

1. Effect of SiO_2 on an Si Surface. An extensive experimental study of SiO_2 as a passivation material has been made by Atalla and his associates.[40,41] They found that oxides grown at temperatures of about 1000°C in dry or wet oxygen are continuous, amorphous, and stable over long periods of time. Using field effect techniques, they further found that oxide-covered Si surfaces showed no effects due to slow states, and that the presence of either wet or dry oxygen or nitrogen caused no shifts in surface conductivity resulting from the presence of slow surface states. The presence of surface impurities on the semiconductor before oxidation, however, was found to be very important and, depending on preoxidation conditions, diode reverse currents from 10^{-10} to 10^{-3} A could be obtained. Reproducible ressults were only obtained if the treatment of the surface before oxidation was carefully controlled.

A study of floating zone silicon which had been thermally oxidized showed that both donor and acceptor type fast surface states were present with concentrations from 10^9 - 10^{11} per cm^2.

After oxidation, the floating zone material generally had a p-type surface, indicating a predominance of acceptor states. Again there was no evidence of slow states on the oxide surface. On the other hand, oxidized surfaces of pulled crystal Si showed strongly n-type surfaces. The discrepancy between the Si surface types after oxidation for the two types of Si was traced to fast diffusing impurities in the body of the pulled crystal, which were gettered by the surface oxide.

It has been shown that acceptor states arise at the interface between two dissimilar crystals in a similar manner to the formation of the so-called Tamm acceptor states which arise at a clean crystal surface. Based on this fact and the work outlined above, Atalla proposed the following model for surface oxide layers. At the $Si-SiO_2$ interface, a region of gradual transition from crystalline Si to amorphous SiO_2 occurs, and it is assumed that Tamm-like states exist in this transition region. These states together with states arising from vacancies caused by mismatch between the Si and SiO_2 are acceptor states. Donor states arise only from impurities at the interface.

2. Charge Storage Effects in SiO_2. Recent investigations have revealed charge storage effects in SiO_2 films such as those used for surface passivation on Si devices. Yamin[42,43] has studied the charges in thermally grown SiO_2 films using a $Si-SiO_2$-metal sandwich. The Si used was either n- or p-type, the oxide was typically 6000 Å thick, and the metal was usually Al or Au in the form of a circular dot. Yamin investigated the charge flow in and out of these devices for Si potentials between ±5 volts with respect to the metal at temperatures from 200°C to 400°C. At negative Si potentials, it was observed that the amount of charge entering the device was much greater than expected from the device capacitance. Furthermore, the excess charge could be recovered if the Si potential was again made more positive, or it could be stored almost indefinitely in the device if the leads were opened. Yamin demonstrated that the charge storage was associated only with the oxide directly under the metal dot and estimated its density to be 4×10^{12} to 2×10^{14} charges/cm^2, depending primarily on the method of preparation of the oxide. Devices which were baked for 15 minutes at 1000°C in dry oxygen, nitrogen or hydrogen showed a spontaneous discharge at 400°C corresponding to charge densities in the oxide of $\sim 10^{12}$ charges/cm^2. Since these devices had not been previously voltage-stressed, it appears that thermally produced oxides may contain a built-in charge. A study of the conductivity of the Si beneath the oxide showed that the conductivity became more n-type, indicating that positive charge was being stored.

Yamin has proposed a model to explain the observed charge storage. The model supposes the presence of mobile positive ions in the oxide which act as charge carriers. Yamin suggested that Na^+ ions may be the mobile species. This possibility is supported by the work of Snow a d others,[44] who have observed changes in the voltage-capacitance characteristics of metal-oxide-semiconductor structures under temperature and voltage stress and have explained their observations in terms of alkali ion transport through the oxide. On the other hand, Kerr and his associates[45] believe that oxygen vacancies rather than sodium ions are the charge carriers. They deduce this result from the effect of a phosphosilicate glass layer on top of SiO_2 passivation which was found to increase device stability. The P_2O_5 treatment which produces the phosphosilicate glass presumably supplies oxygen to the SiO_2 and thus removes the charge-carrying vacancies. Yamin[43] also finds that a P_2O_5 treatment eliminates the charge storage effects in his experiments. Other ions, such as the hydroxyl ion, also have been suggested as the mobile species. At present, however, the identity of the charge carrier responsible for charge storage effects in SiO_2 has not been definitely established.

C. Electrical Behavior of SiO_2 Passivated Devices

Atalla[41] has studied SiO_2 passivated p-n junctions under various conditions of bias and relative humidity and has proposed a model which satisfactorily explains his findings. Briefly, he found the reverse leakage current of the junction unaffected by moisture when the junctions were subjected to extended periods of forward or zero bias. For a steady reverse bias, however, the reverse current increased with time and saturated in a few hours at a value of about five times its initial value. The increase in current was a function of relati e humidity, bias voltage, and oxide thickness. Under normal conditions, the reverse current could be "frozen" at its saturation value for extended periods of time by replacing the wet atmosphere with a dry one but maintaining the bias voltage. The leakage current could be returned to its initial value by "swamping" the junction by exposing it to 100 percent relative humidity with no bias applied. By optically scanning the junctions, Atalla observed that the increase of reverse current occurred simultaneously with the formation of channels on both sides of the junction.

The following model was proposed by Atalla to explain the above observations. When the SiO_2 surface is exposed to moisture, a layer of water containing mobile ions is formed. When a reverse bias is applied to the junction, an electric field appears at the oxide surface in the region of the junction, Figure 28(a). This field causes mobile ions on the surface of the oxide to migrate, positive ions toward the p side, negative ions toward the n side. If the charge separation is severe enough, the semiconductor surface near the junction will become inverted and

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NEGATIVE ION MIGRATION ◄———————► POSITIVE ION MIGRATION

OXIDE

n   p

(a) ELECTRIC FIELD AT THE OXIDE SURFACE

OXIDE

+ + + +   - - - -

n   p

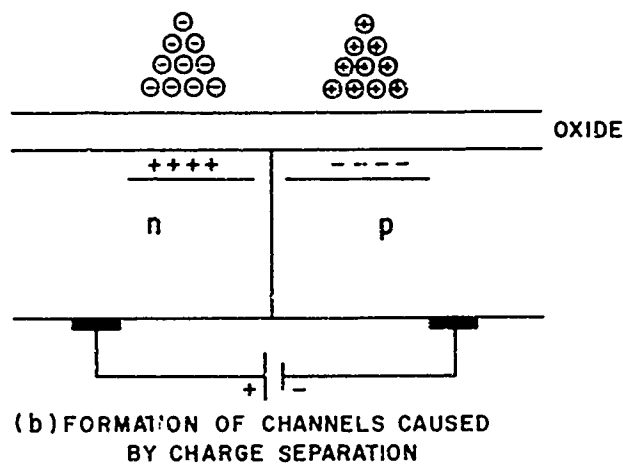(b) FORMATION OF CHANNELS CAUSED
BY CHARGE SEPARATION
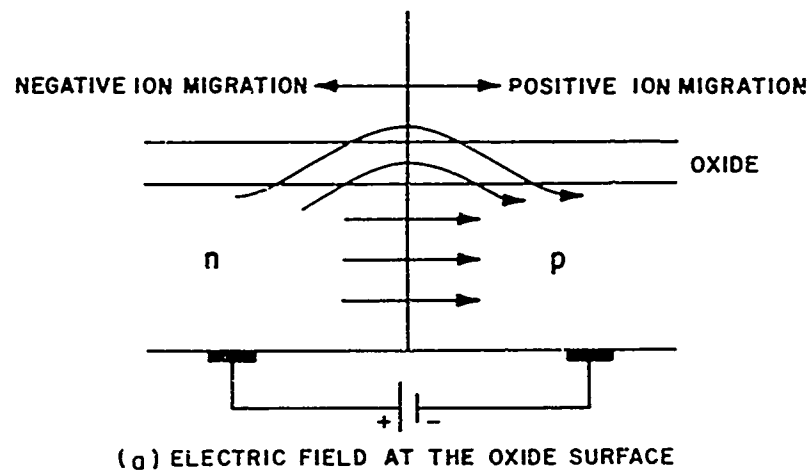
Figure 28.   Separation of the charge on the surface
of a reverse-biased p-n junction

channels will form, Figure 28(b). It is apparent that the effect depends on the
humidity and the field strength at the oxide surface, and in turn on the bias voltage
and oxide thickness. As with nonpassivated devices, the channels cause an increase
in reverse leakage current.

Failure mechanisms in SiO_2 passivated planar transistors were also studied
by Metz[46] who observed changes in the I_{CBO} vs bias voltage characteristics as the
devices were aged under operating conditions (emitter junction forward-biased,
collector junction reverse-biased). Again I_{CBO} degradation occurred at elevated
junction temperatures, with I_{CBO} increasing several orders of magnitude in some
cases. Metz found that the current increases were reversible and that I_{CBO} could
be returned to its original value by heating for several minutes without bias or by
removing the bias and opening the can, exposing the device to normal ambient

atmosphere. The model discussed by Metz is essentially the model proposed by Atalla and satisfactorily explains the observed recovery. Heating without bias increases surface ion mobility, and the separated ions redistribute themselves to a neutral condition through their mutual attraction field. Exposing the surface to ambient atmosphere (and hence moisture) also increases the ion mobility and hence promotes a neutralization of surface charge.

Atalla's model has received support from the work of Shockley and others[47,48] who investigated contact potential variations on SiO_2-covered Si surfaces using a Kelvin probe. They were able to account entirely for the observed variations by assuming the presence of mobile charges on the outer surface of the SiO_2, which migrated under the influence of applied electric fields.

In contrast to Atalla's model, in which the surface potential of the device is controlled by charges on the surface of the passivation layer, there is growing evidence that charge storage and transport effects within the SiO_2 passivation may be responsible for device degradation. If mobile positive charges do exist in SiO_2, as Yamin's experiments seem to indicate, it is possible that under the proper conditions serious degradation could occur. Electric fields will certainly exist in regions of the oxide near biased junctions and these fields could cause positive charge to accumulate at the Si-SiO_2 interface. Such a charge accumulation would, of course, strongly influence the surface potential of the adjacent Si and lead to degradation by the methods discussed earlier.

This model is supported by the work of Griffin and his associates[49] who have investigated the effect of Na contamination of the passivation layer on device stability. They concluded that Na ion migration through the oxide was an important cause of degradation of their devices. Snow and others[44] have also suggested that trace alkali impurities in the passivation oxide may cause reliability problems in devices operated at high temperatures and voltages.

Basically, then, it appears that surface conditions in passivated devices can be controlled by two possible mechanisms, charge storage in the SiO_2 layer and charge separation on the surface. Of course, it is possible that under some circumstances both mechanisms may be operative.

D. Results of Device Passivation

In spite of the problems of charges present in or on the surface of the SiO_2 film, passivation has unquestionably improved the performance of many silicon devices. I_{CBO} values are relatively low and very stable, surface recombination near the emitter junction is low and, consequently, achievable current gains are

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quite high. This reduction in surface recombination is quite important in extremely narrow base transistors because the junctions are so close to the surface.

Under almost all conditions of preparation, the charges stored in or on the oxide are positive and hence tend to induce n-type surface conductivity in any underlying material. In the case of npn transistors, such surface layers will tend to reduce the collector breakdown voltage and increase recombination in the base region (i.e., lower h_{FE}). On the other hand, for pnp transistors such surface conductivity results in unstable collector channels and very low recombination at the base interface. Current manufacturing processes for pnp devices stabilize the collector channels with a p^+ diffused guard ring about the collector junction. Because of the low recombination currents in the base, passivated pnp transistors have very high h_{FE} values down to very low emitter currents.

E. Radiation Effects on Passivated Devices

1. Introduction. The question of importance here is, of course, what effect passivation will have on the response of devices to radiation. Unfortunately, although a considerable amount of investigation has been carried out on passivation per se, the amount of work done on the effects of radiation on passivated devices is rather scant. Despite this handicap, however, some facts are fairly well established. In general, the effects observed are quite similar to those observed in nonpassivated devices and seem to be associated again with channels resulting from the formation of ions in the neighborhood of the surface. However, because of the variety of ways in which SiO_2 layers are produced, the nature and charge state of the ions before and after ionizing radiation are not reproducible.

2. Experimental Results. The effects of radiation on diffused planar diodes and npn transistors passivated with 1.3μ of thermally grown oxide followed by 1.3μ of fused lead borosilicate glass have been reported by Kerr.[50] Typical results for the devices, under 20 volts of reverse bias, are shown in Figure 29. The reverse current appears to saturate at a dose of 10^5 to 10^6 rads, and further investigation showed little change for doses up to 10^8 rads. There is no obvious explanation why the diodes are more sensitive to radiation than the transistors. Kerr also reports recovery of the leakage current degradation in one hour in radiation at a 1.9×10^5 rads/hr dose rate with no bias and recovery in longer periods with bias and no radiation or with no bias and no radiation. This author has also compared SiO_2-protected devices, with similar varnish-protected Si mesa diodes. The superiority of the SiO_2-protected devices is shown in Figure 30. The degradation is about an order of magnitude smaller for the oxide-covered diodes.

The effects of low-energy X-rays (150 keV) on the ac and dc current gains of SiO_2-passivated npn planar transistors have been investigated by
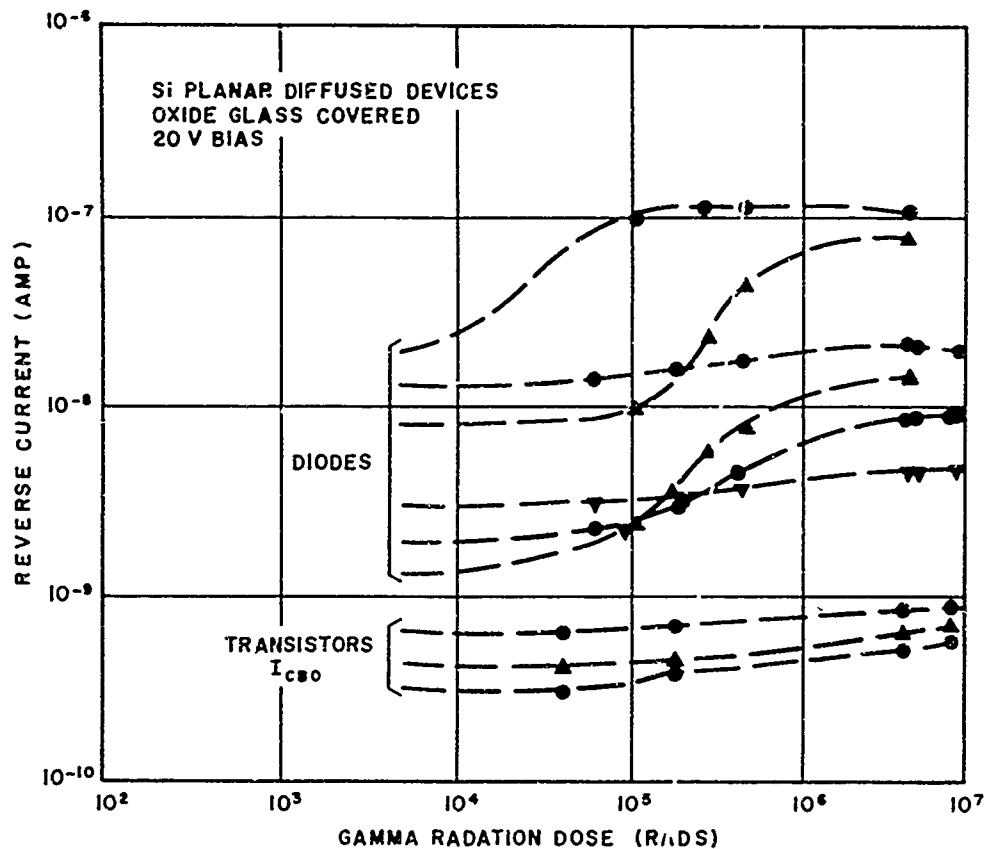
Figure 29. Degradation produced by reverse bias and
γ-irradiation of oxide-glass covered planar diodes
and transistors

Taulbee and others.[51] At such low X-ray energies, atomic displacement effects
should be negligible. The degradation of dc gain for three devices irradiated in
the passive condition (i. e., with no bias applied to either junction) appeared to satu-
rate at a dose of about 10^7 rads. The effect of the degradation was strongly depend-
ent on the emitter current, I_e, as shown in Figure 31. In this figure, $1000/h_{FE}$ is
shown as a function of I_e for the three devices before and after exposure to
10^7 rads of 150 keV X-rays. The effective degradation is much more severe at
low emitter currents with current gains falling to as low as unity at 1 μA.

Taulbee found that the effects were also dependent on junction bias applied
during the irradiation. The gain degradation increased if either junction was
reverse-biased and decreased if either junction was forward-biased.

The X-ray-induced damage appears to be relatively stable under shelf-life
conditions. Over a period of 200 days, the irradiated devices recovered about
20 percent with no significant difference observed between devices with and without
cans. Recovery was achieved if bias was applied to the transistor, high values of
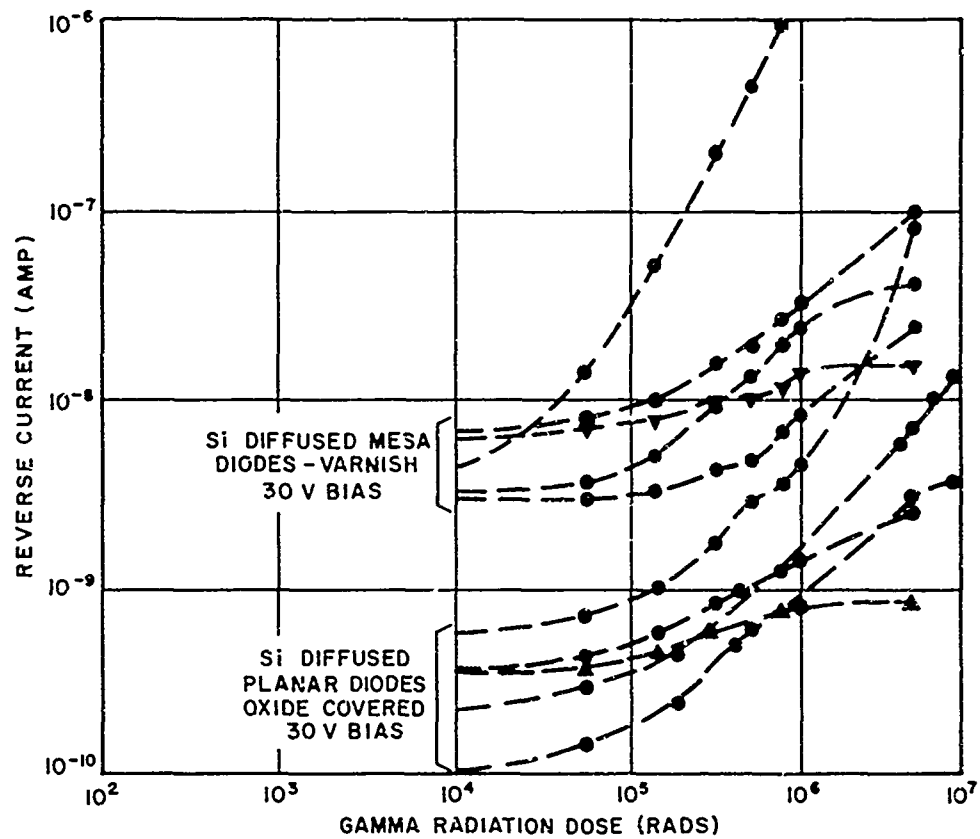
48

Figure 30.   Degradation produced by reverse bias and
γ irradiation of oxide covered planar diodes
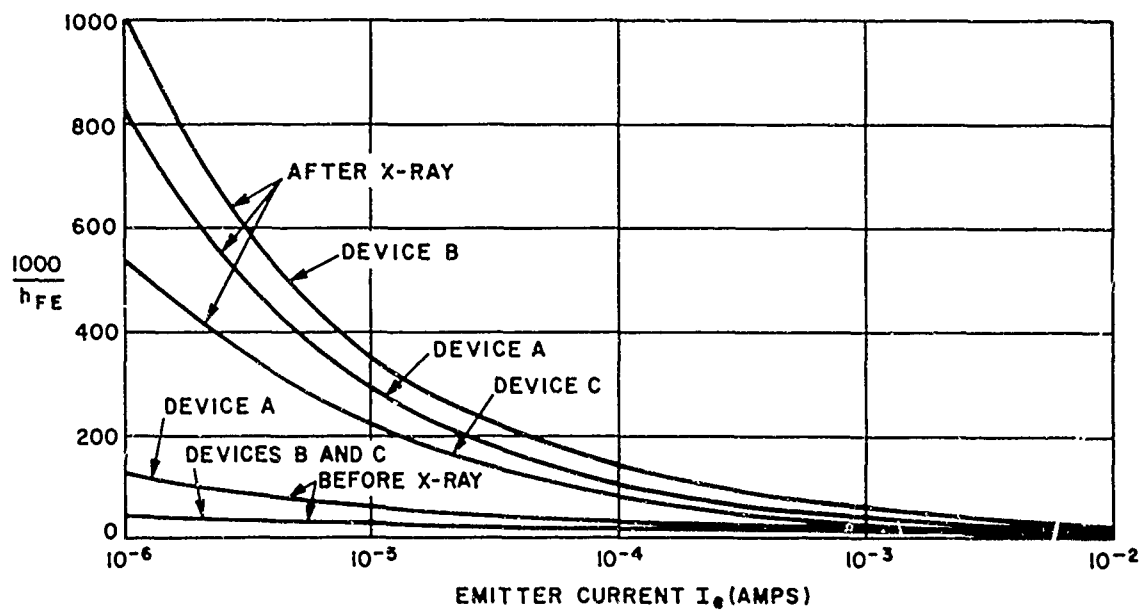and varnish covered mesa diodes

Figure 31.   Dependence of h_{FE} degradation on emitter current

emitter current producing the most rapid recovery. The amount of damage exhibited by a given type of device appeared to vary with the manufacturer; five lots of the same devices supplied by five manufacturers showed widely varying responses. It is, of course, natural to suspect that the cause is the different surface treatments given the devices by each manufacturer.

An extensive and systematic study of passivated planar devices has been made by Schmid,[52] who finds a predictable pattern of response for many types. All npn devices exhibit a rapid drop in dc current gain (to as low as 10 percent of the initial value at doses of 10^6 rads) accompanied by a slow increase in I_{CBO}. The pnp structures, on the other hand, show little decrease in gain, but I_{CBO} increases as much as six orders of magnitude at 10^6 rad doses. In some cases, I_{CBO} saturates and actually recovers slightly with increasing dose. The response of a given device is found to be characteristic of the manufacturer, and it has been shown that changes in the device surface structure will significantly change the response. High-gain devices were found to degrade proportionally faster than devices with low gain.

Contrary to the findings of Taulbee,[51] the h_{FE} degradation was found by Schmid, to a first approximation, to be independent of bias. In fact, the decrease in gain was sometimes greater without bias. Schmid did not examine the effects of reverse emitter bias. Over relatively long periods, the degradation appeared to be permanent under shelf-life conditions. However, a two-hour bake at about 300°C restored the original characteristics, and a second exposure to radiation repeated the previous degradation.

Schmid explained the difference between the behavior of npn and pnp transistors as follows: Ionizing radiation creates a positive charge in the oxide layer or at the oxide-semiconductor interface which affects the base regions of the transistors. For an npn device, the positive surface charge increases the surface recombination in the base. The result is an increase in base current required to maintain a given collector current and hence a decrease in gain. For pnp transistors, the positive surface charge creates a collector channel which results in an increased I_{CBO} as discussed previously.

Many of the degradation features observed by Peck and his colleagues[23] on gamma-irradiated nonpassivated devices have also been observed by Stanley[53] in high-gain pnp and npn Si planar transistors irradiated with 1.5 MeV electrons. The degradation was found to be most pronounced in the collector-to-emitter leakage current, I_{CEO}. Figure 32 shows the I_{CEO} increase for an npn transistor as a function of the total electron dose. It appears that I_{CEO} will saturate after increasing several orders of magnitude. It is also apparent that both radiation and bias, V_{CE}, must be present for degradation to occur. During the times AA, BB, etc.,

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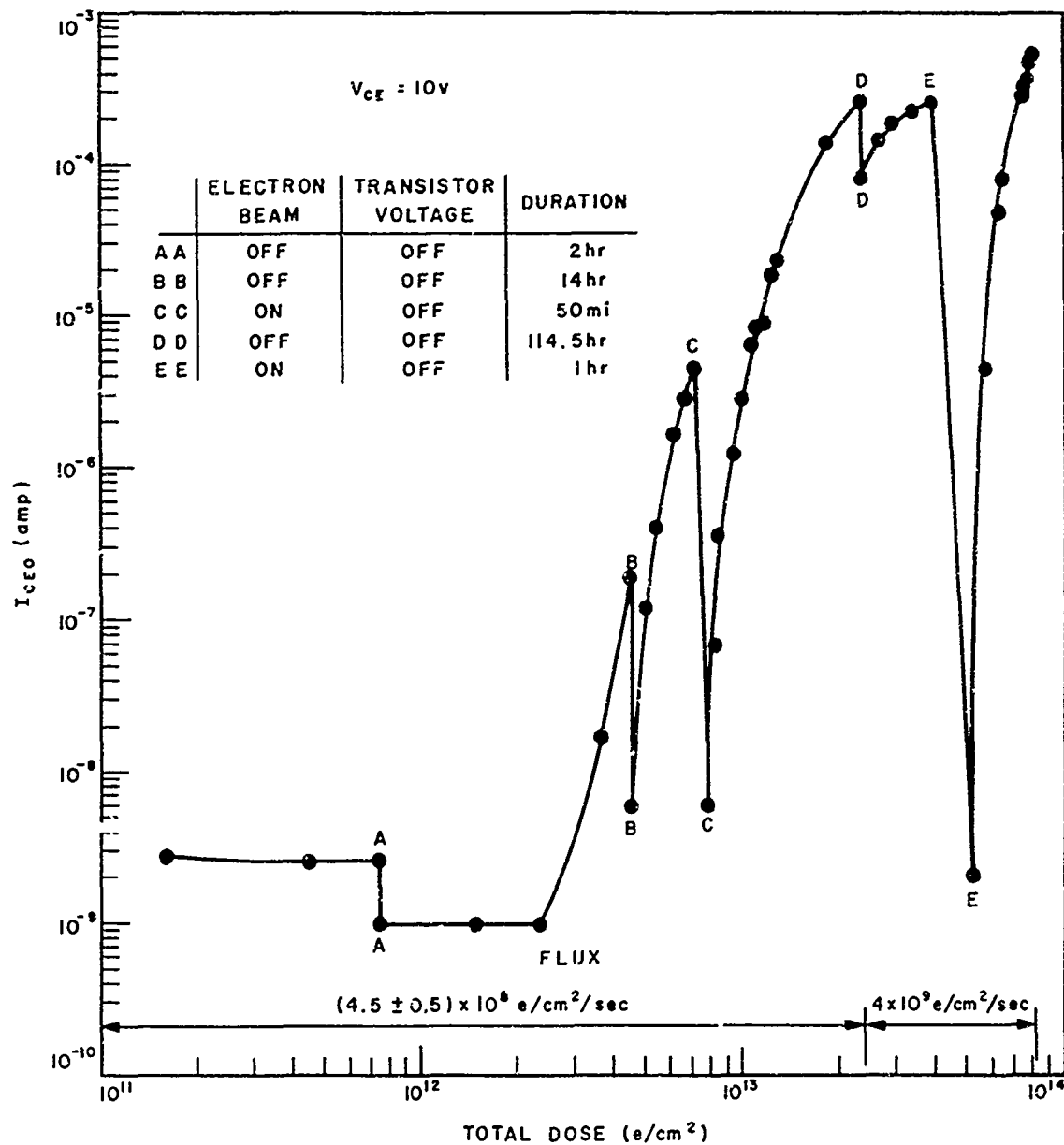
Figure 32. I_{CEO} vs total electron dose

1965-11   Figure 2.
Lincoln Laboratory, MIT
Reprinted by permission

when $V_{CE} = 0$, the transistor shows recovery. As with nonpassivated devices, the recovery is much more pronounced when radiation is present (compare DD with EE). Stanley reported that forward-biasing the emitter junction also improved the recovery of the leakage current and in many cases restored I_{CEO} to its pre-irradiation value.

Figure 32 also shows evidence of a memory effect similar to that observed by Peck;[23] i. e., after the annealing periods BB, CC, DD, and EE, I_{CEO} returns to

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its preannealing value very quickly (compared with the overall rate at which I_{CEO} is increasing) as though it "remembered" its previous irradiated condition.

The transistors examined by Stanley also showed h_{FE} degradation under electron bombardment. The degradation was much more severe at low emitter currents, 5 to 10 μA, than at higher currents, ~ 1 mA. The final gain at 10^{15} e/cm^2 dose was about the same (~ 10) for many units and showed no correlation with preirradiation values. One type of transistor encapsulated in a high-density silicone compound did not exhibit such severe gain reduction, presumably because of increased shielding which was able to stop 1.5 MeV electrons. However, two other types of plastic encapsulated transistors showed severe gain degradation at low currents.

The effects of neutron bombardment on planar npn Si transistors have been investigated by Goben.[54] Using techniques similar to those used by Iwersen[12] to separate bulk and surface effects, Goben concurs with Iwersen that before irradiation the low injection level current gain of npn transistors is controlled by surface recombination in the emitter-base space charge region. After neutron irradiation, however, he finds the controlling source of recombination to be in the bulk space charge region. Moreover, the bulk space charge recombination centers were found to anneal out at a different rate than those outside the space charge region.

The effects of electron and Co^{60} gamma rays on the dc gain of npn and pnp Si transistors have also been reported by Brucker and others.[55] They found the loss of gain caused by increased surface recombination effects to be nonlinear with radiation dose. By irradiating npn planar transistors with 125 keV electrons (below the energy threshold for bulk damage in Si) they found, in general,

$$\frac{1}{h_{FE}} \propto \phi^{0.5}$$

Furthermore, at higher dose levels the surface effects caused by radiation appeared to saturate. Brucker also reported that the surface effects readily annealed out at 250° C.

For Si planar transistors Hughes[56] has found that a dose of 10^6 rads of Co^{60} radiation can cause I_{CBO} to increase four orders of magnitude and h_{FE} to decrease to 25 percent of its preirradiation values. The response of the devices to radiation was found to be quite dependent on bias conditions but, interestingly enough, independent of whether the ambient was a gas or a high vacuum. This last observation lends support to the view that charges within the oxide rather than on the oxide surface are responsible for degradation. The effect of surface charge was observed to be severe enough to invert even the highly doped p$^+$ guard ring on pnp transistors.

The degradation of h_{FE} and other parameters in both npn and pnp Si planar-passivated transistors exposed to electron beams (5 to 50 keV) has been observed by Green and others.[57] The degradation was found to be reversible in that it could be removed completely by annealing for several hours at 250°C. Partial recovery was observed at lower temperatures. The interesting point in these experiments is that the degradation only occurred when the electrons had sufficient energy to penetrate to the Si-SiO$_2$ interface; electrons stopped in the oxide away from the interface had no effect. Subsequent measurements with a small scanning light spot showed that the surface recombination velocity had increased in the base region of the transistors.[58]

F. Radiation Effects in Metal-Oxide-Semiconductor Field Effect Transistors

Field effect transistors are majority carrier or unipolar devices and as such were originally believed to be relatively insensitive to radiation effects because their characteristics did not depend on minority carrier lifetime. The effects of electron irradiation on planar junction field effect transistors has been investigated by Stanley.[61] He finds this device more resistant to surface ionization and other radiation effects than any other active semiconductor device. However, surface ionization effects, especially on n-channel devices, produce large leakage currents across the gate-to-drain junction when the devices are operated under bias. This leakage current is important in the high-impedance circuits which use FETs.

Recent investigations have shown the metal-oxide-semiconductor field effect transistor (MOS-FET) to be quite sensitive to radiation due to surface effects. The MOS-FET is shown schematically in Figure 33. The device consists of a base, in this case p-type Si, into which an n-type source and drain have been diffused. The conductivity of the base and hence the source-to-drain current, I_D, is controlled by the potential applied to a metal gate electrode insulated from the semiconductor surface by a layer of SiO$_2$.
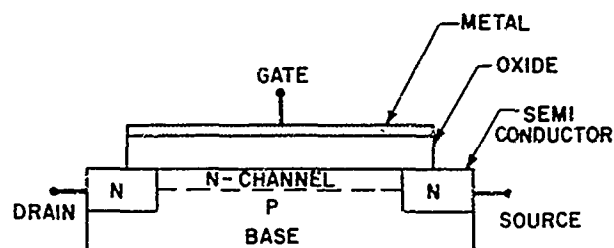

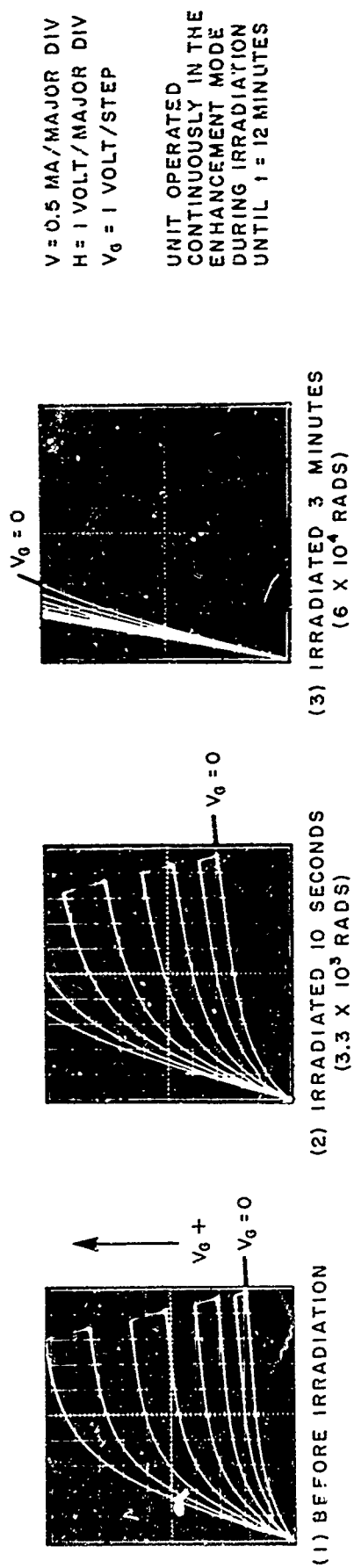Figure 33. N-channel metal-oxide-semiconductor field effect transistor

If a positive potential is applied to the gate, minority carriers are attracted to and majority carriers repelled from the base surface. As a result, an n-channel is formed between the source and drain. The conductivity of this channel depends on the gate potential, and thus the gate is able to control the drain current.

The effects of Co^{60} gamma radiation (simulating space environment conditions) on MOS-FETs have been studied by Hughes and Giroux[62,63] who found that the devices show changes in transconductance, g_m, and channel conductance at dose levels corresponding to one-half hour in space. Furthermore, the degradation appears to be bias-polarity dependent, as is evident in Figure 34. Little or no effect is seen when the device is irradiated in the depletion mode, but large changes in the drain current and the transconductance are seen for irradiation in the enhancement mode. For n-channel devices, the zero gate voltage drain current ultimately increased from 1 mA to 45 mA in the enhancement mode (gate biased positively with respect to the source), but showed little change in the depletion mode (gate biased negatively with respect to the source) for a total dose of 10^6 rad. The effects of the radiation appear to be permanent with no apparent annealing after six months.
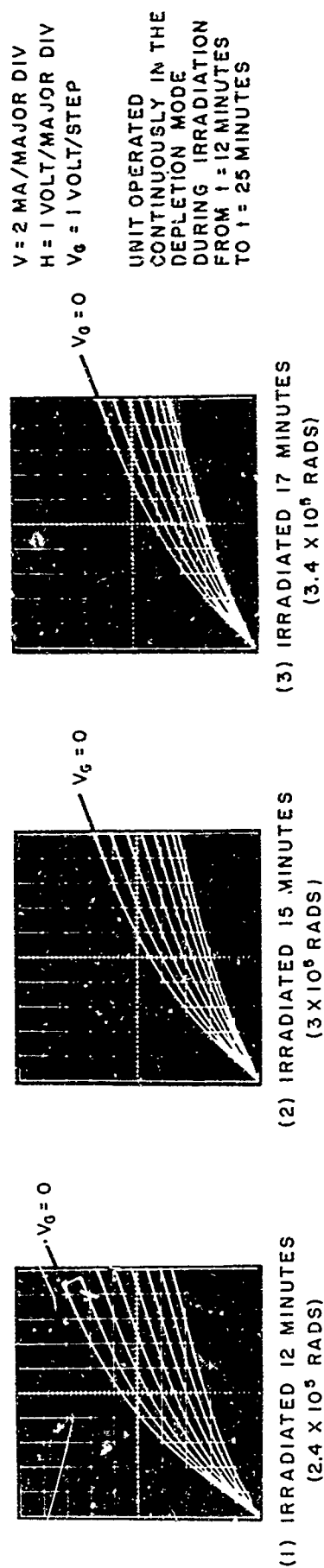
The degradation of the MOS-FET can be explained if it is assumed, as in the case of passivated transistors discussed earlier, that positive charges can be produced in the SiO_2 layer by radiation. In the enhancement mode, with the gate electrode positive, a strong electric field is set up which causes positive charge to migrate toward the $Si-SiO_2$ interface. Positive charge accumulation at this interface would, of course, increase the channel conductivity and drain current. In the depletion mode, the field in the oxide will be reversed and positive charges will be attracted to the gate (where they have much less effect on the channel). Negative charge (in the form of electrons) migrating to the $Si-SiO_2$ interface will enter the Si and no negative charge will build up at the interface.

To support this picture, Hughes and Giroux observed the gate capacities of n-channel MOS-FETs biased in both the enhancement and depletion modes as a function of gate-to-source potential, V_{GS}, before and after 10^6 rads of Co^{60} gamma irradiation. The results are shown in Figure 35. The capacitance minimum, which is observed as the gate voltage is increased from large negative values, occurs when the surface layer changes from depletion to inversion. If there were no charge stored at the $Si-SiO_2$ interface, the minimum should occur near $V_{GS} = 0$.

In the enhancement mode, Figure 35(a), the irradiation causes the minimum to shift -11.5 volts. This is to be expected if, as proposed above, a positive charge collects at the $Si-SiO_2$ interface. For the depletion mode, Figure 35(b), the minimum shifted only -1 volt indicating, as expected, relatively little positive charge accumulation. From these results, Hughes and Giroux estimated that the capacity minimum shift for the enhancement mode corresponds to a positive charge layer of 10^{12} charges/cm^2 at the interface (this charge density would result from 10^{-3} monolayers of singly charged ions). The experiment was, however, incapable

(1) BEFORE IRRADIATION

(2) IRRADIATED 10 SECONDS
(3.3 X 10³ RADS)

(3) IRRADIATED 3 MINUTES
(6 X 10⁴ RADS)

V = 0.5 MA/MAJOR DIV
H = I VOLT/MAJOR DIV
V$_G$ = I VOLT/STEP

UNIT OPERATED
CONTINUOUSLY IN THE
ENHANCEMENT MODE
DURING IRRADIATION
UNTIL t = 12 MINUTES

(a)

(1) IRRADIATED 12 MINUTES
(2.4 X 10⁵ RADS)

(2) IRRADIATED 15 MINUTES
(3 X 10⁵ RADS)

(3) IRRADIATED 17 MINUTES
(3.4 X 10⁵ RADS)

V = 2 MA/MAJOR DIV
H = I VOLT/MAJOR DIV
V$_G$ = I VOLT/STEP

UNIT OPERATED
CONTINUOUSLY IN THE
DEPLETION MODE
DURING IRRADIATION
FROM t = 12 MINUTES
TO t = 25 MINUTES

(b)

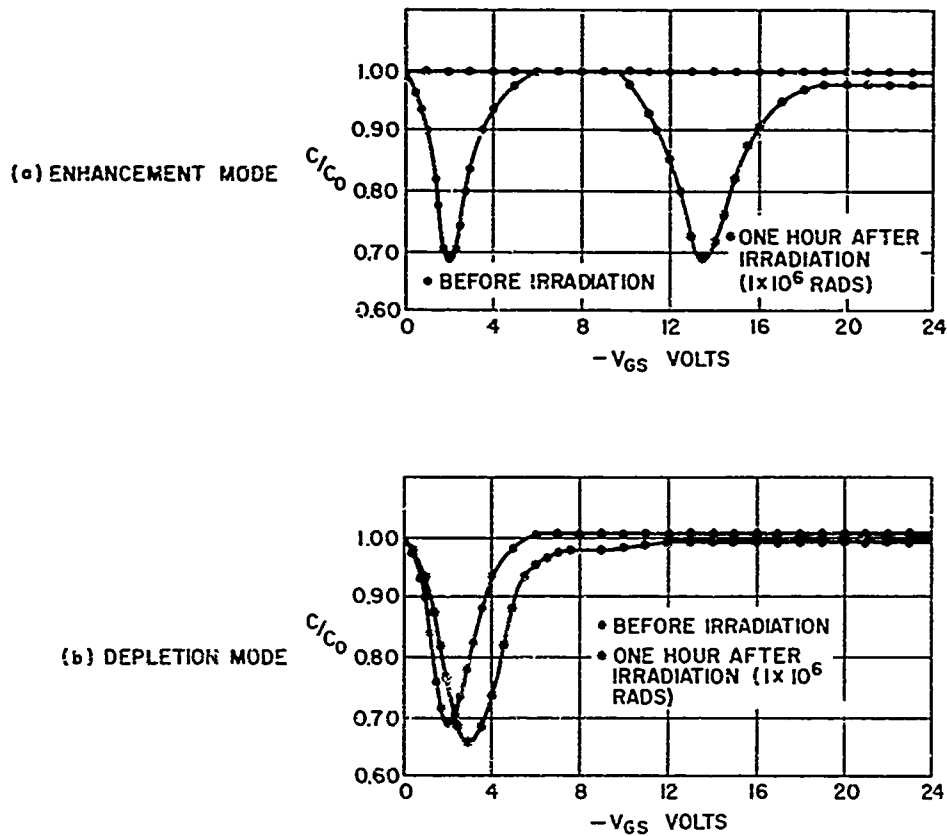Figure 34.   Effect of radiation on n-channel MOS-FET

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Figure 35. Gate capacitance of an n-channel MOS-FET vs V_{GS}

of giving information about the charge accumulation process or the nature of charge carriers.

The behavior of n-channel MOS devices in a radiation environment has also been studied by Kooi[64] using 150 keV X-rays. He found that large erratic changes in the drain current occurred when the devices were irradiated in the enhancement mode; these findings are similar to those of Hughes and Giroux. However, Kooi observed fairly significant changes for the depletion mode as well. Under fixed gate and drain potentials, he found a rapid initial increase in the drain current in the depletion mode with increasing dose. The effect was found to saturate after a few minutes of irradiation at 10^4 R/min. The magnitude of the saturated drain current depended strongly on the magnitude of the gate potential during irradiation. The more negative the gate potential, the less the change in drain current during irradiation. Changes in the transconductance were small during the irradiations.

Kooi's model of the oxide differs somewhat from the models discussed previously in that he does not assume the presence of mobile positive charges in the oxide. Instead, he suggests that the X-rays produce electrons and positive centers

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in both the oxide and adjacent silicon. If the gate is positive with respect to the silicon, electrons migrate to the gate when they are collected. Electrons produced in the silicon cannot cross the silicon-oxide boundary because of a large potential barrier (Kooi reports that 4.2 eV are required to move an electron across the barrier as determined from ultraviolet light experiments). Thus a net positive charge accumulates in the oxide. This charge inverts the silicon surface and increases I_D; i.e., the transfer characteristics increase. If the gate potential is made more negative, then the amount of positive charge in the oxide is obviously reduced and the change in characteristics under irradiation decreases.

The degradation of enhancement mode, p-channel MOS-FETs irradiated with 1.5 MeV electrons has been studied by Stanley.[65] With a drain-to-source potential of -5 volts and the gate connected through 100 MΩ to the source, the drain current remained 5×10^{-10} A until the dose reached $5 \times 10^{+12}$ e/cm^2. At this dose, I_D increased rapidly and then saturated at $\sim 4 \times 10^{-5}$ A at $\sim 10^{14}$ e/cm^2.

The drain current as a function of the gate-to-source voltage, V_{GS}, is shown in Figure 36 for three dose levels. Before irradiation, the turn-on voltage (i.e., the minimum value of V_G at which a channel is destroyed for a p-channel device or created for an n-channel device) is $\sim$ -3 volts. (This corresponds to the gate-source voltage where the drain current begins to increase rapidly.) After 10^{14} e/cm^2, however, the turn-on voltage has decreased to $\sim$ -10 volts and the current for positive V_{GS} values has substantially increased. At 5×10^{14} e/cm^2 it is impossible to turn the device on.

The decrease in turn-on voltage can be explained in this case if it is again assumed that positive charge carriers are produced in the oxide by radiation. The electric field in the oxide is in such a direction as to cause positive charges to migrate to the Si-SiO$_2$ interface. In this case, however, the positive charges cause an inversion layer (n-channel) on the p-type drain where it is overlapped by the gate (see Figure 37). A high density of positive charge must be present in the oxide, since it is difficult to invert a highly-doped material such as the drain. As a result, the p-channel is isolated from the drain until the gate potential becomes negative enough to produce a p-channel deeper than the
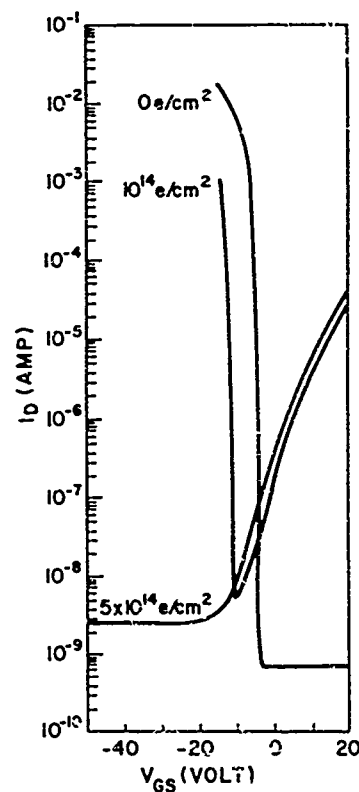

Figure 36. Effects of electron irradiation on transfer characteristics; I_D vs V_{GS} at V_{DS} = -20V
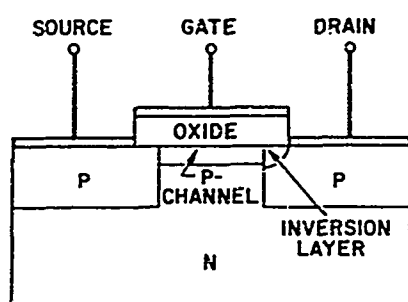
Figure 37. P-channel MOS-FET after irradiation

drain channel. With increasing radiation dose, the drain channel becomes deeper and the device more difficult to turn on.

The effect of low-energy electrons (10 to 20 keV) on the charge in an SiO_2 film on Si has been studied by Szedon and Sandor using an MOS capacitor.[66] As in the experiments of Hughes and Giroux, Szedon and Sandor observed a shift in the C-V curve of the capacitor as a result of irradiation. From the results they estimated the density of surface states at the SiO_2-Si interface for two capacitors before and after radiation. The results are shown as a function of position in the energy gap of Si in Figure 38. It can be seen for both capacitors that a significant number of states have been added, $\sim 2 \times 10^{12}$ states/cm^2-eV, over a considerable portion of the energy gap. Szedon and Sandor also report that the effects of irradiation could be removed by a 15-minute anneal at 150-200°C with the capacitor shorted.

The effects of neutron irradiation on MOS transistors have been reported by Messenger and Steele.[67] They find the most important effect to be a positive charge build up in the oxide, which causes the gate capacity minimum to move to more negative values of V_{GS}. They define the gate voltage at which the capacity minimum occurs as the turn-on voltage, V_T. Figure 39 shows the change in V_T with neutron flux. According to Messenger, the tendency of V_T to saturate indicates a decreasing net accumulation rate of positive charge which may be caused by a diffusion or recombination process. The existence of such processes implies that the degradation should be dose-rate dependent and also that the diffusion or recombination process has a substantially higher rate during irradiation since the degradation appears to be permanent after irradiation. At present there is no independent evidence to support this view. Annealing at elevated temperatures was found to remove the degradation; typically, V_T showed 90 percent recovery after 70 hours at 150°C.

As with the previous MOS-FET experiments, the results give no information about the positive charge formation or the nature of the charge carriers. Messenger suggests that oxygen vacancies are the charge carriers.[45]

A study by Kuehne[68] of insulated gate thin-film transistors using polycrystalline CdS has revealed similar surface effects due to ionizing radiation. These devices showed bias-dependent semipermanent changes in transconductance and channel conductivity at doses of 10^5 rad. Analysis showed that interface trapping states are at least partly responsible.
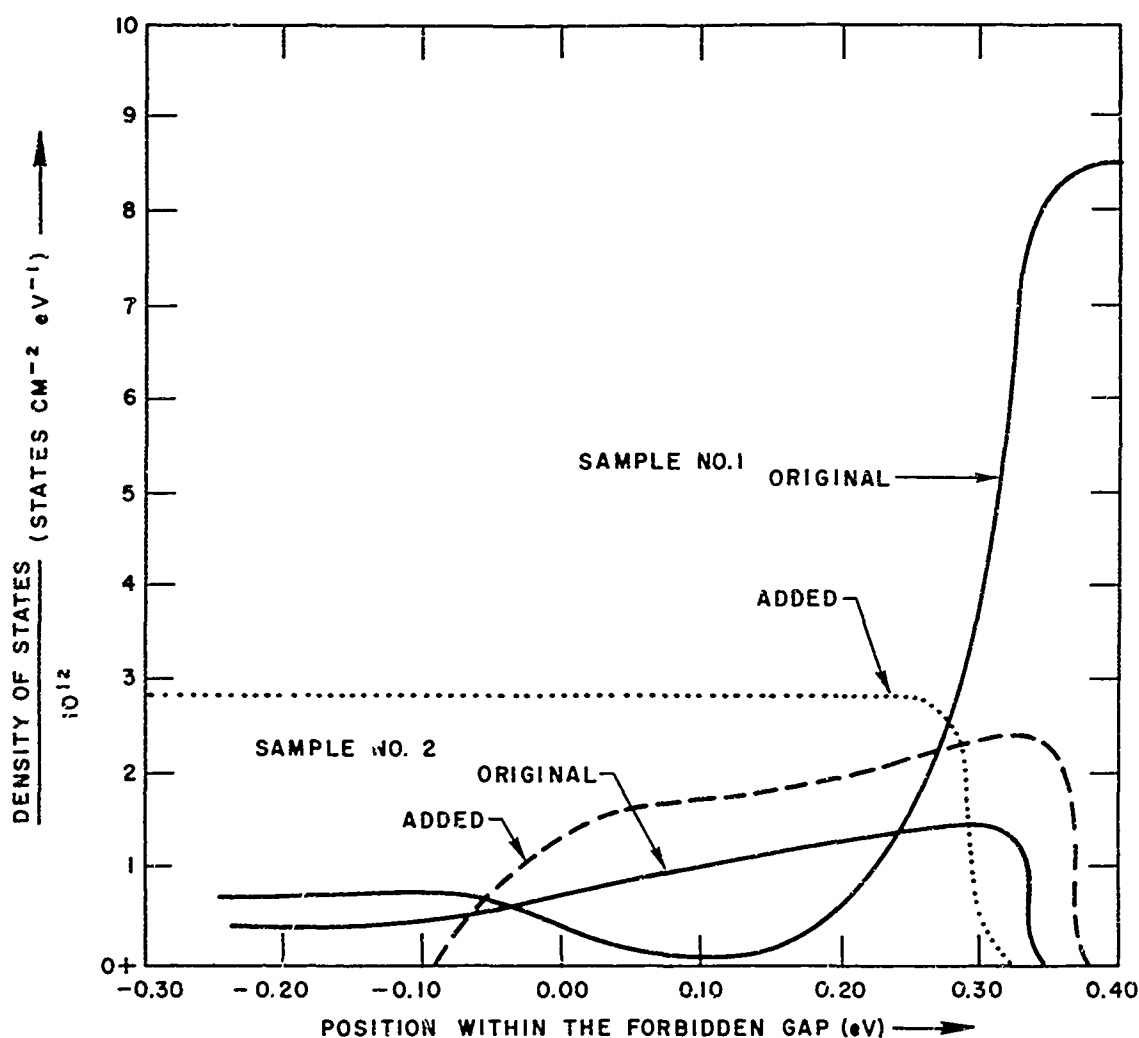
Figure 38. Typical densities of states added by low energy electron bombardment of Al-SiO$_2$-Si capacitors, compared with original densities. Sample 1: 5Ω-cm N-type Si, 1600 Å oxide grown in wet O$_2$, capacitance-voltage data taken at 600 mcs. Sample 2: 50Ω-cm N-type Si, 1500 Å oxide grown in dry O$_2$, capacitance-voltage data taken at 1 mcs.

G. Integrated Circuits

The direction of present-day semiconductor device technology is towards increased use of integrated circuits. These circuits contain many passivated areas where surface effects due to radiation may cause degradation. Unfortunately, very little work has yet been reported on surface effects of ionizing radiation on these devices. Stanley[69] has studied the effects of electron irradiation on a number of hybrid and monolithic integrated circuits. The hybrid circuits usually responded as would be expected from their component parts. Bulk and surface effects were difficult to separate in the monolithic circuits. It was apparent, however, that surface ionization did cause increases in I_{CEO} and decreases in h_{FE} for the integrated transistors.
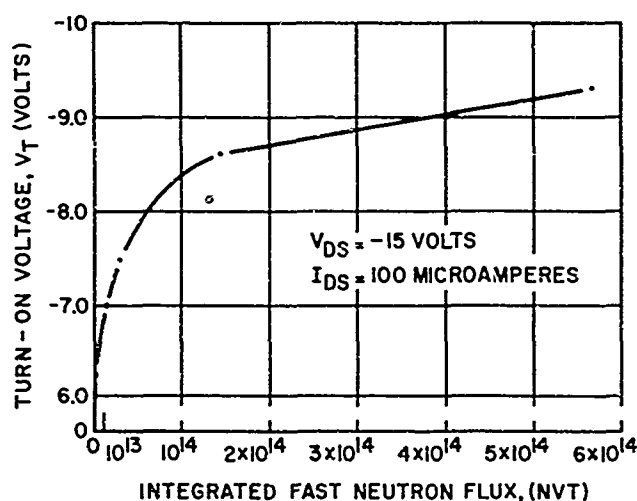
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Figure 39.   Turn-on voltage vs neutron
flux for a p-type MOS transistor

6.   DISCUSSION

A.   Introduction

The most recent trend in the electronics industry has been toward increasing use of silicon planar transistors, integrated circuits, and low-power devices such as the MOS-FET. Silicon dioxide films, in one way or another, are an integral part of these devices and it is necessary, therefore, that SiO_2 and its effect on devices be thoroughly understood.   This is especially true in the cas˜ of radiation effects, since processes occurring in SiO_2 appear to be the cause of degradation.   It is not surprising, then, that a large portion of this discussion is concerned with the problems of radiation effects in SiO_2.

B.   Location of Surface Charge Responsible for Radiation Degradation of SiO_2-Protected Devices

1.   Saturation Effects.   The results of the various studies on passivated bipolar and unipolar devices described earlier appear to be somewhat contradictory and irreconcilable.   The question is whether the surface charge which controls the degradation process is located on the outer surface of the oxide (Atalla's model[41]), or in the oxide, or at the Si-SiO_2 interface.   It is not inconceivable, of course, that both views are valid and that under some circumstances charge on the SiO_2 surface dominates while in other cases charge within the oxide is more important.   For some observations, both models are capable of an explanation.   For example, Kerr,[50] Stanley,[53] Taulbee and others,[51] Brucker and others,[55] and to some extent Schmid[52] observe a saturation of degradation.   Intuitively one would expect both models to predict saturation since both processes, surface charge separation and charge accumulation, are self-limiting.

2.   Importance of Bias.   With the exception of Schmid's observations, the experimental evidence indicates that bias is an important factor in degradation due to radiation.   This result is not surprising since both models require an electric field; Atalla's model requires a parallel field component at the oxide surface, the other a transverse component in the oxide.   These field components may arise from bias voltages across p-n junctions or from overlaying contacts.[70]   It is also possible

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that built-in fields are produced in the SiO_2 layers during their formation. Built-in fields may reduce the dependence of degradation on bias voltage. At present it is impossible to predict quantitatively how degradation should depend on bias conditions and hence it is impossible to distinguish between the two models from the experimental results given above.

3. Recovery of Surface Effects. Recovery of passivated devices from surface effects due to radiation is to be expected under proper conditions for reasons similar to those for nonpassivated devices. Some recovery is expected to start as soon as the device is removed from the radiation. Removal of bias and increase in temperature should contribute to recovery; under these conditions, recovery has been observed as discussed above. One might, however, expect to see a difference in recovery depending on where the surface charge responsible for degradation is located. If the charge is located on the oxide surface, recovery might be somewhat easier than it would be for a charge located inside the oxide, well isolated from the ambient. For example, simply exposing a nonpassivated device to the atmosphere can cause considerable recovery. For passivated devices, however, the bulk of the evidence points to a charge in the oxide, since recovery usually requires elevated temperatures; the degradation appears quite stable under shelf conditions, and exposure to the atmosphere does not produce noticeable recovery.

4. Additional Evidence. The model of charge storage in the oxide is further supported by Estrup's[71] finding that ion bombardment of passivated diodes did not produce the leakage current degradation observed with nonpassivated diodes. The strongest support, however, has come from the observation that degradation of irradiated passivated devices occurs even with a high vacuum ambient.

All in all, the bulk of evidence supports the model of ionizable defects located in the oxide, apparently quite close to the SiO_2-Si interface, as being the principal source of slow states in these devices.

C. Nature of the Ionizable Species

There is, as yet, no experiment which has definitely labeled the ionizable species responsible for charge in the oxide. As has been pointed out, some authors believe ionizable sodium atoms are the important defects, whereas others feel that oxygen vacancies are the source. Indeed, because of the variety of ways in which the oxide is prepared, it is very possible that any one of several possible defects could be responsible. Among those that have been considered are sodium, aluminum, hydrogen, oxygen vacancies, and trivalent silicon.[72] The identification of the responsible species under any given oxide growth conditions would undoubtedly be most difficult.

However, identification of the particular species of ion in the oxide may not be essential in understanding the physical processes in the oxide which give rise to the slow surface states. It has been repeatedly pointed out that the charge built up near the SiO_2-Si interface is always positive and results in an n-type layer at the surface of the Si. This observation raises the questions why only positive charge builds up in the oxide and why the charge does not tend to be neutralized when the oxide is exposed to high temperatures or ionizing radiation.

A model which answers both these questions has been proposed by Lindmayer and Busen.[73,74] They view the SiO_2-Si interface as a heterojunction with a work function difference between the SiO_2 and Si of approximately 0.4 eV. The work function for Si is greater than for SiO_2. As a consequence of this mismatch in work function, electrons are transferred from the oxide to the silicon, creating an n-type layer on the silicon. The electrons come from relatively deep traps in the oxide near the SiO_2-Si interface, leaving behind positively charged ions. Because the traps are deep, the transfer of electrons takes place slowly and equilibrium is not readily achieved. The authors find, however, that a heat treatment at ~ 250°C brings the region into equilibrium rapidly. In this case the density of ionized traps approaches 10^{11} charges/cm^2, which is that required to equilibrate the differences in work function. On the other hand, before equilibrium is achieved the surface charge density in the oxide may be as low as 10^6 charges/cm^2. The most important feature of this heterojunction model is that the tendency of the oxide to acquire a positive charge is a natural result of the difference in work function between the oxide and the silicon. Reduction of the induced surface charge on the silicon, therefore, would require modification of the oxide to match the work function of the silicon.

D. Origin of Charge Separation in the Oxide Under Radiation

The heterojunction model of the SiO_2-Si interface leads to a rather straight-forward explanation of the separation of charge in an oxide exposed to ionizing radiation. When ionized, the traps in the neighborhood of the interface would tend to give up electrons to the silicon and consequently the interface would come to equilibrium fairly rapidly. Thus, there would be a build up of positive charge in the oxide at the interface even in the absence of applied bias.

The result of the application of bias to a heterojunction during irradiation can be understood with the aid of Figure 40. Figure 40(a) shows the band structure at the SiO_2-Si interface in the absence of applied bias. The work function difference between the SiO_2 and Si, $\Delta \phi$, appears partially across the SiO_2, qV_i, and partially across the silicon, qV_s. With no ionizing radiation present, almost all of any applied voltage, V_a, will appear across the bulk of the oxide. Under ionizing
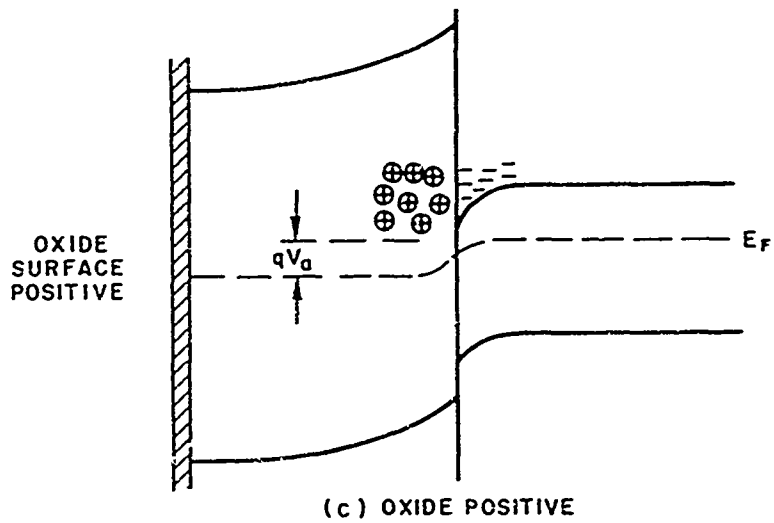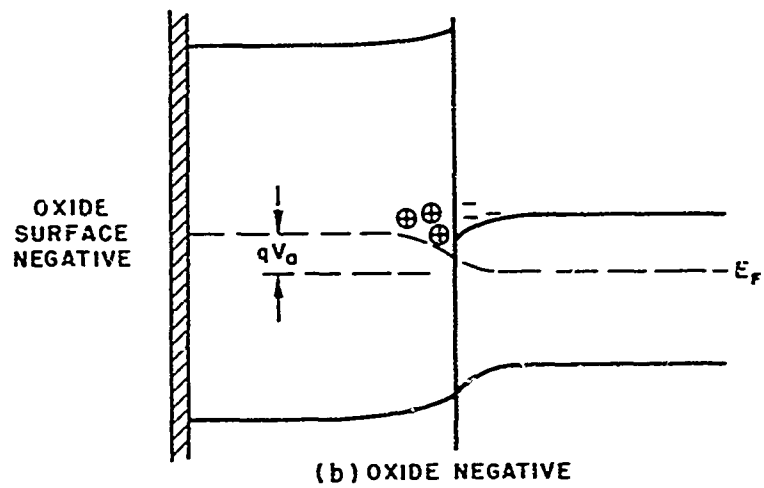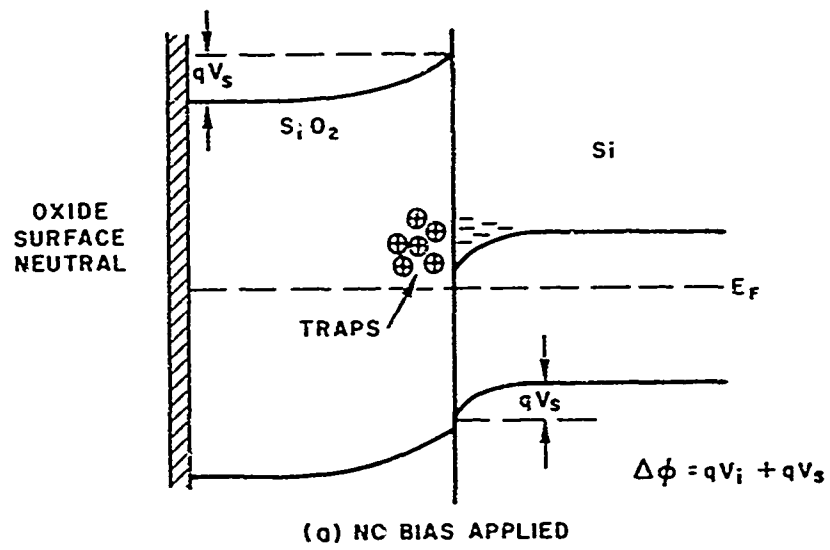
Figure 40. Heterojunction model for SiO_2-Si interface

bombardment, however, more of the applied voltage appears at the heterojunction interface because of the increased conductivity of the oxide. In the case of a negative bias on the oxide, Figure 40(b), the effect is to reduce the potential barrier at the interface so that relatively little charge is needed at the heterojunction to achieve equilibrium. Kooi[64] indeed found that equilibrium under ionizing conditions was achieved quickly for negative bias on its oxide. On the other hand, a positive bias on the oxide, Figure 40(c), increases the barrier height at the heterojunction so that much more positive charge storage is required in the oxide for equilibrium.

In this model of charge production under ionizing conditions, there is an obvious saturation effect; i. e., when enough charge has been built up at the interface to equilibrate the barrier height, no further increase of charge in the oxide should occur. Furthermore, since both the rate of approach to equilibrium and the fraction of the voltage across the oxide which appears at the heterojunction depend strongly on the dose rate, there should be a marked dose rate dependence of charge build up.

The alternate model for the origin of separated charge in the oxide under irradiation assumes the motion of ions in the oxide in place of, or in addition to, the motion of electrons. In this model, the application of bias to the oxide either moves the positive ions produced by radiation to the SiO_2-Si interface or away from it. Again the heterojunction model may have to be invoked to understand the large amounts of uncompensated charge that can be built up in the oxide. The ionic motion model has to stand on the fact that appreciable ionic motion has been observed in several insulators, such as quartz and glass, down to fairly low temperatures ($\sim 300°C$). However, the possibility that such ions migrate at room temperature in SiO_2 is subject to some doubt.

A satisfactory experiment to distinguish between electronic or ionic motion has yet to be performed. The most satisfactory way of separating the two processes is probably on the basis of their temperature dependencies; i. e., the ionic motion should have a higher activation energy for motion and one that could be compared with measurements of ionic motion in pure SiO_2.

E. Recommendations for Future Surface Radiation Effects Studies

1. Fundamental Studies. There is, at present, little information on radiation-induced changes of the surface potential at a clean semiconductor surface. In principle, it would be relatively easy to study these changes by comparing the effects of radiation with those produced by, say, known ambient changes. In practice, reproducibly clean surfaces would be required and these are difficult to prepare and maintain. The radiation used should, of course, be of low enough energy to prevent bulk damage effects (low-energy electrons might be suitable).

The effects of radiation-induced lattice damage at a semiconductor surface are unknown. Usually it is assumed that this type of damage is unimportant in a region such as a surface where lattice irregularities are already numerous. It is possible, however, that lattice damage sites may be created at energies significantly lower than in the bulk, and that these additional sites do, in fact, lead to an increase in the surface state density.

It is important to determine the species of charge-carrier responsible for positive charge accumulation at the SiO_2-Si interface. This determination will help to substantiate or invalidate the heterojunction model of the interface.

2. <u>Device Studies.</u> Continued emphasis should undoubtedly be placed on device studies, both for the role such studies play in validating the various models presented here and because the preparation of semiconductor surfaces by most of the device manufacturers has been a constantly evolving process. Two years ago a simple but satisfactory model of surface effects on (nonpassivated) devices existed. Today, however, the situation is, in a certain sense, worse since the problems of passivated devices are just beginning to be resolved.

Particular emphasis should be placed on understanding radiation surface effects in MOS-FETs, high-frequency transistors, thin-film transistors, metal-semiconductor junction, and other low-level logic devices that are especially useful for low-power space applications.

It is essential that the effects of ionizing radiation on metal-semiconductor and heterojunction interfaces be understood. This important area has heretofore been neglected. Studies of noise arising from surface effects in both unipolar and bipolar devices is another area that has unfortunately been neglected. Noise in MOS structures has been discussed by Sah[75] and by Jordan and Jordan,[76] but a study of the effects of radiation on noise on MOS devices has not been reported.

Perhaps the most important practical goal of the device studies at present is the development of a satisfactory model for device degradation that could be used by a device designer to minimize the effects of radiation on devices. To this end, it is important to develop a surface stabilization technique which will reduce surface effects as much as possible. Once the charge transport mechanism in SiO_2 is understood, it may be possible to improve the passivation layer by further treatment such as the P_2O_5 treatment mentioned earlier.

At present, the method of oxide preparation varies from manufacturer to manufacturer, making it difficult to compare results on devices from different sources. It may prove necessary to develop a standard procedure for device passivation, at least for devices exposed to radiation. If it is shown that charge

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formation on the SiO_2 surface is responsible for degradation, then it may also be necessary to control the device ambient.

Other manufacturing steps, such as the deposition of contacts or the bonding of leads, may lead to local damage areas. These areas may be more sensitive to radiation effects and should be investigated.

3. Procedures for Selecting Devices for a Radiation Environment. Ultimately, the device studies outlined above should lead to procedures for selecting both the type and individual device best suited with respect to surface effects for use in a radiation environment. To date, very little has been done to evolve such procedures. Peck and his associates,[23] in choosing transistors for the Telstar satellite, devised a straightforward selection process. The various device types were subjected to a gamma exposure of 1.4×10^4 rads (8.5 rads/hr for 1 min) followed by an exposure at 3 rads/hr for at least one week. Device types showing no significant changes in I_{CBO} and h_{FE} were considered satisfactory.

Peck and the others also studied screening and selection procedures using diffused Si transistors. They showed that, by selecting devices which had an I_{CBO} value of less than 10^{-8} A after a screening dose of $\sim 10^4$ rads, they could eliminate 90 percent of the devices which ultimately suffered severe I_{CBO} or h_{FE} degradation.

A selection procedure for planar Si transistors which uses microplasma noise measurements in addition to a screening radiation procedure has been developed by Bostian and Manning.[77] According to these investigators, microplasma noise is an indicator of the presence of surface defects which act as acceptor states. These acceptor states aid in channel formation on pnp devices and oppose it on npn. Thus pnp transistors exhibiting the least microplasma noise and npn exhibiting the highest should be least susceptible to radiation.

Based on the above model, Bostian and Manning give a selection procedure. First, select transistor types with the highest upper frequency limit to reduce gain degradation due to bulk radiation damage. Next, select the pnp transistor type with the lowest or the npn type with the highest average microplasma noise level. Then, select the individual devices by choosing the pnp's with lowest and the npn's with the highest noise levels. Finally, expose the devices to a screening dose of 5×10^4 rads and reject any showing I_{CBO} values significantly above average.

Using the procedure outlined above, the authors report improvement factors (defined as the ratio of average leakage current of all devices in a group to the average current for selected devices) of about 10, depending on device type.

7. SUMMARY

The degradation of many semiconductor devices resulting from surface effects of radiation may be explained, qualitatively at least, using the presently accepted model of semiconductor surfaces. The explanations are based on the creation by ionizing radiation of localized charged energy states on semiconductor surfaces.

These states are created both at the termination of a semiconductor lattice itself, the so-called "fast" states, and in any surface layer, such as an oxide, the so-called "slow" states. The slow states are the more numerous and the charge they contain controls the surface potential and hence the number and type of charge carriers in the surface region. The fast states, on the other hand, are the states which actually interact directly with the surface charge carriers. They act as generation and recombination centers for holes and electrons, and their activity is measured by the surface recombination velocity, which depends on the surface potential.

As a result of irradiation, a device accumulates charge principally in the slow states, and this charge affects the underlying semiconductor surface. As a result of changes in the surface potential, the surface recombination-generation may be increased (because of changes in both the recombination velocity and the number of fast states), causing device degradation. Inversion layers (channels) may also be formed at p-n junctions, leading to increased reverse leakage currents and degraded emitter efficiency.

For nonpassivated devices, the slow states are in close proximity to the surface and hence strongly influence the surface layer. These devices are, therefore, very sensitive to ambient changes such as those caused by radiation. In passivated devices, the slow states tend to be further removed from the semiconductor surface, and hence these devices are generally one or two orders of magnitude less sensitive to radiation.

For nonpassivated devices in a gaseous ambient, the mechanism by which radiation produces charge in the slow surface states is reasonably well established. Radiation produces gaseous ions, some of which are attracted by electric fields to the device surface, where they subsequently deposit charge. When sufficient ionic charge (generally positive) has been collected on the surface, inversion layers (channels) form on the underlying semiconductor which in turn alter junction leakage currents and transistor gain. For a pnp device, channels tend to form on the p-type collector side, causing large increases in I_{CBO}. The surface recombination in the n-type base region is relatively unaffected by this positive surface charge, and therefore the h_{FE} degradation is usually minor. For npn transistors, on the other hand, the channel forms on the base. Because the base width of a transistor

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is usually small, this channel is restricted in size and hence I_{CBO} does not increase as much as for pnp devices. However, recombination at the base surface is increased, causing a large decrease in h_{FE}. If the base channel extends from the collector to the emitter, then I_{CEO} will increase and h_{FE} may appear to increase because of the increase in I_C.

The simple model used to explain the degradation of nonpassivated devices is of somewhat limited usefulness. It does predict the bias dependence of degradation and also the recovery of devices under proper conditions. However, this model at present does not explain the observed memory effects, nor does it generally apply to devices with grease or similar ambients.

The number of passivated Si planar devices has greatly increased in the past few years and will most likely continue to do so in the future. Thermally grown SiO_2 films are used to passivate the surfaces of these devices by stabilizing the interface structure and isolating the Si from the ambient. The SiO_2 film becomes, therefore, an integral part of the device and it is necessary to understand the role this passivation layer plays when the device is subjected to radiation.

It is well established that the surfaces of passivated devices degrade in ways quite similar to nonpassivated devices when exposed to radiation, although they are generally less sensitive than their nonpassivated counterparts. The degradation appears to result from the formation of positive surface charge in or on the oxide, with the consequent production of channels on the device surface. The channels manifest themselves by increased junction leakage currents and reduced transistor gain. The behavior of npn and pnp transistors follows the pattern outlined above for the nonpassivated case. Passivated devices also exhibit memory and recovery effects similar to those observed with nonpassivated devices.

The main point of controversy among the models used to explain the degradation is the process by which the positive surface charge accumulates. In one view, the charge is created by ionization of impurities on the surface of the oxide, and these ions are then separated by surface electric fields. The majority of experiments, however, indicate that the charge exists within the SiO_2, probably close to the SiO_2-Si interface. Several species of charge carrier, including Na^+ ions, oxygen vacancies, and electrons, have been suggested as the means by which charge is transported through the oxide. None of these has, as yet, been conclusively demonstrated as the responsible carrier, nor has the role played by radiation in the accumulation process been clarified.

MOS-FETs have been shown to be quite sensitive to radiation, more sensitive than conventional passivated devices. The cause again appears to be positive charge

accumulation in the oxide near the SiO_2-Si interface. Presumably, the explanations of degradation in MOS-FETs and passivated devices will be very similar, since the same oxide is used in both cases.

It has been found experimentally that oxide-covered Si surfaces invariably tend to be n-type regardless of the conductivity type of the Si. This fact implies the existence of a rather large built in positive charge in the oxide after the growth of the film. If the SiO_2-Si interface is viewed on a heterojunction, it can be shown that, as a natural result of the work function difference between the SiO_2 and the Si, the Si surface should have an equilibrium charge density of $\sim 10^{11}$ electrons/ cm^2. The oxide will, of course, have a positive charge density of equal magnitude.

It may well be that, during growth of an SiO_2 film, the equilibrium charge density is not attained. Furthermore, it cannot be attained after growth at room temperature since the oxide cannot supply suffficient electrons to the Si because of the large energy gap of the oxide. Radiation will, however, cause ionization in the SiO_2 and allow at least some equilibration of charge, i.e., further accumulation of positive charge in the oxide. This rather simple picture of a SiO_2-Si interface can be elaborated to explain, qualitatively at least, many of the observed features of degradation, such as saturation and rate effects.

The need for further work on both fundamental and practical problems in surface radiation effects is self-evident. Devices, particularly those suitable for low-level logic in space applications, will require extensive study, since these device types are likely to be quite sensitive to surface radiation effects.

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