FAST LOGIC CIRCUIT TEST ASSEMBLY

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ELECTRONIC SYSTEMS DIVISION

AIR FORCE SYSTEMS COMMAND

UNITED STATES AIR FORCE

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Project 5080

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ABSTRACT

This document describes the Fast Logic Circuit Test Assembly built to evaluate the system operating characteristics of nanosecond switching circuits which have been developed at The MITRE Corporation. The Test Assembly, which includes most of the classes of logic functions which might be encountered in a full scale serial or parallel computer, will also serve as a vehicle for evaluation of circuit reliability and for signal and power distribution methods.

The Test Assembly includes two serial registers which use electromagnetic delay line storage. The shift registers, associated with these delay lines to implement the serial-to-parallel conversion or vice versa, shift at a 100-mc rate. Also included, in addition to a 100-mc counter and various control networks, is an 8-bit parallel adder which may be expanded using identical adder modules to form a 64-bit adder with 30-nanosecond addition time.

REVIEW AND APPROVAL

This technical report has been reviewed and is approved.

SEYMOUR JEFFERY
Major, USAF
Chief, Computer Division

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ILLUSTRATIONS

SECTION I

INTRODUCTION

The purpose of the Fast Logic Circuit Test Assembly is to evaluate the system operating characteristics of nanosecond switching circuits which have been developed at The MITRE Corporation. The test assembly includes most of the classes of logic functions which might be encountered in a full-scale, serial or parallel computer.

Specifically, the test assembly consists of a 48-bit-input serial register which communicates with a shift control network through an 8-bit, serial-to-parallel converter. The shift control network couples to an 8-bit, parallel adder, which in turn couples to an 8-bit, parallel-to-serial converter that is integral with a 48-bit, serial-output register. Appropriate control sequencing circuits are also included. Normal operation consists of two cycles: an add cycle followed by a subtract-and-compare cycle; 100% checking results.

The input and output registers use electromagnetic delay-line storage operating at a 50-mc clock rate (NRZ) which corresponds to a 100-mc information-bit rate.

The circuitry associated with the serial storage is synchronous and includes 8-bit shift registers which shift at a 100-mc rate. The shift registers implement the serial-to-parallel and parallel-to-serial conversions.

The 8-bit parallel adder is asynchronous and utilizes single-level, 4-bit, carry anticipation. Execution time is approximately 20 nanoseconds for an 8-bit addition. The adder modules may be used to build a 64-bit parallel adder with 30-nanosecond addition time (see page 10).

The test assembly will serve as a vehicle for evaluation of circuit reliability and methods for signal and power distribution. All electronic

components have been measured and catalogued for the purpose of correlating circuit performance during all phases of testing. Initially, the circuit components will be conventional, discrete, semiconductors and passive components mounted on printed circuit cards. There are nine logic cards and 268 circuit cards.

SECTION II

GENERAL DESCRIPTION

In the test assembly, except for the timing and control networks, the functional blocks used are those which are commonly used in general-purpose digital systems. Certain of these functional blocks, in either 4-bit or 8-bit parallel form, are designed for maximum operating speed, although no particular effort was made to obtain savings in hardware. The serial one-word registers and conversion registers are also essential elements of a serially organized computer.

Figure 1 is the system block diagram; Figure 2 is a timing chart.

NORMAL OPERATIONS

The shift register P, which is a part of the 48-bit-input, serial register, converts serial information to 8-bit, parallel form in addition to receiving input information in 8-bit parallel blocks during the input phase, IN. The output register Z, is used to obtain parallel-to-serial conversion. P and Z are simple shift registers.

The natural cycles of the system have a period of 144 clock times (3 times 48 bit times). During the first 48 bit-times, T1, the 8-bit, parallel information block in Register P (bits P_0 through P_7) is strobed into Register A at the zeroth bit time, T^0. t_0 (mod 8) and becomes block $\{A_0 \ldots A_7\}$. At the output of Register A, this information $\{A_0 \ldots A_7\}$, is transferred to an 8-bit, parallel adder through one of the three paths on the shift control network. The path taken depends on whether a one-bit, toggle switch, control register, CR, is one or zero.

If CR is equal to one, then the eight bits of information are transferred to the adder and added to a constant stored in the 8-bit toggle switch register.

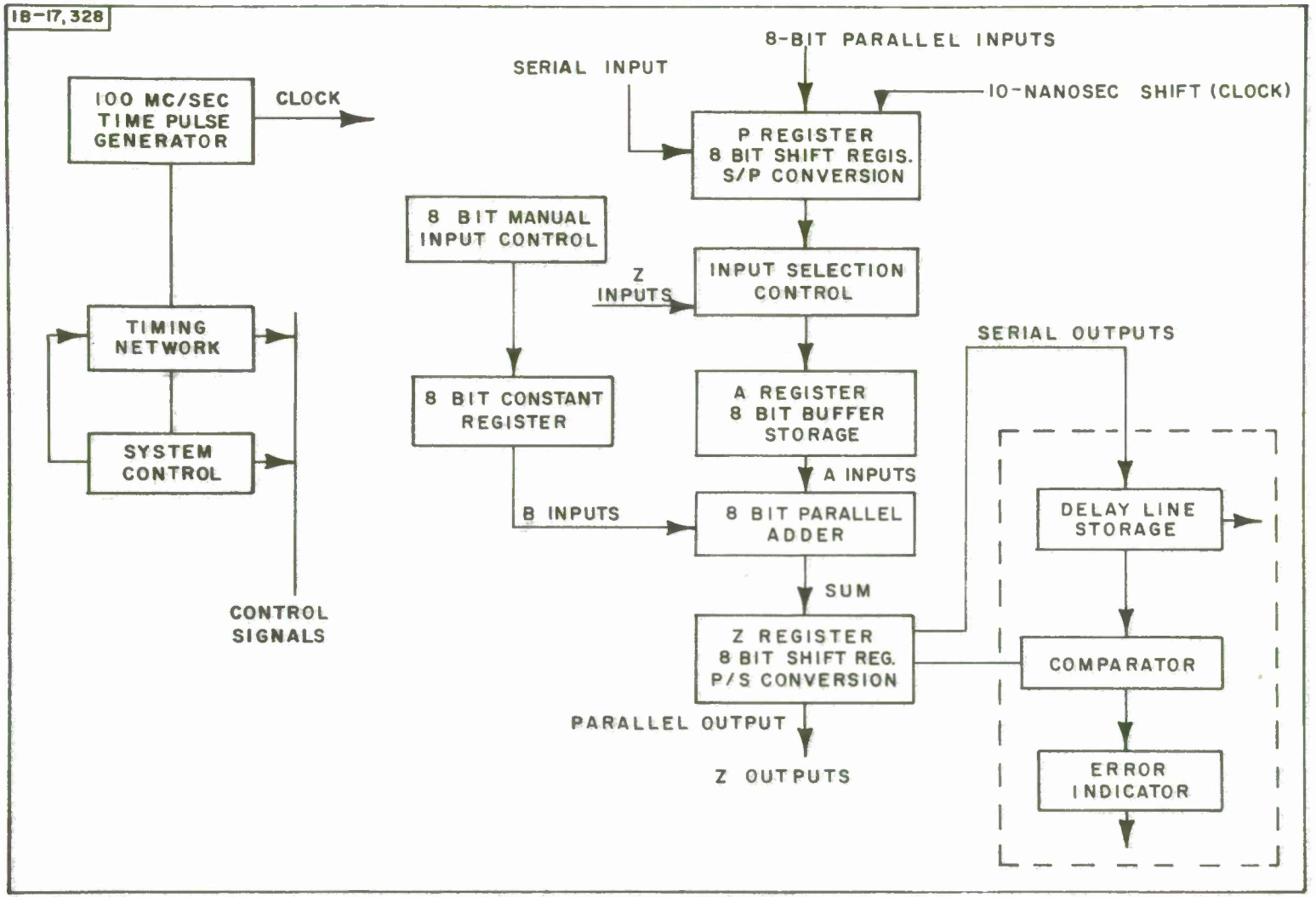


Figure 1. System Block Diagram

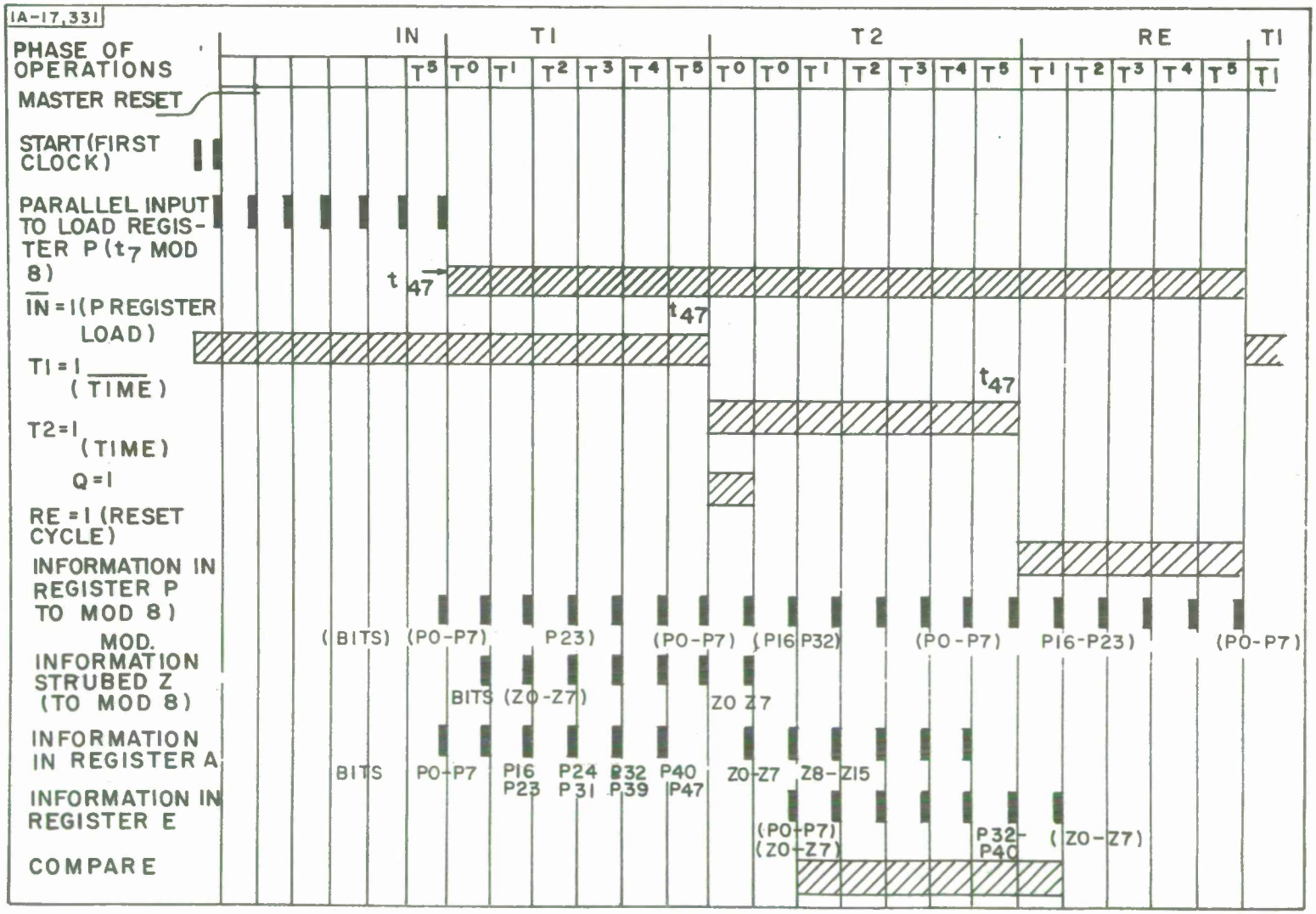


Figure 2. System Timing Chart

At time $T^0 \cdot t_7$ (mod 8), the last bit time in the block time, the result from the adder (modified information) is transferred into the output register, Z, where it is converted back to serial form, and stored in the output 48-bit serial register. At the next zeroth bit time, $T^1 \cdot t_0$ (mod 8), the next information block (bits P_8 through P_{15}) in Register P is transferred to Register A and a similar operation is again performed.

If CR content is zero, the information bits are first end-shifted left one position $\{A_1 \ldots A_7, A_0\}$ before being transferred to the adder for a zero addition. The control register CR must be set before system operation is started. The contents of the registers at each t_0 (mod 8) is shown in the system timing chart, Figure 2. At the last bit time in this phase, $T^5 \cdot t_7$ (mod 8) = t_{47}, the register TIME in the control network is set and the system goes into the second operation phase, T2.

T2 actually lasts 52 bit-times. During the first 8-bit time, T^0, the system is "idling." At the 8th-bit time of this idling period, the timing circuit is reset to $T^0 \cdot t_0$ (mod 8) and the first 8-bit modified information block $\{Z_0 \ldots Z_7\}$ in Register Z is strobed into the storage register — Register A.

In this phase, if control register CR is equal to one, the content of the constant register is subtracted from the information $\{A'_0 \ldots A'_7\}$ passing through the adder. The subtraction is done by adding the 2's complement of the constant to the operand A'. The result from the adder is strobed into Register Z at $T^0 \cdot t_7$ (mod 8). The next information block $\{Z_8 \ldots Z_{15}\}$ is strobed into Register A at the same time. At time $T^1 \cdot t_0$ (mod 8), the information in Register Z is equal to the corresponding 8-bit block in Register P (See Figure 2).

If CR is equal to zero, the eight bits of information are cycled right one position $\{A_7, A_0 \ldots A_6\}$ before the 8-bit block reaches the adder, and the constant is again zero. At the end of phase T2, $T^5 \cdot t_7$ (mod 8), reset Register RE and the reset phase starts. In this period, zeros are fed into output Register Z and the content of Register P is not changed.

MANUAL CONTROLS

If at any time during T1, the information-hold switch is turned on, the system will stay in the phase T1 until the switch is turned off, whereupon the system will continue its normal operation as described above. If the switch is turned on during other phases of operation, the system will go through the natural cycle until phase T1 is reached. It will then remain in phase T1 until the switch is turned off.

After Master Reset Time, the system starts its natural cycle when the start pushbutton is activated. Before the first manual phase, information may be transferred in 8-bit parallel form into the input Register P. This period during which the register IN is in "one" state is called the "input" phase.

SECTION III

DESCRIPTION OF FUNCTIONAL BLOCKS

The test assembly will be built with logic boards, each of which may mount 70 logic circuits that perform logic functions described in Figure 3. The logic boards used in the system are listed in Table I. The input and output signals to and from these logic boards are levels (as contrasted to pulses).

The following logical equations describe each of the functional blocks used:

1. Registers P and A (Figure 4)

Let

$$F = T1 \cdot C \cdot \overline{IN} \cdot t_0 \pmod 8$$

$$G = T2 \cdot C \cdot \overline{Q} \cdot t_7 \pmod 8$$

then

$$S_{p_i} = P_{i+1} \cdot C \oplus U_i\,(1) \cdot \text{strobe}$$

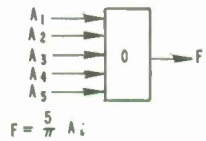
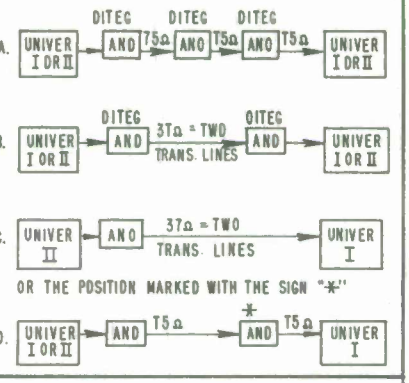
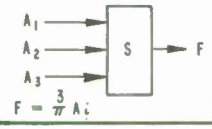
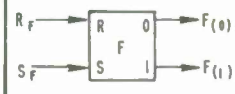
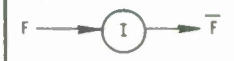
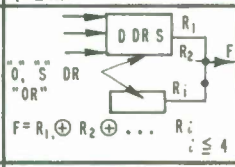
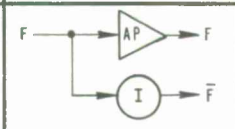
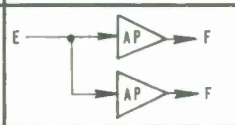
$$R_{p_i} = \overline{P}_{i+1} \cdot C \oplus U_i\,(0) \cdot \text{strobe}$$

$$S_{A_i} = P_i \cdot F \oplus Z_{i+1} \cdot G$$

$$R_{A_i} = \overline{P}_i \cdot F \oplus \overline{Z}_{i+1} \cdot G$$

where

$$i = 0, 1, \ldots 7$$

LOGIC FUNCTIONS	LOGIC SYMBOL	TYPES OF CIRCUIT USED	FAN IN FAN OUT	REMARKS
AND "•"		DITEG	FAN IN = 5 FAN OUT = 8 (TWO TRANS-MISSION LINES)	1. 2 GATES PER PACKAGE 2. THESE TYPES OF AND GATES MUST BE USED IN THE FOLLOWING LOGIC CONFIGURATIONS: 
		SIDEL	FAN IN = 3 FAN OUT = 8 (TWO TRANS-MISSION LINES)	2 CIRCUIT PER PACKAGE
FLIP-FLOP		UNIVER I	EACH SIDE OF FLIP-CAN DRIVE (TWO TRAN. LINES 8 AND GATES)	1 CIRCUIT PER PACKAGE
INVERSION		UNIVER I	OUTPUT CAN ORIVE (TWO TRANS-MISSION LINES)	2 CIRCUIT PER PACKAGE
OR "+"		ALTG	FAN IN = 4 FAN OUT = 8 (TWO TRAN. LINES)	1 CIRCUIT PER PACKAGE
BUFFER OR "⊕"				THIS FUNCTION IS ACCOMPLISHED BY WIRING BY WIRING THE OUTPUTS OF AND GATES OR OR GATES TOGETHER
AMPLIFICATION INVERTER		UNIVER II	EACH OUTPUT CAN ORIVE TWO TRAN. LINES (8 AND OR OR GATE)	1 CIRCUIT PER PACKAGE
AMPLIFICATION EITHER BOTH + OR BOTH −		UNIVER	EACH OUTPUT CAN DRIVE TWO TRAN. LINES (8 AND OR OR GATES)	1 CIRCUIT PER PACKAGE
DELAY		DELAY LINES		

IC-17,332

Figure 3. Logic Functions

2. Adder (Figure 5)

Let

$$D_i = A_i \cdot B_i; \quad T_i = \overline{A}_i B_i \oplus \overline{B}_i A_i$$

where

$$i = 0, 1, \ldots 3$$

$$C_1 = D_0 \oplus T_0 \cdot C_0$$

$$C_2 = D_1 \oplus T_1 \cdot D_0 \oplus T_1 \cdot T_0 \cdot C_0$$

$$C_3 = D_2 \oplus T_2 \cdot D_1 \oplus T_2 \cdot T_1 \cdot D_0 \oplus T_2 \cdot T_1 \cdot T_0 \cdot C_0$$

$$D_G = D_3 \oplus T_3 \cdot D_2 \oplus T_3 \cdot T_2 \cdot D_1 \oplus T_3 \cdot T_2 \cdot T_1 \cdot D_0$$

$$T_G = T_0 \cdot T_1 \cdot T_2 \cdot T_3$$

$$RS_i = T_i \overline{C}_i \oplus \overline{T}_i C_i$$

This 4-bit adder module was designed to achieve maximum speed when it is grouped with other identical modules to form a parallel adder which is capable of adding two 64-bit binary numbers in 30 nanoseconds (12 stage delays). For detailed design information, see Fast Circuit Design Note, JL-1.

3. Register Z (Figure 6)

Let

$$F = \overline{Q} \cdot C \cdot t_7 \pmod 8$$

Set

$$Z_i = Z_{i+1} \cdot C \oplus RS_i \cdot F$$

$$R_{Z_i} = \overline{Z_{i+1}} \cdot C \oplus RS_1 \cdot F$$

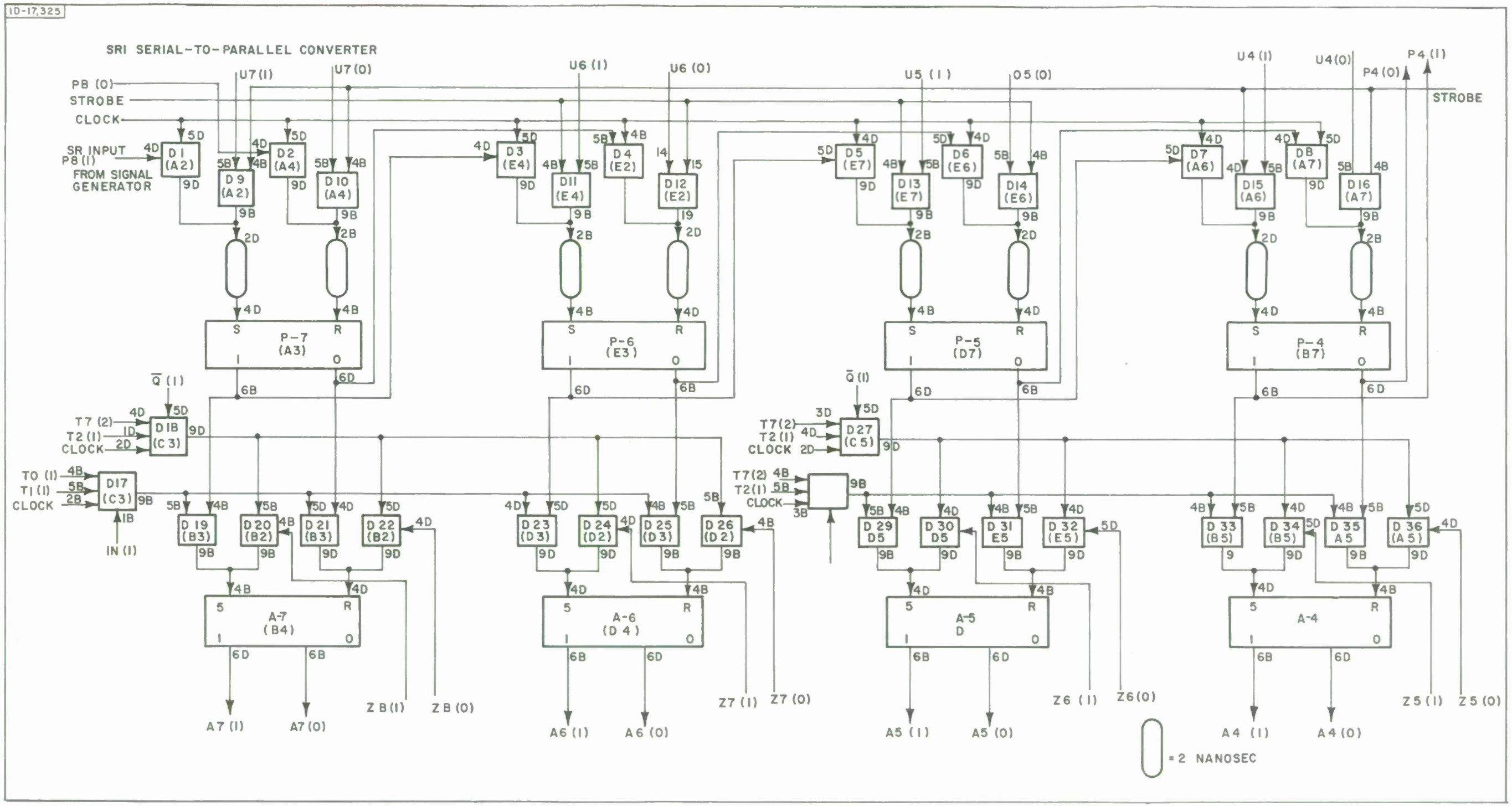


Figure 4. Serial-to-Parallel Converter

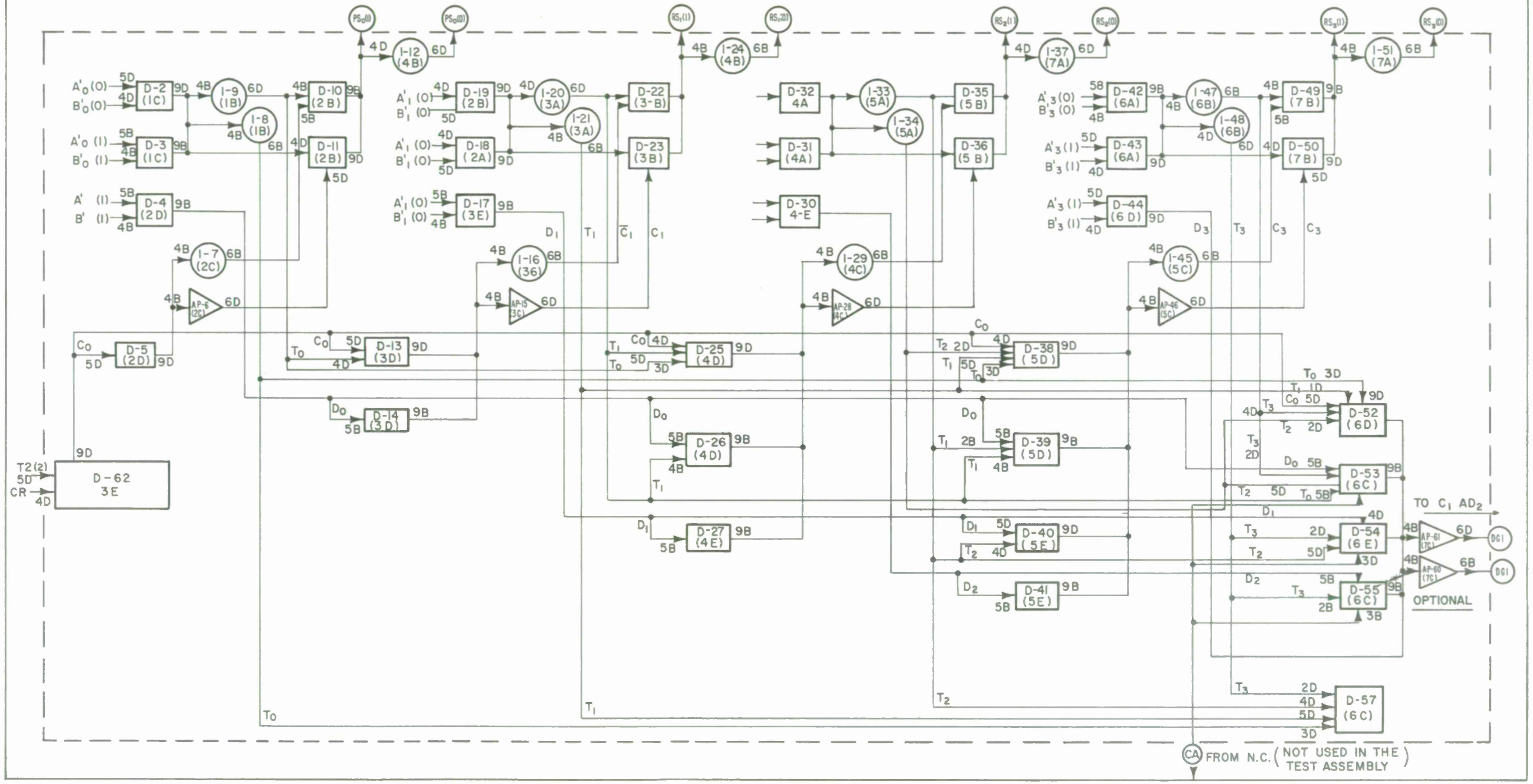


Figure 5. Adder

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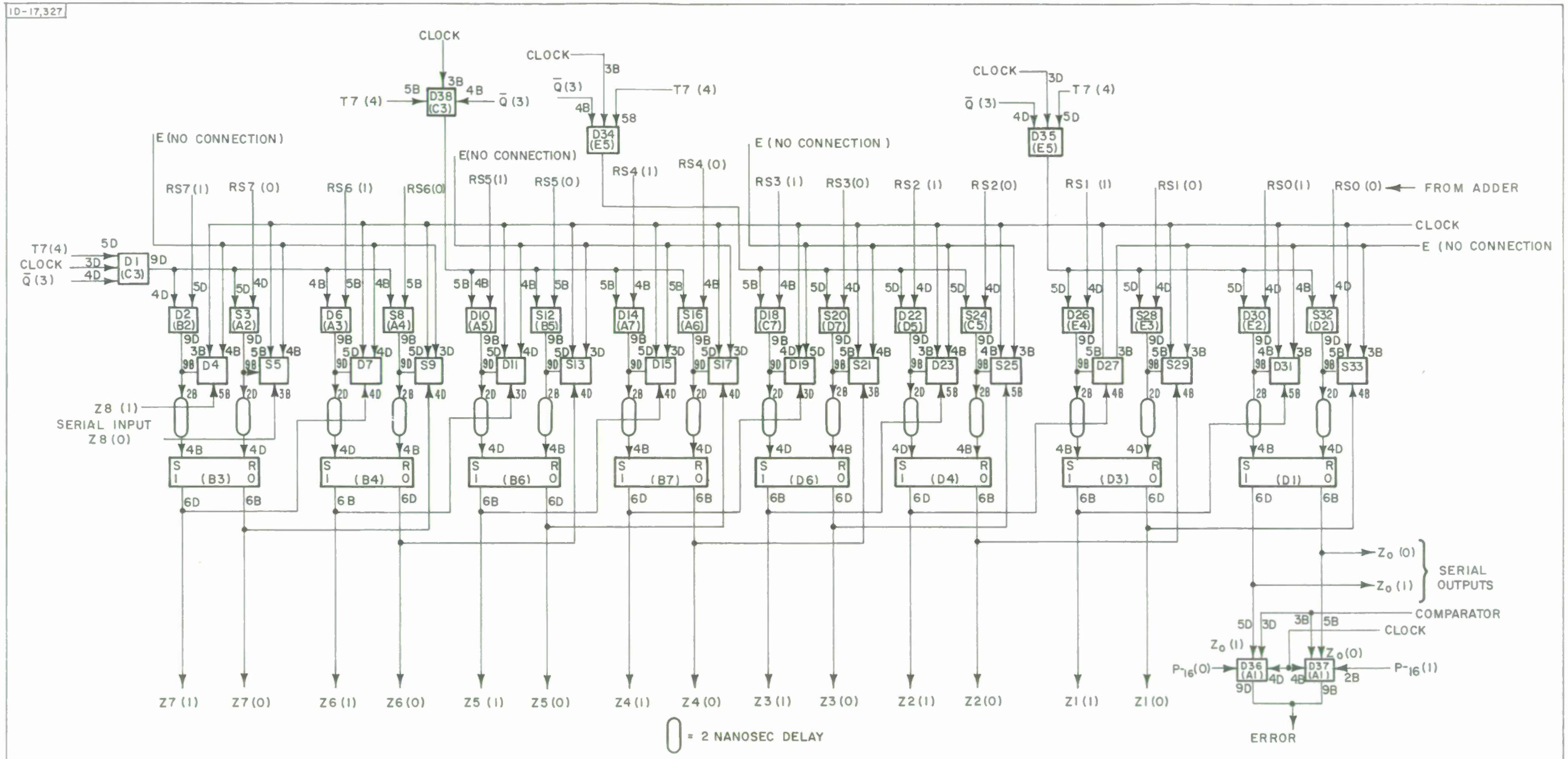


Figure 6. Parallel-to-Serial Converter

$$\text{ERROR} = C \cdot Z_0 \cdot \overline{P}_{-16} \cdot \text{comp} \oplus C \cdot \text{comp} \cdot \overline{Z}_0 \cdot P_{-16}$$

4. Control Circuits

Let

$$NO = \overline{IN} \cdot \overline{CH}$$

$$S_{TIME} = t_{47} \cdot C \cdot NO \cdot \overline{RE} \cdot \overline{TIME}$$

$$R_{TIME} = t_{47} \cdot C \cdot \overline{IN} \cdot \overline{RE} \cdot TIME \oplus MR$$

$$T1 = (\overline{TIME}) \cdot (RE)$$

$$T2 = (TIME) \cdot (RE)$$

$$S_Q = T1 \cdot N0 \cdot (t_{47} \cdot C)$$

$$R_Q = Q \cdot (t_7 \ (\text{mod } 8)) \cdot C \oplus MR$$

$$S_{RE} = t_{47} \cdot C \cdot T2$$

$$R_{RE} = MR \oplus RE \cdot (t_{47} \cdot C)$$

$$S_I = (t_{47} \cdot C) \cdot \overline{I}$$

$$R_I = MR$$

$$S_{IN} = MR$$

$$R_{IN} = IN \cdot I \cdot (t_{47} \cdot C)$$

$$S_{comp} = T2 \cdot (t_7 \ (\text{mod } 8)) \cdot \overline{Q} \cdot C$$

$$R_{comp} = t_7 \ (\text{mod } 8) \cdot RE \cdot C \oplus MR$$

5. Timing Networks (Figures 7, 8, 9)

Counter L

$S_{Lo} = \bar{L}_0 \cdot C \oplus MR$

$R_{Lo} = L_0 \cdot C$

$S_{L_1} = \bar{L}_1 \cdot L_0 \cdot C \oplus MR$

$R_{L_1} = L_1 \cdot L_0 \cdot C$

$S_{L_2} = \bar{L}_2 \cdot L_1 \cdot (\bar{L}_0) \cdot C \oplus MR$

$R_{L_2} = L_2 \cdot L_1 \cdot (\bar{L}_0) \cdot C$

$T_0 \pmod 8 = \bar{L}_0 \cdot \bar{L}_1 \cdot \bar{L}_2$

$T_7 \pmod 8 = L_0 \cdot L_1 \cdot L_2$

$t_{47} = L_0 \cdot L_1 \cdot L_2 \cdot M_0 \cdot M_2$

Counter M

Let $F = L_2 \cdot L_1 \cdot L_0 \cdot \bar{t}_{47} \cdot \bar{Q}$

$S_{Mo} = \bar{M}_0 \cdot C \cdot F \oplus MR \oplus RE \cdot Reset \cdot C$

$R_{Mo} = M_0 \cdot C \cdot F \oplus Reset \cdot C \cdot \overline{RE}$

$S_{M_1} = \bar{M}_1 \cdot M_0 \cdot C \cdot F$

$R_{M_1} = M_1 \cdot M_0 \cdot C \cdot F \oplus Reset \cdot C$

$S_{M_2} = \overline{M_2} \cdot M_1 \cdot M_0 \cdot C \cdot F \oplus MR$

$R_{M_2} = M_2 \cdot M_1 \cdot M_0 \cdot C \cdot F \oplus Reset \cdot C$

$Reset = M_0 \cdot M_2 \cdot G \oplus M_0 \cdot \bar{M}_1 \cdot M_2 \cdot \bar{Q}$

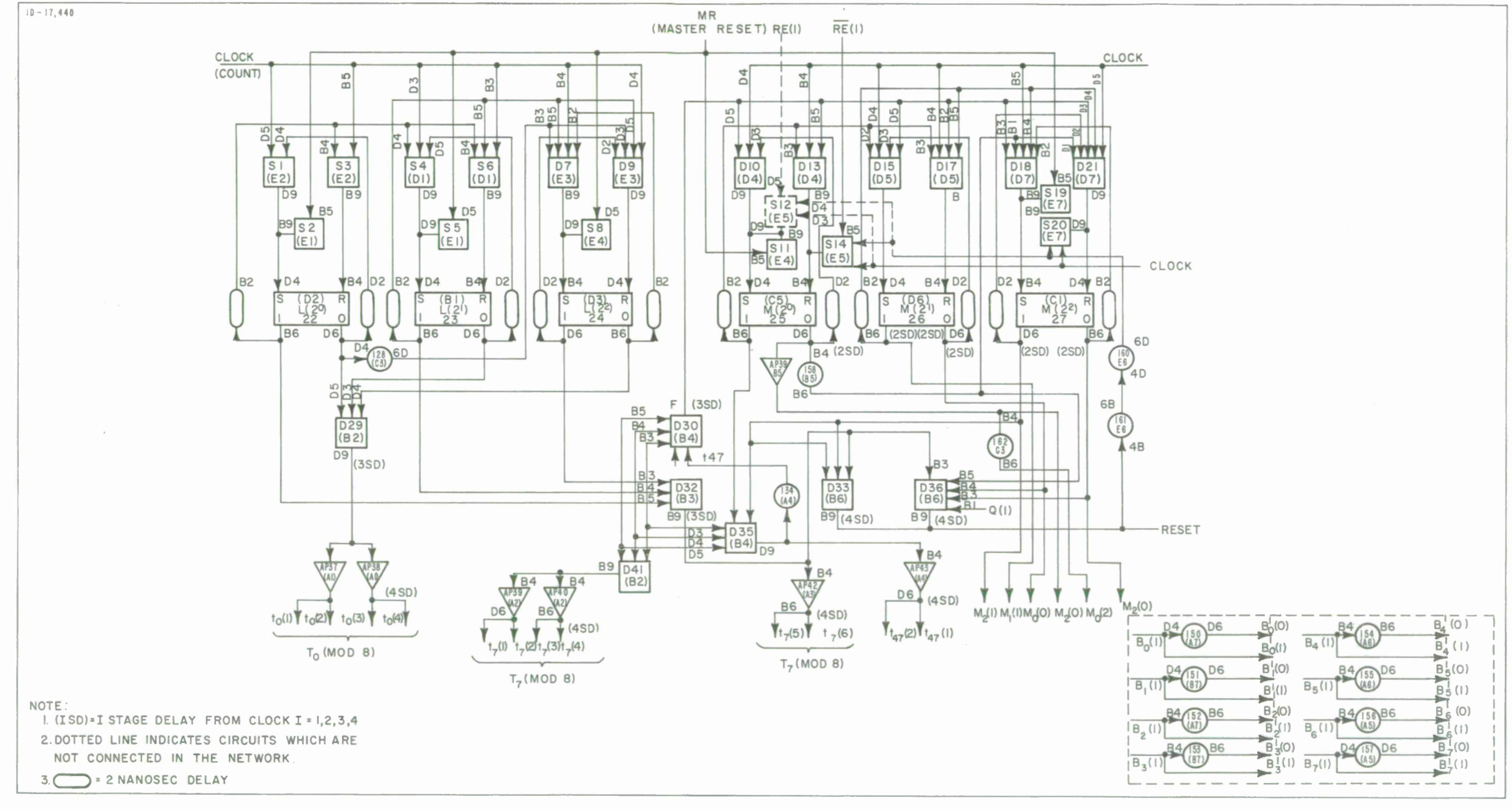
6. Constant Register (Figure 10) and Shift Control Networks (Figure 11)

$$B_i = CR \cdot T1 \cdot CT_i$$

where

$$i = 0, 1, 2, \ldots 7$$

$$\bar{B}_i = CR \cdot T2 \cdot \overline{CT_i}$$



NOTE:
1. (ISD)=I STAGE DELAY FROM CLOCK I = 1,2,3,4
2. DOTTED LINE INDICATES CIRCUITS WHICH ARE NOT CONNECTED IN THE NETWORK.
3. ⬭ = 2 NANOSEC DELAY

Figure 7. Timing Networks

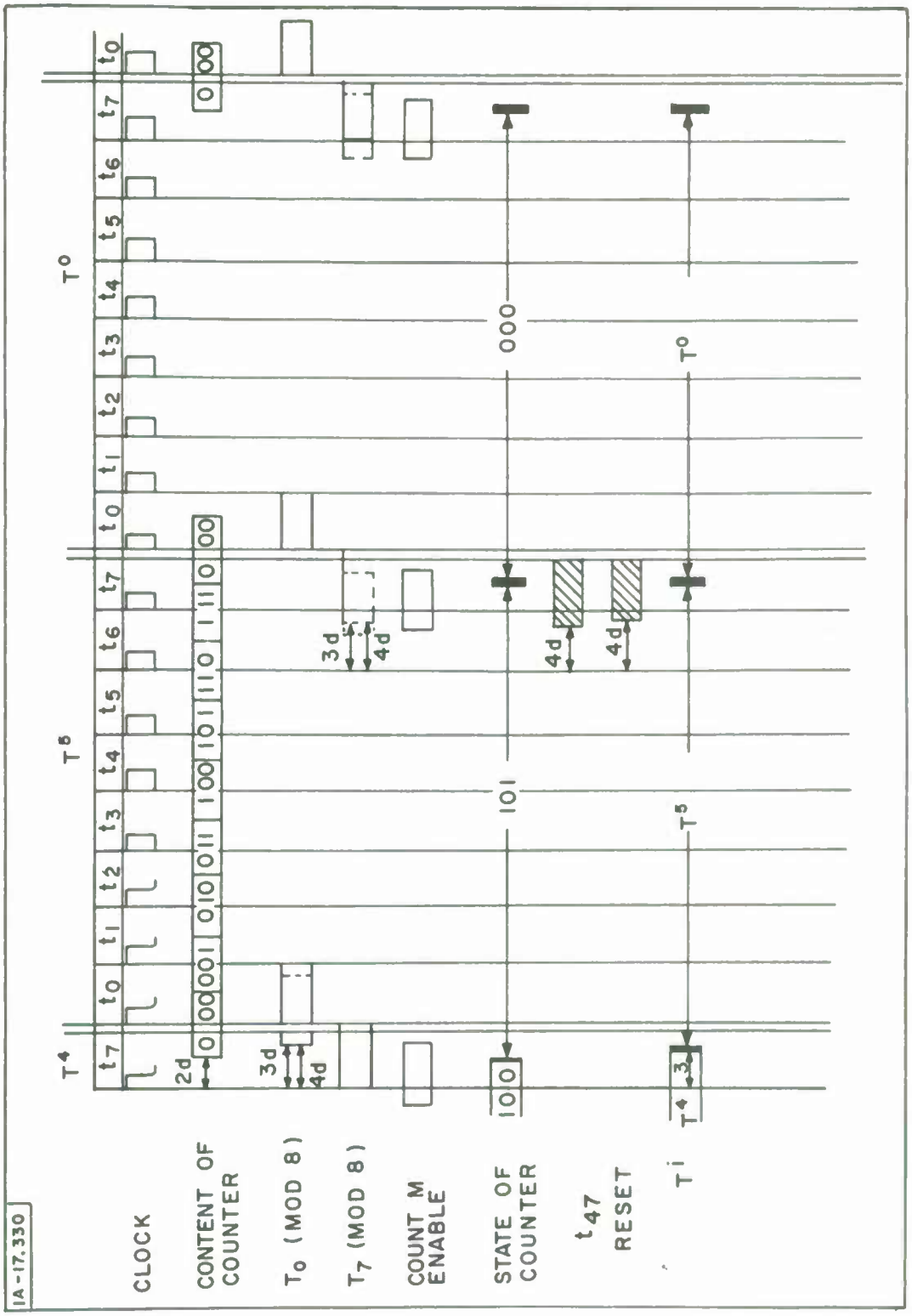


Figure 8. Timing Chart for Timing Network

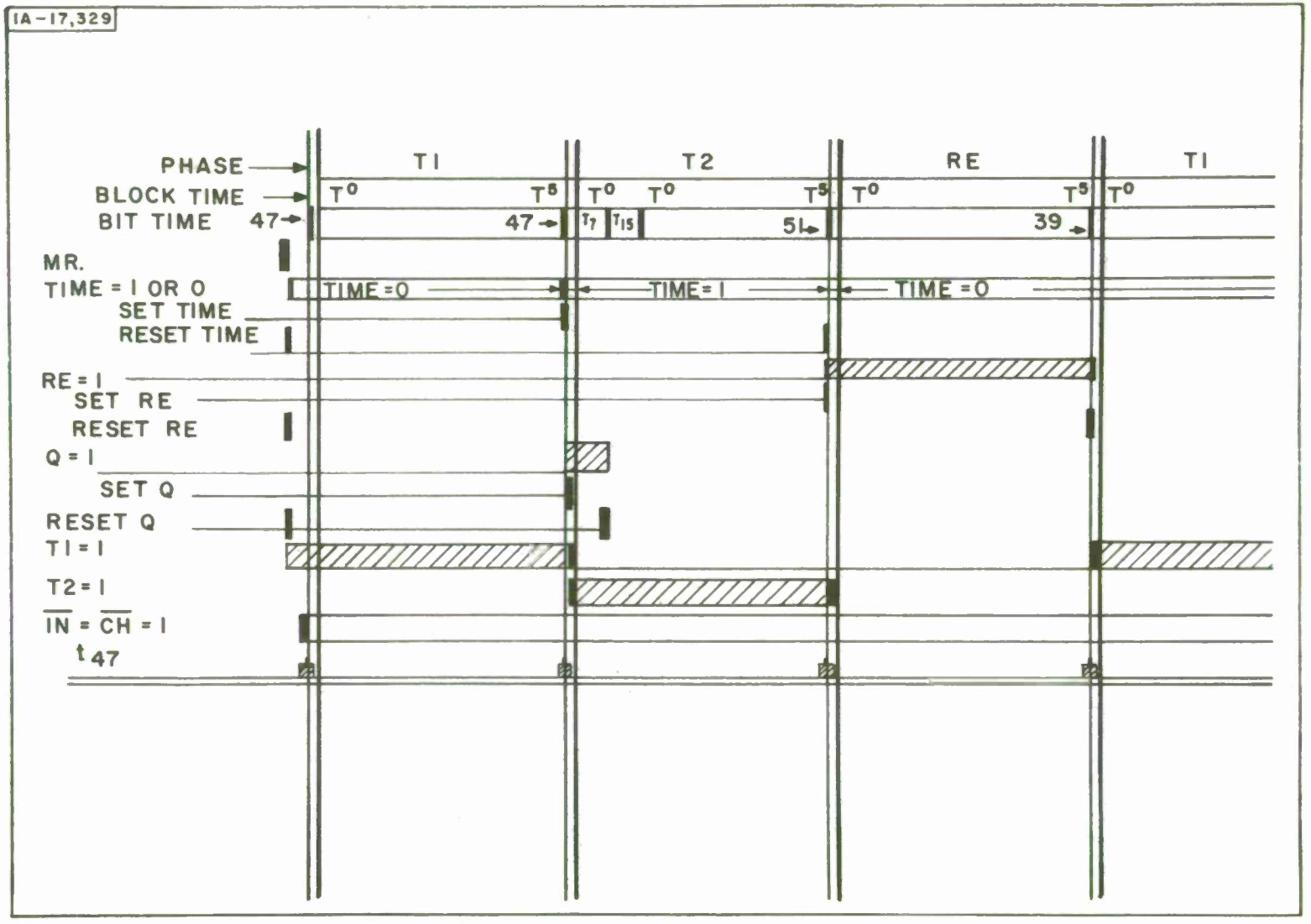


Figure 9. Control Network Timing Chart-Natural Cycle

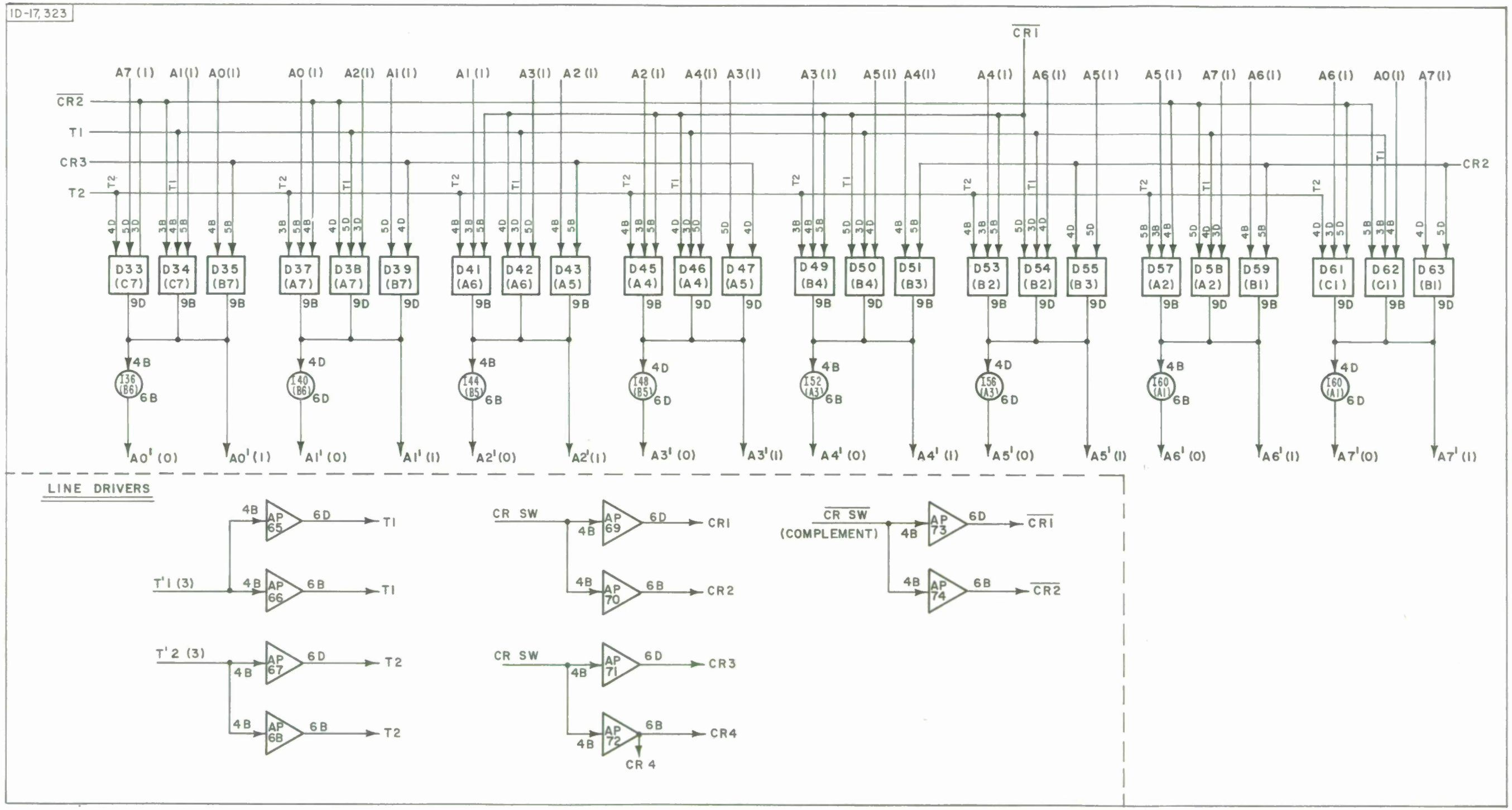


Figure 10. Constant Register

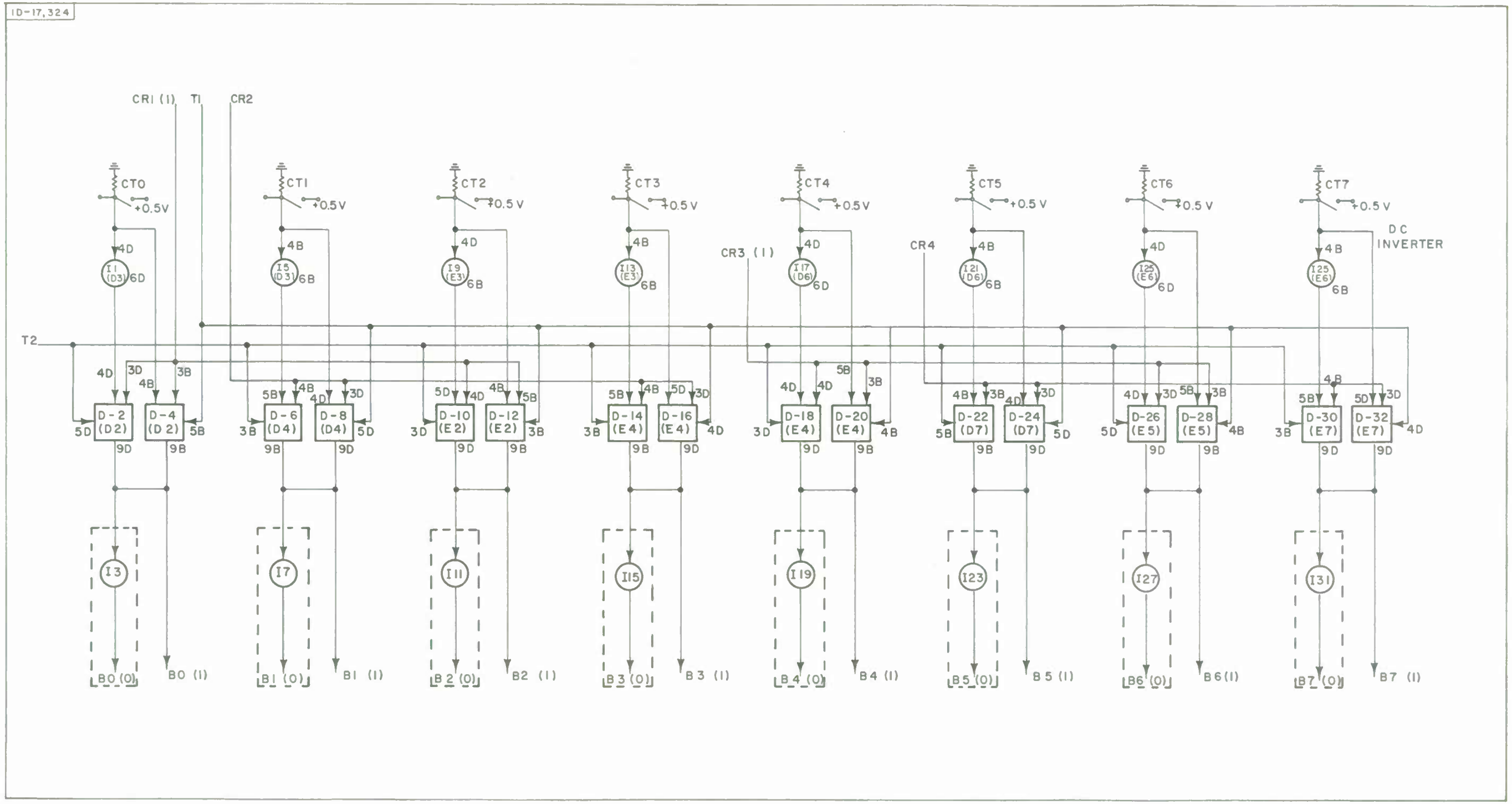


Figure 11. Shift Control Network

$$A'_i = A_i \cdot CR \oplus \overline{CR} \cdot T1 \cdot A_{i+1} \oplus \overline{CR} \cdot T2 \cdot A_{i-1}$$

for

$$i = 0, 1, \ldots 7$$

and the addition or subtraction of subscribed is in mod 8

$$\overline{A'_i = A_i \cdot CR + \overline{CR} \cdot T1 \cdot A_{i+1} \oplus \overline{CR} \cdot T2 \cdot A_{i-1}}$$

TABLE I

Functional Blocks / Description	Adder	Parallel-To-Serial Converter S Registers	SRI Serial-To-Parallel Converter P&A Register	Constant Register & Shift Control Network	System Operation Control	Timing Network	Misc.
UNIVER I	6	8	8	8	7	12	5
UNIVER II	6			5	1	4	
PDA		3	3		3	3	
Board PDA		1	1		1	1	
DITEG and Gate	19	19	18	20	9	13	5
SIDEL					2	2	
2-Nanosecond Delays		16	8		11	13	
OR Gate							1
Register Packages	25	25	25	25	25	25	
No. of Boards Req. in the System	2	1	2	1	1	1	
Logical Diagram	Fig. 5	Fig. 6	Fig. 4	Fig. 10, 11		Fig. 7	

Unclassified
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13. ABSTRACT

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DD FORM 1 JAN 64 1473

Unclassified
Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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Logic circuits						
Digital computer						
Serial computer						
Parallel computer						
Serial-to-parallel conversion						
Parallel-to-serial conversion						

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