ESD-TDR-65-421



# Technical Note

1965-43

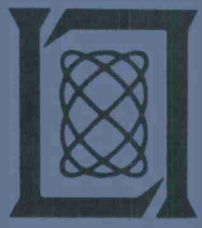
B. E. White

# Conceptual Description of a Family of Frequency Synthesizers

8 September 1965

Prepared under Electronic Systems Division Contract AF 19(628)-5167 by

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Lexington, Massachusetts



The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology, with the support of the U.S. Air Force under Contract AF 19(628)-5167.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

# CONCEPTUAL DESCRIPTION OF A FAMILY OF FREQUENCY SYNTHESIZERS

*BRIAN E. WHITE*

*Group 66*

TECHNICAL NOTE 1965-43

8 SEPTEMBER 1965

LEXINGTON MASSACHUSETTS

## ABSTRACT

A family of frequency synthesizers is described. Each member of the family generates one of many equally-spaced frequencies by utilizing identical modules, the number of which is related to the number of possible frequencies. For any design in the family which uses frequency division in the modules, there exists a dual design which utilizes frequency multiplication. Block diagrams and formulas are included which may be useful in designing frequency synthesizers for communication system applications.


Accepted for the Air Force
Stanley J. Wisniewski
Lt Colonel, USAF
Chief, Lincoln Laboratory Office

# CONCEPTUAL DESCRIPTION OF A FAMILY OF FREQUENCY SYNTHESIZERS

## I. INTRODUCTION

A frequency synthesizer is a deterministic, time-invariant device which produces one of a number of possible output frequencies when a particular input is applied. Such a device is useful for anti-jam and/or multiple-access communication systems.

For purposes of this report, it is convenient to restrict the discussion to frequency synthesizers which perform a one-to-one mapping between a set of binary inputs and a set of sinusoidal outputs. Two classes of synthesizers will be described – one based on frequency division, and one based on frequency multiplication in each of several identical modules. The report is intended as a guide for designing frequency synthesizers of the type described.

The idea of implementing frequency synthesizers by modular composition is not new. In particular Group 62 has developed a synthesizer for the Lincoln Experimental Terminal (LET) which is based on octal frequency division in each module.

## II. MODULAR COMPOSITION

The function of the frequency synthesizer is to select one of N possible frequencies spaced B cps apart. It is assumed that N is at least an order of magnitude greater than unity and a power-of-two, so that each particular output frequency can be uniquely specified by $\log_2 N$ bits. For large N the complexity of the synthesizer can be greatly reduced by generating fewer frequencies directly and by utilizing an iterative technique involving identical modules as shown in Fig. 1. The synthesizer consists of a frequency generator, n identical modules (each composed of one stage and one switching network), and a frequency converter.

From a single frequency standard the frequency generator produces $f_o$, $f_c$, $f_g$, and $\Delta f$. The frequencies $f_o$ and $f_c$ feed only stage 1 and the frequency converter, respectively. Let the $2^m$ frequencies be designated $f_g + i_k \Delta f (1 \le k \le n)$, where

$$-2^{m-1} + 1 \le i_k \le 2^{m-1} \quad (m \ge 1) \qquad . \qquad (1)$$

These $2^m$ equally-spaced frequencies all feed each switching network.

Each switching network receives an independent set of m bits from an external source which uniquely specifies one of the $2^m$ frequencies. The function of switching network k is to pass only the specified frequency $f_g + i_k \Delta f$ to stage k.

Stage 1 operates on $f_g + i_1 \Delta f$ and $f_o$ so as to produce one of $2^m$ equally-spaced frequencies. Similarly stage k operates on $f_g + i_k \Delta f$ and

the frequency produced by stage k-1 ($k \geq 2$) to produce one of $2^{km}$ equally-spaced frequencies. Thus the integers m and n are related to N by the formula

$$mn = \log_2 N \quad (m, n \geq 1) \quad . \tag{2}$$

Given N, Fig. 1 and (2) define a family of frequency synthesizers with each member uniquely specified by an (m, n) pair. Complete families of (m, n) pairs for several values of N are listed in Table 1.

| N | m | n |
|---|---|---|
| 16 | 1 | 4 |
| | 2 | 2 |
| | 4 | 1 |
| 32 | 1 | 5 |
| | 5 | 1 |
| 64 | 1 | 6 |
| | 2 | 3 |
| | 3 | 2 |
| | 6 | 1 |
| 128 | 1 | 7 |
| | 7 | 1 |
| 256 | 1 | 8 |
| | 2 | 4 |
| | 4 | 2 |
| | 8 | 1 |
| 512 | 1 | 9 |
| | 3 | 3 |
| | 9 | 1 |

Table 1. Families of (m, n) for Several N.

## III. STAGES

A simple method of realizing each stage of the synthesizer is shown in Fig. 2. Following a standard mixing operation the frequency is scaled either down or up by a factor $2^m$, which is equal to the number of possible equally-spaced frequencies produced by switching network k. This scaling insures that the $2^{km}$ possible frequencies produced by stage k are also equally-spaced. Since all stages are identical, the input and output frequencies of each stage must be approximately equal (i.e., $f_k \approx f_o$) regardless of the values assumed by the indices $i_k$. Assuming that $\Delta f$ is sufficiently small, this requirement is satisfied if

$$f_g = (2^m \mp 1)\, f_o \tag{3a}$$

$$f_g = (1 \pm 2^{-m})\, f_o \quad , \tag{3b}$$

where (3a) and (3b) refer to the design options of scaling down or up, respectively. Furthermore, in (3a) the choice of sign depends on whether or not the upper or the lower sideband, respectively, is passed by the bandpass filter. In (3b) the choice depends on which of the two frequencies $f_{k-1}$ or $f_g + i_k \Delta f$ is subtracted in the mixing operation. Thus a total of four design options (which are designated a-1, a-2, b-1, and b-2, respectively) for each family of synthesizers are available. Henceforth results pertaining to these design options will be presented in the same order as (3).

Using (3) and Fig. 2 it can be verified that the output frequency produced by stage n is

$$f_n = f_o + I \Delta f \quad , \tag{4}$$

where

$$I = 2^{-m} i_n \pm 2^{-2m} i_{n-1} + 2^{-3m} i_{n-2} \pm \cdots \pm 2^{-nm} i_1 \qquad (5a)$$

$$I = \pm 2^{m} i_n - 2^{2m} i_{n-1} \pm 2^{3m} i_{n-2} - \cdots \pm 2^{nm} i_1 \quad . \qquad (5b)$$

If the signs in I alternate, the choice of signs of the right-most term in (5) depends on whether or not n is odd or even, respectively. Note from (1) and inspection of (5) that I can assume $N = 2^{mn}$ equally-spaced values. In (5a) and (5b) an incremental change of $1/N = 2^{-nm}$ and $2^{m}$ results from a unit change of $i_1$ and $i_n$, respectively. The range and center value of I are defined as $I_{max} - I_{min}$ and $(I_{max} + I_{min})/2$, respectively. Note that $I_{max}$ and $I_{min}$ are always non-negative and non-positive, respectively. Explicit expressions for $I_{max} - I_{min}$ and $I_{max} + I_{min}$ for all four design options are derived in the Appendix.

As mentioned previously $\Delta f$ must be sufficiently small for (3) to satisfy the requirement that $f_k \approx f_o$. The restriction on $\Delta f$ depends on $f_o$, the (m, n) pair, and the following condition dictated by general design considerations for implementing bandpass filters: A) the passband should be much less than the center frequency of the filter. This condition is most stringent for stage n, because the size of the passband increases with k*. For stage n condition A) is equivalent to requiring that the range of $f_n$ be

* As can be seen from (5), for design options a and b the greatest contribution to the passband is made by the range of $i_n$ and $i_1$, respectively.

much less than the center value of $f_n$. From (4) these values are $\Delta f(I_{max} - I_{min})$ and $f_o + 2^{-1}\Delta f(I_{max} + I_{min})$, respectively. Therefore, with some algebraic manipulation

$$\Delta f << f_o/[(i_{max} - I_{min}) - (I_{max} + I_{min})/2] \quad . \qquad (6)^*$$

---

* See Appendix for expressions of $(I_{max} \mp I_{min})$.

## IV. CONVERTER

Let the stages of the synthesizer operate at frequencies considerably lower than that of the output. Then the frequency converter following stage n in Fig. 1 must scale $f_n$ up to the desired output frequency f. In general this frequency conversion might involve both multiplication and translation as shown in Fig. 3. Although the specific form of the frequency converter depends on the necessary scaling factor and the physical devices used in the implementation, it is assumed that multiplication by powers-of-two can be realized conveniently. Note that the up-conversion is facilitated by omitting the frequency scaling unit of stage n when the division by $2^m$ design option is selected. With this change (4) becomes slightly modified

$$f_n = 2^m(f_o + I\Delta f) \tag{7a}$$

$$f_n = f_o + I\Delta f \quad . \tag{7b}$$

Regardless of the particular frequency translation selected in Fig. 3, the multiplication factor is completely determined by B (the required final spacing between the possible output frequencies), $\Delta f$, and the (m, n) pair. For fixed $f_o$ and $\Delta f$ the range of $f_n$ is $2^m\Delta f(I_{max} - I_{min})$ and $\Delta f(I_{max} - I_{min})$, respectively, from (7). The multiplication factor times the range of $f_n$ must equal the range of f which is $(N-1)B$. Thus defining $M = M_1 + M_2$ $(M_1, M_2 \geq 1)$

$$2^M = (N-1)B/2^m\Delta f(I_{max} - I_{min}) = NB/2^m\Delta f \tag{8a}$$

$$2^M = (N-1)B/\Delta f(I_{max} - I_{min}) = B/2^m\Delta f \quad . \tag{8b}$$

Note that the upper-bound restriction on $\Delta f$ in (6) implies a lower-bound restriction on M.

Once the final multiplication factor (M) has been determined, individual values for $M_1$ and $M_2$ can be selected (subject to the constraint $M_1 + M_2 = M$) along with $f_c$ and a particular mixing operation to achieve desirable values for f. For simplicity let the mixing operation of Fig. 3 be $2^{M_1} f_n \pm f_c$. Assuming that the upper sideband is passed to facilitate the final frequency up-conversion, condition A) is automatically satisfied by (6) regardless of the values assumed by $f_c$ and $M_1$. However, the following additional condition related to bandpass filter design imposes a certain restriction on $f_c$: B) the separation between two sidebands should be sufficiently large so that only one sideband is passed (this separation must only be positive for an ideal bandpass filter, but let the minimum separation be arbitrarily equated to the width of the passband). For the selected mixing operation condition B) requires that

$$f_c \geq 2^{M_1+m} \Delta f(I_{max} - I_{min}) \approx 2^{M_1+m} \Delta f \tag{9a}$$

$$f_c \geq 2^{M_1} \Delta f(I_{max} - I_{min}) \approx 2^{M_1+m} N\Delta f \quad , \tag{9b}$$

where the approximations are valid for large N.

The output frequency of the synthesizer can be written as

$$f = 2^{M_2} f_c + 2^{M+m}(f_o + I\Delta f) \tag{10a}$$

$$f = 2^{M_2} f_c + 2^{M}(f_o + I\Delta f) \quad , \tag{10b}$$

The center output frequency becomes

$$\bar{f} = 2^{M} 2 f_c + 2^{M+m}(f_o + 2^{-1}\Delta f[I_{max} + I_{min}]) \qquad (11a)^*$$

$$\bar{f} = 2^{M} 2 f_c + 2^{M}(f_o + 2^{-1}\Delta f[I_{max} + I_{min}]) \qquad (11b)^*$$

When the particular output frequency produced by the synthesizer is mixed with the corresponding received carrier frequency ($f_r$), a fixed IF frequency ($f_{IF}$) always results according to the formula

$$f = f_r \pm f_{IF} \quad , \qquad (12)$$

where $0 < f_{IF} < f_r$. The choice of sign in (12) depends on whether or not $f_r$ is subtracted from f or vice-versa in the mixing operation, respectively. Let the bandwidth (B) of the IF amplifier be centered about $f_{IF}$, and let

$$W = NB \qquad (13)$$

represent the total bandwidth related to the received signal modulated within a bandwidth B about one of N possible carrier frequencies. The received frequency spectrum is depicted in Fig. 4.

---

* See Appendix for expressions of $(I_{max} \mp I_{min})$.

## V. GENERATOR

For convenience of implementation let $f_o$ and $\Delta f$ be generated from the frequency standard ($f_s \leq f_o$) by power-of-two frequency scaling

$$f_o = 2^{d_1} f_s \quad d_1 \geq 0 \tag{14}$$

$$\Delta f = 2^{-d_2} f_s \quad d_2 \geq 0 \quad . \tag{15}$$

Note from the ratio $f_o/\Delta f = 2^{d_1+d_2} = 2^d$, that d must be sufficiently large to satisfy condition (6). By (3), let $f_g$ be generated by mixing $f_o$ and $f_o$ scaled by a factor $2^m$. The $2^m$ frequencies $f_g + i_k \Delta f$ can be generated by mixing $f_g$ with harmonics of $\Delta f$. The block diagram of the frequency generator is indicated by Fig. 5. For design option a, an additional frequency scaler ($\times 2^m$) is necessary to produce $f_g$. For option b, however, $f_o/2^m$ may be taken directly from an accessible node between $\Delta f$ and $f_o$. For both design options, the frequencies $2\Delta f$, $4\Delta f, \ldots, 2^{m-1}\Delta f$ may be taken from accessible nodes between $\Delta f$ and $f_o$. Rather than specify the means of generating $f_c$, let this part of the design remain flexible. However, depending on the particular frequency synthesizer design, it is desirable that $f_c$ (if used at all) be generated without adding significantly to the frequency generator operations already defined.

## VI. SWITCHING NETWORK

A block diagram of frequency switching network k is shown in Fig. 6. The contents $(b_1, b_2, \ldots, b_m)$ of the m-cell binary storage register determines which of the $2^m$ frequencies is gated to stage k. The m inputs designated $c_{i_k}$ to AND gate $i_k$ represent a unique combination of the 2m outputs of the storage register – one from each cell. Note that both the true and complemented logical values of the bit stored in each cell are available. Since the entire frequency synthesizer includes n copies of switching network k, the total number of storage cells and AND gates is mn and $n2^m$, respectively. Although the number of storage cells for a given family of synthesizers is invariant (from (2)), the number of AND gates increases rapidly with m for $m \geq 3$ as can be verified using Table 1.

## ACKNOWLEDGEMENT

Thanks are due Ben Hutchinson of Group 62 for sharing his design of the frequency synthesizer used in LET and Walter Morrow of Division 6 for suggesting the further exploration of synthesizers based on frequency multiplication. The guidance of Barney Reiffen is gratefully acknowledged.

## APPENDIX

Precise and approximate (for large N) expressions for $I_{max} - I_{min}$ and $I_{max} + I_{min}$ for each of the four design options can be derived from (1) and (5) by utilizing the fact that

$$\sum_{j=1}^{n} (\pm x)^j = (\pm x)\,[(\pm x)^n - 1]/(\pm x - 1) \quad . \qquad \text{(A-1)}$$

Option a-1: Division and Upper Sideband

$$I_{max} = 2^{m-1}[2^{-m} + 2^{-2m} + \cdots + 2^{-nm}]$$

$$-I_{min} = (2^{m-1} - 1)\,[2^{-m} + 2^{-2m} + \cdots + 2^{-nm}]$$

$$I_{max} - I_{min} = (2^m - 1)\,(2^{-m})\,(2^{-nm} - 1)/(2^{-m} - 1)$$

$$= 1 - 1/N \approx 1 \qquad \text{(A-2)}$$

$$I_{max} + I_{min} = 2^{-m}(2^{-nm} - 1)/(2^{-m} - 1)$$

$$= (1 - 1/N)/(2^m - 1) \approx (2^m - 1)^{-1} \qquad \text{(A-3)}$$

Option a-2: Division and Lower Sideband

$$I_{max} = 2^{m-1}2^{-m} + (2^{m-1} - 1)2^{-2m} + \cdots + (2^{m-1} - \tbinom{0}{1})\,2^{-nm} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$-I_{min} = (2^{m-1} - 1)\,2^{-m} + 2^{m-1}2^{-2m} + \cdots + (2^{m-1} - \tbinom{1}{0})\,2^{-nm} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$I_{max} - I_{min} = (2^m - 1)\,[2^{-m} + 2^{-2m} + \cdots + 2^{-nm}]$$

$$= 1 - 1/N \approx 1 \qquad \text{(A-4)}$$

$$I_{max} + I_{min} = 2^{-m} - 2^{-2m} + \cdots \pm 2^{-nm} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$= -(-2^{-m})\,[(-2^{-m})^n - 1]/(-2^{-m} - 1)$$

$$= (1 \pm 1/N)/(2^m + 1) \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$\approx (2^m + 1)^{-1} \qquad \text{(A-5)}$$

Option b-1: Multiplication and $f_{k-1}$ Subtracted

$$I_{max} = 2^{m-1}2^m + (2^{m-1} - 1)\,2^{2m} + \cdots + (2^{m-1} - \tbinom{0}{1})\,2^{nm} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$-I_{min} = (2^{m-1} - 1)\,2^m + 2^{m-1}2^{2m} + \cdots + (2^{m-1} - \tbinom{1}{0})\,2^{nm} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$I_{max} - I_{min} = (2^m - 1)\,[2^m + 2^{2m} + \cdots + 2^{nm}]$$

$$= (2^m - 1)\,2^m(2^{nm} - 1)/(2^m - 1)$$

$$= 2^m(N - 1) \approx N2^m \qquad \text{(A-6)}$$

$$I_{max} + I_{min} = 2^m - 2^{2m} + \cdots \pm 2^{nm} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$= -(-2^m)\,[(-2^m)^n - 1]/(-2^m - 1)$$

$$= (1 \pm N)/(1 + 2^{-m}) \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix}$$

$$\approx \pm N(1 + 2^{-m})^{-1} \qquad \begin{matrix} n \text{ odd} \\ n \text{ even} \end{matrix} \qquad \text{(A-7)}$$

Option b-2: Multiplication and $f_g + i_k \Delta f$ Subtracted

$$I_{max} = (2^{m-1} - 1)\,[2^m + 2^{2m} + \cdots + 2^{nm}]$$

$$-I_{min} = 2^{m-1}[2^m + 2^{2m} + \cdots + 2^{mn}] \qquad \text{(A-8)}$$

$$I_{max} - I_{min} = (2^m - 1)\,[2^m + 2^{2m} + \cdots + 2^{mn}]$$

$$= 2^m(N - 1) \approx N2^m$$

$$I_{max} + I_{min} = -\,[2^m + 2^{2m} + \cdots + 2^{nm}]$$

$$= -\,2^m(2^{nm} - 1)/(2^m - 1)$$

$$= (1 - N)/(1 - 2^{-m})$$

$$\approx -\,N(1 - 2^{-m})^{-1} \qquad \text{(A-9)}$$

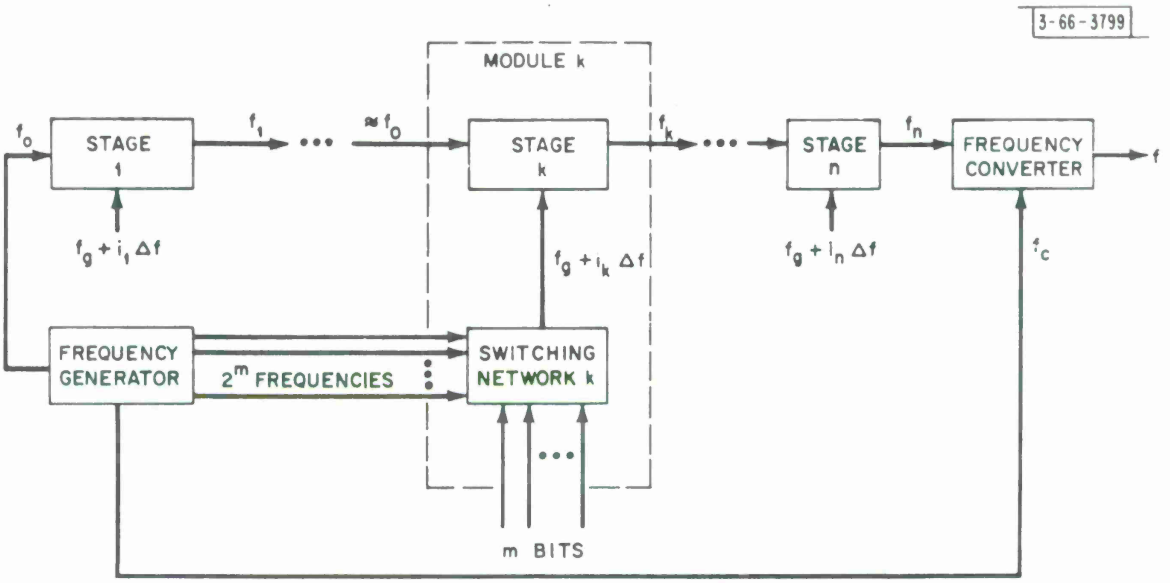



Fig. 1 Modular Composition of Frequency Synthesizer.

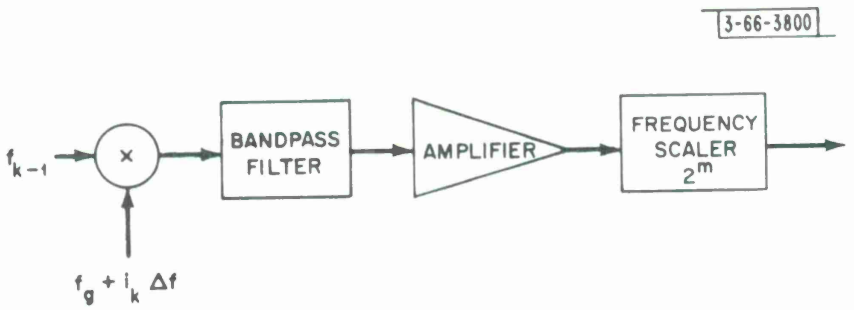



Fig. 2 Block Diagram of Stage k.

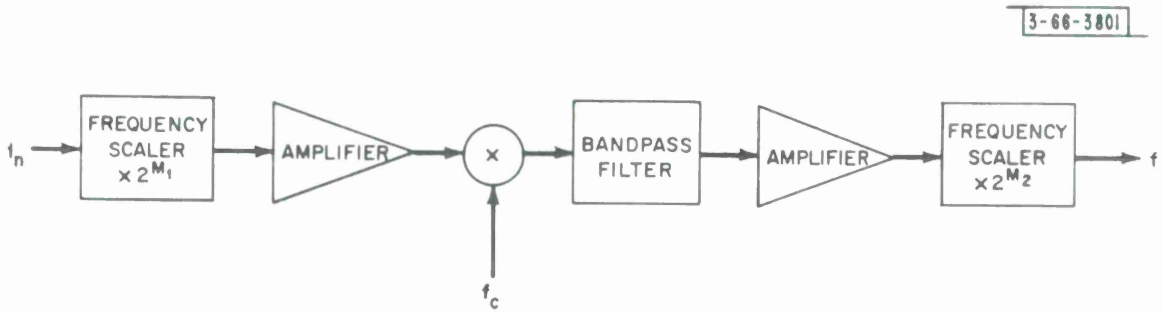



Fig. 3 Block Diagram of Frequency Converter.

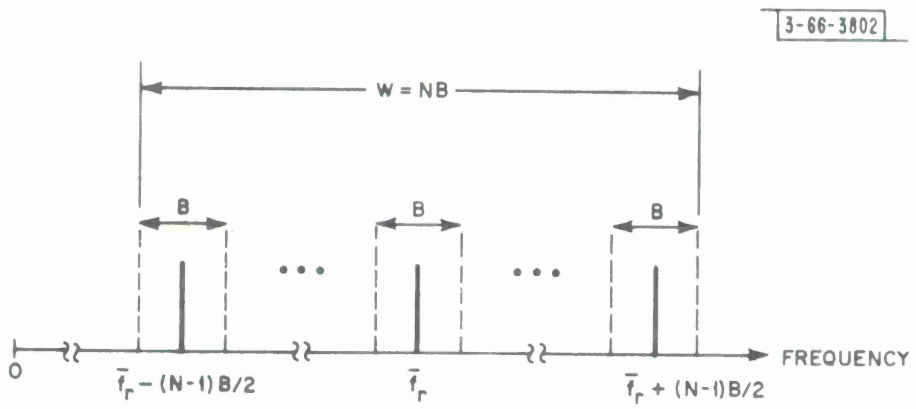



Fig. 4 Received Frequency Spectrum.

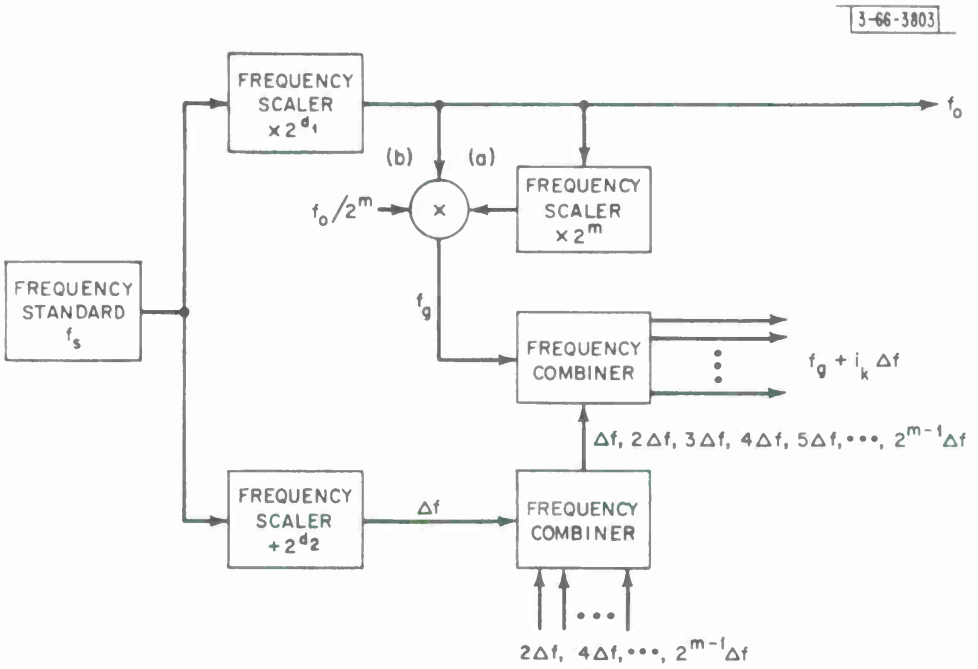



Fig. 5 Block Diagram of Frequency Generator.

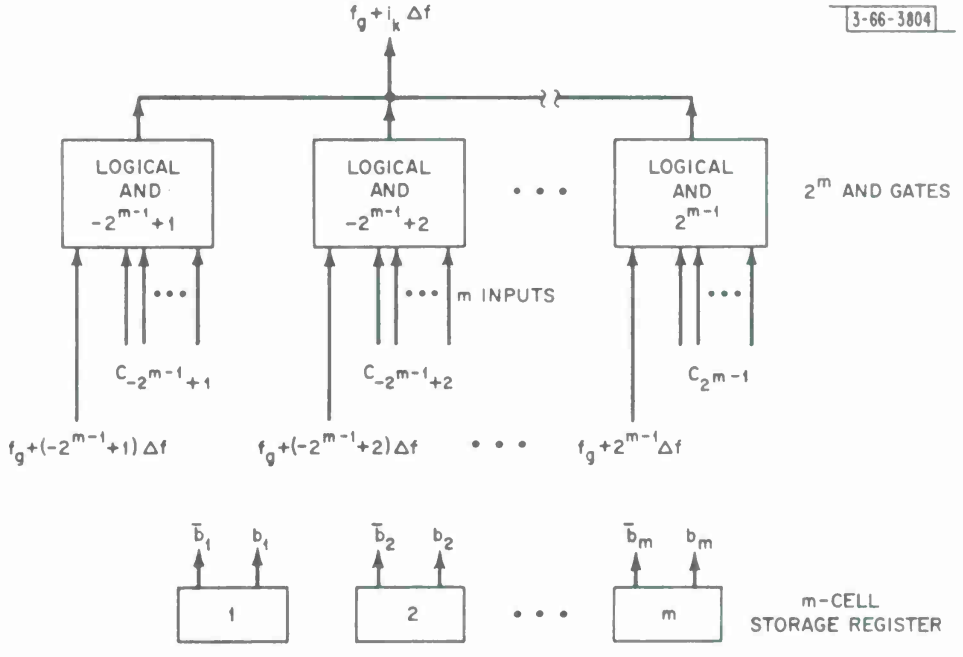



Fig. 6 Block Diagram of Frequency Switching Network k.

DISTRIBUTION LIST

Division 6

G. P. Dinneen
W. E. Morrow, Jr.

Group 62

P. R. Drouilhet
B. H. Hutchinson, Jr.
I. L. Lebow

Group 63

J. B. Connolly
A. I. Grayzel
W. G. Schmidt
H. Sherman
L. J. Travis, Jr.

Group 66

J. U. Beusch
B. Reiffen
B. E. White
Group 66 File (10)

## DOCUMENT CONTROL DATA – R&D

*(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)*

| | |
|---|---|
| 1. ORIGINATING ACTIVITY *(Corporate author)*<br>Lincoln Laboratory, M.I.T. | 2a. REPORT SECURITY CLASSIFICATION<br>Unclassified<br>2b. GROUP<br>None |

3. REPORT TITLE

Conceptual Description of a Family of Frequency Synthesizers

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

Technical Note

5. AUTHOR(S) *(Last name, first name, initial)*

White, Brian E.

| | | |
|---|---|---|
| 6. REPORT DATE<br>8 September 1965 | 7a. TOTAL NO. OF PAGES<br>22 | 7b. NO. OF REFS<br>None |
| 8a. CONTRACT OR GRANT NO.<br>AF 19(628)-5167<br>b. PROJECT NO.<br>None<br>c.<br>d. | 9a. ORIGINATOR'S REPORT NUMBER(S)<br>TN-1965-43<br>9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*<br>ESD-TDR-65-421 | |

10. AVAILABILITY/LIMITATION NOTICES

None

| | |
|---|---|
| 11. SUPPLEMENTARY NOTES<br>None | 12. SPONSORING MILITARY ACTIVITY<br>Air Force Systems Command, USAF |

13. ABSTRACT

A family of frequency synthesizers is described. Each member of the family generates one of many equally-spaced frequencies by utilizing identical modules, the number of which is related to the number of possible frequencies. For any design in the family which uses frequency division in the modules, there exists a dual design which utilizes frequency multiplication. Block diagrams and formulas are included which may be useful in designing frequency synthesizers for communication system applications.

14. KEY WORDS

frequency synthesizers
modulators
frequency converters
frequency generators