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Technical Report

346

B. G. Kuhn

The Orthomatch Data Transmission System

18 February 1964

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts



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THE ORTHOMATCH DATA TRANSMISSION SYSTEM

B. G. KUHN

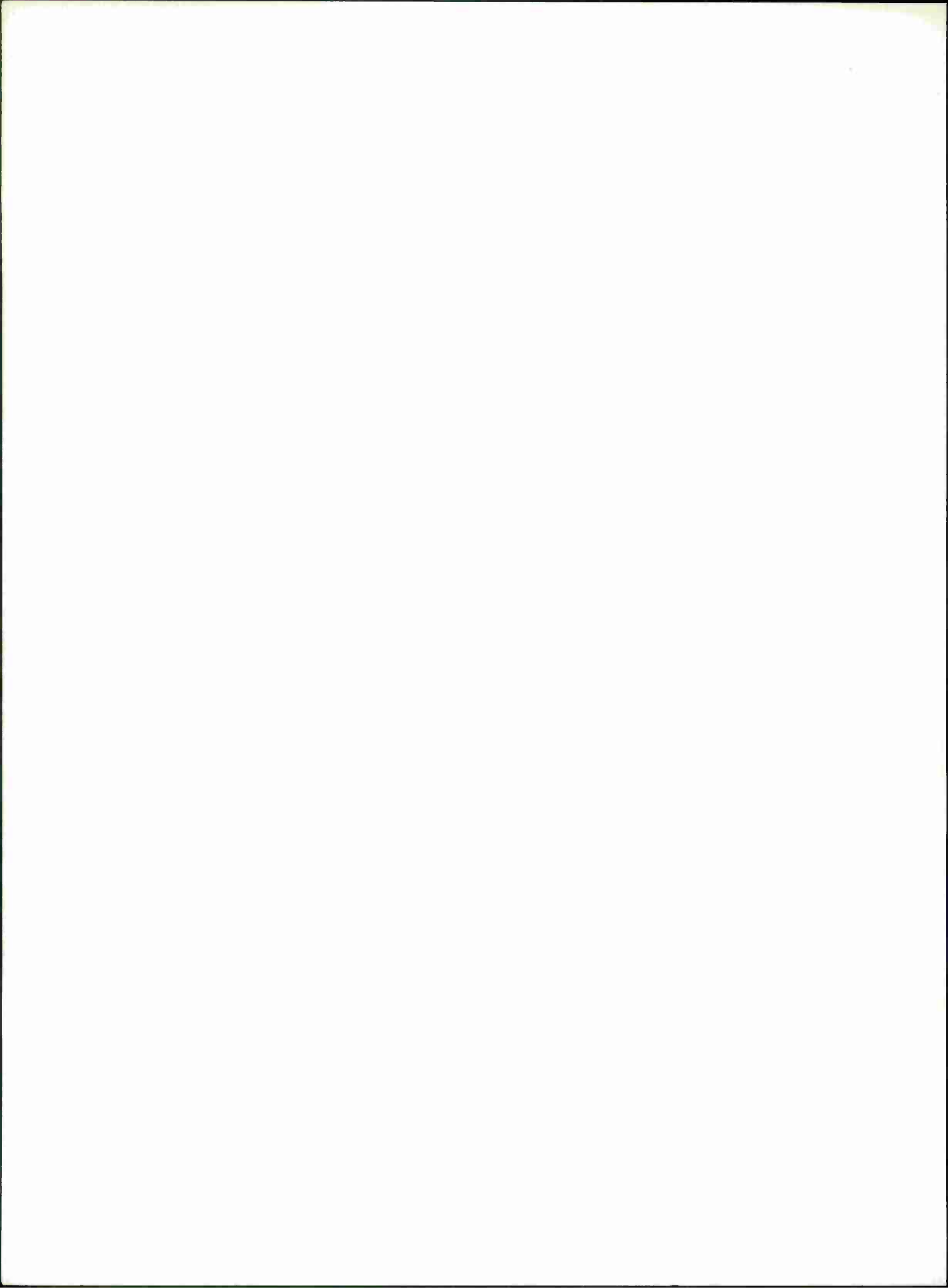
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TECHNICAL REPORT 346

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MASSACHUSETTS



ABSTRACT

Orthomatch is a high-performance data transmission or telemetry system which uses envelope-orthogonal signals in the transmitter and matched-filter detectors in the receiver. Because of the parallel coding and optimum detection techniques of Orthomatch, its calculated performance equals or betters the calculated performance of other available telemetry systems. It is within 10.2 db of Shannon's ideal system.

A practical Orthomatch system, operating with 16 levels of amplitude resolution and a 40-kcps word rate (160-kcps bit rate), has been assembled in field-prototype form and tested with transmitter and receiver components at 2.22 Gcps. Signal-in-noise performance of this practical system was found to be within 1.5 db of calculated performance.

High performance at low signal levels and other advantages of Orthomatch make it attractive for use at high data rates in space-to-ground or other transmission links where transmitter power is at a premium.

Accepted for the Air Force
Franklin C. Hudson, Deputy Chief
Air Force Lincoln Laboratory Office

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ACKNOWLEDGMENT

Large contributions to the Orthomatch work were made by people other than the author of this report.

W.B. Smith of Lincoln Laboratory suggested and outlined the Orthomatch system originally and acted as a consultant and guide on theory and performance throughout the work. K.H. Morey, formerly of Lincoln Laboratory, designed and built many of the circuits which were used. J.F. Tolpa, Lincoln Laboratory technician, did continuous good work in construction and testing of the equipment.

THE ORTHOMATCH DATA TRANSMISSION SYSTEM

I. INTRODUCTION

A. General System Description

Orthomatch is the mnemonic name given to the data transmission or telemetry system which uses envelope-orthogonal signals in the transmitter and a set of matched filters in the receiver. The orthogonal signals are a set of discrete transmitter frequencies, each of which represents an amplitude increment from an analog source and is pulsed on during the sampling interval. Many sampling intervals are arranged in series to allow time-division multiplexing of many data sources. The fineness of amplitude resolution corresponds to the number of transmitter signals provided; for example, four discrete frequencies are required for four amplitude levels. Each of the filters in the receiver is matched to one of the transmitter signals; the filter bank is sampled at the ends of the transmitted pulse intervals to select the correct signal and thus determine which level was sent. An outline diagram in Fig. 1 shows the general configuration of the Orthomatch system. The arrangement of discrete transmitter signals and a corresponding set of filters constitutes a form of parallel digital coding. Matched filters are optimum detectors of signals in the presence of white, Gaussian noise. Because of the coding and the use of matched filters, the Orthomatch system operates at signal-to-noise ratios lower than other telemetry systems such as PAM/FM, PCM/FM, and PCM/biphase.*

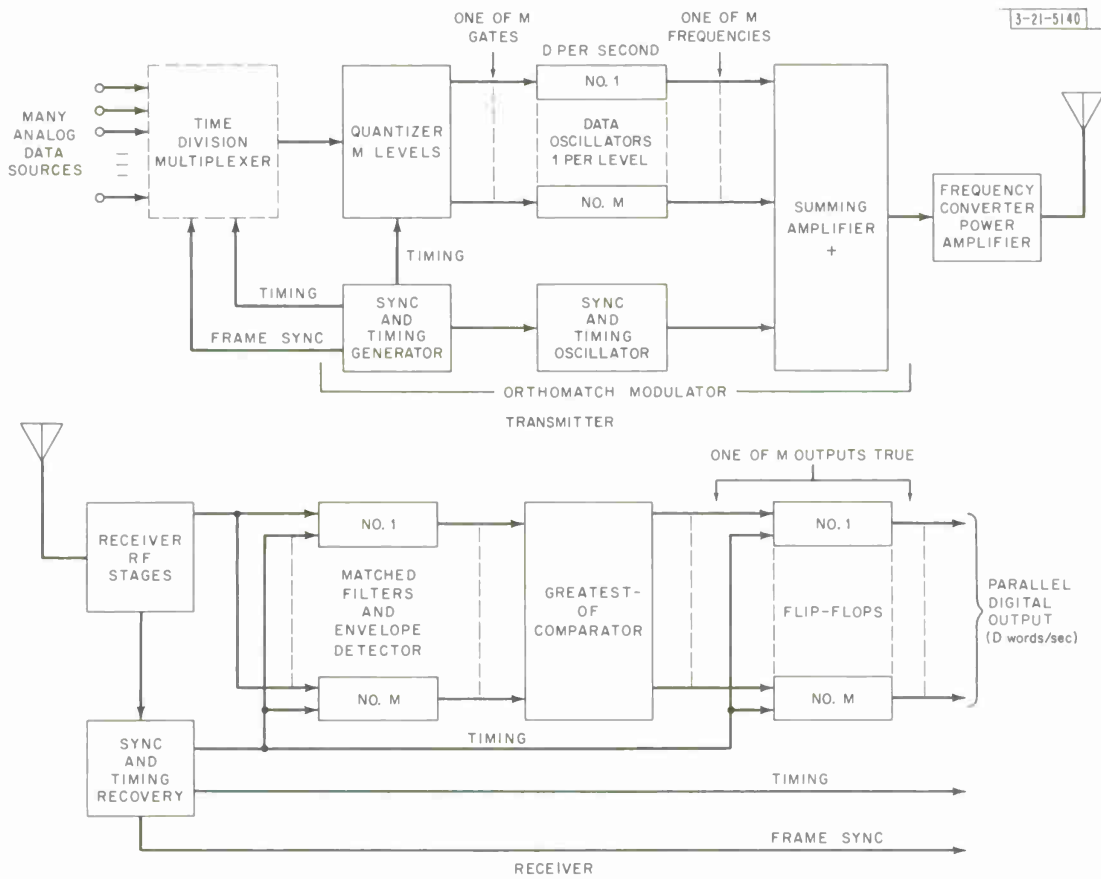
B. Practical Orthomatch System

A practical Orthomatch system has been assembled in field-prototype form. Testing this system has proved that practical performance is very close to theoretical performance. The particular equipment which was built operates at a 40-kcps sampling rate or symbol rate with 16 levels of amplitude resolution, corresponding to an equivalent bit rate of 160 kcps. The frame time is 6.4 msec, and 242 time slots of 25 μ sec each are available for data channels. The Orthomatch method and the equipment components are adaptable to higher and lower symbol rates, amplitude levels, and frame lengths.

C. Stages of Development

The Orthomatch system was suggested by W. B. Smith in 1961 for application in satellite-to-ground data transmission. A small Lincoln Laboratory effort on the system development has continued since the fall of 1961 in the following stages:

* PAM is pulse amplitude modulation, PCM is pulse code modulation, FM is frequency modulation, and biphase is 0° to 180° phase-shift modulation.



NOTE: Bit rate = $D \log_2 M$ bits/sec

M = number of quantized levels

D = symbols or words/sec

Fig. 1. Orthomatch system.

A laboratory model of the equipment was assembled in 1962. This early equipment demonstrated feasibility of the method of signal generation and data recovery, and signal-vs-noise performance was found to be very close to theoretical performance. The equipment was operated at relatively low radio frequency (RF) and it used a synchronization method which required transmission of a synchronizing carrier frequency simultaneously with a data frequency. The work was reported in a Lincoln Laboratory classified document in October 1962 and in Transactions of the IEEE in September 1963.¹ The Orthomatch system was not applied in the satellite for which it was suggested, but it was considered worthwhile to continue development of the system for operation in the 2.2- to 2.3-Gcps telemetry band and to obtain improved models of the transmitter and receiver.

In 1963, the transmitter modulator and the receiver were redesigned and re-built. The modulator was packaged in miniaturized form with consideration given to the likely operating conditions of a space satellite. Transmission of synchronization signals was changed to a serial method which produces synchronizing carrier bursts while data signals are gated off. The purpose of this change was to avoid intermodulation problems in nonlinear transmitter amplifiers and multipliers due to the simultaneous presence of two frequencies.

Late in 1963, satisfactory operation was demonstrated at appropriate power levels in the 2.2- to 2.3-Gcps telemetry band.

This report is intended as a review of the Orthomatch system concepts and of the equipment design and performance.

II. BASIC CHARACTERISTICS AND REQUIREMENTS

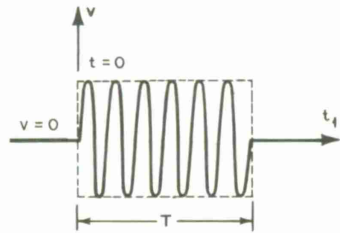
A. System Conception

The aim in suggesting the system originally was to provide a telemetry system that would require substantially less transmitter power than other available systems, while avoiding undue complexity in the transmitter. Recognition of the advantages of data quantization² before transmission indicated that a set of discrete transmitter signals corresponding to quantized input signals should be used. It was reasonable to assume that system noise would be mainly of receiver front-end origin and that it could be represented as white, additive, and Gaussian. Since it has been shown³ that an optimum receiver for the detection of discrete signals in the presence of white, additive, Gaussian noise consists of matched filters followed by envelope detectors, samplers, and a "greatest-of" decision circuit, this type of receiver was chosen. The set of transmitter signals should minimize the probability of error in the receiver's selection of the correct signal. A set of "envelope-orthogonal" signals, made up of rectangular bursts of sine waves³ in which the sine-wave frequencies are spaced by integral multiples of $1/T$ cps (where T is the burst duration), was chosen. In the absence of phase information, such a set of signals, with zero cross correlation at sample time, is considered to be optimum^{3,4} for use with a matched-filter receiver, although it apparently has not been proved. A set of receiver filters, also spaced by $1/T$ cps and each "matched" to its corresponding transmitter waveform, was expected to be realized without difficulty. The envelope-orthogonal characteristic of such a set of signals and matched filters causes the output of all the matched filters, except the one containing the signal, to be zero at sample time, thus minimizing the probability of error.

B. Orthogonal Signals

The basic transmitter signal is a pulsed sinusoid of T seconds in duration, as shown in Fig. 2(a). The frequency spectrum of this signal has the $\sin x/x$ form shown in Fig. 2(b), with a maximum at the carrier frequency f_0 and nulls at frequencies spaced integral multiples of

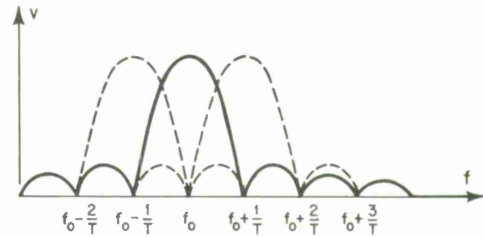
PULSED SINE WAVE, FREQUENCY f_0 , WITH RECTANGULAR ENVELOPE



(a) Time function

$$V(t) = \sin(2\pi f_0 t) \quad , \quad 0 < t < T$$

$$= 0 \text{ elsewhere} \quad .$$

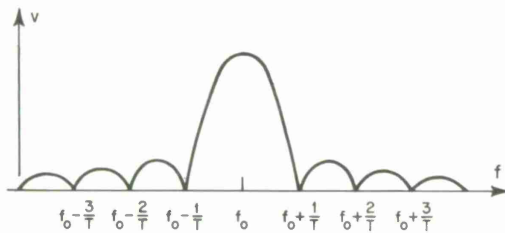


(b) Frequency spectrum (rectified and filtered)

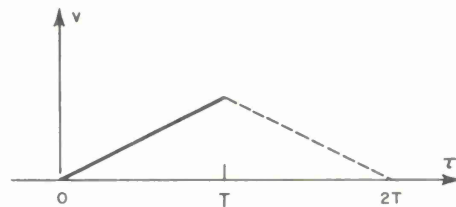
$$V(f) = K \frac{\sin(\pi T \Delta f)}{\pi T \Delta f}$$

$$\Delta f = f - f_0 \quad .$$

MATCHED-FILTER RESPONSE TO PULSED SINE-WAVE SIGNAL



(c) Frequency response at sample time (rectified and filtered) = Fourier transform of impulse response = $K_1 [\sin(\pi T \Delta f) / \pi T \Delta f]$ where $\Delta f = f - f_0$.



(d) Time response = autocorrelation function of input signal (after rectification and filtering).

Fig. 2. Orthogonal-signal and matched-filter characteristics.

$1/T$ cps from the carrier frequency. A separate carrier frequency is required for each of the amplitude levels which are to be represented. If the additional carrier frequencies are placed $1/T$, $2/T$, $3/T$ cps distant from f_o , the whole set of frequencies will have the envelope-orthogonal characteristic. The spectra of two additional pulsed frequencies of a set are shown by the dashed lines in Fig. 2(b).

C. Matched Filters

In order for a filter to be "matched" to an input signal, its impulse response must be the time reverse of the signal.³ The time response of the matched filter is then the autocorrelation function of the input signal. The time reverse of the pulsed sine-wave signal is the same as the signal itself in the phase-incoherent case which applies here. Thus, the frequency response of a matched filter, as shown in Fig. 2(c), is the same as the spectrum of a transmitter signal. The time response is the isosceles triangle shown in Fig. 2(d).

The set of matched filters has been realized by building high-Q resonant circuits, each tuned to a frequency that corresponds to one of the signal frequencies. Short pulses, spaced T seconds apart, are introduced to dump or squelch the resonant circuit energy at the ends of pulse intervals. The waveforms of Fig. 3 depict actual matched-filter responses. The triangular autocorrelation function is clearly visible in the RF response and detected output; this apparently faithful autocorrelation function indicates that the filters are operating as matched filters. The squelch pulses are timed to bracket the RF input signals accurately, and the filter outputs are sampled at the peak of the autocorrelation function, just before squelching. The falling half of the autocorrelation function beyond the peak is rejected. The response of adjacent filters is zero at sample time, corresponding to nulls in the frequency response shown in Fig. 2(d). The decision as to which filter received the signal is made by a "greatest-of" or auction circuit which sets a flip-flop corresponding to the matched filter with the greatest output.

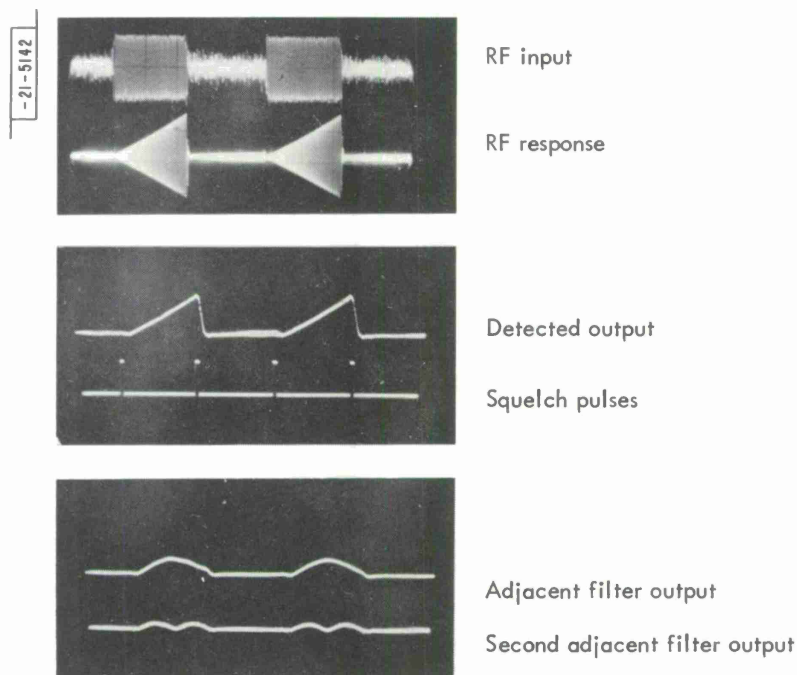


Fig. 3. Matched-filter waveforms.

D. Timing and Synchronization Requirement

The sampling and squelch pulses for the matched filters must be timed or phased accurately to maximize the response (at sample time) of the filter containing the signal, and to minimize the response of all the other filters in the set. Timing information is not recoverable from matched filters of the type used, so an auxiliary means of transmitting and recovering timing signals was needed. Digital data transmission systems of the serial type such as PCM generally require accurate bit timing; in the Orthomatch system, it is symbol or word timing that is required. In common with other time-division multiplex systems, Orthomatch also requires frame synchronization for identifying the data slots. The method of transmitting and recovering timing and synchronization for Orthomatch is covered in Secs. IV-B-7 and IV-I-4.

III. COMPARATIVE PERFORMANCE OF SYSTEMS

A. Shannon Formula

The channel capacity formula developed by C. E. Shannon^{5,2} relates data rate, bandwidth, and signal-to-noise ratio in an ideal communications system and establishes performance limits which may be approached, but not exceeded, by practical systems. The formula is

$$C = W \log_2 \left(1 + \frac{S}{N} \right)$$

where C is the number of bits per second which may be transmitted with arbitrarily small probability of error, W is the system bandwidth in cycles per second, S is the average signal power, and N is the white noise power.

The parameter E/N_o , the signal energy divided by the noise power per cycle per second, is a basic, normalized parameter which is very useful in considering and comparing communications systems. It is related to the signal-to-noise ratio, bandwidth, and data rate as

$$\frac{E}{N_o} = \frac{STW}{N} = \frac{SW}{NC}$$

where T is the signal duration time or the time allotted to send one bit.

The Shannon formula can be manipulated as shown in Appendix A to yield minimum $E/N_o = 0.693$. This minimum E/N_o is obtained by allowing the bandwidth to increase without limit; in addition, the Shannon formula implies long serial coding sequences. Although it is clear that practical systems will be inhibited by practical limits on bandwidth usage and on length of coding sequences, the Shannon E/N_o minimum is a useful yardstick by which to gauge the performance of practical systems. In the following paragraphs, some practical systems, including Orthomatch, will be compared with each other and with the ideal system.

B. Orthomatch Theoretical Performance

Reiger⁶ and Ward⁷ have calculated the probabilities of error vs E/N_o for systems like Orthomatch in which one of M incoherent signals with noise added is selected by means of matched filters, envelope detectors, and a greatest-of or maximum-likelihood circuit. Reiger's and Ward's calculations agree, and they have been used to obtain calculated or theoretical performance data for the Orthomatch system. Calculated curves appear later in this report.

C. Incoherent PCM

The envelope-orthogonal signals and matched filters of Orthomatch, when reduced to an appropriate set of two, can be used to carry binary PCM data. This modulation and demodulation method will be assumed for a comparison of the two systems on the basis of signal power required for the same symbol or word transmission rate and error rate. The relative power required is affected by these factors:

In the Orthomatch system, one of M quantized levels is transmitted by one of M symbols or pulses of T seconds in duration, where $1/T$ is the symbol or word rate. In binary PCM, one of M levels is transmitted by a serial sequence of n pulses or bits where $2^n = M$. For the same word rate and 100-percent duty ratio in both systems, the PCM pulses are of T/n second duration. Since the PCM pulses or bits should have the same energy as the Orthomatch symbols for the same detectability, the PCM signal will require more power (6 db more than Orthomatch in a 16-level system). This is caused by time division in PCM serial transmission alone.

To obtain a given low probability of word error in PCM, assumed to be the same as the probability of Orthomatch symbol error, the probability of PCM bit error must be approximately $1/n$ times the word error probability. From Ward's⁷ curves, at a word error probability of 10^{-4} and assuming 16 levels, this factor shows a comparative loss of 0.7 db for PCM.

The PCM detector must decide only which of two signals was sent, whereas a 16-level Orthomatch detector must select one of 16 signals. By use of Ward's curves at a 10^{-4} word error rate and interpolating, this factor represents a comparative loss of 1.1 db for Orthomatch.

To summarize, 16-level PCM requires $(6.0 + 0.7 - 1.1)$ db = 5.6 db more power than 16-level Orthomatch for a 10^{-4} word error rate and the same modulation and demodulation method. For 8 levels, the Orthomatch advantage is 4.4 db, and for 32 levels, the Orthomatch advantage is 6.2 db. The comparison is not sensitive to choice of error rate between 10^{-3} and 10^{-6} .

D. PCM/Biphase

Biphase (0° to 180° phase shift) modulation is another suitable vehicle for PCM (provided phase can be determined) and, assuming an optimum detector, biphase PCM will work with 3.7 db less power than the incoherent PCM discussed above. This is due to the -1 cross correlation (as compared with zero for the incoherent case) between the binary elements, and to the knowledge of phase. Therefore, the power advantage of Orthomatch over biphase PCM is theoretically 0.7, 1.9, and 2.5 db for 8, 16, and 32 levels, respectively.

E. PCM/FM

An FM system, in which the RF carrier is shifted abruptly between two frequencies, is commonly used for transmission of PCM data. This modulation method is similar to the incoherent PCM discussed in Sec. III-C, but in the PCM/FM system the frequencies are not orthogonally spaced, and a discriminator is used as a detector. Shaft⁸ has recently published calculated and measured error data for PCM/FM (discriminator detector) and compares it with results for other PCM systems, including the incoherent PCM and PCM/biphase (optimum binary system) already reviewed here. Shaft's results show that the PCM/FM system, which has been made optimum or near optimum with respect to frequency separation and receiver IF filtering, performs approximately 1 db better than incoherent PCM, and approximately 2.7 db poorer than PCM/biphase.

F. PAM/FM

In a PAM/FM system, amplitude variations of the signal source are transmitted by proportionate frequency deviations of the transmitted frequency; demodulation is accomplished by a limiter, discriminator, and video filter in the receiver. Comparison of a continuous or analog system like PAM/FM with a discrete or digital system like Orthomatch is somewhat awkward, but the following figures are indicative of relative capabilities. The Orthomatch system has 16 levels and a 40-kcps symbol rate; the PAM/FM system has the following characteristics:

PAM pulse rate	40 kcps
Duty ratio	50 percent
Deviation ratio, peak signal	3.5
Receiver IF bandwidth	500 kcps
Receiver video bandwidth	70 kcps.

For the PAM/FM system, noise fluctuations of six percent from peak signal were counted as errors, and in the Orthomatch system, false-level outputs were counted as errors. Calculations and measurements on the PAM/FM system agreed very well, and the power advantage of the Orthomatch system for the same error rate was 11.5 db.

G. Digilock System

Digilock⁹ is a coded, serial-binary, phase-modulated system in which symbols or words corresponding to amplitude levels are represented by orthogonal codes with good correlation properties. Tapped delay lines are used as matched-filter elements in the receiver, and word synchronization is accomplished by use of the autocorrelation functions of the codes. In a 32-level Digilock system, 16-bit codes are used; thus, the serial code is 11 bits longer than the 5-bit binary code of an ordinary PCM system. Sanders, the developer of Digilock, calculated and reported⁹ that this and other orthogonally coded systems require E/N_0 (bit) = 5 for 32 levels and E/N_0 (bit) = 6.7 for 16 levels at a bit-error probability of 10^{-6} . The measured performance of the 32-level Digilock system was within 2 db of the calculated performance. This places Digilock on a performance level that is approximately the same as that of Orthomatch.

H. Summary

In Appendix B, the comparative performance of the five digital communications systems reviewed above are summarized in tabular form. The power comparison is in the normalized E/N_0 form with bandwidth and data rate removed; however, for the purpose of tabulating estimates of bandwidths required, a bit rate of 160 kcps was assumed. On the basis of E/N_0 or power required, Orthomatch and Digilock are very nearly equal, but they are 10 db poorer than Shannon's ideal system. PCM/biphase, PCM/FM and PCM (incoherent) follow in that order. The power level equivalence of the Digilock serial system and the Orthomatch parallel system is interesting. From the standpoint of power level and bandwidth, both important features of practical systems, Orthomatch is superior to all the others. Orthomatch and Digilock are the same with respect to bandwidth increase with the number of levels, since Digilock doubles the code length when the number of levels is doubled, and Orthomatch doubles the number of discrete transmitter frequencies. However, the PCM systems without special coding increase their bandwidth only according to the logarithm of the number of levels.

IV. EQUIPMENT REVIEW

A. General

A review of the Orthomatch transmitter and receiver, referred to as the field-prototype equipment, will be given here to acquaint the reader with the design approach, operation, and performance of important Orthomatch components. Circuit details will be omitted unless they are of particular interest.

B. Orthomatch Modulator

1. Design Approach

The Orthomatch modulator consists of the quantizer, timing and sync-code generator, data oscillators, sync oscillator, and summing amplifier (Fig. 1). The modulator contains all the necessary Orthomatch components between the analog voltage source (usually a time-division multiplexer) and the RF conversion and output amplifier stages. The design approach for the modulator resulted from the following considerations:

All the components peculiar to Orthomatch are kept within the modulator so that common telemetry components such as time multiplexers and various transmitter amplifiers can be used with the Orthomatch system.

The building-block assembly of quantizer units and data oscillators allows the number of quantization levels to be changed readily.

The size, weight, and power consumption of the modulator were kept low, consistent with good design practice and available components, because of space-borne applications for the system. Silicon semiconductors were used throughout.

Fixed-frequency, crystal-controlled oscillators were chosen in preference to a single voltage-controlled oscillator or LC oscillators, for the sake of initial-setting accuracy, repeatability, and stability.

The oscillator frequencies are spaced in increments equal to one-ninth of the orthogonal output spacing to allow for a multiplication factor of nine in succeeding transmitter stages. An odd multiplication factor is required by the biphasic (0° to 180°) sync-frequency modulation, which would be destroyed by any even multiplication factor.

Transmission of data and sync frequencies are time-shared; only one frequency is turned on at any time. This was meant to avoid intermodulation problems which might be caused by co-existing frequencies in succeeding transmitter stages.

Oscillator frequencies around 7 Mcps are high enough to allow use of small L and C components but are low enough to keep down stray coupling between many oscillators operating side by side.

2. Quantizer

The Orthomatch system uses an analog-to-digital converter or quantizer that detects which one of M voltage increments in which the analog input lies, and provides a gate to the corresponding one of M oscillators. The quantizer's output circuitry has M leads to M oscillators; thus, the quantizer operates in parallel-digital fashion as compared with the serial-binary output mode (one lead) of a PCM analog-to-digital converter. The quantizer is clocked, so that the input voltage is sampled at clock time, and one gate is turned on and remains on during the whole word or symbol time between clock pulses. The Orthomatch quantizer uses a clocked comparator, flip-flop, and two AND diodes in each of M quantizer elements for M quantizing increments,

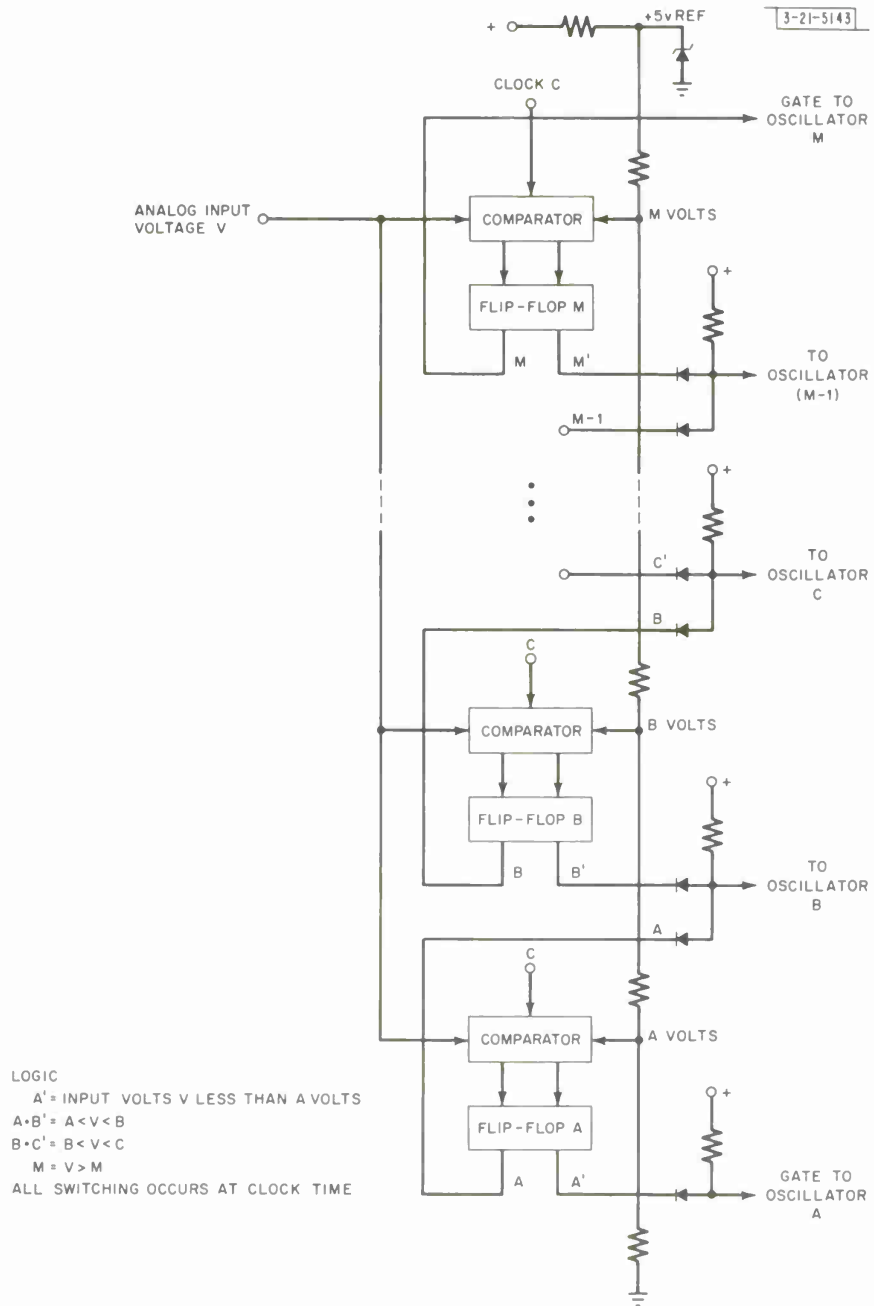


Fig. 4. Orthomatch quantizer connections and logic.

as may be seen in the block diagram of Fig. 4. The analog input or signal voltage is on a common bus to all comparators, and the comparison voltage levels for the comparators are obtained from a voltage-dividing string of resistors. The diode logic, which provides a gate to only one of the oscillators at a time, is shown in the diagram. Since an input voltage higher than M will always produce gate M out, the number of quantizer elements needed is one less than the number of quantizer increments.

Figure 5 is the circuit diagram of a quantizer element. Q_2-Q_3 and Q_4-Q_5 make up a two-stage differential amplifier which drives the flip-flop Q_6-Q_7 with high gain for fast switching. Q_1 is a clock buffer which drives current through Q_4 and Q_5 only at clock time, and thus the flip-flop may switch only at clock time.

The voltage-sensing accuracy of the quantizer depends upon the accuracy of the voltage reference, the accuracy of the resistive divider string, and upon the degree of match of the transistors in the comparator, particularly the input pair. It was found in the Fig. 5 quantizer that a total decision error of ± 25 mv, including decision offset and hysteresis, can readily be obtained at room temperature by selection of stock transistors. More accurate voltage sensing and good stability with temperature can be achieved by the use of single-cased matched pairs of transistors.

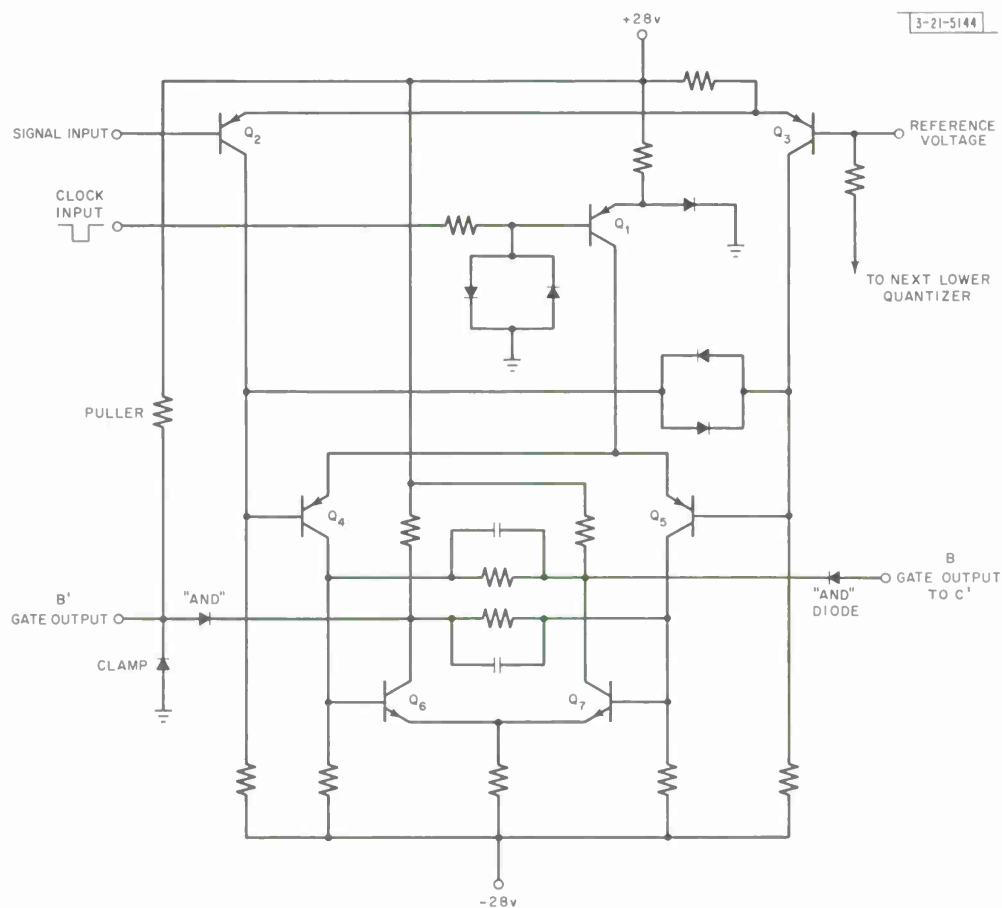


Fig. 5. Quantizer element.

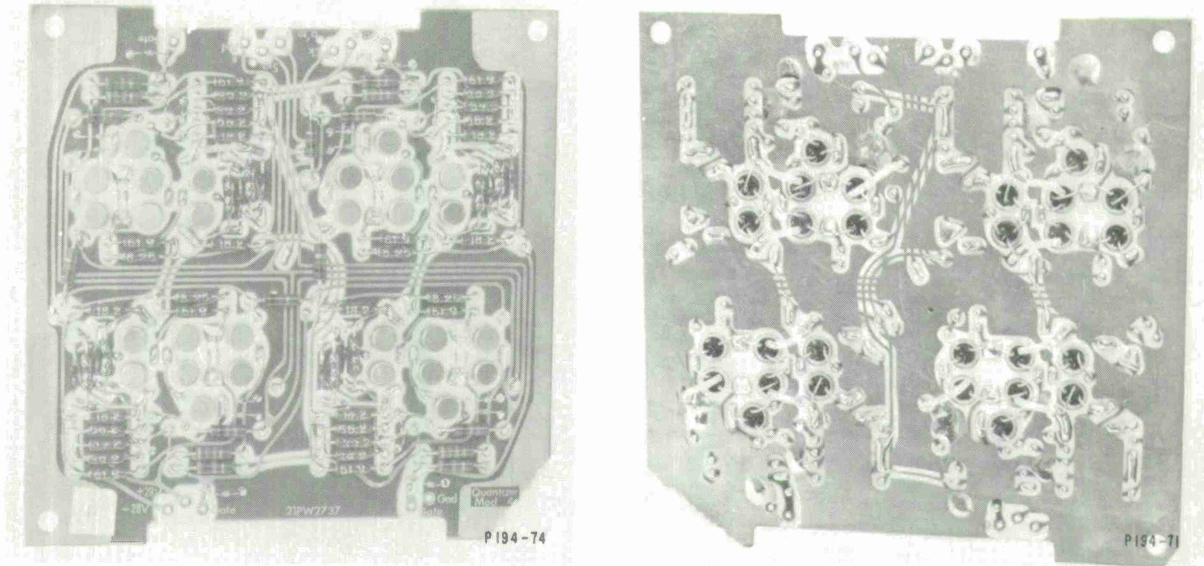


Fig. 6. Front and rear views of quantizer card.

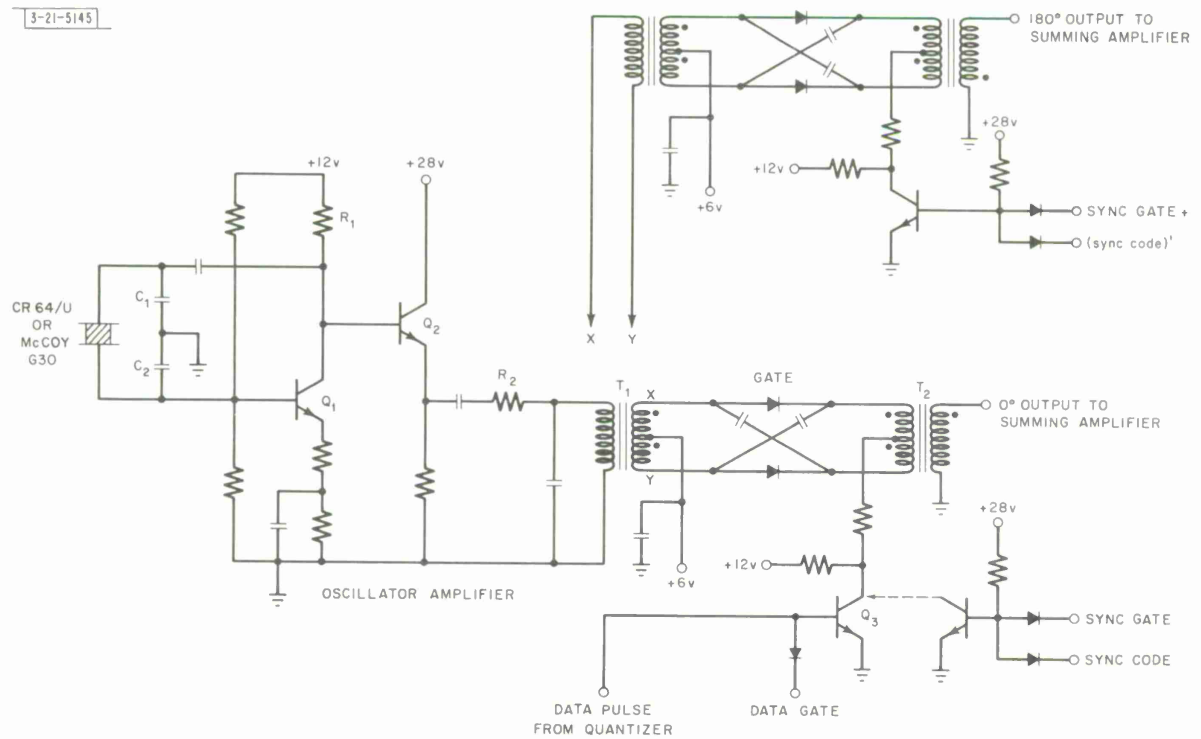


Fig. 7. Gated crystal oscillator.

Four quantizer elements are assembled on a $4\frac{1}{4}$ -inch-square printed-circuit card as shown in Fig. 6. Quantizer cards are interleaved with oscillator cards in the modulator assembly.

3. Gated Oscillators

Figure 7 is the circuit diagram of a gated oscillator. It consists of a continuously-running crystal oscillator, a buffer amplifier, and a transformer-coupled diode gate. The crystal oscillator uses a crystal near parallel resonance in a circuit similar to the Colpitts. The frequency is adjusted by changing the values of C_1 and C_2 ; the amplitude is adjusted coarsely by R_1 , and in fine steps by R_2 . Fixed capacitors and resistors were used, since they are smaller and more reliable than variable components. The gate uses a pair of low-capacitance diodes which are normally reverse biased but are turned on and conduct the RF signal from T_1 to T_2 when the switching transistor Q_3 is turned on. The criss-cross capacitors compensate for diode capacitance by antiphase voltages.

The solid-line connections of Q_3 apply to data oscillators. Two inputs are applied to Q_3 ; the positive data gate from the timing and code generator enables data output during its allotted time, and the positive data pulse from the quantizer turns on the selected oscillator. The data gate and quantizer output are in an AND circuit which has the puller resistor and two more diodes in the quantizer.

The sync oscillator requires two gated outputs, one each for 0° and 180° phase; the additional gate connections are shown in the top part of the diagram. The sync gate comes from the inverse side of the flip-flop which supplies the data gate, so that sync information is gated on while data output is turned off. The sync code and sync-code prime come from opposite sides of another flip-flop in the timing-and-code generator, so that during the sync gate the sync oscillator transmits with 0° or 180° phase, according to sync-code switching.

Four data oscillators are placed on one circuit board $4\frac{1}{4}$ inches square as shown in Fig. 8. The sync oscillator occupies a board of its own.

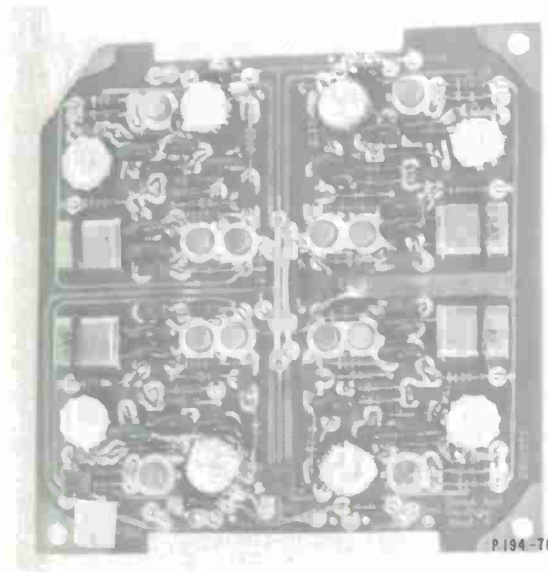


Fig. 8. Gated oscillator card.

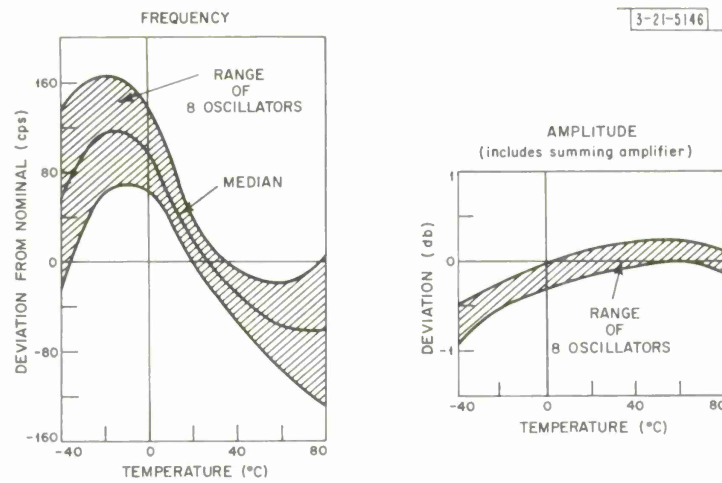
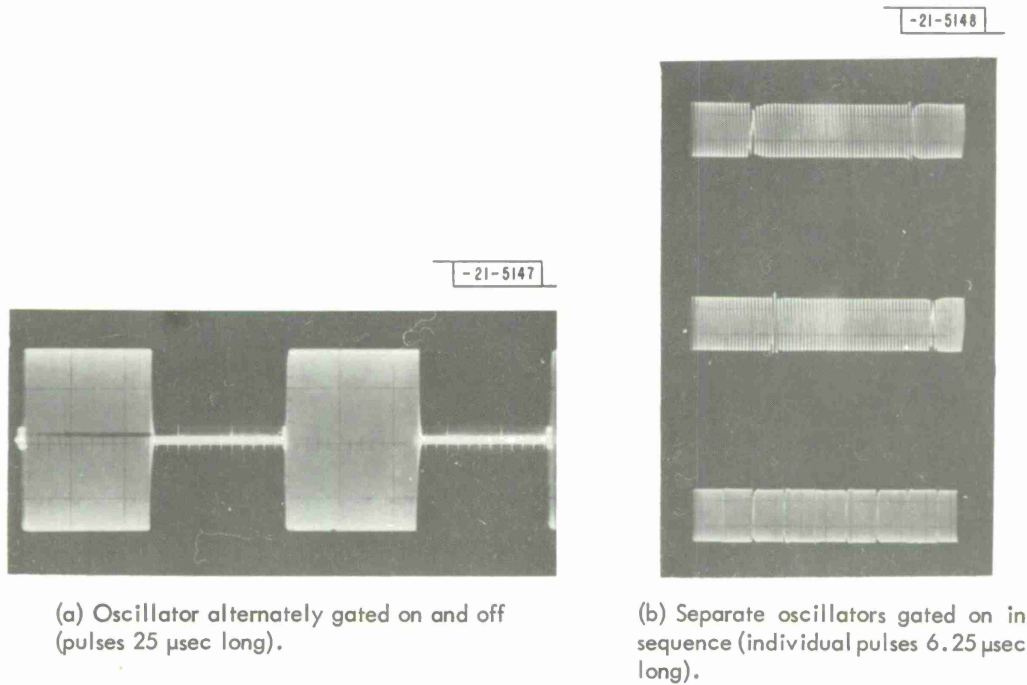


Fig. 9. Temperature stability for set of eight oscillators (McCoy G30 crystals near 7 Mcps).



(a) Oscillator alternately gated on and off (pulses 25 μ sec long).

(b) Separate oscillators gated on in sequence (individual pulses 6.25 μ sec long).

Fig. 10. Gated oscillator waveforms.

4. Oscillator Setup and Performance

During assembly of the 16-level Orthomatch modulator, all oscillator frequencies were adjusted within ± 25 cps of nominal crystal frequencies. Amplitudes of all 16 oscillators were equalized within ± 0.25 db. A fairly small tolerance on initial frequency setting is needed to maintain orthogonality of the set of frequencies despite the multiplication factor of nine, and to minimize the contribution of initial setting error to total differential deviation of the set of frequencies. A fairly small tolerance on amplitude adjustment of the set of oscillators is required so that all frequencies will be weighted equally in the greatest-of comparison in the receiver.

Figure 9 is a plot of amplitude and frequency deviation vs temperature for a set of eight oscillators. The frequency curve has the S-shape which is normal for AT-cut crystals. The spread in frequency deviations is 35 cps at 25°C , the initial setup temperature, and is a maximum of 160 cps at -40°C . The median curve shows the average drift of the set and is relatively unimportant, since it would be corrected by automatic frequency control (AFC) in the receiver. The worst deviation from orthogonality for any two frequencies in this set of eight would be $160 \times 9 = 1440$ cps. It is estimated that detection errors due to such an orthogonality error would be observable only at very low signal-to-noise ratios. In amplitude, the spread among oscillators is 0.25 db at 25°C and it increases to about 0.5 db at -40°C . The average power of the set of eight oscillators drops 0.65 db between $+25^{\circ}$ and -40°C .

Two types of oscillator crystals were used in oscillator assemblies: the military CR 64/U and McCoy G30. McCoy G30 crystals are of glass-encased, ruggedized design, and are similar to CR 73/U and CR 74/U crystals with respect to environmental and aging specifications. These crystals were found superior to CR 64/U crystals in uniformity of frequency and amplitude deviation with temperature. Test results with CR 64/U crystals varied over considerably wider ranges than those shown in Fig. 9. Use of G30 or equivalent crystals is recommended for Orthomatch oscillators.

Gated RF waveforms are shown in Fig. 10 for two pulsing rates, 40 and 160 kcps. The rise and fall times of the pulses are less than $0.5 \mu\text{sec}$. The notches in the $6.25\text{-}\mu\text{sec}$ pulse sequence show that the oscillators are usable at a 160-kcps switching rate with small loss due to switching time.

The quality of oscillator isolation and gating is indicated by the signal-to-leakage ratio. On the assembled 16-level modulator, the signal-to-leakage ratio was measured at 40 db, where the signal was due to one oscillator gated on and the leakage was the sum of the gate leakage and stray-coupling leakage of all 17 oscillators when gated off. The measurement was made at the output of the summing amplifier. This is very good isolation; it is due to good gates, isolation resistors in the summing amplifier, and toroidal transformers that minimize stray fields. Many more oscillators could be added to the modulator without causing system problems due to leakage.

The sync oscillator is required to produce a 180° phase shift with fair accuracy. The multiplication factor of nine in the solid state transmitter multiplies the phase shift by nine, so that an incorrect phase shift from 0° to 160° would be multiplied to $(160^{\circ} \times 9) - (360^{\circ} \times 4) = 0^{\circ}$, which demonstrates complete destruction of the modulation due to an original error of 20° . The accuracy of the 180° phase shift was tested by a null method, that is, by measuring the summing amplifier output first with the 0° gate on and then with both the 0° and 180° gates on. In the latter case, the 180° output cancels the 0° output, if the two outputs are equal. A "one on" to "both on" ratio of 33 db was measured. Spectrum tests at 2.2 Gcps on the output of the solid state multiplier showed qualitatively that the 0° to 180° phase shift was still very good.

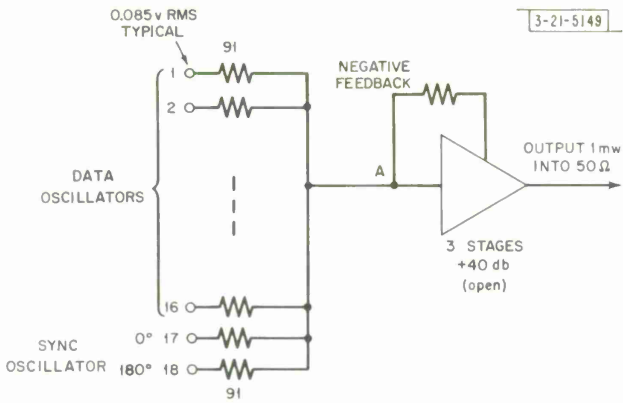


Fig. 11. Summing amplifier.

Fig. 12. Summing amplifier card.

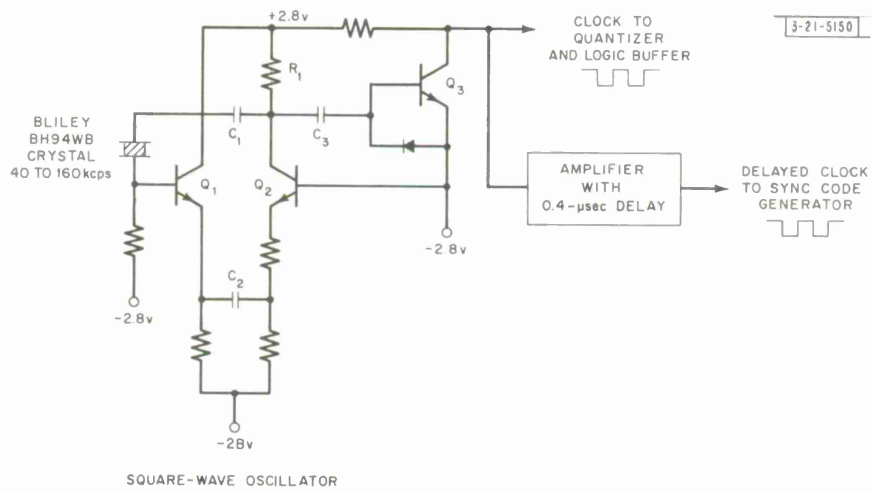
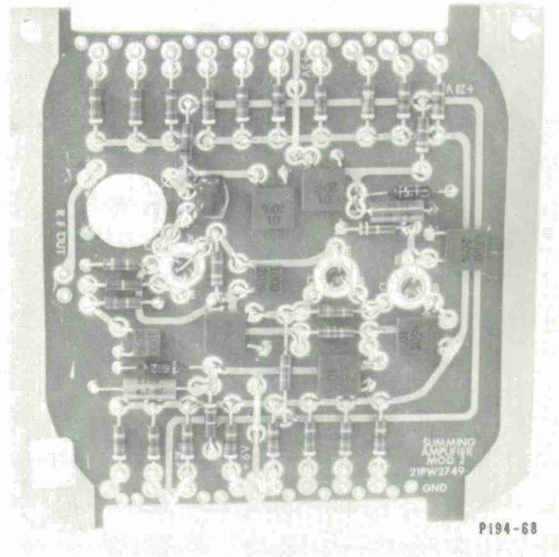


Fig. 13. Clock generator.

In summary, it was feasible to set up the oscillators with reasonable care and obtain the results just reviewed. The temperature tests which were made on 25 oscillators showed some which had abnormal frequency and amplitude deviations with temperature, particularly among the 16 oscillators which used CR 64/U crystals. One of nine oscillators with G30 crystals had deviations well outside the ranges of the other eight. Aside from its use in checking temperature tracking of a set of oscillators, the temperature testing aids in weeding out oscillators with substandard crystals or circuits.

5. Summing Amplifier

Figure 11 is a block diagram of the summing amplifier which is made up of 18 summing or isolation resistors and a 3-stage amplifier. The input impedance of the amplifier at point A is about 5 ohms; this low impedance in conjunction with the 91-ohm input resistors produces low coupling between oscillators. The amplifier has an open-loop gain of 40 db and 14 db of feedback. The over-all gain of the circuit, including the isolation resistors, is approximately 11 db. The amplifier has a nominally flat frequency response from 4 to 10 Mcps. The power output of one milliwatt was chosen as a nominal value suitable for driving succeeding transmitter stages. The summing amplifier on its $4\frac{1}{4}$ -inch-square card is shown in Fig. 12.

6. Clock Generator

Timing-clock pulses for the transmitter system are derived from the clock generator of Fig. 13. The oscillator circuit, composed of Q_1 , Q_2 , and other components, is a crystal-controlled square-wave oscillator in which a series-resonant crystal is the only tuned element. Regenerative feedback is produced by capacitor C_1 , the series resistance of the crystal, and capacitor C_2 . The amplitude of oscillation is limited between ± 3 volts peak to peak by the collector supply and collector saturation voltages of Q_2 . Capacitor C_3 serves as a coupling capacitor from the oscillator to the buffer amplifier Q_3 ; in addition, it acts with R_1 as a low-pass filter which inhibits oscillations at harmonic modes of the crystal. The crystal is a ruggedized type manufactured by the Bliley Electric Company. The frequency-vs-temperature characteristic of the oscillator is parabolic in shape; the frequency decreases approximately 5 cps from $+25^\circ$ to -40°C and from $+25^\circ$ to $+80^\circ\text{C}$. This oscillator circuit was found to operate satisfactorily at both 40 and 160 kcps.

Delays in the quantizer cause the quantizer output gates to lag the quantizer clock by $0.4\ \mu\text{sec}$. The clock generator output to the sync-code generator is therefore delayed by $0.4\ \mu\text{sec}$ so that sync and data gates and sync-code switching will be phased the same as data pulses. Figure 14 shows the clock generator card.

7. Frame Timer and Sync-Code Generator

This logic assembly is the timer for the transmitter system. It counts $25\text{-}\mu\text{sec}$ time slots up to the frame length and generates an appropriate synchronization code with sync and data gates for modulation of the sync and data oscillators. The output of the frame timer may be used along with the 40-kcps clock to synchronize an external time multiplexer. The frame length is 6.4 msec, made up of 256, $25\text{-}\mu\text{sec}$ time slots, of which 24 are used for transmission of synchronization information to the receiver, leaving 232 slots for data transmission. Thus, a synchronized time multiplexer could sample 232 separate data sources, and each source would be sampled at the frame repetition rate of 156.2 cps.

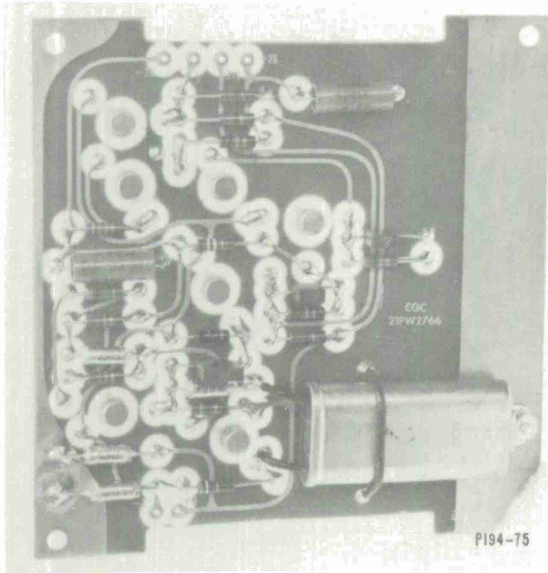
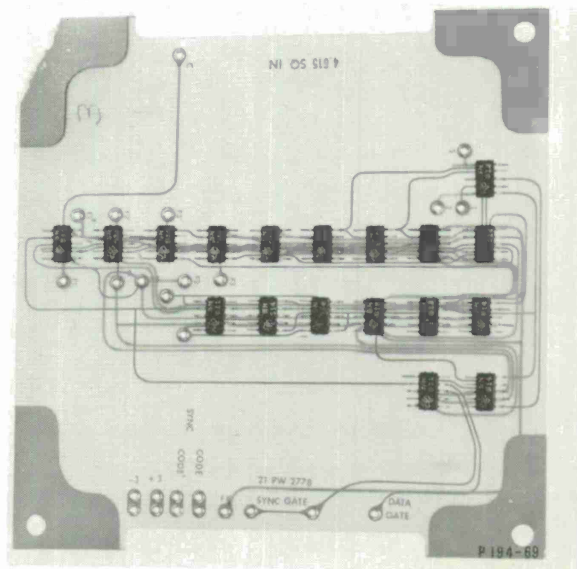


Fig. 14. Clock generator card.

Fig. 15. Frame-timer and sync-code generator card.



The timer and code generator was made of microminiature logic units of Texas Instruments, Incorporated, series 51, so that the whole logic assembly could be built on one printed board. A series-51 unit (flip-flop, NAND gate, etc.) is $0.25 \times 0.125 \times 0.035$ inch thick. Interunit connections are all welded. Figure 15 shows the assembled timer and code generator card.

The series-51 units operate in NAND logic, where logical one is represented by -2.8 volts and logical zero by $+2.8$ volts. Figure 16 is a logic diagram of the timer and code generator. It may be considered in four parts:

The ripple-through counter, units 1 to 8, is the frame timer. Counter stages are tapped at appropriate points for generation of the sync code and gates. Counter waveforms and count numbers may be seen in Fig. 17 (the numbers on the figure refer to the corresponding numbers of the logic diagram of Fig. 16).

The sync and data gate generator consists of units 12, 14, 19, and 15. The sync gate is true from counts 6 to 18 and from 134 to 146; the data gate is the inverse of the sync gate.

The sync-code generator section is made up of units 10, 11, 13, 14, and 16. The code is the 11-bit Barker¹⁰ code 11100010010. One bit is added at the right-hand end of the code to accommodate the one-bit delay and phase comparison method of demodulation in the receiver. Appropriate stages of the counter are tapped and combined in units 10, 11, and 13 to produce the code and the code complement at the output of units 13 and 14. Unit 16 is a gate that passes 000111011011 during the first half of the frame and its complement during the second half of the frame.

Units 9, 17, and 18 commutate the code in synchronism with the clock. The one-bit delay and phase comparison method of code demodulation in the receiver requires that ones be represented in transmission by phase changes (logic level changes in the code commutator). Therefore, the commutator switches levels when ones are present at its input, and does not switch on zeros. Figures 17 and 18 show the timing relations of the code and gate waveforms.

8. Logic Buffer

The logic buffer is used as an output buffer-amplifier following the clock and code generator. It comprises five 2-stage amplifiers plus a NAND gate and amplifier. The following logic waveforms are amplified by the logic buffer: sync code, sync-code prime, data gate, sync gate, and auxiliary clock. In addition, the sync gate and F'_8 from the frame counter are "NANDed" and amplified to produce a frame sync pulse for an external system. The logic buffer inverts all inputs. It is assembled of conventional components mounted on a $4\frac{1}{4}$ -inch-square circuit board.

9. Packaging

Printed-circuit cards were selected as the basic elements for the Orthomatch modulator rather than "cordwood" assemblies because the cards permit easier assembly, inspection, testing, and replacement of components after assembly. Connections were soldered instead of welded because soldering was more suitable for the available components. Input and output connections of the cards are made by eyelets on two edges. Interconnections are made by flexible insulated wires, except for RF connections and some video leads which are miniature coaxial cable to minimize stray coupling. The cards are stacked in sandwich fashion and the stack is held together by four long threaded bolts with nuts and lockwashers on each side of each card. The 40-kcps timing oscillator, sync-code generator, and logic buffer assembly of three cards may properly be considered a part of a multiplexer or the Orthomatch modulator, since the

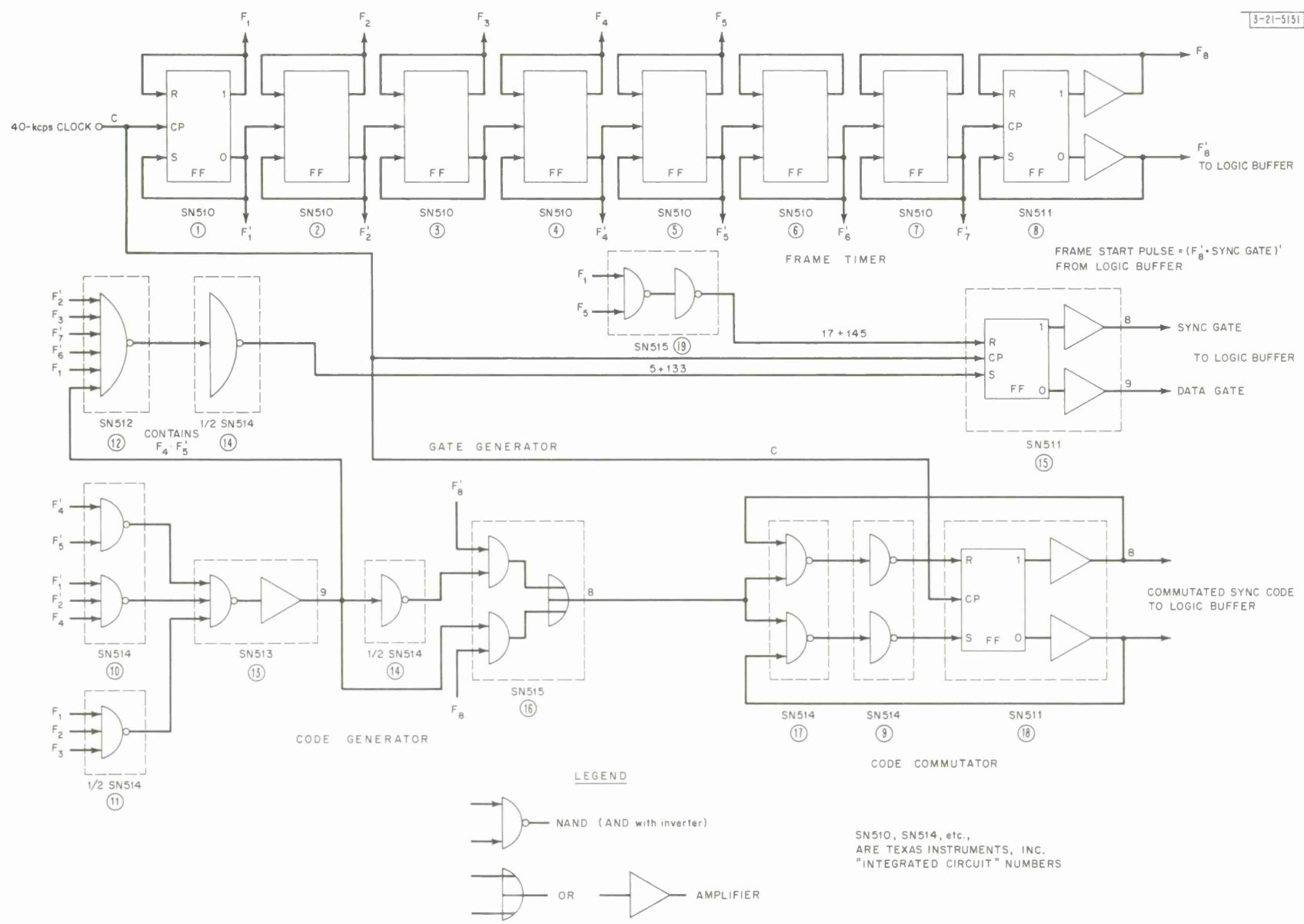


Fig. 16. Transmitter frame-timer and sync-code generator logic.

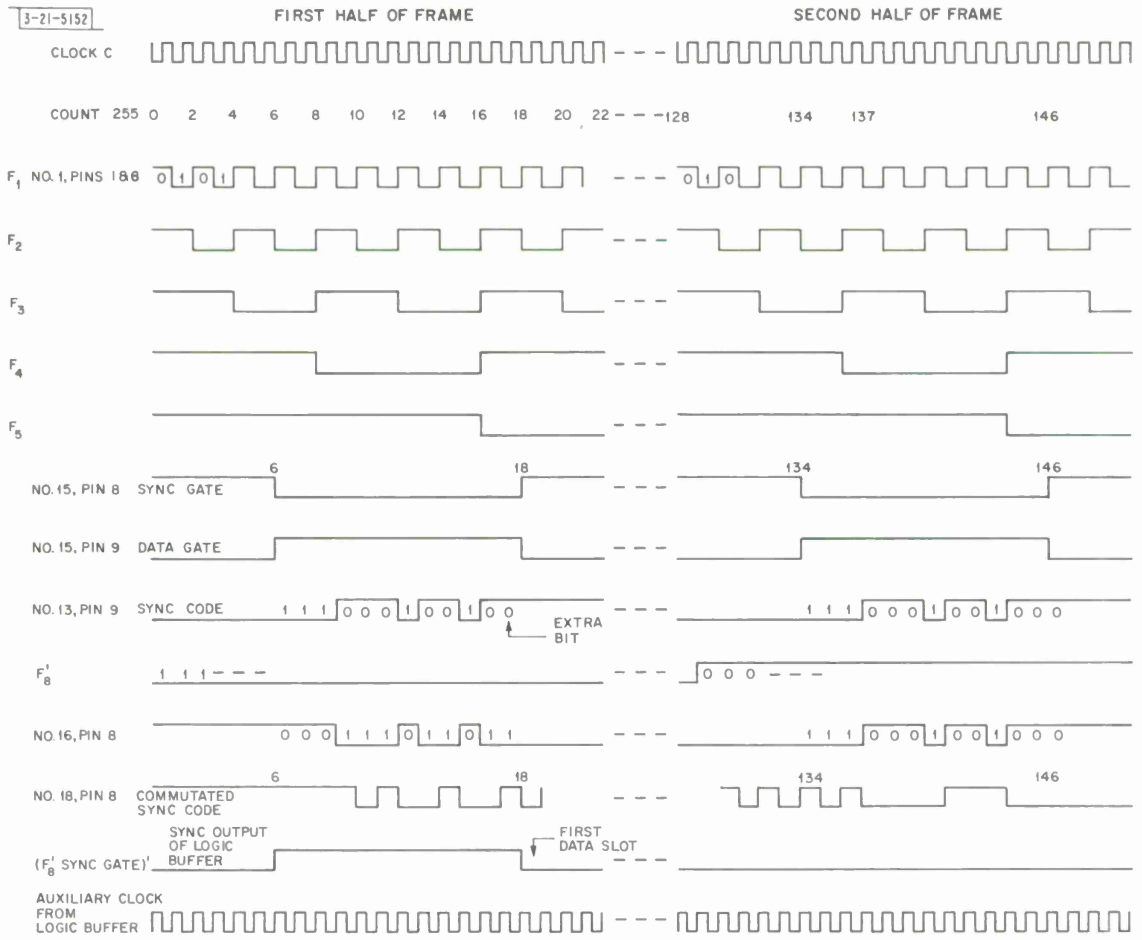
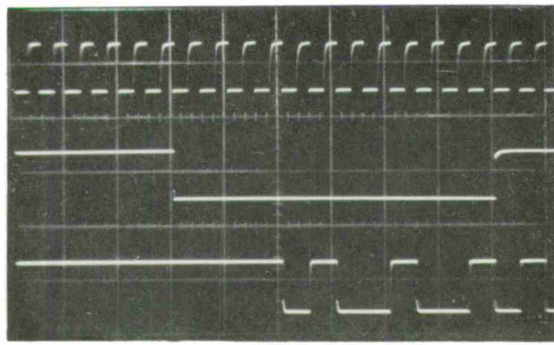


Fig. 17. Transmitter timing.



-21-5153

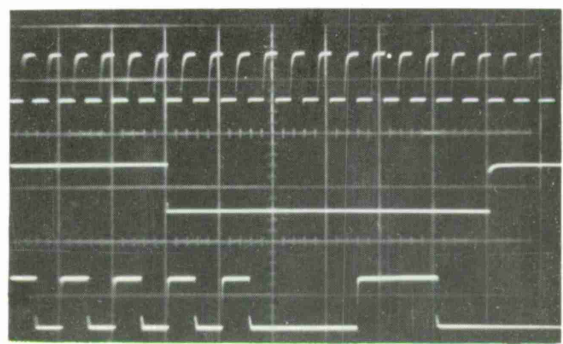
CLOCK INPUT C
TO SYNC CODE
GENERATOR

SYNC GATE:
NO. 15, PIN 8

COMMUTATED
SYNC CODE:
NO. 18, PIN 8

Vertical scale 5 volts/cm
Horizontal scale 50 μ sec/cm
Scope sync fall of F'_8

(a) First half of frame.



-21-5154

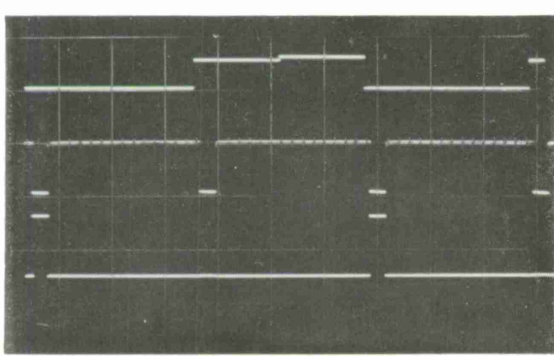
CLOCK C

SYNC GATE:
NO. 15, PIN 8

COMMUTATED
SYNC CODE:
NO. 18, PIN 8

Vertical scale 5 volts/cm
Horizontal scale 50 μ sec/cm
Scope sync rise of F'_8

(b) Second half of frame.



-21-5155

F'_8 : NO. 8, PIN 8

SYNC GATE:
NO. 15, PIN 8

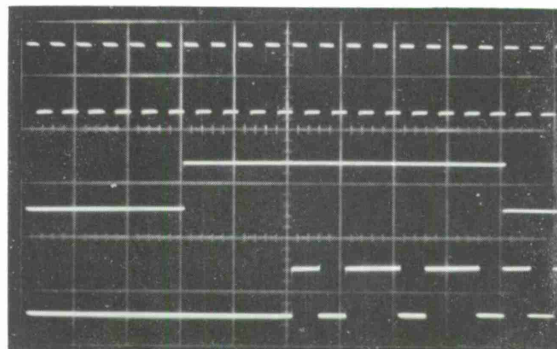
SYNC PULSE OUTPUT
OF LOGIC BUFFER

Vertical scale 5 volts/cm
Horizontal scale 1 msec/cm

(c) Whole frame.

Fig. 18. Transmitter timing waveforms.

Vertical scale 5 volts/cm
Horizontal scale 50 μ sec/cm



AUXILIARY CLOCK
OUTPUT OF LOGIC
BUFFER

SYNC GATE OUTPUT
OF LOGIC BUFFER

COMMUTATED SYNC
CODE OUTPUT OF
LOGIC BUFFER

(d) First half of frame.

Fig. 18. Continued.

timing system is common to both. The timing system cards were made in the same format as the other modulator cards and were mounted with them for the sake of convenience. Figure 19 exhibits the assembled stack of modulator cards. The receptacles, one each for the quantizer-oscillator and timing sections, are Microdot B43EF-15CP miniature connectors, each containing six coaxial and thirteen single connections. There are sufficient connections in each receptacle to allow one of them to be eliminated. Two connectors were installed for convenience in test operations. The modulator is shown with its cover on in Fig. 20. Its dimensions are $9\frac{1}{4} \times 5\frac{1}{4} \times 5\frac{1}{4}$ inches overall and it weighs $2\frac{1}{4}$ lb.

10. Power Supplies

The Orthomatch modulator uses plus and minus 28 volts DC and plus and minus 2.8 volts DC from external supplies. The plus and minus 2.8-volt supplies are required for the timing section. Auxiliary voltages required in the quantizer-oscillator section (+12, +6, and +5 volts) are obtained internally from zener diodes. The current drains are:

Supply (volts)	Regulation (volts)	Current Drain (ma)
+28	± 1	102
-28	± 2	55
+2.8	± 0.2	34
-2.8	± 0.2	34

The total power consumption is 4.6 watts, and the required voltage regulation is shown by the plus and minus values above.

11. Reliability Comments

Orthomatch modulator components were tested over the temperature range from -40° to $+80^{\circ}$ C with satisfactory results, some of which have been discussed. The modulator operated perfectly in the laboratory environment during more than 100 hours of system tests. In order to qualify the Orthomatch modulator for operation in space, reliability analyses and extensive environmental testing would be required. Lack of a specific application and manpower and time limitations have precluded reliability analyses and further tests.

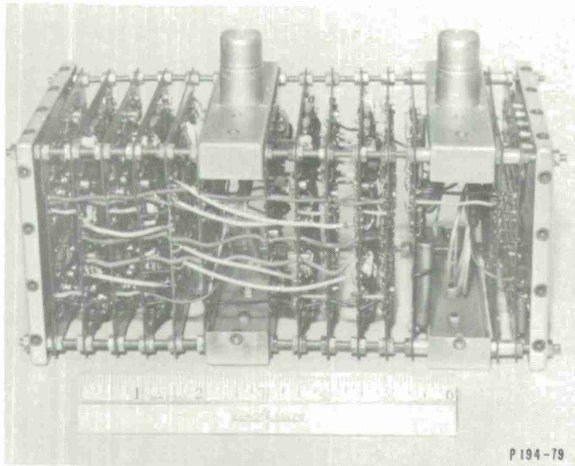


Fig. 19. Assembled modulator cards.

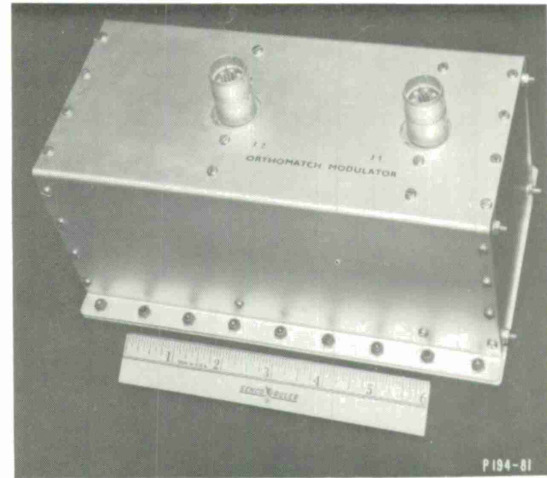


Fig. 20. Orthomatch modulator.

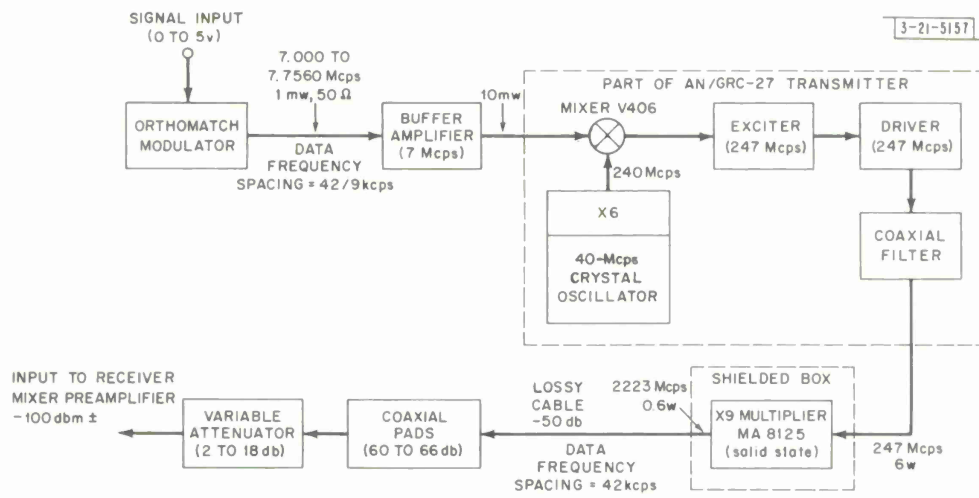


Fig. 21. Orthomatch transmitter test setup.

C. Test Transmitter System

A complete transmitter system, including the Orthomatch modulator and high-frequency components, was assembled for Orthomatch tests in the 2.2- to 2.3-Gcps telemetry band. Previous Orthomatch tests had been made at low frequencies, and it was desired to learn if conversion and multiplication of Orthomatch signals to 2.2 to 2.3 Gcps would cause signal degradation and increased error rates. Because it was available, the expedient of using part of an AN/GRC-27 transmitter and a borrowed solid state multiplier was adopted. Figure 21 is a block diagram of the test transmitter assembly, with power and frequency levels marked. The power loss in the solid state multiplier is 10 db; this large loss is due to the fact that frequencies in the multiplier's normal response band were not available from the GRC-27 transmitter. Normal output from this multiplier is more than 2 watts for a 10-watt input.

Test signals from Orthomatch oscillators were passed through the transmitter in Fig. 21 and observed on a spectrum analyzer to check the results of multiplication. Observations of pulse-modulated signals at 247 and 2223 Mcps showed that multiplication increased the spacing of carrier frequencies by an amount equal to the multiplication factor, but did not affect the frequency spacing of individual signal side lobes, as was expected. This is illustrated by Fig. 22. Of more concern was the effect of multiplication on the phase-modulated sync oscillator signals, since phase shifts are multiplied, and the phase modulation may even be destroyed, as discussed in Sec. IV-B-4. An oscillator whose phase is switched abruptly between 0° and 180° at a 50-percent duty ratio exhibits a frequency spectrum in which the carrier frequency is absent and which has side-lobe spikes spaced at frequencies $1/T$ apart, where T is the modulating pulse width. Asymmetry in pulse width or departures from 180° phase shift cause the carrier frequency to reappear. Figure 23 shows the spectra of an Orthomatch sync oscillator that is symmetrically biphas modulated. The absence of the carrier at 2.22 Gcps shows that the accuracy of the biphas modulation is very good and is not degraded by the GRC-27 transmitter or by the X9 multiplier.

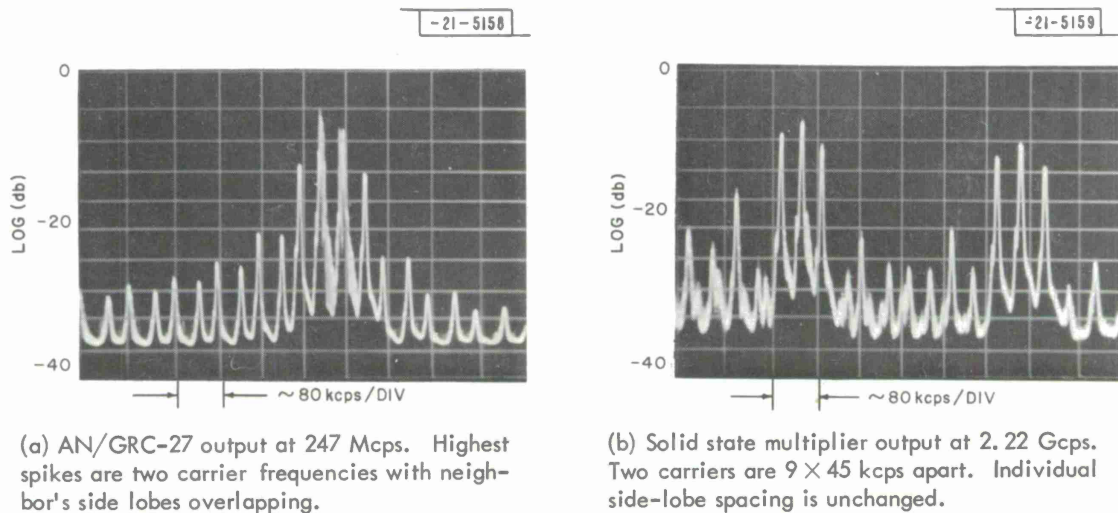
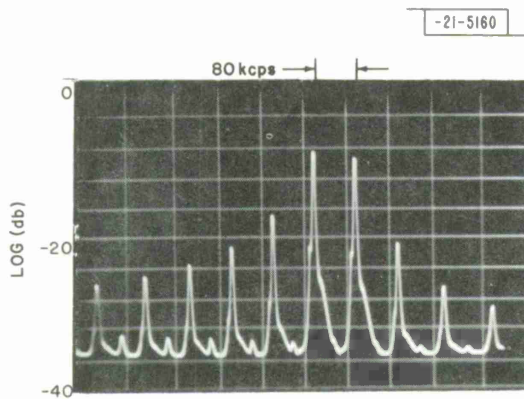
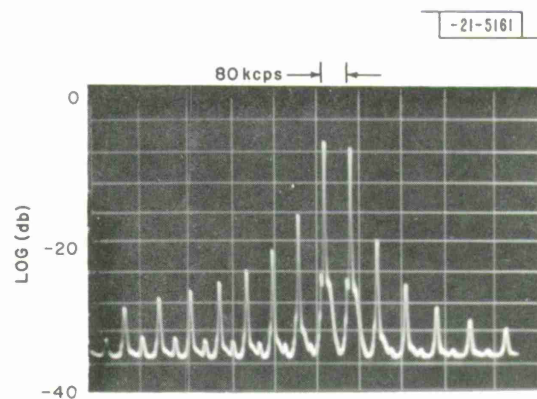


Fig. 22. Pulse-modulated test signals. Two oscillators 45 kcps apart, keyed alternately with 12.5- μ sec pulses, 50-percent duty ratio. NOTE: The spectrum analyzer amplitude-vs-frequency response is non-uniform.



(a) AN/GRC-27 output at 247 Mcps. Carrier null is between two highest spikes.



(b) Solid state multiplier output at 2.22 Gcps. Carrier null is between two highest spikes.

Fig. 23. Biphase-modulated test signals. Modulating pulses 12.5 μ sec wide, 50-percent duty ratio. NOTE: The spectrum analyzer amplitude-vs-frequency response is non-uniform.

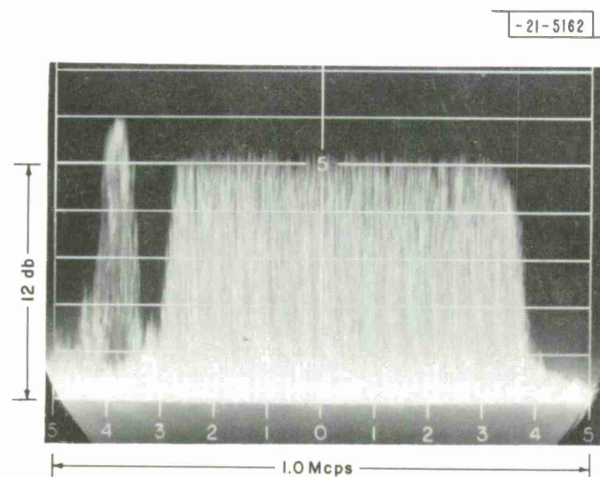


Fig. 24. Orthomatch spectrum at 2.22 Gcps. Sixteen data oscillators and sync oscillator operated in sequence.

Figure 24 displays the spectrum at 2.22 Gcps of the Orthomatch transmitter signals due to the staircase test signal which operated all 16 data frequencies in repeated sequences. Sync-frequency transmission, in its normal time slots within a frame, is also present. The sync frequency at the left is 126 kcps above the highest data frequency. It appears higher in amplitude because it is gated on for a longer time than any single data frequency. This spectrum shows that the bandwidth occupied by an Orthomatch system at 16 levels and a 40-kcps word rate is approximately 900 kcps at -12-db points.

D. Proposed Transmitter System

A solid state transmitter system suitable for Orthomatch is outlined in Fig. 25(a). The Orthomatch signals are frequency-converted and amplified by semiconductor diodes and transistors to 250 Mcps and then multiplied to 2.25 Gcps by two varactor triplers in cascade. Power output of at least a few watts from such a transmitter is practical, considering the current state of the art. Efficiency (RF power output divided by DC power input) would be in the neighborhood of five percent. Satisfactory proposals for design and construction of a solid state transmitter following the general configuration of Fig. 25(a) were received in 1963 from a number of solid state equipment manufacturers.

An alternate transmitter system for 2.2 to 2.3 Gcps is shown in Fig. 25(b). Here an exciter is used to convert the Orthomatch signals to 2.25 Gcps at low-power level, and an amplifier at 2.25 Gcps increases the output power. A traveling-wave tube (TWT), triode, ampliftron, or klystron amplifier might be used; however, TWT amplifiers are most advanced with regard to reliability for space operation. Over-all efficiencies of 15 to 20 percent are achieved by available TWT amplifiers of 2- and 10-watt outputs; therefore, a TWT transmitter requires less DC power than a solid state transmitter.

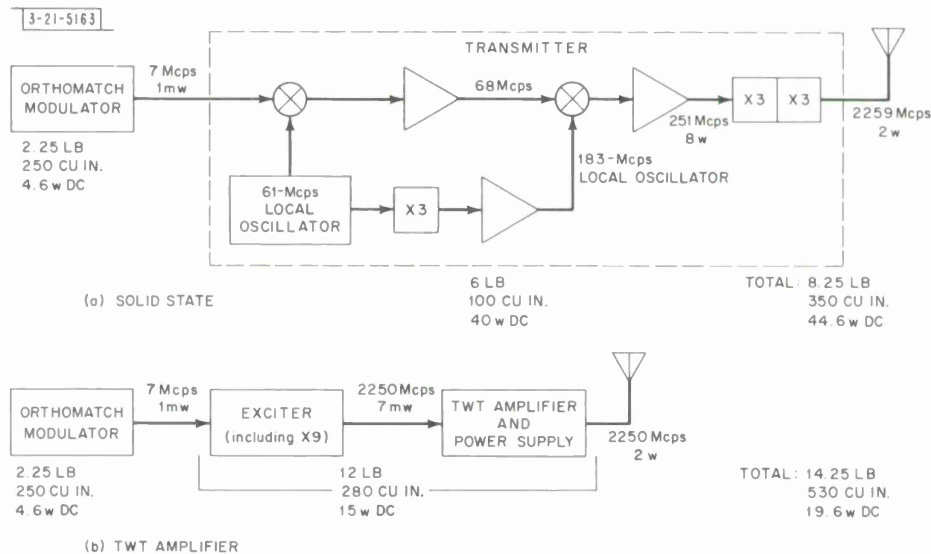


Fig. 25. Orthomatch transmitters.

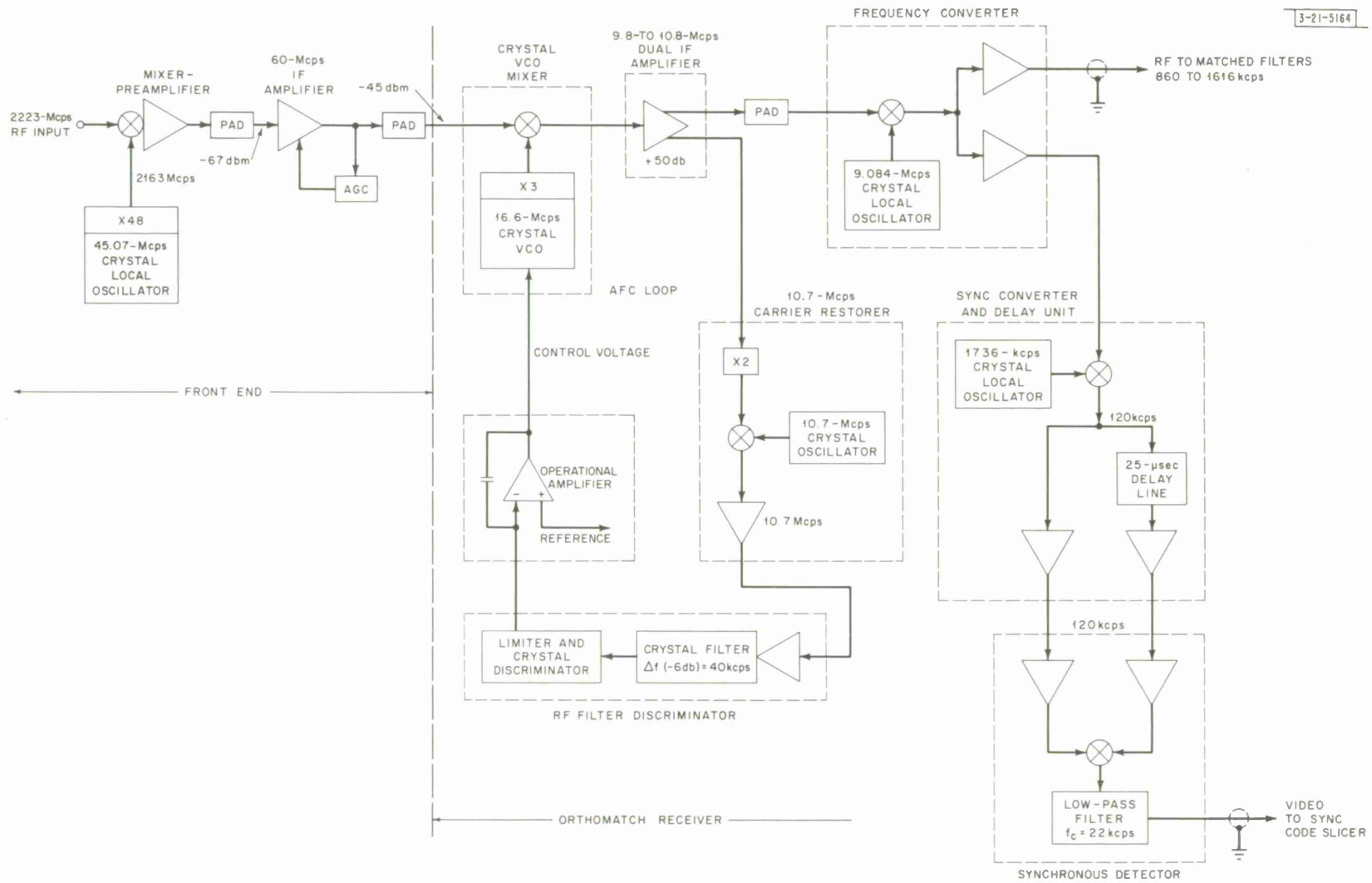


Fig. 26. RF section of Orthomatch receiver.

The solid state transmitter has inherent reliability advantages over vacuum-tube amplifier transmitters because solid state transmitters do not use vacuum envelopes, heated cathodes, or high-voltage power supplies. Size, weight, and over-all complexity also favor the solid state transmitter. These advantages would overcome the efficiency disadvantage of the solid state transmitter in most applications. However, if power output of more than a few watts is needed at 2.2 to 2.3 Gcps or higher frequencies, vacuum-tube amplifiers undoubtedly would be required, both because of limitations in the capabilities of current solid state devices and because of efficiency factors.

E. Transmitter Frequencies

The 2.2- to 2.3-Gcps telemetry band has been emphasized in this report because it has been designated by government authorities for current and future operational transmitters in earth satellites and deep-space vehicles. This band of frequencies is suitable for operation with earth-based receivers because it is in the "window" where sky noise and atmospheric absorption are low. The Orthomatch system can easily be operated at frequencies below 2.2 to 2.3 Gcps with appropriate oscillator spacings and multiplication factors of three or one. For frequencies above 2.2 to 2.3 Gcps, up-conversion of Orthomatch modulator signals could be adopted without multiplying by more than nine. A multiplication factor of 27 can be considered, but this would require careful control of the differential deviation with temperature of data oscillators. This might be accomplished by specification and selection of oscillator crystals or by placing the oscillator circuits in a temperature-controlled oven.

F. Receiver Outline

A receiving system for Orthomatch has been assembled and tested satisfactorily. A block diagram of the RF section of the receiver is given in Fig. 26. RF subassemblies below 60 Mcps were built in Lincoln Laboratory particularly for Orthomatch and were packaged in a special plug-in rack. The front end of the receiver, including the 2.22-Gcps mixer-preamplifier, local oscillator, and 60-Mcps IF amplifier, was assembled with available commercial equipment.

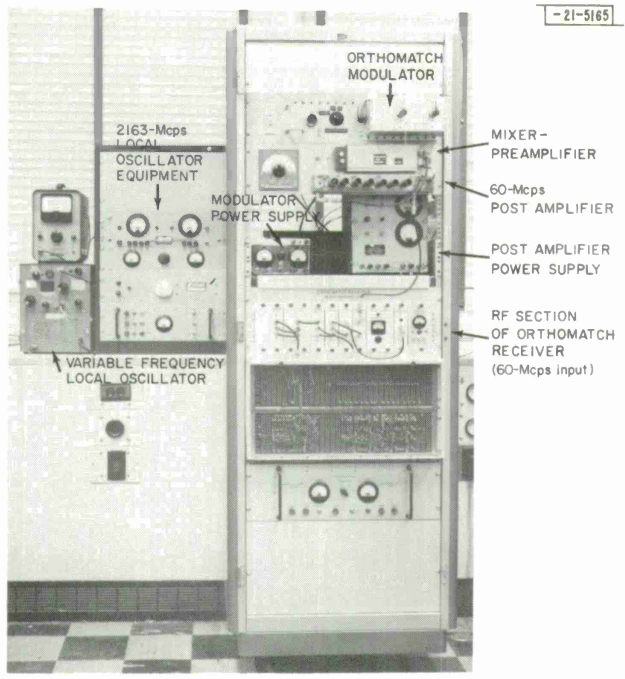
The other major sections of the Orthomatch receiver are outlined in Fig. 1. Matched filters, "greatest-of" circuitry, and parts of the sync and timing recovery system were designed and built specially for Orthomatch; the remaining circuits are logic elements which were available from existing Lincoln Laboratory designs.

G. Receiver Test Assembly

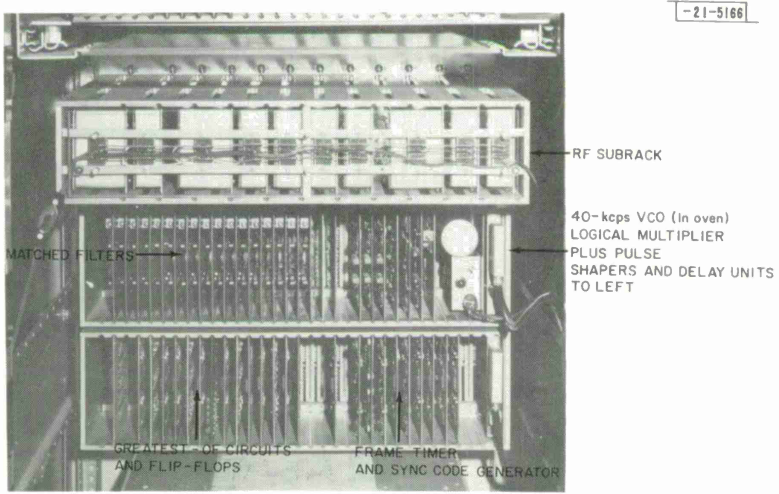
Figure 27 shows the Orthomatch receiver equipment assembled in a cabinet along with other components for convenient test purposes. In an operational system, the mixer-preamplifier, local oscillator, and 60-Mcps IF amplifier should be mounted near the antenna and connected to the input of the Orthomatch RF chassis by a length of 50-ohm cable. The logic subracks contain the set of 16 matched filters and all other essential data, sync, and timing recovery circuits.

H. Receiver Front End

No difficult performance demands are made upon the receiver front end for Orthomatch. The front-end passband should encompass the Orthomatch spectrum with nominally flat response. A crystal-controlled local oscillator, with a frequency stability of approximately one part per



(a)



(b)

Fig. 27. Orthomatch receiver test setup.

million, is recommended to avoid putting undue frequency-tracking demands upon the AFC system. The 60-Mcps IF amplifier should have automatic gain control (AGC) to maintain the IF output within a few decibels of the output due to receiver noise alone. This is needed because the AFC loop, matched filters, and "greatest-of" circuits operate best with a fairly constant input level. The output level required of the 60-Mcps IF amplifier is approximately -45 dbm.

I. Orthomatch Receiver

The receiver assembly, beginning with the 60-Mcps input to the voltage-controlled crystal oscillator and mixer unit, is referred to as the Orthomatch receiver, since it contains all the subassemblies needed for Orthomatch signals. A front view of the Orthomatch receiver RF and logic subracks is shown in Fig. 27(a) and Fig. 27(b) is the rear view.

1. RF Section

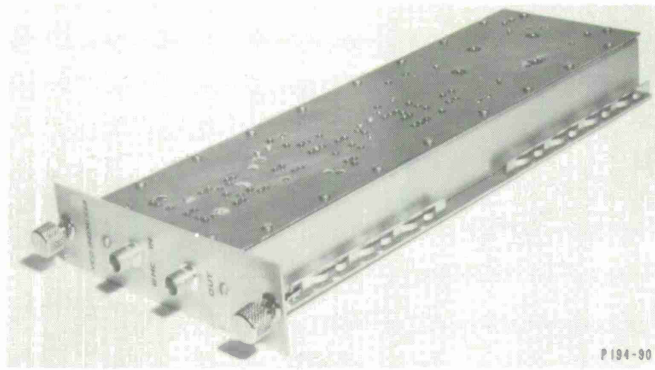
The Orthomatch RF chassis contains the AFC units, frequency converters, and amplifiers needed to present the Orthomatch signals to the matched filters, sync, and timing circuits at suitable frequency and power levels. Successive conversions downward in frequency were made to allow easy separation of desired from undesired products of mixing. The AFC loop and sync-frequency demodulator sections are of some particular interest and will be discussed separately later.

Circuits of the RF chassis were built in modular, plug-in packages to allow use of printed circuit boards, side-by-side assembly of circuits, and convenient interconnections. A typical RF plug-in package is shown in Fig. 28. The printed circuit board is on one side and a flat cover with extending edges is placed on the other side. The extending edges fit into slots in the chassis to position and guide the package into its receptacle. DC connections to the package are made via the plug at the rear, and RF connections are made on the front panel by coaxial cables. The printed circuits in these packages allow much easier installation of components, and produce a better final wiring job than the three-dimensional component assemblies normally used for RF circuits. The plug-in assembly of packages is tidier and more convenient to handle than a tray layout of boxed circuits.

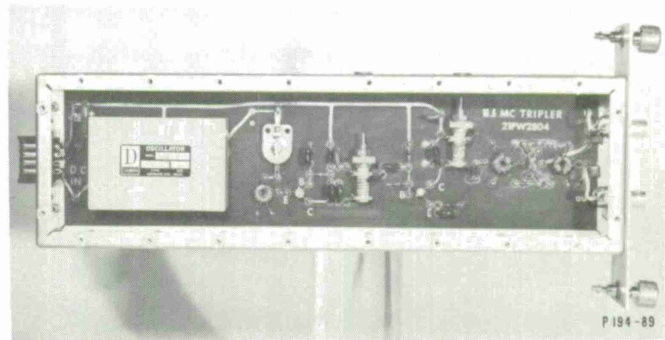
2. AFC Loop

Frequency control is required in the Orthomatch receiver to keep input data signals close to the center frequencies of matched filters and to keep the final sync frequency close to 120 kcps for optimum demodulation of the sync code. Matched-filter response falls off one db for a ± 12 -kcps deviation from center frequency (word rate = 40 kcps) and the sync demodulator response falls off 3 db for approximately a 3-kcps deviation from 120 kcps; the latter is due to changes in phase shift through the 25- μ sec delay line. From these considerations, it is estimated that frequency control within ± 3 kcps is required to avoid appreciable system degradation.

The AFC system operates on the sync frequency, since it is transmitted continually at nearly a 10-percent duty ratio. The components in the AFC loop, which operate on the sync frequency at 10.7 Mcps, are shown in Fig. 26. The IF amplifier raises the signal amplitude to a level high enough to produce limiting in the limiter which precedes the discriminator. A narrow-band crystal filter is used to reject unwanted data signals and to increase the signal-to-noise ratio. The discriminator provides a DC voltage proportional to RF deviation which is

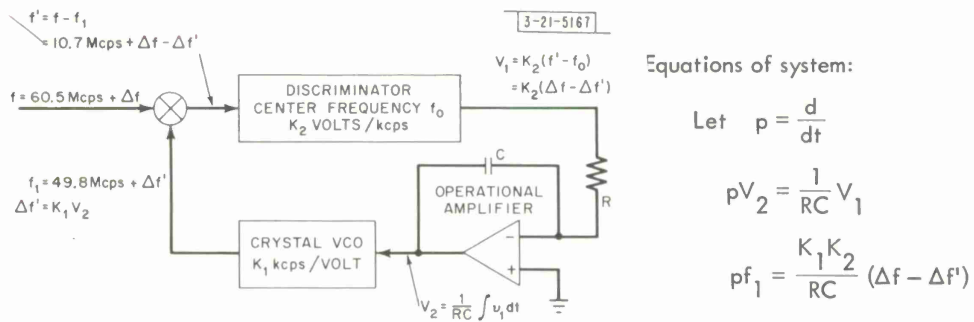


(a)



(b)

Fig. 28. Typical receiver plug-in package.



NOTES:

- (1) In the steady state, $pf_1 = 0$ and the frequency error $(\Delta f - \Delta f') = 0$.
- (2) Circuit time constant $S = RC/K_1 K_2$.
- (3) If the input frequency changes at a constant rate α , the frequency error $(\Delta f - \Delta f') = S\alpha$ (frequency lag).
- (4) In the system built, $R = 100$ kcps, $C = 0.44 \mu f$, $K_1 = 6.7$ kcps/volt, $K_2 = 0.16$ volt/kcps, $S = 0.041$ sec. The frequency lag at 60-cps/sec input rate is 2.46 cps.

Fig. 29. AFC system.

applied to the integrating operational amplifier. This amplifier's output is a signal, proportional to the time integral of the frequency error, which is used to control the voltage-controlled crystal-oscillator (VCXO) frequency. The discriminator determines the frequency to which the nominal 10.7-Mcps signal is corrected; therefore, a crystal discriminator is used for stability.

The AFC system was first planned to operate on the central portion of the spectrum of the biphase-modulated sync signal; the central portion was to be selected by the crystal filter of 40-kcps bandwidth. Initial tests showed, however, that the AFC circuit locked readily upon either of the main side lobes of the spectrum, but was quite unstable in the central carrier-frequency region. As a result, the "carrier restorer circuit" was incorporated to destroy the biphase modulation by frequency doubling, which in effect folds the side lobes back on the carrier frequency. Carrier restoration produced satisfactory results but, because the AFC system had to be completed with components at hand, the assembly is not an optimum one. Since the 10.7-Mcps sync signal is doubled, operation of the filter, limiter, and discriminator at 21.4 Mcps would result in simplification. The crystal filter could also be narrowed in bandwidth because the modulation spectrum is removed.

An estimate of the required AFC tracking range for a practical 2.2- to 2.3-Gcps Orthomatch receiver is ± 90 kcps, including 30 kcps for received Doppler shifts, 55 kcps for transmitter local-oscillator drift, and 5 kcps for receiver local-oscillator drift. The Orthomatch AFC loop is capable of a ± 90 -kcps tracking range.

Figure 29 diagrams and notes the important characteristics of the AFC loop. This type of control circuit, incorporating a single integrator, has the following theoretical characteristics:

Zero frequency error when the input frequency is constant.

Frequency memory when the input signal is removed.

Frequency lag proportional to the rate of change of the input frequency.

In practice, the AFC loop tracked ± 90 -kcps input deviations with errors of 3 kcps or less at signal-to-noise ratios of +11 db or greater in the passband of the 40-kcps crystal filter. The signal-to-noise ratio at which matched-filter error rate is 10^{-5} , designated "system threshold," is +15.5 db, referred to a 40-kcps band. The contribution of AFC-corrected frequency deviations to matched-filter errors at and near the threshold was not measurable. Therefore, the AFC system has at least a 4.5-db performance margin over low-error data recovery. At signal-to-noise ratios below +11 db, AFC performance fell off rapidly, probably due to reduction of noise suppression by signals in the limiter. The lock-in range is ± 20 kcps, due to the 40-kcps filter.

Locking of the AFC loop is automatic only when the loop is resting within ± 20 kcps of the incoming signal frequency. In the system built, automatic search and lock features were not included. Locking over ranges greater than ± 20 kcps was manually aided by using the operational amplifier offset as a tuning control. An auxiliary narrow-band filter tuned to the sync frequency was used to observe the presence of the sync-frequency bursts as correct tuning was approached. Locking can also be observed by watching the action of the "AFC deviation" meter. The offset control knob and the deviation meter are on the front panel of the operational amplifier.

3. Sync-Code Demodulator

The sync-code demodulator converts biphase-modulated sync signals at 120 kcps to a video replica of the transmitter's sync code. It consists of the sync converter and delay unit plus the synchronous detector, which are shown in the RF block diagram of Fig. 26.

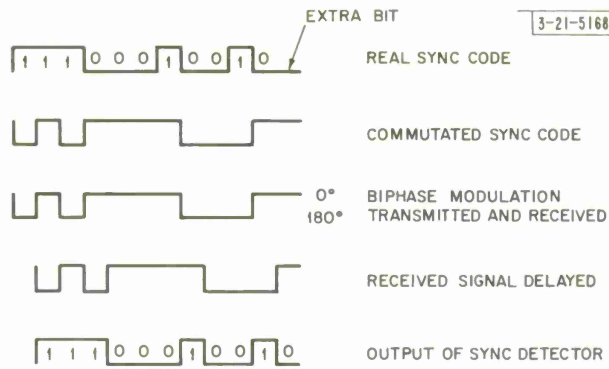


Fig. 30. Biphase modulation and demodulation waveforms.

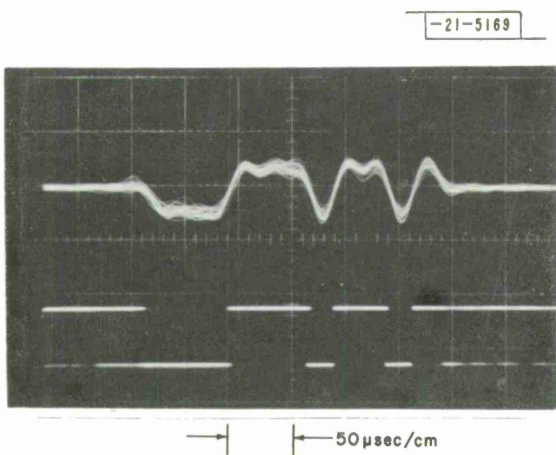


Fig. 31. Sync detector and slicer outputs.

Upper trace: sync detector output to slicer.
 Vertical scale: 2 volts/cm.
 Lower trace: sync slicer output.
 Vertical scale: 10 volts/cm.

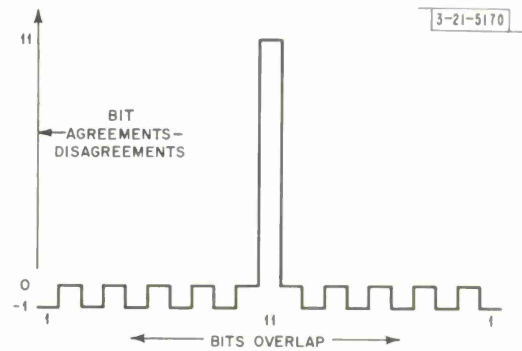


Fig. 32. Eleven-bit Barker code 11100010010 (noncyclic autocorrelation function).

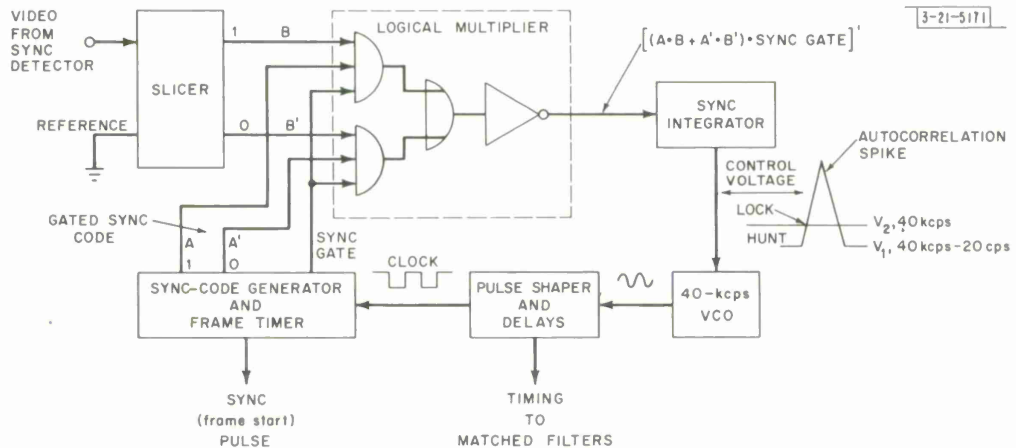


Fig. 33. Phase-locked timing loop.

Biphase demodulation is accomplished by one-bit delay and phase comparison; that is, the biphase signal at 120 kcps is delayed by one pulse interval and then compared with the undelayed signal to detect phase changes. This demodulation scheme requires that the code be commutated before transmission so that ones (or zeros if desired) are represented by phase changes. Furthermore, an additional bit is required at the end of the transmitted code in order to make the demodulator's phase comparison continuous to the end of the delayed code. The waveforms in Fig. 30 illustrate the modulation and demodulation scheme. A typical video output waveform of the synchronous detector is shown in Fig. 31.

The final sync frequency of 120 kcps was chosen because of the delay line. The delay line used was a commercial lumped-constant type with a low-pass cutoff frequency of 240 kcps. Operation of the delay line at 120 kcps permits passage of the first two side lobes of the modulation spectrum on each side of the carrier frequency. The phase shift through the delay line is required to be an integral multiple of π radians; at 120 kcps, the 25- μ sec line has a phase shift of 6π radians. If the input frequency changes to 110 or 130 kcps, the phase shift becomes an integral multiple of $\pi/2$ radians, which results in zero output signal from the synchronous detector. Therefore, input frequency control within a few kilocycles per second is required.

The synchronous detector is a straightforward phase detector. The low-pass filter on the synchronous detector output is a constant delay or linear-phase response filter which cuts off at 22 kcps, just above the highest fundamental frequency of the code waveform.

4. Phase-Locked Timing Loop

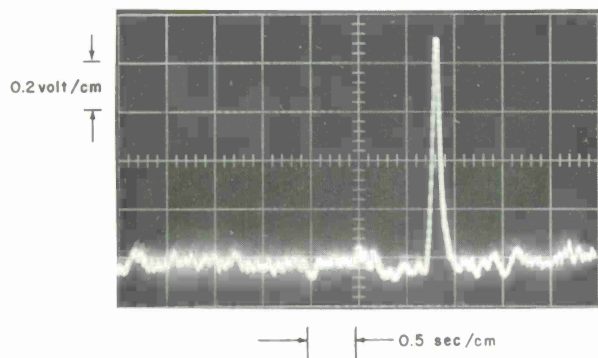
Recovery of both word and frame timing is accomplished in the phase-locked timing loop. This circuit acts as a correlator of the received sync code and a locally generated code. In the unlocked condition, the locally generated code "slides through" the received code; a logical multiplier detects the autocorrelation function of the code, producing a voltage which phase locks the local timing oscillator when the codes coincide. Since the local code is clocked by the local timing oscillator, locking of the oscillator on the autocorrelation function results in phase or time coincidence of the receiver's frame timer and sync-code generator with respect to the transmitter's timing system. In the locked condition, correctly phased timing pulses are available for clocking the matched-filter data system and for identifying the start of data frames.

The sync code used is the 11-bit Barker code 11100010010 which has a noncyclic autocorrelation function with a peak-to-tail ratio of 11 to 1. The idealized autocorrelation function of this code is shown in Fig. 32. This function is formed by sliding two code groups past one another, bit by bit, and taking the total of bit agreements minus disagreements in the overlap interval; this is actually done by the logical multiplier and integrator in the correlation circuit. The Barker code is transmitted twice per frame to increase the signal-to-receiver noise ratio; one code group is inverted to avoid ambiguity in correlation and frame locking.

Figure 33 is a block diagram of the phase-locked timing loop. This phase-locked loop, as compared with the usual continuous-wave loop, is complicated by the fact that the input signals are discontinuous and a pulse integrator is used. The circuit was developed by experiment and it will be described qualitatively.

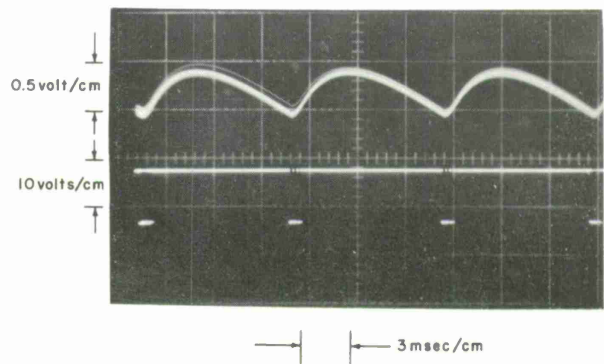
The slicer converts the video signal from the synchronous detector to a logic-level signal for application to the logical multiplier. Figure 31 shows the input and output of the slicer. The slicer's output contains the received sync code during the sync time slot and is noisy elsewhere.

-21-5172



(a) Autocorrelation spike (11-bit Barker code) observed at sync-integrator test point (loop opened). Hunt frequency: 20 cps.

-21-5173



(b) Upper trace: sync-integrator output to VCO. Lower trace: input to sync integrator.

Fig. 34. Timing loop waveforms.

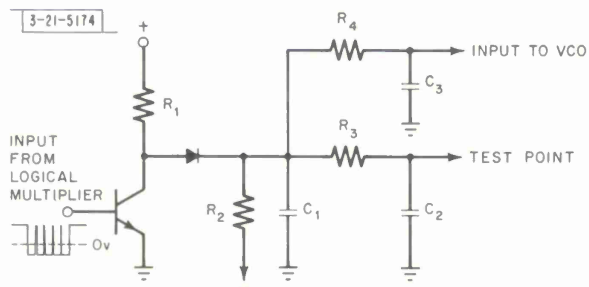


Fig. 35. Sync-integrator circuit.

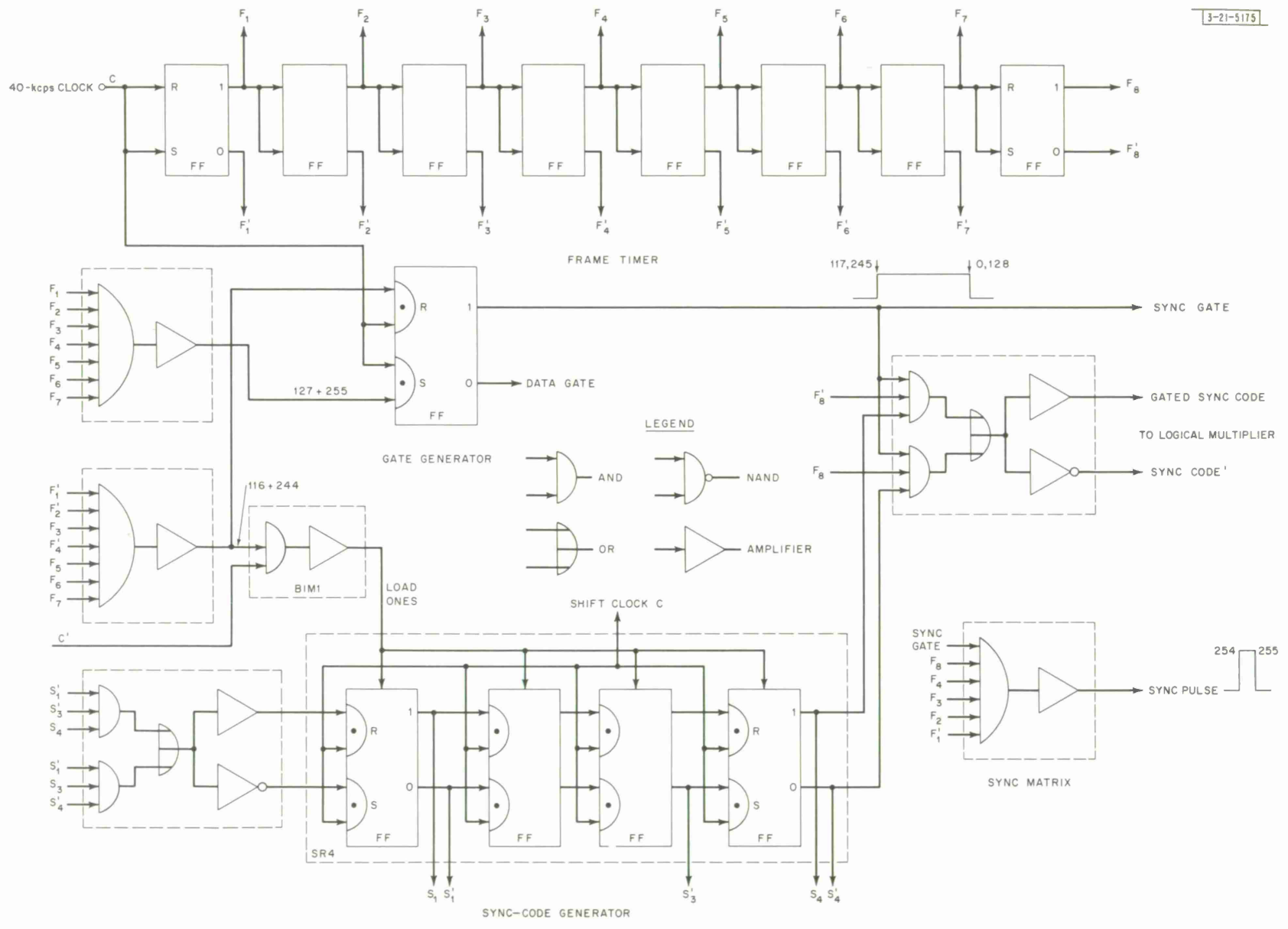
Locally generated code, with the same time spacing as the received code, is applied also to the logical multiplier. The logical multiplier (exclusive-OR circuit) is the digital equivalent of an analog phase detector. The logical multiplier is gated by the local sync gate so that it will sample the received signal only during the time of occurrence of the local code. Omitting the gate and making a continuous signal comparison would permit noise during intercode intervals to contribute unnecessarily to the correlation and averaging, resulting in a greatly reduced autocorrelation spike.

The 40-kcps voltage-controlled oscillator (VCO) is adjusted to run at 39,980 cps when unlocked. This is 20 cps lower than the transmitter clock, and causes the local code to slide continuously in time with respect to the received code. With a 256-word frame, the local code traverses a complete frame in 12.8 seconds. When received code is present, frame coincidence produces a rising voltage due to correlation, causing the VCO frequency to increase, and phase lock at 40 kcps occurs on the side of the autocorrelation spike. Figure 33 contains a diagram illustrating the hunt and lock conditions of the VCO. Figure 34(a) shows the autocorrelation spike. The VCO has a frequency-voltage constant of approximately 120 cps/volt near 40 kcps. It is normally adjusted to hunt at 0.16 volt and locks at 0.32 volt. The VCO as built is an LC oscillator provided with fine voltage-tuning control by a pair of varactor diodes. The complete VCO circuit is mounted inside a temperature-controlled oven. The oscillator's stability with a constant input voltage is approximately ± 1 cps.

Figure 35 is the sync-integrator circuit. This circuit stores and smoothes the gated voltages that result from correlation in the logical multiplier, and supplies the control voltage to the VCO. During gates, the transistor amplifies negative input signals and supplies charge via R_1 to C_1 . Since the loop hunts between code groups, the amount of negative signal within gates is relatively small; however, it increases rapidly as code correlation is approached and causes an increase of charge on C_1 which corresponds to the autocorrelation spike. Charge leaks off C_1 via R_2 between gates; this leak-off is necessary to prevent continuous increase of charge on C_1 due to noise input during hunting between code groups. R_4 and C_3 form a low-pass filter to provide additional smoothing. Figure 34(b) shows the input and output signals of the sync integrator. A test point with a very-low-pass filter (R_3 - C_2) is provided to permit noise-free observation of the autocorrelation spike.

Tests with varying signal-to-noise ratios in the receiver showed that reliable lock-on of the phase-locked loop is obtained at signal-to-noise ratios several decibels below levels which produce high error rates in the matched filters. At a signal-to-noise ratio which gave a 10^{-5} word error rate in the matched filters, jitter in recovered timing was slightly less than ± 1 - μ sec peak, corresponding to phase jitter of approximately $\pm 15^\circ$ in the phase-locked loop. This timing jitter causes degradation of approximately one decibel in matched-filter data recovery. Appreciable timing jitter was still present at higher signal-to-noise ratios. Failure of the timing loop to reduce phase jitter sharply is due to the fact that lock-on occurs on the side of the autocorrelation spike, leaving the received and local codes slightly out of phase and always allowing some noise to be gated through the integrator. This situation could be corrected by adding "guard" bits to the transmitted sync code; however, it is not considered necessary for the 40-kcps data rate system.

Lock-on time for the system is 12 to 13 seconds maximum due to the 20-cps difference frequency of hunting; average lock-on time is approximately six seconds, based on random starts.



38

Fig. 36. Receiver frame-timer and sync-code generator logic.

Hunt and lock takes place automatically after the receiver is tuned by automatic frequency control.

5. Frame Timer and Sync-Code Generator

The frame timer and sync-code generator produce a locally generated sync-code sequence which corresponds to the transmitter's code sequence. When the received code and locally generated code are correlated in the logical multiplier and locking of the phase-locked timing loop occurs, the receiver's frame sequence becomes phase locked to the transmitted frame. Then the receiver frame timer may be used to identify the start of the frame and the data slots within the frame; that is, it can serve as a timer for de-multiplexing.

The logic diagram of the frame timer and sync-code generator is Fig. 36. The logic units are of the Lincoln Laboratory - West Ford logic series which operate in AND/OR logic. The frame timer and gate generator follow the same logic arrangement used in the transmitter. Since, in the demodulation process, the transmitted 12-bit sync code is reduced to the 11-bit Barker code, only the 11-bit code and an 11-bit gate are required in the receiver. The sync code is generated by a 4-stage shift register with a feedback matrix. The shift register generates the Barker code sequence immediately after it is loaded with ones. The code and the code complement are gated out to the logical multiplier during the first and second halves of the frame, respectively.

The count numbers of the receiver's frame timer do not agree with the count of the transmitter's frame timer. This does not matter, but the receiver sync or block start pulse must be placed correctly to identify the first data slot. The first data slot does not occur immediately after the receiver sync gate because there is more delay in the sync-code demodulation and filtering process than in the matched-filter data decoding. The relative demodulation delays are such that the receiver sync pulse's falling edge at count 255 occurs near the beginning of the first data slot. Figure 37 shows received and local codes while locked, and Fig. 38 shows the position of the receiver sync pulse with respect to the beginning of data.

It is possible, if polarities in the receiver are incorrect, to identify the middle of the transmitter frame as the beginning, and thus incorrectly identify all the data slots. At the beginning of the frame, the transmitter sends phase reversals corresponding to the inverted Barker code 00011101101. These phase reversals can be recognized by observing the output of the auxiliary sync-burst filter which is used to check AFC lock; the receiver sync pulse should occur just after this phase-shift sequence.

6. Matched Filters

Figure 39 is a circuit diagram of a matched filter. Basically, it comprises a high-Q series-resonant filter with a short-circuiting switch, followed by a detector and filter. Q_1 is an input amplifier which drives L_1 and C_1 via transformer T_1 . T_1 has a one-turn secondary winding to minimize its resistance in the series circuit. L_1 and C_1 are in series resonance at the desired frequency. Q_2 and Q_3 are cascaded emitter followers which take the output from the resonant circuit without loading it appreciably. Regenerative or "Q-multiplier" feedback is applied from the emitter follower to the center tap of L_1 . Q_4 , Q_5 , and driving transformer T_2 form a switch that dumps the resonant circuit's energy when "squench" pulses are applied. R_d is a resistor which is adjusted for critical damping. A full-wave detector and

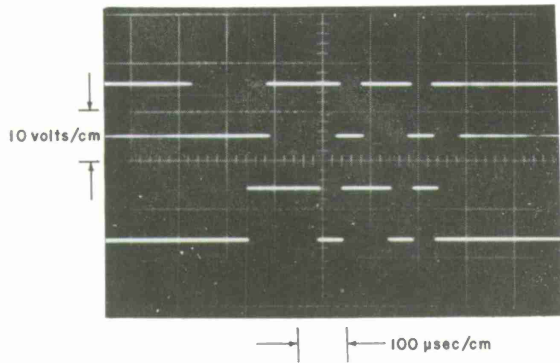


Fig. 37. Code inputs to logical multiplier (locked condition, first half of frame).

Upper trace: received sync code.
Lower trace: local sync code.

Fig. 38. Receiver sync pulse and ladder output with respect to the beginning of data.

Upper trace: receiver sync pulse.
Lower trace: analog data output from resistive ladder on flip-flops. Noisy output at left is in sync time slot. Sync pulse trailing edge is in first data slot of frame.

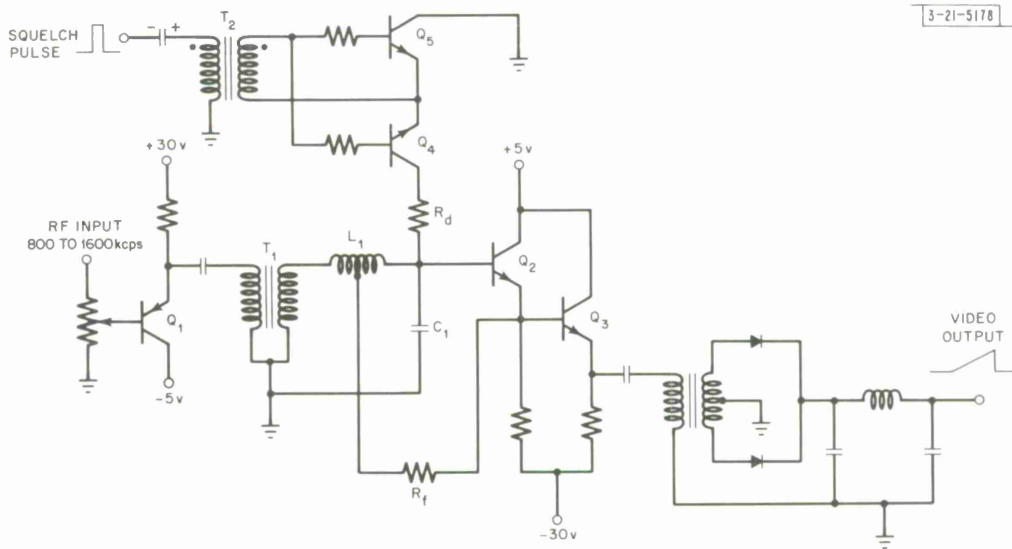
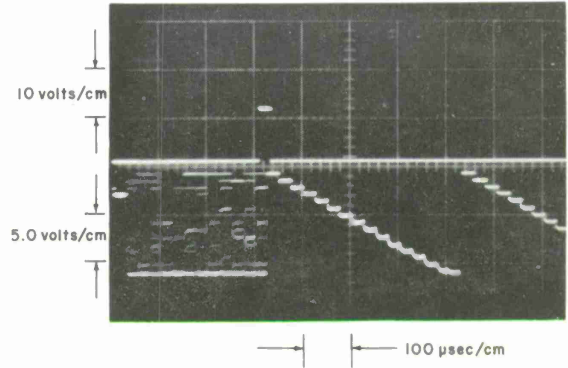


Fig. 39. Matched-filter circuit.

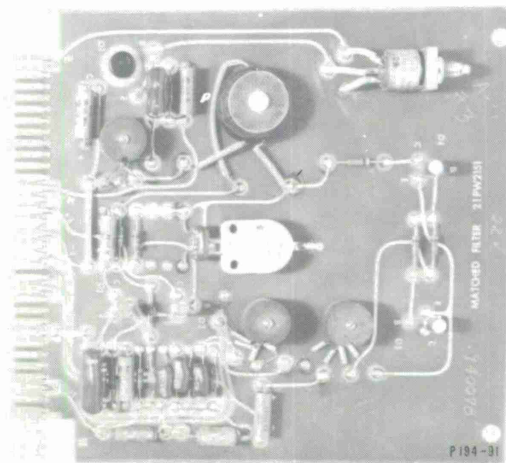
low-pass filter are in the output circuit; these components effectively detect the envelope of the response of the series filter.

In setup, the circuit is excited by a continuous sine wave at the desired frequency; squelch pulses of correct spacing are applied and C_1 is adjusted for resonance; the feedback resistor R_f is adjusted until a linear sawtooth output is obtained. This linear sawtooth time response demonstrates the desired autocorrelation function, as shown in Fig. 3.

A set of 16 matched filters for the 16-level Orthomatch system at a 40-kcps word rate was assembled with nominal 40-kcps spacing in the frequency band from 800 to 1600 kcps. Toroidal inductors of 100, 50, and 25 μ h with Q's varying from 280 to 210 were used. Squelch pulses 1.2 μ sec wide, bracketing at least one cycle of the radio frequency, were necessary to squelch the filters thoroughly. As a result of the finite width of the squelch pulses, transmitter frequencies were spaced 42 rather than 40 kcps apart, in order to obtain optimum time response in intervals between squelch pulses. Tuning a whole set of filters was easiest when a corresponding set of correct transmitter frequencies pulsed on in repeated sequences was used. This sequence of test signals allows observations of each filter's response to adjacent frequencies, and each filter is tuned for minimum response to adjacent frequencies rather than for maximum response to its own frequency. The greater sensitivity of filter frequency response near adjacent-frequency nulls is apparent from inspection of the $\sin x/x$ function in Fig. 2.

The matched filters were wired on printed-circuit cards which fit a standard Lincoln Laboratory logic subrack. A matched-filter card is shown in Fig. 40.

Fig. 40. Matched-filter card.



7. Greatest-Of and Inverter Circuit

The outputs of a bank of matched filters are applied to a "greatest-of" or auction circuit which selects the greatest input and presents logic-level signals to a flip-flop. The greatest-of circuit has M inputs from M matched filters and has separate outputs to M flip-flops, where M is the number of quantization levels of the system. The greatest-of circuits which were built included inverters. The inverters allow application of output logic levels to both the one and zero inputs of flip-flops; this precludes the necessity of resetting flip-flops after each symbol and produces 100-percent duty ratio in flip-flop operation. The greatest-of circuit is shown

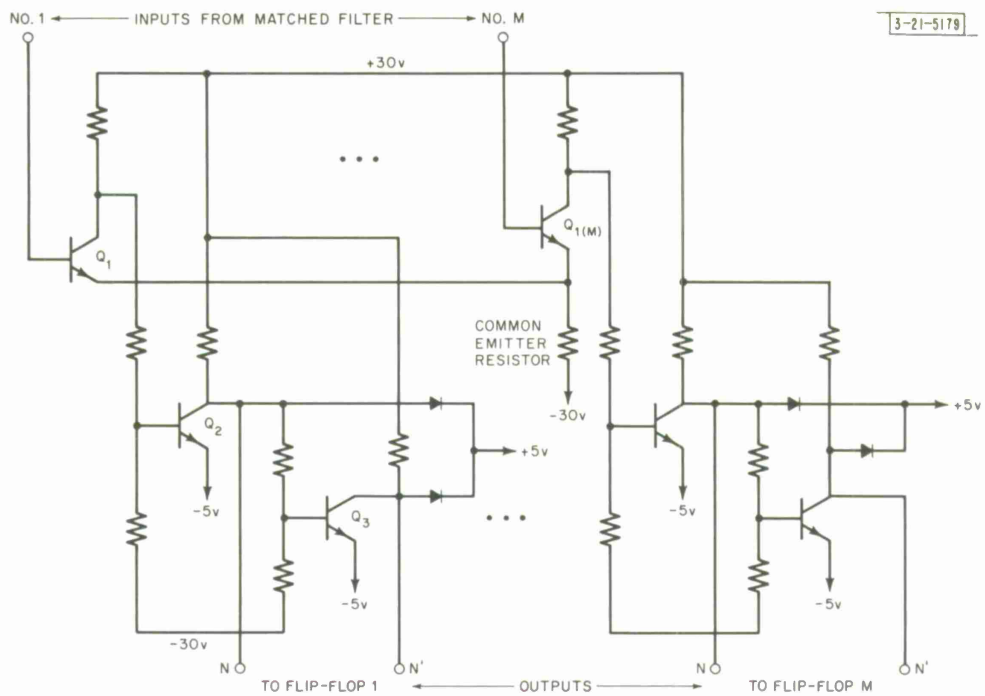


Fig. 41. Greatest-of and inverter circuit.

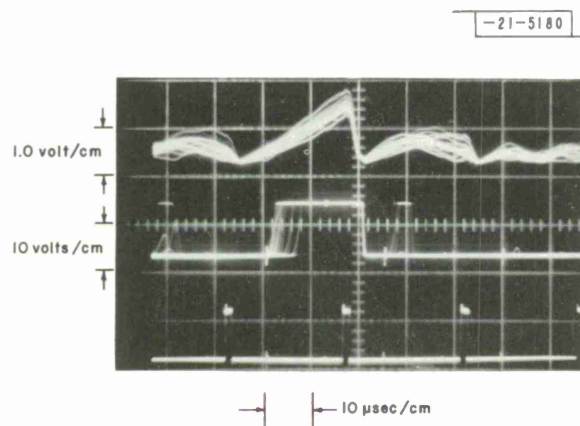


Fig. 42. Output waveforms. $E/N_o \approx 40$.

Upper trace: matched-filter output.
 Center trace: corresponding greatest-of output.
 Lower trace: flip-flop read-in pulses.

in Fig. 41. Greatest-of selection is accomplished by the input transistors, since the transistor with the greatest input current biases off the other input transistors by way of the common emitter resistor. Operation of the input stage is similar to that of a differential amplifier. Approximate matching of the input transistors is required for good results. Transistors Q_2 and Q_3 are saturated amplifiers which convert the output to true and inverted logic levels for application to respective flip-flops.

Figure 42 shows the output waveform of a matched filter, the output of the corresponding greatest-of circuit, and flip-flop read-in pulses. Errors are imperceptible in this display. As the signal-to-noise ratio decreases, the greatest-of output sometimes fails to become true by clock time, and errors result. The flip-flop read-in clock samples the greatest-of waveform after matched-filter peak response and before the greatest-of waveform falls. The delay time of the low-pass filter in the matched-filter output circuit is such that optimum flip-flop timing is obtained by using read-in pulses that have the same timing as squelch pulses.

8. Digital Output

The set of 16 flip-flops (M flip-flops in Fig. 1) constitutes a parallel-digital output register which has a true logic level in only one of the flip-flops. For onward data transmission or digital recording from the Orthomatch receiver, conversion from the parallel format to serial-binary format would allow use of one output lead instead of sixteen. This conversion can readily be made by using straightforward logic and a 160-kcps clock. The frame sync or block start pulse is available from the frame timer section of the receiver.

During tests of the Orthomatch system, serial-binary output was not used. A "ladder" network of scaled resistors was used on the 16 flip-flops to recover the analog voltage originating at the transmitter and to give a convenient oscilloscope display of the receiver's operation.

V. MEASURED PERFORMANCE OF SYSTEM

A. Method

Error rates were carefully measured on the laboratory model and on the field-prototype model of the Orthomatch equipment. These measurements were made to find how well the equipment performed compared with calculated or theoretical performance and to establish signal-to-noise ratios required for safe operation of an actual space-to-ground or other transmission link. The measurements were made by transmitting symbol frequencies in known time slots and counting false-level outputs of the correct receiver flip-flop while varying the signal-to-noise ratio (or E/N_0). Calculated curves were taken from Ward.⁷ "Error rate" is the false output rate divided by the symbol recurrence rate, and E/N_0 refers to a symbol or word, not to a bit.

B. Early Data

Figure 43 is a plot of calculated and measured data for the Laboratory Orthomatch system in which the transmitter signals were converted directly from 7 Mcps down to matched-filter frequencies. Signal and noise were measured at matched-filter inputs by an rms voltmeter. Noise from a broad-band noise source was introduced by way of a band-limiting filter whose equivalent rectangular bandpass was obtained by careful measurement and integration. Signal power was measured directly, and N_0 , the noise power per cycle per second, was calculated by dividing measured noise power by the equivalent square bandpass of the filter. "Greatest-of 2,

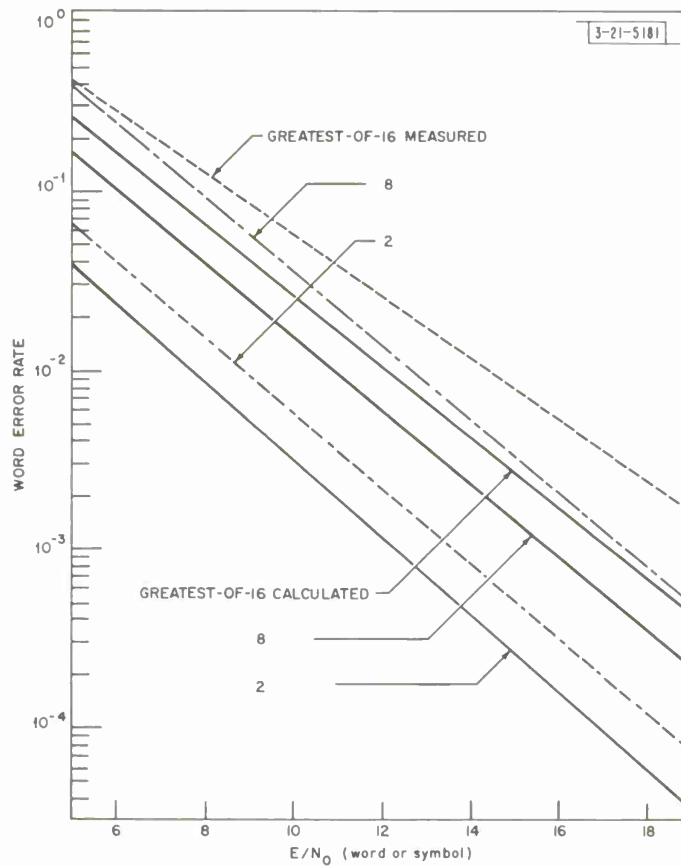


Fig. 43. Error-data orthogonal signals with matched filters (multiple greatest-of comparison, 40-kcps word rate).

4, 8," etc., refers to the comparison of 2, 4, 8 matched-filter outputs in the "greatest-of" comparator. The measured error curves are displaced from the calculated curves by 0.4 to 0.7 db at error rates around 10^{-3} . The above data were taken with correctly phased, jitter-free timing applied to the matched-filter system.

Error data on a greatest-of-4 system, but with timing pulses recovered from the receiver and with AFC-corrected frequency deviation of ± 60 kcps, placed the measured curve 1.6 db above the calculated curve. This showed the effects of jitter in recovered timing and slight de-tuning. In these tests, the laboratory transmitter was operated at 31 Mcps, and the noise source was the front end of the 31-Mcps receiver IF amplifier. Signal and noise were measured at the IF amplifier output, using the IF amplifier as the band-limiting filter. Transmission and reception of synchronization and timing were accomplished by the parallel method outlined in Ref. 1.

C. Data on Later Equipment

1. Test Conditions

Error data measured on the field-prototype transmitter and receiver system are plotted in Fig. 44. The test conditions were:

The word or symbol rate was 40 kcps.

The same set of matched filters described in Sec. V-B was used.

The transmitter and receiver were operated at 2.22 Gcps with components connected as shown in Fig. 45. The noise source was the receiver front end, and signal and noise were measured at the output of the 60-Mcps IF amplifier.

All 16 levels (16 symbol frequencies) were transmitted in sequence by means of a staircase waveform input to the Orthomatch modulator.

The power output of the transmitter frequencies was equalized (during modulator construction) within 0.5-db total range. The synchronization frequency power was nominally equal to the data frequency power. The signal power measured in the receiver IF was the average level of all the transmitter signals.

The matched filters were tuned to the transmitter signals and the matched-filter outputs were leveled nominally.

Error samples for each transmitter frequency and corresponding matched filter were taken, and the errors for all 16 samples were averaged for the data point at each E/N_0 value.

This set of measurement conditions simulated practical operating conditions in a reasonable way, excepting the necessary control of attenuation between the transmitter and receiver.

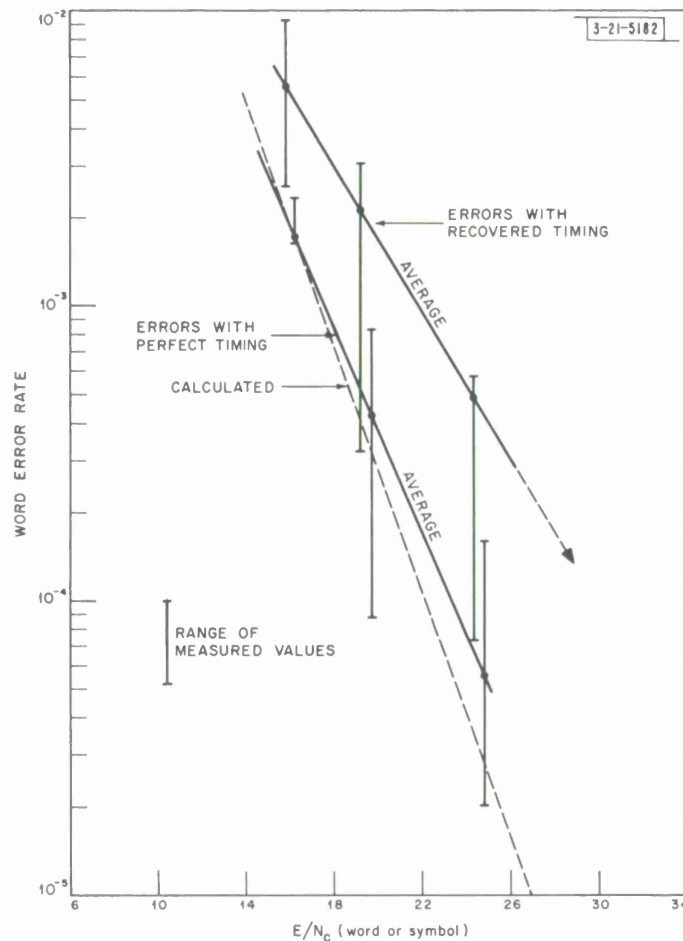


Fig. 44. Orthomatch error rates, 40-kcps word rate (operating from 2.22 Gcps, greatest-of-16 assembly, ± 90 -kcps AFC-corrected deviation).

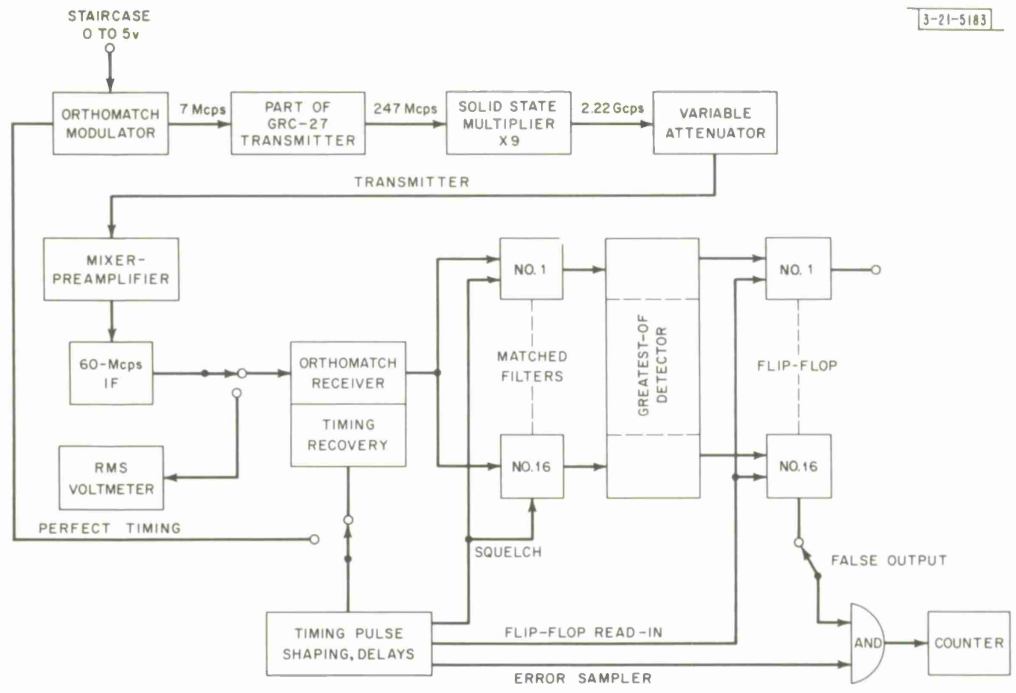


Fig. 45. Test setup for error measurement.

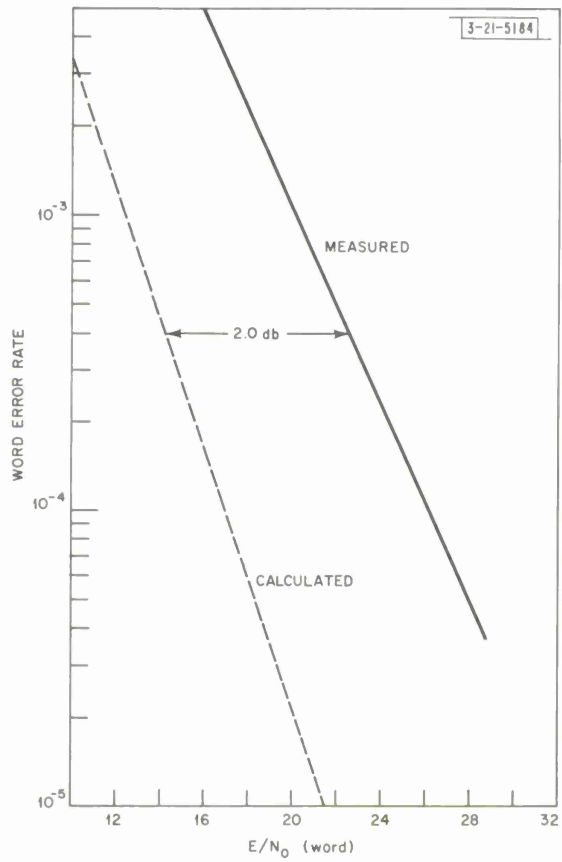


Fig. 46. Matched-filter error rates, 160-kcps word rate (greatest-of-2 comparison, fixed frequency, perfect timing).

2. Results

The average results with perfect timing in Fig. 42 are very close to the calculated error rates, and the average curve with timing recovered from the receiver is approximately one decibel from the calculated curve. This 1-db degradation is due to jitter in the recovered timing which was approximately $\pm 2 \mu\text{sec}$ peak. The data spread over approximately a 1-db range, since it was difficult to maintain precise amplitude stability during these measurements. In addition to the results plotted, it was found that the error rate (with recovered timing) was always less than 10^{-5} when E/N_0 was 38 or more. $E/N_0 = 38$ is 1.5 db above the calculated E/N_0 for a 10^{-5} word error rate.

3. System Threshold

Digital communications systems are, in general, characterized by fairly sharp thresholds² above which the error rate is very small. The errors increase rapidly as the signal-to-noise ratio is reduced below threshold, as can be seen by the slopes of the curves presented in this report. Therefore, a system designer should ensure that his system will operate above threshold, and to do so he needs a reference E/N_0 or S/N to define the threshold. For the 40-kcps Orthomatch system as built and tested, the value of $E/N_0 = 38$ at a 10^{-5} word error rate is taken to be the system threshold.

4. Tests on System at 160-kcps Word Rate

A brief error-test run was made with the Orthomatch system operating at a 160-kcps word rate. The assembly of components shown in Fig. 45 was used; however, only two transmitter frequencies, keyed alternately, and two matched filters were included. The measured error curve in Fig. 46 is 2 db higher than the calculated curve. The additional degradation as compared with the 40-kcps word-rate system was due to:

The amplitudes of the matched-filter outputs were lower than optimum to make the "greatest-of" circuit switch reliably. The matched filters were built for 25- μsec (40-kcps) operation, and their output was low due to less than 6- μsec integration time at 160 kcps.

The rise and fall times of the signal envelopes as observed in the receiver IF were approximately 0.6 μsec each; thus, approximately 1.2 μsec of the 6.25- μsec signal duration were unavailable for integration in the matched filters. This loss was due mainly to response-time limitations of the transmitter components following the Orthomatch oscillators.

The transmitter signals departed slightly from orthogonal spacing, since the correct crystals for the oscillators were not on hand.

5. Summary of 40-kcps Word Rate

The fairly-extensive error tests made on the Orthomatch system at a 40-kcps word rate (160-kcps bit rate) show that practical Orthomatch hardware performs with error rates which are close to calculated or theoretical values. An allowance of 1.5 db above calculated signal-to-noise ratio is sufficient to take care of degradation due to jitter in received timing and AFC-corrected carrier deviations. No degradation due to the use of a high-frequency transmitter, including the solid state multiplier, was observed.

6. Prospects for Higher Word Rates

The results obtained at the 160-kcps word rate can probably be improved 1 db by building matched filters especially for the higher rate and by reducing the response time of the high-frequency components. A multilevel Orthomatch system operating at a 160-kcps word rate would require matched filters operating in the region of 4 Mcps or higher because of 160-kcps spacing between filters. At a 4-Mcps filter frequency, squelch pulses 0.25 μ sec wide would be adequate. The 40-kcps timing recovery system would require improvement for use at 160 kcps, since peak jitter of ± 1 to 2 μ sec would cause considerable degradation in recovery of 6.25- μ sec words. Changes in sync code, gating arrangements, and circuit improvements offer possibilities for improvement of timing. The timing oscillator, data oscillators, and sync oscillators of the Orthomatch modulator are quite suitable, without modification, for use at word rates at least up to 160 kcps. It is estimated that a practical Orthomatch system, operating at a 160-kcps word rate and with 16 or more levels, could be assembled without great difficulty and that it would work within 2.5 db of theoretical performance. Lack of experience with high Orthomatch data rates prevents estimates of performance at word rates above 160 kcps.

VI. SPACE-TO-GROUND SYSTEM

The performance possibilities of an Orthomatch space-to-ground data link will be demonstrated by calculations based on the range equation and practical equipment.

A. Calculations

Calculations of space-to-ground-system operating margins are made in Appendix C, based on 1-watt transmitter power, 3-db transmitting antenna gain, a receiving antenna of 60-ft diameter, a parametric amplifier of 2.5-db noise figure in the receiver front end, and $E/N_o = 38$ for the Orthomatch system at threshold (10^{-5} -word error rate). These system components and values are all practical at 2.2 to 2.3 Gcps. An operating margin of 9.3 db for a 40-kcps word rate, 16-level Orthomatch system is obtained at a range of 10,000 statute miles.

B. Operating Margins

Operating margins or safety margins are required in all systems expected to operate reliably over extended periods of time, particularly if part of a system (a transmitter in space) is inaccessible for servicing or replacement. An operating margin of 10 db is a reasonable requirement for a reliable space-to-ground data transmission link; this 10 db would be expected to compensate for transmitter degradation with time, slight misorientation of antennas, and additional small losses due to errors or omissions in the link calculations.

C. System Variations

System calculations for equipment and systems different than assumed can readily be made by adjustments to the figures in Appendix C. For example, doubling the word rate doubles the power required, doubling antenna size reduces power required by approximately 6 db, halving the range reduces the power required by 6 db. Variations in E/N_o required for different numbers of Orthomatch levels can be obtained from Ward's⁷ curves.

Operating frequency is not explicit in the Appendix C calculations. Operating parameters chosen are directly applicable or are readily adjustable by practical trade-offs to a wide range of frequencies, probably from 100 Mcps to several Gcps.

VII. REVIEW COMMENTS

A. Performance

The calculated signal-in-noise performance of Orthomatch establishes it as a high-performance data transmission system, equal or superior to other available systems. Orthomatch calculated performance is within 10.2 db of Shannon's ideal system. The practical Orthomatch system performance is within 1.5 db of calculated performance and, considering signal power and bandwidth required, the system itself is superior to other available systems such as PAM/FM, PCM/FM, PCM/biphase, and Digilock. In addition, Orthomatch has practical design and construction advantages over these systems. It is capable of high data rates inherently and practically.

B. Suitability of Practical Equipment

The field-prototype transmitter and receiver equipment which has been built and tested through 2.22 Gcps has demonstrated the practical performance mentioned above. The miniaturized Orthomatch modulator has characteristics which adapt it for use with existing telemetry equipment such as time multiplexers and high-frequency converters and amplifiers. It is capable of equivalent bit rates at least as high as 800 kcps. The receiver design, incorporating an efficient set of matched filters, appropriate logic, frequency control, and sync and timing recovery circuits in an appropriate mechanical assembly, has performed very well at the 40-kcps word rate and it can be modified readily for operation at higher rates.

C. Areas for Improvement

Our experience in building and testing the Orthomatch equipment indicates areas for possible improvement. A review of these areas is presented to aid future builders of Orthomatch equipment.

Consideration should be given to alternate methods of card assembly and intercard wiring in the Orthomatch modulator. Difficulties were encountered with wiring between the stacked cards, particularly with the miniature coaxial cable connections (RG 178B/U). These difficulties were due to the size and spacing of the eyelets. The method of wiring and mounting used was chosen to make a rugged assembly. It suffers from the disadvantage that replacement of cards and components is difficult.

Application of the carrier restorer circuit in the receiver AFC loop, which was found necessary during late stages of receiver construction, showed that the narrow-band RF filter, limiter, and discriminator should operate at 21.4 rather than at 10.7 Mcps. This is discussed in Sec. IV-I-2.

The AFC system, operating on pulsed sync signals at approximately 10-percent duty ratio, begins to degrade at a signal-to-noise ratio 4.5 db below data threshold. However, if the frame length is to be extended without proportional increase in sync-code length, the AFC system should be subjected to careful checks for optimization and possible improvement, since the existing margin is not large. Improvement may be obtained by gating sync signals through the AFC IF amplifier. If the sync-code length is increased in favor of reducing jitter in recovered timing, this would result in AFC improvement also. Automatic search and lock accessories for the AFC system were omitted in receiver development; their inclusion may be desirable.

A ± 0.75 - μ sec peak jitter in recovered timing was observed when the signal-to-noise ratio was just above the data threshold. This did not cause a very significant degradation in matched-filter data recovery at the 40-kcps word rate, but reduction of this jitter is indicated for higher word rates. An improvement in lock-on stability in the timing loop may be obtained by adding "guard" bits at the end of the sync code. However, care should be exercised to see that the autocorrelation function of the modified code is not degraded significantly.

D. Modifications in System Operation

1. Number of Levels

The Orthomatch system was assembled and tested with 16 levels of amplitude resolution because this number of levels was considered adequate for many requirements and would result in a fair test of the system. The number of levels can be changed readily by adding or removing transmitter quantizer elements, oscillators, and receiver matched filters. Our experience with 16 levels enables prediction that 32 levels can be operated without difficulty. There is no inherent limit, but an assembly of more than 32 quantizer-oscillator assemblies in the transmitter might be cumbersome. The number of levels may be any number (3, 11, 27, ...) and is not restricted to $2^n = 2, 4, 8$, etc.

2. Data Rates

The Orthomatch system was built and tested at a 40-kcps word rate; only brief tests at a 160-kcps word rate were made. The matched filters used for 40 kcps could be operated at 20 or 80 kcps with only slight modification. Our experience suggests that a 160-kcps, 32-level (800-kcps bit rate) system could be operated with E/N_0 performance only about 1 db worse than the 40-kcps, 16-level system. The Orthomatch modulator is directly suitable for operation at least to the 160-kcps word rate; the matched filters, however, would require redesign to operate at higher frequencies and with higher gain. Operation at high data rates will eventually degrade owing to pulse rise and fall times. At very low data rates, differential frequency stability of oscillators and matched filters will be the important practical consideration.

3. Frame Lengths

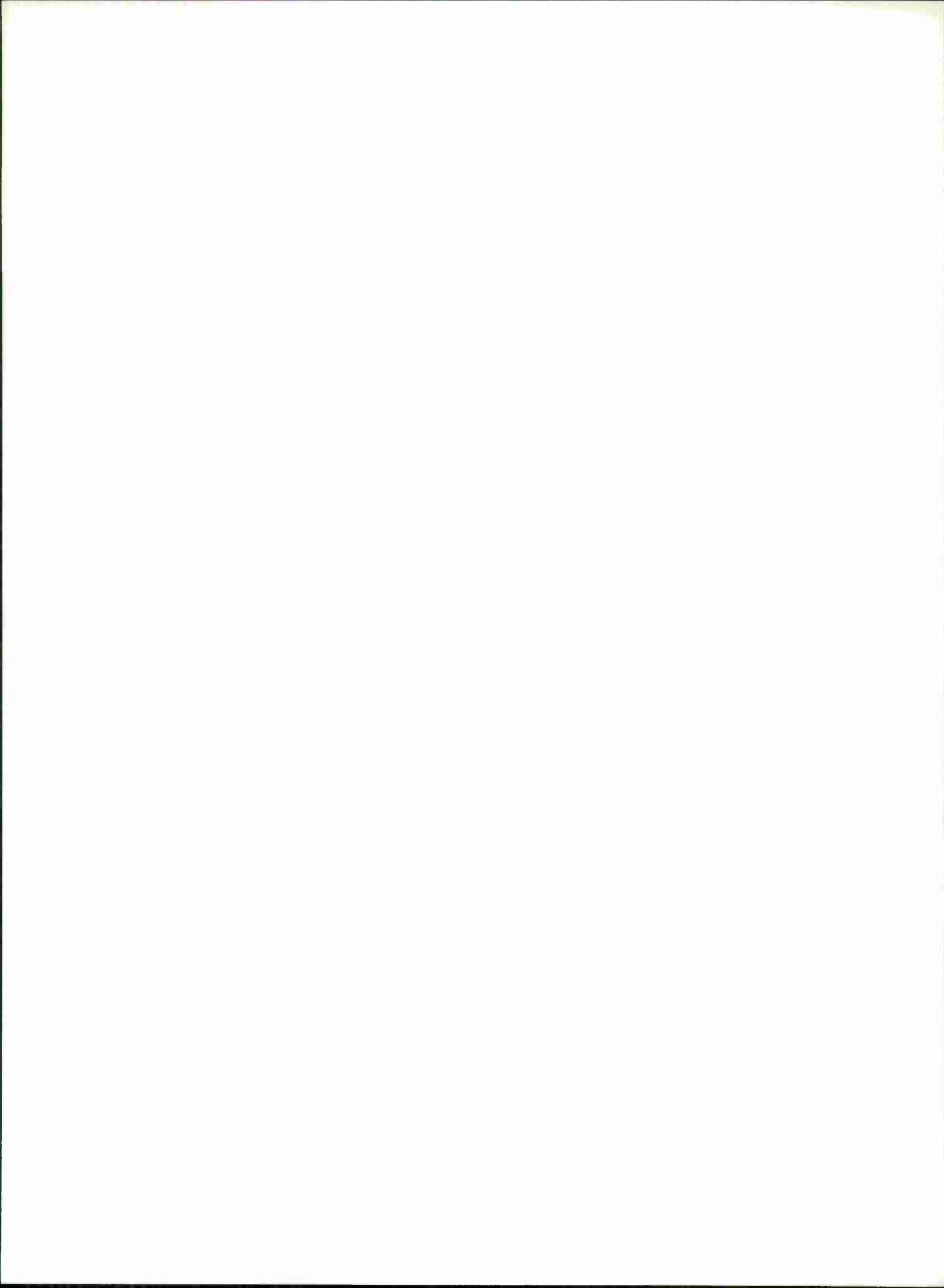
A frame length of approximately 200 data words was required by the satellite system which was originally considered. The Orthomatch system as assembled has 242 data words plus 24 sync words, giving a ratio of sync-to-data time of $24/242 = 9.9$ percent. The sync and timing recovery system has a large margin of safety with this ratio; the AFC system, operating on sync bursts, has a 4.5-db margin. Shorter frames with the same code length can, of course, be used. Frame lengths up to 300 data words with the same code length would probably be safe; longer frame lengths would require improvement of the AFC system or an increase in the code length.

E. Practical Advantages of Orthomatch

Aside from high performance in the presence of noise, Orthomatch has these other practical advantages:

- (1) There is complete flexibility in the number of levels and corresponding amplitude resolution. Any integral number of levels, 7, 11, 15, etc., can be chosen to match the requirement, whereas serial-binary systems such as PCM are restricted to 2, 4, 8, etc., levels.
- (2) Orthomatch has inherent redundancy in the independent data oscillators. Failure of an oscillator may result in loss of only one of M levels, whereas in PCM the failure of the single oscillator results in loss of all levels. However, practical realization of redundancy benefits in Orthomatch will require investigation and establishment of fail-safe (failure with oscillator turned off) operation of the quantizer and oscillator gates.

- (3) Orthomatch pulse techniques are less difficult than in serial-binary systems, because Orthomatch pulses are longer by a factor of three, four, or five (8, 16, or 32 levels) than PCM pulses, and are longer by a factor of eight or sixteen (16 or 32 levels) than Digilock pulses. As data rates increase, loss of signal energy due to rise and fall times is encountered much sooner in the serial systems.



APPENDIX A
SHANNON'S CHANNEL CAPACITY THEOREM

$$C = W \log_2 \left(1 + \frac{S}{N} \right) \quad (A-1)$$

where

C = system capacity, bits per second, for arbitrarily small probability of bit error

W = bandwidth, cycles per second, occupied by system

S = average signal power

N = white noise power .

Introduce

$$\beta = \frac{E}{N_0} = \frac{\text{signal energy}}{\text{noise power per unit bandwidth}}$$

and

$$T = \text{time for one signal bit} = \frac{1}{C} .$$

Therefore,

$$\beta = \frac{STW}{N} = \frac{S}{N} \frac{W}{C} .$$

Let

$$\frac{W}{C} = \alpha .$$

Rewriting Eq. (A-1),

$$\frac{1}{\alpha} = \log_2 \left(1 + \frac{\beta}{\alpha} \right)$$

$$(2^{1/\alpha} - 1) \alpha = \beta .$$

As $\alpha \rightarrow \infty$, $\beta \rightarrow \log_e 2 = 0.693$. Thus,

$$\beta \text{ min} = \frac{E}{N_0} \text{ min} = 0.693$$

for an ideal system with unlimited bandwidth.

APPENDIX B
COMPARATIVE PERFORMANCE OF DIGITAL SYSTEMS

E/N_0 required to send one bit of information at bit error rate = 10^{-6} , 16-level systems (4 bits per level).

System	E/N_0 (bit)		Db Better than Orthomatch (calculated)	RF Bandwidth (160-kcps bit rate) (kcps)	Notes
	Calculated	Measured			
Digilock	6.7	10.6	+0.3	1280	1,2
PCM/biphase	11.0	—	-1.9	640	1,3
PCM (incoherent)	26.2	—	-5.6	800	1
PCM/FM (discriminator detector)	20.8	≈20.8	-4.6	765	1,4
Orthomatch	7.2	10.4	0	880	1,5
Shannon Ideal	0.693	—	+10.2	Indefinitely large	

Notes:

1. For bandwidth, the first side lobes of the modulation spectra have been included. For Orthomatch, an extra guard band of 120 kcps and the spectrum of the sync frequency have been included.
2. An 8-bit code for a 16-level Digilock system has been assumed. The calculated E/N_0 and 2-db degradation for an actual system were taken from Sanders.⁹
3. The PCM/biphase system is the coherent "optimum binary system" referred to by Shaft⁸ and discussed in Sec. III-D.
4. The PCM/FM system uses a discriminator detector and is covered in some detail by Shaft.⁸ A frequency separation of 125 kcps, approximately optimum for a 160-kcps bit rate, is assumed for bandwidth estimate here.
5. Orthomatch E/N_0 (bit) = $\frac{1}{4}E/N_0$ for a symbol or word. Refer also to the discussion in Sec. III-C.

APPENDIX C
SPACE-TO-GROUND SYSTEM CALCULATIONS

I. SIGNAL POWER TRANSMITTED AND RECEIVED

One-way range equation:

$$P_r = \left(\frac{P_t G_t}{4\pi R^2} \right) A_r$$

P_r = power at receiving antenna terminals

P_t = power at transmitting antenna terminals

G_t = transmitting antenna gain

A_r = effective area of receiving antenna

R = range, transmitter to receiver.

A. Normalizing Figures

If $P_t = 1$ watt, $G_t = 1$ (isotropic radiator)

$R = 100$ stat.mi, $A_r = 355$ sq. ft

(27.5-ft-diameter paraboloid, 60 percent effective).

then

$$P_r = -100 \text{ dbw} = -70 \text{ dbm.}$$

B. Example

Satellite at 2000-n.mi altitude, 5° elevation angle.

Slant range = 4520 stat.mi.

Satellite antenna gain = +3 db.

Receiving antenna = 60-ft-diameter paraboloid.

Corrections to normalized P_r above:

$$\text{Range } 10 \log_{10} \left(\frac{100}{4520} \right)^2 = -33 \text{ db}$$

Satellite antenna gain +3 db

$$\text{Receiving antenna gain } 10 \log_{10} \left(\frac{60}{27.5} \right)^2 = +6.8 \text{ db}$$

Include transmitter line and isolator loss -1.5 db

Include receiving line loss -0.3 db

Total correction = -25 db.

Then received power at input terminals of receiver RF preamplifier = -70 dbm -25 db = -95 dbm for a one-watt transmitter.

II. RECEIVER NOISE

$$T_{\text{eff}} = T_A + (L - 1) T_L + LT_r$$

T_A = sky noise temperature. Assume 85°K at 5° elevation.

L = line-loss factor between antenna and parametric amplifier.
Assume 0.3-dB loss, and $L = 1.07$.

T_L = noise temperature of line. Assume 300°K.

T_r = noise temperature referred to parametric amplifier input,
due to noisiness of parametric amplifier itself. Assume
2.5-dB noise figure. Then $T_r = (F - 1) T_o = 233^\circ\text{K}$.

T_{eff} = noise temperature referred to parametric amplifier input,
due to sky, line and parametric amplifier.

$$\begin{aligned} T_{\text{eff}} &= 85^\circ + (1.07 - 1) 300^\circ + 1.07 \times 233^\circ \\ &= 85^\circ + 21^\circ + 247^\circ = 353^\circ\text{K}. \end{aligned}$$

Assume noise contribution of succeeding receiver stages (mixer, etc.) = 13°K. Then

$$\text{over-all } T_{\text{eff}} = 366^\circ\text{K}$$

$$\begin{aligned} N_o &= \text{noise power/cps} = KT_{\text{eff}} \quad (K = 1.38 \times 10^{-23} \text{ joule/}^\circ\text{K}) \\ &= 5.05 \times 10^{-21} \text{ watt/cps} \\ &= -203 \text{ dbw/cps} = -173 \text{ dbm/cps}. \end{aligned}$$

III. SIGNAL-TO-NOISE-RATIO REQUIREMENT

$$(a) \ E/N_o = \frac{ST}{N_o}$$

where

T = pulse duration
= word length in Orthomatch system

S = signal power

N_o = noise power per cycle per second.

(b) In the 16-level Orthomatch system operating at a 10^{-5} word error rate,
 $E/N_o = 38$ is required. For a 40-kcps word rate system, $T = 25 \mu\text{sec}$ and

$$S/N_o = \frac{38 \times 10^6}{25} = 1.52 \times 10^6 \rightarrow +61.8 \text{ db} \quad .$$

For a 160-kcps word rate system, $T = 6.25 \mu\text{sec}$ and

$$S/N_o = \frac{38 \times 10^6}{6.25} = 6.1 \times 10^6 \rightarrow +67.8 \text{ db} \quad .$$

(c) If $N_o = -173 \text{ dbm/cps}$ as calculated in Sec. A-II, and if a 10^{-5} word error
rate or better is required, minimum signal power is:

40-kcps word rate, 16-level system
 $S = -173 \text{ dbm} + 61.8 \text{ db} = -111.2 \text{ dbm}$

160-kcps word rate, 16-level system
 $S = -173 \text{ dbm} + 67.8 \text{ db} = -105.2 \text{ dbm}$

These values of signal power offer no operating margin.

IV. SUMMARY FOR ONE-WATT TRANSMITTER

Under the conditions given in Sec. A-I-B, a one-watt transmitter gives an operating margin of $-95 - (-111.2) = 16.2 \text{ db}$ for a 40-kcps, 16-level Orthomatch system, and a margin of 10.2 db for a 160-kcps, 16-level Orthomatch system.

The 40-kcps, 16-level margin is 9.3 db at a range of 10,000 statute miles and 3.3 db at 20,000 miles.

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