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Final Report
Development and Fabrication of a 5 Kmc Electrochemical Switching Transistor

January 15, 1961 to April 14, 1962

Subcontract No. 242

Prime Contract No. AF 13(604)-7400

PREFACE

This is the Final Report on MIT Lincoln Laboratories Subcontract No. 242 (Prime Contract No. AF-19(604)-7400), for the DEVELOPMENT AND FABRICATION OF A 5 KMC ELECTRO-CHEMICAL SWITCHING TRANSISTOR. This report covers the period from January 15, 1961 to April 14, 1962.

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SECTION I

PURPOSE

The purpose of this contract was to conduct a research program relative to the development of a 5 KMC ELECTROCHEMICAL SWITCHING TRANSISTOR. The Lansdale Division of the Philco Corporation furnished the personnel, material, and facilities required for this program.

Upon completion of the research and developmental work, the Lansdale Division delivered twenty-five (25) transistors having the highest f_t's achieved during this program.

SECTION II

SUMMARY

This report describes the theoretical and experimental investigations which were performed by Philco Corporation, Lansdale Division, to fabricate a germanium transistor exhibiting an f_t of 5 Kmc/sec. Standard electrochemical methods with some necessary modifications were employed to fabricate the transistors. The intrinsic f_t of the fabricated transistor was determined to be 5 Kmc or greater but, due to an electrical interaction between the passive elements in the transistor and the TO-18 enclosure, useful measurement of this quantity could not be made. Recommendations are made for future work involving investigation of the influence of f_t on switching speeds, more accurate definition of relationship between measured f_t and device parameters, development of advanced transistor structures, and design and construction of a suitable enclosure for high speed devices.

SECTION III

FACTUAL DATA

Initial Work

Extensive prior experience with high frequency germanium MADT devices indicated that improvements could be made in two parameters to extend the state of the art in ultra-high frequency transistors:

1. A reduction in the emitter transition capacitance would result in a higher level of f_t at a lower current than that at which the f_t peak had occurred on the existing MADT devices.

2. A reduction in the electrical basewidth would substantially increase the f_t by reducing that part of the total delay time that is associated with the base region of the MADT structure. Since the time delay is directly proportional to the square of the electrical basewidth, a reduction in electrical basewidth by a factor of 3 to 5 would reduce base transit time by a factor of 9 to 25 (assuming the same field enhancement and diffusion rate in the base region).

To accomplish reduction of both C_{TE} (emitter transition capacitance) and ω_b (electrical basewidth) a PINIP structure

was proposed. A theoretical analysis of the PINIP was performed and the results were described in the Final Report, MIT Lincoln Laboratories Subcontract 215 AF-19(604)-5200, PINIP Transistor Material Study. It was shown in this report that a PINIP structure could accomplish the reduction of C_{TE} and ω_b. A thin (0.00001") etched blank of low resistivity germanium was to be coated with high resistivity germanium, the high resistivity layer providing for capacity reduction while maintaining reasonable breakdown voltages of the associated P-N junctions.

Several metallurgical problems had to be solved to permit the fabrication of the PINIP structure. These problems were:

1. Electrochemical etching of a low resistivity germanium blank to a final mechanical thickness of 0.00001", and

2. Achievement of a smooth, single crystalline growth of high resistivity germanium upon the thin etched blank, with the additional requirements that no appreciable diffusion take place during the growth period, and the thickness of the grown layers be precisely controlled (±0.000003 inch),

or a means be provided for subsequently etching the intrinsic regions to such high accuracy.

The first problem was solved by monitoring with infrared transmission during blank etching. This technique, employing electrochemical jet etching, utilizes a chopped infrared light source. The chopping serves to provide noise isolation from the 60-cycle source for high signal-to-noise a-c amplification and also permits a comparison of the control signal with a blank thickness independent signal. The etching operation is interrupted when identical amounts of energy are received by the monitor detectors associated with the control and reference filters. Etched germanium blanks of 0.00001" thickness were obtained, as evidenced by observing the color of transmitted light (orange).

Several systems were considered in detail for the intrinsic layer growth and have been described in the Final Report, MIT Lincoln Laboratories Subcontract 215 AF-19(604)-5200, PINIP Transistor Material Study. Of the systems considered, only solution growth produced smooth layers at temperatures low enough to preclude any diffusion from the low resistivity substrate blank. All high temperature

systems exhibited growth rates of the same order as diffusion rates. The disproportionation of germanium diiodide (another low temperature system) could not be utilized for fabricating transistors because it produced a rough and faceted grown layer surface.

It was not possible, however, to control the solution growth thickness of the intrinsic epitaxial layer to the degree desirable (0.000003 inch), but ±0.00005 inch was typically obtained. Prior to the initiation of an intensive effort to more precisely control the absolute thickness of the intrinsic layers, a study of the electrical effects of the intrinsic emitter was performed.

To accomplish the experimental evaluation of the intrinsic emitter, an intrinsic layer of germanium was grown by the solution growth technique upon a diffused-base germanium blank. The emitter pit had been etched prior to the deposition of the layer and the emitter breakdown voltage was recorded. By measuring the thickness of the grown layer and the change in emitter breakdown voltage on the diffused-base substrate, the resistivity of the layer was determined to be greater than 10 Ω-cm. The electrical properties of the

diffused-base substrate were very precisely known from conventional MADT work. Thus, the effect of the intrinsic emitter was determined by observing the difference between structures with and without the epitaxial layer. The conclusions from this study are:

1. The intrinsic emitter layer has no beneficial or detrimental influence on the injection efficiency of the transistor in which it is incorporated.

2. The emitter transition capacitance of the intrinsic emitter was reduced as expected. However, the reduction in capacitance was accompanied by an additional delay time through the transition region. The delay time is proportional to the square of the intrinsic layer width, and the delay time due to capacitance is inversely proportional to the layer width, hence a design compromise of the layer thickness was necessary. Even though calculations of the compromise showed that an improvement in the low current f_t of the MADT structure could be achieved, continued evaluation of MADT-type transistors pointed to the fact that a transistor could be designed so that the base and collector depletion layer widths could be maintained small to a level

of current where the C_{TE} delay time was negligible. Thus, the difficult intrinsic emitter approach was abandoned.

Conclusions of MADT Evaluations

Several important points led to the conclusion that the transistor structure could be changed so as to permit the operation of the transistor at higher currents where C_{TE} delay time is negligible. That C_{TE} delay time can be negligible is shown by the equations below.

C_{TE} delay time $= 2\pi r_e C_{TE}$, (where the emitter diode resistance, $r_e = \frac{kT}{qI_e}$),

$$= \frac{2\pi kT}{q} \frac{C_{TE}}{I_e} .$$

Hence, as I_e is made large enough, this delay time is negligible.

The important points relating to high current operation mentioned above are:

1. For a PNIP transistor with a given breakdown voltage, the f_t can be limited by the transit time in the collector depletion layer. This is because the depletion layer width at the breakdown voltage is approximately the

same as at the operating voltage, and if a narrower depletion layer is desired, the breakdown voltage must be lowered. No benefits are to be derived by lowering the operating voltage and hence the depletion layer width, because the electrical basewidth widens as the applied voltage is lowered.

2. For a given breakdown voltage, the thinnest collector depletion layer is obtained with the highest resistivity bulk germanium between the base diffusion and the rectifying collector contact. Because of the high bulk resistivity, however, the effect of current modulation of the collector depletion layer causes the basewidth to widen and f_t to decrease with current.

Consideration of the above points made apparent the need for a modification of the NIP base-collector junction to permit the base and collector regions to be less affected by current density. This modification was to change from the NIP to an NP collector where the P-region resistivity was higher than the recrystallized contact used in the NIP structure.

Examination of the cause of the rapid rate of basewidth increase with current showed that the flow of current tended to make the depletion layer fixed charge be more N-type. Hence, the less N-type, or the more P-type, this region, the higher the current density at which detrimental effects would be observed. Consequently, higher f_t transistors could be fabricated, since the emitter delay could be made negligible.

To incorporate the N-P base collector junction in the 5 Kmc transistor design required a modified fabrication technology. This modified fabrication technology has been described in detail in the Third Quarterly Report. In principle, the fabrication scheme used was very similar to the electrochemical jet etch and plate technique used in the manufacture of high frequency MADT transistors.

Microlayer Transistor

Processing of the microlayer transistor presented the need for an N-P junction with the following significant characteristics:

1. The junction transition region should be as thin as possible consistent with breakdown voltage requirements. This would assure a thin collector depletion layer width at low applied voltages.

2. The thickness and resistivity of the N-P junction should give an electrical basewidth $\leq$0.00001" at a low applied voltage (3 to 5 volts).

These desired characteristics of the N-P junction placed stringent requirements on the metallurgical methods to be used. Both epitaxial and diffusion techniques were considered, and initial calculations based on known rates of growth and diffusion showed a steeper base region could be obtained by epitaxial methods. These calculations assumed the metallurgical quality of the grown junction was not dependent upon the growth temperature. However, later work showed that growth temperature was an important factor and that, in fact, good quality growth could not be obtained at low temperatures. The solution growth system, an excellent low temperature system for epitaxial deposition of highly doped or intrinsic germanium, does not lend itself to accurate control of the intermediate dopant concentrations

required in the microlayer transistor. Therefore, only diffusion and epitaxial growth between 700°C and 850°C were used. The epitaxial growth system employed was the hydrogen reduction of germanium tetrachloride.

Analysis of the first transistors produced by both diffusion and epitaxial techniques indicated that an unexpected diffusion was occurring concurrently with the epitaxial growth. The electrical measurements of the epitaxial junction showed that a gettering of dopant impurities from both the N and P sides of the junction was occurring at the substrate-epitaxial layer interface. The gettering action was explained by the presence of a polycrystalline or amorphous germanium layer at the interface. The non-single-crystalline layer could accommodate diffusion of both dopants into it because of the usual increased solid solubility attributed to polycrystalline material as compared with single crystal material. As a result of this gettering action, there was a depletion of dopant on both sides of the junction, thus causing a severe departure from desired junction characteristics.

The accumulation of gettering layers was believed to be caused by the reduction by hydrogen of germanium dioxide (which must be removed or reduced) to amorphous germanium on the substrate surface prior to growth. The amorphous germanium layer provided non-uniform single crystal nucleation and the initial growth was locally polycrystalline. At a later stage of the growth process the single crystal characteristics of growth predominated.

To eliminate the gettering difficulty, the germanium dioxide was removed in an inert ambient (helium) at the temperature of the subsequent epitaxial growth. The inert ambient treatment permitted the relatively slow germanium-germanium dioxide reaction to proceed, forming volatile germanium monoxide. This treatment left a clean single crystal surface, permitting uniform nucleation and growth of the single-crystal N-type epitaxial layer.

As a result of the improved growth quality achieved by this surface treatment, there was no gettering action, and hence no barrier to diffusion through the interface. The grown junctions thus formed were comparable to those obtained by diffusion alone. Electrically similar units were obtained

by epitaxial growth or diffusion of the base-collector junctions. As anticipated, the N-P junctions of the associated transistors were relatively unaffected by current densities above the level at which the C_{TE} time delay was an important consideration. Consequently, it was apparent that further efforts to keep the base-collector junction position constant to higher values of current density would not improve the f_t of the structure. Thinner electrical basewidths and collector depletion layer widths were necessary, maintaining those thinner widths up to the current level where C_{TE} was not an important limitation.

Achievement of a thinner depletion layer width at a given applied voltage increases the maximum electrical field at the junction and hence lowers the breakdown voltage of the transistor. Thinner collector depletion layers were obtained by using lower resistivity P-type collector material, the lowest usable resistivity being 0.05 Ω-cm. This low resistivity material produced diode breakdown voltages in the range of 10 to 15 volts.

Thinner basewidths were obtained by emitter placement on the N-type base at a location where the punch-though voltage

was equal to or slightly less than the collector breakdown voltage. To accomplish the controlled etching of the emitter pit, a technique employing depletion layer monitoring was developed. The technique of depletion layer monitoring has been described in the Third Quarterly Report.

In principle, the depletion layer monitoring technique involves observing an increase in the collector diode saturation current during the emitter etching. The voltage at which an effective current gain is evidenced during the a-c sweep of an oscilloscope is precisely the voltage at which collector-to-emitter punch-through occurs. By locating the emitter junction at the position of collector-emitter punch-through, it was possible to obtain the minimum electrical basewidth (in principle, zero basewidth at the punch-through voltage) for a given applied voltage.

Technical Results

Using the technique of depletion layer monitoring, along with controlled growth or diffusion into low resistivity germanium, extremely thin regions (electrically) were achieved between the emitter and collector junctions. The maximum f_t obtained was 2600 mc.

Electrical data on the 25 best transistors sent to MIT are presented in the appendix to this report.

The task of investigating the factors contributing to the f_t limitation of 2600 mc was divided into two areas:

(1) Impurity control and fabrication

(2) Measurement.

The degree of impurity control was considered together with fabrication because of their mutual interdependence. It was desirable that the transition region of the collector-base junction be made narrower so that the base and depletion layer widths would be narrower at low voltages. The transition region width could not be decreased if accompanied by an increase in collector capacitance. Since the depletion layer of the base-collector junction was to be decreased to lower the delay time, the collector capacitance would increase unless a corresponding reduction in collector-base area could be obtained.

A fabrication problem prevented decreasing the collector-base area relative to the emitter (a factor already governing the maximum usable current density). This problem was

concerned with isolation of the base-collector junction by electrochemical moat etching around the collector metallic contact. To maintain low extrinsic r_b' and to provide a structure of adequate mechanical strength, it was necessary that 0.00005" remain between the N-type surface of the blank and the diffused or grown base-collector junction. The isolated collector junction had to be larger than the emitter junction to realize as close (<0.00005") a location of the emitter to the base-collector junction as permitted by the impurity distribution. In addition, the minimum distance of 0.00005" from the surface for the base-collector junction precluded arbitrary choice of the impurity distribution.

Several other techniques were considered which could possibly alleviate the above-mentioned compromise of relative emitter and collector areas; however, none successfully accomplished the desired improvement in the impurity control and fabrication compromise.

Among the techniques tried were:

1. Moat etching the base-collector junction from the emitter side of the structure and making base contact in

the N region within the moated area. This resulted in a larger base resistance and, more importantly, a larger collector-to-emitter area ratio.

2. Fabrication of a ring emitter and a concentric ring collector by selective etching and alloying. No usable transistors were produced by this technique.

Of the techniques used in the fabrication of high f_t transistors, the microlayer technique proved the most reproducible and provided the highest frequency transistors on both diffused and epitaxial junctions.

Measurements of Fabricated Devices

Extensive measurements of many microlayer transistors support the following observations:

1. Measurements of h_{fe} at frequencies below f_t lack correlation; they do not show the theoretically expected change of 6 db/octave. The bias used during h_{fe} measurement is a primary factor in determining the direction and magnitude of departure from a change of 6 db/octave. For high voltage and low current, the fall-off in h_{fe} with increasing frequency is greater than the theoretical -6 db/octave. For

low voltage and high current, the fall-off in h_{fe} with increasing frequency is less than -6 db/octave.

2. There is a frequency at which the h_{fe} is greater than that obtained at measurement frequencies either slightly higher or lower.

3. By tuning the output line of the Transfer-Function Bridge (G.R. Model 1607-P102), it is possible to maximize the observed h_{fe} at any measurement frequency other than the frequency at which the greatest h_{fe} is obtained as stated in 2, above. At maximum h_{fe}, the length of the tuned output line is either the same or shorter (more capacitive) than that obtained at the original short circuit calibration.

4. Varying the position of the TO-18 transistor enclosure in the testing socket of the Transfer Function Bridge gives a decrease in the measured h_{fe}. However, the h_{fe} value that is observed with the transistor enclosure close to the Transfer-Function Bridge can be obtained with the transistor a small distance away from the socket by a readjustment of the output line. This tuning or readjustment of the output line again involves making it shorter.

5. Measurements which were made by Lincoln Laboratories on microlayer transistors showed an anomaly in

correlation of h_{fe} measurements at 80-100 mc/sec. This anomaly was interpreted to be due to an R-L-C tuned circuit interaction.

On the basis of the observations cited above, there does appear to be an effect of tuned circuit coupling which causes h_{fe} measurement results to be different than expected. The maximizing of h_{fe} by making the output line of the Transfer-Function Bridge more capacitive indicates at least an L-C coupling.

In an effort to more accurately define the true limitations of f_t, a transistor structure (Figure 1) was fabricated with two ohmic contacts to the collector-base junction. The series resistance ($r_{c'}$) to the collector-base junction is different for the two contacts. The emitter and base contacts are each 0.001" in diameter and are placed within 0.001" of each other. (The base-collector junction is isolated from the emitter side of the blank.) The electrical basewidth of this structure was controlled to be less than 0.00002" at any applied voltage.

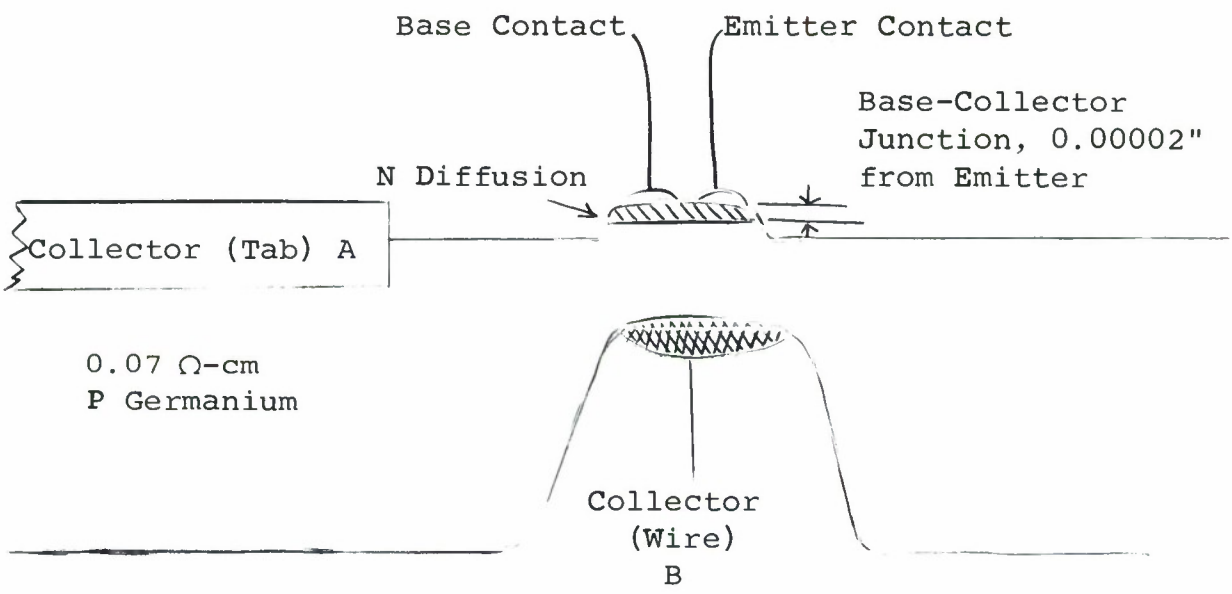

Figure 1. Two Collector Contact Transistor.

Using this structure, it is possible to measure f_t (h_{fe}) with all parameters identical except the series resistance of the collector (also slight difference in series inductance due to wire and tab). This transistor had a large collector capacitance but showed that the difference in f_t (f_t being about 1-300 mc) was due to the difference in the series resistance of the two collector contacts.

In order to test whether series resistance and capacitance could be limiting f_t in the microlayer transistor, and whether the inductive interactions were preventing measurement of the "intrinsic f_t", several 2000 mc f_t

(calculated from 200 mc measurement) units which exhibited the high h_{fe} anomaly at 100 mc were measured as follows:

a. Peak f_t measured at 100 mc with transistor enclosure close to transfer function bridge socket,

b. Peak f_t measured at 100 mc with transistor enclosure 3/8" out of socket. Output line tuned to maximize f_t,

c. C_{ob} was measured at the same bias point as in a and b,

d. f_t and C_{ob} measured with 30 Ω resistance in series with collector lead. Additional voltage was supplied to account for the drop across the 30 Ω resistance.

The data obtained from these measurements is given in Table I.

TABLE I

SERIES RESISTANCE MEASUREMENTS

Transistor	f_t (mc)	f_t at 200 mc/sec.	Cob (pf)	V	Ie	Proximity to Bridge Socket	Added Series Resistance
11	3040	2020	2.75	4.3	30	Close	None
11	3050	----	2.78	4.3	30	Away 3/8"	None
11	1075	----	2.69	5.2	30	Away 3/8"	30.6 Ω
11	----	----	4.52	4.3	--	Away 3/8"	None
9	3300	2100	2.70	4.3	30	Close	None
9	3290	----	2.85	4.3	30	Away 3/8"	None
9	2000	----	2.89	4.6	30	Away 3/8"	10.1 Ω
9	1140	----	2.89	5.2	30	Away 3/8"	30.6 Ω
9	----	----	4.75	4.3	--	Away 3/8"	None

Conclusion of Measurements

It is assumed for the moment that the h_{fe} which is measured at the resonant frequency (100 mc for the microlayer transistor) is controlled by the $r_{c'}C_c$ product. If the h_{fe} as determined is a measure of the $r_{c'}C_c$ product, then the "intrinsic f_t" can be calculated.

$$\frac{1}{f_tm} = \frac{1}{f_ti} + 2\pi r_{c'}C_c,$$

where

f_tm = f_t measured at 200 mc,

f_ti = f_t (intrinsic) excluding $r_{c'}C_c$.

For transistor 11, assuming

$$2\pi r_{c'}C_c = \frac{1}{3040},$$

$$\frac{1}{f_ti} = \frac{1}{f_tm} - \frac{1}{3040} = \frac{1}{2020} - \frac{1}{3040} = \frac{1}{5700},$$

or "intrinsic f_t" = 5700 mc/sec.

For transistor 9,

$$\frac{1}{f_ti} = \frac{1}{2100} - \frac{1}{3300} = \frac{1}{5800},$$

or f_ti = 5800 mc/sec.

An obvious difficulty exists in the choice of f_t to be used as f_tm. The 200-mc readings were chosen because of the

close agreement between measurements made by Lincoln Laboratories at 170 mc and by Philco at 200 mc.

If the resonant frequency measurement is controlled by $r_c' C_c$, then the f_t obtained with different added series resistances should be proportional to the series resistance plus the built-in resistance. Some justification for the assumption that $r_c' C_c$ is measured at the resonant frequency is obtained by calculating the built-in series resistance (r_c'). If r_c' is calculated to be the same with different values of added series resistance, then the assumption is a valid one. r_c' can be calculated by

$$\frac{1}{f_t(r)m} = 2\pi r C_c,$$

where $r = r_c' + R$ added,

then

$$\frac{f_t m(r_c')}{f_t m(r_c' + R)} = \frac{r_c' + R}{r_c'} .$$

The results of this calculation are given in Table II.

TABLE II

CALCULATIONS OF $r_{c'}$

Transistor	$f_{tm}(r_{c'})$	$f_{tm}(R + r_{c'})$	$r_{c'}$
11	3040 mc	1075 mc (30.6 Ω)	16.6 Ω
9	3300 mc	2000 mc (10.1 Ω)	15.6 Ω
9	3300 mc	1140 mc (30.6 Ω)	16.2 Ω

As an additional justification for the assumption that $r_{c'}C_c$ is measured at the resonant frequency, the frequency limitation for the $r_{c'}C_c$ is calculated using the above determined $r_{c'}$ and the previously measured C_c. The results of this calculation are given in Table III. Close agreement is again noted.

TABLE III

MEASURED AND CALCULATED $r_{c'}C_c$

Transistor	$\frac{1}{2\pi r_{c'}C_c} = f_t(\text{calc.})$	f_{tm}
11	3410	3040
9	3540	3300

SECTION IV

CONCLUSIONS

Based on the above measurements and calculations, it is concluded that the microlayer transistor has a sufficiently high "intrinsic f_t" (about 5-6 Kmc), but that the $r_{c'}C_c$ product limits its measurement and use. All efforts which were directed toward decreasing the electrical base and depletion layer widths using the diffusion or epitaxial processes resulted in compromise between the transit time reduction and capacitance increase. In addition, it is concluded that the TO-18 package is not suitable for ultra-high frequency measurements. The effects of f_t, $r_{c'}$, **L,** and C_c upon transistor switching speed were not determined during this contract period.

SECTION V

RECOMMENDATIONS FOR FUTURE WORK

1. Investigate the influence of f_t in switching operations, with particular emphasis being placed upon capacitive and inductive effects.
2. Determine more accurately, if possible, the relationship between measured f_t and device parameters.
3. Design and fabricate a transistor structure in which the limitations of all presently available transistors are reduced to an absolute minimum.
4. Design and build a transistor enclosure which does not interact with switching transistor properties.

APPENDIX

D-C PARAMETERS

A-C PARAMETERS

D-C PARAMETERS

No.	β_1 1v	β_{10} 1v	β_{25} 1v	β_{50} 1v	BV_{CBO} 100 μa volts	V_{CE}^{SAT} 1ma, 10ma mv	V_{BE} 1ma, 10ma mv	I_{CO} 5v μa
14	32.	46.	50.	50.	9.5	97.	390.	.09
15	28.	33.	33.	31.	11.5	96.	392.	.085
16					3.0			1400.
17	19.	26.	29.	29.	6.8	93.	396.	.57
18	8.4	13.	15.	16.	12.9	157.	423.	.028
19	28.	37.	39.	40.	12.9	106.	401.	.042
20	4.5	8.	8.	9.	6.7			51.
21	12.	16.	15.	15.	12.8	141.	408.	.62
22	11.	15.	17.	17.	13.0	154.	425.	.17
23	12.	14.	14.	14.	11.8	175.	417.	3.2
24	6.2	11.	13.	13.	12.9	224.	319.	.11
25	10.	16.	17.	14.	12.9	127.	404.	.036
26	11.	20.	23.	24.	4.4	92.	376.	142.
27	11.	17.	18.	18.	8.8	108.	388.	.074
28	15.	19.	21.	23.	11.6	124.	395.	15.2
29	17.	22.	23.	23.	12.3	117.	396.	3.95
30	52.	46.	43.	44.	2.5	82.	382.	273. (3v)
31	37.	42.	43.	50.	11.7	121.	394.	.22
32	13.	22.	26.	29.	12.1	155.	419.	.18
33	8.	18.	25.	29.	15.0	141.	426.	.072
34	20.	31.	39.	48.	16.1	127.	406.	.10
35	14.	21.	25.	28.	16.3	135.	420.	.10
36	20.	35.	42.	46.	15.0	113.	380.	.14
37	26.	48.	63.	72.	9.0	100.	389.	.11
38	5.3	6.7	7.	6.	12.9			.032

A-C PARAMETERS

No.	0V, 1 Gc Low I_c ma	1V, 1 ma f_t Gc	1V, 20 ma f_t Gc	3V, 30 ma f_t Gc	1V, 50 ma f_t Gc	0V, 1 Gc High I_c ma	3V, 1 mc C_{ob} pf	3V, 1/2 ma r'_b Ω	2 ma K's p coul ma	Lum τ_s p coul/ma
14	21.	0.43	1.6	2.0	1.6	21	4.56	12.9	28	7
15	7.7	0.41	1.7	2.1	1.8	85	3.80	17.4	25	6
17	6.8	0.36	2.0	2.2	2.1	106	3.72	17.3	25	4
18	7.1	0.37	1.8	2.2	1.9	92	4.38	14.5	25	4
19	8.6	0.40	1.8	2.2	1.9	84	4.44	16.3	25	4
20	11.3	0.32	1.6	1.9	1.8	140	5.18	16.1	25	3
21	14.0	0.35	1.7	2.0	1.8	101	5.29	15.0	25	3
22	11.0	0.41	1.7	2.2	1.9	87	5.13	13.2	25	4
23	12.2	0.35	1.6	2.0	1.8	87	5.15	13.9	25	3
24	7.8	0.37	2.0	2.4	2.2	135	5.11	18.8	25	3
25	16.4	0.30	1.5	1.9	1.7	97	5.47	17.0	28	4
26	10.6	0.26	1.6	2.0	1.7	100	4.73	9.6	25	4
27	10.0	0.34	1.7	2.0	1.8	110	4.92	20.3	25	3
28	20.0	0.36	1.6	2.0	1.7	39	5.38	17.0	25	3
29	35.0	0.30	1.6	1.8	1.7	50	5.73	17.6	28	3
30	--	0.36	1.5	- -	1.6	--	5.25	--	--	3
31	6.3	0.44	2.1	2.6	2.2	70	3.90	26.6	20	2
32	7.3	0.46	1.9	2.2	1.9	68	3.58	30.4	20	2
33	6.3	0.36	1.9	2.2	2.0	74	3.51	20.4	23	3
34	19.0	0.42	1.6	2.0	1.7	27	4.20	23.2	23	3
35	5.7	0.40	1.9	2.2	2.0	63	3.32	18.0	23	5
36	8.6	0.32	1.9	2.0	2.2	84	4.52	15.0	23	3
37	--	--	- -	1.8	- -	--	--	--	25	2
38	5.5	0.43	1.7	1.8	1.6	93	4.03	13.8	25	6