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RADC-TR-65-449
Final Report

ELEMENT DEVELOPMENT FOR ADVANCED ASSOCIATIVE MEMORIES

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The Marquardt Corporation

TECHNICAL REPORT NO. RADC-TR-65-449

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Rome Air Development Center
Research and Technology Division
Air Force Systems Command
Griffiss Air Force Base, New York

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AFLC, GAFB, N.Y., 24 Aug 66-161

FOREWORD

This Technical Documentary Report was prepared by Ralph W. Haas, Earl H. Blevis, and Stanley C. Requa of The Marquardt Corporation, Van Nuys, California, under USAF Contract No. AF 30(602)-3709; Project No. 5581, Task No. 558108, "Element Development for Advanced Associative Memories". The work on this task was accomplished between March 1965 and September 1965 and was administered under the direction of the Research and Technology Division, Intelligence and Data Processing Laboratory, Data Processing Branch, RADC, Griffiss Air Force Base, New York, with Mr. James Previte EMIID-I serving as Task Engineer.

Release of subject report to the general public is prohibited by the Strategic Trade Control Program, Mutual Defense Assistance Control List (revised 6 Jan 1965) published by the Department of State.

This report has been reviewed and is approved.

Approved: FRANK J. TOMAINI
Chief, Info Processing Branch

Approved: ROBERT J. QUINN, JR., Colonel, USAF
Chief, Intel and Info Processing Div

FOR THE COMMANDER: IRVING J. GABELMAN
Chief, Advanced Studies Group

ABSTRACT

A research and development program was conducted to investigate the technique of utilizing ferroelectric and photoconductor elements in an advanced associative memory. An analytical and experimental study was performed to examine the inherent logic capability of these electro-optical elements with respect to flexibility of parallel associative search and parallel arithmetic processing. A material effort was directed toward the development of thin film processes for the fabrication of the electro-optical elements. A breadboard model was constructed to provide demonstration of these search and processing techniques. A logic was developed for performing arithmetic processing.

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I. INTRODUCTION

A recent program at The Marquardt Corporation, Van Nuys, California, established the feasibility of utilizing electro-optical elements for the implementation of an associative tag memory. As the result of this effort a concept was evolved for utilizing this electro-optical approach for simultaneous arithmetic operations in an associative processor. A program was funded by RADC to investigate this concept and the materials necessary to implement such a processor. The work under this contract was performed during the period from March 30, 1965 to September 30, 1965. The work consisted of a parallel effort consisting of an analytical and experimental evaluation of the concept and a material program to continue the investigation of basic deposition techniques.

The study was performed to investigate the inherent logic capability of the Marquardt concept as applied to an arithmetic processing memory. One goal of the study was to design and fabricate a four word processor model that could demonstrate feasibility.

The material effort was devoted to the fabrication of single crystal ferroelectric materials, thin film ferroelectric materials, and thin film photoconductor materials. Fabrication techniques were improved for producing single crystal triglycine sulfate, the radio frequency sputtering of thin film barium titanate, and cadmium sulfide photoconductors.

II. ASSOCIATIVE PROCESSING

A. Processor Concept

An associative processor is an associative memory which can be addressed by content and has the capability of performing multiple arithmetic operations simultaneously by associative techniques. The associative addressing permits every word in the memory to be addressed in parallel. Multiple processing can be performed with a number of words which contain dissimilar data. The Marquardt processor utilizes ferroelectric and photoconductor electro-optical elements for associative addressing and processing.

The processor is based upon the electro-optical characteristics of ferroelectric and photoconductor elements when they are combined by a series circuit connection. The photoconductors serve to gate current among the ferroelectric elements when optically interrogated by means of light beams. The photoconductors and ferroelectrics are connected together in a series string configuration to form the individual bits in a word. Illumination of identical photoconductors of each bit of each word provides an associative inquiry by defining a path through the ferroelectrics of each word. If the active path in any word consists only of ferroelectrics with a like polarization (the case where inquiry data matches stored data), the ferroelectrics will switch upon the application of a voltage pulse. If a match is not obtained, at least one of the ferroelectrics in the illuminated photoconductor path will exhibit an opposed polarity and blocking will occur since this ferroelectric will assume most of the applied voltage.

This type of associative inquiry permits a unique active masking operation. Each bit position in each word has an additional photoconductor ferroelectric pair to permit masking, or bypassing of that specific bit.

Utilizing an electro-optical inquiry in which switching of the elements occurs upon match, the elements must be switched again to their original condition of storage. This method allows a "write upon match" operation. Upon match the data in the matching words can be changed by altering the light beam pattern for the rewrite cycle.

The active masking capability, in conjunction with the ability to write upon match, permits the execution of arithmetic functions such as addition, subtraction and multiplication. These functions can be performed by truth table techniques. An interrogation is made for those combinations of variables in which the data would change in the pertinent truth tables and the desired data is rewritten during the write cycle.

B. Truth Table Functions

To illustrate exactly how truth table techniques can be utilized to perform various processing functions, a given format will be assumed for all words in memory. (Figure 1) Two three bit operands are stored in Field 1 and Field 2, four carry bits are stored in Field 3, and five bits in Field 4 are used to store the result of the processing. An additional bit can be used as an identity bit or a bit used to identify a class or set of words in memory.

In processing, the basic method consists of an interrogation of a bit from each of the operands (the same bit position), a carry bit, and a sum or product bit in accordance with a truth table for a selected function. If a match detection occurs during interrogation, data can be rewritten according to the truth table. The following pages discuss this method as applied to addition, subtraction, and multiplication.

If a bit from each operand is considered, either bit can store a digital one or a zero; four combinations are possible: 00,10,11, and 01. It is not known which combination is stored in a word since many words are addressed for simultaneous processing.

The conventional rules of binary addition are

1 + 1 = 0 plus a carry

0 + 0 = 0

0 + 1 = 1

1 + 0 = 1

A truth table for the four combinations with and without a carry is shown in Figure 2.

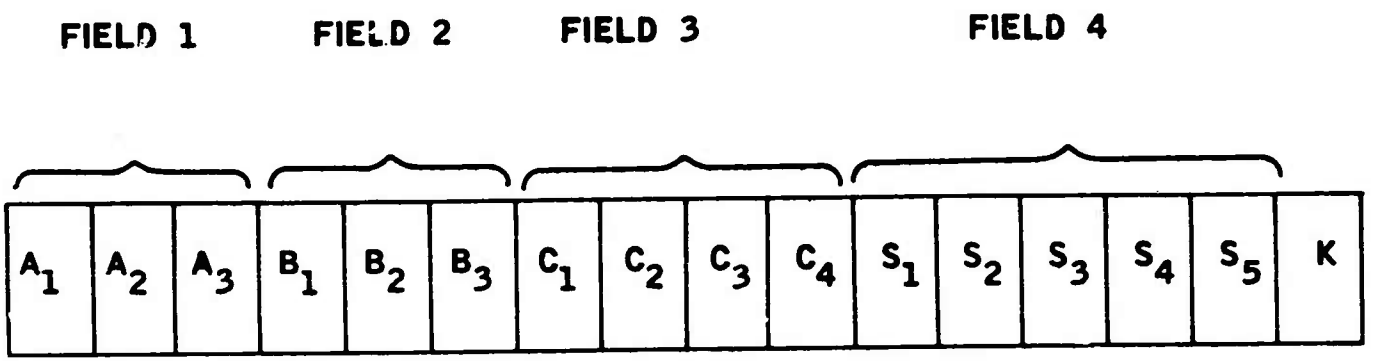


Figure 1. Word Format

INTERROGATE FOR STORED CONDITION				IF TRUE DESIRED STORAGE			
A_1	B_1	C_1	S_1	A_1	B_1	C_1	S_1
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1
1	0	0	0	1	0	0	1
1	0	1	0	1	0	1	0
1	1	0	0	1	1	1	0
1	1	1	0	1	1	1	0
0	1	0	0	0	1	0	1
0	1	1	0	0	1	1	0

Figure 2. Addition Truth Table

As indicated in Figure 2 by heavy underlines, there are four combinations of bit and carry information for which the data must be changed. For example, in the first case in which two zeroes are stored and a carry exists, a zero would be written in the carry position and a one in the sum bit.

In subtraction the conventional rules of subtraction are employed:

$0 - 0 = 0 \quad 1 - 1 = 0 \quad 1 - 0 = 1$ and $0 - 1 = 1$ with a borrow

In this case the corresponding bit positions from each operand, the borrow bit, and the remainder bit are considered. The truth table for subtraction is shown in Figure 3. Again, four combinations of stored information require change of data.

Conventionally, multiplication is carried out by multiplying the multiplicand by each digit in the multiplier thus forming a number of partial products. These partial products are then added to form the product. Therefore, in performing a multiplication both multiplication and addition are necessary. Two methods of multiplication have been investigated utilizing electro-optical series elements: a cumulative partial product method and a cumulative final product digit method. The two methods are described below:

Method (1): Form partial products bit by bit by sequentially multiplying the multiplicand by each bit of the multiplier. The partial products are stored in the product field and updated each time that a new partial product is formed. A cumulative partial product becomes the product.

INTERROGATE FOR STORED CONDITION				IF TRUE DESIRED STORAGE			
A_1	B_1	BORROW	Q	A_1	B_1	BORROW	Q
1	0	0	0	1	0	0	0
1	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1
0	1	0	0	0	1	1	1
0	1	1	0	0	1	1	0
1	1	0	0	1	1	0	0
1	1	1	0	1	1	1	1

Figure 3. Subtraction Truth Table

The necessary storage bits involve the bits for the multiplicand, the multiplier, the final product and (2N-2) carry bits. (N is the number of bits in operand).

Method (2): Form the total product, bit by bit, by sequentially forming the necessary terms of those partial products that relate to a given product digit by multiplication and cumulatively adding the terms. Two carries are involved. One carry must be considered as the cumulative terms are added, and the other carry must be derived from the previous product digit.

The necessary storage bits involve the bits for the multiplicand, the multiplier, the final product, and the two carry bits.

Examination of these methods show that a greater number of carry storage bits are necessary for the first method. However, this method utilizing the cumulative partial product was selected for illustration of principle since the necessary control circuitry was simpler.

Multiplication by conventional methods for two three bit words is shown below:

		A_3	A_2	A_1
		B_3	B_2	B_1
		A_3B_1	A_2B_1	A_1B_1
	A_3B_2	A_2B_2	A_1B_2	
A_3B_3	A_2B_3	A_1B_3		
S_5	S_4	S_3	S_2	S_1

Examination of the sequence indicates that the following steps are necessary:

(1) $A_1B_1 + 0 \longrightarrow S_1$

(2) $A_2B_1 + 0 \longrightarrow S_2$

(3) $A_3B_1 + 0 \longrightarrow S_3$

(4) $A_1B_2 + S_2 \longrightarrow S_2$ and C_2

(5) $A_2B_2 + S_3 \longrightarrow S_3$ and C_3

(6) $A_3B_2 + 0 \longrightarrow S_4$

(7) $A_1B_3 + S_3 + C_2 \longrightarrow S_3$ and C_3

(8) $A_2B_3 + S_4 + C_3 \longrightarrow S_4$ and C_3

(9) $A_3B_3 + 0 \longrightarrow S_5$

(10) $S_5 + C_3 \dashrightarrow S_5$

For example, in step (1) bit position A, would be multiplied by B_1 and stored in bit position S_1. In step (4) bit position A, would be multiplied by B_2, added to S_2, and the result stored in bit position S_2 and C_2.

Truth tables were prepared for each type of operation necessary to perform the multiplicatior function. These tables indicate the "stored" and "desired" combinations possible in all bit positions. Utilizing an electro-optical interrogation for those combinations in which a change is desired, the "desired" data will be rewritten. Multiplication would involve the following types of operations.

		Number of read-write cycles
$A_i B_j + 0$	$\longrightarrow$ Sn	1
$A_i B_j + Sn$	$\longrightarrow$ Sn and Cn	2
$A_i B_j + Sn + Cn$	$\longrightarrow$ Sn and Cn	4
$Sn + Cm$	$\longrightarrow$ Sn, Sn + 1, and Cm	2

The truth tables for these operations are shown in Figures 4, 5, 6, and 7. The combinations of data for which a change is necessary between the "stored" and "desired" data is indicated by heavy underlines on the tables. The number of changes thus represents the number of read-write cycles necessary to perform each operation. The number of these cycles is indicated above. For example, to perform the operation indicated in Figure 4, an interrogation for a "110" would be made and then a "111" would be rewritten. An exception to the rule exists in the truth table shown in Figure 6. In this case the first two changes could be combined. An interrogation would be made for "0 x 01" (the "x" indicates a bypass) and "0 x 10" would be rewritten.

These interrogations can be made on a bit by bit basis. A bit from each operand, a carry bit, and a sum or product bit are considered for the necessary read-write cycles. Successive bits are examined sequentially dependent upon the function.

A selection of interrogation data must be made coincident with the bit selection for each read-write cycle. The specific data selection is in accordance with the truth tables of the function being performed. Figures 8, 9, and 10 show this selection for addition, subtraction, and multiplication.

INTERROGATE FOR STORED CONDITION			IF TRUE DESIRED STORAGE		
A_j	B_j	S_n	A_j	B_j	S_n
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	0	1	1	1

Figure 4. Truth Table for $A_iB_j + 0 \longrightarrow S_n$

INTERROGATE FOR STORED CONDITION				IF TRUE DESIRED STORAGE			
A_i	B_j	S_n	C_n	A_i	B_j	S_n	C_n
0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0
1	1	0	0	1	1	1	0
0	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	0
1	1	1	0	1	1	0	1

Figure 5. Truth Table for $A_iB_j + S_n \longrightarrow S_n$ and C_n

INTERROGATE FOR STORED CONDITION				IF TRUE DESIRED STORAGE			
A_i	B_j	S_n	C_n	A_i	B_j	S_n	C_n
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	0
0	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	0	1

Figure 6. Truth Table for $A_i B_j + S_n + C_n \longrightarrow S_n$ and C_n

INTERROGATE FOR STORED CONDITION			IF TRUE DESIRED STORAGE		
S_n	C_m	S_{n+1}	S_n	C_m	S_{n+1}
0	0	0	0	0	0
0	1	0	1	0	0
1	0	0	1	0	0
1	1	0	0	0	1

Figure 7. Truth Table for $S_n + C_m \longrightarrow S_n$, S_{n+1}, and C_m

READ WRITE CYCLES

FIELD	1	2	3	4	5	6	7	8	9	10	11	12
A	0 0	1 1	1 1	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1	0 0
B	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1
C	1 0	1 1	0 1	0 0	1 0	1 1	0 1	0 0	1 0	1 1	0 1	0 0
S	0 1	0 0	0 0	1 1	0 1	0 0	0 0	1 1	0 1	0 0	0 0	1 1
	A_1B_1	A_1B_1	A_1B_1	A_1B_1	A_2B_2	A_2B_2	A_2B_2	A_2B_2	A_3B_3	A_3B_3	A_3B_3	A_3B_3
	S_1	S_1	S_1	S_1	S_2	S_2	S_2	S_2	S_3	S_3	S_3	S_3

Figure 8. Inquiry Data Selection for Addition

READ WRITE CYCLES

FIELD	1	2	3	4	5	6	7	8	9	10	11	12
A	1 1	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1	0 0	0 0	1 1
B	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1	0 0	0 0	1 1	1 1
C	1 0	1 1	0 1	0 0	1 0	1 1	0 1	0 0	1 0	1 1	0 1	0 0
S	0 0	0 1	0 1	0 0	0 0	0 1	0 1	0 0	0 0	0 1	0 1	0 0
	A_1B_1	A_1B_1	A_1B_1	A_1B_1	A_2B_2	A_2B_2	A_2B_2	A_2B_2	A_3B_3	A_3B_3	A_3B_3	A_3B_3
	S_1	S_1	S_1	S_1	S_2	S_2	S_2	S_2	S_3	S_3	S_3	S_3

Figure 9. Inquiry Data Selection for Subtraction

READ WRITE CYCLES

FIELD	1	2	3	4	5	6	7	8	9	10
A	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 0	1 1
B	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	X X	0 0
C	X X	X X	X X	0 0	0 1	0 0	0 1	X X	1 0	1 0
S	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1
	A_1B_1	A_2B_1	A_3B_1	A_1B_2	A_1B_2	A_2B_2	A_2B_2	A_3B_2	A_1B_3	A_1B_3
	S_1	S_2	S_3	S_2C_1	S_2C_1	S_3C_2	S_3C_2	S_4	S_3C_1	S_3C_1

READ WRITE CYCLES

FIELD	11	12	13	14	15	16	17	18	19
A	1 1	1 1	0 0	1 1	1 1	1 1	1 1		
B	1 1	1 1	X X	0 0	1 1	1 1	1 1		
C	0 0	0 1	1 0	1 0	0 0	0 1	X X	1 0	1 0
S	0 1	1 0	0 1	0 1	0 1	1 0	0 1	0 1	1 0
	A_1B_3	A_1B_3	A_2B_3	A_2B_3	A_2B_3	A_2B_3	A_3B_3		
	S_3C_1	S_3C_1	S_4C_2	S_4C_2	S_4C_2	S_4C_2	S_5	S_5C_3	S_5C_3

Figure 10. Inquiry Data Selection for Multiplication

III. EVALUATION OF CONCEPT

A. Logic Implementation

To perform various types of associative searches and associative processing with an electro-optical processor, it is necessary to generate the required read-write cycles in the correct time sequence. This function must be performed by the external logic control circuitry.

The multiple steps utilized in performing various types of associative searches or arithmetic processing with electro-optical cells must be programmed by sequential control of (1) the selection of the pertinent bit positions to be interrogated and (2) the specific interrogation to be employed. The sequence of the selection and the specific inquiry data are determined by the truth table for the process involved.

The bit selection in addition, for example, consists of selection of the first bit of the augend, the first bit of the addend, the first bit of the sum, and the related carry bit. Sequentially, the second bit in each operand is selected for operation. This sequence is increased in order until the total sum is obtained.

The specific interrogation, or number of interrogations, that is made at each selected bit position depends upon the truth table required for the process being performed. In addition, for example, the specific interrogation data consists of the four possible combinations of ones and zeroes that can exist in the augend and addend with due consideration of the carry for that bit position.

In actual operation,the bit selection and selection of inquiry data must be synchronized. Depending upon the specific arithmetic process, after a bit selection is made, a number of combinations of digital "ones" and "zeroes" may be necessary for interrogation. For example, in addition, an interrogation must be made for a "zero", a "one , another "one", and a "zero" of each bit position of the augend. A simultaneous interrogation must be made for a "zero", another "zero", a "one", and another "one" at each bit position of the addend. In multiplication these combinations of interrogation data can change for each bit position and the complexity increases. A further requirement exists in that the interrogation data sequence must be correlated with the specific bit selection.

The circuitry chosen to implement the logic essentially is divided into three sections; bit selection, inquiry data selection, and light source gating and output indication.

The bit selection circuitry consists of a counter and a group of registers. Four registers are used for bit selection storage to designate the specific bits for switching at a given time. A three bit shift register is used for each of the operands and a four bit shift register is used for carry storage. A five bit register is used for storage of the sum or product. Two of the registers are recirculating in order to provide a repetitive sequence. The sum or product register utilizes logical gating to change the position of recirculation entry during succeeding sequences.

A counter in conjunction with logical gating is utilized to provide shift pulses for the above shift registers. This counter is designed to count by "ones" until a number of timing pulses have occurred then count by "twos". After more timing pulses the count is changed to "fours". This count, however, is not monatonic since a count by ones is required at several points in the switching sequence. This operation is made possible by gating.

The inquiry data circuitry consists essentially of a counter, a shift register, and storage flip flops. A five stage counter is used to provide timing pulses for change of inquiry data in accordance with the pertinent truth tables for the multiplication arithmetic process. A four stage shift register selects the repetitive inquiry data used for interrogation during the addition and subtraction processes. Four flip flops are used to store signals for the digital "ones" and "zeroes" representing this data for each of the bit selection registers.

The signals for exciting the light sources associated with the individual bits are derived from the light drive gating circuits. A gate circuit is provided for the drive associated with the digital "one" and "zero" associated with each bit. For example, a gate is provided to excite the light source which will interrogate for a "one" at the first bit position of all words stored in memory. Each gate, effectively, "ANDS" the bi selection signal and the inquiry data signal.

Output indication is provided by a five stage shift register. Each stage of the register is connected to a light indication circuit. The register can be connected to any word in memory by switching. For readout the register is shifted in synchronism with the storage bits of a word used to store the sum or product of an arithmetic process.

A series of delay multivibrators are used to generate shift pulses and pulses for switching the ferroelectric elements of words in memory. These pulses are delayed in time to accommodate the switching times of the photoconductors and light drive sources.

A simplified block diagram is shown in Figure 11.

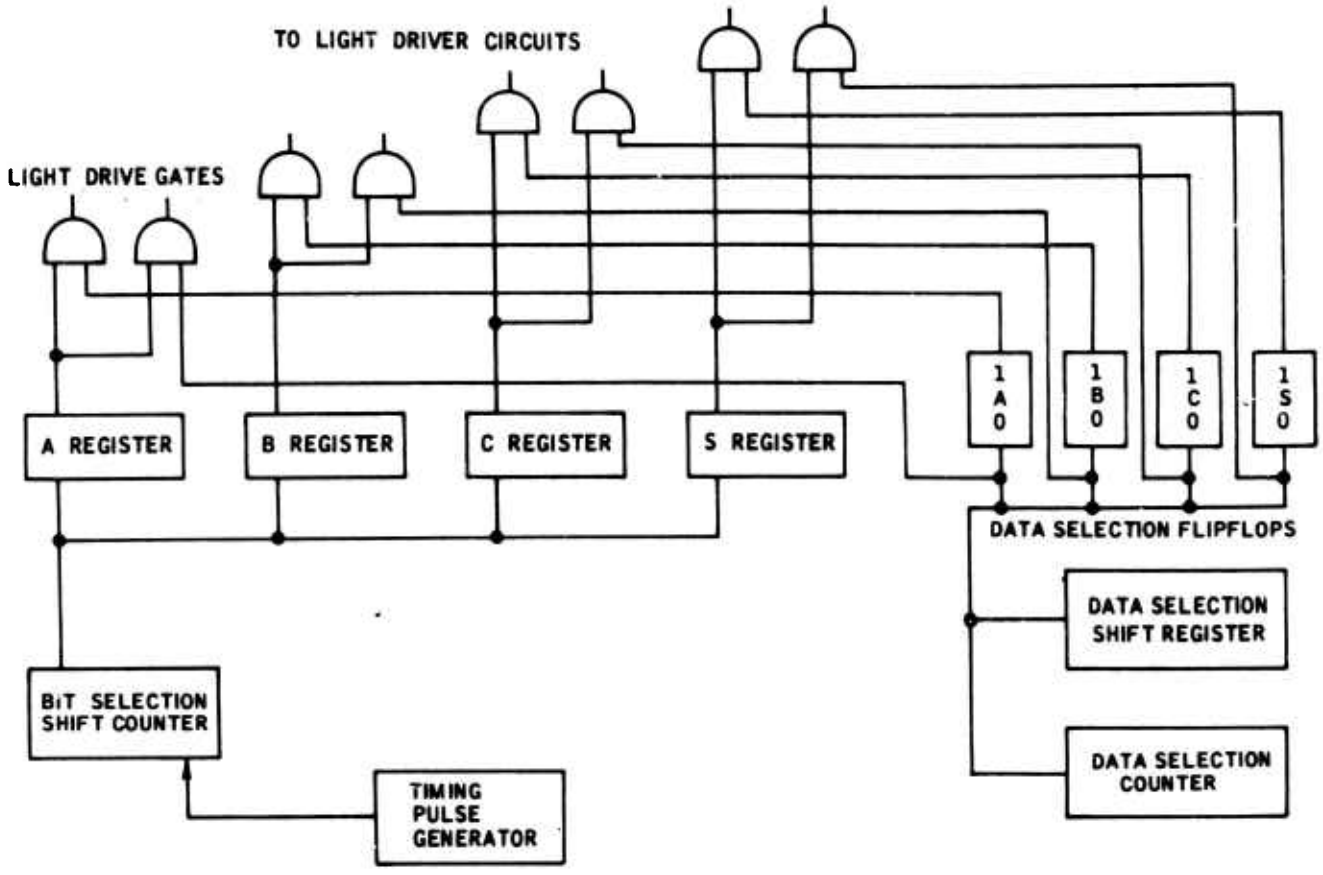


Figure 11. Simplified Block Diagram of Control Circuitry

B. Breadboard Model

An associative processor model was assembled in breadboard form utilizing 16 bit words to demonstrate the feasibility of parallel processing and various associative searches. The model consists of a table relay rack for mounting, a logic "basket" for circuitry, a control panel for switching, individual printed circuit cards for mounting the word elements, and auxiliary driver circuits. (See Figure 12).

The logic basket contains commercial logic cards such as flip-flops, NAND gates, diode gates, and delay multivibrators. The individual circuit cards are interconnected by conventional taper pin connection. Cable harnesses carry the output of the sequencing and control circuitry to the light driver circuits and the voltage pulse circuits. (See Figure 13 and Figure 14).

The control panel provides switching provision for the selection of arithmetic function, data insertion, and input-output or drive selection. Five rotary switches select the function of "ADD", "SUBTRACT", "MULTIPLY", "SEARCH", or "OFF" as shown in Figure 15. A momentary contact switch provides a common reset for all flip flops. A set condition can be realized for any bit selection flip flop representing the operand bits, the carry bits, or the sum product bits by individual momentary contact switches. Toggle switches can select any or all of the words for voltage drive. Any word can be chosen for individual readout purposes.

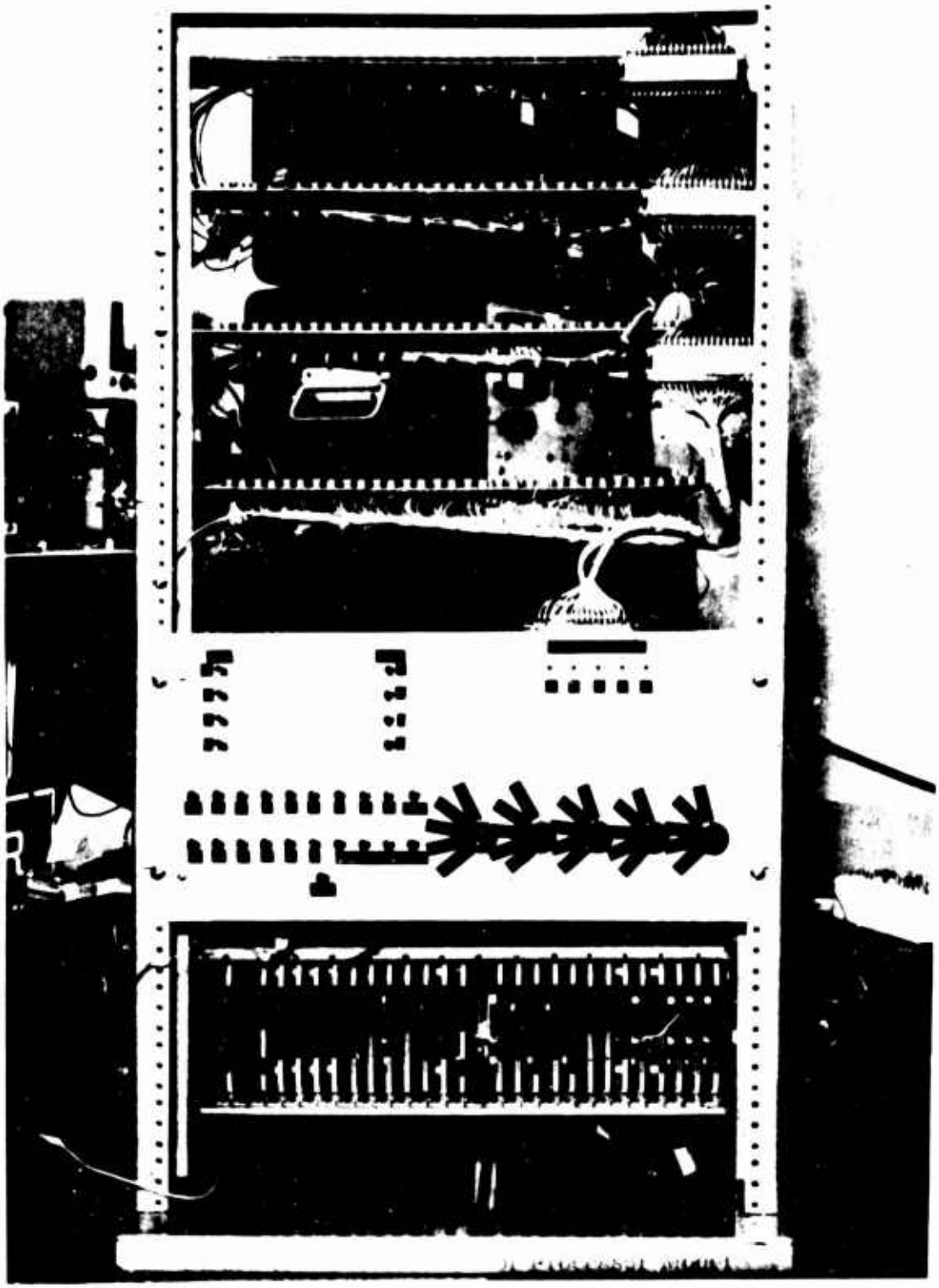


Figure 12. Overall View of Processor Model

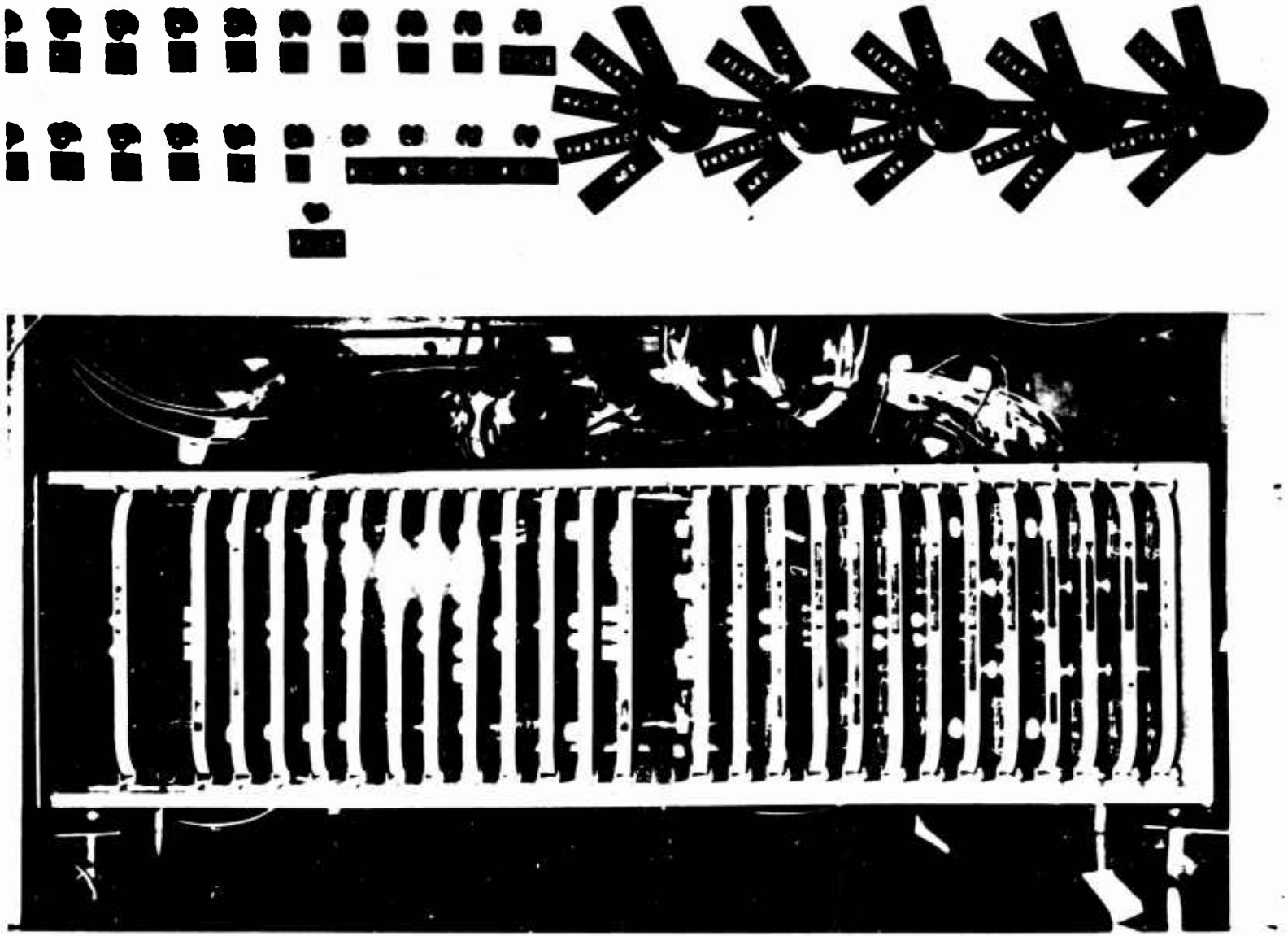


Figure 13. Logic Basket of Processor Model

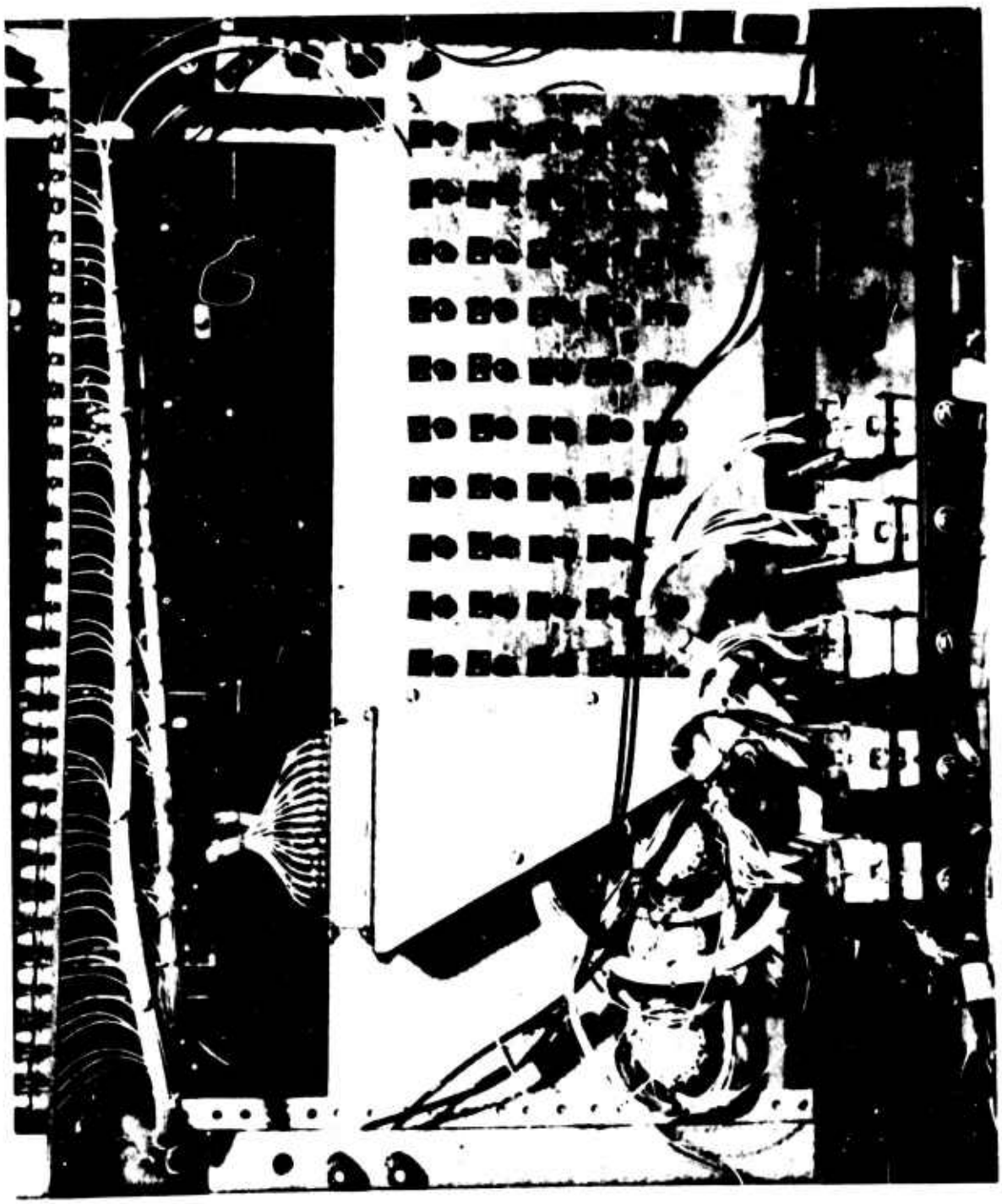


Figure 14. Cable Connections of Model

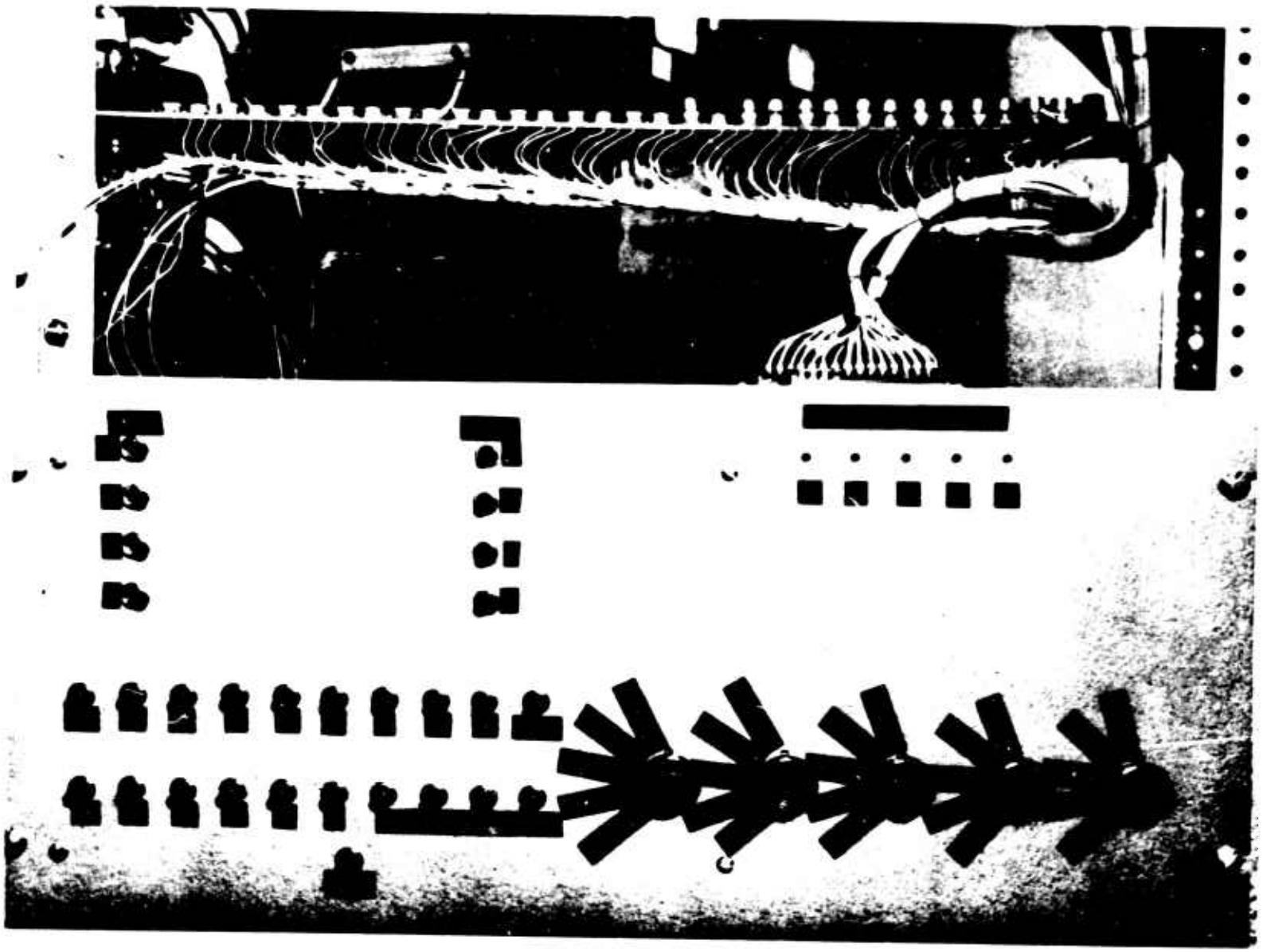


Figure 15. Control Panel of Model

The circuitry interconnecting the elements of each word is contained on separate printed circuit cards. The ferroelectric and photoconductor elements that form the individual bits of the words are mounted in transistor cases. These elements are mounted by transistor sockets on the cards. (Figure 16).

The breadboard model logic was made operational by circuit checkout. The cards containing the ferroelectric and photoconductor elements were examined individually for their respective quality in performance characteristics. The various control functions of the complete model were checked on a bit by bit basis. Limited automatic searches were performed. Operational testing of the parallel processing remains to be completed.

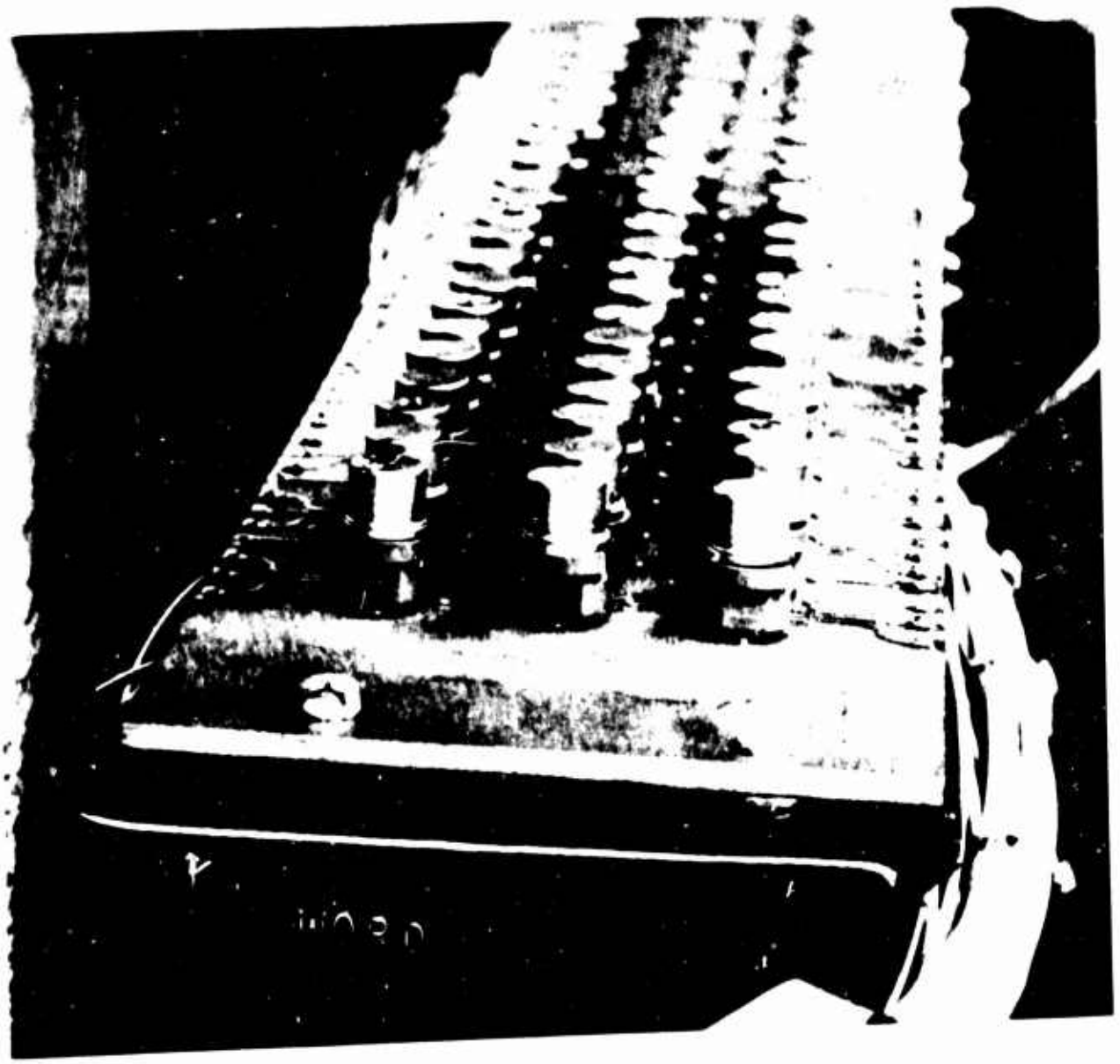


Figure 16. Word Card of Model

IV. MATERIAL DEVELOPMENT

A. Thin Film Ferroelectric

Initial investigation of the deposition of barium titanate films by radio frequency sputtering has been conducted. To this end a radio frequency sputtering apparatus has been designed and built and a number of deposition samples prepared and analyzed. While much of this work was conducted under an internally supported research and development program, all related work is contained in this report.

Properties of $BaTiO_3$. Barium titanate is one compound of a complex system of compounds and solid solutions of compounds formed when barium oxide (BaO) and titanium dioxide (TiO_2) are mixed and heated. Barium titanate results from an equimolar mixture. A complete phase diagram is shown in Figure 17. Stoichiometric or near stoichiometric $BaTiO_3$ is known to exist in the several polymorphic forms listed.

POLYMORPHS OF $BaTiO_3$

Hexagonal	1460° to 1618°C	Metastable at room temperature
Cubic	120°C to 1460°C	Perovskite type point group m3m not ferroelectric
Tetragonal	5°C to 120°C	Point group 4mm ferroelectric
Orthorhombic	-90°C to 5°C	Ferroelectric
Rhombohedral	to -90°C	Ferroelectric

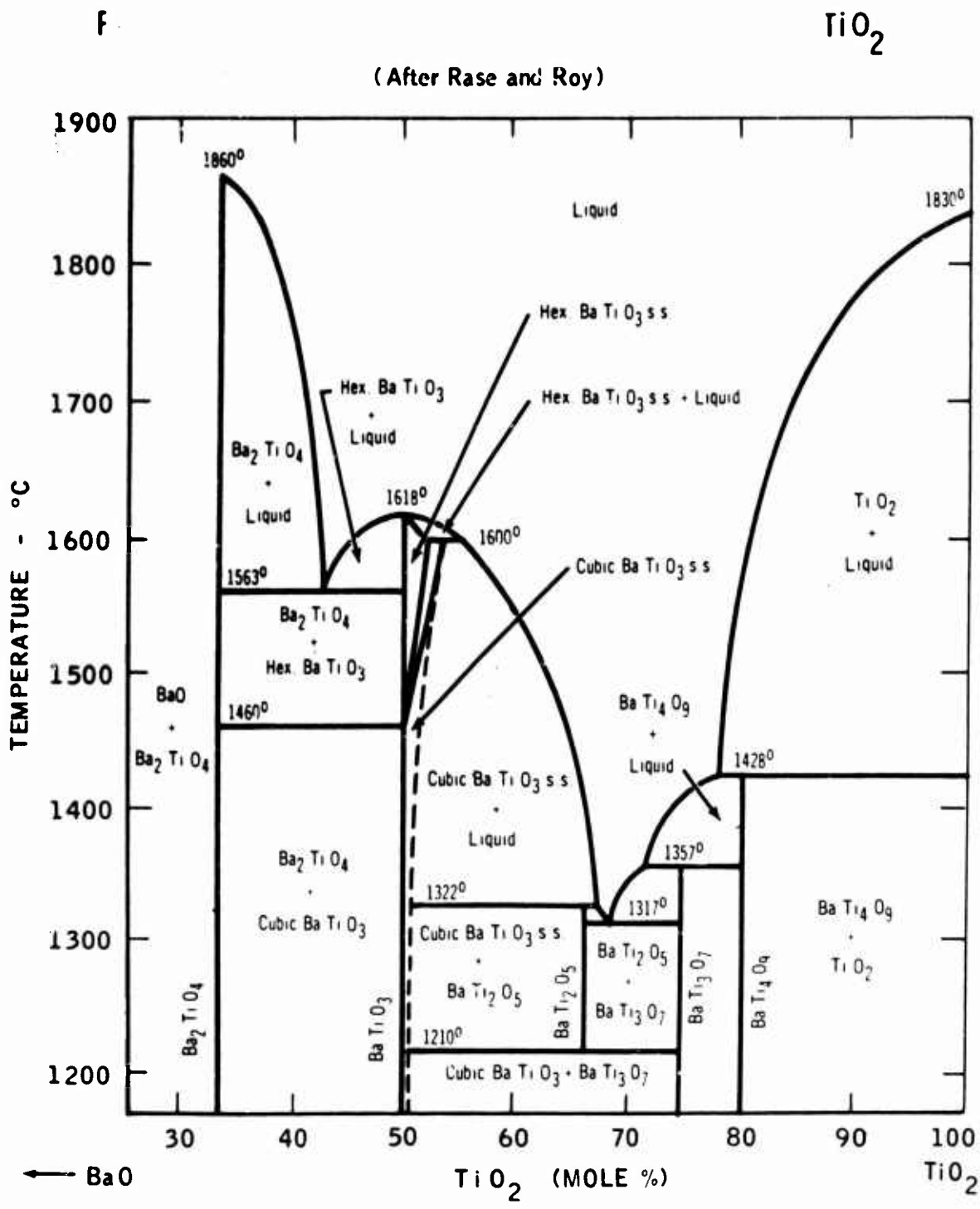


Figure 17. Phase Diagram of the System BaO - TiO_2

The tetragonal, orthorhombic, and rhombohedral low temperature forms are all ferroelectric. The cubic form undergoes a displacive type phase transition at 120°C to become the pseudo-symmetric ferroelectric tetragonal form. The hexagonal form, however, which is metastable at room temperature does not undergo the phase transition and remains non-ferroelectric to very low temperatures. Care must, therefore, be exercised in preparing ferroelectric $BaTiO_3$ to avoid rapid quenching from temperature above 1460°C or other preparation conditions which might freeze in the hexagonal form. Hard ceramic body samples are readily prepared by a number of standard techniques such as sintering at temperatures between 1350-1450°C.

Some of the more important physical properties of $BaTiO_3$ are summarized below.

PHYSICAL PROPERTIES OF $BaTiO_3$

Density	6.14 gm/cc	Tegragonal based on X-ray determinations
Melting Point	1618°C	For stoichiometric $BaTiO_3$ compositions only
Index of Refraction	2.4	Cubic
Dielectric Constant	1000-2000	Non-polarized ceramic (experimental)

In the low temperature forms, the thermal expansion coefficient, piezoelectric coefficient and dielectric constant are strongly anisotropic. Polarized polycrystalline $BaTiO_3$ ceramic is also strongly anisotropic in

its properties. The thermal expansion coefficient of non-polarized polycrystalline $BaTiO_3$ and dielectric constant of crystalline $BaTiO_3$ are given as a function of temperature in Figures 18 and 19 respectively.

When heated in a vacuum or a dry hydrogen atmosphere to temperatures above 400°C, $BaTiO_3$ samples are reduced and oxygen deficiencies are produced. At low temperatures (600°C), however, the diffusion velocity of the oxygen deficiencies is very low, and, therefore, only the surface is reduced. At somewhat higher temperatures (800°C) the samples are reduced throughout. When annealed in air, reduced samples tend to return to their initial state; however, the coloration darkening that accompanies reduction remains when treatments at temperatures above 100°C are used. The oxygen deficiency turns the normally insulating samples semi-conductive where resistivities in the range of 1 to 10^5 ohm-cm are reported. The optical activation energy of reduced semi-conducting $BaTiO_3$ is approximately 0.5 eV, while the thermal activation energy is approximately 0.17 eV. When heated to still higher temperatures in vacua, barium oxide is evolved leaving a residue which is very rich in titanium oxides. Further heating causes the residue to volatilize as a mixture of titanium dioxide, titanium suboxides and titanium metal.

Review of Other Techniques. A number of techniques have been used in the past to prepare thin film of the barium titanate for study. These are summarized in Figure 20 While in a number of cases

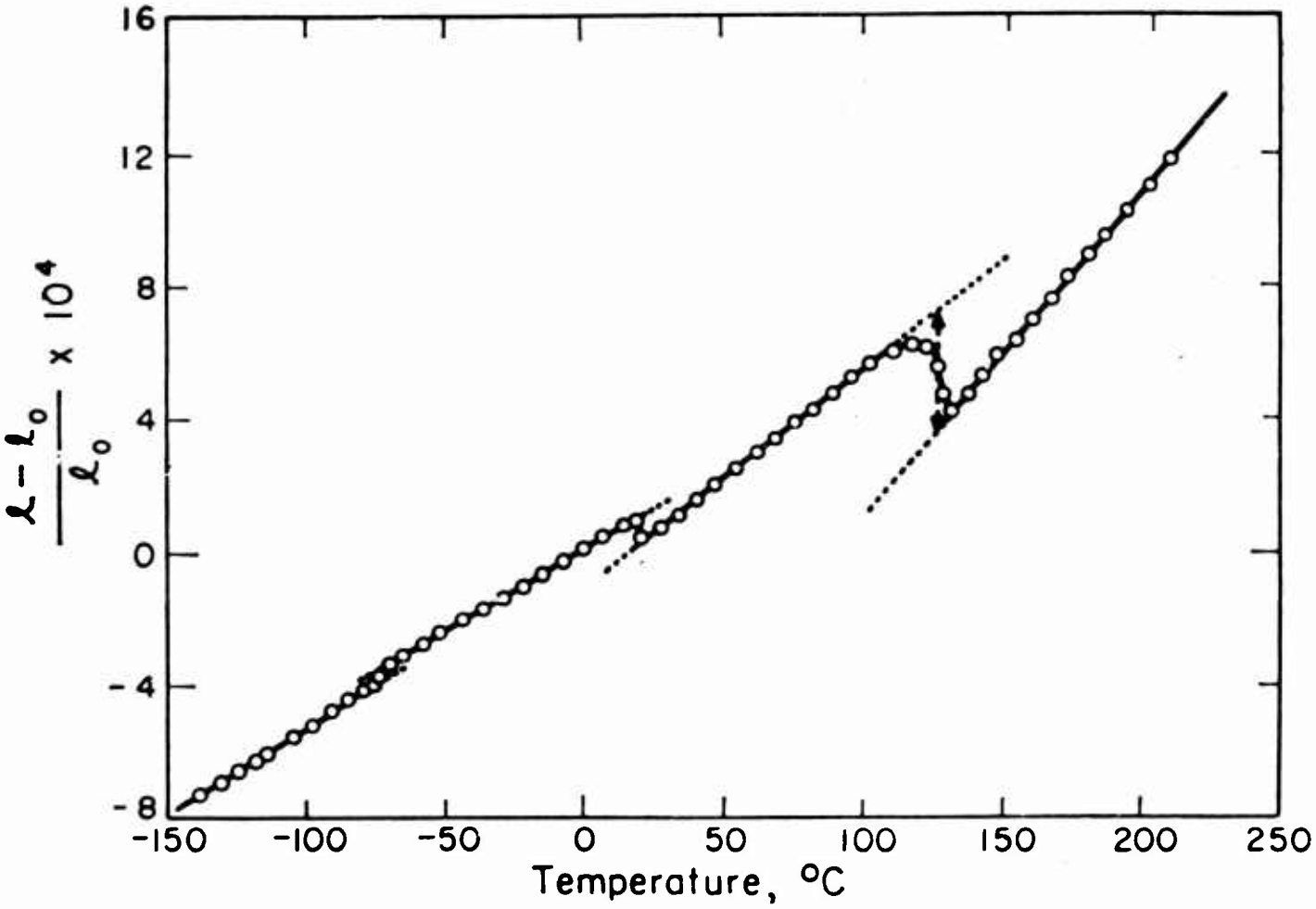


Figure 18. Thermal Expansion of Polycrystalline $BaTiO_3$

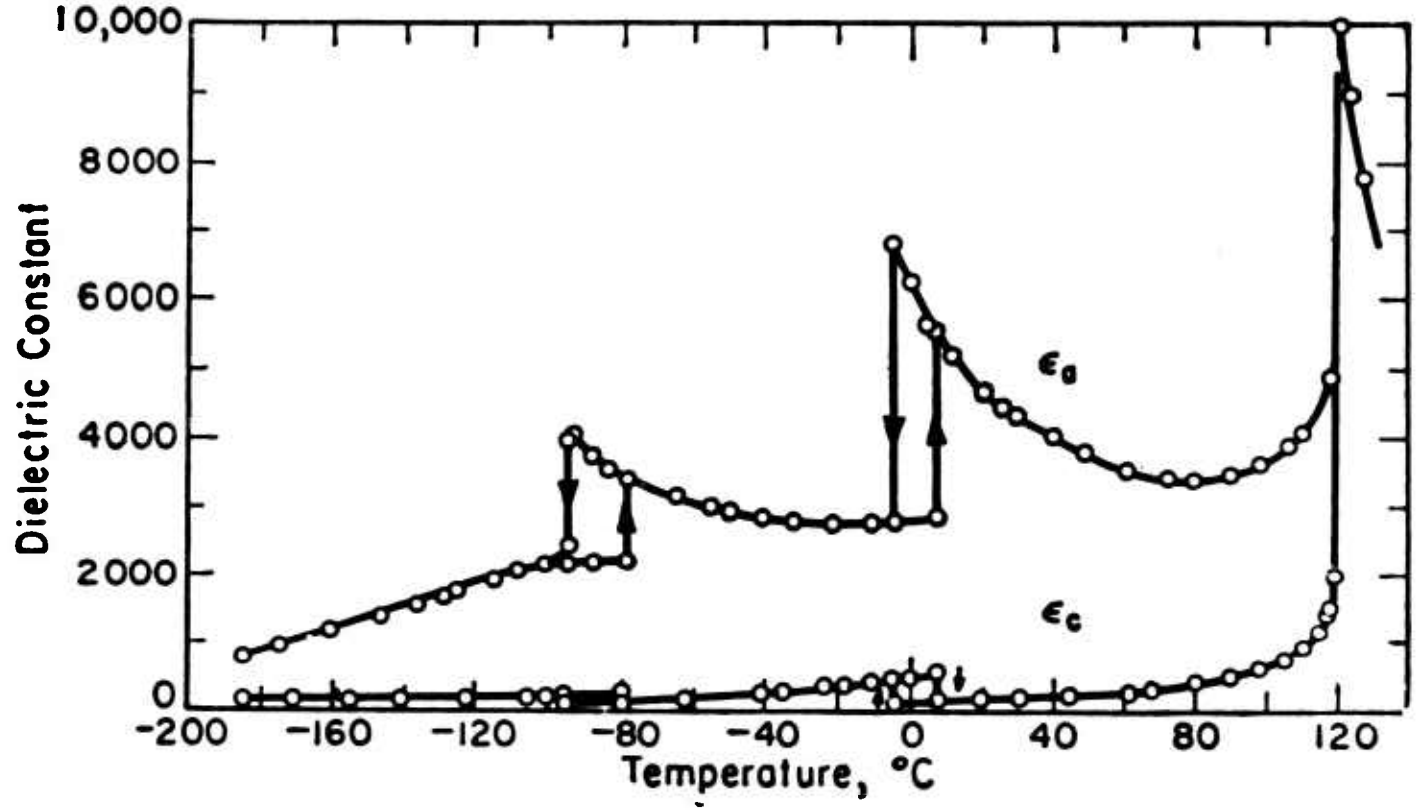


Figure 19. Dielectric Constants of $BaTiO_3$

Principal Investigator	Material	Method Employed	Reference
C. Feldman	$BaTiO_3$	Evaporation followed by post deposition heat treatment	Rev. Sci. Instr. 26 463 (May 1955)
M. S. Lure, E. I. Vasileva, and I. V. Ignateva	$Pb(Zr,Ti,Sn)O_3$	Hydrolysis from a solution of the tetra-chlorides	Izv. Akad. Nauk USSR 24 1376 (1960)
E. V. Bursian and N. P. Smirnova	$BaTiO_3$	Melting of powder onto wettable (Platinum) foil	Fiz. Tverdogo Tela 4 1675 (1962)
V. A. Lamb and H. I. Salmon	$BaTiO_3$	Electrophoretic	Cer. Bull. 41 781 (1962)
E. Sekine and H. Toyoda	$BaTiO_3$	Evaporation and flash evaporation onto heated substrates	Jour. Vac. Soc. (Japan) 5 310 (1962)
E. K. Muller B. J. Nicholson and G. L'E. Turner	$BaTiO_3$	Grain by grain (flash) evaporation onto heated polycrystalline and monocrystalline substrates	Jour. Electrochem. Soc. 110 969 (Sept. 1963)
A. E. Feuersanger A. K. Hagenlocker and A. L. Solomon	$BaTiO_3$	Coevaporation in oxygen using electron beam sources onto heated substrates	Jour. Electrochem. Soc. 111 1387, December 1963.

Figure 20. Summary of Previous Work on Thin Films of the Double Oxides

satisfactory films were produced for study, all tended to show lack of stoichiometry, low densities, voids, cracks and pinholes and somewhat degraded properties were obtained.

When evaporation techniques, whether simple resistance heated boat, flash, or coevaporation using electron beam sources, are used, it is found necessary to either heat the substrates during deposition or to bake the films in air after deposition to produce crystallization. Temperatures required for post deposition heat treatments were in excess of a 1000°C necessitating the use of platinum foil substrates. However, when deposited onto heated substrates the minimum temperatures required were only between 500 and 800°C.

Radio Frequency Sputtering. Sputtering is the process whereby, when bombarded by heavy atoms or ions, material is evolved from a target. The material thus evolved can be condensed on suitable substrates to produce thin films of the target material. The physical process thought to be responsible for most sputtering is one of momentum transfer between the bombarding particles and the atoms of the target material. It is, therefore, essentially an atomic process and material is transported to the substrates in atomic or molecular vapor form.

Particle energies required to produce efficient fast sputtering are of the order of 400 to 4000 eV. Since it is difficult to produce a high density beam of neutral particles with these energies, ions are normally used for most sputtering work. These ions may be readily generated by creating a discharge in a moderate pressure gas by means of a cold cathode discharge (glow discharge), a hot (thermonic) discharge, or a radio frequency discharge.

When a beam of ions is directed at an insulating target to produce sputtering, the surface of the target rapidly acquires a charge sufficient to repel additional incident ions and continuous bombardment is not possible. However, by applying a radio frequency potential to a metal plate behind the insulating surface this accumulated charge can effectively be removed and extremely high average bombardment rates sustained.

A number of workers have reported that several advantages are inherent in the sputtering technique as a method of thin film preparation. These are: (1) the ability to produce large, uniform layers, (2) freedom from pinholes caused by spitting of the source, (3) freedom from contamination introduced by heated crucibles, and (4) faithful compositional reproduction of the parent material used as the source. While this work has been done mainly on elemental metals and semiconductors, alloys, and intermetallic compounds, there is every reason to believe at this time that the advantages are of a sufficiently general nature that they will prove valid for all types of sputtering and, in particular, for radio-frequency sputtering of barium titanate.

Apparatus. The Radio Frequency sputtering apparatus is shown in Figure 21. It consists of a 4" x 4" hard pyrex pipe cross housing, a tungsten thermionic emitter, primary anode, and R. F. sputtering electrode. The apparatus is evacuated by a pump system consisting of a 15 cfm mechanical pump, 4" oil diffusion pump, water cooled baffle, liquid nitrogen trap and suitable gauging. Provision has been made for

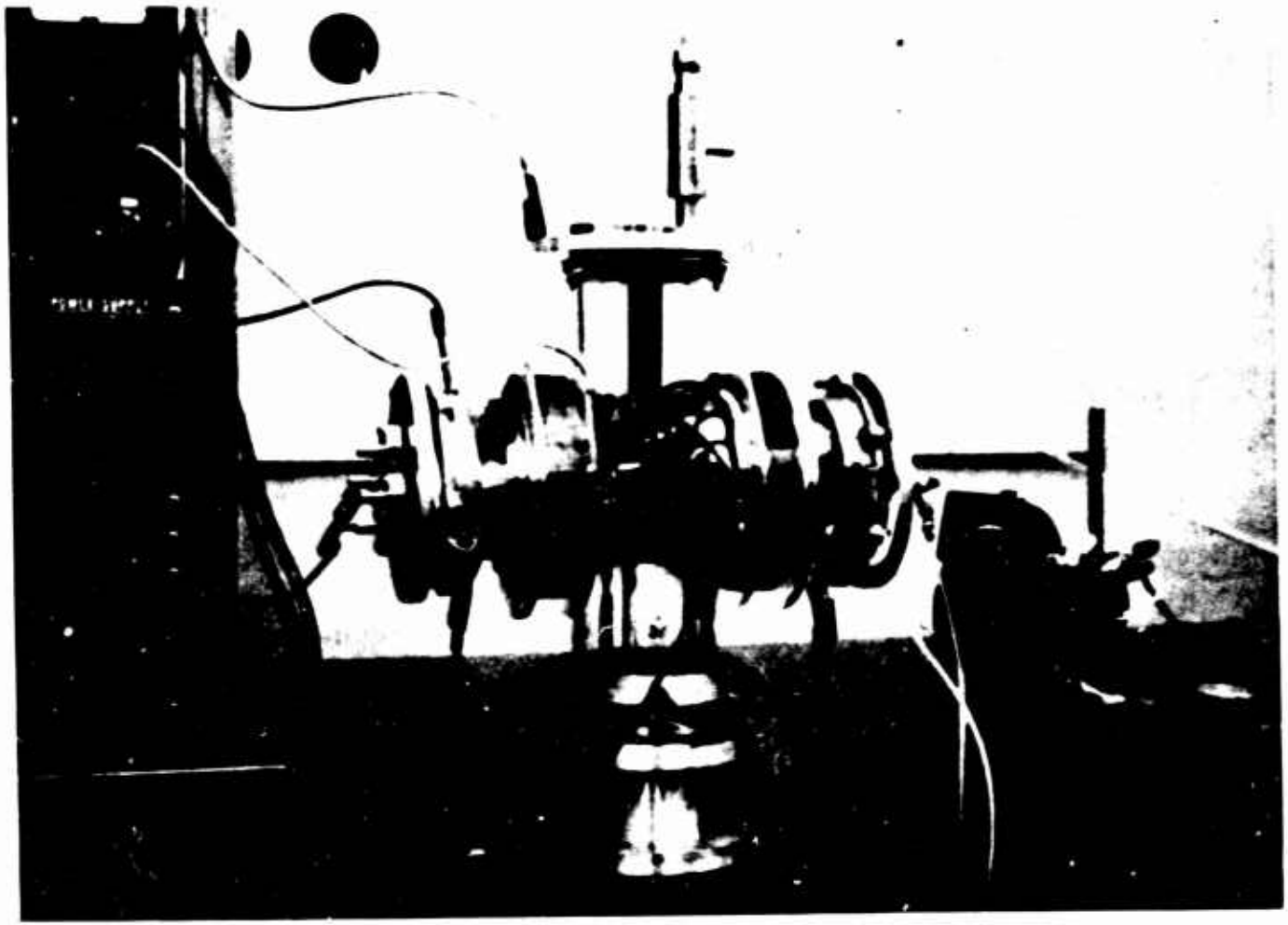


Figure 21. Radio Frequency Sputtering Apparatus

admitting pre-mixed oxygen and argon gas through a leak valve into the high vacuum side of the system. Power supplies for the apparatus are mounted in a standard 19" relay rack located adjacent to the system. The thermionic emitter is heated by a 60 cycle 300 VA center-tapped transformer. Primary anode power is supplied by an adjustable 250 volt 3 amp bridge rectified and capacitively filtered unit. The radio frequency generator consists of a crystal controlled oscillator and 500 watt power amplifier operating a 100 KC.

Normal operating pressure in the system during sputtering is maintained at a pre-set level in the range between 5×10^{-4} and 10^{-2} torr by balancing the pumping speed as controlled by a high vacuum gate valve and the leak rate as controlled by an adjustable leak valve. Pressure is read on a control unit for a Bayard Alpert type ionization gauge modified to operate at pressures up to 10^{-2} torr. Modification has been accomplished by placing a 0.25 megohm potentiometer and switch in series with the 1 milliampere emission sensing resistor of the control unit and adjusting its value to produce 100 microampere of gauge emission. By lowering the emission current rather than attenuating the gauge output the linearity of the pressure measurement has been maintained.

The R. F. electrode and target assembly has been fabricated from a heavy wall 3-1/2" diameter pyrex tube flanged on one end to provide a vacuum seal to the upper arm of the hard pyrex pipe cross and sealed with a flat pyrex plate on the other end to hold the target. A copper disc placed in the bottom of the well thus formed is connected through a matching network to the R. F. generator. A concentrated brine solution is used to provide good R. F. contact between the copper disc and the target and to limit the temperature rise of the target during operation.

Target. For the most part, targets used have been discs 3-1/2" in diameter and 1/8" thick of sintered commercial grade $BaTiO_3$ cemented to the bottom of the target well with Astroceram (American Thermocatalytic Corp., Mineola, N. Y.). No attempt has been made to date to determine trace impurities in the target material which was designed for transducer applications. An X-ray fluorescent spectrograph, however, was run on a target sample. The intensity ratio of the K 1 line of titanium to that of the L 1 line of barium obtained was 1.1:1. In addition, X-ray diffractometer curves (Figures 22 and 23) were taken on a target sample before use and after the target had been used for 24 hours. Both curves show the pattern of tetragonal $BaTiO_3$. The target after 24 hours use, however, shows a more distinct splitting of the peaks and matches the National Bureau of Standards reference curve much more closely than the target before use. Visual observation of the target after use showed some darkening of the surface from which sputtering had occurred. A section of the used target was fractured to provide an edge view of the target through the center. It was observed that the darkening had occurred at the front surface only. The 1/16" next to the sputtered face had become much brighter yellow than the unused target. It was concluded that as a result of sputtering some reduction of the target surface had occurred and that an appreciable layer adjacent to the sputtered face had annealed and recrystallized to form more perfect tetragonal $BaTiO_3$.

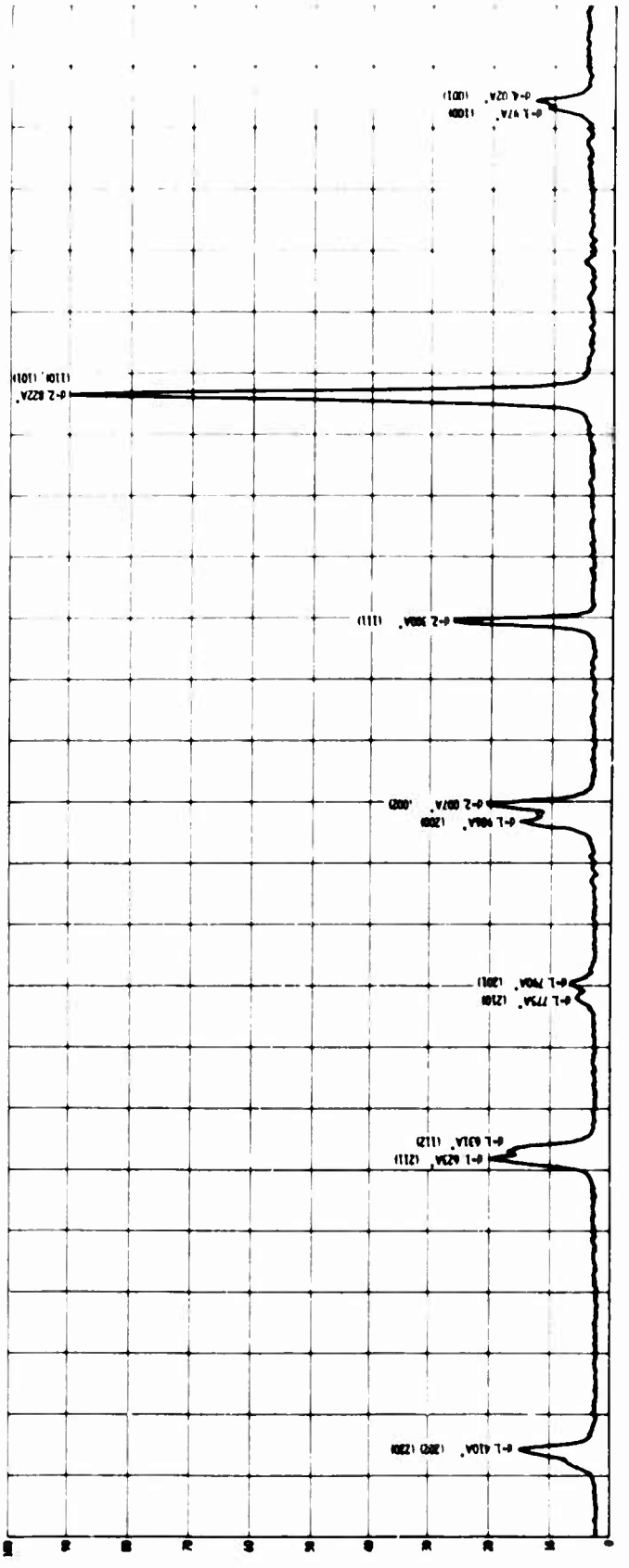


Figure 22. X-Ray Diffractometer Curve of Target Before Use

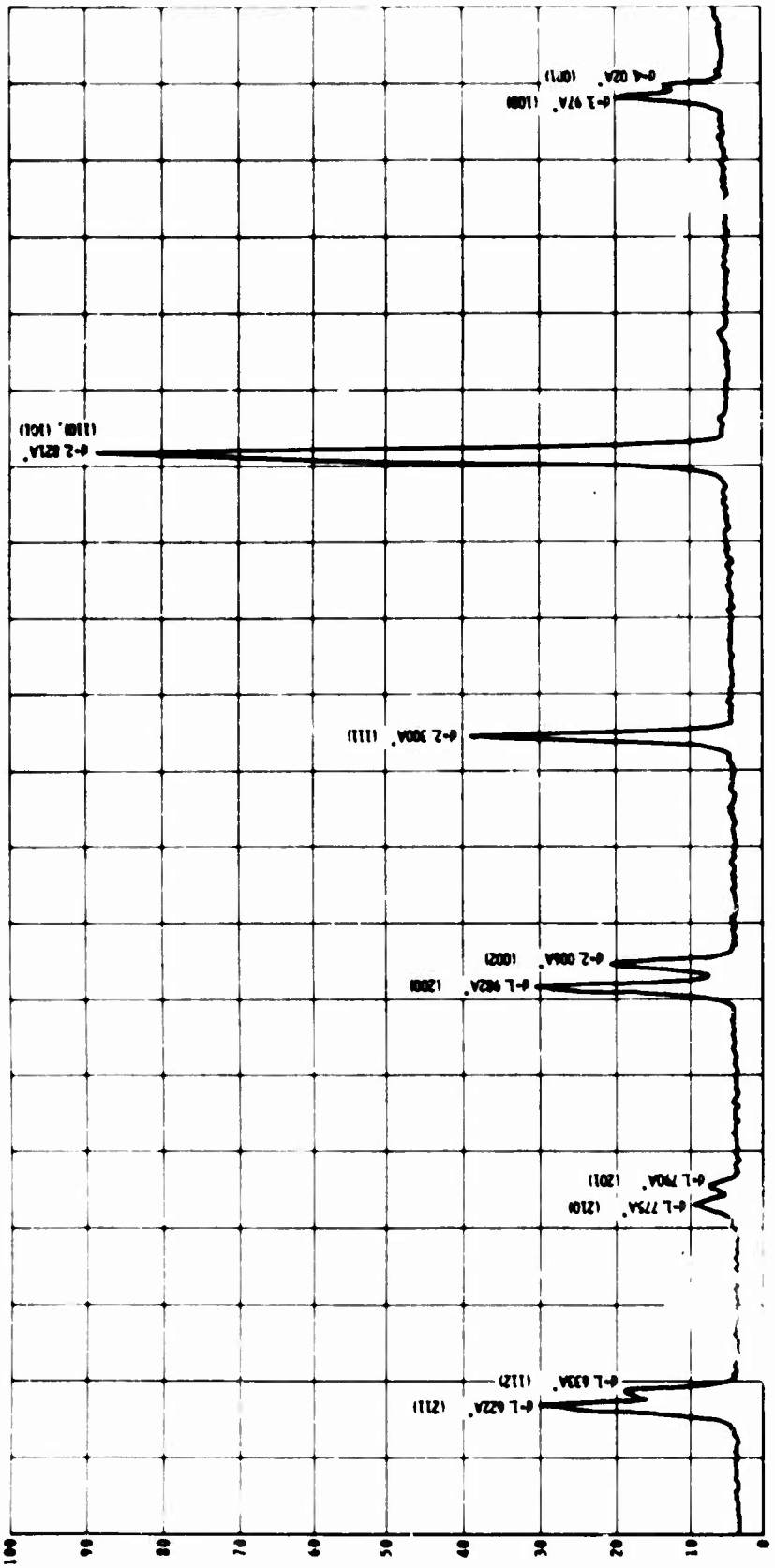


Figure 23. X-Ray Diffractometer Curve of Target After Use

A small section of unused target was lapped to a thickness of 0.015" and electroded with an evaporated gold layer on one side. Gold squares 0.063" x 0.063" were evaporated on the other side. The result of capacitance measurements on this sample are shown in Figure 24 where C and 1/C are plotted against temperature. The sample shows a Curie temperature of 128°C and follows the Curie-Weiss law at high temperatures. Room temperature dielectric constant is approximately 1100.

Initial Experiments. Before affixing the target to the target-well the apparatus was run to obtain a sample (G1) pyrex glass film. The deposit was collected on a sputtered tantalum coated microscope slide. A standard 0.063"x0.063" gold electrode pattern was evaporated through a mask over the sample for electrical measurements. Leakage current measured at 30V was less than 2×10^{-10} amps. Capacitance was 420 pfds at 1 kilocycle and independent of frequency up to 5 megacycles. Film thickness was approximately 2500 Å. The calculated dielectric constant of approximately 5.2 is comparable to the 4.0 to 6.0 value attributed to glasses.

A number of films were then prepared from a barium titanate target to obtain a feel for the operation of the apparatus and to determine the most significant deposition parameters. These are summarized in Figure 25. All samples were deposited on sputtered tantalum predeposited on glass microscope slides or 7059 glass and after deposition were electroded with a standard 0.063" x 0.063" gold pattern. Measurements

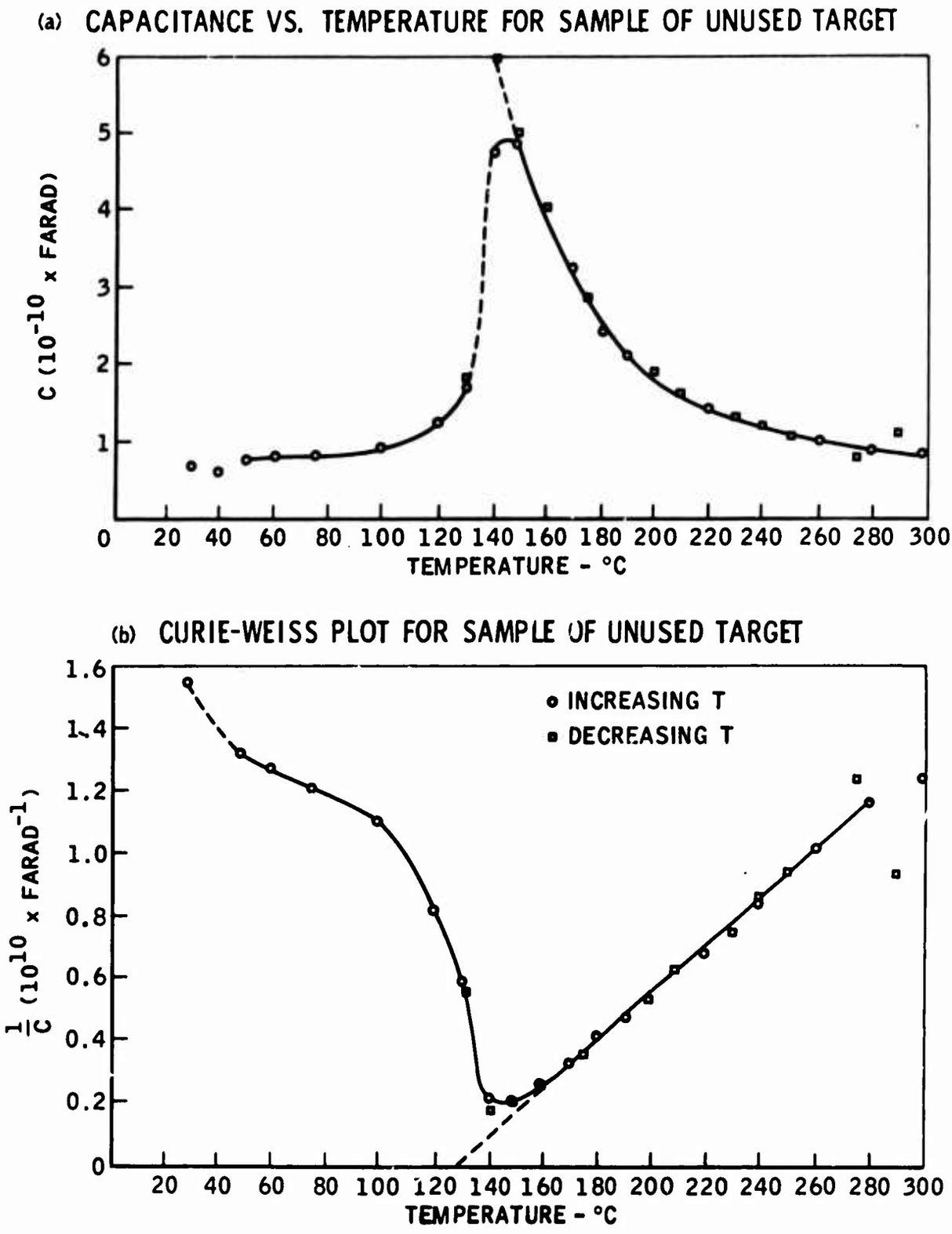


Figure 24. Capacitance vs. Temperature for Sample of Unused Target

Deposition Number	Target	Sputtering Gas	Deposition Time in Hrs.	Remarks
B_1	$BaTiO_3$	Argon		Target imploded after 1/2 hr. operation
B_2	"	"	1-3/4	New target
B_3	"	95% Argon +5% Oxygen	"	
B_4	"	Argon	"	
B_5	"	"	"	
B_6	"	"	"	
B_7	"	95% Argon	"	
B_{12}	"	Argon	3	
B_{13}	"	95% Argon 5% Oxygen	7	
B_{14}	"	Argon		Target fractured at 5-1/3 hrs.
B_{17}	"	Argon	1-1/2	New target
B_{26}	"	Argon	3	Hot substrate

Figure 25. Summary of $Ba\,TiO_3$ Films Prepared

performed on the samples included: capacitance as a function of frequency, capacitance as a function of temperature, X-ray fluorescent spectrographs, X-ray diffractometer curves, X-ray powder diffraction prints and electron surface replica micrographs. The "capacitance as a function of temperature" tests were the only ones performed on all samples. Other tests were performed on some samples only.

Preparation of Samples. Samples were prepared for X-ray diffractometer curves by merely positioning them into the sample holder of a Norelco X-ray diffractometer. In order to obtain a pattern of randomly oriented material for identification and comparison purposes the following technique was developed when simple scraping of the films failed to produce usable samples. A dilute solution of parlodian (a commercial peel film solution) was spread over the sample areas and allowed to dry. This coating was then scraped off using a sharp flat faced tungsten carbide cutting tool. This effectively scratched through the sputtered films and the particles adhering to the parlodian were thus collected. The samples were then softened with a small amount of amyl acetate and rolled into a .022" diameter fiber for exposure in a Debye-Scheuer powder camera.

Samples were prepared for electron micrographs by first covering the surface with a 3% parlodian/amyl acetate solution. When dry, these parlodian films were stripped off and discarded leaving a surface free of contamination. Replicas were then taken with the parlodian solution, shadowed at a 45° angle with evaporated germanium. Shadowed replicas were then re-replicated with carbon evaporated normal to the sample surface. The parlodian replicas were then dissolved and the preshadowed carbon replicas mounted on grids for examination.

Measurements. Capacitance as a function of temperature was measured at 1 Kc with a GR type 1650A impedance bridge driven by a HP type 200 CD wide range oscillator. A specially designed sample holder allowed the temperature to be slowly raised from room temperature to 300°C over a period of one hour. Capacitance as a function of frequency was measured between 1 and 50 Kc using the above described test setup. Measurements between 0.3 and 5 Mc were made on a Wayne Kerr B601 radio frequency bridge driven by a HP type 606A signal generator. A Rohde and Schwarz type USVH-BN1521 microvoltmeter was used as a high frequency null detector.

Results. X-ray fluorescent spectrographs for the unused target, Sample B2 and Sample B7, are shown in Figure 26. Ratios of titanium to barium as calculated from the intensity of the K 1 titanium to that of the L 1 barium line are given below:

Ratio Titanium/Barium

Sample	Ratio (Ti/Ba)
Unused Target	1.1
B2	1.3
B5	1.6

X-ray diffractometer curves for Samples B2, B3, B5, B13, B14, and B17 are shown in Figure 27. The curves in all cases show a single strong peak corresponding to the (110) plane in tantalum and a second unidentified peak. The noticeable lack of, or attenuation of

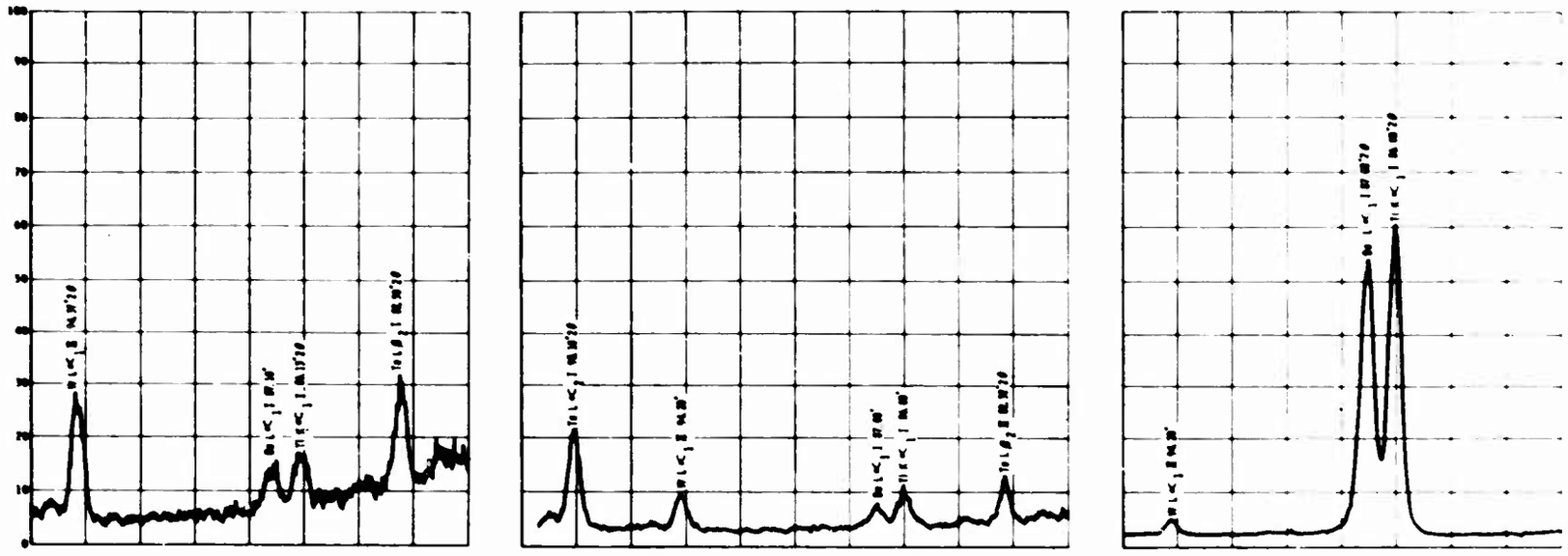
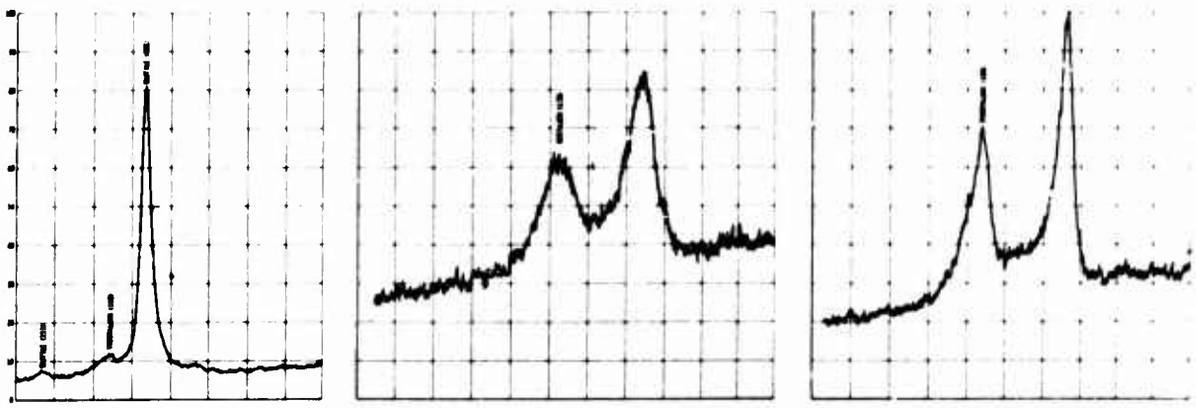
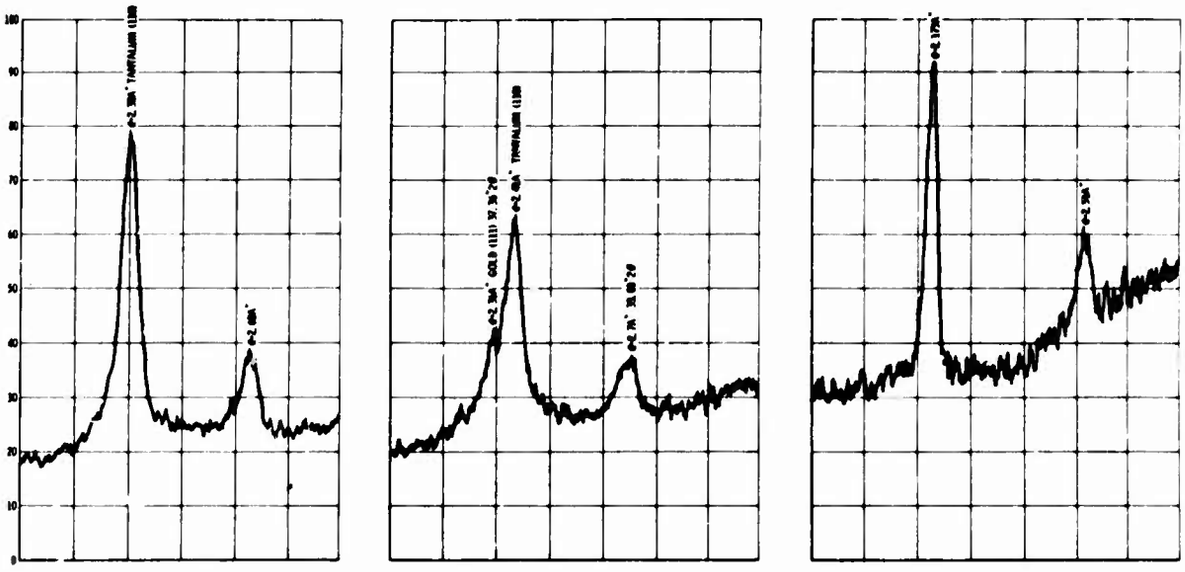


Figure 26. X-Ray Fluorescent Spectrographs



SAMPLE # B3 SAMPLE # B2 SAMPLE # B5

(a)



SAMPLE # B13 SAMPLE # B14 SAMPLE # B17

(b)

Figure 27. X-Ray Diffractometer Curves

secondary peaks of tantalum would indicate that the tantalum film used as a substrate has an extremely strong preferred orientation. The second peak must at this time remain unidentified as it is not possible to give a positive identification from the d-spacing of only one crystallographic plane particularly when d-spacing shift due to solid solution formation may occur. Some of the possibilities for this peak are

BaO_2 (110) --- 2.7 A°

Ti_3O_5 (203) -- 2.68 A°

Ti_2O_3 (104) -- 2.71 A°

$BaTi_3O_7$ -- 2.67 A°

BaO (200) --- 2.75 A°

X-ray powder diffraction prints of specimens prepared from Samples B13, B14 and B17 made in an attempt to identify the line observed in the diffractometer curves failed (even after 20 hours exposure) to reveal any lines except those belonging to the tantalum substrate material.

Electromicrographs of the surface replicas showed all the samples to be essentially the same in regard to surface topology. Figure 28 is taken from a thin Sample B5 and Figure 29 from a thick Sample B12. The magnification employed is approximately 50,000X and the distance between the inner edges of the two black bars represents a distance of one micron on the surface. The surface irregularities observed are less than 50 A° in size and no pinholes, voids, or cracks are observed. Evidence of crystallization is almost completely absent.

(Magnification : 48,000 X)

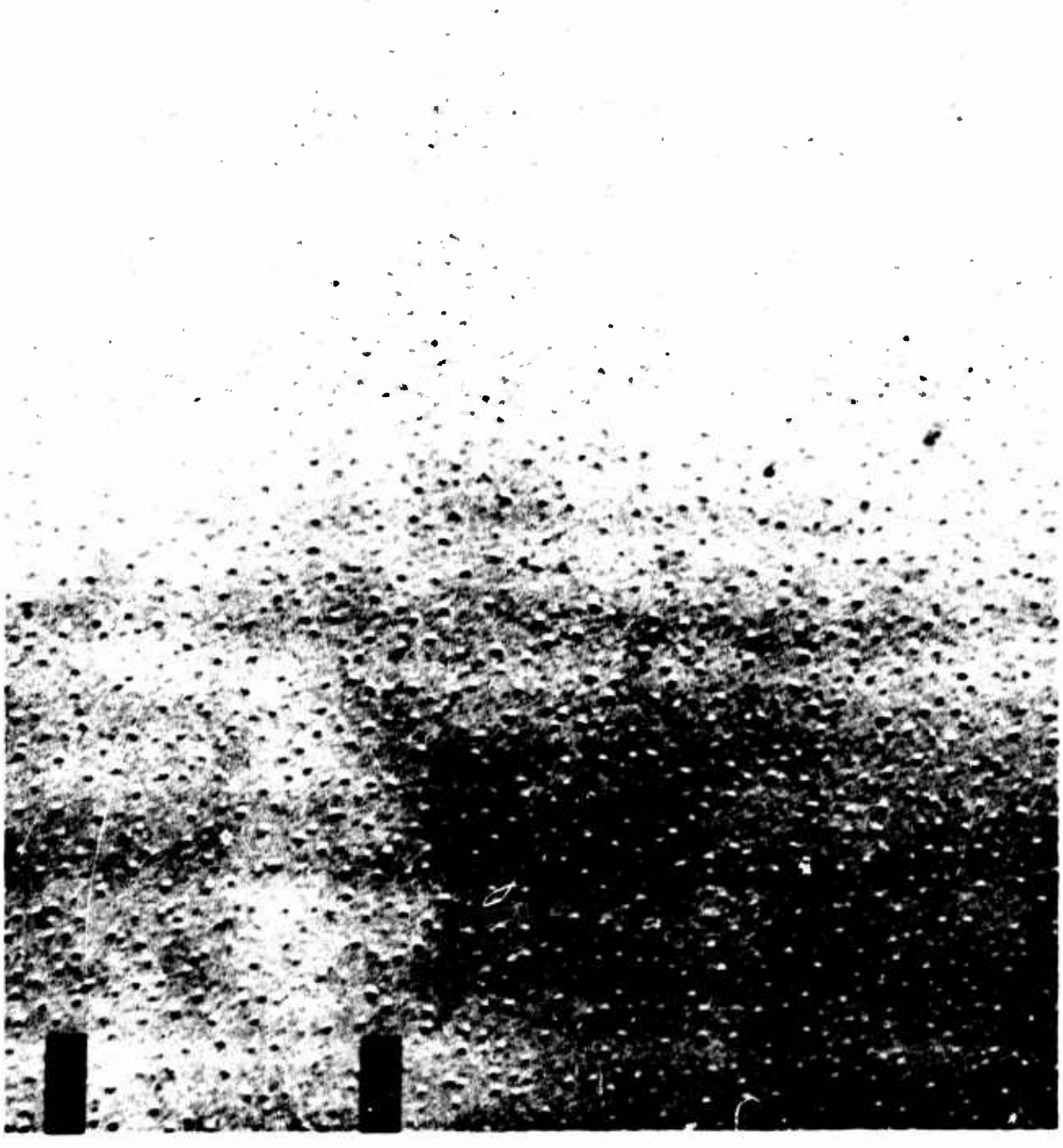


Figure 28. Electronmicrograph of Thin Sample B5

(Magnification: 51,000 X)

Figure 29. Electronmicrograph of Thick Sample B12

While no attempt was made to optimize the electrical properties of these films, low frequency capacitance measurements show them to have room temperature dielectric constants of between 50 and 80 depending on the exact deposition conditions used. Even the thinnest films showed essential 100% yield of good electrical units. Capacitance as a function of frequency measured on Sample B1, Figure 30, shows that a rapid decrease in capacitance and increase in dissipation factor occurs just below 2 Mc. Capacitance as a function of temperature, Figure 31 and 32, failed to show the ferroelectric anomaly at 120°C normally associated with tetragonal barium titanate. Sample B2, however, showed a large anomaly at 230°C and Sample B5 showed a small anomaly at the same temperature. All other samples tended to show a slow increase in capacitance between room temperature and 300°C.

Preliminary tests, electronmicrograph and X-ray diffraction, run on Sample B26 show evidence that some surface recrystallization occurred in this deposit on a heated substrate. A slight rise was observed in the X-ray diffraction chart at approximately d = 2.84A. This is the position of the strongest diffraction maximum of tetragonal $BaTiO_3$. Although the appearance of this one line alone cannot be accepted as positive identification of this phase, no other likely phases have strong reflection in this range.

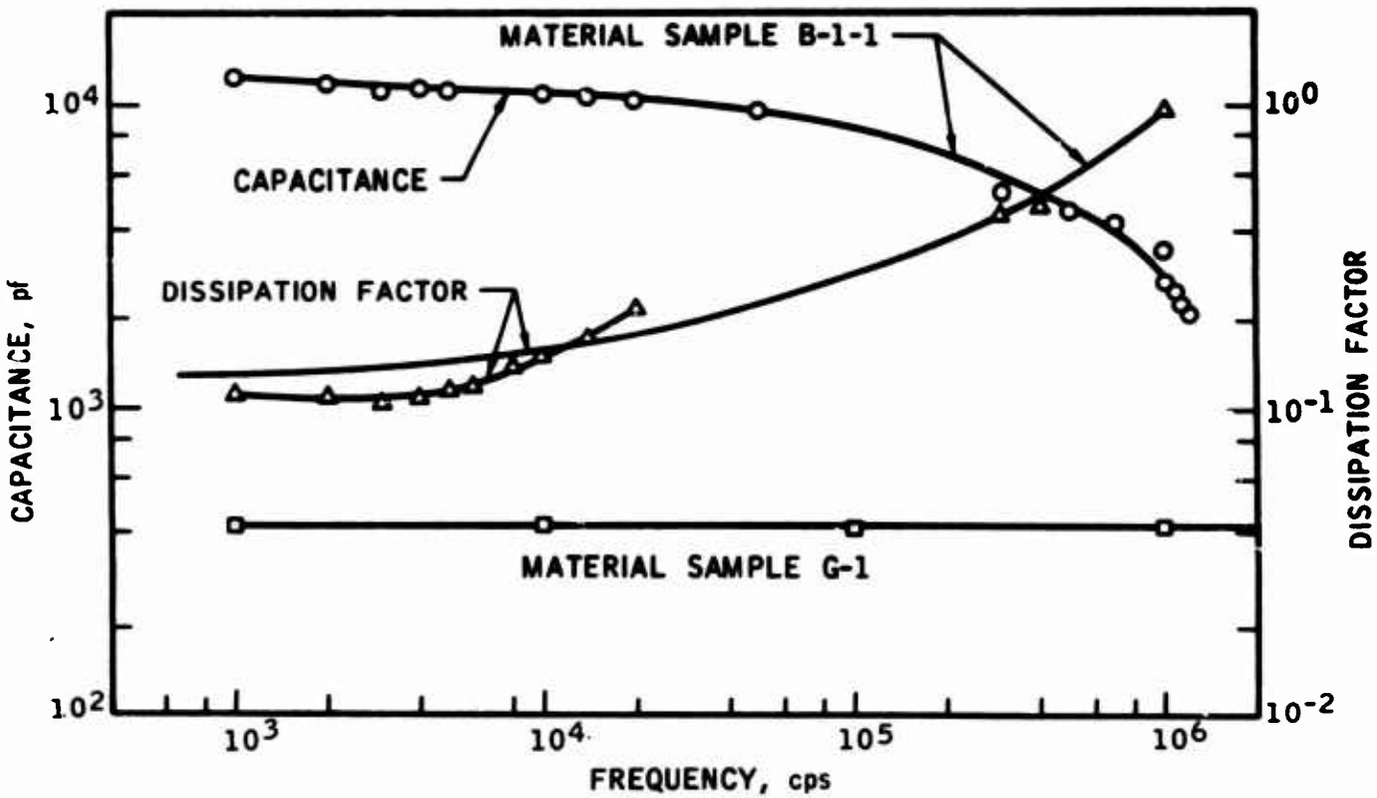


Figure 30. Radio Frequency Sputtering Test Data

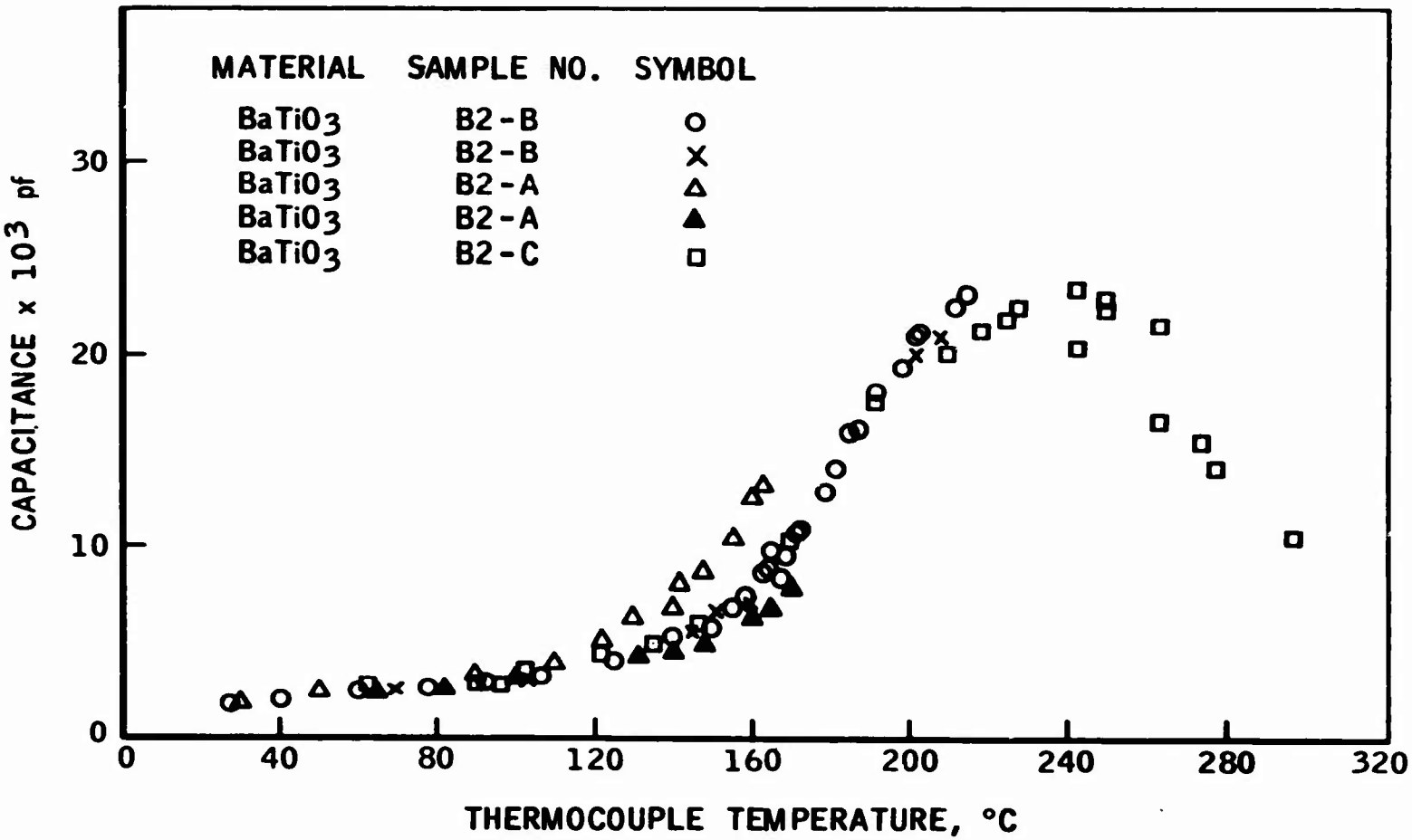


Figure 31. Radio Frequency Sputtering Test Data

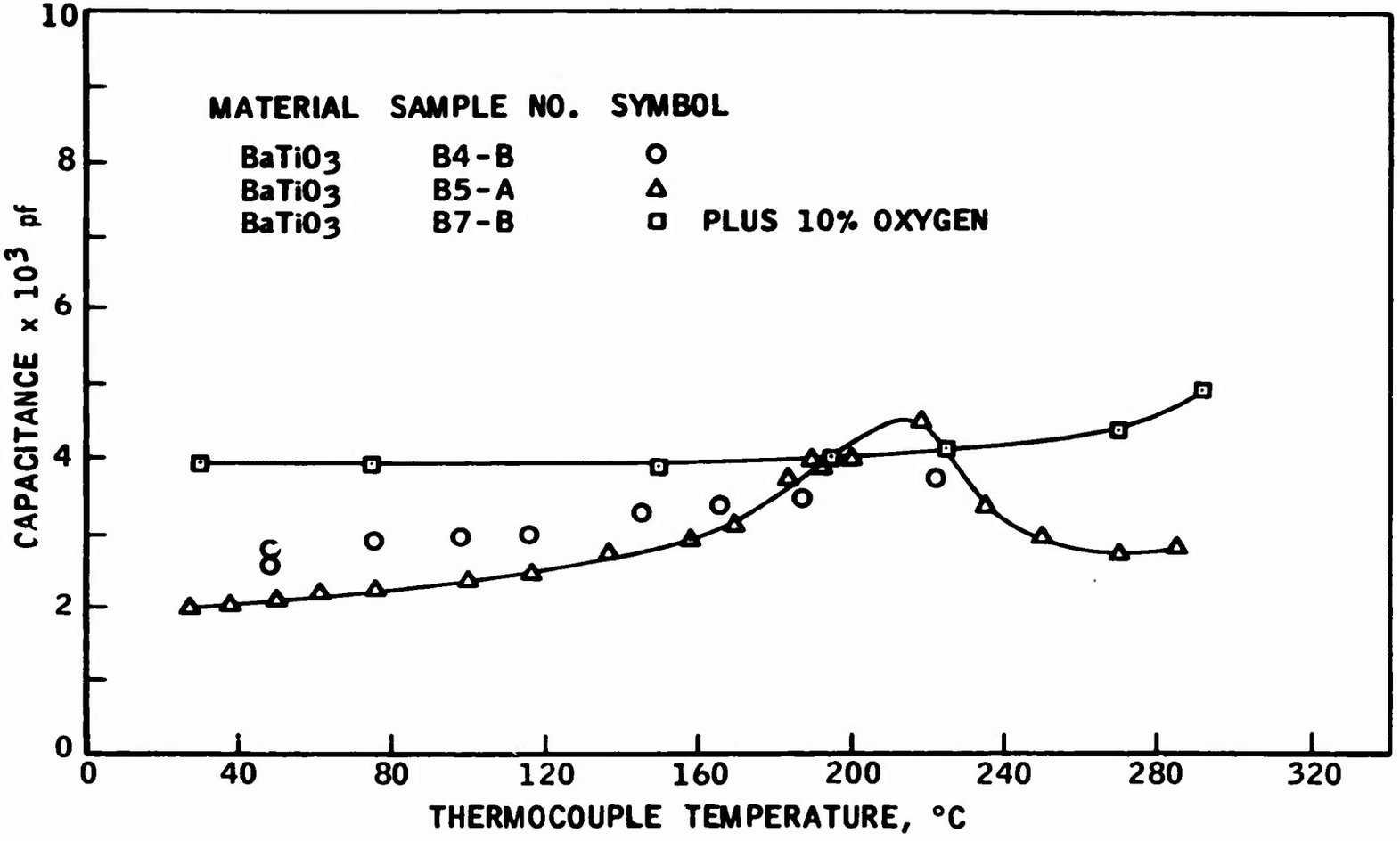


Figure 32. Radio Frequency Sputtering Test Data

Examination of all the data including X-ray, electron-microscope, and electrical measurements on films prepared to date lead to the tentative conclusion that when $BaTiO_3$ is radio frequency sputtered, material is evolved as a dissociated vapor of approximately stoichiometric proportions. Deposits condensed on unheated substrates, while of good physical quality, are largely amphorous. Initial results of sample B26 deposited on a heated substrate show some signs of surface crystallization indicating that crystalline films can be obtained on suitably heated substrate. Additional work will be required, however, before suitable films are available.

In order to investigate other possible means of economical production of ferroelectric thin films, vapor phase deposition was attempted. The main reasons for this parallel effort in conjunction with sputtering was (1) the higher rate of deposition attainable and (2) the better accessibility to control stoichiometry by measurement of the partial vapor pressures of both barium oxide and titanium dioxide including its polymeric species. To secure monocrystalline growth respectively, epitaxy and pseudo-epitaxy was used during deposition. For this purpose, true epitaxy was obtained using lithium fluoride plates of one inch diameter and one eighth inch thickness. These plates were optically polished and etched in a .005 molar concentration of sulfuric acid in order to remove dislocations produced by polishing. A second type of substrate, magnesium oxide, selected for its nearly isomorphous characteristic, was obtained in the form

of platelets approximately 3/4 inch square and 1/16 inch thickness by direct cleavage. This substrate was chosen because of its very low cost and near compatibility to the desired lattice spacing. Both types of crystal were electroded by evaporation of pure gold with a thickness between 1500 and 2000 Angstroms. This electroding performed two tasks: (1) permitted electrical measurement of the volume properties of the dielectric and (2) promoted the growth of the crystal in presenting a greater surface mobility to the condensing elements of the vapor and, therefore, a greater lifetime for association was achieved. The two substrates, in order to secure uniform crystallization, were maintained at a constant temperature during evaporation at respectively 550°C for lithium fluoride and 750°C for magnesium oxide. The reason for this difference in temperature was to maintain the vapor pressure in the vicinity of 10^{-7} torr and, therefore, obtain a negligible evaporation of lithium fluoride, whereas for magnesium oxide the vapor pressure is not a parameter of importance since it remains in the vicinity of 10^{-15} torr at 750°C. Below this value the film grows in isolated nucleations. The main problem of evaporation is to maintain the temperature of evaporation constant within narrow limits at the surface of evaporation and to avoid reaction between the evaporant and the heating source. Since the temperature of evaporation of titanium dioxide is very high, the reactivity with normal crucible material results into a reduction of the compound into titanium monoxide leaving only materials such as

indium or iridium-osmium as suitable heating boats. Heating such material by resistance with a current flowing through the boat is very impractical since both materials become very brittle and fragile and break under their own weight. A more plausible method of heating the device is by electron bombardment of a dice of iridium in which the evaporant is contained. The vapor pressure of the iridium at 2000°C is very low, namely, less than 10^{-5} torr. Small traces of iridium are observed in the film although they do not produce any measurable changes in electrical losses. Since thermometric measurements are very difficult to apply in the range of operating temperature, the control of the vapor pressure cannot be secured by applying that technique. Other means of control are contemplated by the utilization of a mass spectrometric attachment in a closed loop fashion to control the temperature.

To date the films obtained which have provided the most satisfactory results have been grown by the above technique on magnesium oxide electroded with gold. Both optical and electrical properties indicate satisfactory characteristics by the observation of "a" and "c" domains under polarized light indicative of the ferroelectric phase of the barium titanate and electrical measurement of the hysteresis loop. These results to date are essentially qualitative and more data is needed to ascertain all of the properties. The largest area of perfectly homogeneous crystal observable in this case were 3 millimeter by one millimeter with a 1.5 micron thickness. The coercive field necessary for switching was slightly lower than 0.4 volts. (The theoretical value is 0.001 volt). The discrepancy

between these values probably egresses from the electroding operation during the post evaporation processing. This assumption is supported by the observed loop asymmetry. This suggests a potential barrier most likely due to the chemical reaction of the film surface prior to the deposition of the second electrode. The results obtained above are promising enough to provide incentive for future use of this fabrication technique.

B. Discrete Electro-Optical Elements

Discrete ferroelectric and photoconductor-light source elements were utilized to implement the associative processor model. The purpose of such discrete units in a breadboard associative memory was to allow individual selection of elements. Associative processor performance can then be related to material performance to establish guidelines for further thin film development.

Assembly. Figure 33 illustrates a typical element mounted in a TO-12 can. Gating function is provided by a surface mode cadmium sulfide photoconductor illuminated by a miniature incandescent lamp.

Referring to Figure 34, basic assembly process consists of welding miniature lamp on two of the TO-12 posts, insertion and lead attachment of the photoconductor and encapsulation.

Optical source for gating is provided by a miniature Sylvania ML 202A lamp of .055" diameter and 0.175" length. Lamp drive requirements of 11 ma at 1.4 volts allows direct use of transistor drive circuitry.

A surface mode photoconductor was employed which is 0.2" in length and of gap width .030". Preparation of discrete photoconductor elements was carried out as follows: Thin film cadmium sulfide photoconductors doped with chlorine and silver were prepared by a two step process consisting of vacuum deposition and subsequent air bake. Each evaporation run can produce twenty or more cadmium sulfide plates of 1" square geometry. The film was deposited on Corning Type 7059 glass

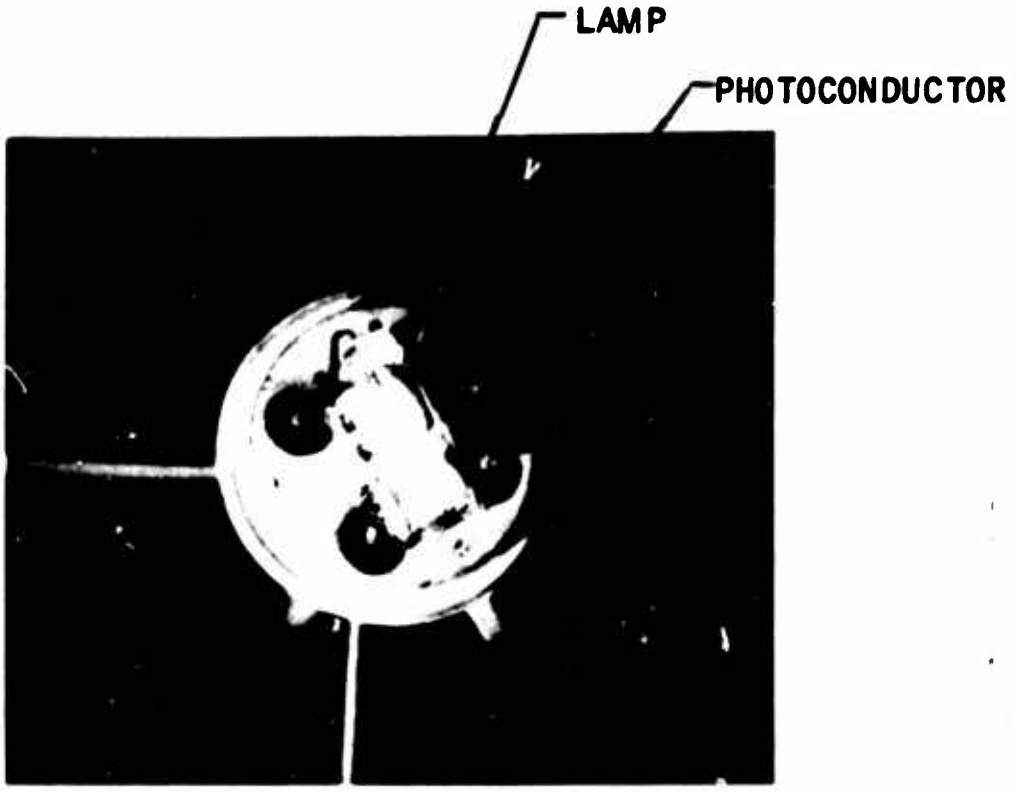


Figure 33. Discrete Optoelectronic Gate Element

(1) TO-12 4 LEAD HEADER
(2) SYLVANIA ML-202A LAMP
(3) CdS SURFACE MODE PHOTOCONDUCTOR
(4) ASSEMBLED OPTOELECTRONIC GATE
(5) FINAL ENCAPSULATION

Figure 34. Gate Element Assembly Operation

substrates of 1" x 1" x .032" size. After post-evaporation activation of film each substrate was electroded with vacuum deposited indium electrodes to yield a gap of .030" width. Each substrate was cut to size to provide 20-25 elements of 0.1" x 0.2" size for mounting in TO-12 transistor headers. Lead attachment from TO-12 header posts (Figure 34) to indium photoconductor electrodes was accomplished with conductive epoxy. Approximately one hundred thirty such elements were assembled.

Average Performance. Basic design criteria for usable units was the following: 1) sufficient photocurrent to switch ferroelectric element in a reasonably short period, 2) sufficiently low dark current to prevent switching in the blocked state.

As an example of 1) consider the following:

(switched) $Q = 5 \times 10^{-9}$ coulomb

the light current for an average unit, $i = 2 \times 10^{-5}$ amp at 6 volts

then $t = 250$ microseconds

Figure 35 tabulates typical light and dark current measurements for devices assembled to date. A larger portion of this type of data is presented by Figure 36. Point A of Figure 36 represents an optoelectronic gate element from photoconductor run 77 with the following characteristics:

light current $= 2.6 \times 10^{-5}$ amp at 5.4 volts (230 kilo ohms)

light/dark current ratio $= 10^{4}$ or dark resistance (2300 megohm)

GATE ID NO.	'LIGHT' CURRENT[1,2] $i_L \times 10^{-5}$ amp	'DARK' CURRENT[1] $i_D \times 10^{-10}$ amp	CURRENT RATIO $i_L/i_D \times 10^4$
(RUN 77) G-1	2.1	3.0	7.
G-3	1.7	0.2	85.
G-12	1.2	30.	0.4
G-18	1.5	10.	1.5
(RUN 75) B-1	1.5	1.0	15.
B-15	3.0	600.	0.05
B-36	3.5	130.	0.27
(RUN 95) Y-1	5.0	3.5	14.
Y-16	3.3	250.	0.13
(RUN 97) V-1	0.03	2.	0.15
V-21	1.	8.	1.2

(1) Current at 5.4 volts dc (2) Lamp at 1.35 volts dc

Figure 35. Optoelectronic Gate Element Typical Data

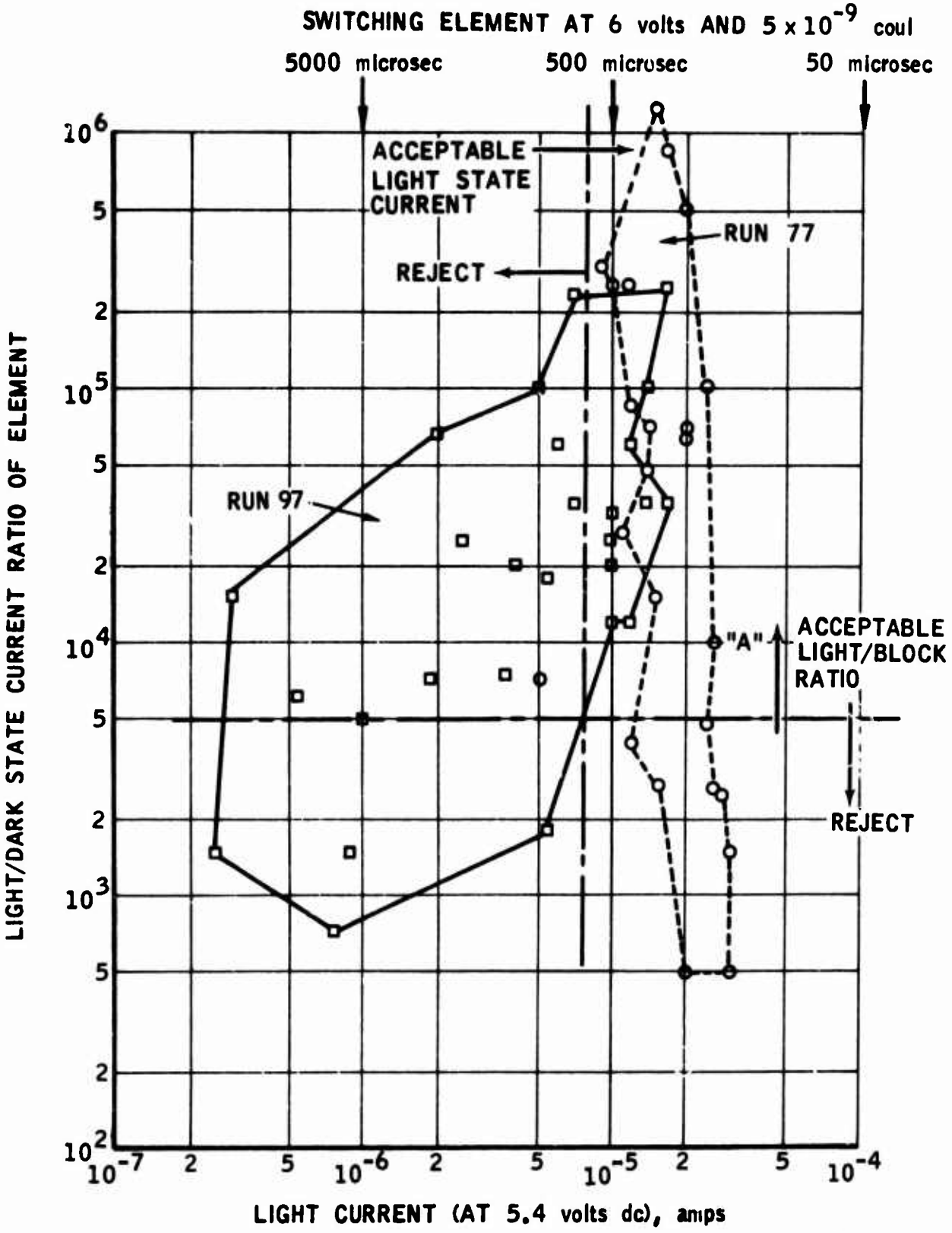


Figure 36. Performance Distribution of Packaged Opto-Electronic Gate Elements

Data on 50 of 130 elements assembled to date are shown by Figure 36. The spread in data is sufficient to preclude assignment of average values. For example, run 77 of Figure 36 has three orders of magnitude variation in light/dark current ratio. This is principally due to the increase of dark current. The small variation in light current represented by abscissa of Figure 36 is presumably due to the variation in photoconductor gap length or lamp output. On the other hand, the variation in data from run 97 of the figure indicates non-uniform photoconductor sensitization.

Criteria for acceptable units is represented by dashed lines (Figure 36) for minimum light current and light/dark current ratio. The term acceptable is in terms of the breadboard model only, not a final design criteria.

It should be noted that data shown is for developmental photoconductor evaporation runs. The purpose of such developmental evaporation runs was to substantially reduce photoconductor rise and decay time constants below that of a prior deposition technique. Hence, the spread in performance is much greater than would be obtained with a stabilized optimum deposition process. In an optimized process nearly all units would fall in upper right quadrant of Figure 36.

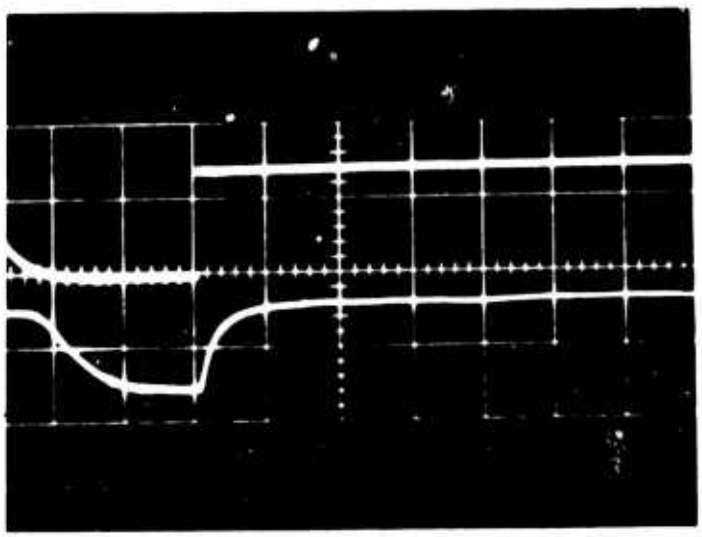
Photocurrent Dependence on Lamp Drive. Table II tabulates element resistance as a function of lamp drive. At 1 volt a normalized resistance of one unit exists. Increasing the drive to 2 volts reduces resistance by a factor of six in normalized units. However, increasing drive voltage and current reduces lamp life. At 1.2 VCD rated life is 500 hours continuous operation, while at 1.7 volts life is less than 1 hour.

PHOTOCONDUCTOR RESISTANCE AS FUNCTION OF LAMP POWER

LAMP			PHOTOCONDUCTOR
Voltage	Current	Power	Normalized Resistance
1.03	15 mA	15.4 mW	1.00
1.22	16	19.5	0.41
1.30	16.5	21.5	0.34
1.48	17.2	25.5	0.24
1.58	17.5	27.6	0.21
2.0	19	38	0.16

Under pulsed operation as in associative memory operation lamp drive can be increased without severe degradation in life. For example, under pulsed conditions, illustrated by Figures 37 and 38, a unit gate element was operated in excess of 3 million flashes, with 1.4 volts pulse applied to lamp (upper trace of Figure 37) with a 7% duty cycle. Lower trace of Figure 38 is the photocurrent transient response. As indicated by the figure, the photocurrent decay time is 10-15 milliseconds, which is due to two factors: 1) photoconductor decay time, 2) relatively slow turn off of optical source (Figure 37) due to the thermal inertia of the filament.

Dark State Impedance. Properly prepared photoconductive films of optimum characteristics exhibit light/dark current ratios of 10^8 to 10^9. Current ratios of this magnitude are for saturation illumination (1000 footcandles) to total absence of residual illumination

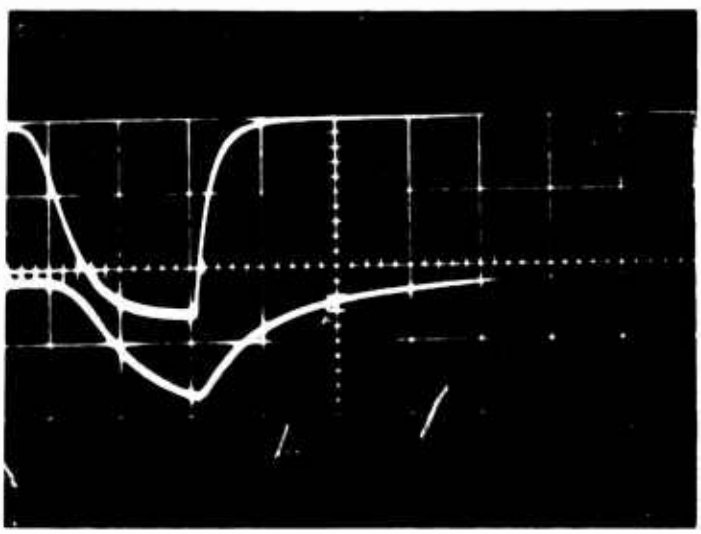


UPPER TRACE –
LAMP VOLTAGE AT 1 volt/div

LOWER TRACE –
LAMP ILLUMINATION
AS SENSED BY PHOTODIODE

TIME BASE, 5 microsec/div

Figure 37. Response Time of Gate Element Optical Source



UPPER TRACE –
LAMP ILLUMINATION
AS SENSED BY PHOTODIODE

LOWER TRACE –
CdS PHOTOCURRENT
AT 2.25×10^{-5} amp/div

TIME BASE, 5 microsec/div

Figure 38. Optoelectronic Gate Element Photoconductor Response Time

(less than 10^{-7} footcandles). Ratios obtained for two photoconductor developmental runs are illustrated by Figure 35. Two of elements shown near the top of that figure have a light/dark ratio of 10^6 despite the low (50-80 footcandle) illumination provided by the miniature lamps.

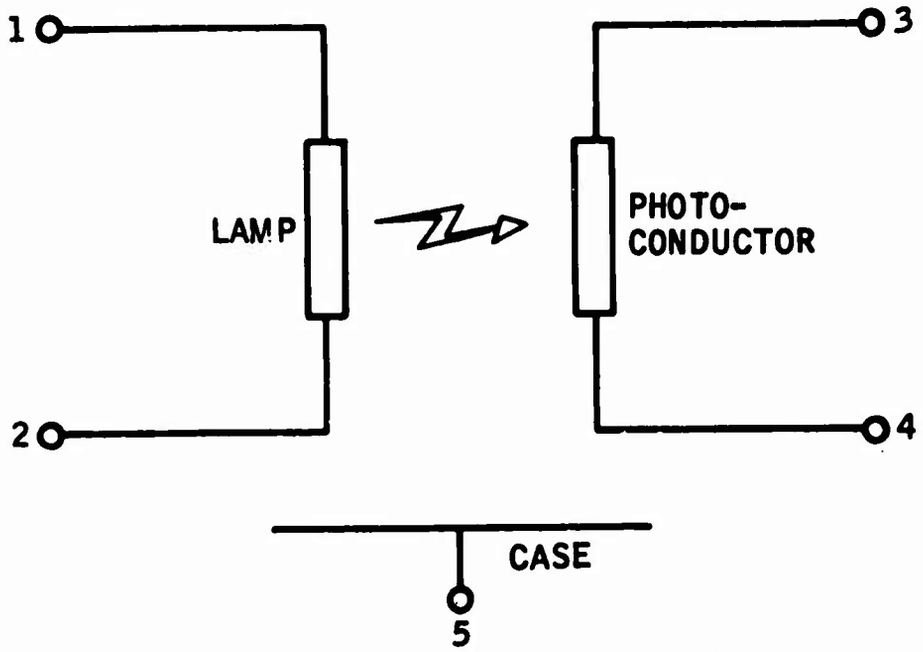
Referring to Figure 35 a light/dark current ratio of 10^4 is exhibited by more than 50% of the units. For an average light current of 1.5×10^{-5} amp at 5.4 volts this corresponds to a dark resistance of 3.6×10^9 ohms. According to Figure 39 the two terminal capacitance C34 of an average element is 0.58 picofarad. Accordingly, an 'average' value for blocked state impedance is:

$$R = 4 \times 10^9 \text{ ohm}$$

(dark state)

$$C = 0.6 \times 10^{-12} \text{ farad}$$

While this perhaps represents a minimum capacitance due to the package of the discrete element, it by no means represents maximum dark resistance which can be obtained with well compensated photoconductive material. It should also be noted that above values correspond to a surface mode photoconductor of 0.02" length and 0.030" gap. Employment of volume mode photoconductivity or surface mode gap of varying geometry allows wide variation in light and dark impedance levels which can be obtained.



C_{34} = 0.58 picofarads

C_{13} = 0.80 picofarads

C_{15} = 0.88 picofarads

C_{25} = 0.85 picofarads

FOR C_{ij} i,j ARE TERMINAL NUMBERS

Figure 39. Package Capacitance of Optoelectronic Gate

C. Single Crystal Ferroelectric Elements

Each word of the breadboard associative memory consists of a 3 x 16 configuration of ferroelectric-photoconductor pairs. A discrete package is employed for each ferroelectric cell as illustrated by Figure 40.

Cell Assembly. A number of improvements in chemical processing and mechanical processing of elements have been made during this phase. Work was initiated to improve surface preparation in the form of moderated etchant solutions, visual checks and thickness measurement.

Subsequently, effort was directed at application of photoresist and etch technique for the following reasons: 1) to eliminate damage inherent in mechanical dicing, 2) to obtain uniform geometry, preferably a die concentric about the electrode area. This effort was only partially successful due to fragility of TGS material - which precludes a high yield with the multi-step photoresist technique.

In view of relatively poor adhesion of evaporated silver to the TGS surface, a possible cause of degradation, electrodes of silver-epoxy were investigated. Samples so prepared resulted in a rather high coercive field due to the poor contact provided by the epoxy-silver mixture.

In the course of the above investigation, it was determined that samples prepared with evaporated silver electrodes and an overlay of silver-epoxy performed well and exhibited little or no change in characteristics with time.

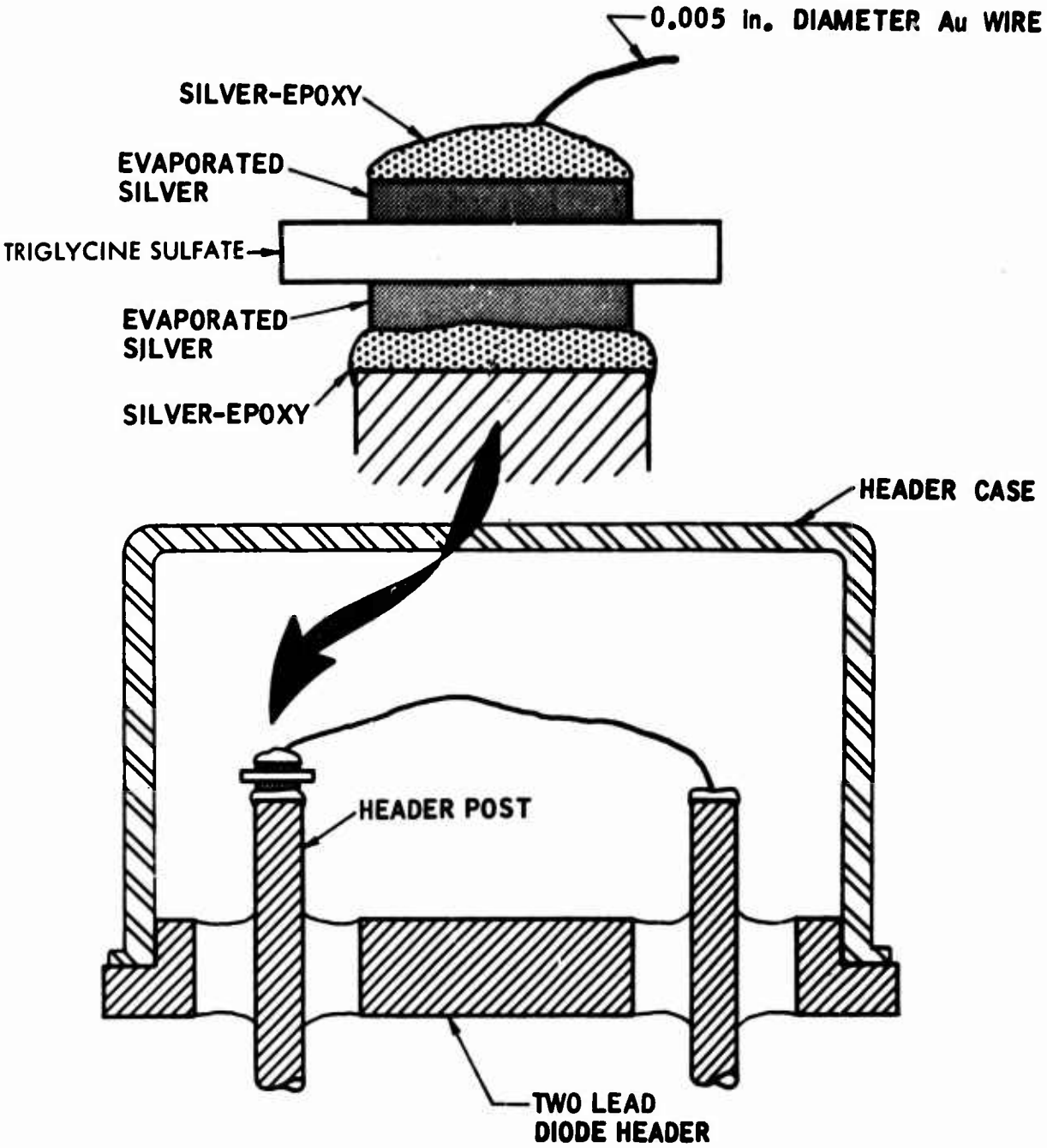


Figure 40. Ferroelectric Cell Mounting in Diode Header

Accordingly, work proceeded on production of associative memory elements mounted in transistor type header, Figure 40. The TGS element mechanically diced to small area is mounted on one header post with silver-epoxy Dupont type 5504-A (thermosetting). The top contact is made via small (.005") diameter gold wire with reliable contact to evaporated silver electrode assured with silver-epoxy.

The preparation sequence proceeds as follows:

(1) Simple morphology of triglycine sulfate allows visual determination of 'c' axis. Cleavage normal to 'c' - axis yields plates 15-30 mils in thickness and 0.5 to 2 cm^2 in area.

(2) Lap to approximately 6 mils thickness with dry (400 and 600 grit abrasive paper) and wet (10 and 16 micron SiC abrasive slurry).

(3) Pole in alcohol with 500 volts dc.

(4) Removal of lapping damage with slow etch (2 mil/hr) consisting of a 2:1 ratio by volume of methyl alcohol and water.

(5) Surface etch prior to electroding to yield lowest coercive voltage with 4:8:1 ratio of water, alcohol, and hydrochloric acid. Insofar as this is a quite rapid etch, several seconds only is necessary, followed by immediate alcohol quench.

(6) Vacuum deposition through evaporation mask of .015" diameter silver electrodes (approx. 2000 A°) consisting of symmetrical dot pattern on opposite surfaces.

(7) Mechanical dicing of multi-element slabs results in TGS elements of approximately .050" diameter with .015" dot electrodes in the center.

(8) Mounting of elements in two lead header with electrical contact to header via conducting silver preparation Dupont 5504-A.

(9) Cycle elements (at 60 cps) while silver is drying.

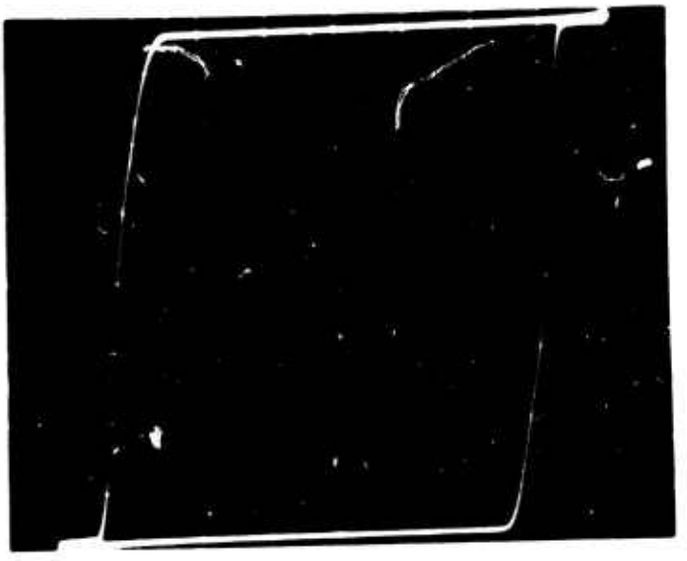
(10) Attach can to header to complete packaging.

Ferroelectric Cell Measurement. Two types of measurement have been performed: 1) 60 cps hysteresis loop characterization as tabulated by Figure 41 and defined by Figure 42 and 43; 2) pulse measurement of switching interval and charge switched, Figures 44 and 41. Such measurements quantify element performance for the following purposes: 1) determination of average cell performance for associative memory application, 2) selection of units for associative memory, and 3) determination of degradation via quantified tabulated data.

Average Cell Characteristics. Figure 41 tabulates five basic measurements $2Q_{rs}$, $\pm V_1$, $\pm V_2$, C_1, C_2, defined by Figure 43. Tabulation given is for typical data taken on approximately 130 such elements. Average values which may be employed for equivalent circuit representation (Figure 45) are:

FERRO-ELECTRIC CELL I.D.	60 H_2 HYSTERESIS LOOP CHARACTERIZATION							9 volt PULSE	
	$2Q_{rs}$ $\times 10^{-9}$C	V_1		V_2		C_{1+} pF	C_{2+} pF	ΔQ $\times 10^{-9}$C	Δt $\times 10^{-6}$sec
		+	-	+	-				
15	4.5	4	5	7	7.5	5.1	2600	4	140
16	4.3	4.5	4.8	7	7	5.1	1950	3.8	300
17	4.6	1.5	2.2	3.5	4.5	4.5	2270	5	250
18	4.5	4	5.5	8	9.5	5.3	1800	3	250
19	4.1	4.2	4.5	7	6.5	11	3800	-	-
20	4.0	1.5	1.8	2.8	3	5.8	2500	4	40
35	4.6	2.5	2.8	5	4.7	5.5	1950	4.4	500/500
36	4.5	2.8	3	5	4.5	5.5	1600	4.4	250
37	4.6	2	2.2	4.5	4.8	7.1	1950	-	-
38	4.4	2.2	3	4.5	5	4.5	1950	4.2	300
39	4.0	3	2	7	4.5	4.5	650	3.2	150/500
40	4.6	1.8	2.3	3.3	4.0	8.4	3800	4.7	150/250
115	ASYMMETRIC-REJECT								
116	4.7	3	4	7	8	7.1	2600	5.7	300
117	4.1	2	3	4.5	3	4.4	3800	4.3	75
118	5.3	3.5	3.5	5	5.5	5.8	2600	4.9	200
119	4.3	0.7	1.0	2	3.3	5.8	3600	POOR 1/0 RATIO	

Figure 41. Typical Data for Ferroelectric Cells



VERTICAL AXIS Q
AT 6.5×10^{-10} coul/div

HORIZONTAL AXIS V
AT 2 volt/div

TIME BASE, 100 microsec/div

Figure 42. Hysteresis Loop Characteristics

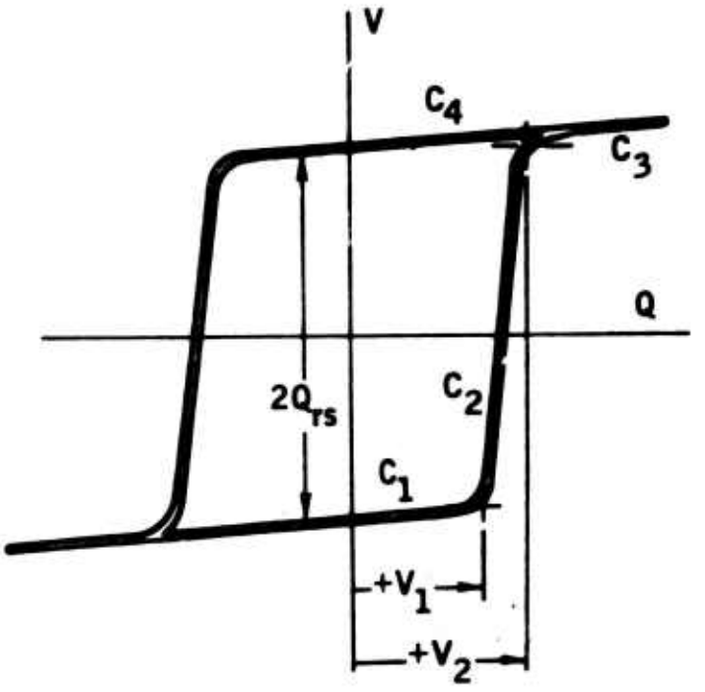
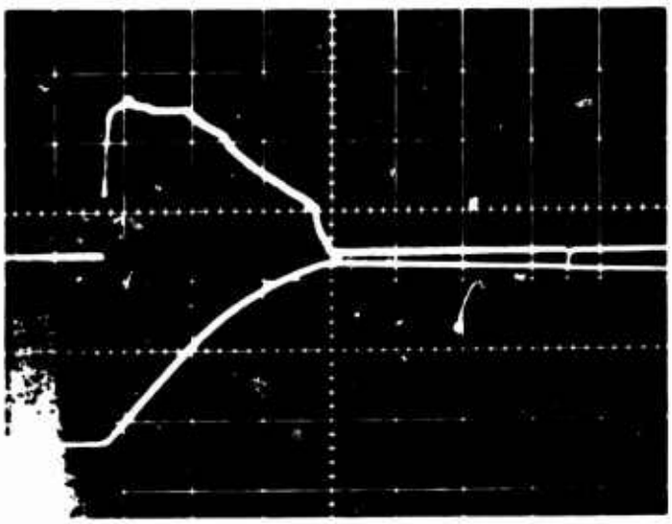


Figure 43. Sixty Hz Saturation Hysteresis Loop

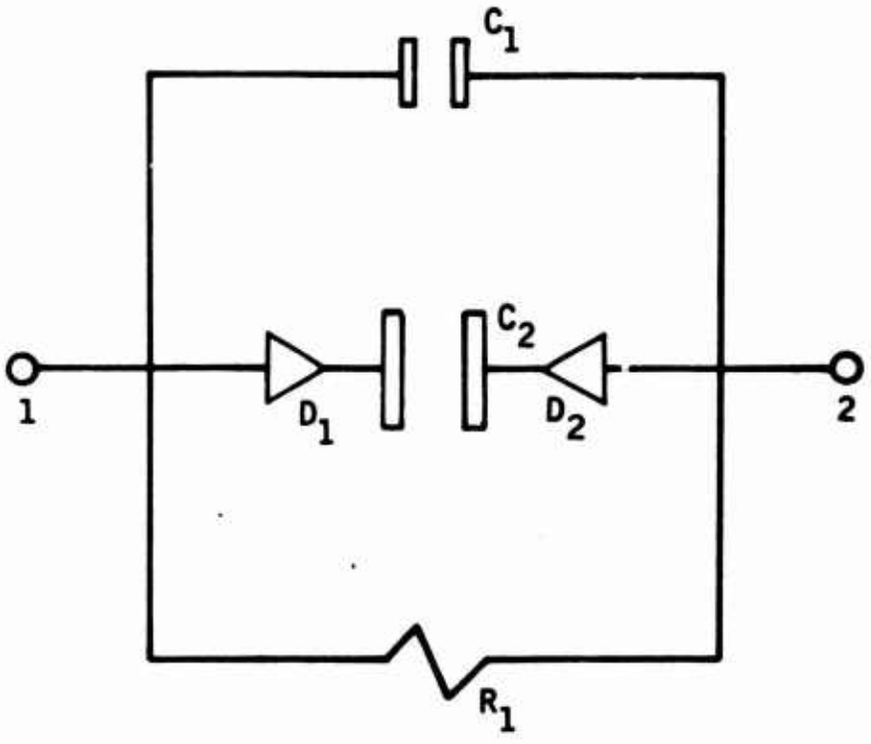


UPPER TRACE --
CURRENT AT 10^{-5} amp/div

LOWER TRACE —
CHARGE AT 2×10^{-9} coul/div

TIME BASE, 100 microsec/div

Figure 44. Switching Current and Charge Waveform



C_1 = 2500 picofarads

C_2 = 6 picofarads

$\pm V_1$ = 2.4 volts

V_2 = 4.7 volts

DIODES D_1, D_2

1) FORWARD, NO THRESHOLD

2) REVERSE, CONDUCT ONLY BETWEEN 2.4 AND 4.7 volts

PARALLEL RESISTANCE R_1

1) VOLUME dc LEAKAGE

2) SURFACE dc LEAKAGE

Figure 45. Triglycine Sulfate 0.015 Inch Diameter Element Equivalent Circuit Representation

C_1 = 6 picofarads

C_2 = 2500 picofarads

V_1 = $\pm$ 2.4 volts

V_2 = $\pm$ 4.7 volts

$2 Q_{rs}$ = 4.7 microcoulombs

Circuit representation (Figure 45) may be used for design analysis. Diodes shown are two stage elements which conduct only between 2.4 and 4.7 volts reverse bias, and have no threshold in forward bias.

Switching Interval. Figure 46 illustrates field dependence of switching speed for an 'excellent' and 'poor' element. Note that with a 10 volt pulse #43 requires 340 microseconds to switch, while #20 switches in 30 microseconds. Tabulated data of Figure 41, ΔQ and Δt, indicates spread in switching interval.

A series configuration of sixteen elements will presumably switch in an interval which is an average of the individual elements. With 9 volts/element we have an average value of 230 microseconds.

(ave) Δt = 230 microseconds at 9 volt

To decrease Δt the voltage must be increased as shown by Figure 46.

Saturation Polarization. Polarization measurements are tabulated in Figure 41 for both 60 cps and pulse conditions. Average polarization is 4.7×10^{-9} coulombs. Insofar as elements in series should have nearly equal polarization, elements have been selected as follows:

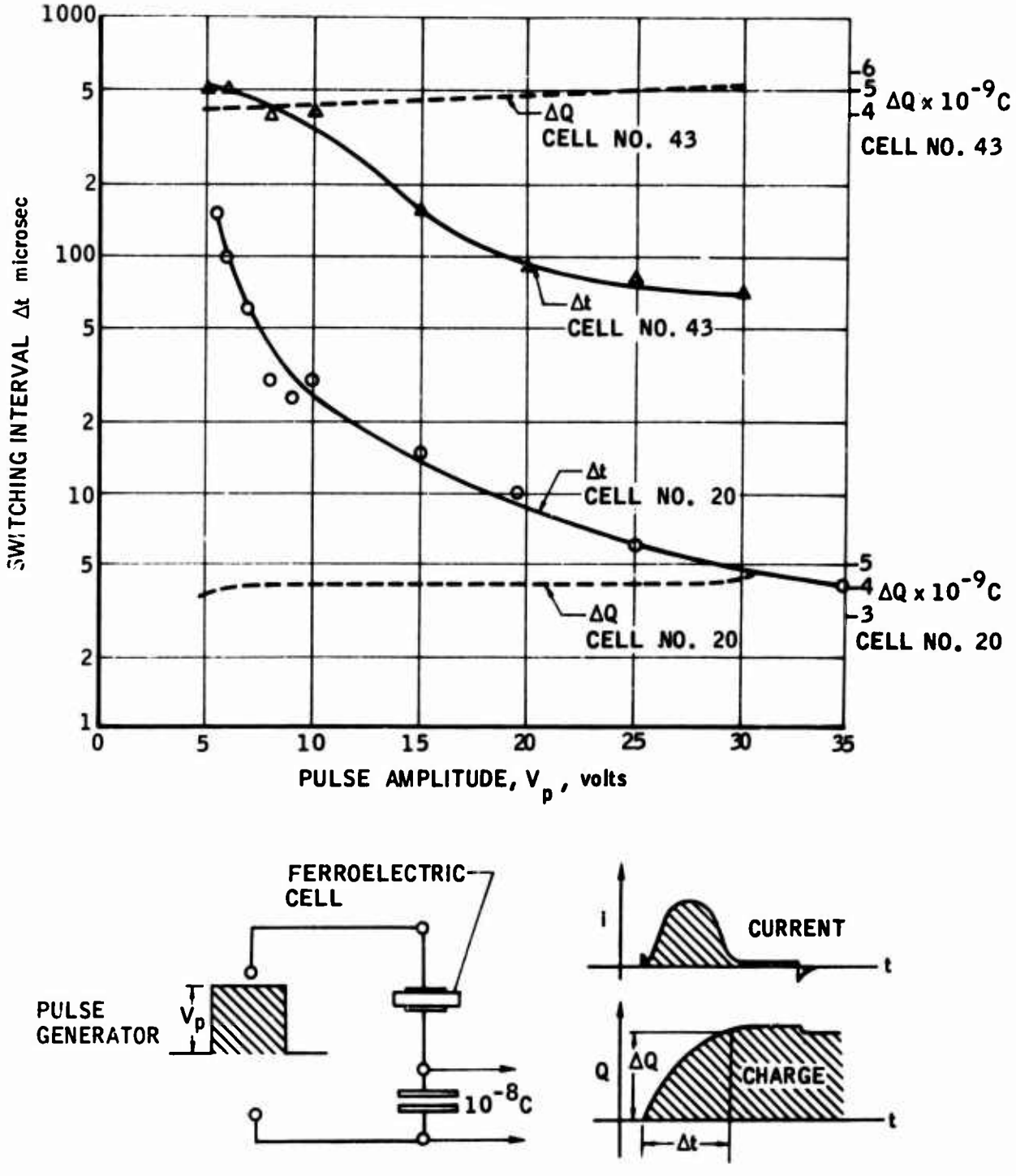


Figure 46. Switching Interval As a Function of Voltage for Two Ferroelectric Cells

48 elements at 5.1 microcoulombs ± 10% Word 1

32 elements at 4.2 microcoulombs ± 10% Word 2

Some latitude in tolerance is with a digital system. Further as shown by element #43 of Figure 46 ΔQ (switched) is a function of voltage. An element of lower than average polarization can assume a higher voltage to provide some of the necessary charge.

A thin film ferroelectric element will switch with a fraction of a volt since the switching voltage is thickness dependent.

V. CONCLUSIONS

The use of electro-optical elements in advanced associative memories provides a high degree of inherent logic capability. This conclusion is confirmed by:

(1) The development of a detailed logic for performing parallel arithmetic processing in addition to conventional parallel associative searches. This logic is verified by examination of the various logical function truth tables.

(2) Limited operational searches with a breadboard employing this logic.

From the material effort directed toward the development of thin film fabrication processes it has been concluded that thin film implementation of an associative electro-optical processor is feasible. This conclusion is based upon the following accomplishments:

(1) The development of a highly sensitive cadmium sulphide photoconductor with a high dark to light current ratio that may be utilized in the surface or volume mode of operation.

(2) A sputtering process for the deposition of barium titanate that can produce films with approximately correct stoichiometric ratios.

(3) A vapor deposition process utilizing epitaxial growth that has produced films with satisfactory characteristics verified by observation of "a" and "c" domains and a hysteresis loop.

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13. ABSTRACT

A research and development program was conducted to investigate the technique of utilizing ferroelectric and photoconductor elements in an advanced associative memory. An analytical and experimental study was performed to examine the inherent logic capability of these electro-optical elements with respect to flexibility of parallel associative search and parallel arithmetic processing. A material effort was directed toward the development of thin film processes for the fabrication of the electro-optical elements. A breadboard model was constructed to provide demonstration of these search and processing techniques. A logic was developed for performing arithmetic processing.

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