EIGHTH QUARTERLY REPORT

COMPATIBLE TECHNIQUES

FOR

INTEGRATED CIRCUITRY

U.S. AIR FORCE
CONTRACT NO. AF33(616)8276

Period Covered
1 February Through 30 April 1963

prepared for

U.S. AIR FORCE

AERONAUTICAL SYSTEMS DIVISION

WRIGHT-PATTERSON AIR FORCE BASE, OHIO

FROM DIODES TO INTEGRATED CIRCUITS . . .
ADVANCED TECHNOLOGY THROUGH MOTOROLA RESEARCH

MOTOROLA INC. *Semiconductor Products Division*

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MOTOROLA, INC.
SEMICONDUCTOR PRODUCTS DIVISION
PHOENIX, ARIZONA

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1.0 COMPATIBLE THIN FILM TECHNIQUES

1.1 Resistors

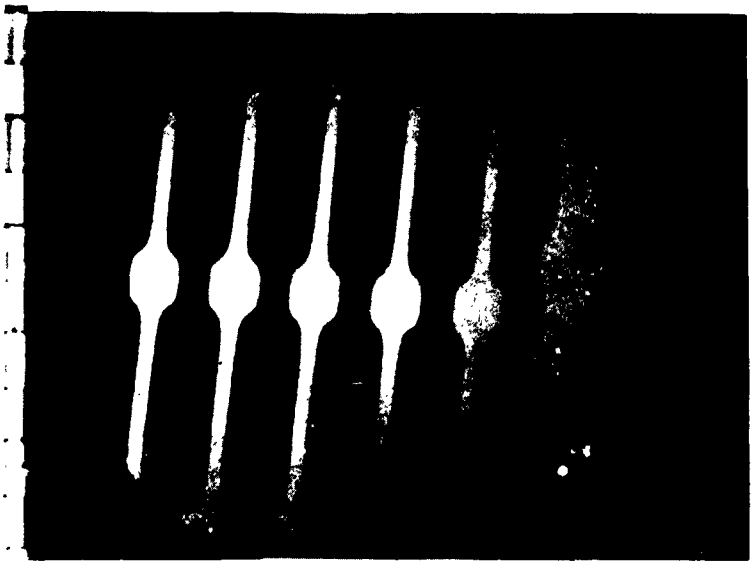
1.1.1 Nichrome

Two methods, compatible with integrated circuits, were investigated for defining the configuration of the nichrome. One is the reverse masking process and the other an etching technique.

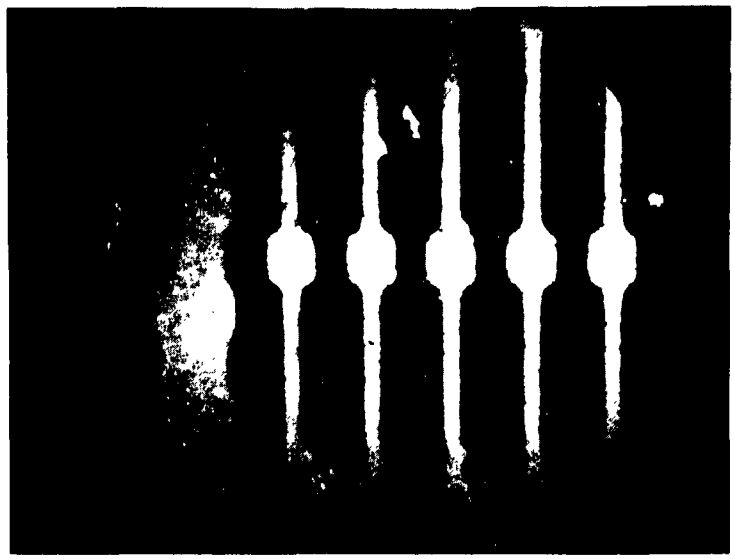
For the reverse masking technique, we have used photoresist materials, both KMER and KPR. Of the two, only KPR works satisfactorily, because it can be removed by a high temperature bake leaving the nichrome unsupported with its subsequent easier removal. KMER could only be removed with difficulty by a scrubbing operation and this resulted in poor definition.

The following photographs (Figure 1 and 2) illustrate the definition obtainable with the etching method and the reverse masking.

It is evident from the photographs that films of lower than 150 or 200 ohms per square can be etched nicely and give better definition than the reverse masking, using photoresist materials with films higher than 200 Ω/□; both of the methods work equally well. To get good adhesion of the nichrome with the photoresist reverse mask, it is necessary to slightly etch the substrate in order to remove the last vestage of the resist. We are experimenting with evaporated metal, such as aluminum and silver



Etched



Reverse Masking

Figure 1
Nichrome 100 Ω/□

Etched

Reverse Masking

Figure 2
Nichrome 250 Ω/□

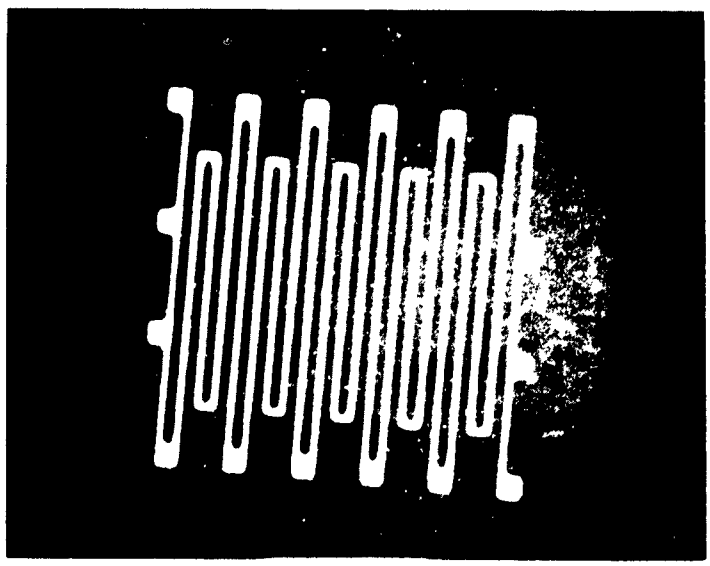


Figure 3

Etched Nichrome 38 Ω/□

to determine if these materials will give better results by the reverse masking method.

The minimum line width shown on the photographs is ½ thousandth of an inch. This indicates that the etching method is sufficiently controllable, so that resistors of large values using nichrome are practical.

Figure 3 is a photograph of an etched nichrome resistor, 38 Ω/□ deposited film. This pattern consists of ½ mil line widths with a total length of 750 squares. This photograph again illustrates that nichrome can be configurated using standard photoresist techniques into patterns of sufficient quality to make its uses on integrated circuits completely realistic.

1.1.2 Tin Oxide

The life tests with tin oxide resistors "passivated" with aluminum silicate glass continue to show good results with regard to stability and integrity of the metallized contacts.

We are attempting to improve the etching quality of the oxide "passivation". This has, in some cases, resulted in poor ohmic contacts or ragged metallization openings through the glass overlayer.

1.2 Capacitors

During this period, the major effort has been expended in making a good compatible thin film capacitor using aluminum silicate as the dielectric.

Figure 4 is a photograph of a completed multi-capacitor unit. The size of the array is 40 x 40 mils.

The primary concern in fabricating this capacitor is compatibility. That is, all materials must be those that will adhere to and be etchable on a SiO_2 substrate. They must also be able to be configured by standard photoresist procedures and no metal evaporation masks allowed.

1.2.1 Preliminary Electrical Evaluations

The following performance data is for thin film capacitors after die and wire bonding.

1. At 20 Mc

WAFER	DIE	Cp	Rp	Xp	Q	CAPACITANCE PER AREA
52A (1)	1	44.7 pf	870	180	5	.35 pf/mil^2
	2	36.9 pf	4700	210	22	.29 pf/mil^2
	3	44.9 pf	2800	180	16	.35 pf/mil^2
52D (3)	1	59.3 pf	1950	130	15	.46 pf/mil^2
	2	62.2 pf	2200	130	17	.48 pf/mil^2
	3	55.8 pf	2000	140	14	.43 pf/mil^2

Measurements were made at 20 Mc. Capacitors were self resonant with wire bond leads at 120 Mc. Units were die and wire bonded only with no encapsulation. Measurements made on C2 of 294 mask (area = 130 mil^2).

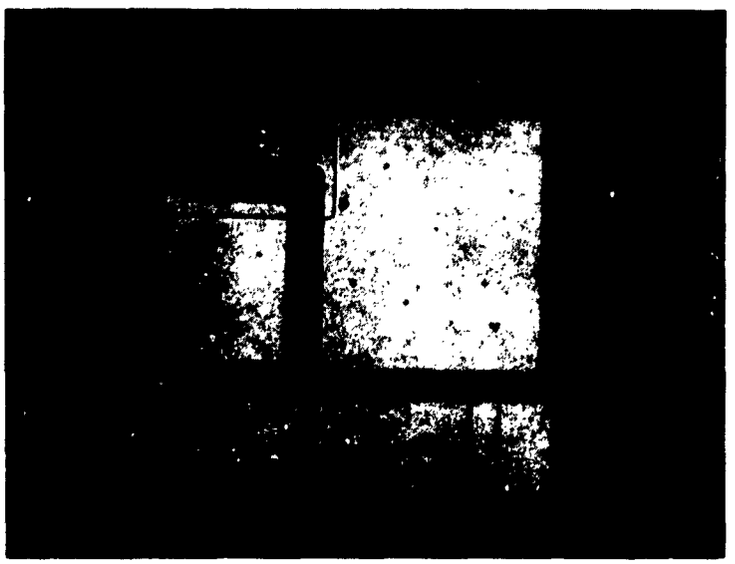


Figure 4

Completed Multi-Capacitor Unit

2. Breakdown (Measured before die bonding on 5)
(2 patterns)

Wafer	BV	Dielectric Color
52A (1)	40 V	Grey
52A (2)	44 V	Grey
52D (3)	32 V	Purple
52D (4)	23.4 V	Brown

No aging or storage tests have, as yet, been performed.

2.0 SILICON INTEGRATED CIRCUIT TECHNOLOGY

2.1 A Method for Controlling the Base-Width of Diffused Structures

2.1.1 Introduction

At present, when base-width control of the order of $\pm 0.1\mu$ is desired, a pilot chip of the circuit is emitter diffused for a period of time based on previous experience. The oxide is then stripped from the chip and the base-width is determined by either beveling and staining the junction regions or the device is probed for its electrical characteristics. If these measurements are within the limits, the entire wafer or wafers is emitter diffused for the same time. If the measurements indicate the base-width is not within the limits, another chip is emitter diffused for a new time interval based on the first chip and the "guesser's" experience. This process is repeated until the operator is "homed in".

This is the first of two reports which describe a method which should reduce the time and skill required to measure base-width and graphically eliminate much of the guesswork of correctly determining diffusion times. The second part of this report will be covered in the ninth quarterly report.

The method can be briefly summed up in the following steps:

1) A special control pattern is emitter diffused for a time interval dictated by its base junction depth, sheet resistance, and its collector concentration.

2) The base sheet resistance under the emitter is measured in the special control pattern.

3) This sheet resistance is converted to base-width with the aid of the enclosed graphs.

4) If a time adjustment is necessary, another set of empirically derived graphs is consulted which give emitter-base junction behavior versus time.

Steps one and four are the subject of the second report. The remaining steps are discussed in this report.

2.1.2 Determining Base-Width W_B

a) The control pattern

The special control pattern should possess the following qualities:

1) Be located on the edge of the wafer where it is accessible, if it is to be scribed off wafers containing the device.

2) Contain approximately one square since typical resistance values are in the range of 4-30K/□.

3) Have large contact areas for easy probing with two voltage and two current probes.

4) The emitter pattern must overlap the base pattern to prevent conduction around the sides of the emitter.

5) Be of sufficient dimensions to minimize the rounded base diffusion front effect.

Figure 1 gives an example of a special control pattern.

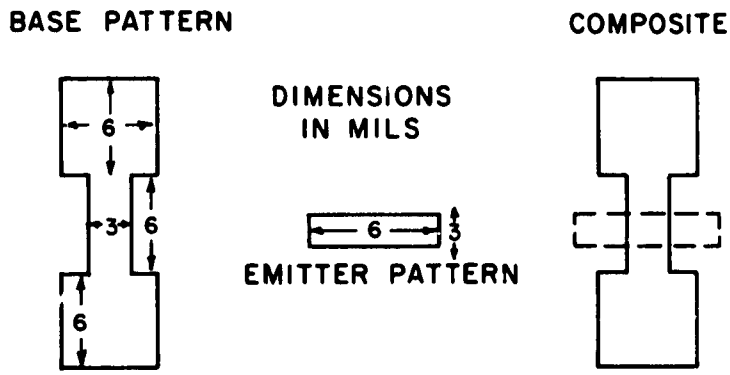


Figure 1

EXAMPLE OF SPECIAL CONTROL PATTERN
FOR DETERMINING BASE WIDTH W_B

b) Determining base width

In the absence of empirical information, two mathematical models are presented followed by a graph derived from graphs showing the conductivity of sub-surface layers in silicon. Erfc: In the first analysis, both the emitter and base diffusion profiles are assumed to be erfc. Figures 2 and 4 show these profiles for base widths of .575μ and 1.13μ respectively. In these graphs as well as the following analysis:

C_{S_B} = surface concentration of the base = 5×10^{18} (erfc) "P" type 3.5×10^{18} (gaussian)

C_{S_E} = surface concentration of the emitter = 1×10^{21} (both) "N" type

N_B' = concentration of the base at emitter-base junction (variable)

N_{BC} = background concentration = 1.2×10^{16} at/cc (0.5Ωcm) "N"

W_B = base-width (variable)

μ_n = minority carrier mobility in the base (variable)

μ_p = majority carrier mobility in the base (variable)

$b = \frac{\mu_n}{\mu_p}$

ρ_s = base sheet resistance = 200Ω/□

R_{BB}' = sheet resistance in the base under the emitter (variable)

$N_B(x)$ = concentration as a function of penetration in the base

$N_E(x)$ = concentration as a function of penetration in the emitter

$N_{(net)}$ = total net impurities in the base region per unit area

$$N_{net} = \int_{X_{jE}}^{X_{jB}} [N(x) - NE(x) - N_{BC}]dx$$

X_{jb} = base-collector junction depth

X_{jE} = emitter-base junction depth

$\alpha = \frac{1}{\sqrt{4Dt}}$ = horizontal rationalization factor

$\beta = C_s$ = vertical normalization factor

$N_{b\ net}(x)$ = net impurity concentration in the base region

$\bar{\mu}pb$ = average mobility of majority carriers in the base

$\mu pb\ (X_{jE})$ = majority carrier mobility at the emitter-base junction

$\mu pb\ (X_{jb})$ = majority carrier mobility at the base-collector junction

Figures 3 and 5 are plots of the net impurity concentration in the base region corresponding to Figures 2 and 4 respectively.

These were plotted from:

$$1)\quad N(x)_{net} = N_B(x) - N_E(x) - N_{BC}$$

R_{BB}' was calculated by dividing the net base impurities into small volumes, looking up the μ_n' and b Figures 6 and 7 corresponding to the average $N_b(x)_{total}$ and using the relation.

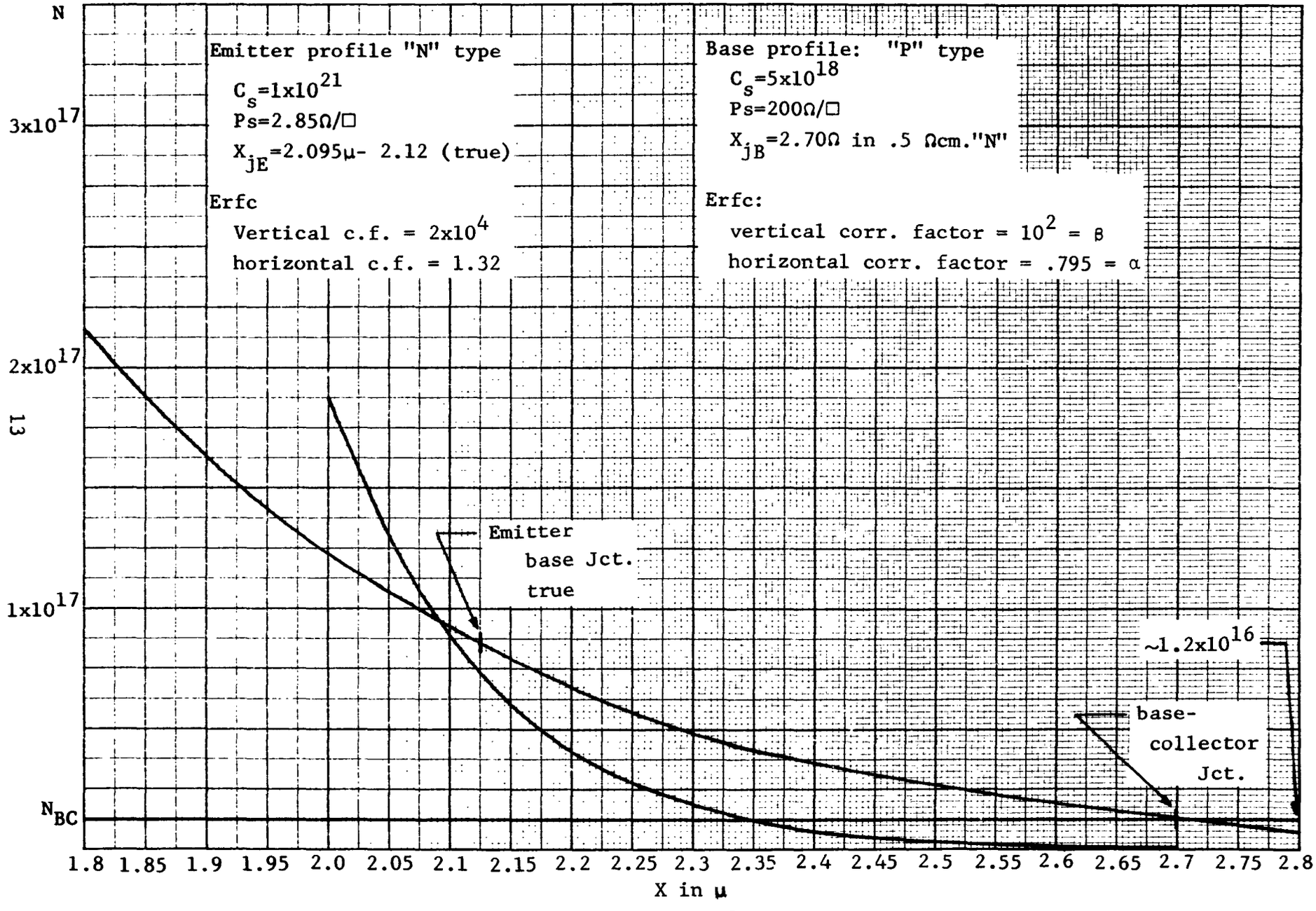

N
3x10^17
2x10^17
1x10^17
N_BC
Emitter profile "N" type
C_s=1x10^21
Ps=2.85Ω/□
X_jE=2.095μ- 2.12 (true)
Erfc
Vertical c.f. = 2x10^4
horizontal c.f. = 1.32
Base profile: "P" type
C_s=5x10^18
Ps=200Ω/□
X_jB=2.70Ω in .5 Ωcm."N"
Erfc:
vertical corr. factor = 10^2 = β
horizontal corr. factor = .795 = α
Emitter base Jct. true
~1.2x10^16
base-collector Jct.
1.8 1.85 1.9 1.95 2.0 2.05 2.1 2.15 2.2 2.25 2.3 2.35 2.4 2.45 2.5 2.55 2.6 2.65 2.7 2.75 2.8
X in μ

Figure 2

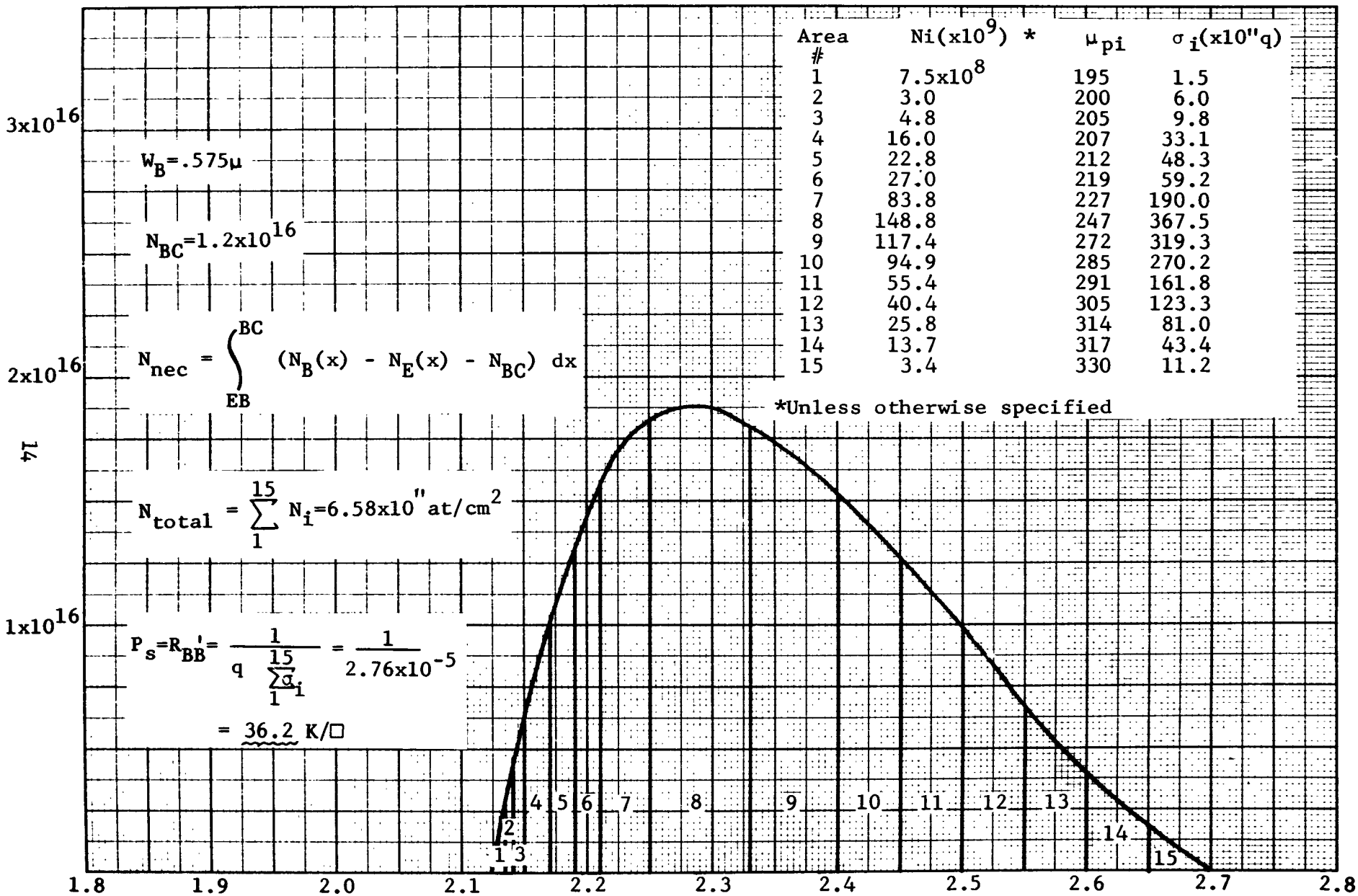
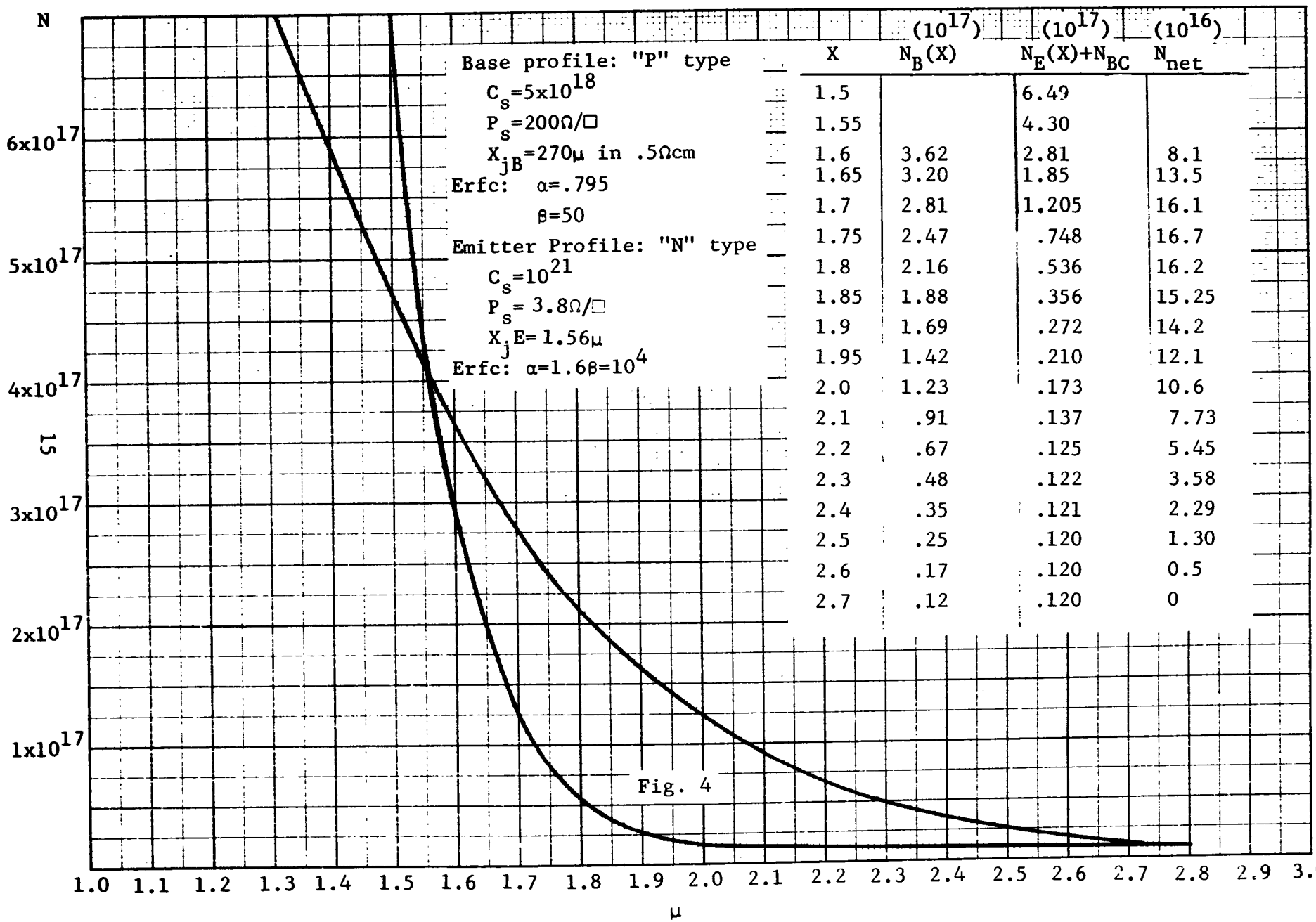

Area # | Ni(x10^9) * | μpi | σi(x10"q)
1 | 7.5x10^8 | 195 | 1.5
2 | 3.0 | 200 | 6.0
3 | 4.8 | 205 | 9.8
4 | 16.0 | 207 | 33.1
5 | 22.8 | 212 | 48.3
6 | 27.0 | 219 | 59.2
7 | 83.8 | 227 | 190.0
8 | 148.8 | 247 | 367.5
9 | 117.4 | 272 | 319.3
10 | 94.9 | 285 | 270.2
11 | 55.4 | 291 | 161.8
12 | 40.4 | 305 | 123.3
13 | 25.8 | 314 | 81.0
14 | 13.7 | 317 | 43.4
15 | 3.4 | 330 | 11.2
*Unless otherwise specified
W_B=.575μ
N_BC=1.2x10^16
N_nec = ∫ from EB to BC (N_B(x) - N_E(x) - N_BC) dx
N_total = Σ from 1 to 15 N_i=6.58x10" at/cm^2
P_s=R_BB'= 1 / (q Σ from 1 to 15 σ_i) = 1 / 2.76x10^-5
= 36.2 K/□
3x10^16
2x10^16
1x10^16
14
1.8
1.9
2.0
2.1
2.2
2.3
2.4
2.5
2.6
2.7
2.8
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Fig. 3



X	$N_B(X)$ (10^{17})	$N_E(X)+N_{BC}$ (10^{17})	N_{net} (10^{16})
1.5		6.49	
1.55		4.30	
1.6	3.62	2.81	8.1
1.65	3.20	1.85	13.5
1.7	2.81	1.205	16.1
1.75	2.47	.748	16.7
1.8	2.16	.536	16.2
1.85	1.88	.356	15.25
1.9	1.69	.272	14.2
1.95	1.42	.210	12.1
2.0	1.23	.173	10.6
2.1	.91	.137	7.73
2.2	.67	.125	5.45
2.3	.48	.122	3.58
2.4	.35	.121	2.29
2.5	.25	.120	1.30
2.6	.17	.120	0.5
2.7	.12	.120	0

Fig. 4

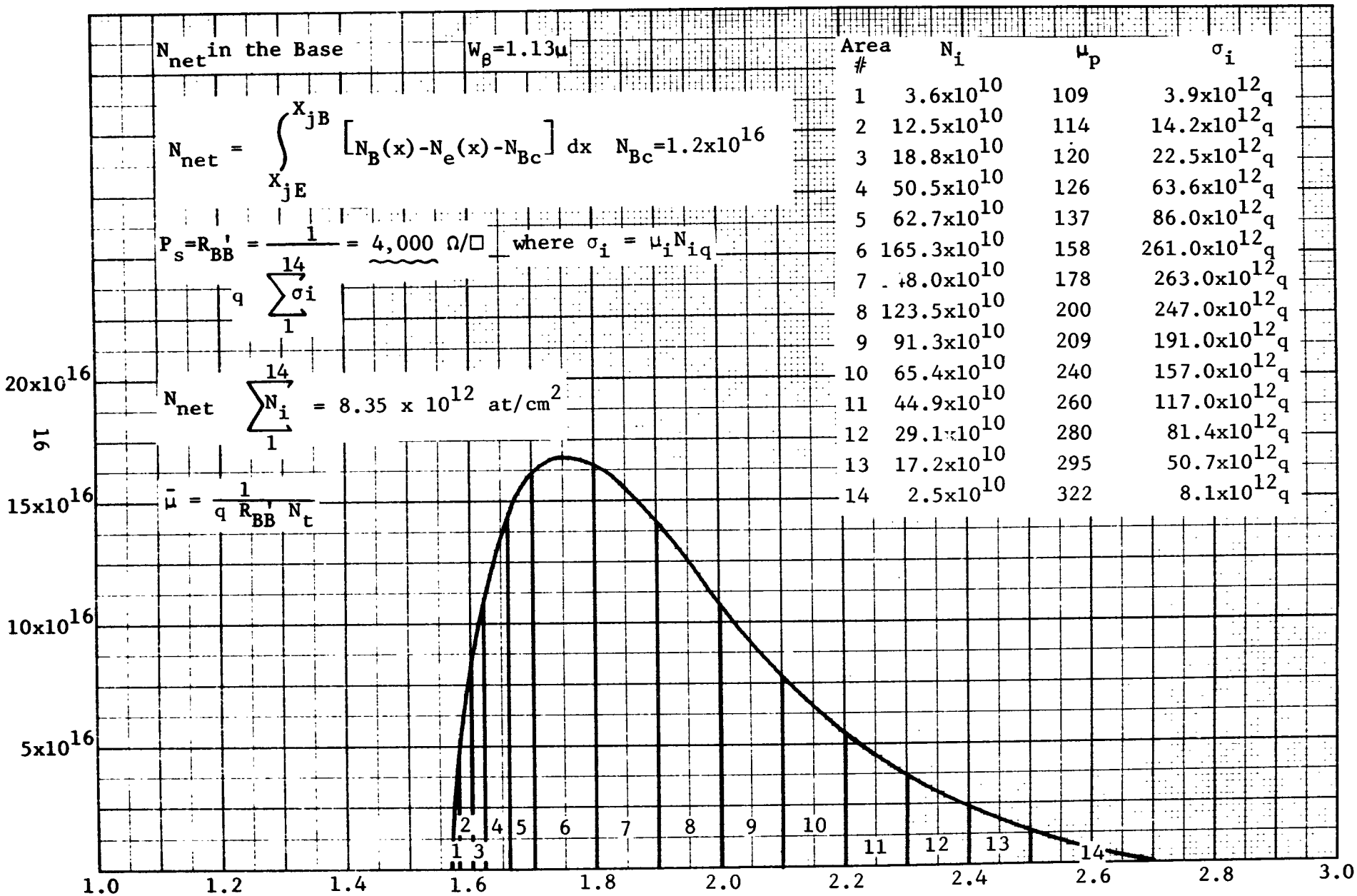

N_{net} in the Base
W_β=1.13μ
$N_{net} = \int_{X_{jE}}^{X_{jB}} [N_B(x) - N_e(x) - N_{Bc}]\, dx$
N_{Bc}=1.2x10^16
$P_s = R_{BB}' = \frac{1}{q \sum_1^{14} \sigma i} = 4{,}000\ \Omega/\square$ where $\sigma_i = \mu_i N_{iq}$
$N_{net} \sum_1^{14} N_i = 8.35 \times 10^{12}$ at/cm^2
$\bar{\mu} = \frac{1}{q\, R_{BB}'\, N_t}$
Area # | N_i | μ_p | σ_i
1 | 3.6x10^10 | 109 | 3.9x10^12 q
2 | 12.5x10^10 | 114 | 14.2x10^12 q
3 | 18.8x10^10 | 120 | 22.5x10^12 q
4 | 50.5x10^10 | 126 | 63.6x10^12 q
5 | 62.7x10^10 | 137 | 86.0x10^12 q
6 | 165.3x10^10 | 158 | 261.0x10^12 q
7 | 78.0x10^10 | 178 | 263.0x10^12 q
8 | 123.5x10^10 | 200 | 247.0x10^12 q
9 | 91.3x10^10 | 209 | 191.0x10^12 q
10 | 65.4x10^10 | 240 | 157.0x10^12 q
11 | 44.9x10^10 | 260 | 117.0x10^12 q
12 | 29.1x10^10 | 280 | 81.4x10^12 q
13 | 17.2x10^10 | 295 | 50.7x10^12 q
14 | 2.5x10^10 | 322 | 8.1x10^12 q
16
20x10^16
15x10^16
10x10^16
5x10^16
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Fig. 5

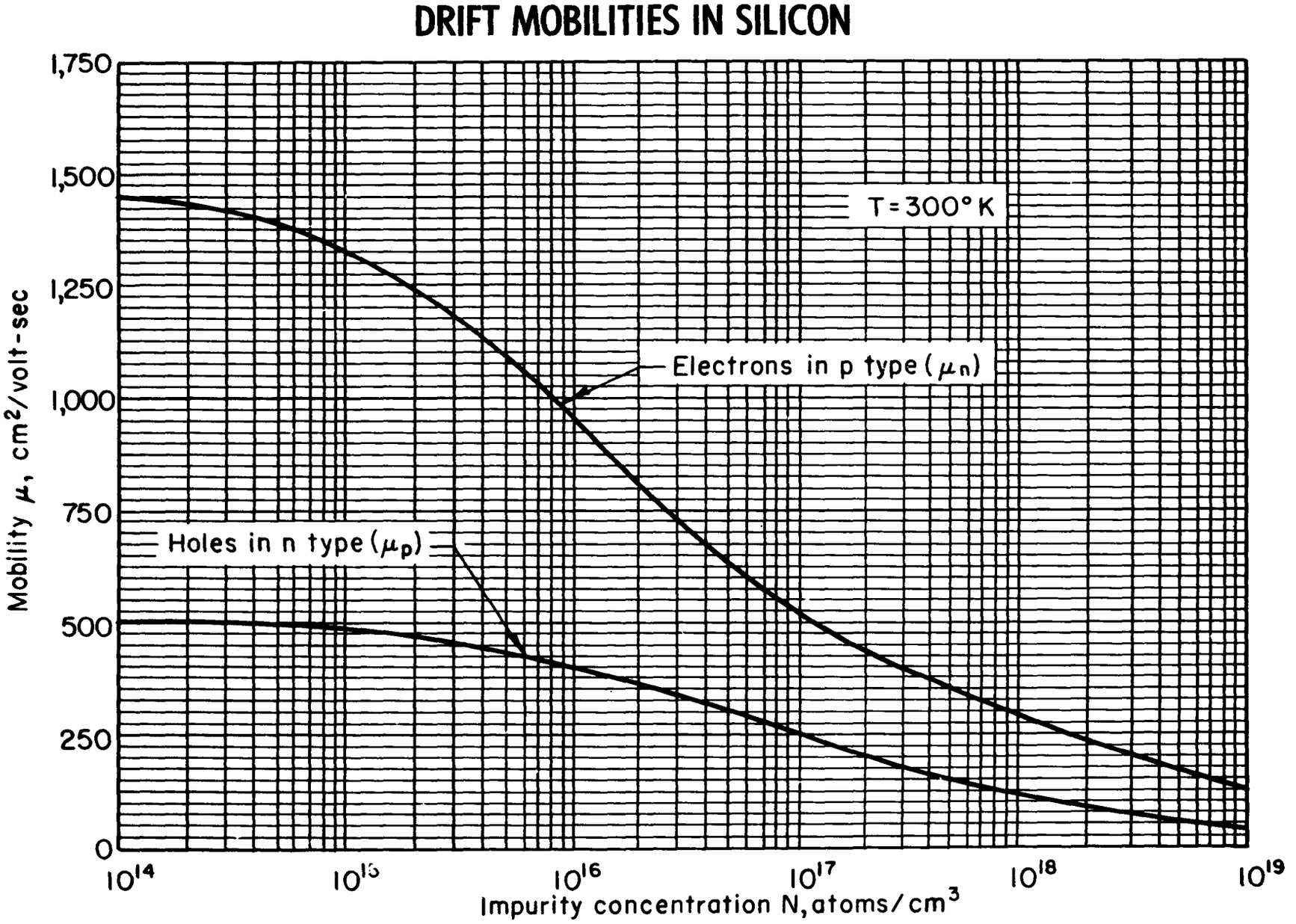

DRIFT MOBILITIES IN SILICON
1,750
1,500
1,250
1,000
750
500
250
0
Mobility μ, cm²/volt-sec
T = 300° K
Electrons in p type (μn)
Holes in n type (μp)
10¹⁴
10¹⁵
10¹⁶
10¹⁷
10¹⁸
10¹⁹
Impurity concentration N, atoms/cm³

FIGURE 6

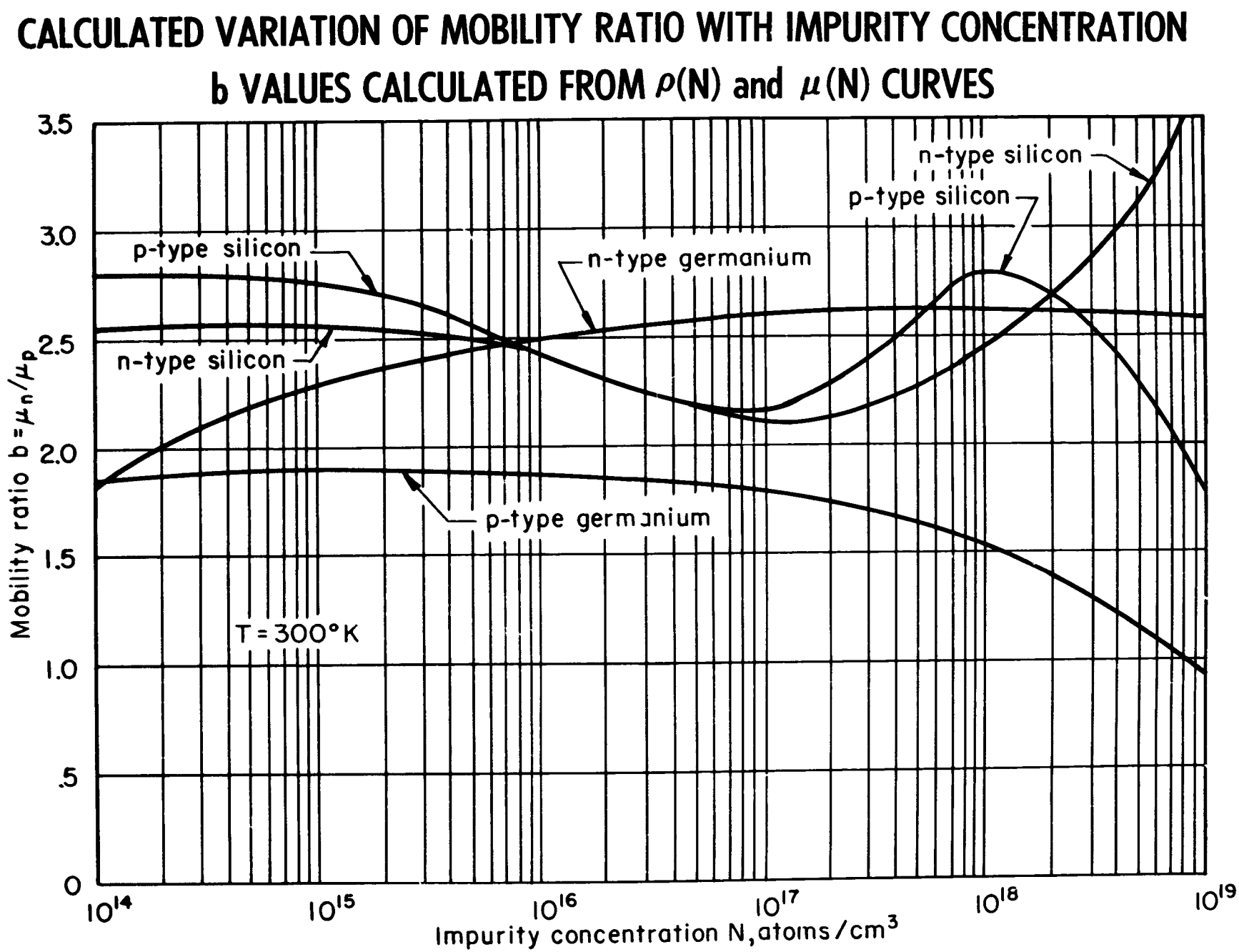

CALCULATED VARIATION OF MOBILITY RATIO WITH IMPURITY CONCENTRATION
b VALUES CALCULATED FROM ρ(N) and μ(N) CURVES
Mobility ratio b = μn/μp
3.5
3.0
2.5
2.0
1.5
1.0
.5
0
p-type silicon
n-type silicon
n-type germanium
p-type silicon
n-type silicon
p-type germanium
T = 300°K
10^14
10^15
10^16
10^17
10^18
10^19
Impurity concentration N, atoms/cm^3

FIGURE 7

$$2)\quad R_{BB}' = \frac{1}{q\sum_{1}^{n} \frac{\mu_{n_i}}{b} N_i}$$

This graphical technique is very laborious and can be closely approximated for the erfc distributions if we assume an exponential mobility dependence[2] and integrate between the junctions.

$$3)\quad \bar{\mu}_{pb} = \frac{\mu_{pb}(X_{jB}) - \mu_{pb}(X_{jE})}{\ln\left[\frac{\mu_{pb}(X_{jb})}{\mu_{pb}(X_{jE})}\right]}$$

Equation (2) can now be written in the form:

$$4)\quad R_{BB}' = \frac{1}{q\,\bar{\mu}_{pb}\int_{X_{jE}}^{X_{jB}} [N_B(x) - N_E(x) - N_{BC}]dx}$$

where for the assumed erfc case,

$$5)\quad N_B(x) = C_{S_B}\ \text{erfc}\ \left(\frac{X}{\sqrt{4Dt}}\right) = C_{S_B}\ \text{erfc}\ (\alpha_B X)$$

and

$$6)\quad N_E(x) = C_{S_E}\ \text{erfc}\ \left(\frac{X}{\sqrt{4Dt}}\right) = C_{S_E}\ \text{erfc}\ (\alpha_E X)$$

Substituting (5) and (6) into (4)

$$7)\quad R_{BB}' = -\frac{1}{q\,\bar{\mu}_{pb}\left[C_{S_B}\int_{X_{jE}}^{X_{jB}} \operatorname{erfc}(\alpha_B X)\,dx - C_{S_E}\int_{X_{jE}}^{X_{jB}} \operatorname{erfc}(\alpha_E X)\,dx - N_{BC}W_B\right]}$$

While these integrals cannot be expressed explicitly, tables[3] are available which give the integral values in terms of the argument αx. Figure 8 includes figures adequate for rough calculations.

Using this method and the tables,[2,3,4] Figure 9 was plotted. Gaussian - Again equation (4) is used, but this time both emitter and base distributions are assumed to be gaussian, i.e.,

$$8)\quad N_B(x) = C_{S_B}\,\epsilon^{-\frac{X^2}{4Dt}} = C_{S_B}\,\epsilon^{-\alpha_B^2 X^2}$$

$$9)\quad N_E(x) = C_{S_E}\,\epsilon^{-\alpha_E^2 X^2}$$

The α's can be found from the boundary conditions

$$N_{BC}(X_{jB}) = C_{S_B}\,\epsilon^{-X_{jb}^2\,\alpha^2}$$

$$\ln\frac{C_{SB}}{N_{BC}(X_{jB})} = \alpha^2\,X_{jB}^2$$

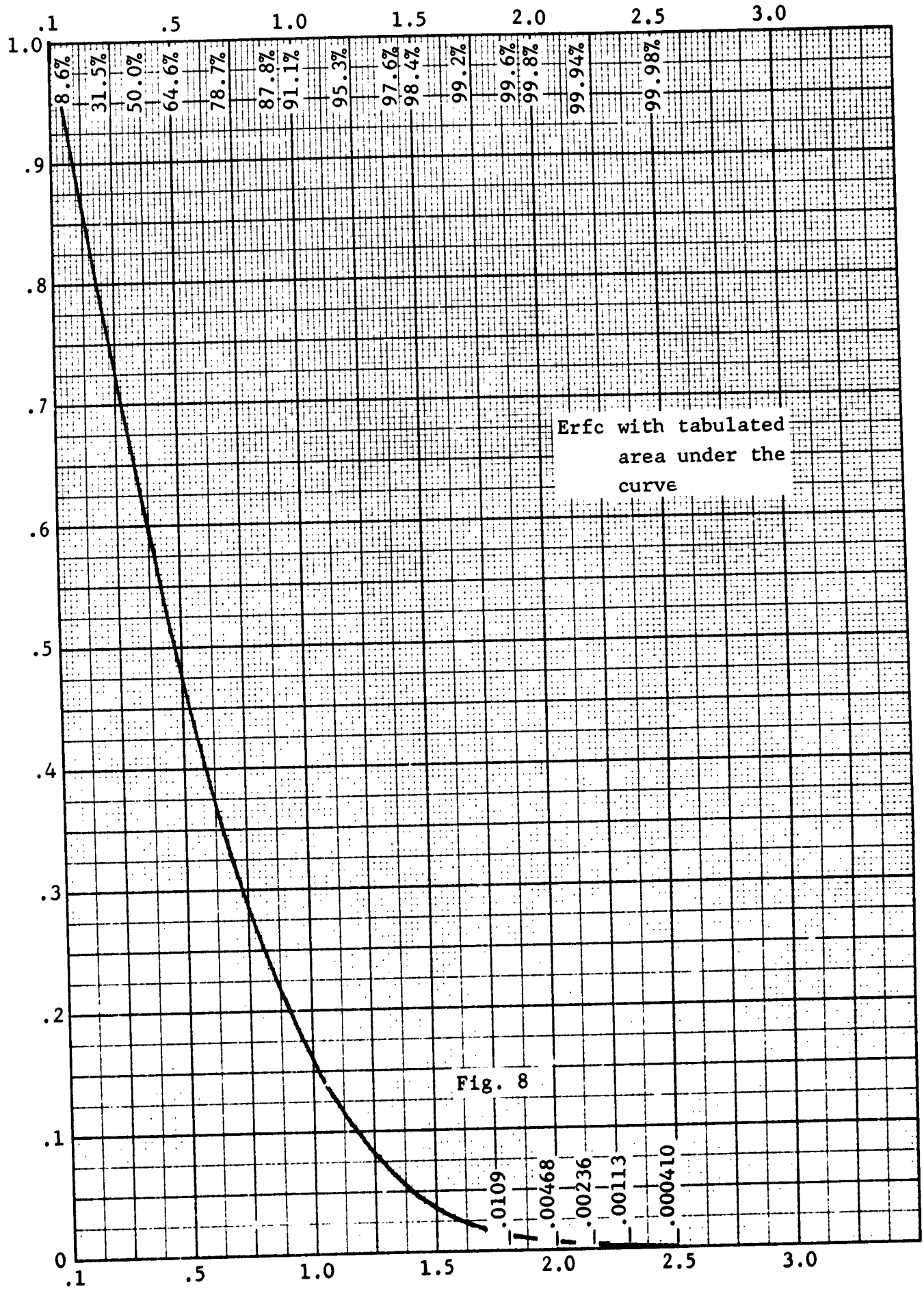
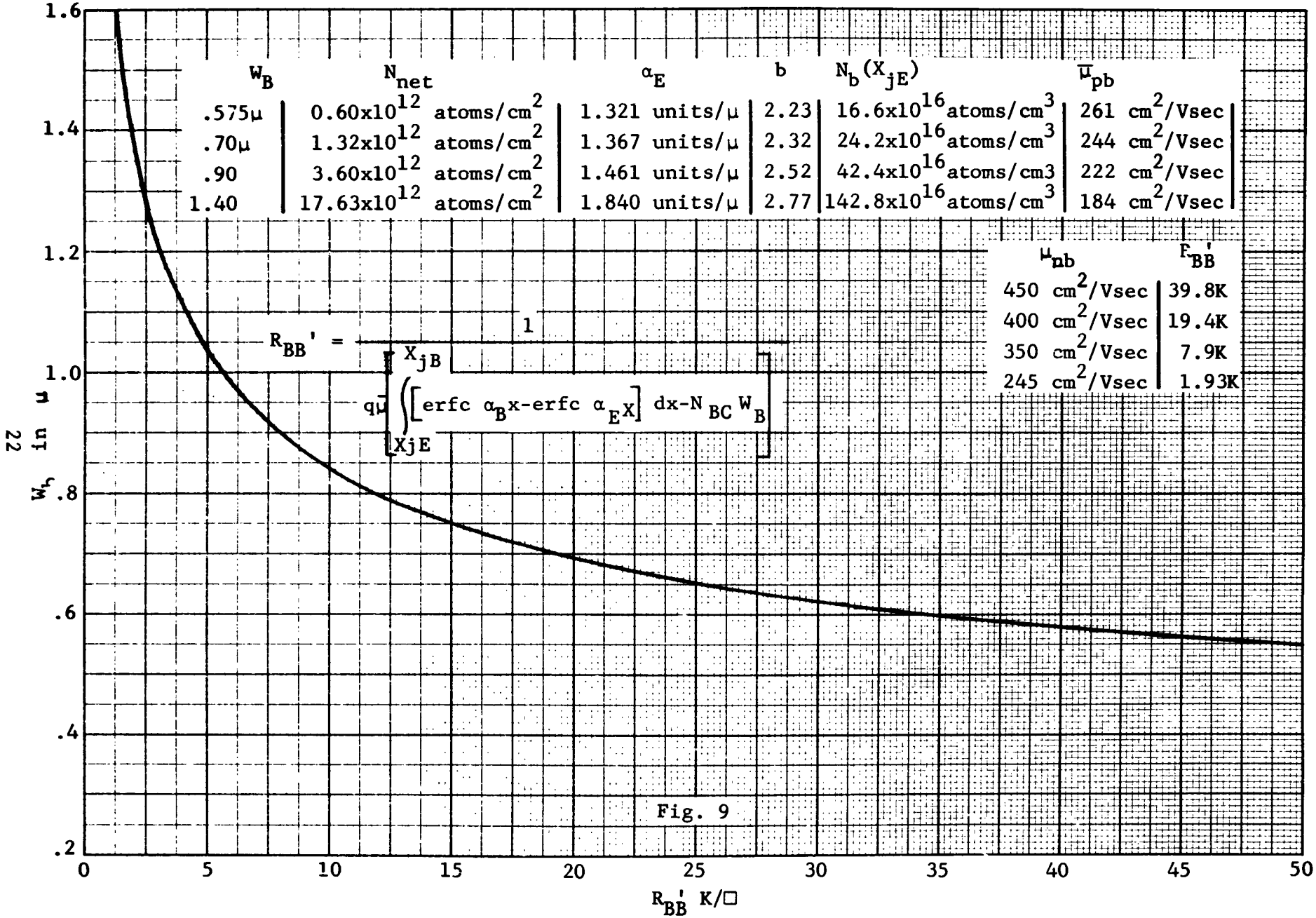

.1
.5
1.0
1.5
2.0
2.5
3.0
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
8.6%
31.5%
50.0%
64.6%
78.7%
87.8%
91.1%
95.3%
97.6%
98.4%
99.2%
99.6%
99.8%
99.94%
99.98%
Erfc with tabulated area under the curve
.0109
.00468
.00236
.00113
.000410

Fig. 8

Base Width W_B Vs Base Sheet Resistance R_{BB}'
for Erfc Emitter and Base Distribution



W_B	N_{net}	α_E	b	$N_b(X_{jE})$	$\bar{\mu}_{pb}$
.575μ	0.60×10^{12} atoms/cm^2	1.321 units/μ	2.23	16.6×10^{16} atoms/cm^3	261 cm^2/Vsec
.70μ	1.32×10^{12} atoms/cm^2	1.367 units/μ	2.32	24.2×10^{16} atoms/cm^3	244 cm^2/Vsec
.90	3.60×10^{12} atoms/cm^2	1.461 units/μ	2.52	42.4×10^{16} atoms/cm3	222 cm^2/Vsec
1.40	17.63×10^{12} atoms/cm^2	1.840 units/μ	2.77	142.8×10^{16} atoms/cm^3	184 cm^2/Vsec

μ_{nb}	F_{BB}'
450 cm^2/Vsec	39.8K
400 cm^2/Vsec	19.4K
350 cm^2/Vsec	7.9K
245 cm^2/Vsec	1.93K

$$R_{BB}' = \frac{1}{q\bar{\mu}\left[\int_{XjE}^{X_{jB}} \left[\operatorname{erfc} \alpha_B x - \operatorname{erfc} \alpha_E X\right] dx - N_{BC} W_B\right]}$$

Fig. 9

$$10)\quad \alpha_B = \sqrt{\frac{\ln \frac{C_{S_B}}{N_{BC}}}{X_{jB}}}$$

and at the emitter junction,

$$N_B(X_{jE}) = N_{BC}\, \epsilon^{+\alpha^2(X_{jB}^2 - X^2_{jE})} = N_E(X_{jE}) + N_{BC}$$

$$11)\quad N_E(X_{jE}) = N_{BC}\, \epsilon^{+\alpha_B^2(X_{jB}^2 - X_{jE}^2)} - N_{BC} = N_{BC}(\epsilon^{\alpha_B^2(X_{jB}^2 - X_{jE}^2)} - 1)$$

Substituting 11) →9

$$N_E(X_{jE}) = N_{BC}(\epsilon^{\alpha_B^2(X_{jB}^2 - X_{jE}^2)} - 1) = C_{SE}\, \epsilon^{-\alpha_E^2 X_{jE}^2}$$

$$12)\quad \therefore \alpha_E^2 = \frac{\ln \left[\frac{C_{SE}}{N_{BC}(\epsilon^{\alpha_B^2(X_{jB}^2 - X_{jE}^2)} - 1)} \right]}{X_{jE}^2}$$

Substituting equation (8) and (9) into (4)

13) $$R_{BB'} = \frac{1}{\text{gaussian } q\,\bar{\mu}_{pb}\int_{X_{jE}}^{X_{jB}} \left[C_{S_B}\,\epsilon^{-\alpha_B{}^2X^2} - C_{S_{E\epsilon}}\,\epsilon^{-\alpha_E{}^2X^2} - N_{B_C}\right]dx}$$

letting $\xi_B = \alpha_B X$ $\xi_E = \xi_E X$ the integral of equation 13 can be written

14) $$\frac{C_{S_E}}{\alpha_B}\int_{\alpha_B X_{jE}}^{\alpha_B X_{jB}} \epsilon^{-\xi_B{}^2}\,d\xi - \frac{C_{S_E}}{\alpha E}\int_{\alpha_E X_{jE}}^{\alpha_E X_{jB}} \epsilon^{-\xi_E{}^2}\,d\xi - N_{BC}\,W_B$$

since $dx = \frac{1}{\alpha}\,d\xi$

but these integrals are simply $\frac{\sqrt{\pi}}{2}\,\text{erf}\,(\alpha x)$

Since

$$\text{erf}\,(\alpha x) = \frac{2}{\sqrt{\pi}}\int_0^{\alpha x} \epsilon^{-\xi^2}\,d\xi$$

15) $$\int_{\alpha_B X_{jE}}^{\alpha_B X_{jB}} \epsilon^{-\xi^2}\,d\xi = \frac{\sqrt{\pi}}{2}\left[\text{erf}(\alpha_B X_{jB}) - \text{erf}(\alpha_B X_{jE})\right]$$

$$16)\quad \int_{\alpha_E X_{jE}}^{\alpha_E X_{jB}} \epsilon^{-\xi^2}\, d\xi = \frac{\sqrt{\pi}}{2}\left[\operatorname{erf}(\alpha_E X_{jB}) - \operatorname{erf}(\alpha_E X_{jE})\right]$$

Substituting (15) and (16) into (14) into (13)

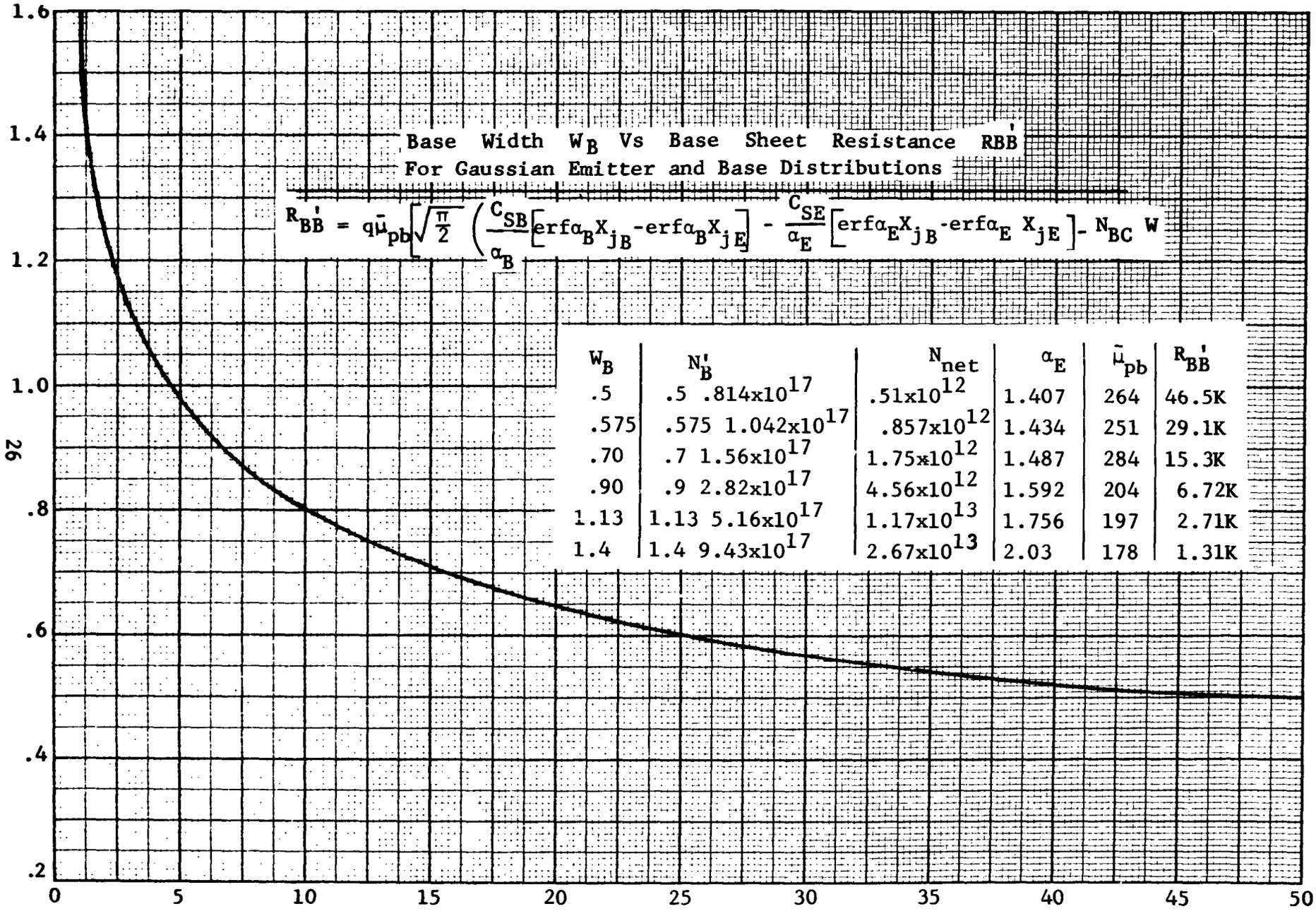
$$17)\quad R_{BB}' = \frac{1}{q\,\bar{\mu}_{pb}\left[\frac{\sqrt{\pi}}{2}\left(\frac{C_{S_B}}{\alpha_B}\left\{(\operatorname{erf}\alpha_B X_{jB}) - \operatorname{erf}\alpha_B X_{jE}\right\} - \frac{\sqrt{\pi}}{2}\left(\frac{C_{S_E}}{\alpha_E}\left\{\operatorname{erf}\alpha_E X_{jB} - \operatorname{erf}\alpha_E X_{jE}\right\}\right) - N_{BC}\, W_B\right]\right.}$$

where the α's are given in equations 10 and 12 and $\bar{\mu}_{pb}$ by equation (3).

This gives an explicit expression for R_{BB}' which is plotted in Figure 10 versus $W_B = X_{jB} - X_{jE}$.

Irwin's Curves: A third method involves recent data[1] by Irwin on the conductivity due to sub-surface layers in silicon. Unfortunately, the partial compensation in the base region caused by the emitter profile must be ignored in favor of an assumed step junction since any attempt to mathematically introduce emitter type layers in the base region confuses the mobilities there.

Figure 11 shows the results for assumed erfc and gaussian base distributions.



W_B	N_B'	N_{net}	α_E	$\bar{\mu}_{pb}$	R_{BB}'
.5	.5 $.814\times10^{17}$	$.51\times10^{12}$	1.407	264	46.5K
.575	.575 1.042×10^{17}	$.857\times10^{12}$	1.434	251	29.1K
.70	.7 1.56×10^{17}	1.75×10^{12}	1.487	284	15.3K
.90	.9 2.82×10^{17}	4.56×10^{12}	1.592	204	6.72K
1.13	1.13 5.16×10^{17}	1.17×10^{13}	1.756	197	2.71K
1.4	1.4 9.43×10^{17}	2.67×10^{13}	2.03	178	1.31K

Fig. 10

Base Width W_B Vs Base Sheet Resistance R_{BB}'

from Irwin's Curves of Sub Surface Layers

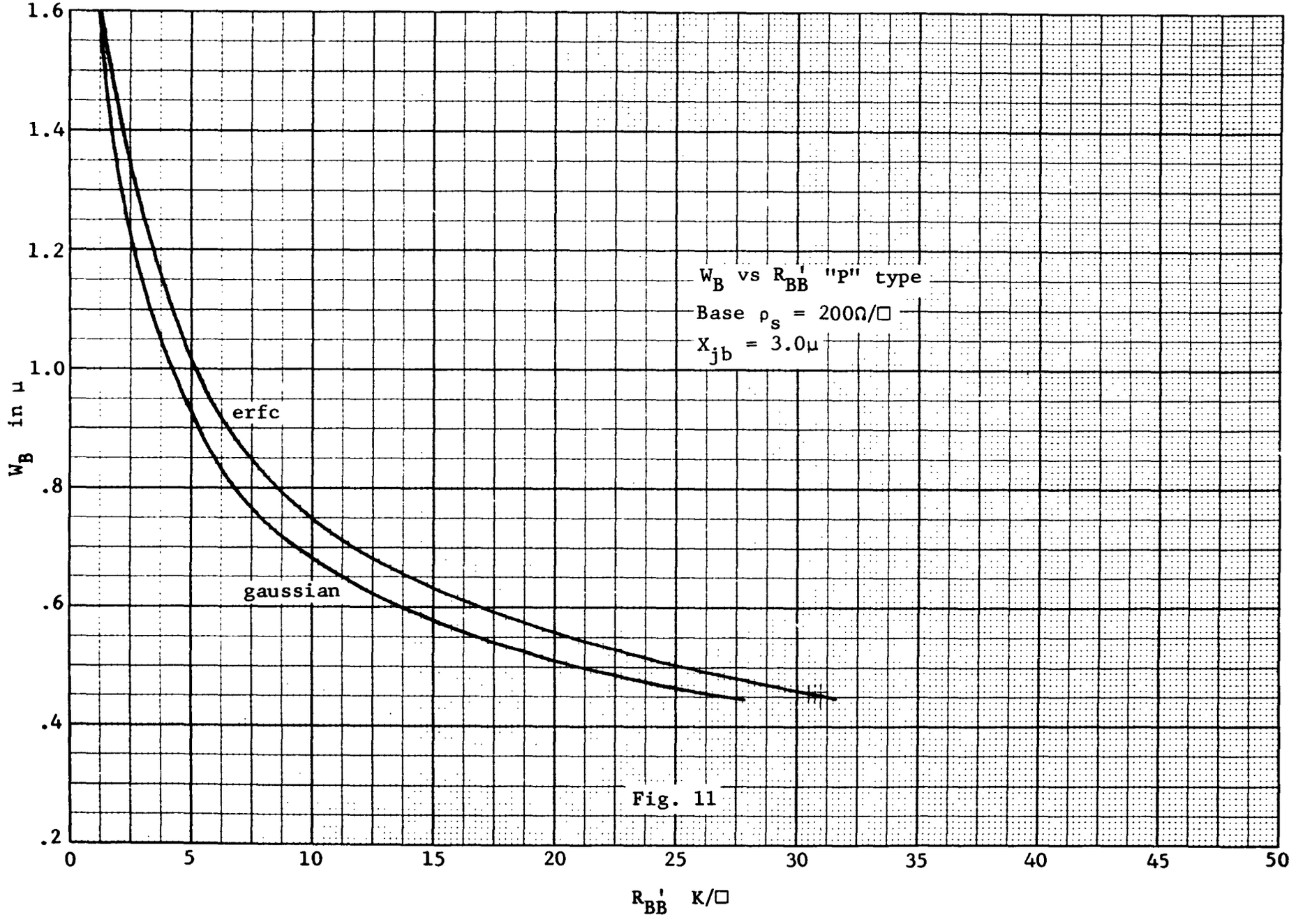


Fig. 11

Work is being done in Integrated Circuits R & D to determine an empirical curve of W_B versus R_{BB}'. Comparing this curve with the mathematical curves given here may provide an insight to the true nature of the impurity profiles in the region of the two junctions.

References:

1. John C. Irvin: "The Bell System Technical Journal" Number 2; March 1962, Page 387
2. Alvin B. Phillips: "Transistor Engineering." McGraw-Hill Book Company, Inc., New York, 1962.
3. O. S. Berlyand, R. I. Gavriloba and A. P. Prudnikov: "Tables of Integral Error Functions and Hermite Polynomials." The Macmillan Company, New York, 1962.
4. U. S. Department of Commerce, National Bureau of Standards Applied Mathematics Series 41: "Tables of the Error Function and Its Derivative." October 22, 1954.

2.2 Reduction of R_{SAT} by the Buried Layer Technique

Many problems have arisen which have limited the progress of the buried layer technique. However, most difficulties have either been side-stepped or surmounted, and one type circuit has been successfully processed with a buried layer. This circuit was the radio frequency amplifier prototype (IC295) - a linear circuit that is resistive isolated. It is hoped that a successful introduction of the buried layer to the standard monolithic integrated circuit will have been completed by the next reporting period. The technique for this circuit is more stringent due to the requirement of diode isolation.

The diffused buried layer techniques have not been successful, due to the inability to obtain arsenic or aluminum diffusion capabilities. Due to the closeness of the diffusion constants of boron and phosphorous in silicon, the channel diffusion that gives diode isolation makes the use of other impurities, with slower or faster diffusion constants, very desirable.

The diffusion constant of arsenic is an order of magnitude slower than phosphorous, making it an ideal impurity to use in a buried layer. The research diffusion group has developed an arsenic diffusion capability of a surface concentration of 3 x 10^{19}/cc with a depth of 0.3 microns. This is inadequate since the pre-epitaxial treatment removes a minimum of one (1.0) micron. Heavier initial surface concentrations are needed to obtain significant concentrations at a drive-in depth of two to four microns.

∴ An epi layer is grown subsequent to the "buried layer" diffusion and prior to the standard device processing.

The arsenic source being used is a trichloride of arsenic, and if the source temperature is raised to increase the surface concentration, the chlorine reduction products attack the silicon so severely that the surface is rendered unusable. If an oxide is grown as a protective mask of the silicon the arsenic diffusion is prohibited and a lower surface concentration results. Further advance of arsenic diffusion capabilities will result in an effective way of lowering R_{SAT}.

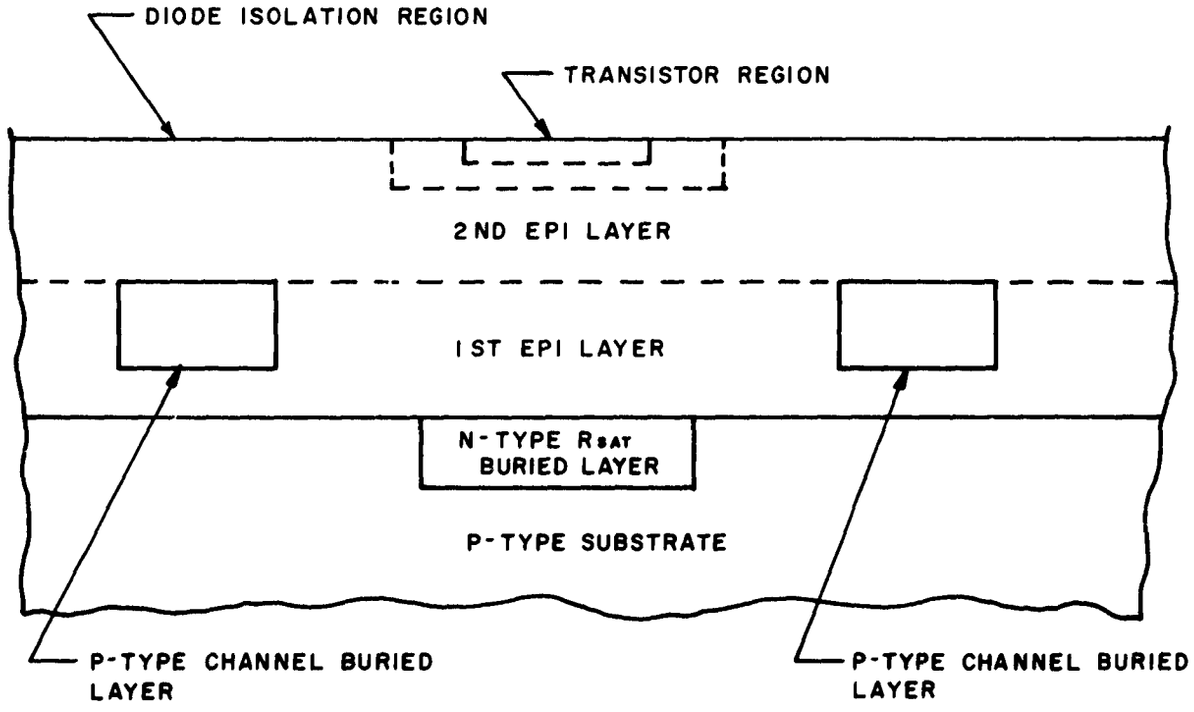
The diffusion constant of aluminum is nearly an order of magnitude faster than phosphorous making it an ideal impurity to use for isolation diffusion as a complement to a phosphorous type buried layer. An attempt to circumvent the problem by evaporating aluminum, alloying, then redistributing or growing epi, was tried and failed. Failure was precipitated by the surface migration characteristics of aluminum at elevated temperatures.

Another method of circumvention in order to use diffusion capabilities is being investigated. The procedure consists of four (4) steps. See Figure 12, namely;

a. Diffusing a phosphorous R_{SAT} buried layer into the p-type substrate.
b. Growing a partial epitaxial layer.
c. Diffusing a boron source for a channel isolation buried layer.
d. Continuing to deposit the remainder of the epitaxial layer desired.

This procedure introduces seven additional operations* to the standard process and is for that reason undesirable.

* An oxidation, a photoresist, and a diffusion, are required for each type of buried layer plus an additional epi cycle.



PHOSPHOROUS & BORON BURIED LAYER
TECHNIQUES TO REDUCE RSAT

Figure 12

Due to the difficulties encountered in trying to obtain a diffused buried layer, an investigation into the possibilities of an epitaxial buried layer were initiated. The linear circuit application was first chosen since the epi-plug would be of the same type as the substrate, and diode characteristics would not be a consideration. First attempts were made at etching out the silicon and then back filling with epitaxial growth. Although these attempts failed, they are very feasible and are still being considered. Figures 13 and 14 are pictures of reasons of failure. Figure 13 is a picture of the etched out hole refilled with epi growth. It is difficult to obtain a nice uniform and flat hole. Both chemical and gas etching of (111) type substrates were tried. Some (100) type substrate will be investigated, as well as some new chemical etches. Figure 14 is a picture that shows two things: one, the unevenness of growth in the etched out hole, and; two, the polycrystalline growth that abounds over the surface of the wafer. This must be removed before the overlaying epi growth can be made. Methods of removal of this polycrystalline are being investigated, including chemical etching and sand blasting. One of the most promising methods is that of mechanical polishing. However, in this method the pattern is obliterated, and it is necessary to provide additional alignment keys that withstand the polishing and will be evident after a subsequent treatment; namely an epi-growth, an oxidation and a coating of photoresist. The adequate delineation of alignment keys has proved to be an obstacle not yet surpassed.

However, another manner in obtaining the buried epi plug has been devised. It was this method that provided the first successful device with a buried layer. Essentially, it consists in growing epi in a preferential area, then growing an epi layer

Figure 13
Hole Etched in Silicon Refilled With Epi Growth

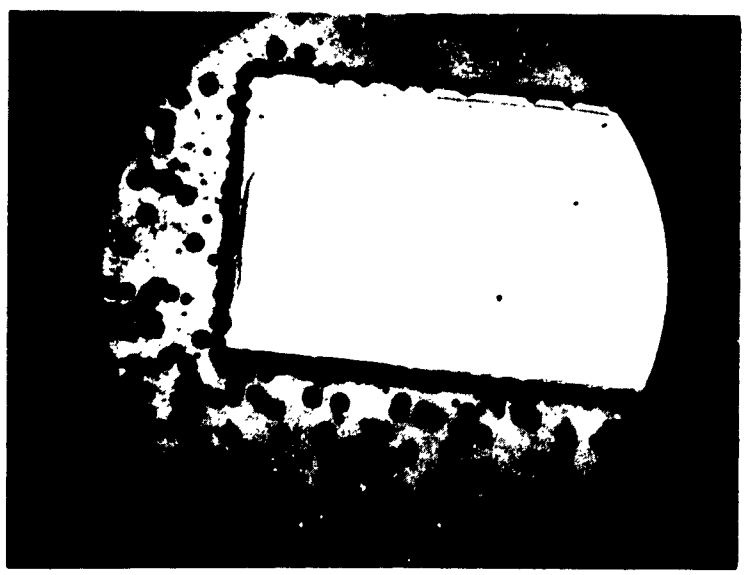


Figure 14
Hole Etched in Silicon Indicating:
(a) Unevenness of Growth in Etched Out Hole
(b) Polycrystalline Growth That Abounds Over the Surface of the Wafer

over the entire wafer, and finally, polishing smooth the step in the second layer caused by the localized growth. This latter step has been initiated since analysis of the first device (completely processed with a buried layer) shows that the epi step caused by the localized growth is too steep for adequate adherence of the metallization.

2.3 KMER Process Technology

The general status of photolithographic is good in routine processed materials. Using KMER, image resolution is quite adequate down to 1/2 mil wide lines.

A severe problem of resist adhesion during etching has occurred on certain specialty diffusion processes. These processes had a common denominator of glass growing by purely dry oxygen methods. Alteration of DF cycle processes has eliminated this problem.

Adhesion problems and resist removal problems are areas of further study and are being investigated.

2.4 Semiconductor Device Surface Technology

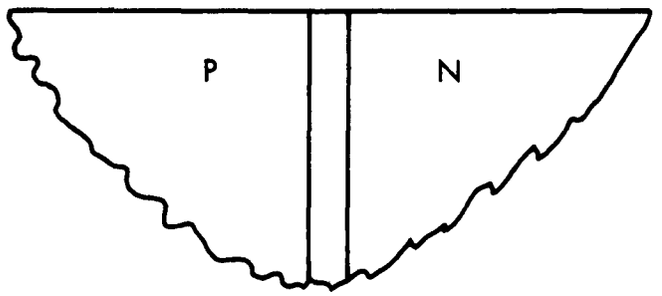
One of the most important fields in semiconductor technology, and one about which relatively little is understood, is surfaces.

The semiconductor surfaces of a p-n junction device (and of many not utilizing p-n junctions) are of vital concern; they control many of its important characteristics, and also its

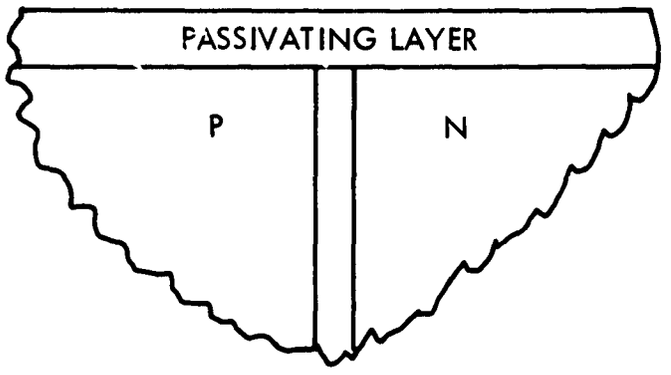
stability. For the example of a silicon transistor, the emitter junction surface area controls its current gain, the collector junction surface area its reverse leakage current and breakdown voltage.

There are three cases to be considered for a p-n junction intersecting a surface, as shown in Figure 15. Figure 15(a) depicts a surface without any purposefully added passivating layer such as occurs in alloy and mesa devices. Figure 15(b) illustrates a passivated junction. The passivating layer may be silicon dioxide (as is commonly the case with planar devices) an organic layer (i.e., silicon varnish, which is often used for high voltage rectifiers), glass (used for some diode types), or other lesser used materials. An encapsulating layer, Figure 15(c), is sometimes placed on top of the passivating layer. If the passivating or encapsulating layer is thick enough, it may form the package for the device. More generally, however, a separate glass-to-metal seal hermetic package is utilized.

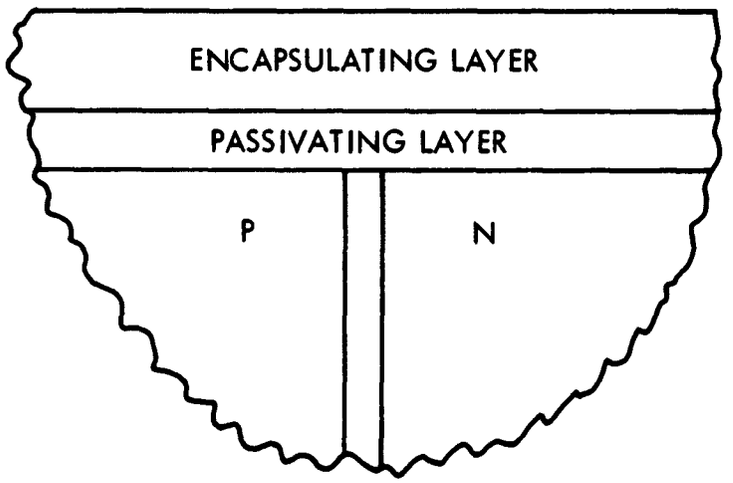
Because it shows promise of future application far larger than any other semiconductor material, silicon alone will be considered for the course of this program. There is no question that much of what is learned using silicon, particularly the surface effect models, can be applied to other semiconductor materials (i.e., germanium, gallium arsenide). However, since each material displays different properties, surface work on devices made from each material of importance must eventually be done. Also, since silicon p-n junctions employing surface layers have demonstrated properties unattainable by those without them (i.e., high injection efficiency at low currents), and are applicable to a much wider range of components (i.e., integrated circuits, UHF transistors), this study will be limited to them.



(a) Bare Surface



(b) Surface with passivating layer



(c) Surface with passivating and encapsulating layers

Figure 15

We are concerned with two main types of effects, both of which give rise to electrical characteristics in parallel to those of the bulk p-n junction under consideration.

1. Electrical effects induced in the silicon by charges on, or slightly removed from, the silicon surface. The shunt electrical effects in this case occur in the silicon in a very thin surface layer.
2. Electrical effects occurring on the surface of the silicon on or in the passivating or encapsulating layer. The shunt electrical effects in these cases occur outside the silicon.

Both of the above types of effects can occur simultaneously. Considering the low reverse leakage currents commonly attainable with silicon p-n junctions (i.e., 1na at 10 volts), a shunt resistance of 10^{10} ohms or less will constitute a major perturbation. Hence, surface conduction over the glass (or ceramic) on the outside of the package (between terminals) can be a major consideration. Because of the very high electrical impedances displayed by reverse-biased p-n junctions, passivating and encapsulating layers, and package insulations, these effects generally occur very slowly compared to the operating speed of a device.

A thorough investigation of surface effects must include consideration of effects induced in the silicon by

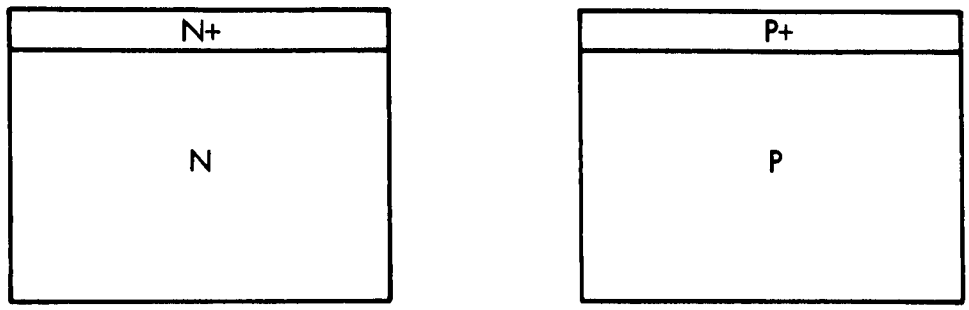
(a) Charges at the silicon-passivating layer interface (or on the silicon surface if no passivating layer is used)
(b) Charges in the passivating layer

(c) Charges at the passivating layer-encapsulating layer interface
(d) Charges in the encapsulating layer

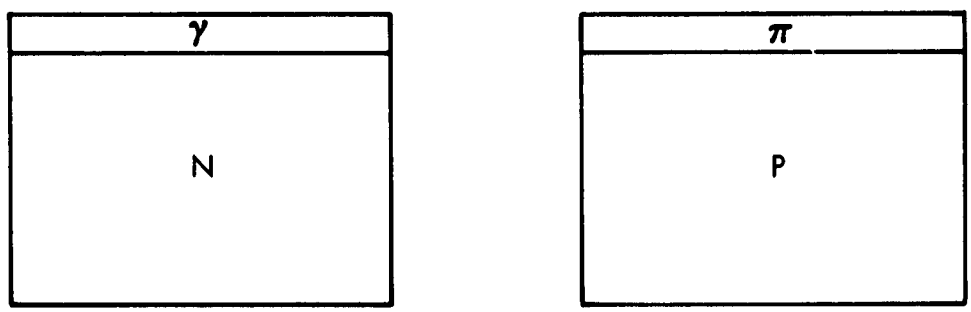
It is possible to have a fixed charge, in which case it controls device characteristics but does not produce changes with time. Of major concern, however, are the charges that can either move as ions or polar molecules along a surface or interface or through a layer, or remain fixed but exhibit an electronic transfer and, hence, change their state of bonding (i.e., from physical adsorption to chemisorption). It is assumed here that the encapsulating layer is so thick that charges on its surface cannot produce an effect in the silicon; if this is not the case, it becomes a second passivating layer.

There are three types of surface layers that can be induced; accumulation, exhaustion, and inversion (channel) as shown in Figure 16. Of major importance is the change in effective lifetime (or surface recombination velocity) that accompanies any of these surface conditions. The changed surface state condition, or, for the same surface state distribution, the changed surface potential, can both (or in combination) produce extremely large effects on device performance.

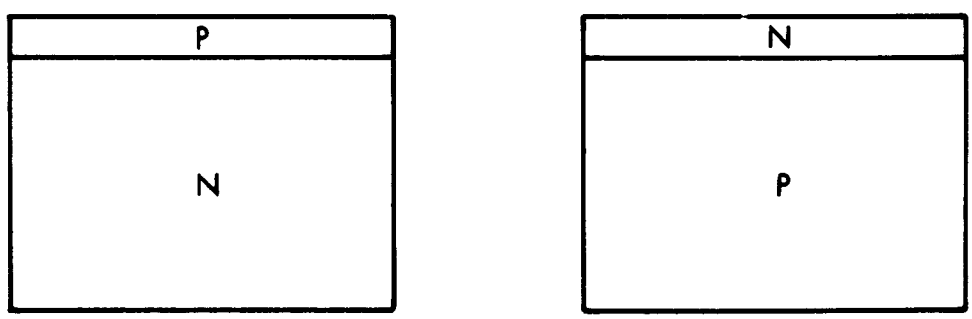
It is to be emphasized that we are considering only induced surface effects, and not layers that are produced by chemical doping as would occur, for example, if oxide masking during one or more diffusion steps were not entirely effective. The induced nature of the effects can be demonstrated experimentally by repetitive cycling. The electrical performance of a device can be repeatedly changed (by a large factor) and repeatedly brought



(a) Accumulation Surface Layers



(b) Exhaustion Surface Layers



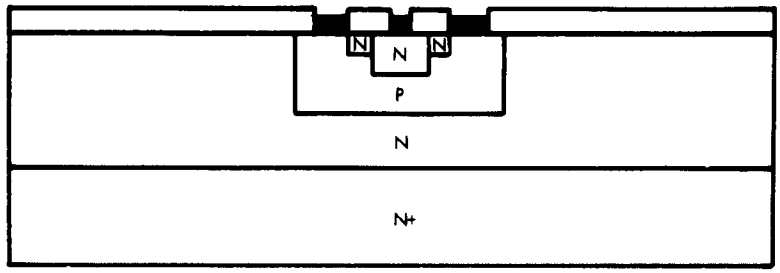
(c) Inversion Surface Layers (Channels)

Figure 16

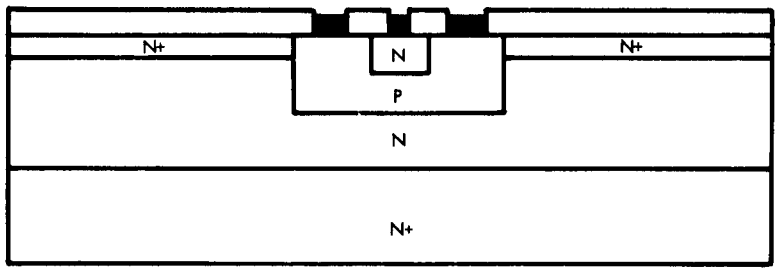
back to its initial condition. Experiments of this type, by virtue of demonstrating how precisely electrical characteristics can be reproduced cyclically, in most cases can be used to indicate the charge we are dealing with is a constant. Hence, this charge must be a definite part of the surface system rather than moving to or from the surface with time.

Some surface conditions that commonly cause transistor failures are shown in Figure 17. The limited base channel can cause low current gain (and high emitter junction leakage current) if its recombination rate is high. The collector accumulation layer lowers BV_{CBO}. A collector inversion layer effectively changes the place where the base-collector junction intersects the surface from under the passivating layer to the edge of the pellet, which is not only unpassivated, but also has generally a very poor surface treatment. The annular process, recently introduced by Motorola to overcome this effect, was one result of device surface studies. The guard band introduced by this process, shown in Figure 17(d), prevents the base collector junction from reaching the edge of the pellet and forces it to the surface under the passivating oxide.

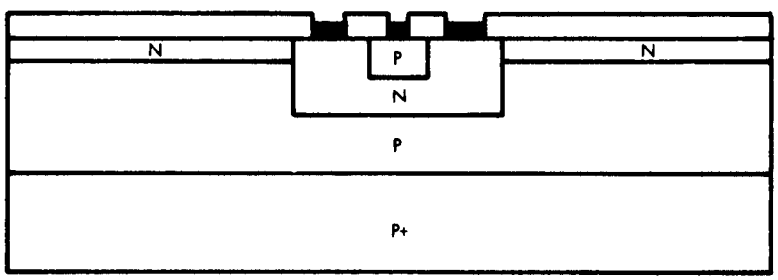
Silicon planar transistor structures are being used as the vehicles for surface studies. This concentrates effort on the problems of interest to transistors, minimizing unnecessary studies. Both pnp and npn versions will be utilized. The extreme sensitivity of transistors to surface effects makes them sensitive research tools, (i.e., leakage current changes by a factor of 10^6 can be induced by strictly surface means.) As the study progresses, other devices, integrated circuits, and also structures specifically designed for surface effects studies, will be utilized.



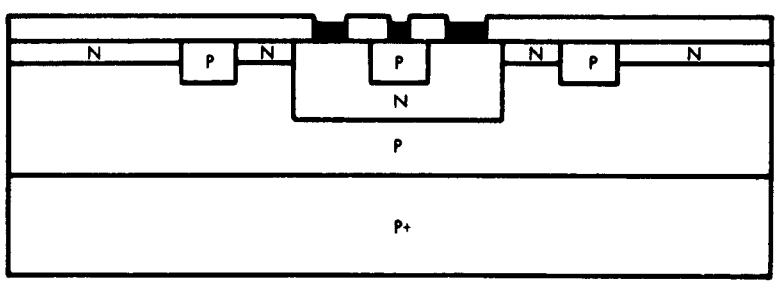
(a) Limited Base Channel - Low h_{FE}



(b) Extended Collector Accumulation Layer - Low BV_{CBO}



(c) Extended Collector Inversion Layer - Unpassivated Device



(d) Guard Band to Limit Extended Collector Inversion Layer

Figure 17

Some specific items that are being studied as part of a device surfaces program are:

1. Effects of diffusion of gases through passivating and encapsulation layers. It is known, for example, that hydrogen has a higher diffusion coefficient through SiO_2 at 300°C than boron through silicon at 1100°C (or gold through silicon at 500°C). It appears that hydrogen produces a strong collector inversion layer in npn transistors, and that, since the effect can be removed by a modest voltage and current at room temperature, the diffusing species is ionic.

2. Effects of fast diffusing impurities precipitating at the Si - SiO_2 interface during diffusion. Precipitates in the bulk are known to cause soft breakdown; their effects at the surface (or even whether or not they form at the surface) are unknown. Included are accidental impurities, as well as those purposely added to control lifetime (i.e., gold).

3. Effects of the pure Si - SiO_2 interface. The "grading" of the Si to SiO_2 transition, dangling bonds, interface activity, and diffusion are all factors vitally affecting the surface condition. For example, it appears that donor levels at the Si - SiO_2 interface can provide electrons sufficient to compensate 2 - 4 Ω-cm p-type silicon.

4. Use of the new electron microscope at the Motorola Semiconductor Products Division to study the surface of the passivating layer for pinholes, cracks, and other structural defects.

5. Treatment of the outside surface of the passivating layer, exclusive of any encapsulating layer, to minimize adsorption of gases. For example, SiO_2 is hydrophillic, can be made to be hydrophobic by means of a properly bonded organic molecular layer.

6. Identification and transport mechanisms of ionic materials through passivating layers.

7. Use of low temperatures for studies of mobility on surfaces and along interfaces.

8. Use of high stress conditions (temperature, current, voltage, transverse field, ambient atmosphere) in various combinations to accelerate surface effects. The use of high temperatures (up to 500°C is planned) requires the use of a metallurgical contact system that is stable under these conditions. This type of system has been developed at Motorola, utilizing only aluminum (aside from the header leads).

9. Sorting out failure modes. In many cases, more than one mechanism will be active at the same time, sometimes producing counteracting effects. This will require utilizing different surface treatments (i.e., oxide formation and processing steps) beginning with the first surface treatment the wafer sees.

10. Study the feasibility of producing surface conditions that are different for different parts of a structure. For example, in a transistor it may be desirable to have a different surface condition at emitter and collector junctions; in integrated circuits, different elements (i.e., npn and pnp transistors) may require specific and conflicting surface conditions.

11. As surfaces become better understood and controllable, evaluate the feasibility of improved devices that utilize surface effects for their operation (i.e., isolated-gate field-effect transistor, silicon hot carrier rectifier, metal-oxide-semiconductor (MOS) varactor diode).

Summary - Many surface effects of vital importance to the operation and reliability of silicon planar passivated structures have been experimentally verified or inferred. The results of this

research will yield fundamental information concerning surface-controlled transistor parameters, reliability, process control, and reproducibility. In addition, the information will be of direct application to other semiconductor devices, integrated circuits, and that class of devices utilizing surface effects for their fundamental mode of operation.

2.5 High Speed Monolithic Development

A 3-input high speed monolithic gate (IC3361) has now been developed by R&D and placed in production. A photograph of this unit is shown in Figure 18.

A very detailed report on a sample of 14 units is attached. From these figures, it is seen that the unit runs into soft saturation at elevated temperatures. Gold diffused units will be characterized very shortly, and various experimental runs have been made to decrease R_{SAT}. No characterization has yet been done on the low R_{SAT} units.

Dimensions and important parameters of the transistors used in the 3361 gate are shown in Figure 19.

High speed monolithic half adders have been produced and are currently being characterized.

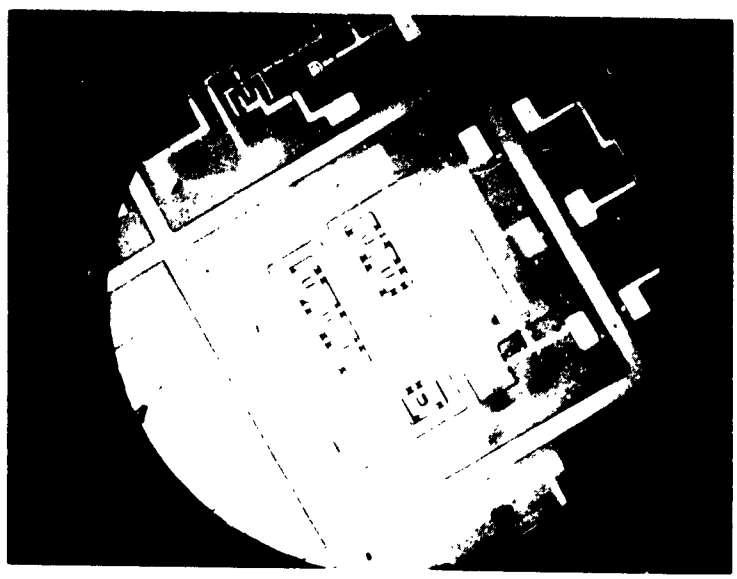
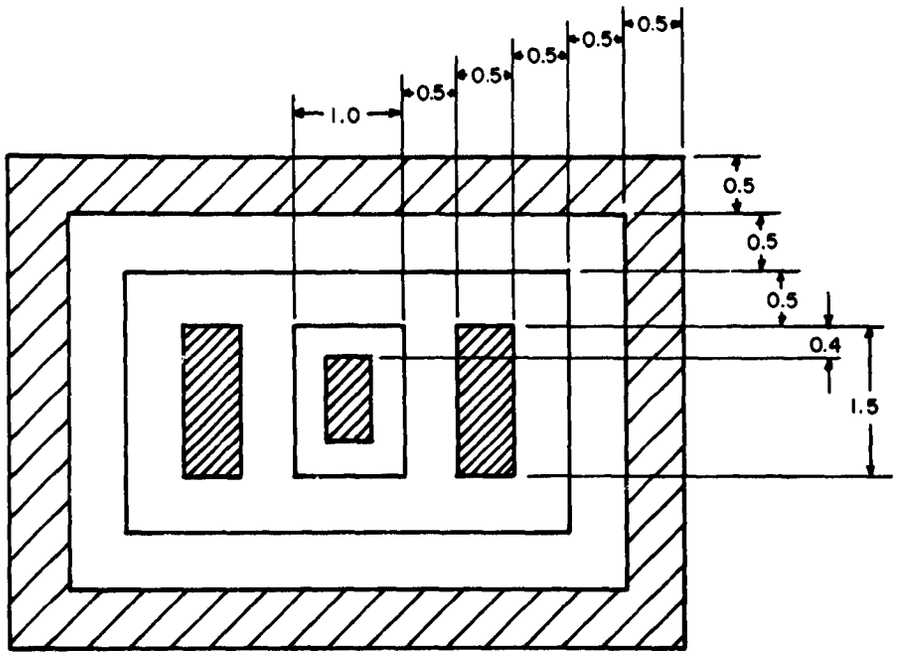


Figure 18

High Speed Monolithic Gate



DIMENSIONS OF IC3361 MONOLITHIC GATE TRANSISTOR
(ALL DIMENSIONS IN MILS)
FIGURE 19

IC 3361 Transistor Characteristics:

PARAMETER	TYPICAL	CONDITIONS
BV_{CBO}	40 V	100 μA
BV_{EBO}	6.8 V	100 μA
BV_{CEO}	25 V	100 μA
BV_{CSO}	60 V	100 μA
I_{CBO}	<1 nA	-10 V
I_{EBO}	<1 nA	-5 V
I_{CSO}	<1 nA	-20 V
$V_{CE(sat)}$	0.75 V	I_B = 1 mA, I_C = 10 mA
C_{OB}	2 pf	-5 V
C_{CS}	4 pf	-5 V
f_τ	500 mc	β = 1
T_{ON}	12 ns	$I_{b_1}=I_{b_2}=I_c$=10mA
T_{OFF}	33 ns	$I_{b_1}=I_{b_2}$=3 mA, I_c=10 mA
T_{ST}	25 ns	$I_{b_1}=I_{b_2}$=3 mA, I_c=10 mA

3.0 120 Mc RF AMPLIFIER FABRICATED WITH COMPATIBLE TECHNIQUES

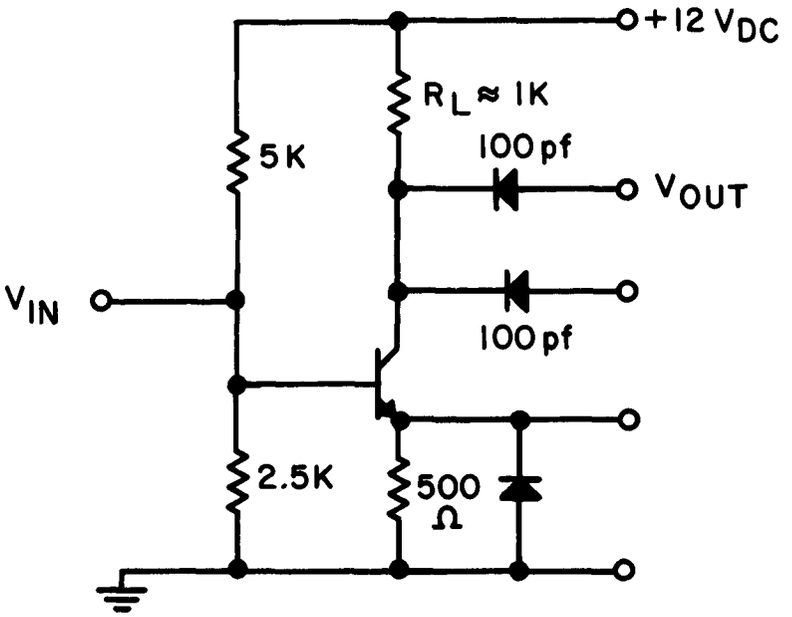
3.1 Introduction

To demonstrate the compatibility of the various thin film technologies with silicon integrated circuits, a research vehicle was chosen which would illustrate the advantages of thin film components such as resistors and capacitors, over the diffused versions. As a result, an amplifier circuit capable of operating at 120 Mc was chosen. This circuit requires both low-loss bias resistors and high Q coupling capacitors which are possible only by thin film techniques. In addition, the circuit was designed to compare various techniques such as nichrome resistors, tin oxide resistors, Al_2O_3 capacitors and SiO_2 capacitors along with the diffused versions.

3.2 Design

To obtain amplification at 120 Mc, a resistive type of isolation was used. This method is necessary at higher frequencies due to the losses in the standard junction type of isolation because of the associated parasitic capacitances.

The basic amplifier circuit is shown in Figure 1. The bypass and coupling capacitor values were chosen to obtain a broad band operation between 10 and 120 Mc. The bias resistors were determined by a design center of I_c at 5 ma. As may be seen from the values, the primary consideration was to obtain component values which could be integrated. The result of these considerations is shown in Figure 2, which is the response curve for the breadboard model of this amplifier.



120 Mc RF AMPLIFIER

FABRICATED IN THE MONOLITHIC FORM BY
COMPATIBLE TECHNIQUES

Figure 1

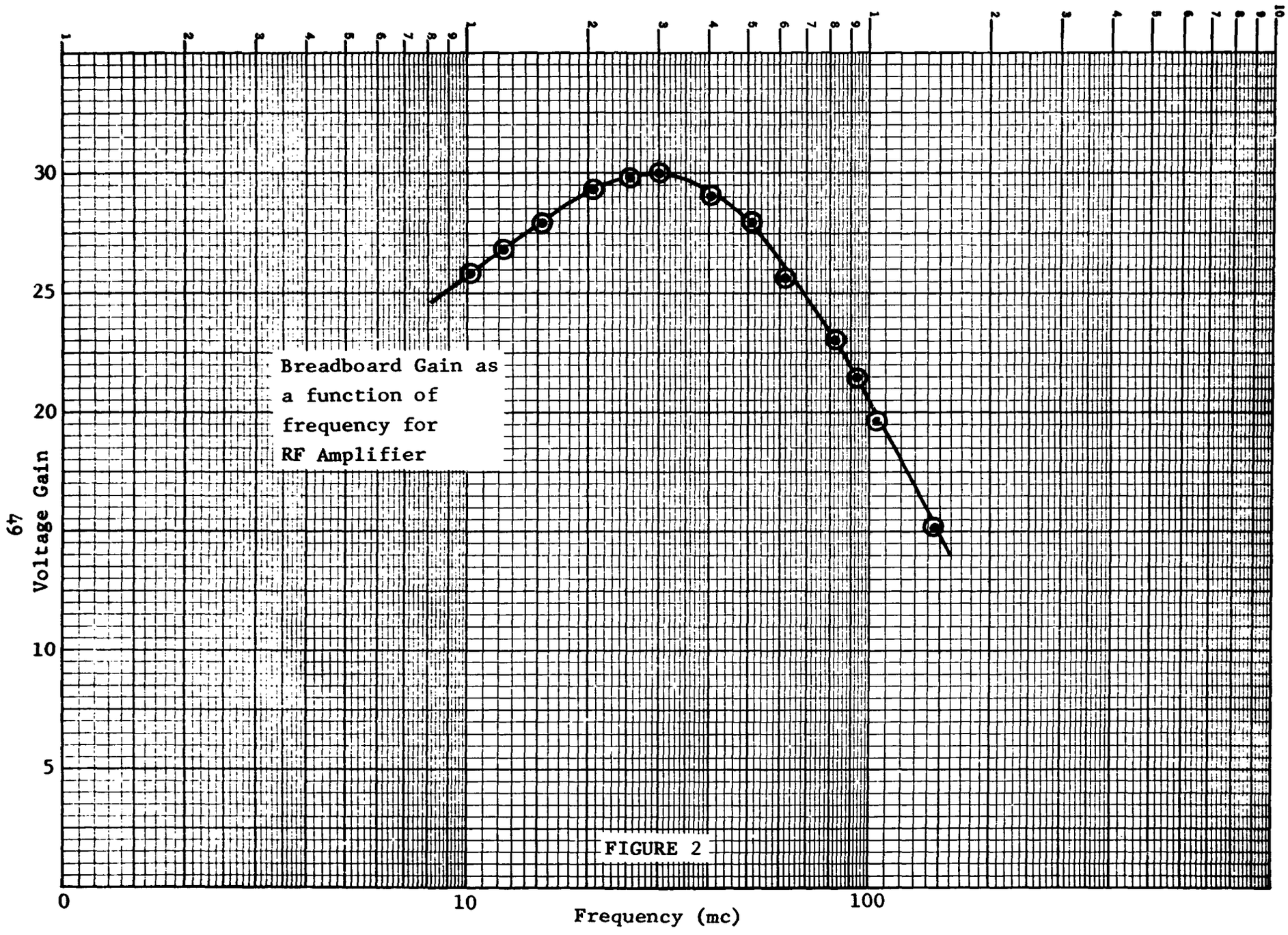

Breadboard Gain as
a function of
frequency for
RF Amplifier
Voltage Gain
30
25
20
10
5
0
10
100
Frequency (mc)

FIGURE 2

The load resistor R_L requires special consideration. Because the basic construction of the diffused portion of this amplifier utilizes resistive type of isolation, R_L is determined by the resistivity of both the substrate and the epitaxial material. As shown in the photo of Figure 3, the amplifier is formed on a 50 x 100 mil die of silicon. By locating the transistor and the coupling capacitor at one end and the supply voltage terminal and bypass capacitor at the other end, all parasitic shunt capacitance is thus eliminated. The remaining unoccupied area, approximately 50 mils square determines the value of the load resistor. Assuming a high resistivity substrate, (50 ohm-cm) and an epitaxial layer of 1 ohm-cm 10 microns deep, the value of the load resistor is approximately 1k. Because of the shunting effect of the lower resistivity epitaxial layer, the temperature coefficient is on the order of 2000 ppm/°C.

3.3 Compatible Processing of 120 Mc Amplifier

The VHF Amplifier Mask Set was designed to produce five different configurations of compatible circuits. A total of 26 different photo masks were utilized to give, 1) an all diffused circuit, 2) diffusion plus nichrome resistors, 3) diffusion plus tin oxide resistors, 4) diffusion plus Al_2O_3 capacitors and 5) diffusion plus SiO_2 capacitors. The masks and the process procedure are designed to obtain compatibility in materials, etching and surface structures.

3.3.1 Diffusion

As a control for performance comparison, an all diffused circuit was designed with both diffused resistors and junction type

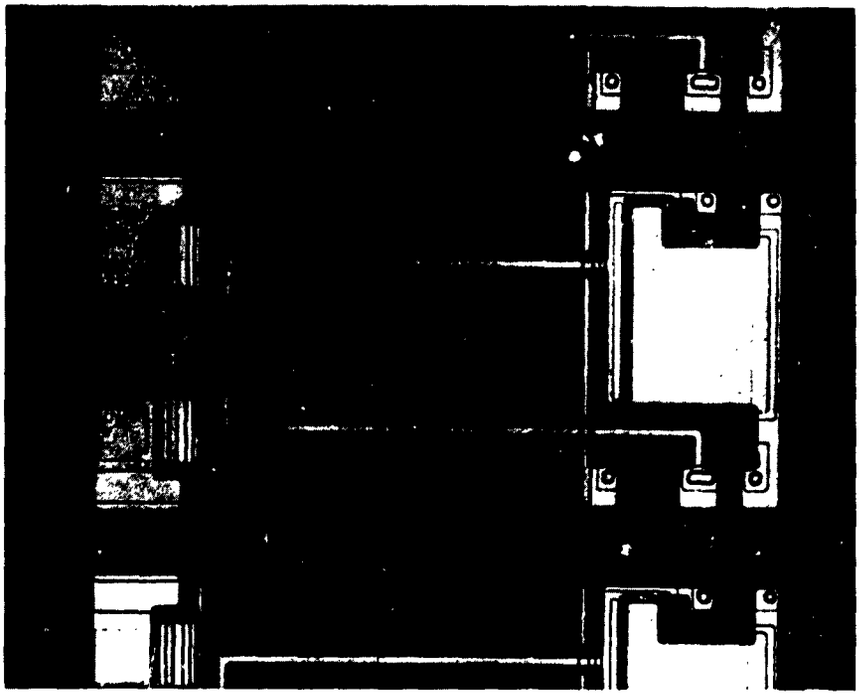


FIGURE 3

120 Mc RF Amplifier on 50 x 100 Silicon Die

capacitors. The substrate basic to all processes is formed by epitaxially growing a 10 micron layer of 1 ohm-cm n-type silicon on a 500 to 800 ohm-cm n type substrate. The epitaxial layer is then used for both the collector of the transistor and the load resistor. To increase transistor performance, the above process is modified to add a diffused N+ layer under the transistor prior to the epitaxial growth. This technique reduces the R_{SAT} of the transistor and, thus, increases the high frequency response. Mask Set #IC 295 RF 01-40 is used for this diffusion. For the all diffused amplifier, the next operation is the base oxide etch using mask #04-40. This step forms the pattern for the base of the transistor, the resistors, and the junction capacitors. The second diffusion step utilizes mask #05-40 to form the emitter fo the transistor and the junction capacitors. Mask #06-40 is used to form the ohmic contact areas for the circuit interconnections. The circuit is then completed with the aluminum metallization pattern formed by mask #08-40. Because these steps follow the standard integrated circuit processes, there is no problem of compatibility with the all diffused unit.

3.3.2 Diffusion plus Nichrome Resistors

One of the best examples of compatible thin film techniques is the use of nichrome to replace the diffused resistors. In this circuit, the use of nichrome resistors will greatly reduce any input losses caused by the shunt capacitance of the bias resistors.

The starting material for this circuit is the same as that for the all diffused version. Mask #01-40 is used to form the buried N+ layer under the transistor prior to the epitaxial growth.

MASK SET FOR ALL DIFFUSED UHF COMPATIBLE AMPLIFIER

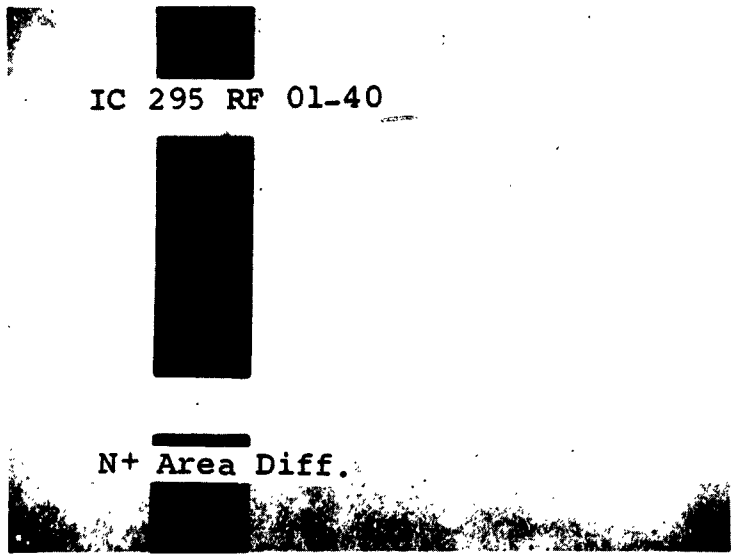


Figure 4

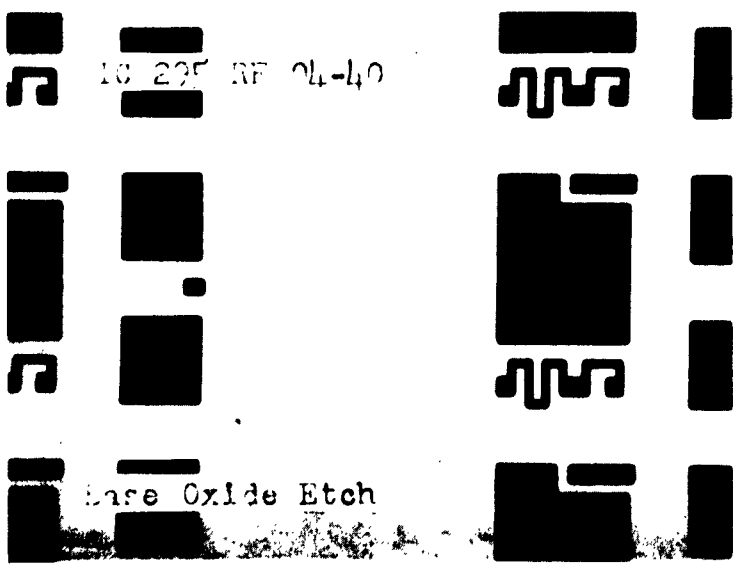


Figure 5

MASK SET FOR ALL DIFFUSED UHF COMPATIBLE AMPLIFIER

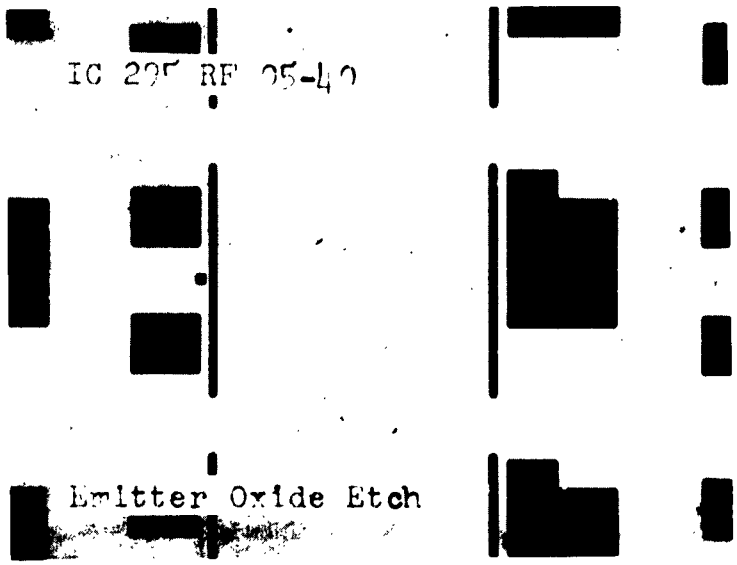


Figure 6

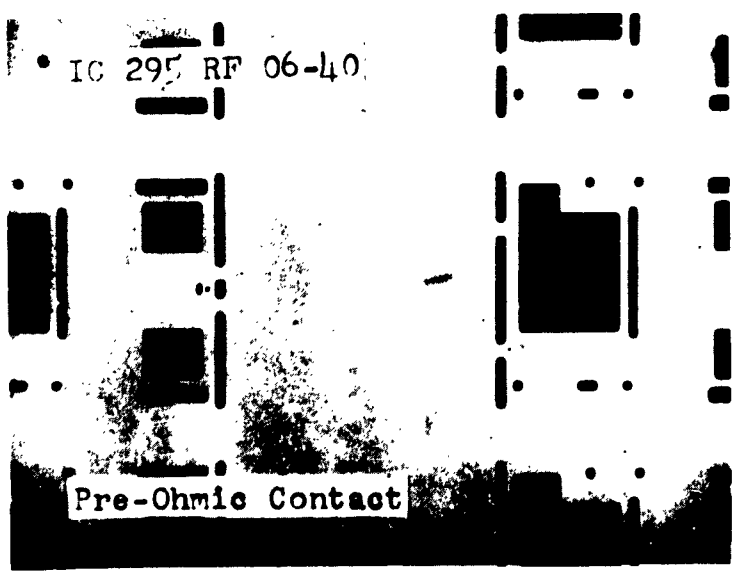


Figure 7

MASK SET FOR ALL DIFFUSED UHF COMPATIBLE AMPLIFIER

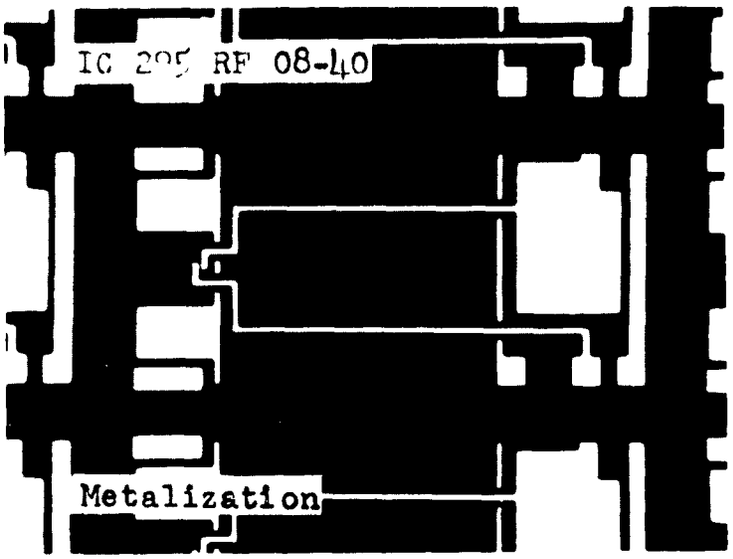


Figure 8

MASK SET FOR DIFFUSION PLUS NICHROME RESISTORS

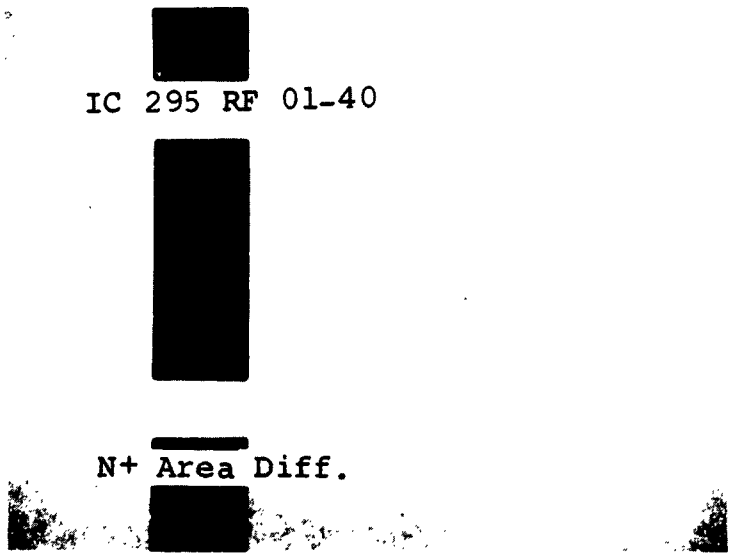


Figure 9

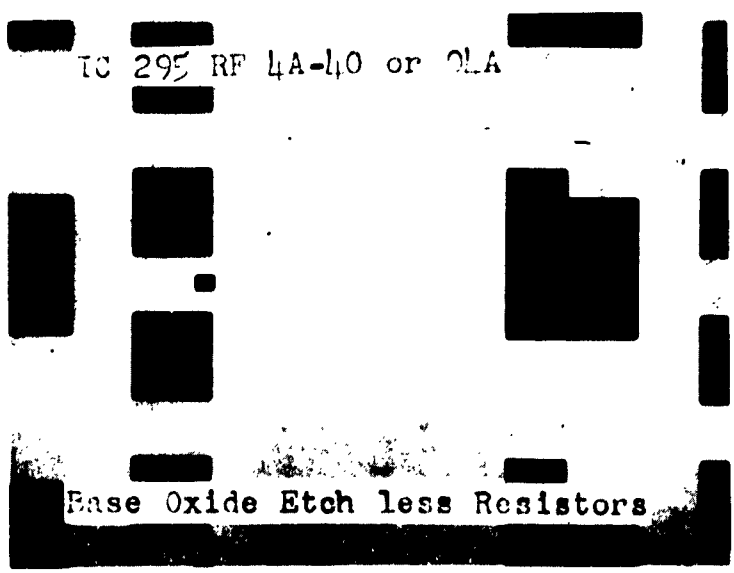


Figure 10

MASK SET FOR DIFFUSION PLUS NICHROME RESISTORS

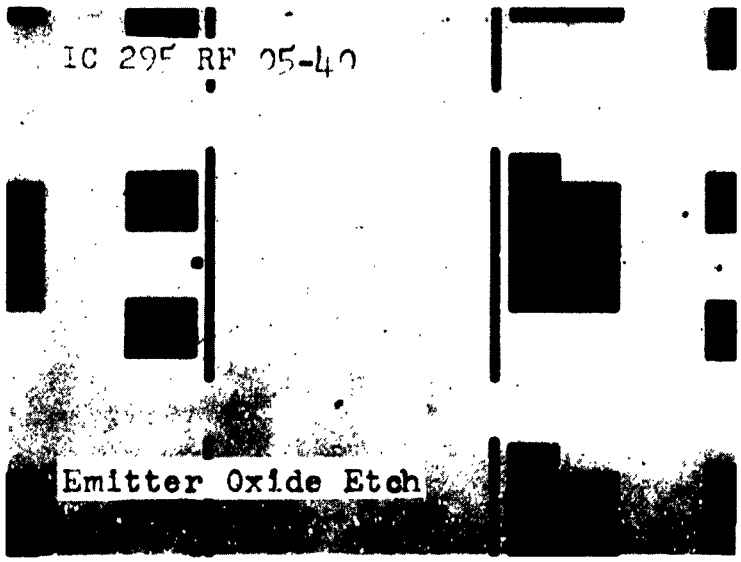


Figure 11

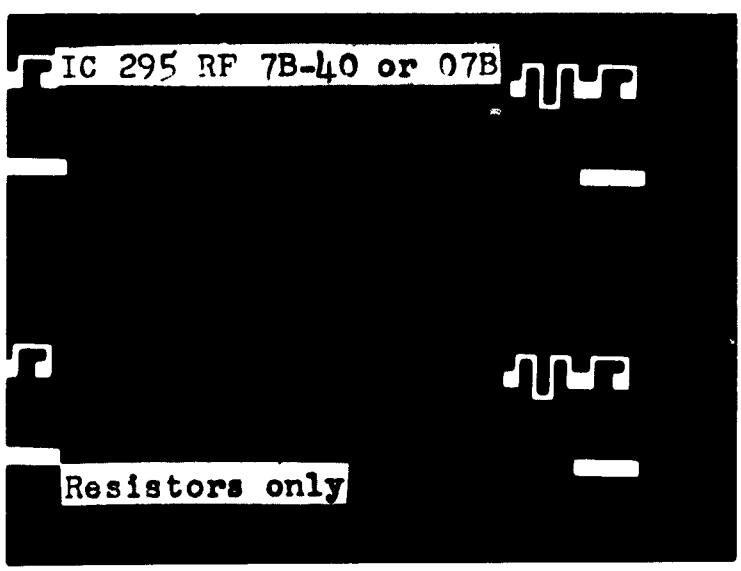


Figure 12

MASK SET FOR DIFFUSION PLUS NICHROME RESISTORS

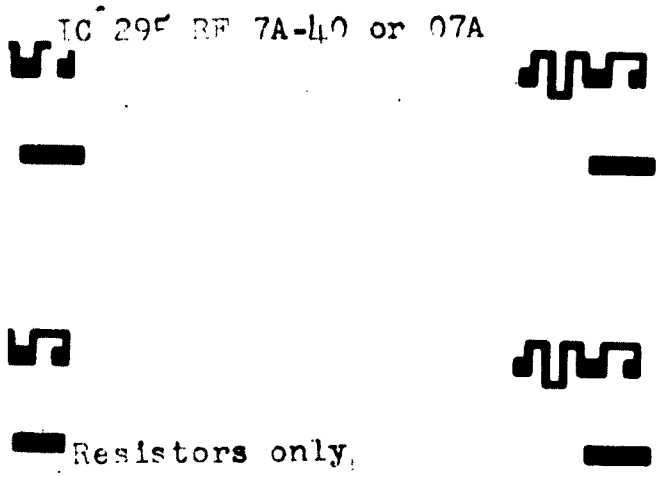


Figure 13

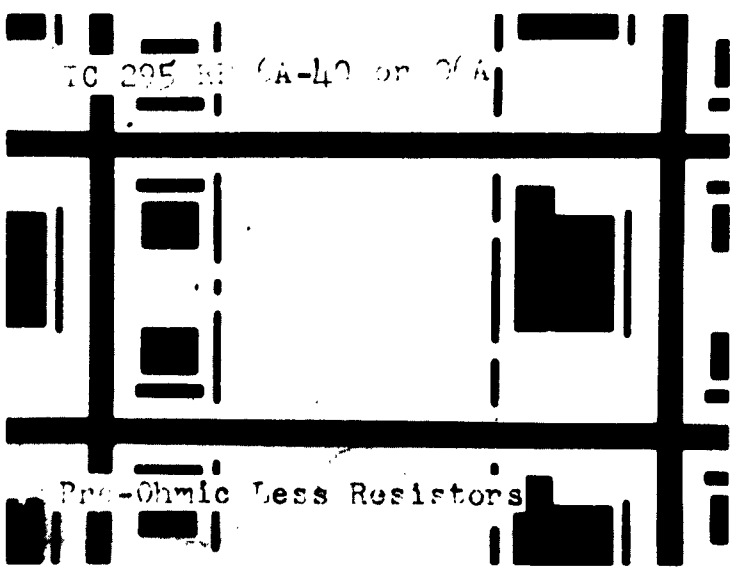


Figure 14

MASK SET FOR DIFFUSION PLUS NICHROME RESISTORS

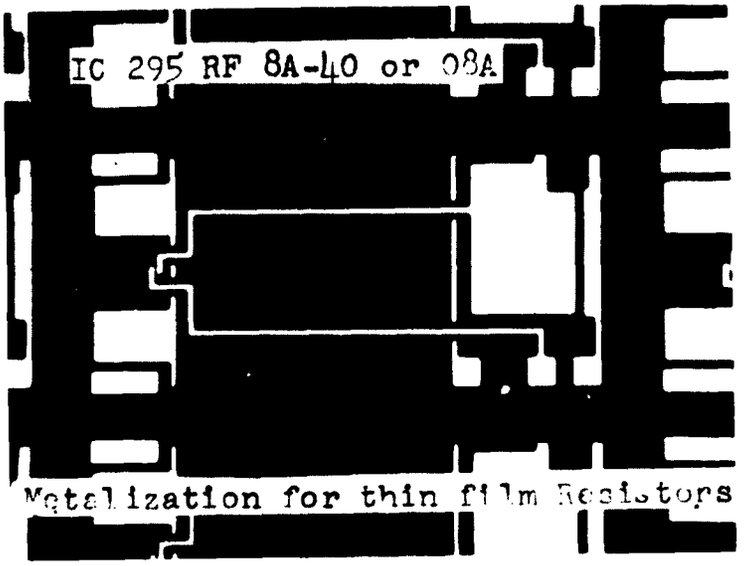


Figure 15

The epitaxial layer again acts as the collector material and as the load resistor R_L. Now, however, the base oxide mask #04A-40 only forms the base of the transistor and the junction capacitors. The resistors are formed at a later step. The emitter oxide etch mask #05-40 is the same as the previous circuit. Next, NiCr is deposited over the surface of the wafer and the resistor's patterns are found by photoresist techniques using mask #07B-40 or mask #07A-40 for reverse photo techniques. Ohmic contact to the diffused portions only, is made with mask #06A-40. The circuit is then completed by aluminum metallization with mask #08A-40.

This circuit required etching techniques which were compatible with the previously formed portions of the wafer. The chart of Figure 16 shows that NiCr etched by HCl will not affect the remainder of the circuit. A study of this chart will illustrate other examples of compatible techniques for SnO_2, Al_2O_3 and SiO_2.

3.3.3 Diffusion Plus Tin Oxide Resistors

The compatible techniques required for tin oxide resistors are identical with the previous steps for NiCr with the exception of a nichrome contact masking to obtain ohmic contact between the SnO_2 and the aluminum metallization. Masks #01-40, 04A-40, 05-40, 07B-40, 07D-40 or 07E-40, 06A-40, and 08A-40 are used in the process.

3.3.4 Diffusion Plus Al_2O_3 Capacitors

In this technique of compatible thin films, the resistors are formed by diffusion while the coupling and by-pass capacitors are found with an Al_2O_3 dielectric.

Material / Etch	Si	SiO_2	Al	NiC_r	Ni	SnO_2
CP4	X	X	X		X	
HPO_3			X		X	
HCl				X		X
HNO_3					X	
HF		X	X			

FIGURE 16

Chart of Compatible Etching Techniques

MASK SET FOR DIFFUSION PLUS TIN OXIDE RESISTORS

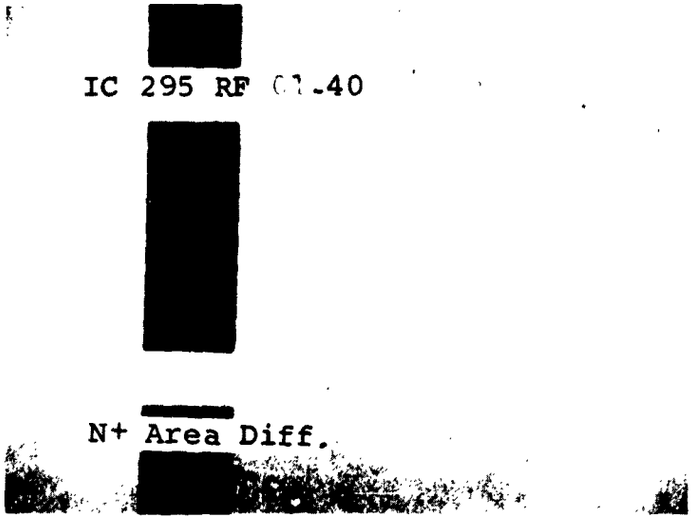


Figure 17

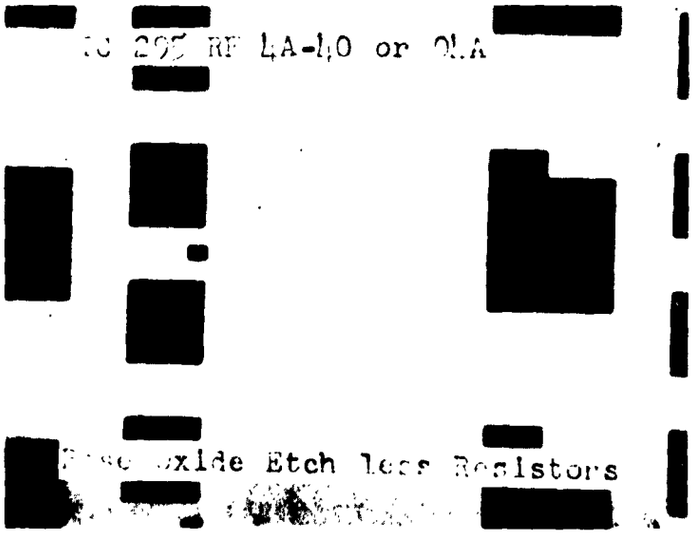


Figure 18

MASK SET FOR DIFFUSION PLUS TIN OXIDE RESISTORS

Figure 19

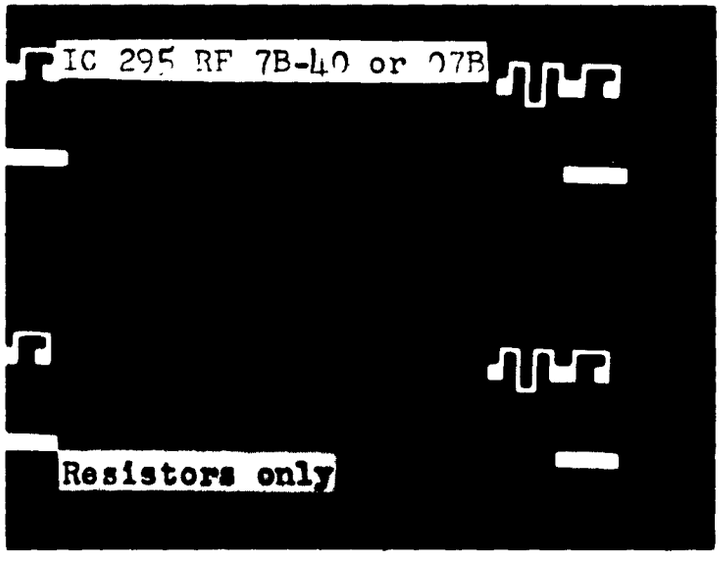


Figure 20

MASK SET FOR DIFFUSION PLUS TIN OXIDE RESISTORS

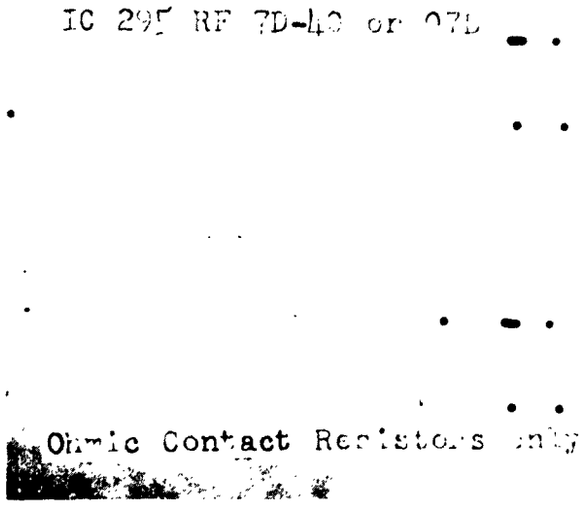


Figure 21

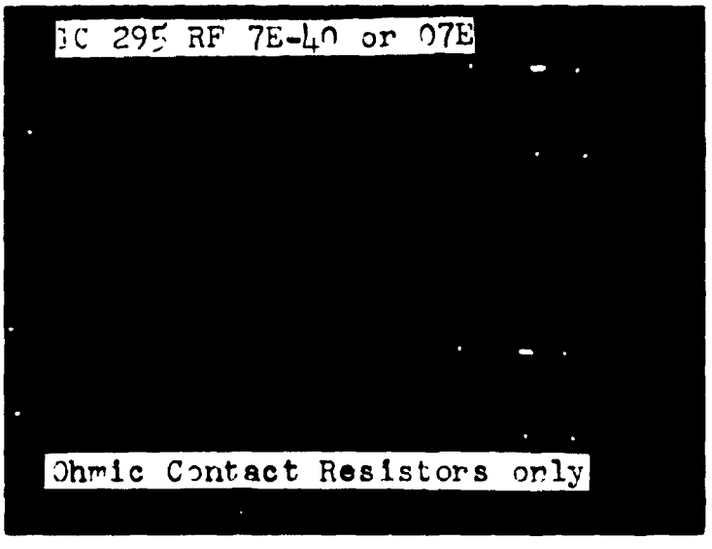


Figure 22

MASK SET FOR DIFFUSION PLUS TIN OXIDE RESISTORS

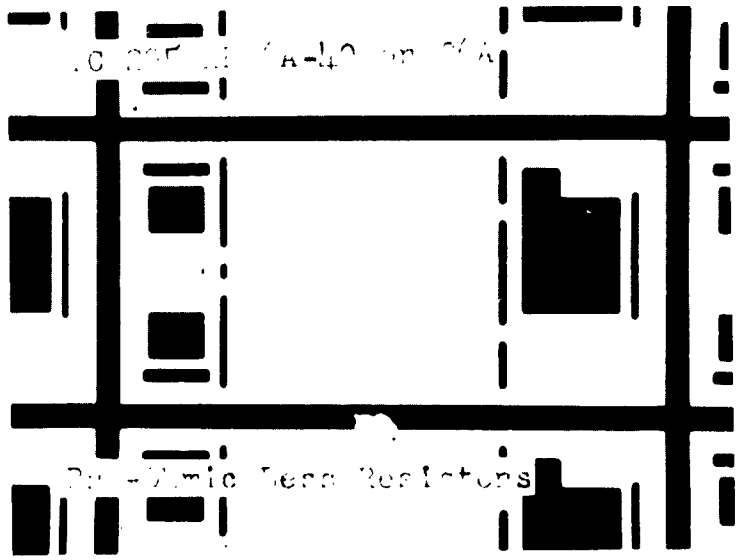


Figure 23

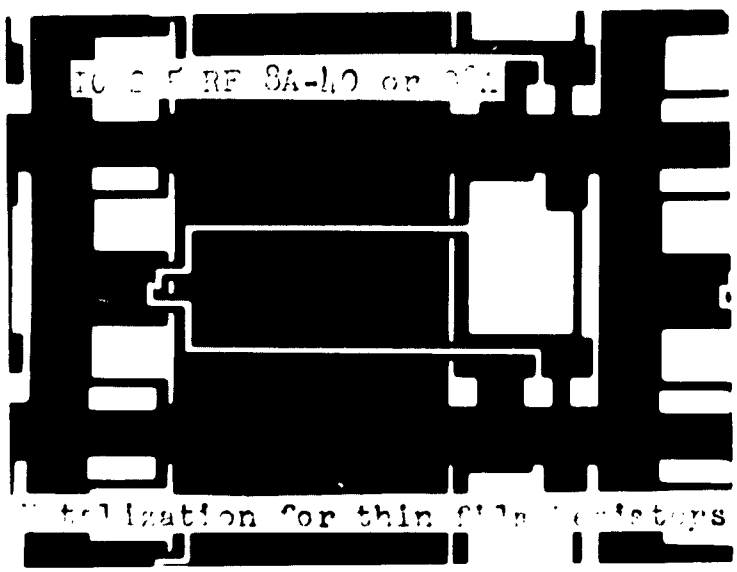


Figure 24

MASK SET FOR DIFFUSION PLUS Al_2O_3 CAPACITORS

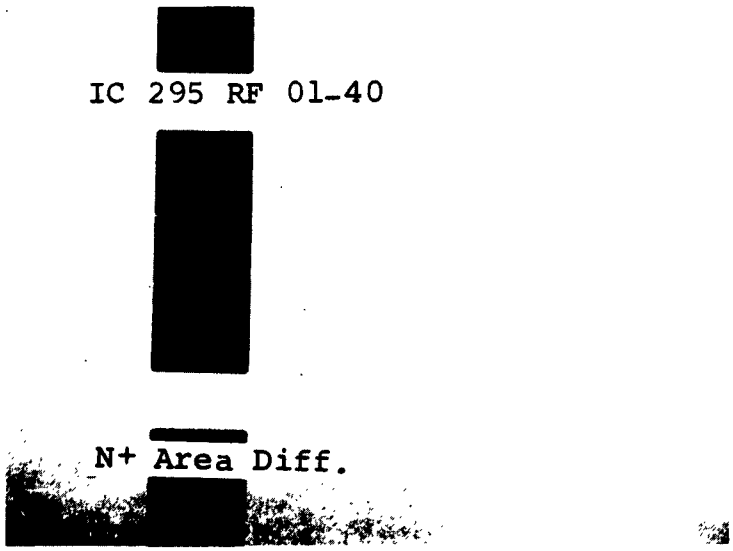


Figure 25

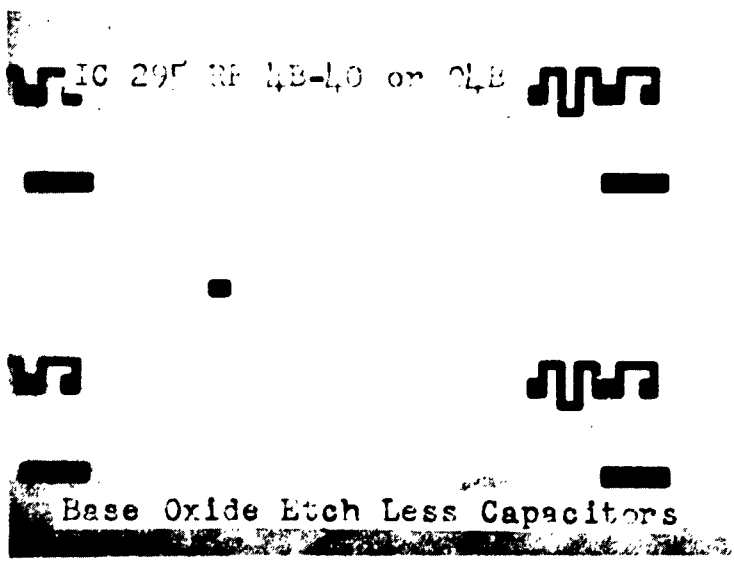


Figure 26

MASK SET FOR DIFFUSION PLUS Al_2O_3 CAPACITORS

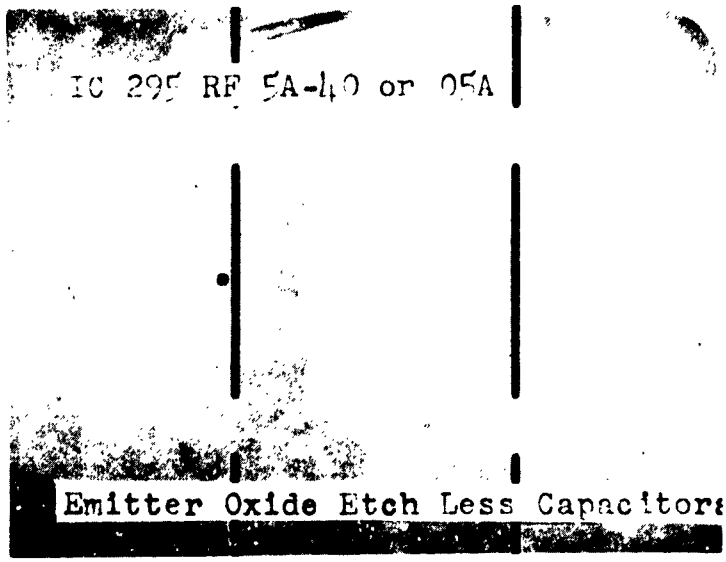


Figure 27

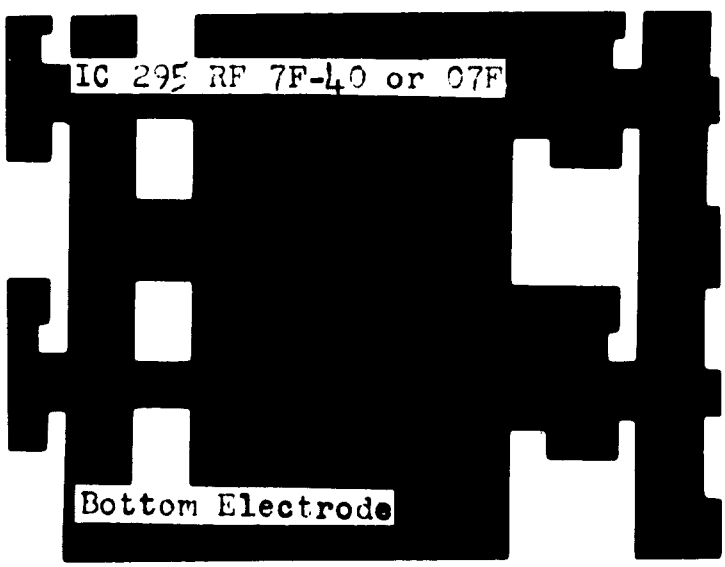


Figure 28

MASK SET FOR DIFFUSION PLUS Al_2O_3 CAPACITORS

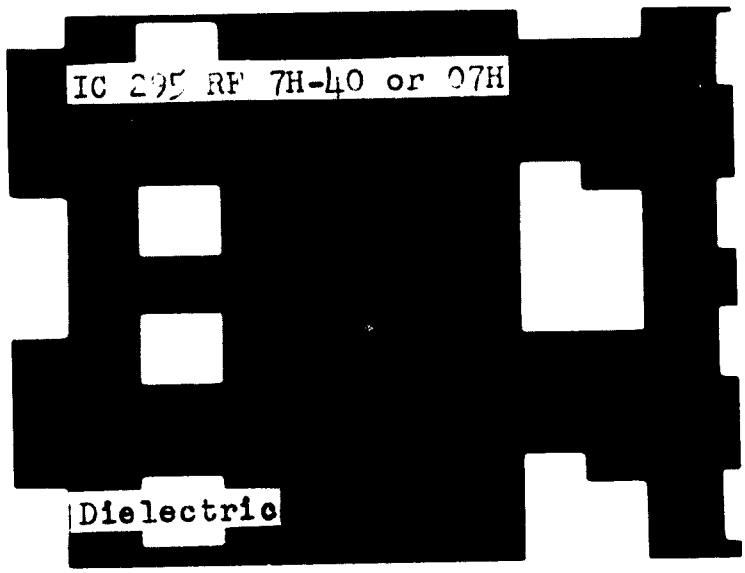


Figure 29

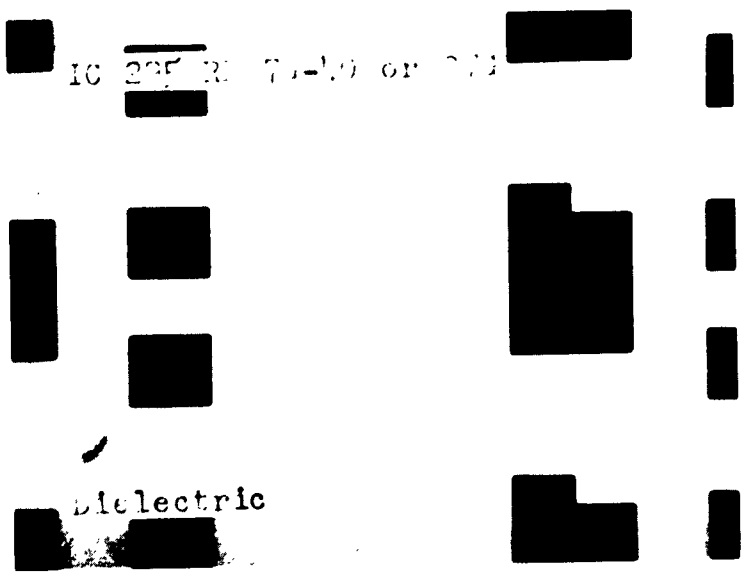


Figure 30

MASK SET FOR DIFFUSION PLUS Al_2O_3 CAPACITORS

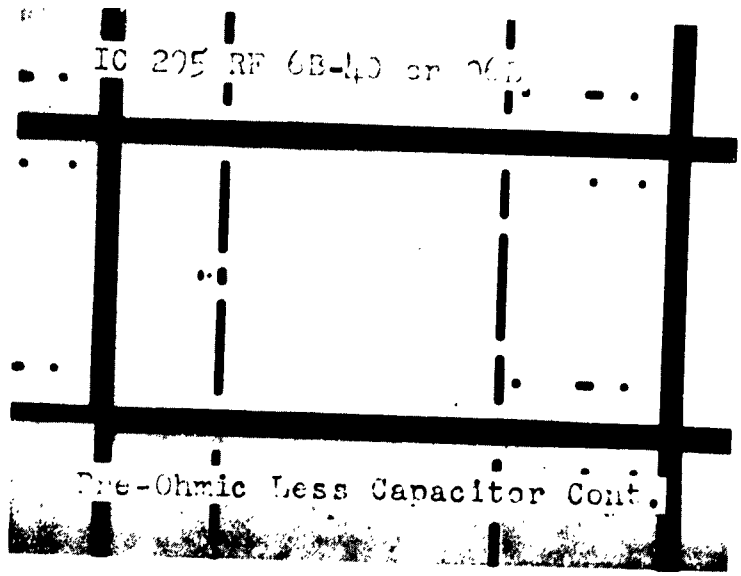


Figure 31

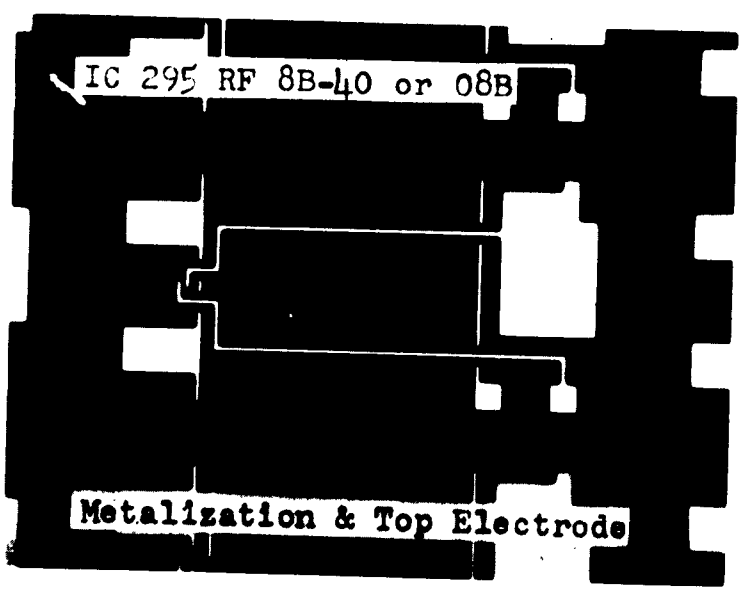


Figure 32

The basic techniques are the same as the previous steps. The following masks are used: #01-40, 04B-40, 05A-40, 07F-40, 07H-40 or 07G-40, 06B-40 and 08B-40.

3.3.5 Diffusion Plus SiO_2 Capacitors

Here, the resistors are again formed by diffusion, but the capacitor dielectric now becomes a thin layer (500Å of SiO_2). The following masks are used: #01-40, 04-40, 05B-40, 06C-40, 07J-40, and 08D-40. The result of this technique of construction is shown in the photo of Figure 39. Figure 40 is a chart of all five processes with the mask set required for each.

3.3.6 Nichrome Resistor Data

Some preliminary data has been taken on the first runs of the compatible UHF amplifier with NiCr thin film resistors. This data as shown in Figure 41, indicates that with further work, very accurate resistor ratio control is possible for applications such as bias resistors.

3.3.7 Test Results on the Compatible RF Amplifier

3.3.7.1 Summary of Previous Development

The RF Amplifier in the transreceiver is a grounded emitter RC coupled configuration (Figure 42). This design was selected because it lent itself easily to fabrication as a functional electronic block. Furthermore, such an RC coupled stage would serve as a general high frequency RF or IF amplifier, for use in the transceiver.

MASK SET FOR DIFFUSION PLUS SiO_2 CAPACITORS

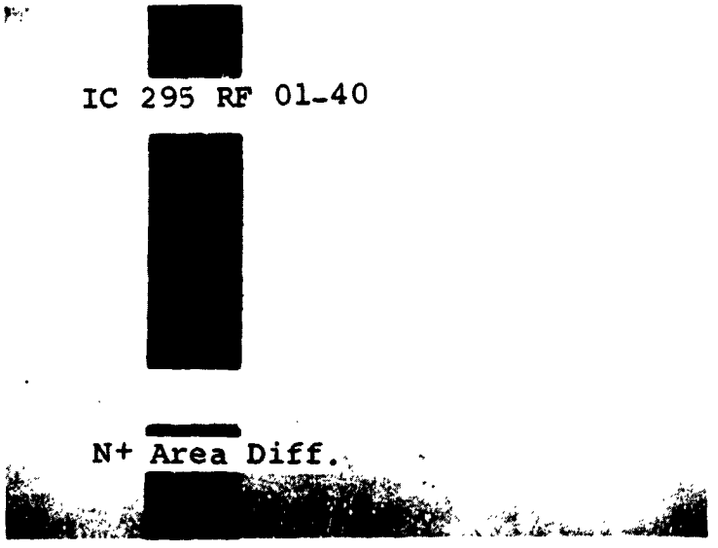


Figure 33

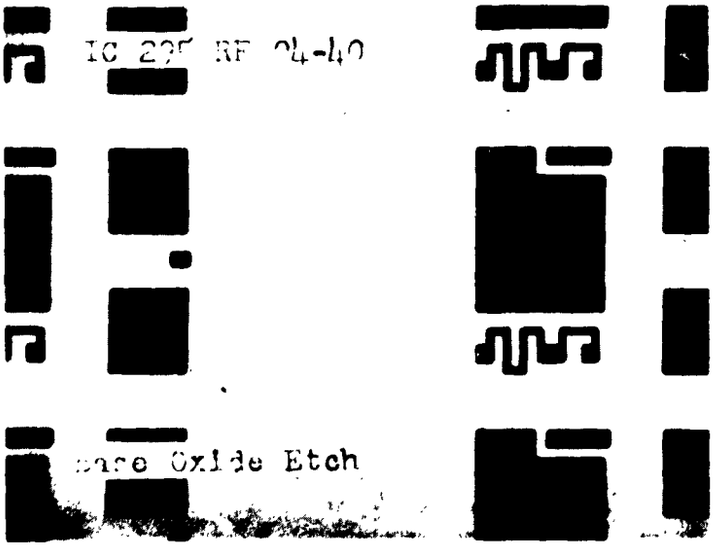


Figure 34

MASK SET FOR DIFFUSION PLUS SiO_2 CAPACITORS

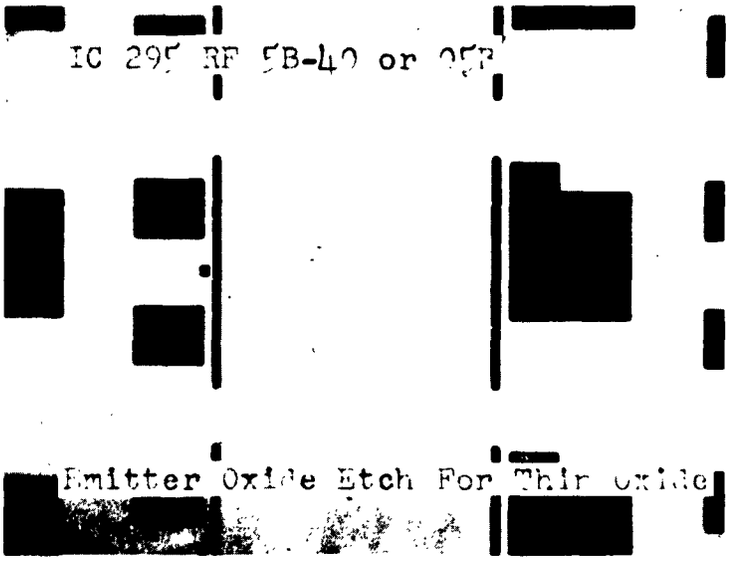


Figure 35

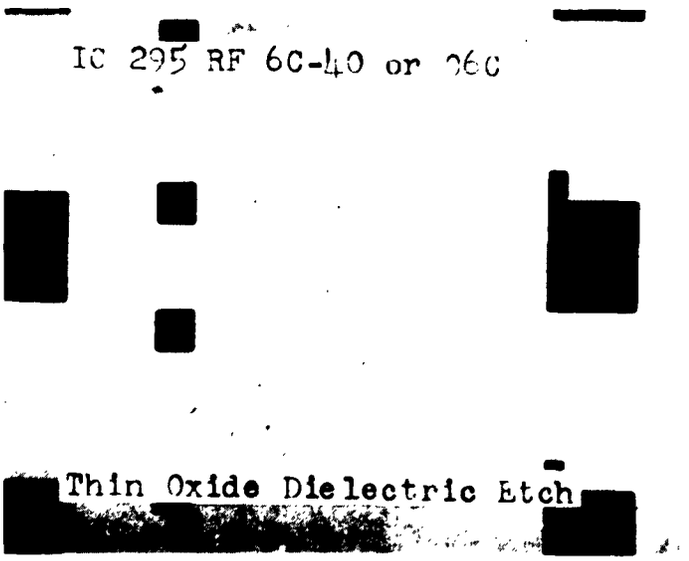


Figure 36

MASK SET FOR DIFFUSION PLUS SiO_2 CAPACITORS

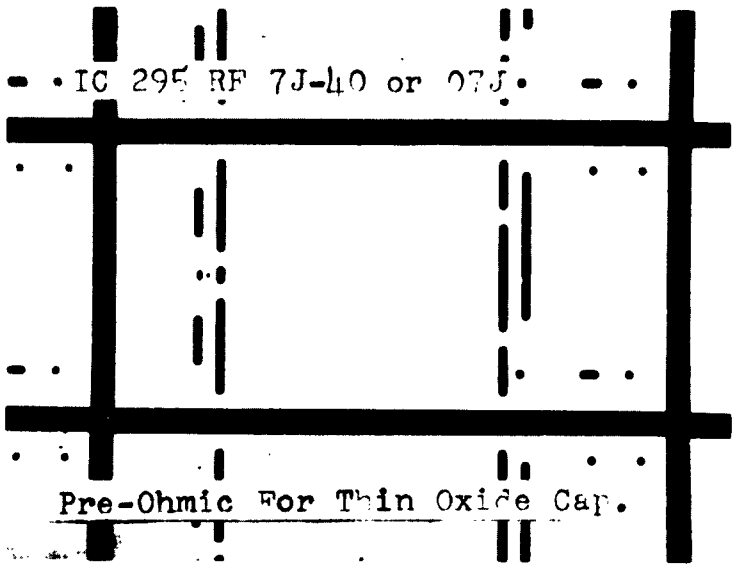


Figure 37

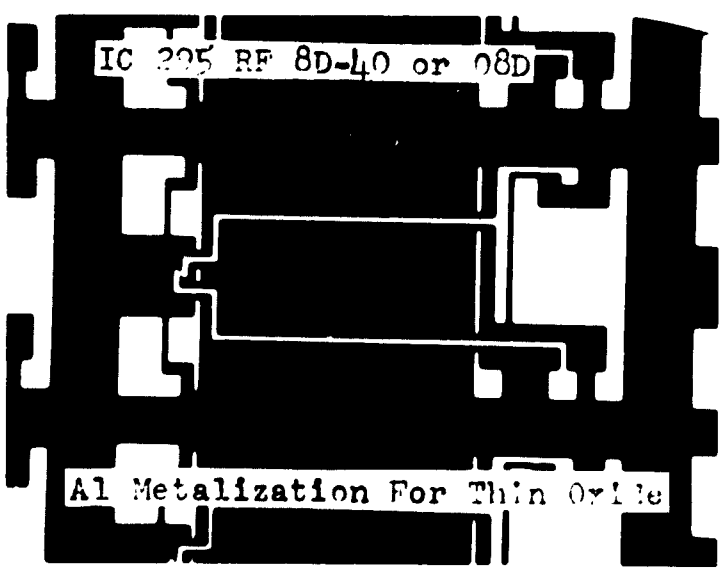
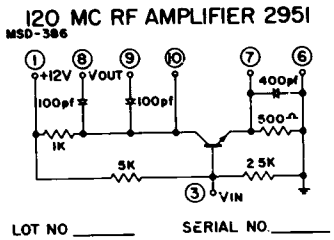


Figure 38



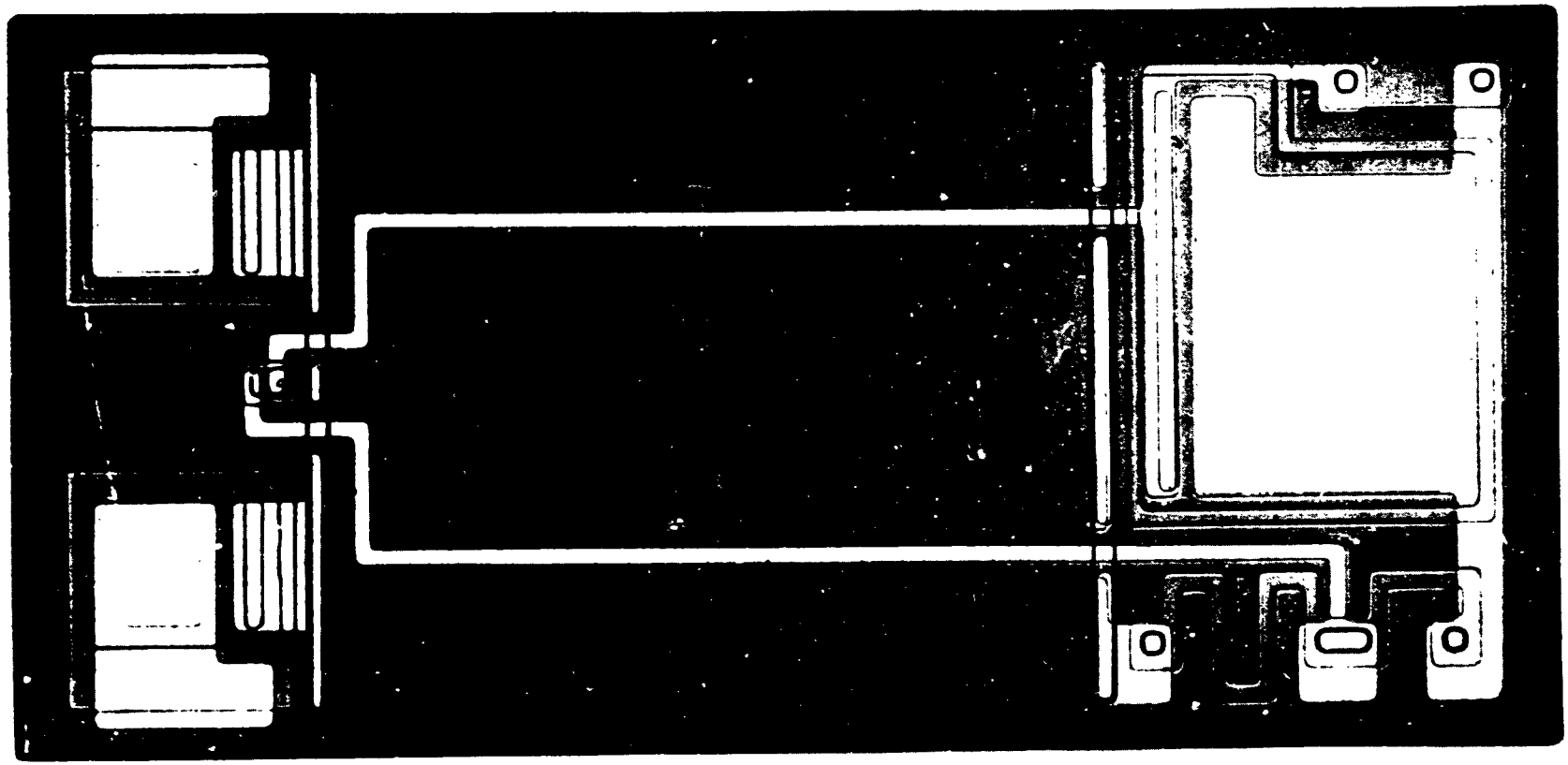


Figure 39

120 Mc RF Amplifier Utilizing SiO_2 Thin Film Capacitors

PROCESS / TARGET	DIFFUSION	DIFFUSION WITH NICHROME RESISTORS	DIFFUSION WITH TIN OXIDE RESISTORS	DIFFUSION WITH Al_2O_3 CAPACITORS	DIFFUSION WITH TIN OXIDE CAPACITORS
4	BASE OXIDE ETCH (P) IC295RF04-40	BASE OXIDE ETCH LESS RESISTORS (P) IC295RF04A-40	BASE OXIDE ETCH LESS RESISTORS (P) IC295RF04A-40	BASE OXIDE ETCH LESS CAPACITORS (P) IC295RF04B-40	BASE OXIDE ETCH (P) IC295RF04-40
5	EMITTER OXIDE ETCH (P) IC295RF05-40	EMITTER OXIDE ETCH (P) IC295RF05-40	EMITTER OXIDE ETCH (P) IC295RF05-40	EMITTER OXIDE ETCH LESS CAPACITORS (P) IC295RF05A-40	EMITTER OXIDE ETCH FOR TIN OXIDE CAPACITORS (P) IC295RF05B-40
	EMITTER OXIDE ETCH - TRANSISTOR ONLY (P) IC295RF05C-40				
6	PRE-OHMIC (P) IC295RF06-40	PRE-OHMIC LESS RESISTOR CONTACTS (P) IC295RF06A-40	PRE-OHMIC LESS RESISTOR CONTACTS (P) IC295RF06A-40	PRE-OHMIC LESS CAPACITOR CONTACTS (P) IC295RF06B-40	TIN OXIDE DIELECTRIC ETCH (P) IC295RF06C-40
7	OHMIC CONTACT (N) IC295RF07-40	RESISTORS ONLY (P) IC295RF07A-40 RESISTORS ONLY (N) IC295RF07B-40 OHMIC CONTACT LESS RESISTORS (N) IC295RF07C-40	RESISTORS ONLY (N) IC295RF07B-40 OHMIC CONTACT RESISTORS ONLY (P) IC295RF07D-40 OHMIC CONTACT RESISTORS ONLY IC295RF07E-40	BOTTOM ELECTRODE (N) IC295RF07F-40 DIELECTRIC (P) IC295RF07G-40 DIELECTIRC (N) IC295RF07H-40	PRE-OHMIC FOR TIN OXIDE CAPACITORS (P) IC295RF07J-40 OHMIC FOR TIN OXIDE CAPACITORS (N) IC295RF07K-40
8	ALUMINUM METALLIZATION ETCH (N) IC295RF08-40	ALUMINUM METALLIZATION FOR THIN FILM RESISTORS (N) IC295RF08A-40	ALUMINUM METALLIZATION FOR THIN FILM RESISTORS (N) IC295RF08A-40	TOP ELECTRODE AND METALLIZATION (N) IC295RF08B-40	ALUMINUM METALLIZATION FOR TIN OXIDE CAPACITORS (N) IC295RF08D-40

IC 295 MC RF AMPLIFIER

FIGURE 40

WAFER	AVERAGE RATIO OF R_1/R_2
4	1.7
7	2.2
11	2.15
1	2.2
2	2.1
3	2.33
8	2.8
12	2.1
Design Center	2.0

Figure 41

Ratios of NiC_r Bias Resistors on the VHF Amplifier

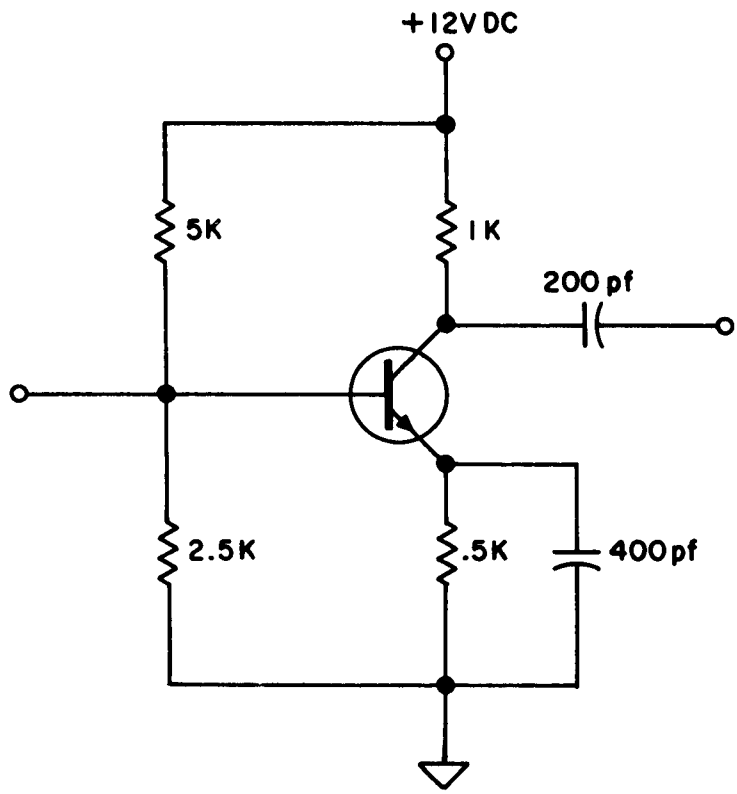


FIGURE 42
RF AMPLIFIER

Two types of FEB's were evaluated: 1) a diffused structure FEB with resistors and capacitors formed in the epitaxial layer by the same diffusions which form the transistor and 2) a compatible block using nichrome resistors and thin oxide capacitors. The results to date have shown that the thin film technique is to be preferred. The advantage of the compatible fabrication lies in the fact that the design of the resistor and capacitor elements is not compromised by the selection of impurity levels required by the transistor design. Use of the thin film elements also avoids the necessity of isolating each resistor and capacitor by means of a reverse biased diode, helping to eliminate parasitic capacitance effects.

3.3.7.2 Summary of Recent Developments

Gain versus frequency of the FEB RF amplifier is shown in Figures 43 and 44. These gain curves were taken with a 500 ohm load resistor capacitively coupled to the collector resistor of the FEB.

The curves of F_T versus V_{CE} and I_C are shown in Figure 45.

Comparative measurements have been made on the RF transistors fabricated in the FEB, both with and without the buried layer. The results are given in Table I.

Work on the compatible RF amplifier for the reporting period has been in the following areas:

(1) Evaluation of transistor performance which involves the evaluation of the buried layer technique. Comparative measurements have been made on FEB transistors with and without the buried layer approach.

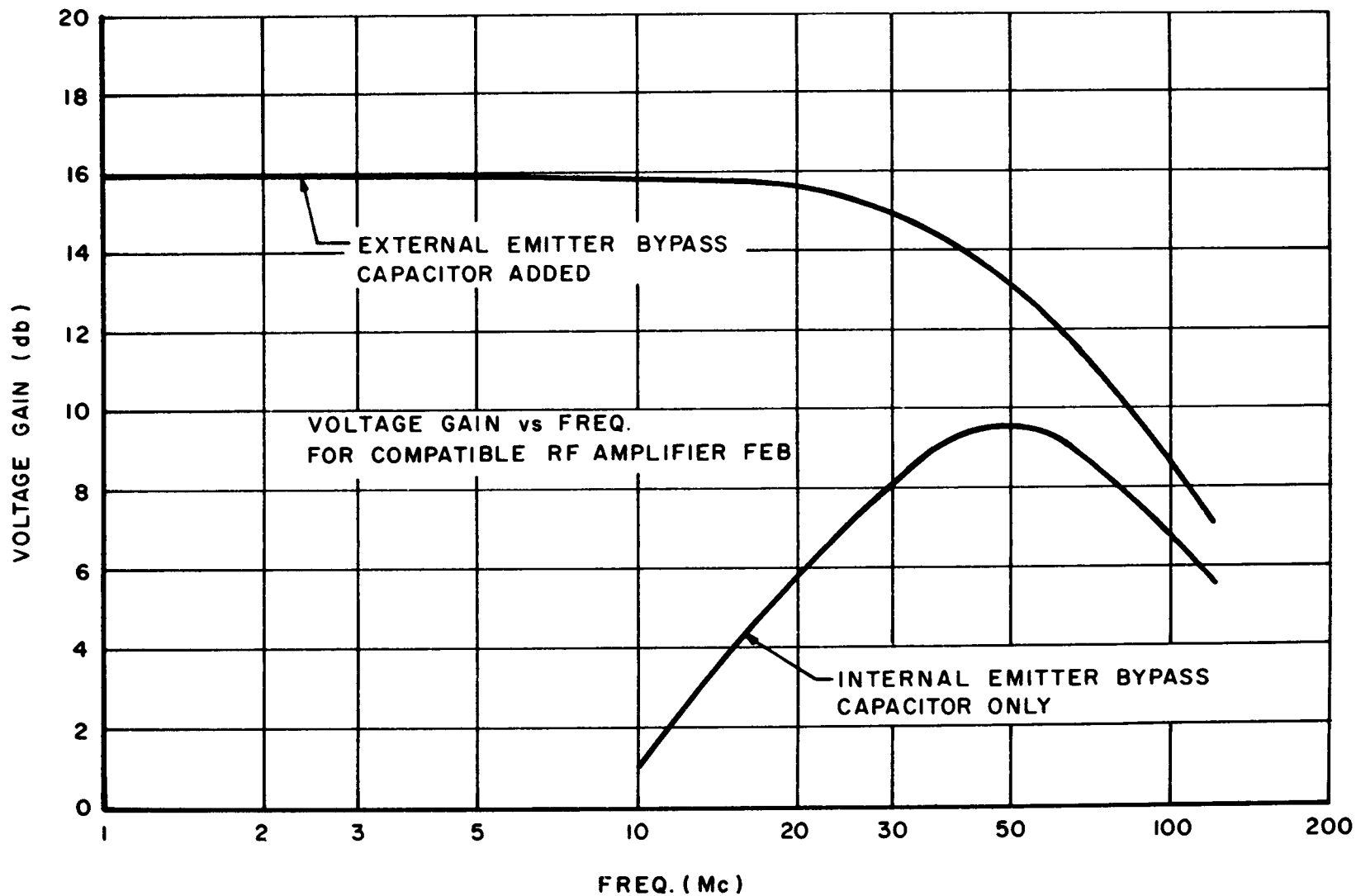

20
18
16
14
12
10
8
6
4
2
0
VOLTAGE GAIN (db)
EXTERNAL EMITTER BYPASS
CAPACITOR ADDED
VOLTAGE GAIN vs FREQ.
FOR COMPATIBLE RF AMPLIFIER FEB
INTERNAL EMITTER BYPASS
CAPACITOR ONLY
1
2
3
5
10
20
30
50
100
200
FREQ. (Mc)

FIGURE 43

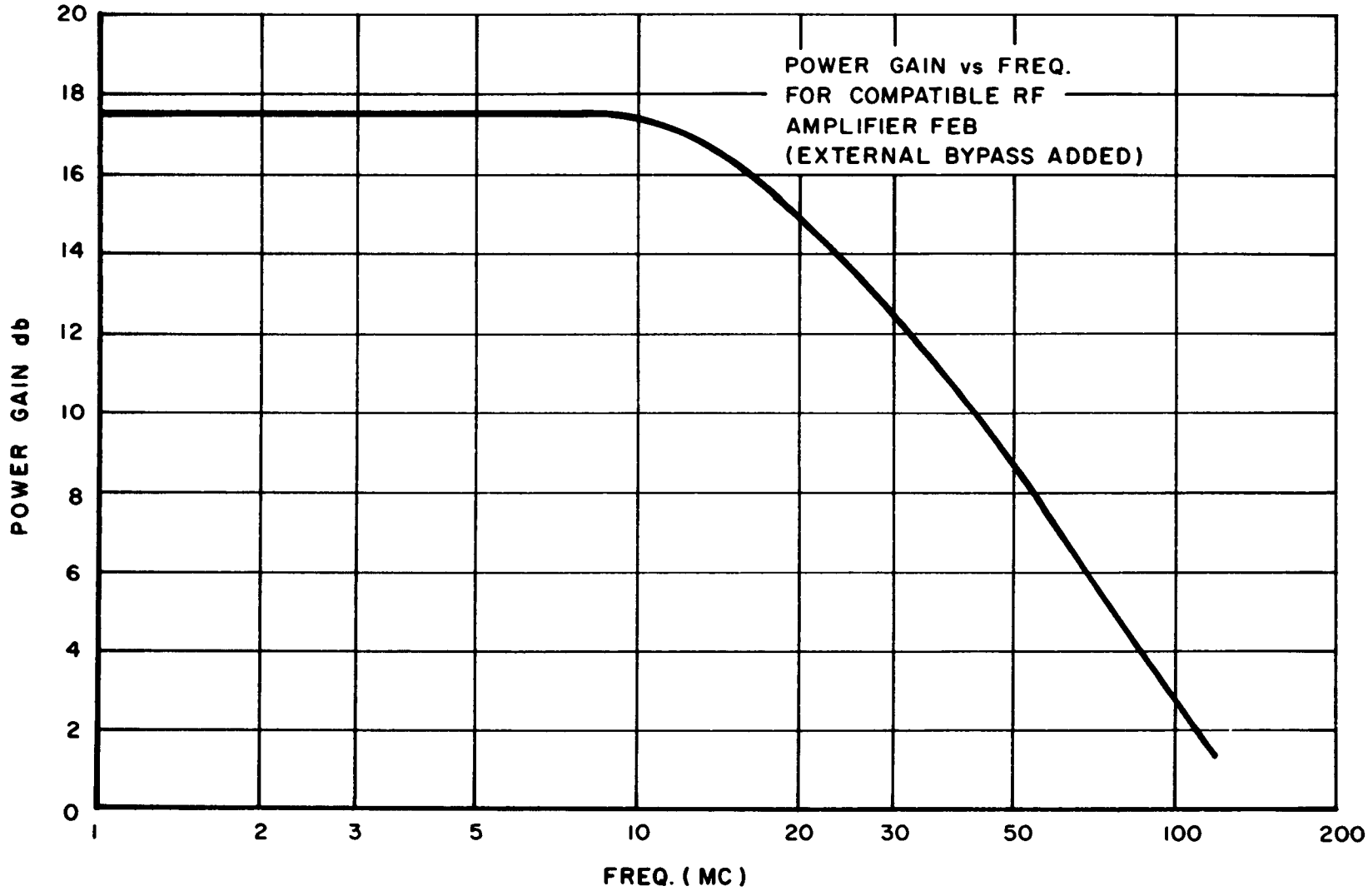
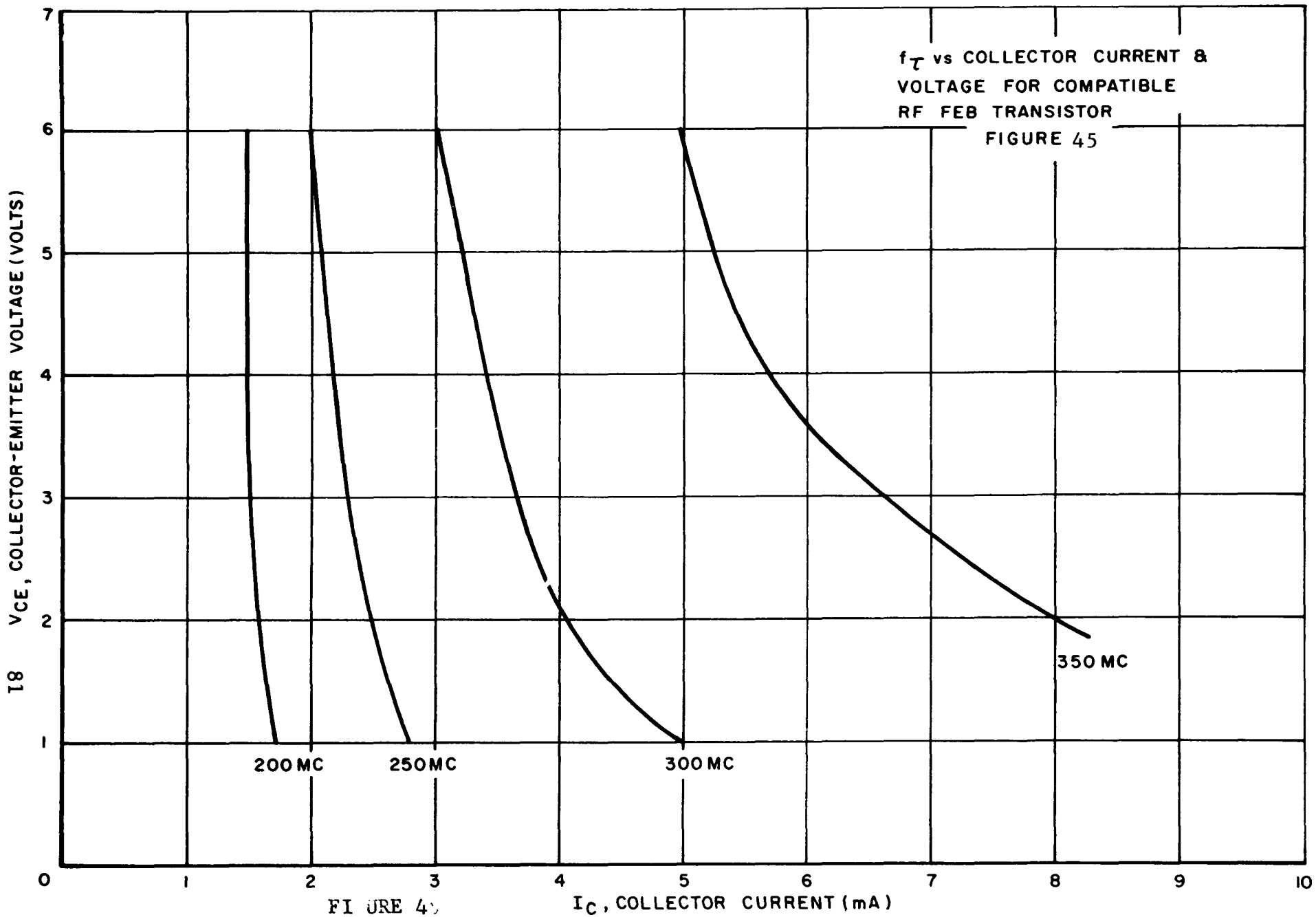

POWER GAIN vs FREQ.
FOR COMPATIBLE RF
AMPLIFIER FEB
(EXTERNAL BYPASS ADDED)
POWER GAIN db
20
18
16
14
12
10
8
6
4
2
0
1
2
3
5
10
20
30
50
100
200
FREQ. (MC)

FIGURE 44


f_τ vs COLLECTOR CURRENT & VOLTAGE FOR COMPATIBLE RF FEB TRANSISTOR
FIGURE 45
18 V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)
I_C, COLLECTOR CURRENT (mA)
200 MC
250 MC
300 MC
350 MC
0
1
2
3
4
5
6
7
8
9
10

FI URE 4

TABLE I

Effect of Buried Layer

	RF Transistor Without Buried Layer	RF Transistor With Buried Layer
BV_{CBO}	50 V	50 V
h_{FE} @ 2.5 V, 2.5 mA	40	40
@ 2.5 V, .05 mA	-	11
$V_{CE(sat)}$ @ 10 mA	600 Ω	80 Ω
f_T @ V_{CE} = 6V, I_C = 5 mA	-	335 Mc

(2) Evaluation of SiO_2 capacitors used in the RF amplifier.

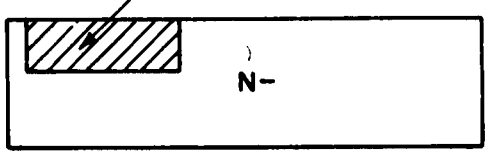
3.3.7.3 Transistor Development

The buried layer technique used in the RF transistor refers to the process whereby a highly doped layer is sandwiched or "buried" between the wafer and the epitaxial grown layer (Figure 46). During the subsequent heat cycles involved in the epi growth and the base and emitter diffusions, the impurities in the buried layer diffuse up in a pre-calculated manner to the neighborhood of the collector base junction.

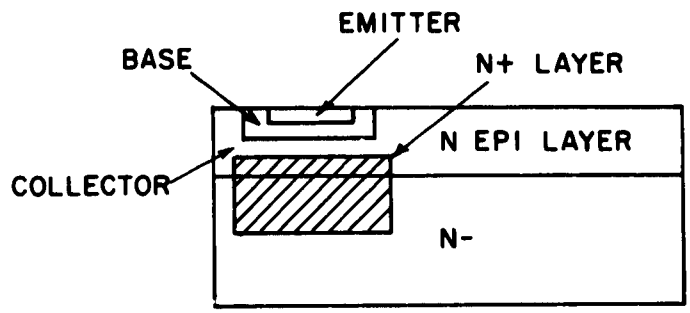
The effect of the buried layer is to improve the performance of the transistor by lowering the series resistance of the collector (R_{sc}). This reduction in R_{sc} is accomplished by the low resistivity material placed in the die near the collector by means of the buried layer. The reduction in R_{sc} is responsible for a better transistor performance for two reasons. First, R_{sc} is in series with the collector load resistor and the output power will be divided proportionally between them. Second, f_τ is directly related to $\frac{1}{R_{sc}}$; consequently, reducing the collector series resistor improves the high frequency capacilities of the FEB transistor.

3.3.7.4 Thin Film Capacitors

Another process which is receiving a large amount of effort is the SiO_2 capacitor formation. Capacitors have been successfully fabricated from SiO_2 dielectric films and are used currently in hybrid integrated circuits. But capacitors are the largest elements on a FEB and a reduction of capacitor size would



BURIED LAYER BEFORE
EPITAXIAL GROWTH



BURIED LAYER AFTER
TRANSISTOR FABRICATION

FIGURE 46

make possible more complicated circuits on the same die or more reliable circuits on a smaller die. In addition, the smaller a capacitor geometry, the higher the Q of the capacitor and the better its high frequency performance.

We are currently investigating the reproducibility of thin SiO_2 films in the 100 - 500 Å thickness region. The breakdown voltage of these films has been measured and determined to be approximately 70V for a 1000 Å film. If the SiO_2 growth process can be accurately controlled, it should be possible to achieve high value capacitances per unit area with films several hundred angstroms thick and a breakdown voltage greater than 10 V.

Data has been obtained on several types of FEB capacitors at 120 Mc. Table II lists typical results to date.

TABLE II

	Junction Capacitor	SiO_2 Capacitor With Emitter Diffusion (2.2 Ω/□) as Bottom Plate	SiO_2 Capacitor With Low Resistivity Material As The Bottom Plate
C_{pf}	50 pf	50	50
Q	1	3	10

4.0 AUDIO AMPLIFIER UTILIZED IN 120 Mc AM TRANSRECEIVER

Reference should be made to Figure 1 for a picture of a 100 mil by 100 mil die of a monolithic audio amplifier. Figure 2 shows a schematic of the circuit. The structure is an all diffused structure including the resistors.

Operable die have been produced. The voltage gains of 14 to 16.5 db and standby current drains of 8 to 14 milliamperes from a 12 V supply are essentially the same as those on a bread-board. These die will be scribed and bonded to headers and more complete measurements will then be taken.

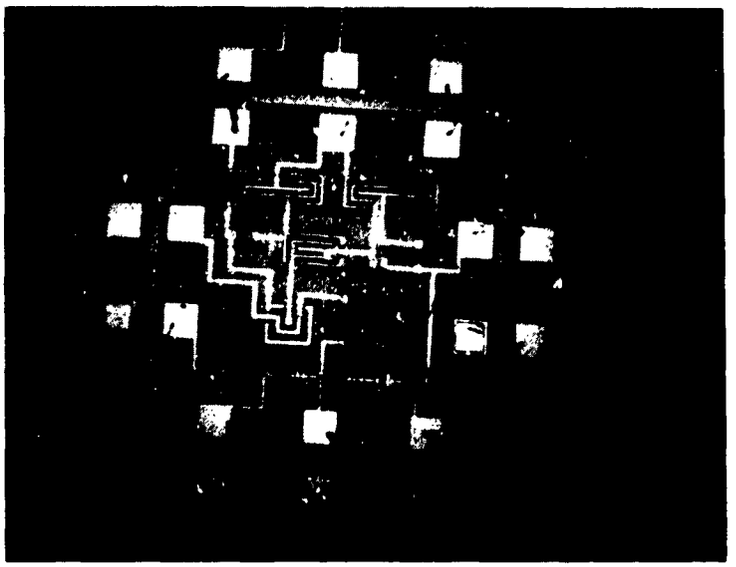
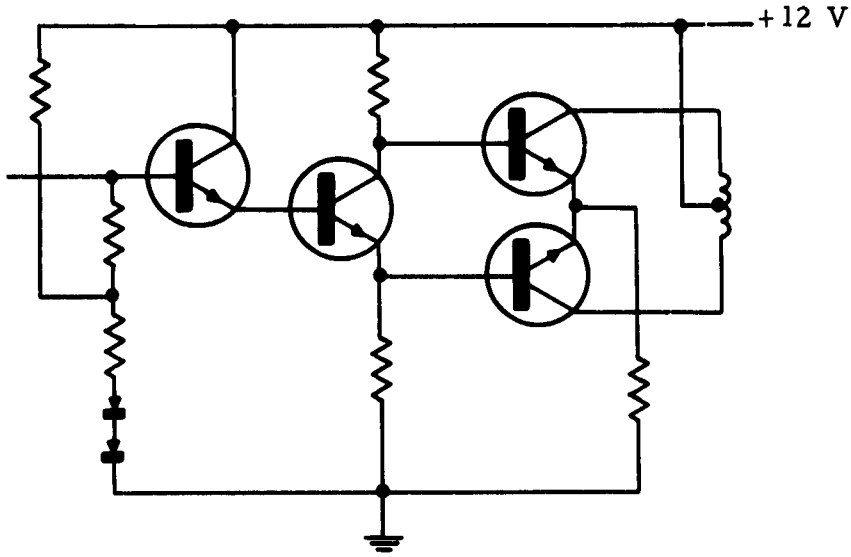
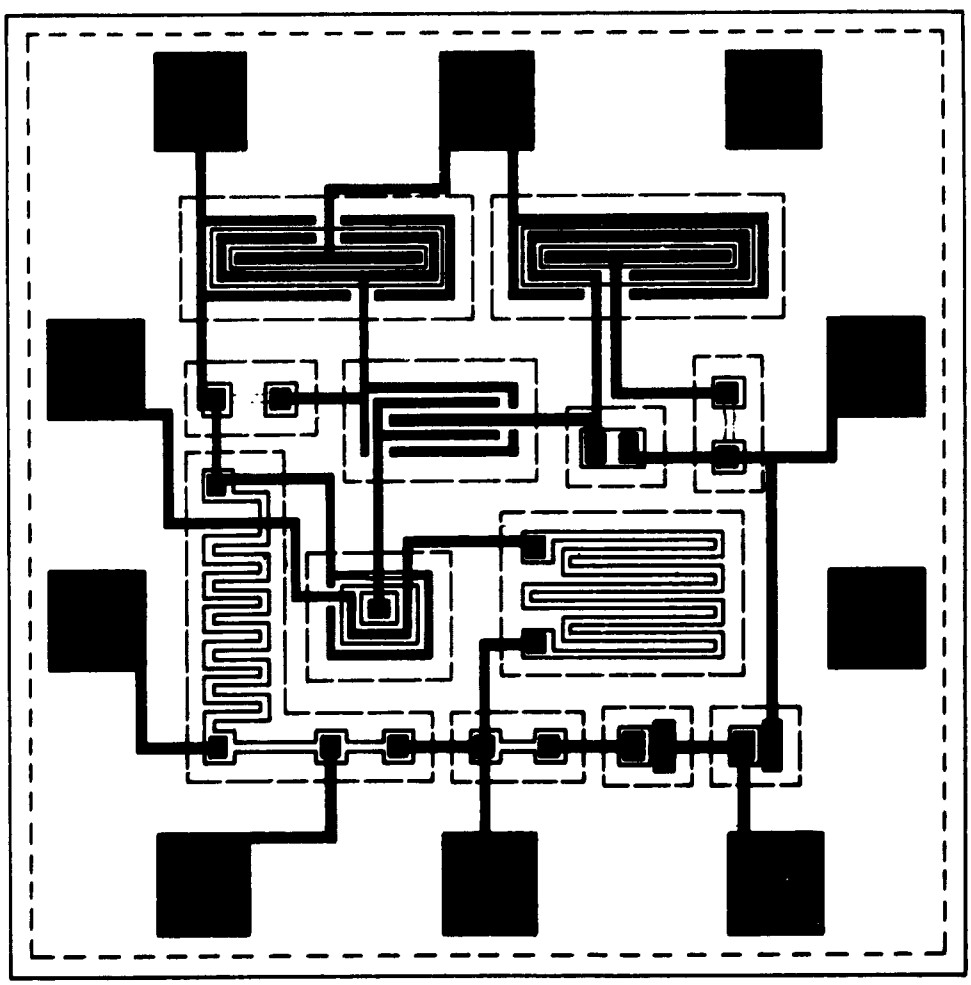


Figure 1

100 Mil by 100 Mil Die
of a
Monolithic Audio Amplifier



Audio Output Amplifier Schematic Diagram



Audio Amplifier Composite Mask Drawing

Figure 2

5.0 PNP-NPN MONOLITHIC INTEGRATED CIRCUIT TECHNOLOGY

5.1 Monolithic Gate Using PNP Transistors

Alternating NPN and PNP monolithic gates eliminates the need for level setting with emitter followers. Although fan-in, fan-out is reduced, the power reduction for use in low power, serial operation is substantial. In addition, the temperature tracking of the system improves.

Direct replacement of NPN transistors with PNP's in the monolithic system is possible. The major problem that is encountered is with diffusion control. Since the resistors are formed during the base diffusion, a very closely controlled N type, low concentration diffusion is needed.

Diffusion work has started using monolithic gate masks. Since both the diffusion process and the network must be developed, the first functional units will be available in two to three months.

5.2 Compatible PNP-NPN Structures

Direct coupling PNP and NPN differential amplifier stages increases temperature stability and circuit flexibility. Two problems encountered with monolithic FEB's using this structure are: switching characteristics from PNPN parasitic structures and performance trade offs which must be made in each transistor.

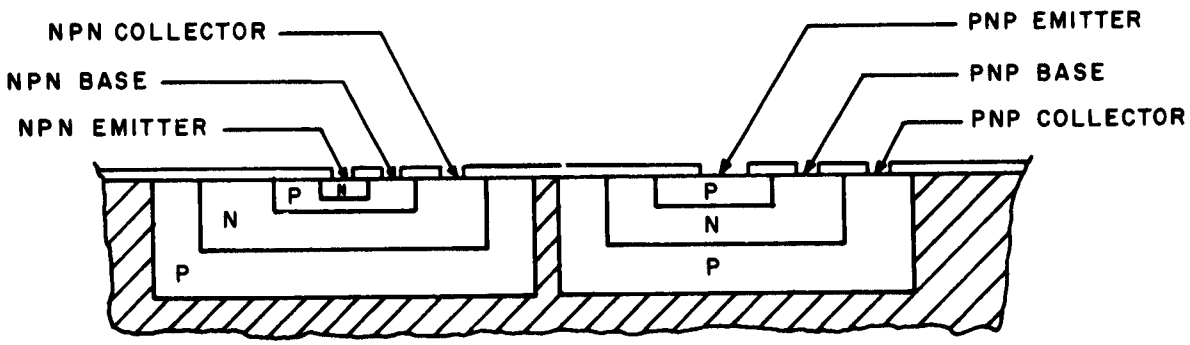
The basic FEB structure employing both PNP and NPN transistors is shown in Figure 1. A parasitic PNPN structure is formed between the PNP emitter and the N type substrate. For very

low PNP base currents, the BV_F of the parasitic PNPN approximates the BV_{CBO} of the PNP transistor. With characterization of the I_g (PNP base current) versus BV_F in the PNPN, a careful choice of bias current and collector voltage for the PNP circuit eliminates the undesirable switching mode.

Normally, both the PNP base and NPN collector regions are formed during the same diffusion. Both are then identical in both impurity concentration and penetration. During the next diffusion, the NPN base and the PNP emitter are made. In this structure, a trade off must be made between the PNP base width (wide base, low h_{FE}) and the NPN collector (narrow width high R_{cs}). One major advantage of this structure is that it requires only four diffusions.

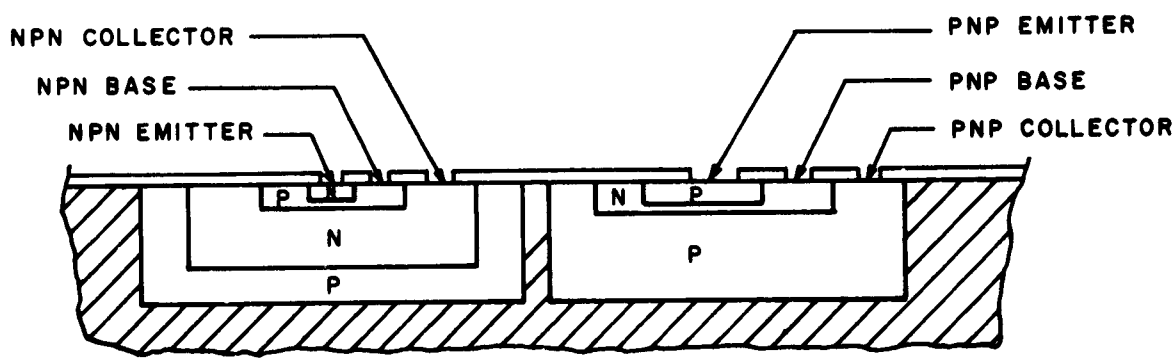
A slight modification of the PNP base-NPN collector diffusion improves the structure. A cross section of this is shown in Figure 2. No compromise is made between transistor characteristics.

A single ended operational amplifier as shown in Figure 3 will be used to develop this structure. Monolithic design of this circuit uses available compatible techniques including thin film resistors. Preliminary performance specifications are given in Table 1. Complete mask set drawings have been made and are being processed.



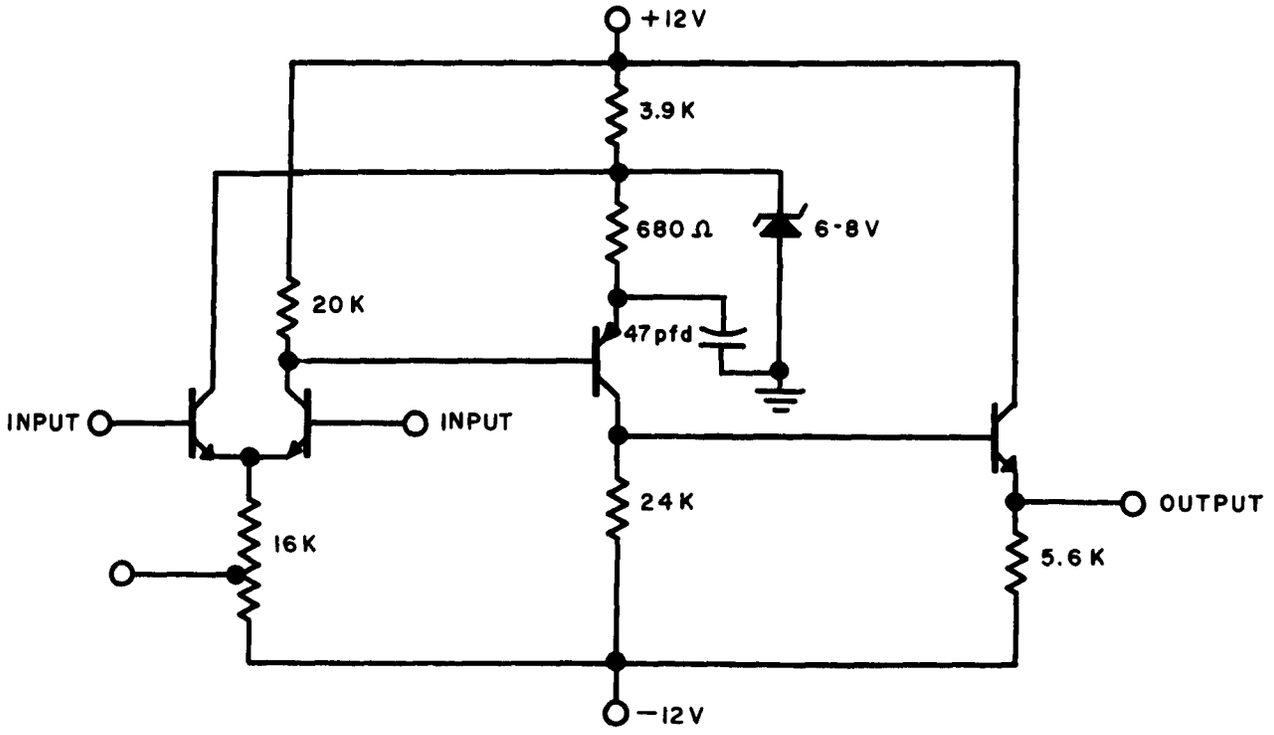
FEB STRUCTURE USING COMPATIBLE PNP-NPN TRANSISTORS

FIGURE 1



IMPROVED PNP-NPN STRUCTURE

FIGURE 2



SINGLE ENDED OPERATIONAL AMPLIFIER

FIGURE 3

OPEN LOOP GAIN: 1000 Minimum

MAXIMUM OUTPUT: ± 5 Volts into 10K

BANDWIDTH: Open Loop 65 Kc
Gain-Bandwidth 6.5 Mc

GAIN LINEARITY: 2% to ± 5 Volts Output

MAXIMUM LOAD CAPACITANCE: 150 Picofarads

MAXIMUM DC OFFSET: Dependent on Power Supply Tolerance
(Design Goal 3 mv at 0% Tolerance)

POWER DRAIN: 87 mW

TABLE 1

Single Ended Operational Amplifier Performance Specifications

6.0 FLAT PACKAGE DEVELOPMENT

Early flat package developmental work was initiated to prove feasibility of design and associated processes. Two areas of major effort were the package construction and direct bond of the feed-through to the Al metallization of the silicon die.

An early start in the process of bonding Al plated Kovar to the Al metallization of the die was accomplished in the TO-5 10-pin package using a Kovar pinwheel contact frame. One hundred thermal compression bonds were made and sent to the quality control lab for evaluation. A temperature step stress test for 24 hours each at 125°C, 200°C, 250°C, 275°C, 300°C and 325°C was completed first. Changes of 0.5Ω and 0.6Ω resistance in two bonds were detected. Other tests included the Mil standard in temperature cycling, shock, vibration fatigue, vibration, variable frequency and constant acceleration. One bond opened during this test (the bond that had a 0.6Ω resistance increase as a result of the temperature step stress test). Early flat package finger bonds are presently being evaluated.

Early evaluation of the flat package has shown a package weakness. During the 100 pounds psi pressure test of the assembled package, the hermetic seal was often broken. Analysis indicated that the 9010 glass side frame and the .010 inch alumina bottom and top cover to the package would often fracture. Maximum safe pressure of the above mentioned package was 60 pounds psi.

Two minor changes have been made to correct this. The side frame has been changed from 9010 glass to alumina. The .010 inch thick alumina bottom and cover has been changed to .020 thick.

A new piece part has been designed, as shown in Figure 1, that incorporates the existing side frame and bottom into one piece part. This box type structure can also be used for the sides and cover as one approach to the hybrid flat package.

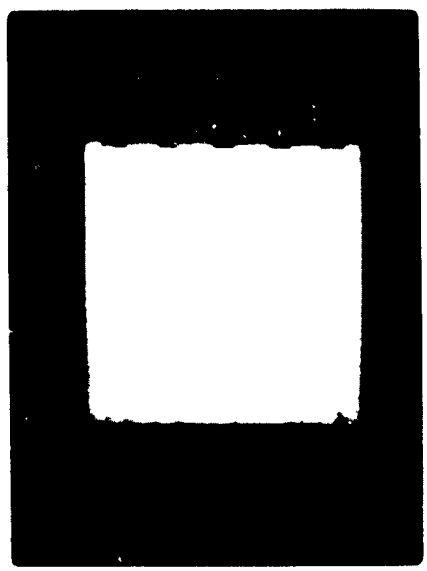


Figure 1

Flat Package Piece Part

7.0 VHF TRANSRECEIVER CIRCUIT DESIGN AND EVALUATION

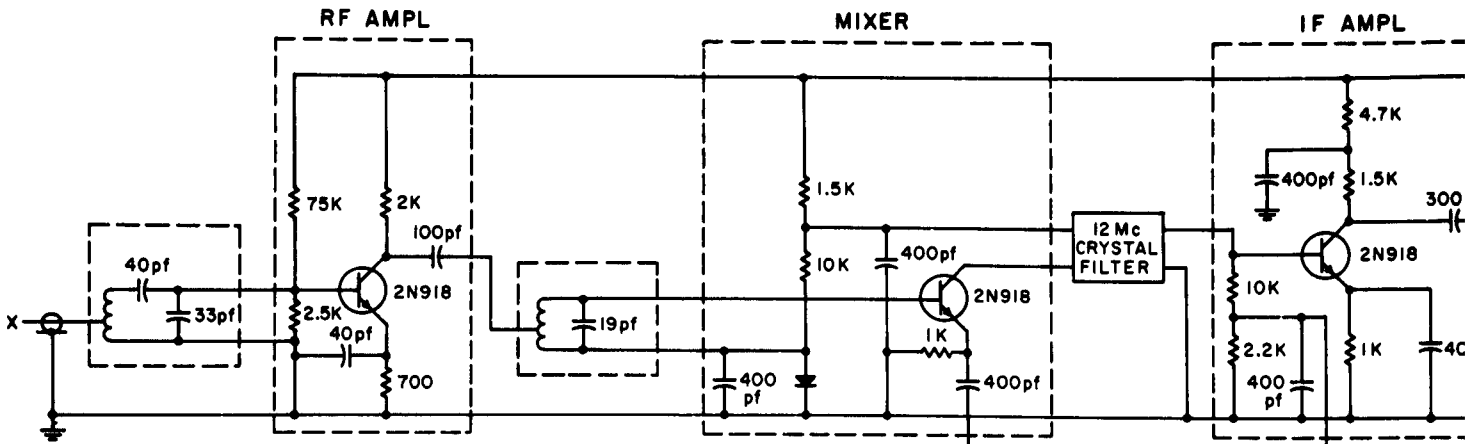
7.1 Introduction

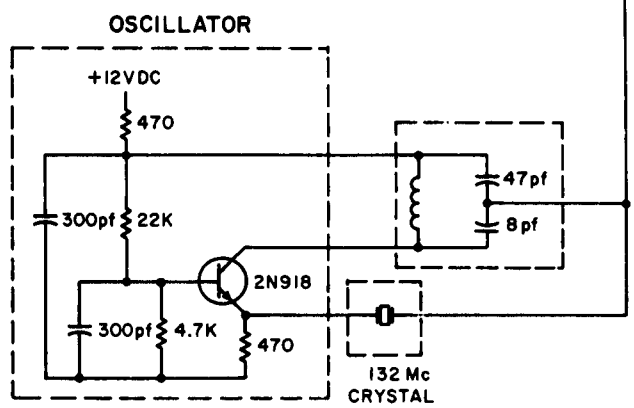
Some significant changes have been made in the design of both the receiver and the transmitter. In both cases, the design change will make the circuit more adaptable to integrated circuit design. The transmitter design change will make the transmitter performance more immune to component tolerance. The receiver design change will make the circuit less complex.

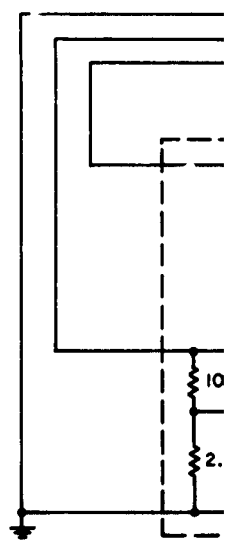
7.2 Transmitter Design

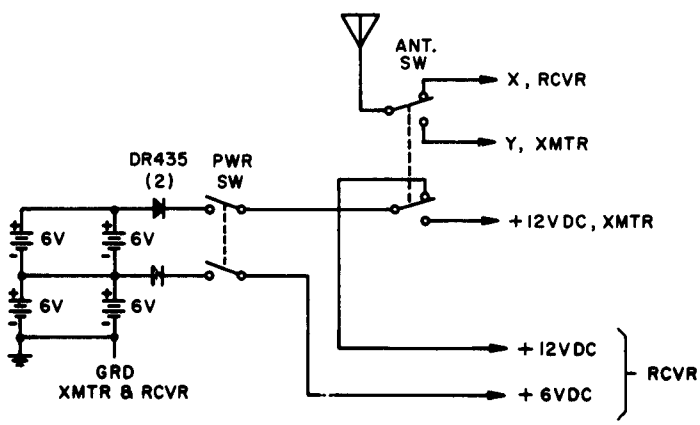
The transmitter schematic is shown in Figure 1. Figures 2 and 3 illustrate packaging design and TO-5 can configuration. As one can readily see, the transmitter is made up of conventional oscillator, driver and output stages. Stability is achieved by limiting in the driver and output stages. The degree of limiting determines the amount of insensitivity the output has to gain variations. These gain variations may be caused by malfunctioning parts, voltage variations, temperature variations and loose component tolerances.

Modulation is achieved by collector modulating the final transistor. This type of modulation does not require the amount of gain and, therefore, the linearity of the circuits to be controlled. Modulation is achieved by varying the voltage on the collector of the final transistor. This transistor, when operating properly, will be saturation limited. The power output will, therefore, be equal to the square of the RMS voltage divided by the load resistance.

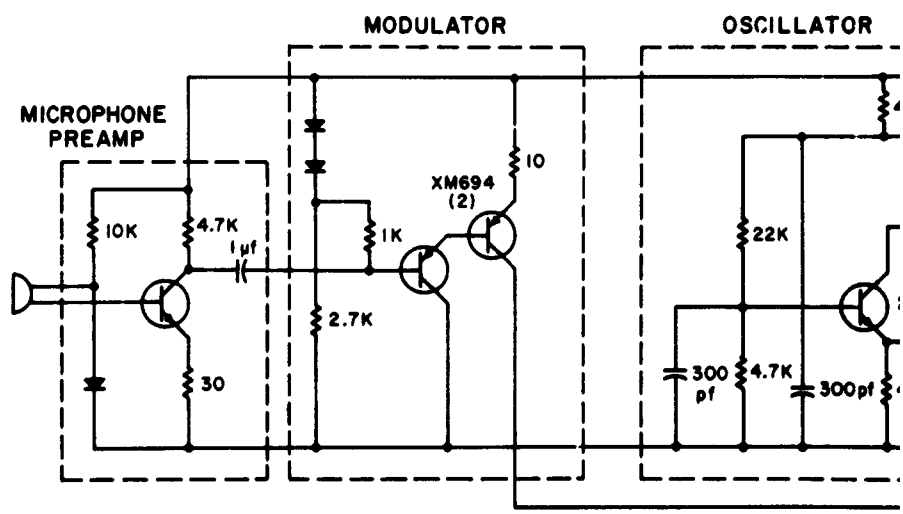


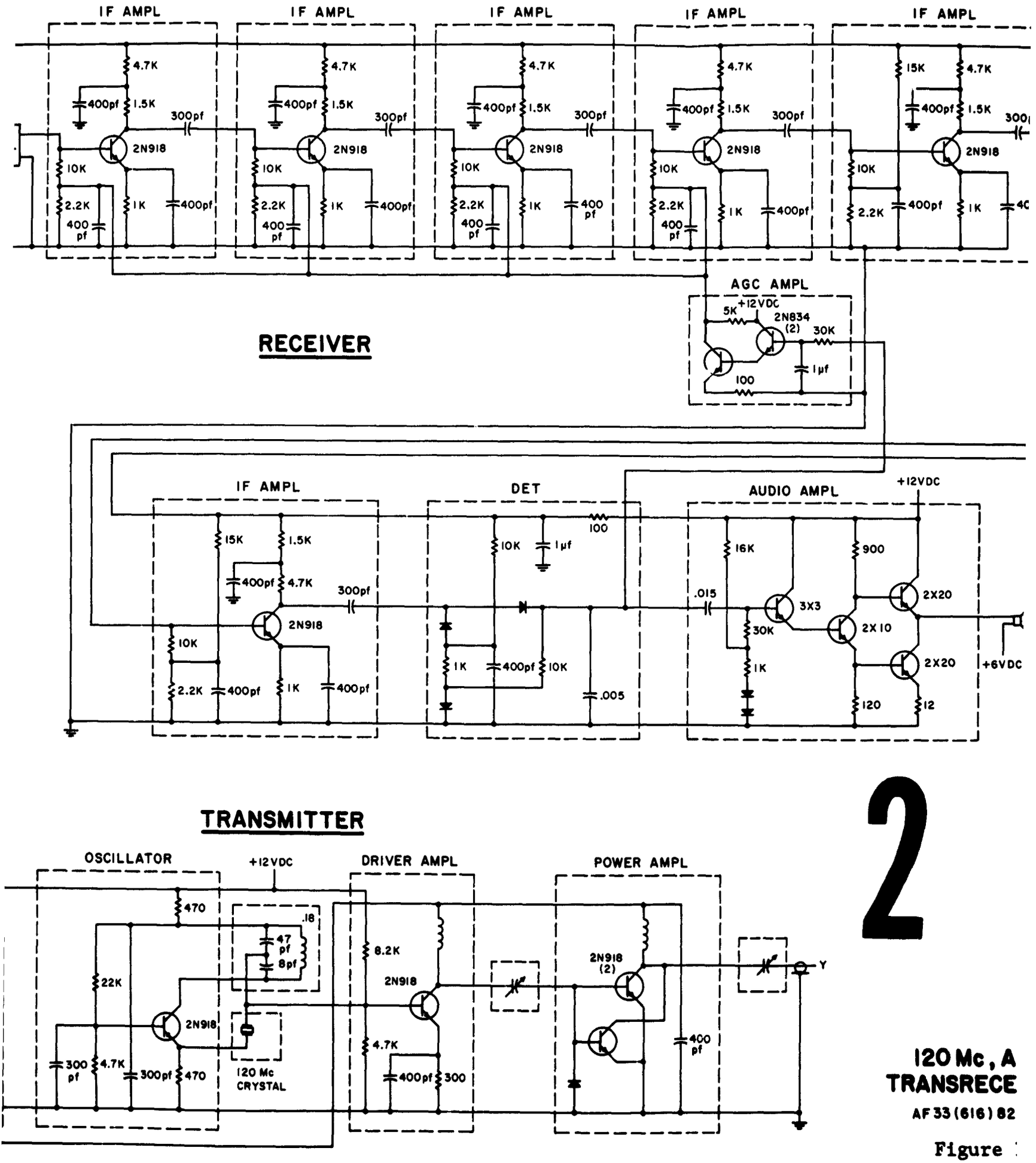






SWITCHING DIAGRAM



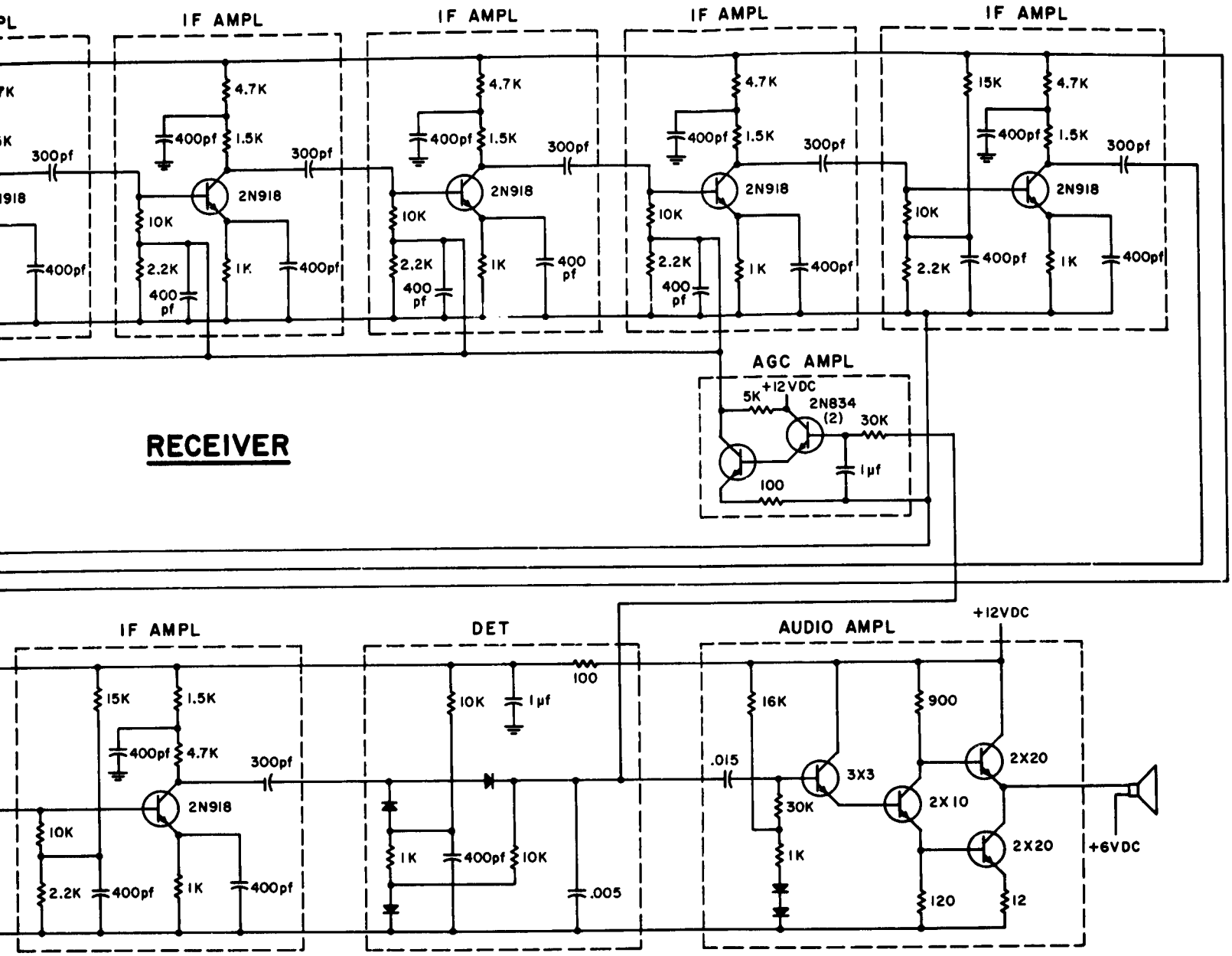


2

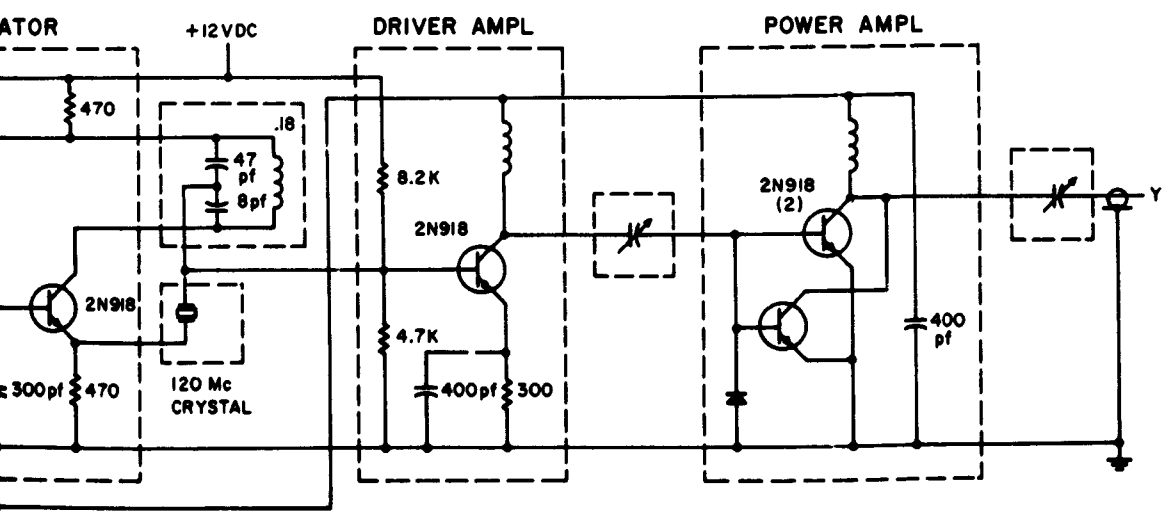
120 Mc, A
TRANSRECE

AF 33(616)82

Figure



TRANSMITTER



3

120 Mc, AM TRANSRECEIVER

AF 33(616)8276

Figure 1

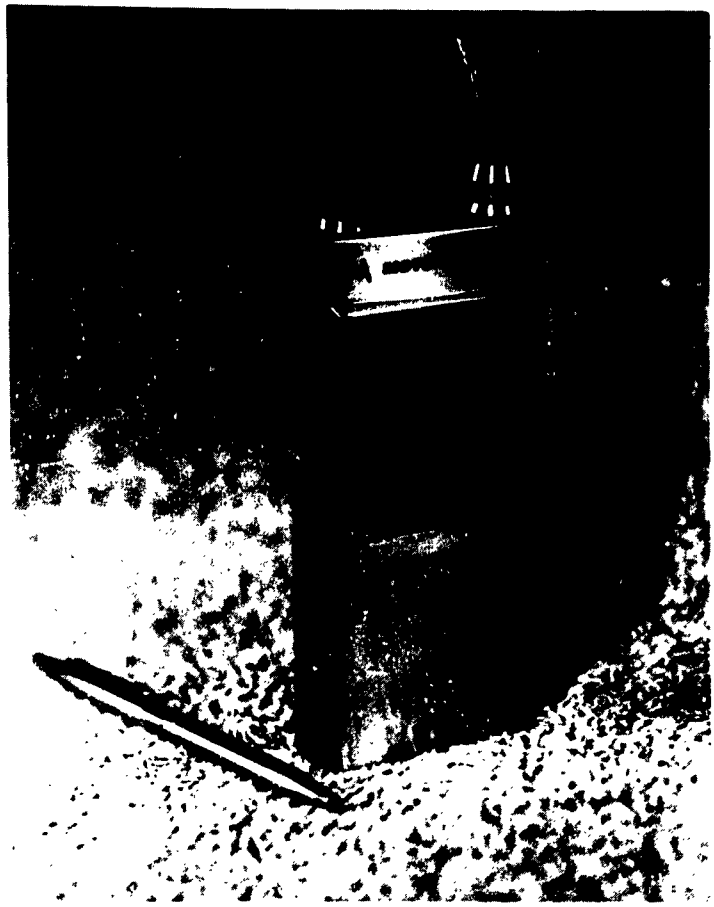


Figure 2

Model II Transreceiver

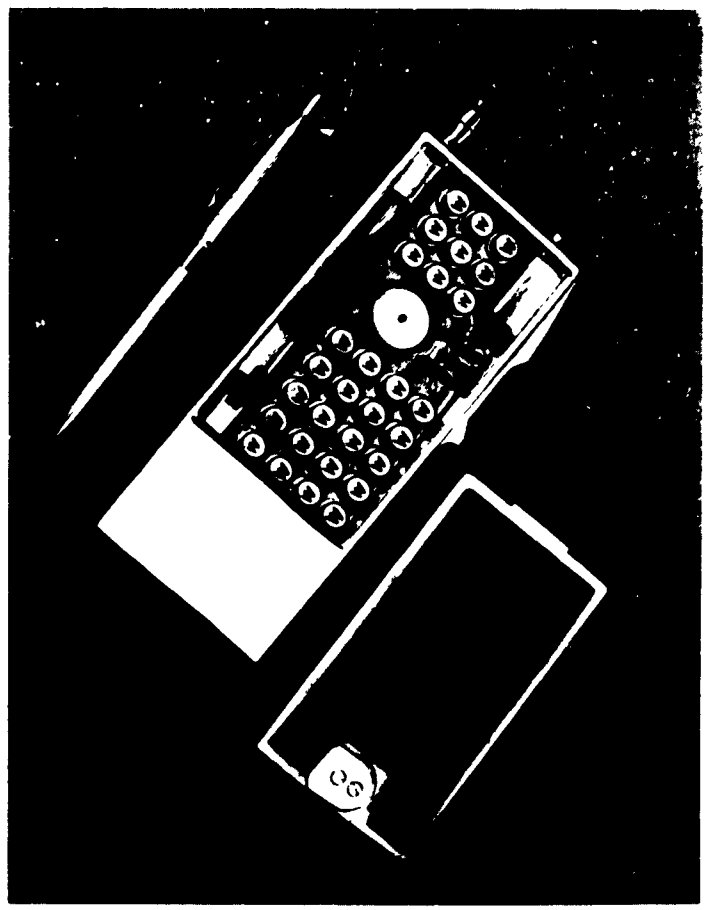


Figure 3

Model II Transreceiver

The voltage on the collector of the transistor is controlled by the modulation transistor. In a quiescent unmodulated condition, the collector voltage on the output transistor is adjusted to be one-half the supply voltage. The other half of the voltage is dropped across the modulation transistor. When the transmitter is modulated, the voltage across the modulation transistor drops to $V_{CE(sat)}$, thereby supplying almost the full supply voltage to the output transistor. Since the supply voltage is twice the quiescent or unmodulated collector voltage of the output transistor and the power goes up as the square of the collector voltage, the peak power will be four times as great as the unmodulated power. During the other half cycle of the modulation swing, the power will in a like manner drop to zero. The average modulated power will be 50% greater than the unmodulated power as is the case with all true amplitude modulated transmitters.

The only critical feature in the entire transmitter is the collector voltage of the modulation transistor. The degeneration ten ohm emitter resistor has been added to minimize the effect of Beta variations and the two forward biased diodes have been added to compensate for V_{BE} changes with temperature. This stabilization has proved so successful that a variation of less than one decibel in power out is realized. No noticable change in percent modulation was observed in a breadboard model from -25°C to +100°C.

A power output of 60 milliwatts unmodulated or 90 milliwatts modulated (240 milliwatts peak) power output is expected.

The principal change in the receiver design is in the IF section. The design has been changed to incorporate RC coupled

common emitter stages instead of the MECA amplifier stages. The MECA amplifier was first proposed because the high input and output impedances caused by the common collector input and the common base output and the small reverse feedback voltage by calculation would give the highest gain and best performance. It has in fact been demonstrated that the MECA amplifier made with discrete components has many desirable features when used as low frequency or medium frequency RC or tuned amplifiers, or high frequency tuned amplifiers. The monolithic MECA amplifiers at medium and high frequencies lose much of their advantage, however, when used with RC coupling because of ~ 7 pf parasitic capacitor between the collector of the output transistor and ground. The impedance of this capacitor (approximately 2K at 12 Mc) reduces the output impedances of the MECA amplifier, thereby causing mismatching and loss of gain. Motorola has, therefore, changed to the lower impedance common emitter stages for the RC coupled IF strip in the transceiver.

7.3 Status of Transmitter

The breadboard of the transmitter has been completed. Most of the ceramics for the hybrid circuits have been metallized. These ceramics and the remainder that will be made shortly, will be ready for fabrication of the hybrid integrated circuits.

7.4 Status of Receiver

The entire receiver is being fabricated first with hybrid integrated circuits with the possible exception of the RF stage and the audio amplifier stage. The effort to finalize the layout of the receiver is temporarily delayed by the 12 Mc crystal filter. The filter presently used in the breadboard has a higher insertion

loss than the filter that will be used in the final models. The high insertion loss of the present filter necessitates moving an IF amplifier in front of the filter in order that the noise figure of the receiver be determined by the RF amplifier instead of the first IF stage. The lower insertion loss filter should enable the entire IF strip to be placed behind the filter.

Work is also being done to fabricate all stages either in hydrid form or monolithic form as quickly as possible in order to find any problems that there might be in the printed circuit board layout. Presently, the IF circuits are being made in hybrid form. The remainder of the circuits have been laid out and ceramics have been metallized.

7.5 Forecast

After all circuits have been fabricated and connected together on the printed circuit board, the monolithic circuits will be substituted in as they are processed.

As reported elsewhere in this report, the RF amplifier and audio amplifier have already been processed with some degree of success. These will be improved upon in future models as soon as the analysis of these current units are studied in detail.

The next monolithic block to be started in the immediate future is the IF amplifier.

A monolithic IF amplifier, RF amplifier and audio amplifier will make the majority of the receiver monolithic blocks. The remainder of the stages will, however, be considered for

monolithic blocks. The mixer amplifier is a likely candidate because of its similarity to the IF stages. The AGC amplifier detector and oscillator also should not be too difficult.

8.0 DIGITAL COMMUNICATIONS SYSTEM

8.1 Research Test Vehicle

8.1.1 Summary

a) Testing of MECL circuits for use in the DCS breadboard has been completed and the fabrication of the breadboard has started using MECL gates available.

b) The A to D converter configuration using successive approximations with current reference sources has been selected for this system.

c) The preliminary mask design of the resistor summing network in the A to D converter has been completed for single chip fabrication.

d) The mask layout of a tapped differential amplifier has been completed. This is a preliminary building block design and is to be fabricated on a single chip.

8.1.2 MECL Testing

A test specification to provide a criteria for compatible MECL circuit to circuit operation in the DCS breadboard system was completed. The specification included tests on:

a) Input characteristics (loading at logic "1" and "0")
b) Transfer characteristics (logic levels & noise margin)
c) Output characteristics (loading at logic "1" or "0")
d) Speed (average propagation time)

The single chip MECL five input gate No. 2671 was selected for fabrication and the resulting units tested to this criteria.

8.1.3 Breadboard Fabrication

Twenty-six MECL gates were used in the construction of the Program Counter portion of the Transmitter. This circuit has been tested and functioned satisfactorily in every respect.

The next planned construction will be the two phase clock driver, PN Generator, Decoder, A to D converter and Multiplexer.

8.1.4 Digitizer Configuration

Considerable effort has been spent in arriving at an A to D converter configuration which will be compatible with the state of the art in integrated circuit technology. Figure 1 illustrates the selected configuration.

8.1.4.1 Choice of Analog to Digital Conversion Technique

The purpose of the Digital Communications System is to demonstrate integrated circuits and apply them in a working system. Therefore, the first consideration in designing the A to D portion of the system was based primarily upon ease of implementation by integrated circuits and performance compatible with the system performance requirements. The next consideration was that the encoder have the fastest conversion time possible for the bandwidth capabilities of the circuitry.

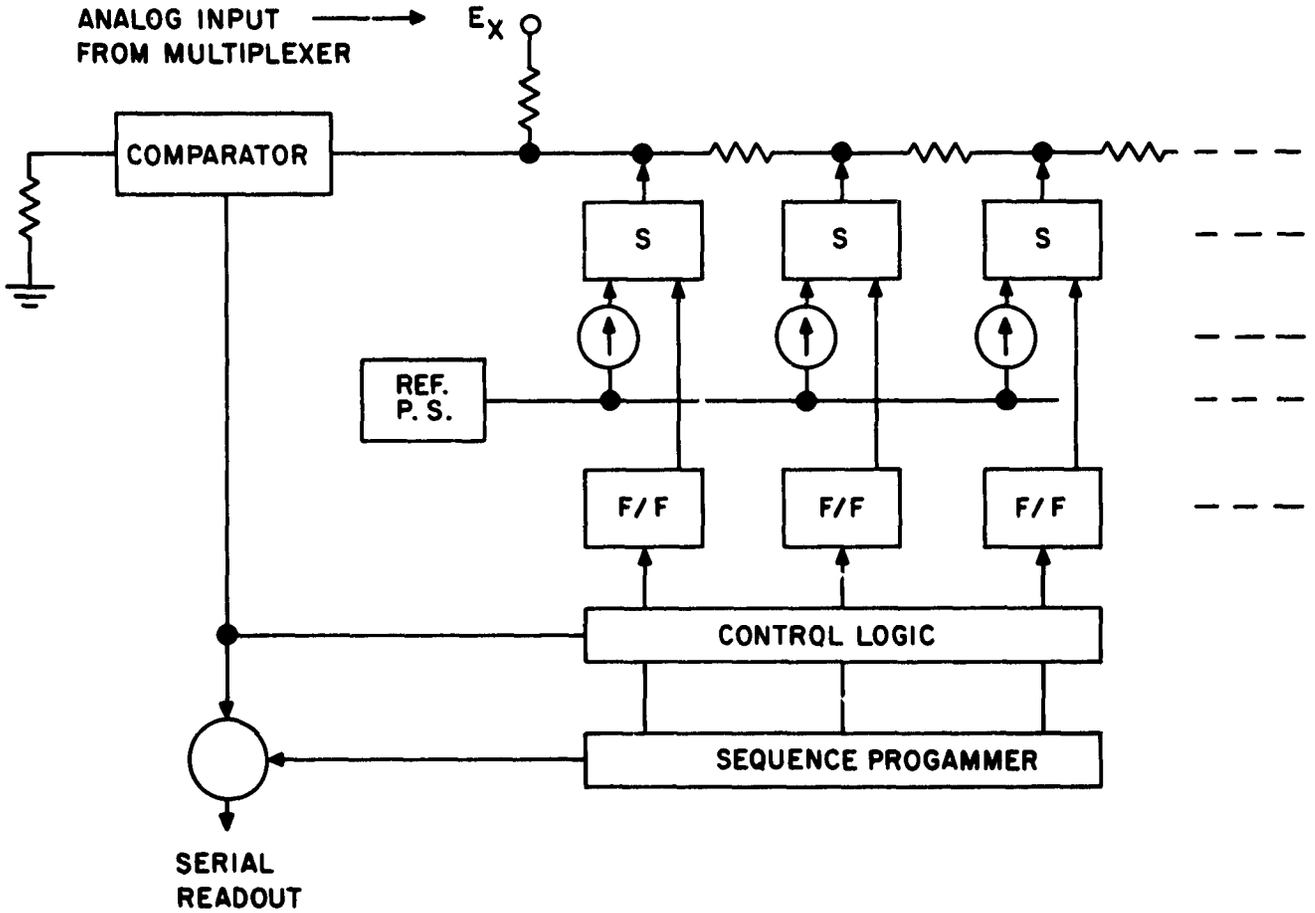


FIGURE 1

A TO D CONVERTER

The approaches[1] considered were (1) time base encoding, (2) coding by cascaded stages, (3) successive approximation encoding.

Time base encodings are immediately ruled out because they require excessive bandwidths. To encode a full scale voltage requires that the circuits have a bandwidth $2^n/n$ times larger than that required by the most efficient successive approximation which will encode a bit in one bit time.

Coding by cascaded stages is also ruled out on this program because of the stringent requirements on drift and gain stability of the amplifier stages. The MSB amplifier must be very stable with the stability requirements decreasing for succeeding stages.

Another type of encoder, the Capcoder[2], which is a version of successive approximation encoding, was also considered. This approach was also rejected because: (1) The amplifiers must have high input impedance, low output impedance, and a high degree of both gain and drift stability. The combination of all of these characteristics make the amplifiers very difficult to implement. (2) The encoder also requires capacitors which must be precise in ratio and have linear charge-voltage characteristics. (3) The switches used to transfer charge from one capacitor to another must maintain both voltage and current integrity. These characteristics are not compatible in switch construction.

---

1 Notes on Analog-Digital Conversion Techniques Edited by Alfred K. Susskind, Technology Press.

2 Development of 10 Bit Airborne Analog to Digital Converter. Prepared under Navy, Bureau of Naval Weapons, Contract No. 60-0256-C, Towson Laboratories Inc., ASTIA No. AD 259-561.

The encoding technique that was selected is a successive approximation current summing approach with the configuration shown in Figure 2. This configuration uses the fastest conversion technique known at this time without utilizing an excessive amount of hardware. The comparator has the same drift requirements as the other schemes but does not have critical gain or input impedance specifications. There are no critical gain, high input impedance amplifiers.

The greatest advantage this approach has over a voltage summing technique is that by making each current source independent and adjustable, it is possible to use a ladder network that has a very loose accuracy compared with the over-all A/D accuracy. The only real effect of the ladder network is to allow all current sources to operate at approximately the same current level, instead of being binarilly related. Thus, all current sources will be identical in every respect. The only stringent parameter associated with the ladder network is that the ratios of the resistors track with temperature.

Another important advantage is that the switches required do not have to have a low impedance. The switch in fact, will have a very simple configuration, as in Figure 3.

The only requirements of the switch are that it have high speed capabilities and low leakage. Both these requirements are compatible in a diode. Since this switch arrangement does not turn the current source off and on, but only steers the current, it induces a minimum transient into the current source, thus, minimizing transient recovery requirements. In voltage summing, the switch that has the function of switching the ladder leg to

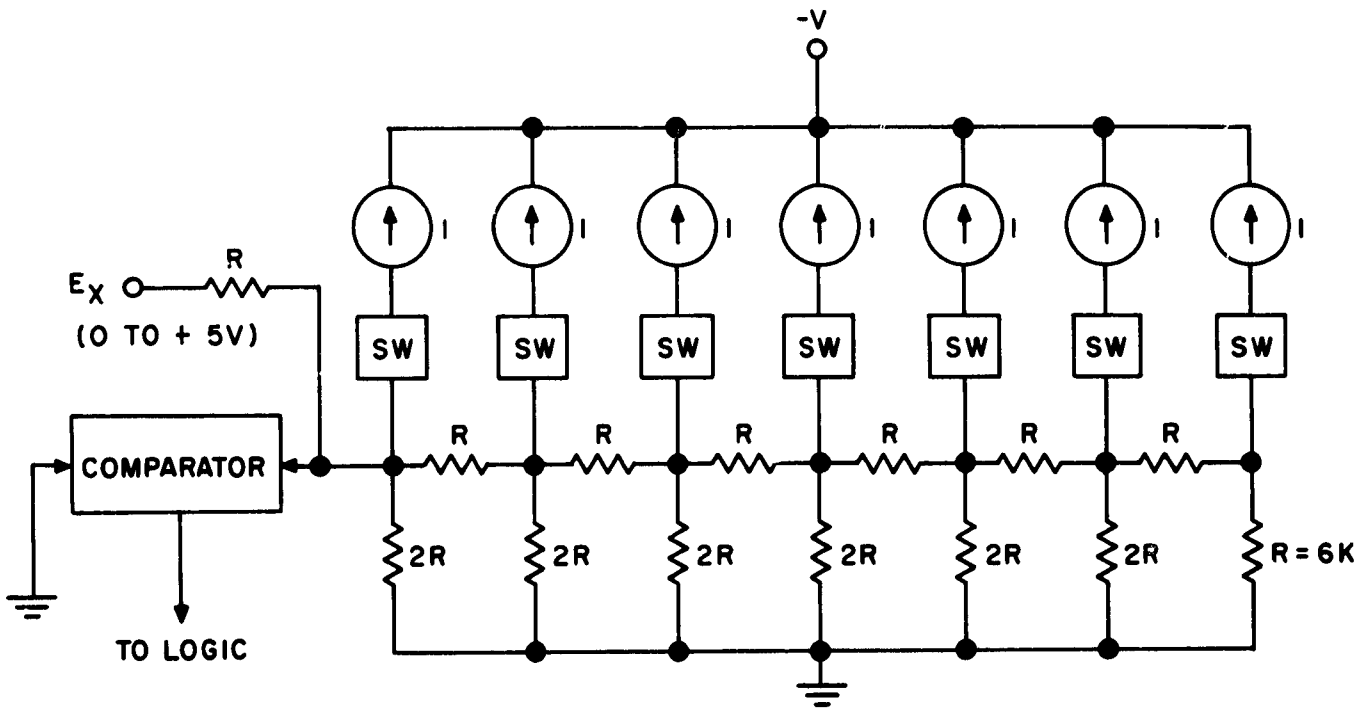


FIGURE 2

SUCCESSIVE APPROXIMATION CURRENT SUMMING CONFIGURATION

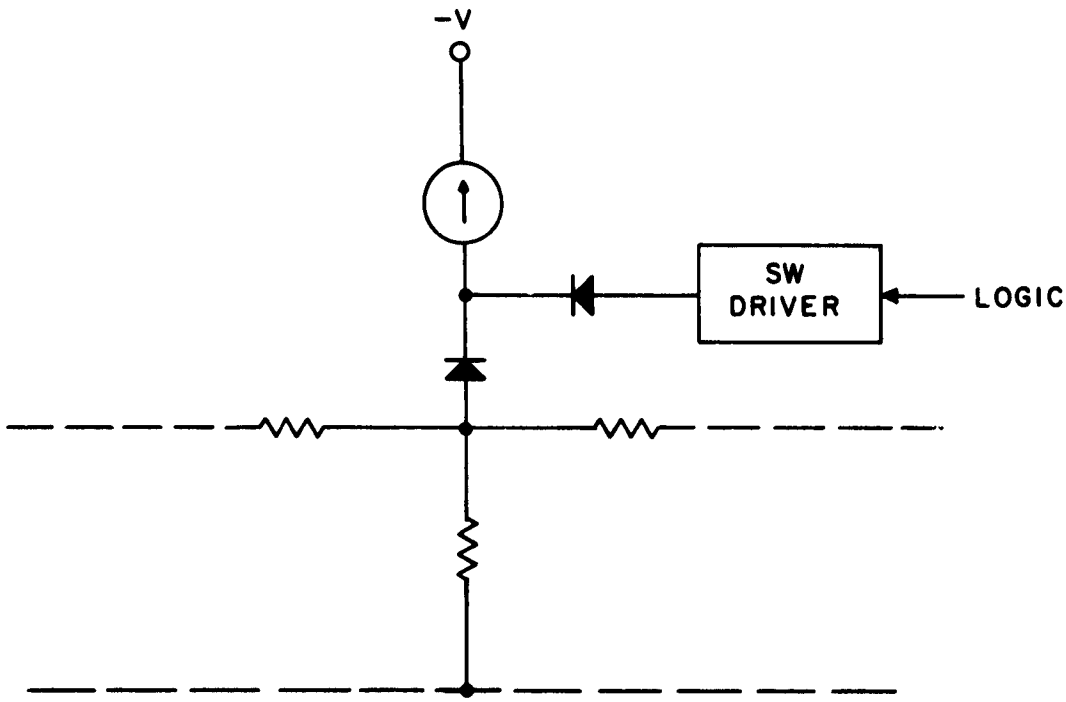


FIGURE 3

SWITCH FOR CURRENT SUMMING

ground or the reference voltage, Figure 4, is actually two switches, both of which must have low on resistance.

Thus, the switch requirements for voltage summing demand a much higher quality switch and twice the number that are required for current summing. If a scheme of independently adjustable voltage references were used to allow the ladder tolerance to be greater, this would put an additional requirement on the switches that they all be very closely matched with respect to the on impedance.

The summing approach was chosen over the straight comparison scheme because it has the advantage of using a limited input range comparator, thus, eliminating the common mode rejection requirement for the comparator amplifier.

The current source configuration, Figure 5, employs a field effect transistor for the current control. The FET is used, instead of a bipolar transistor, to eliminate the error induced into the output current due to the change in beta and base current with temperature.

The current source has been breadboarded, using conventional components, and tested with the following results: 1) Output impedance approximately 50 megohms, 2) Stability with temperature (0 to 50°C) at .5ma output current is $\pm$0.25%. The switches, amplifiers and resistor network have been investigated to a degree which confirms the fact that it is feasible to implement this approach to A to D conversion.

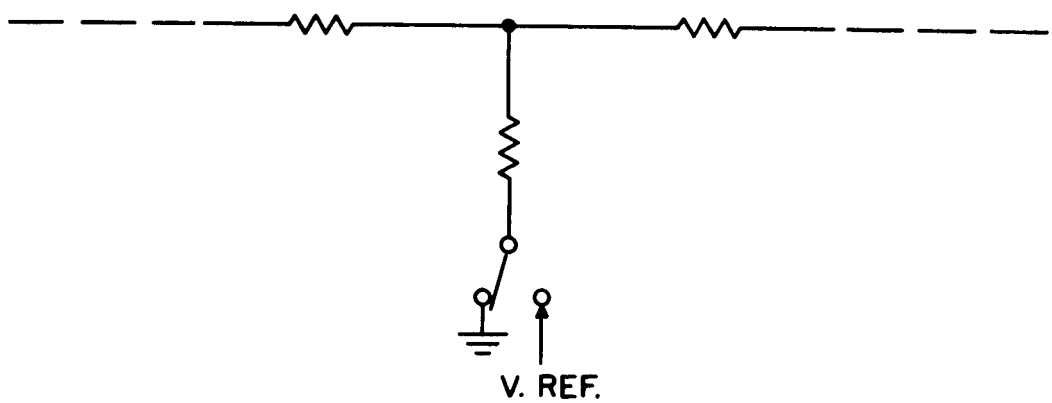


FIGURE 4

SWITCH FOR VOLTAGE SUMMING

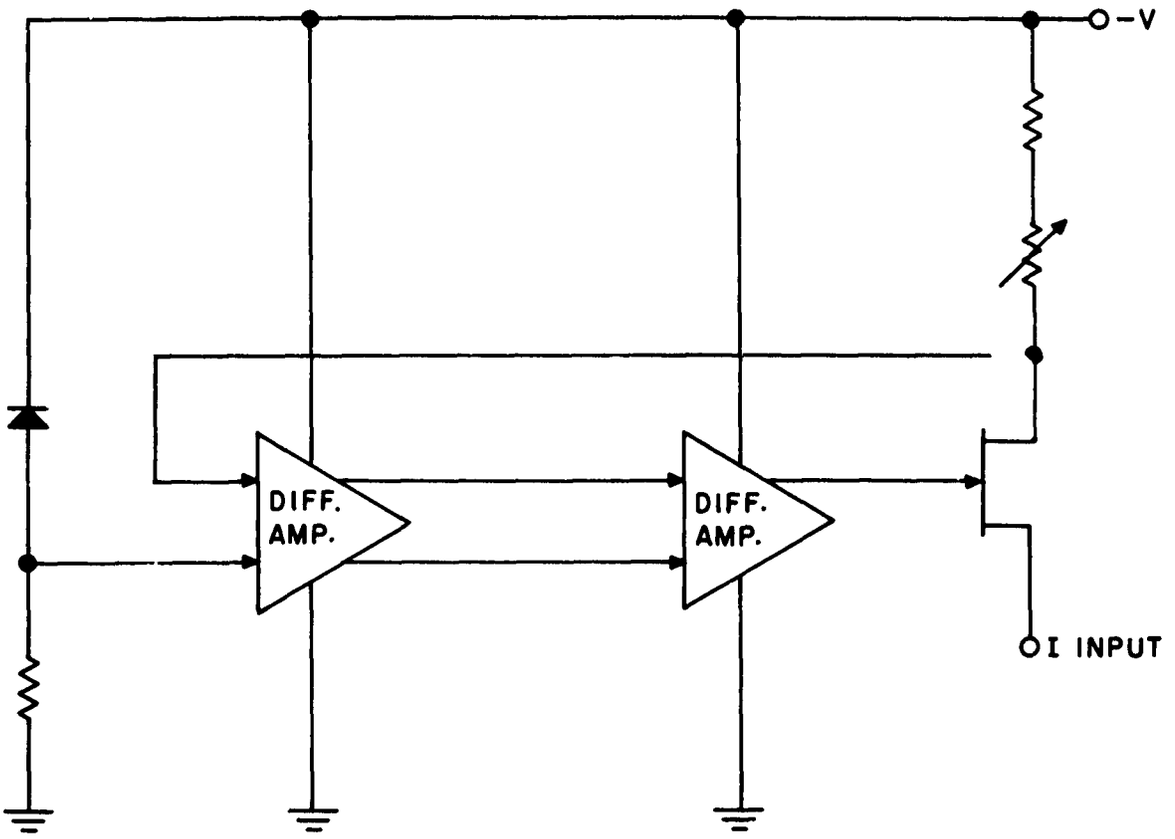


FIGURE 5

CURRENT SOURCE CONFIGURATION

This approach offers the potential of utilizing a greater percentage of integrated circuits than any other scheme which would meet our system requirements.

8.1.5 Resistor Network for A to D Converter

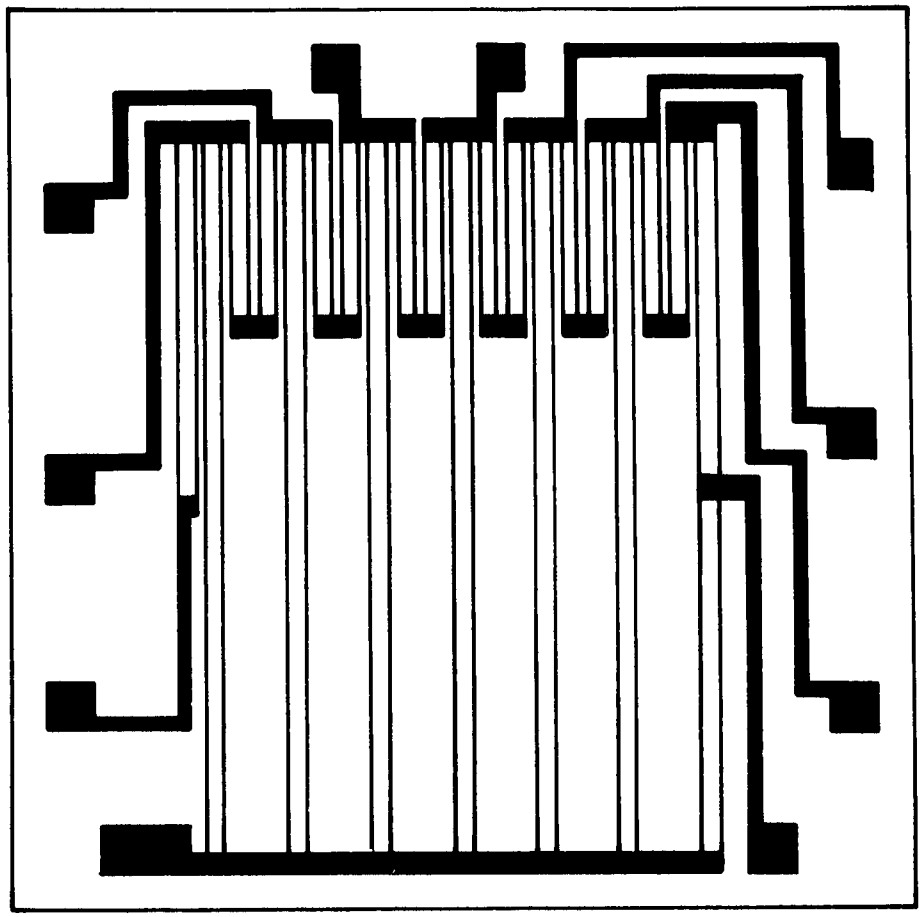
The preliminary mask design of the resistor network has been completed. The resistors are to be nichrome film on an oxidized silicon substrate. The connection to the resistors will be made with aluminum. The absolute value of resistance may vary -5 +10% with ratios being accurate to $\pm$5%. The ratio tracking over the temperature range of 0°C to +50°C must be within $\pm$.08%. These tolerances will allow the A to D converter to operate with errors from this source to be within the design goals. The preliminary layout is shown in Figure 6.

8.1.6 Switch and Amplifier Designs

8.1.6.1 Multiplexer Switch

A multiplexer switch design that is adequate to meet the DCS operation requirements was designed and evaluation tests using discrete components were conducted during this period. The circuit being studied is shown in Figure 7.

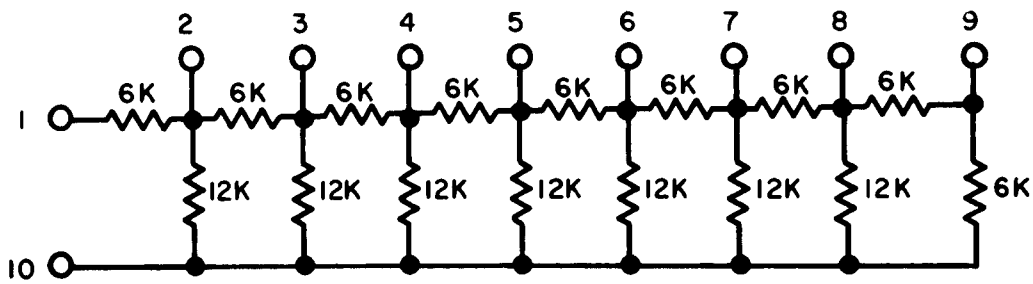
This circuit utilizes an N-channel FET to switch the 0 to +5V input signals and is controlled by a -6V to +6V control signal. The investigation included developing a switching model of the FET, studying the resistance, capacitance, and switching speed characteristics of the Model II and III Motorola FET and determining static and dynamic characteristics of the circuit configuration under simulated system operation conditions.



AL.

Ni CR

SCALE - 50/1



INDIVIDUAL TOLERANCE -5%, +10%

RATIO TOLERANCE ±5%

RATIO TRACKING WITH TEMP. 0°C - 50°C = .08 %

INTERGRATED CIRCUIT A/D CONVERTER

FIGURE 6

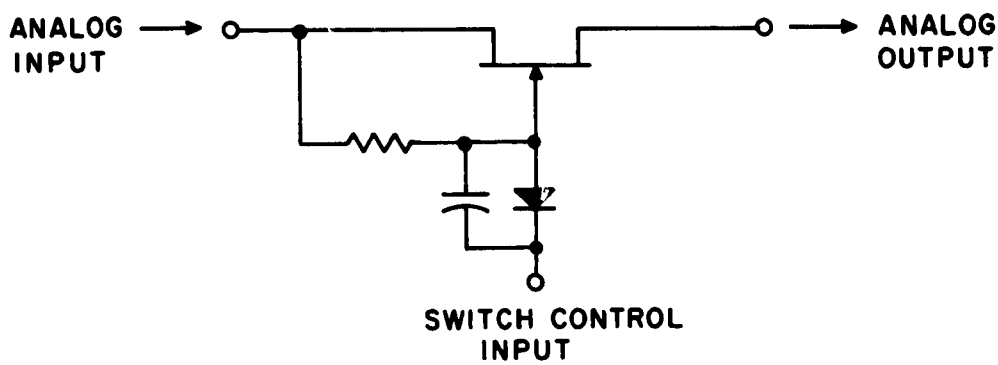


FIGURE 7
MULTIPLEXER SWITCH

8.1.6.2 Building Block Amplifier Design

Effort continued on investigation of the appropriate building block amplifier configuration. The basic NPN differential performance was tested using 3 mil emitter integrated circuit transistors. The comparison with its discrete component counterpart is given below:

	Actual Non-Gold Doped 2N834 Performance	Expected Single Chip Performance	Actual 3 Mil Emitter Integrated Component Performance
Gain (single ended)	4.0	4.6	4.0
Bandwidth	3 Mc	1 Mc	3 Mc
Offset (referred to input)	1 mV	50 mV	10 mV
Common Mode Rejection	80 db	40 db	50 db

A layout of this basic NPN configuration has been completed. This layout is quite flexible and will allow evaluation of several different circuit configurations.

The amplifier includes tapped resistors for increased flexibility. These taps may be shorted by wire bonding to provide data on amplifiers with a variety of constants from the first mask set. The transistors used in this amplifier will be a small geometry type to provide higher beta at low currents. This parameter allows the amplifier to be designed for low power and higher input impedance.

Test data was taken on other potential building block amplifier configurations and will be used for comparison with this configuration.