RESEARCH AND DEVELOPMENT
EPITAXIAL OVERGROWTH STRUCTURES
IN SILICON

Third Quarterly Progress Report

15 October 1962 to 14 January 1963

Contract No. DA-36-039-SC-89070

DA Project No. 3A99-21-001

U. S. Army Signal Research and Development Laboratory

Fort Monmouth, New Jersey

Philco Project No. R-114.1

PHILCO CORPORATION

LANSDALE DIVISION

Lansdale, Pennsylvania

(5) 509 600

PHILCO CORPORATION
LANSDALE DIVISION
Lansdale, Pennsylvania

(6) RESEARCH AND DEVELOPMENT

EPITAXIAL OVERGROWTH STRUCTURES IN SILICON •

(9) ~~Third~~ Quarterly Progress ~~Report~~ rept no. 3,

15 Octo[redacted]62 ~~to~~ 14 Janu[redacted]963,

(15) Contract ~~No.~~ DA-36-039-SC-89070

(16) DA Project No. 3A99-21-001

U.S. Army Signal Research and Development Laboratory

Fort Monmouth, New Jersey

Object of Program:

Research and Development work to conduct investigations of epitaxial overgrowth structures in silicon in accordance with Technical Guidelines for PR&C No. 62-ELP/R-4901, dated 25 September 1961.

(Philco Project No. R-114.1)

Report Prepared by:

Wby G. Schnable,

PREFACE

This is the third quarterly progress report covering the period 15 October 1962 to 14 January 1963 on a program for RESEARCH AND DEVELOPMENT OF EPITAXIAL OVERGROWTH STRUCTURES IN SILICON. This program is being carried out by the Semiconductor Research and Development Laboratories of Philco Corporation, Lansdale Division, for the United States Army Signal Research and Development Laboratory, Fort Monmouth, New Jersey, under Contract No. DA-36-039-SC-89070, DA Project No. 3A99-21-001, Philco Project No. R-114.1.

Prepared and submitted by:

G. L. Schnable
Senior Engineering Specialist

Approved by:

C. G. Thornton, Manager
Advanced Development

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I - PURPOSE

The purpose of the program is to conduct investigations of epitaxial overgrowth structures in silicon. The structures may contain multilayers of similar or dissimilar conductivity types at various thicknesses as determined by the number and depth of layers mutually agreed upon by the contractor and the Contracting Officer's Technical Representative. Doping levels shall also be as mutually agreed upon. The structures, as mutually agreed upon, are to be constructed and delivered to the United States Army Signal Supply Agency, Fort Monmouth, New Jersey.

SECTION II - ABSTRACT

Details are provided on the work performed in meeting the third quarter goal of preparation and delivery of:

1. Structures prepared by oxide masking of selected areas during deposition of epitaxial silicon,

2. Structures prepared by oxide masking of selected areas during HCl etching,

3. Structures made by preferential growth of epitaxial silicon through holes in an oxide mask to form a transistor base followed by reoxidation and a second preferential growth to form emitters.

A brief review of oxidation and growth techniques is presented. Evaluation results are given for some specific structures produced during the quarter.

SECTION III - PUBLICATIONS, LECTURES, REPORTS & CONFERENCES

No publications, lectures or reports pertaining to work developed on this contract were issued or given during the period covered by this report. Three conferences pertaining to the contract were held during the quarter covered by this report. Representatives of the United States Army Signal Research and Development Laboratory and of the Philco Corporation, Lansdale Division, were present at each of the conferences held as indicated below.

First Conference:	October 18, 1962 (at Lansdale)
Second Conference:	November 20, 1962 (at Ft. Monmouth)
Third Conference:	December 18, 1962 (at Lansdale).

SECTION IV - INTRODUCTION

The work accomplished in the third quarterly period of Contract No. DA-36-039-SC-89070 is described in Section V - Factual Data. By mutual agreement, the delivery of epitaxially grown structures was to consist of a total of 12 wafers as follows:

The specification for the November 15 and December 15 deliveries (4 wafers each) included structures having the following layers:

substrate:	n^+, 0.05 ohm-cm
first layer:	p, 1.4 ohm-cm, 4 microns
second layer:	p^+, 0.02 ohm-cm, 3 microns
substrate:	p, 50 ohm-cm
first layer:	n, 2 ohm-cm, 10 microns
second layer:	n^+, 0.05 ohm-cm, 3 microns
substrate:	p^+, 0.05 ohm-cm
first layer:	p, 110 ohm-cm, 5 microns
second layer:	n, 60 ohm-cm, 15 microns
third layer:	n^+, 0.05 ohm-cm, 3 microns
substrate:	p^+, 0.05 ohm-cm
first layer:	p, 1.4 ohm-cm, 4 microns
second layer:	n^+, 0.005 ohm-cm, 3 microns.

In those wafers delivered November 15, the structure was oxidized prior to growth of the final layer, holes were cut

in the oxide photolithographically, and the final epitaxial layer was preferentially grown through holes in the oxide.

For the December 15 delivery, all of the layers were grown over the entire wafer surface, and the wafer was then oxidized. The oxide was removed in selected areas by photolithographic techniques, and the resulting structures, with oxide masking in selected areas, were subjected to HCl etching at 1200°C. Etching conditions were such as to remove silicon down to the substrate in unmasked areas, and to leave, as much as possible, the desired pattern of masked areas.

The specification for the January 15th structures was as follows:

substrate:	p^+, 0.05 ohm-cm
first layer (over entire wafer):	p, 6 ohm-cm, 5 microns
second layer (preferential through holes in an oxide mask):	n, 1 ohm-cm, 3 microns
third layer (preferential through holes in a mask formed by reoxidation of the structure):	p^+, 0.006 ohm-cm, 2-3 microns.

SECTION V - FACTUAL DATA

5.0 General

The structures supplied during this quarter were prepared using the apparatus described in the First and Second Quarterly Reports. Substrate preparation, doping techniques, and methods for determination of layer thickness and of carrier concentration were also as described previously.

5.1 Characteristics of Delivered Wafers

The characteristics of the 12 wafers delivered in accordance with the requirements for this quarter are shown in Table 5-1.

5.2 Mask Formation

The required silicon dioxide mask was prepared by thermally growing SiO_2 in steam or in wet oxygen at 900°C. The conditions were selected to minimize diffusion during growth of the required oxide. Approximately 240 minutes in steam at 900°C was employed to grow an oxide about 6000Å thick. Previous tests had shown that 5000Å oxide layers, grown in steam at

TABLE 5-1

Characteristics of Wafers Delivered per November 15, 1962, December 15, 1962, and January 15, 1963 Requirements

Date Required	Wafer No.	Layer No.	Resistivity ohm-cm	Conductivity Type	Thickness Mag Fringes*
Nov. 15	5308	Substrate	0.07	n^+	>500
		1	1.4	p	15
		2	0.025	p^+	10
Nov. 15	5315-2	Substrate	0.05	p^+	>500
		1	50.	p	12
		2	66.	n	54
		3	0.03	n^+	10
Nov. 15	5360-3	Substrate	50.	p	>500
		1	2.	n	27
		2	0.048	n^+	11
Nov. 15	5349-2	Substrate	0.05	p^+	>500
		1	1.56	p	12
		2	0.009	n^+	15
Dec. 15	5398-2	Substrate	0.05	n^+	>500
		1	2.6	p	14
		2	0.042	p^+	10
Dec. 15	5412-2	Substrate	50.	p	>500
		1	2.	n	44
		2	0.05	n^+	11
Dec. 15	5418-4	Substrate	0.05	p^+	>500
		1	22.4	p	13
		2	42.	n	50
		3	0.05	n^+	13
Dec. 15	5417-2	Substrate	0.05	p^+	>500
		1	18.2	p	14
		2	42.	n	46
		3	0.05	n^+	10
Jan. 15	5444-2	Substrate	0.05	p^+	>500
		1	1.5	p	15
		2	0.9	n	10
		3	0.0004	p^+	12
Jan. 15	5441-3	Substrate	0.05	p^+	>500
		1	6.	p	16
		2	1.	n	10
		3	0.003	p^+	10
Jan. 15	5441-4	Substrate	0.05	p^+	>500
		1	6.	p	15
		2	1.	n	10
		3	0.003	p^+	10
Jan. 15	5439-1	Substrate	0.05	p^+	>500
		1	5.	p	13
		2	1.	n	10
		3	0.005	p^+	8

* One interference fringe (Hg light) = 0.295 micron = 0.0116 mil.

900°C, were adequate for masking during HCl etching at 1200°C. The steam grown oxide was removed in selected areas by means of conventional photolithographic techniques. The pattern shown in Figure 5-1, or the negative of that pattern, was used to prepare the eight structures for the first two deliveries of this reporting period. The pattern, which was designed by Signal Corps personnel, includes squares of 0.002 inch and 0.05 inch, and lines 0.002 and 0.02 inch wide. Since the overall diameter of this pattern is one inch, wafers approximately 1-1/4 inch in diameter were used to prepare all of the structures for the November 15 and December 15 deliveries, rather than the 1-inch wafers used for other work on this contract.

The activation energy for substitutional diffusion of common dopants in silicon[1] is roughly twice that of the reaction for thermal oxidation of silicon[2, 3, 4, 5]. Therefore, diffusion is far less when a given thickness of oxide is grown at 900°C, rather than at a higher temperature, such as 1100°C. However, it must also be realized that with some structures under certain conditions, the pile-up effect[6] can result in an undesirable accumulation of dopant in the silicon

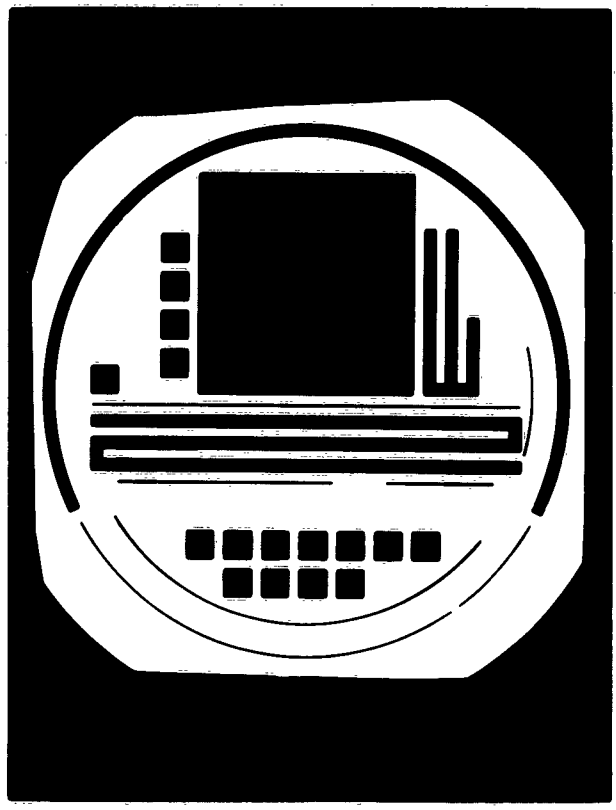

Figure 5-1. Pattern of lines and squares used for feasibility studies of oxide masking.

immediately under the thermally-grown oxide layer and, because of the differences in activation energies, the use of lower oxidation temperatures may aggravate this problem.

5.3 HCl Etching

The flow diagram for the HCl etching system is shown in Figure 5-2. The furnace part of the system is exactly as used for epitaxial silicon growth. Flow meters on the anhydrous HCl and purified H_2 stream indicate the relative ratio of HCl gas to H_2. The Molecular Sieve-filled cold trap on the HCl line may be used to insure low moisture content in the HCl gas. Dry ice (-78°C) is used as the coolant rather than liquid N_2 (-195°C) since HCl liquefies at -84°C.

Etching conditions were adjusted to obtain a good polish and reasonable etch rates in unmasked areas, with minimum undercutting or disturbance of the masked areas, with good definition and delineation. In particular, it was necessary to remove up to 27 microns of silicon in selected areas with a minimum of disturbance to the desired pattern, using the mask shown in Figure 5-1, including 0.002-inch squares and 0.002-inch lines. Typical results are shown in Figures 5-3 and 5-4.

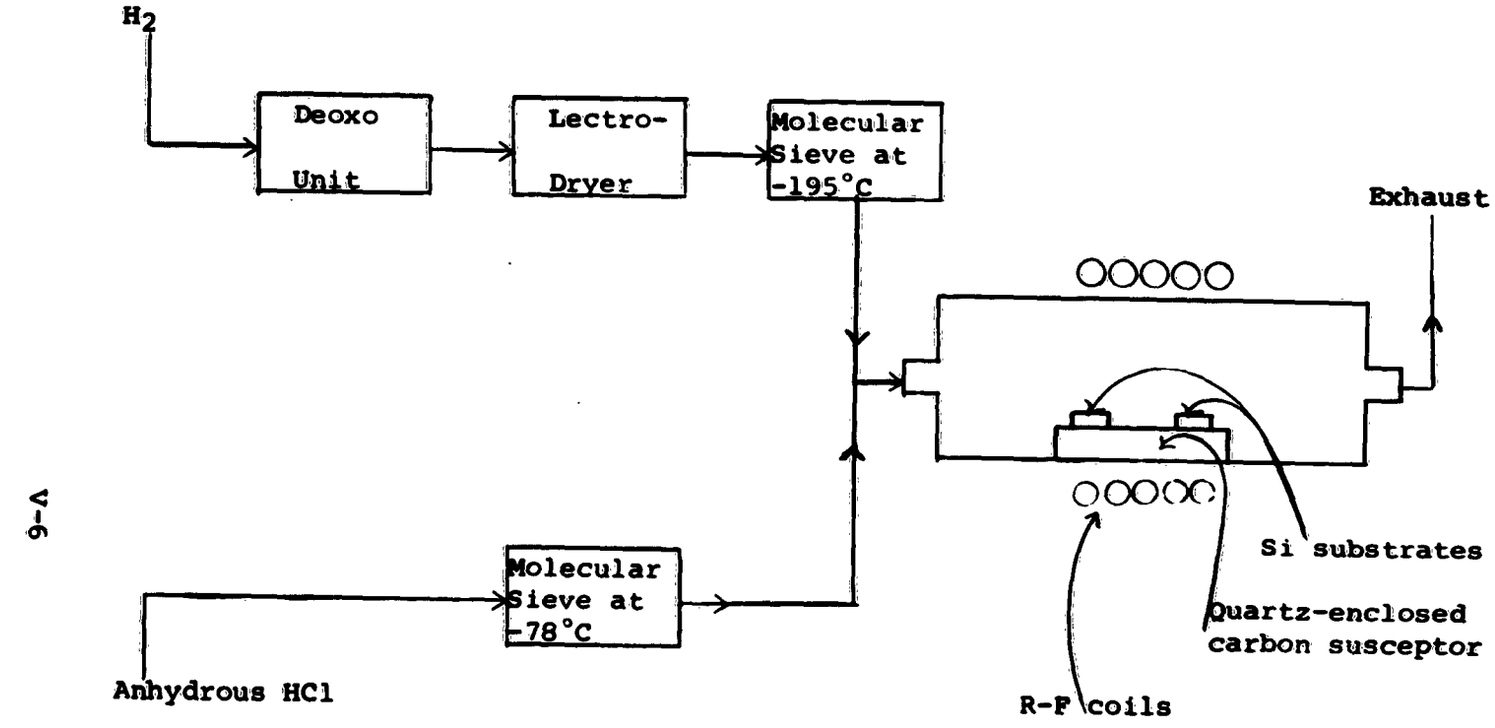

Figure 5-2 Flow diagram for HCl etching system.

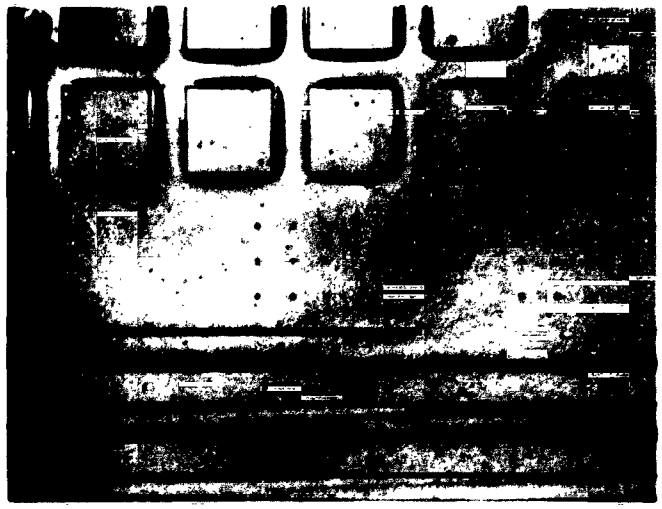

Figure 5-3. Top view of HCl-etched structure.

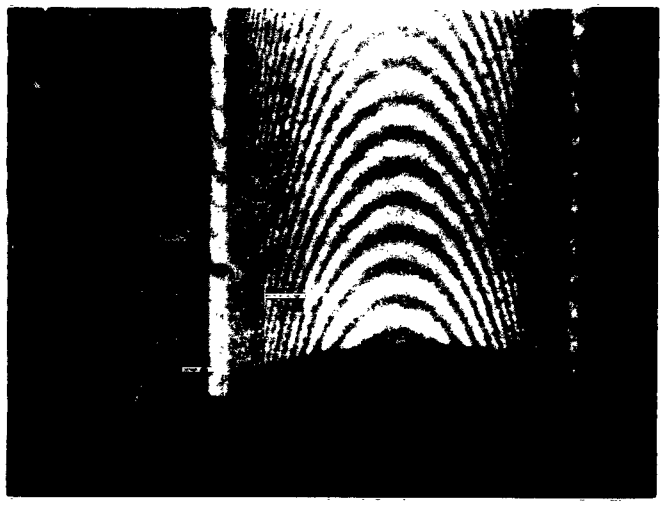

Figure 5-4. Angle-lapped section through an etched groove 0.02 inch wide.

Figure 5-3 is a top view of a wafer in which the lines and squares were oxide masked, and 10 microns of silicon was removed in surrounding areas. Figure 5-4 shows an angle-lapped section through the 20-mil spacing between 20-mil lines. The depth averages about 13 microns. It was found that with an oxide mask about 5000Å thick, up to about 10 microns of silicon could be removed with little disturbance of the 0.002-inch squares.

Typical conditions for HCl etching of selected areas of oxide-masked silicon wafers were as follows:

Flow rate, liters/min.	40.
Mole ratio, HCl to H_2	0.025
Substrate temperature, °C (optical pyrometer)	1175.

Under these conditions, etching proceeds at a rate of roughly 2 microns/minute. As indicated in Figure 5-4, the etch rate is somewhat higher immediately adjacent to masked areas than in the center of unmasked areas, and thus a slight "moat" surrounds the masked areas.

The samples agreed upon for January 15 involved preferential growth of epitaxial silicon through holes in an

oxide mask to form a transistor base, followed by reoxidation and a second preferential growth to form emitters. This work is intended to demonstrate the feasibility of preparing transistors by two preferential silicon growth steps with an intermediate reoxidation. The patterns used for this feasibility study were available solid circuit masks containing transistor and resistor patterns, as shown in Figures 5-9 through 5-11. The first epitaxial layer is to serve as a collector region of transistors. The second epitaxial layer, preferentially grown in selected areas, provides base regions and also provides structures which are to be used as resistors. The third epitaxial layer (second preferential layer) provides emitter areas. Figure 5-5 shows an angle-lapped section through a typical wafer after the reoxidation. Figure 5-6 shows the final structure after preferential growth of the emitter areas.

5.4 Selective Epitaxial Growth with Oxide Masking

The capabilities and limitations of oxide masking during selective epitaxial growth of silicon were investigated during this period. In one series of experiments in which a thermally-grown SiO_2 film covered the white areas of the pattern

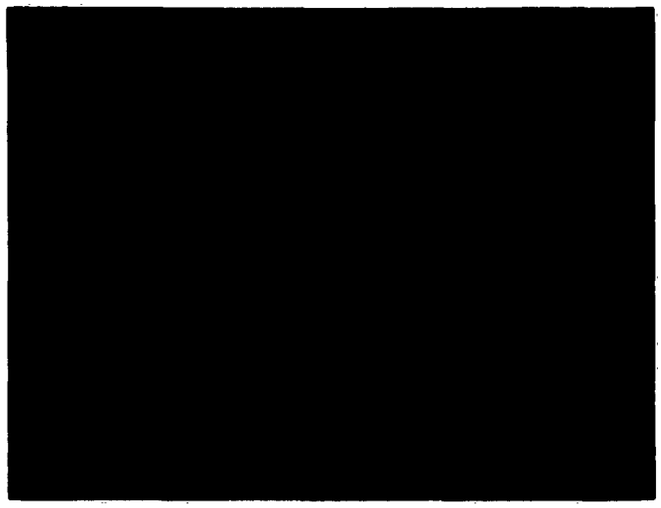

Figure 5-5. Angle-lapped section through a typical wafer after first preferential growth and reoxidation.

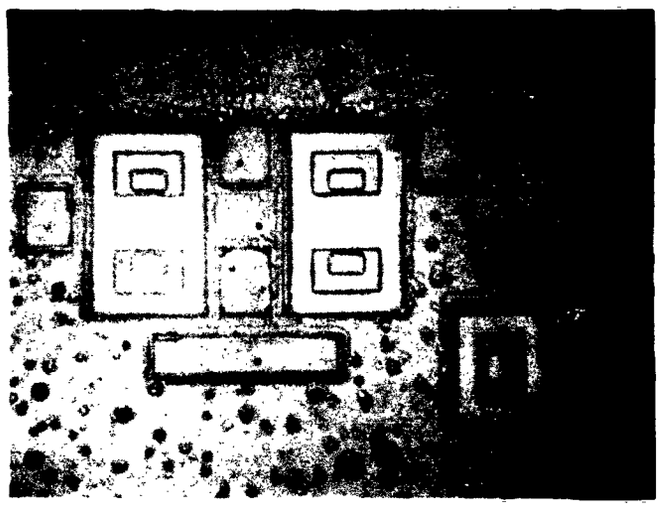

Figure 5-6. Typical structure after final growth of emitter areas.

of Figure 5-1, but was removed in the black areas, epitaxial silicon was grown preferentially. Growth conditions were adjusted as much as possible to obtain smooth epitaxial layers in the desired areas without growth of silicon crystallites over the oxide-covered areas. The structures submitted were grown under the following conditions:

Gas flow rate, liters/min	100.
Mole ratio of $SiCl_4$ to H_2	0.01
Substrate temperature, °C (optical pyrometer)	1200.

The apparatus used was similar to that described in the First Quarterly Report, with the one exception that the silicon wafers were placed directly on a silicized carbon susceptor rather than on a quartz-enclosed carbon susceptor. The silicized carbon susceptor was prepared by vapor phase deposition of silicon on a high-purity carbon susceptor at 1200°C, followed by a step in which the silicon-coated carbon was heated at about 1450°C for five minutes. Any excess silicon on the outside of the susceptor was removed by etching in a hydrofluoric acid-nitric acid mixture.

In general it was not possible to adjust epitaxial growth conditions so that the SiO_2-masked areas were entirely free of vapor-grown silicon. As indicated in Figure 5-7, which is a top view of preferential growth on 0.002-inch squares and 0.002- and 0.02-inch lines, a large number of crystallites formed on the surface in oxide-masked regions. Crystallite formation was also observed by Hirshon[7]. Figure 5-8 is an enlarged top view of the crystallites on the SiO_2 mask. It can be seen from examination of structures such as that shown in Figure 5-9 that the density of crystallites (number per area of surface) is frequently an order of magnitude greater in areas relatively distant from unmasked areas than in areas immediately adjacent to masked areas. Also, it was found that for a given set of epitaxial growth conditions, the growth rate was higher when the ratio of unmasked areas to total area was small than when that ratio was larger or unity.

The foregoing observations are evidence that under the conditions used, epitaxial silicon growth rates are influenced by the magnitude of the available silicon areas, and that significant localized changes in concentration of reactants must be occurring, even at the relatively high gas flow rates which

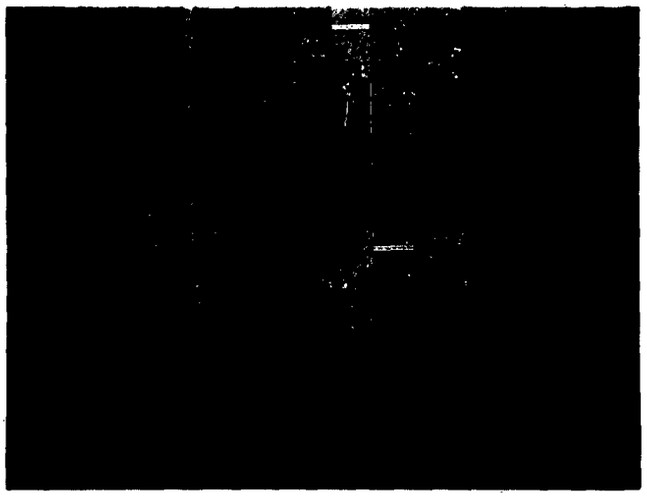

Figure 5-7. Top view of preferentially grown 3μ silicon deposits.

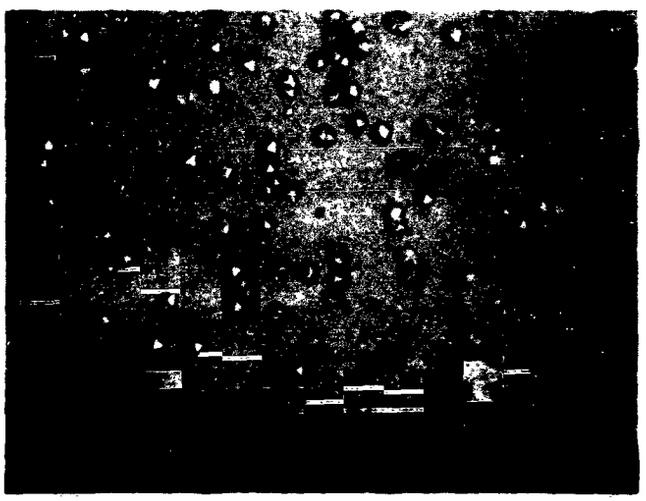

Figure 5-8. Enlarged view of silicon crystallites on an SiO_2 mask.

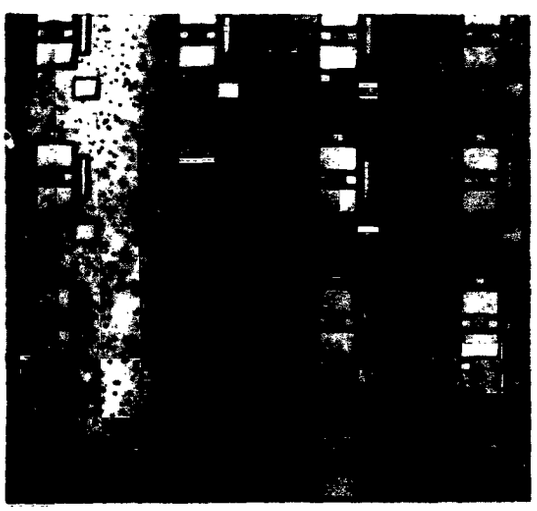

Figure 5-9. Preferentially deposited base regions.

are employed. Consequently it is very difficult to obtain freedom from silicon crystallites on oxide-masked regions and to obtain selective epitaxial growth which is controlled in terms of thickness and resistivity, without carefully determining optimum growth conditions for each desired masked structure. Moreover, with the above-described mechanisms prevailing, better results, in terms of relative freedom from formation of extraneous crystallites in oxide-masked areas, are more readily attained with recurring patterns with a high degree of uniformity in terms of distances to the nearest unmasked area. For example, structures consisting of small square openings on a recurring square array, such as the 0.011-inch squares located at 0.08-inch centers in the pattern used during the second quarter of this program, permit cleaner, more crystallite-free preferential growth than the structure indicated in Figure 5-7.

Electrical tests of diodes prepared by selective epitaxial growth on oxide-masked silicon substrates and microscopic observations demonstrate the feasibility of preparing devices with satisfactory characteristics by selective epitaxial growth. However, it must be pointed out that, for microelectronic

applications in which complete freedom from stray crystallites is required on SiO_2-covered areas in which metallic interconnections are to be placed, feasibility has not yet been established. Experiments performed subsequent to this reporting period have resulted in substantial reduction in the incidence of stray crystallites, and it may be expected that further work would eliminate the stray crystallite problem.

Tests in which a tungsten point, prepared as described by Pany[8,9], was touched to crystallites, indicated that they were usually in electrical contact with the underlying silicon. Also, the crystallites, when viewed microscopically at high power magnifications, appeared to have triangular facets, the sides of which were parallel to each other and to the three <111> planes intersecting the plane of the surface of the silicon wafer.

Tests were made to determine the extent to which crystallite formation could be attributed to pin-holes in the thermally-grown oxide film. Several wafers with patterns of oxide masks were quartered, and two diagonally opposite sections were subjected to preferential epitaxial growth. The other two quarters were subjected to chlorine etching[2,10] at

800°C to reveal pin holes. It was found that the density of pin holes, as revealed by Cl_2 etching, was on the order of 10 per cm^2, whereas the density of crystallites ranges from about 10^4 to 10^5 per cm^2 in areas most distant from unmasked areas to roughly 10^3 to 10^4 per cm^2 in areas immediately adjacent to unmasked areas. It was thus concluded that although pin holes in the oxide may be a factor in crystallite formation, other factors are more important. It should be pointed out, for example, that when preferential epitaxial growth of silicon on partially masked wafers is performed with wafers resting on fused quartz pedestals, growth of polycrystalline silicon generally occurs on the hot fused quartz surfaces, and obviously such growth is not a result of pin holes. In addition to the oriented crystallites observed on the masked surfaces, crystallites which do not appear to be oriented, and which are apparently not attached to the underlying silicon are sometimes observed. Possible nucleation sites for such crystallites include particles of non-volatile residue resulting from dust on the oxide surfaces, β-cristobalite crystallites at localized sites of devitrification of the amorphous SiO_2 film, scratches, etc.

PHILCO CORPORATION

A SUBSIDIARY OF Ford Motor Company

LANSDALE DIVISION • Church Road, Lansdale, Pennsylvania

24 May 1963

OASD (R&E), Rm 3E1065
Attn: Technical Library
The Pentagon
Washington 25, D.C.

Subject: Contract DA-36-039-SC-89070
Lansdale No. R-114

Enclosures: Third Quarterly Progress Report
Period 15 October 1962 to 14 January 1963

Gentlemen:

In accordance with Contract Item 1-3-1 and the Distribution List, we forward herewith one copy, (copies), of the Third Quarterly Progress Report for the subject contract.

Very truly yours,

PHILCO CORPORATION
LANSDALE DIVISION

John R. Gordon

John R. Gordon
Contract Administrator

JRG/kaw
enclosure/s

mask. The mask pattern used was an available solid circuit pattern which provided resistor structures as well as base cuts. The wafer was then reoxidized to mask the base regions. Finally, holes were cut through the oxide in regions where emitters were desired, and a final p^+ layer was preferentially deposited to form emitters.

Several variations in sequence were investigated. In initial experiments the first oxide layer was not removed prior to the growth of the second oxide layer. In subsequent experiments, the first oxide layer was removed with hydrofluoric acid prior to the second oxidation step. The latter procedure resulted in less formation of stray crystallites on the oxide outside of the base regions. Also, in initial work a base layer 3 microns thick was grown; in subsequent tests a 1.5-micron base layer was grown.

The above-described all-epitaxial structures were tested for emitter-base diodes and collector-base diodes by point contacting after removal of the oxide film in hydrofluoric acid.

Figure 5-9 shows a typical structure after preferential epitaxial growth of the base and resistor regions. The largest rectangles on this pattern are 0.015 by 0.024 inch. Stray crystallites are evident on the SiO_2 mask. Figure 5-10, an enlarged view of preferentially deposited regions, and Figure 5-7 both show the lower density of crystallites immediately adjacent to the preferentially grown areas. Figure 5-11 shows a typical January 15 structure after reoxidation to form a 6000 Å thick oxide layer; emitter cuts have been made in preparation for the final preferential epitaxial layer.

Figure 5-12 shows a typical structure after the first preferential epitaxial growth and the subsequent reoxidation. The preferential silicon growth area is at the left. The thickness of the first oxide layer, originally 8000 Å thick, was increased to about 12,000 Å during the second oxidation. The preferential growth spread slightly over the edge of the oxide mask, and the original oxide thickness can be seen at the left side of the thicker oxide layer.

Diode measurements were made on wafers containing structures similar to wafers #5360-3 and #5417-2 required for November and December, respectively, and wafer #5444-2

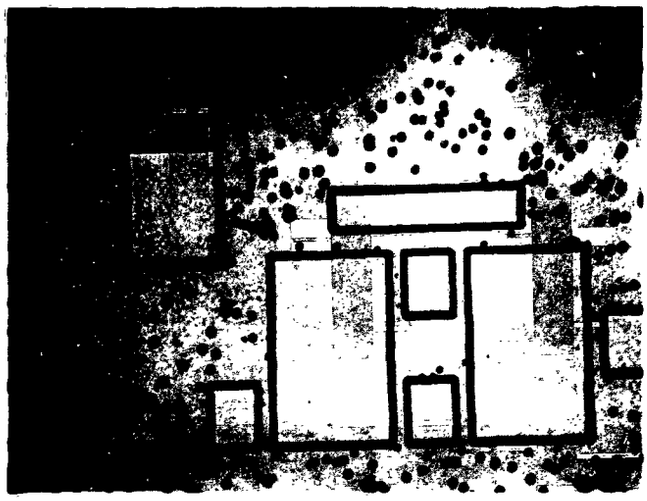

Figure 5-10. Enlarged view of preferentially deposited regions with SiO_2 removed.

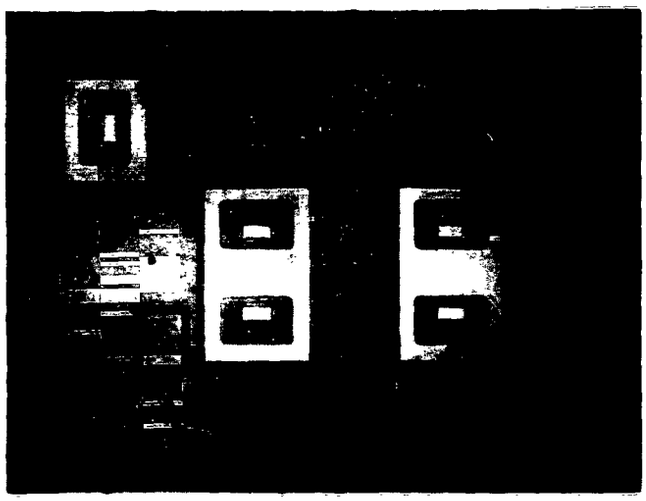

Figure 5-11. Structure after reoxidation, with emitter cuts made.

Figure 5-12. Typical structure after first preferential growth and reoxidation without removal of first oxide.

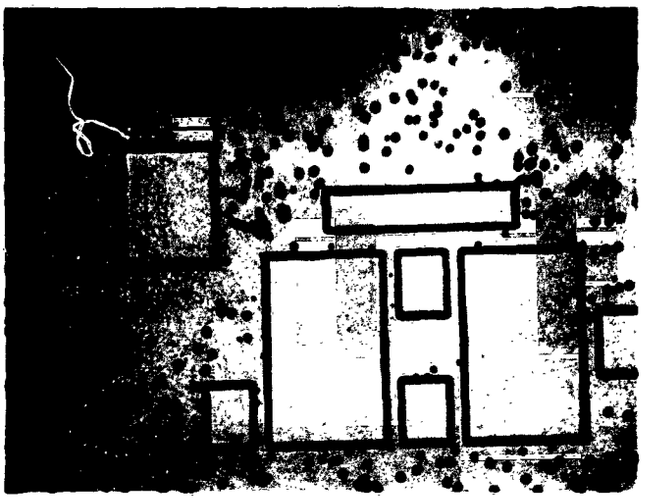

Figure 5-10. Enlarged view of preferentially deposited regions with SiO_2 removed.

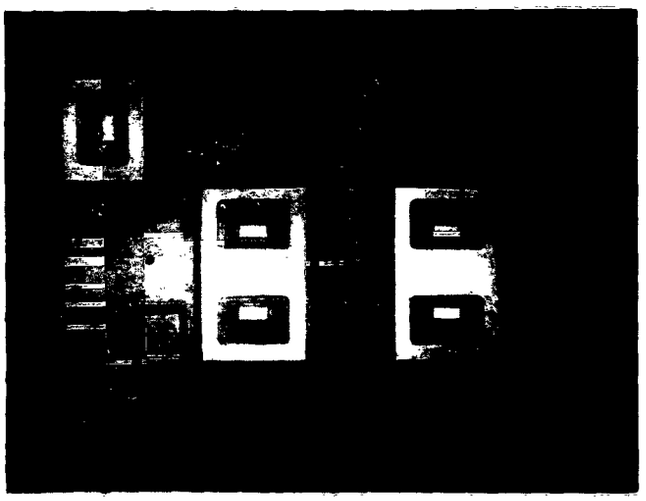

Figure 5-11. Structure after reoxidation, with emitter cuts made.

Figure 5-12. Typical structure after first preferential growth and reoxidation without removal of first oxide.

required for January. Median values for 10-μa diodes were 36 volts on the 0.050-inch squares and 74 volts on the 0.002-inch squares for the November requirement, and 7 volts on the 0.050-inch squares and 50 volts on the 0.002-inch squares for the December requirements. Emitter-to-base diodes of 8-30 volts, median 15 volts; and collector-to-base diodes of 15-40 volts, median 20 volts; both at 10 μa, were measured on wafer #5444-2.

Philco has a company-sponsored program to explore the limitations and capacities of preferential epitaxial growth with oxide masking. The findings of this program will be applicable to the fabrication of future structures on this contract.

REFERENCES

1. C. S. Fuller, "Diffusion Techniques," pp. 64-89 in "Transistor Technology," Volume 3, edited by F. J. Biondi, D. Van Nostrand Company, Inc., Princeton, New Jersey, 1958.

2. M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides," Bell System Technical Journal, 38, 749-784 (1959).

3. W. G. Spitzer and J. R. Ligenza, J. Phys. Chem. Solids, 17, 196-202 (1961).

4. P. S. Flint, "Rates of Oxidation of Silicon," presented at the Los Angeles Meeting of the Electrochemical Society, May 6-10, 1962; Electronics Division Abstracts, Vol. 11, No. 1, pp. 222-223 (1962); J. Electrochem. Soc., 109, 72C (1962) (abstract).

5. B. E. Deal, "Oxidation of Silicon in Dry Oxygen, Wet Oxygen, and Steam," presented at the Los Angeles Meeting of the Electrochemical Society, May 6-10, 1962; Electronics Division Abstracts, Vol. 11, No. 1, pp. 224-229 (1962); J. Electrochem. Soc., 109, 72C (1962) (abstract).

6. M. M. Atalla and E. Tannenbaum, "Impurity Redistribution and Junction Formation in Silicon by Thermal Oxidation," Bell System Technical Journal, 39, 933-946 (1960).

7. J. Hirshon, "Silicon Epitaxial Junctions with Compatible Masking," presented at the Los Angeles Meeting of the Electrochemical Society, May 6-10, 1962; Electronics Division Abstracts, Vol. 11, No. 1, pp. 242-243 (1962).

8. F. G. Pany, "A Technique for Etching Tungsten Probe Needles to Microscopic Sharpness," Electrochemical Society Electronics Division Abstracts, Vol. 11, No. 1, May 1962, pp. 205-210.

9. F. G. Pany, "Tungsten Needles for Semiconductor Tests," Electronics, Vol. 35, No. 20, pp. 102, 104 (1962).

10. M. M. Atalla, "Semiconductor Surfaces and Films; the Silicon-Silicon Dioxide System," pp. 163-182 in "Properties of Elemental and Compound Semiconductors," edited by H. C. Gatos, Vol. 5, Metallurgical Society Conferences, Interscience Publishers, New York, 1960.

11. H. C. Theuerer, "Epitaxial Silicon Films by the Hydrogen Reduction of $SiCl_4$," J. Electrochem. Soc., 108, 649-653, (1961).

12. E. G. Bylander, "Kinetics of Silicon Crystal Growth from $SiCl_4$ Decomposition," J. Electrochem. Soc., 109, 1171 - 1175, (1962).

SECTION VI - SUMMARY

Specifications for the agreed-on structures prepared during the third quarter involved five different multi-layer combinations of various doping concentrations and thicknesses. The feasibility of using an SiO_2 mask which was thermally grown at lower temperatures, where diffusion is not a problem, was demonstrated during this quarter.

A mask pattern was designed and provided by the Signal Corps for use in preparing the required structures. Structures delivered in November were prepared by preferential deposition of epitaxial layers through holes cut through the masking oxide. Photo resist techniques were used in cutting the desired holes. For the December delivery, structures were prepared by first growing epitaxial layers over the entire wafer surface and then by oxide masking and photo resist processing. HCl was used to remove material down to the substrate.

Knowledge was gained about some of the factors which influence spurious crystallite formation on oxide masks and, since no inherent limitations have been uncovered, it is expected that further work could solve the stray crystallite problem.

SECTION VII - PROGRAM FOR THE NEXT INTERVAL

Work for the next interval will involve growth and characterization of structures as mutually agreed upon by the contractor and the Contracting Officer's Technical Representative. Among the wafers which will be prepared during the next quarter will be structures in which epitaxial techniques are used to improve isolation between components on a wafer.

SECTION VIII - IDENTIFICATION OF PERSONNEL

The key technical personnel who have taken part in the work covered by this report are listed below. The approximate man-hours of work performed by each of the individuals is also indicated. A total approximate man-hours figure is given for the work performed during this report period by technicians assisting the key technical personnel. Background resumes of the key individuals added to the program are included.

Name	Title	Approx. Man-Hours
Hillegas, W., Jr.	Engineer	123
Khatchadourian, Z.	Project Engineer	154
Scher, P.	Junior Engineer	41
Schnable, G.	Senior Engineering Specialist	99
Taylor, S.	Junior Engineer	160
Watkins, A.	Junior Engineer	121
Technical Assistants		1217

HILLEGAS, WILLIAM J. JR. - Engineer

Mr. Hillegas received his B.S. in Chemical Engineering from Drexel Institute of Technology in 1960, having worked as a cooperative student engineer at the Lansdale Division of Philco Corporation from 1956 to 1959. He is currently doing graduate work in chemistry at Temple University. He has five years accumulated experience investigating the chemical problems related to the manufacture and improvement of performance and reliability of semiconductor devices, including investigations of the surface problems associated with high thermal conductivity potting compounds and reinforcing chemical coatings. During the past year his work has been chiefly concerned with the research and development of controlled epitaxial deposition of silicon, gallium arsenide and germanium on various substrates and with development of oxide masking techniques. He is a member of Tau Beta Pi and the American Association for the Advancement of Science, and is an associate member of the Electrochemical Society.

TAYLOR, SHELDON A. - Junior Engineer

Mr. Taylor received his B.S. in Electrical Engineering from Drexel Institute of Technology in 1962. Before graduation

he had worked for Philco as a cooperative student engineer for several periods, one of which was spent on the tunnel diode program. He has had experience in product engineering with emphasis on problems associated with plating and lead attachment. Currently he is evaluating epitaxially grown junctions.

Distribution List

	# of Copies
OASD (R&E), Rm 3E1065 Attn: Technical Library The Pentagon Washington 25, D.C.	1
Chief of Research & Development OCS, Department of the Army Washington 25, D.C.	1
Commanding General U. S. Army Electronics Command Attn: AMSEL-AD Fort Monmouth, New Jersey	3
Director U. S. Naval Research Laboratory Attn: Code 2027 Washington 25, D.C.	1
Commanding Officer & Director U. S. Navy Electronics Laboratory San Diego 52, California	1
Commander Aeronautical Systems Division Attn: ASAPRL Wright-Patterson Air Force Base, Ohio	1
Commander Air Force Cambridge Research Laboratories Attn: CRXL-R L. G. Hanscom Field Bedford, Massachusetts	1

	# of Copies
Commander Air Force Command & Control Development Division Attn: CRZC L. G. Hanscom Field Bedford, Massachusetts	1
Commander Rome Air Development Center Attn: RAALD Griffiss Air Force Base, New York	1
Commanding General U. S. Army Material Command Attn: R&D Directorate Washington 25, D.C.	1
Commanding Officer U. S. Army Communications & Electronics Combat Development Agency Fort Huachuca, Arizona	1
Commander Armed Services Technical Information Agency Attn: TISIA Arlington Hall Station Arlington 12, Virginia	10
Chief U. S. Army Security Agency Arlington Hall Station Arlington 12, Virginia	2
Deputy President U. S. Army Security Agency Board Arlington Hall Station Arlington 12, Virginia	1
Commanding Officer Harry Diamond Laboratories Attn: Library, Rm. 211, Bldg. 92 Washington 25, D.C.	1

	# of Copies
Commanding Officer U. S. Army Electronics Materiel Support Agency Attn: SELMS-ADJ Fort Monmouth, New Jersey	1
Corps of Engineers Liaison Office U. S. Army Electronics R&D Laboratory Fort Monmouth, New Jersey	1
AFSC Scientific/Technical Liaison Office U. S. Naval Air Development Center Johnsville, Pennsylvania	1
Advisory Group on Electron Devices 346 Broadway New York 13, New York	2
Marine Corps Liaison Office U. S. Army Electronics R&D Laboratory Fort Monmouth, New Jersey	1
Commanding General U. S. Army Combat Developments Command Attn: CDCMR-E Fort Belvoir, Virginia	1
Headquarters Electronics Systems Division Attn: ESAT L. G. Hanscom Field Bedford, Massachusetts	1
Director Fort Monmouth Office U. S. Army Communications & Electronics Combat Development Agency Fort Monmouth, New Jersey	1

	# of Copies
Mr. A. H. Young Code 618A1A Semiconductor Group Bureau of Ships Department of the Navy Washington 25, D.C.	1
Peter B. Myers, Mgr. Research & Advanced Technology Martin Company Mail No. T-683 Baltimore, Maryland	1
Kearfott Division General Precision, Inc. Clifton, New Jersey Attn: Dr. H. M. Pollack, Microelectronic Laboratory	1
Sylvania Electric Products 100 Sylvan Road Woburn, Massachusetts Attn: Dr. T. Longo	1
Motorola Semiconductor Products Phoenix, Arizona Attn: Dr. A. Lesk	1
Union Carbide and Carbon, Inc. Parma Laboratories Parma, Ohio Attn: Dr. R. Breckenridge	1
Merck, Sharp and Dohme Research Laboratories Rahway, New Jersey Attn: Dr. P. Pollack	1
Radio Corporation of America Semiconductor & Materials Division Somerville, New Jersey Attn: Dr. W. Bosenberg	1

	# of Copies
International Resistance Company Philadelphia, Pennsylvania Attn: Dr. J. Hirshon	1
Pacific Semiconductor, Inc. Lawndale, California Attn: Dr. J. Peterson	1
Shockley Transistor Stanford Industrial Park Palo Alto, California Attn: Dr. W. Shockley	1
Fairchild Semiconductor A Division of Fairchild Camera & Instrument Corp. 545 Whisman Road Mountain View, California Attn: Mr. Michael J. Mahoney	1
Texas Instruments, Inc. Semiconductor Components Division Dallas, Texas Attn: Dr. W. Adcock	1
IBM Federal Systems Division Kingston, New York Attn: Dr. E. Wajda	1
Hoffman Electronic Science Center Santa Barbara, California Attn: Mr. J. Spanos	1
Melpar, Inc. Falls Church, Virginia Attn: Dr. N. Fuschillo	1

	# of Copies
Commanding Officer U. S. Army Electronics R&D Laboratory Fort Monmouth, New Jersey	
Attn: Director of Research	1
Attn: Technical Documents Center	1
Attn: Technical Information Division	3
Attn: Rpts. Dist. Unit, Solid State & Frequency Control Division (Record Cy)	1
Attn: Ch, MQE Branch, Solid State & Frequency Control Division	1
Attn: W. Glendinning, Solid State & Frequency Control Division	1
Total number of copies to be distributed	60

This contract is supervised by the Solid State & Frequency Control Division, Electronic Components Department, USAELRDL, Fort Monmouth, New Jersey. For further technical information contact Mr. W. Glendinning, Project Engineer, Telephone 596-1447 (New Jersey Area Code 201).

AD

Philco Corporation, Lansdale, Pa.
RESEARCH AND DEVELOPMENT - EPITAXIAL OVERGROWTH STRUCTURES IN SILICON, by G. Schnable, Third Quarterly Progress Report for 15 November 1962 - 15 January 1963. 15 April 1963. (32)p. incl. illus., table, 13 refs. Contract DA-36-039-SC-89070 Unclassified Report

Details are provided on the work performed in meeting the third-quarter goal of preparation and delivery of:

1. Structures prepared by oxide masking of selected areas during deposition of epitaxial silicon,
2. Structures prepared by oxide masking of selected areas during HCl etching,
3. Structures made by preferential growth of epitaxial silicon through holes in an oxide mask to form a transistor base, followed by reoxidation and a second preferential growth to form emitters.

A brief review of oxidation and growth techniques is presented. Evaluation results are given for some specific structures produced during the quarter.

Unclassified

1. Epitaxial Overgrowth
2. Silicon

I. Schnable, G.
II. USAEMA, Ft.Monmouth, N.J.
III Contract DA-36-039-SC-89070

Unclassified

AD

Philco Corporation, Lansdale, Pa.
RESEARCH AND DEVELOPMENT - EPITAXIAL OVERGROWTH STRUCTURES IN SILICON, by G. Schnable, Third Quarterly Progress Report for 15 November 1962 - 15 January 1963. 15 April 1963. (32)p. incl. illus., table, 13 refs. Contract DA-36-039-SC-89070 Unclassified Report

Details are provided on the work performed in meeting the third-quarter goal of preparation and delivery of:

1. Structures prepared by oxide masking of selected areas during deposition of epitaxial silicon,
2. Structures prepared by oxide masking of selected areas during HCl etching,
3. Structures made by preferential growth of epitaxial silicon through holes in an oxide mask to form a transistor base, followed by reoxidation and a second preferential growth to form emitters.

A brief review of oxidation and growth techniques is presented. Evaluation results are given for some specific structures produced during the quarter.

Unclassified

1. Epitaxial Overgrowth
2. Silicon

I. Schnable, G.
II. USAEMA, Ft.Monmouth, N.J.
III Contract DA-36-039-SC-89070

Unclassified

AD

Philco Corporation, Lansdale, Pa.
RESEARCH AND DEVELOPMENT - EPITAXIAL OVERGROWTH STRUCTURES IN SILICON, by G. Schnable, Third Quarterly Progress Report for 15 November 1962 - 15 January 1963. 15 April 1963. (32)p. incl. illus., table, 13 refs. Contract DA-36-039-SC-89070 Unclassified Report

Details are provided on the work performed in meeting the third-quarter goal of preparation and delivery of:

1. Structures prepared by oxide masking of selected areas during deposition of epitaxial silicon,
2. Structures prepared by oxide masking of selected areas during HCl etching,
3. Structures made by preferential growth of epitaxial silicon through holes in an oxide mask to form a transistor base, followed by reoxidation and a second preferential growth to form emitters.

A brief review of oxidation and growth techniques is presented. Evaluation results are given for some specific structures produced during the quarter.

Unclassified

1. Epitaxial Overgrowth
2. Silicon

I. Schnable, G.
II. USAEMA, Ft.Monmouth, N.J.
III. Contract DA-36-039-SC-89070

Unclassified

AD

Philco Corporation, Lansdale, Pa.
RESEARCH AND DEVELOPMENT - EPITAXIAL OVERGROWTH STRUCTURES IN SILICON, by G. Schnable, Third Quarterly Progress Report for 15 November 1962 - 15 January 1963. 15 April 1963. (32)p. incl. illus., table, 13 refs. Contract DA-36-039-SC-89070 Unclassified Report

Details are provided on the work performed in meeting the third-quarter goal of preparation and delivery of:

1. Structures prepared by oxide masking of selected areas during deposition of epitaxial silicon,
2. Structures prepared by oxide masking of selected areas during HCl etching,
3. Structures made by preferential growth of epitaxial silicon through holes in an oxide mask to form a transistor base, followed by reoxidation and a second preferential growth to form emitters.

A brief review of oxidation and growth techniques is presented. Evaluation results are given for some specific structures produced during the quarter.

Unclassified

1. Epitaxial Overgrowth
2. Silicon

I. Schnable, G.
II. USAEMA, Ft.Monmouth, N.J.
III. Contract DA-36-039-SC-89070

Unclassified