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SEMICONDUCTOR SINGLE-CRYSTAL CIRCUIT DEVELOPMENT

TECHNICAL DOCUMENTARY REPORT ASD-TDR-63-281

MARCH 1963

Electronic Technology Laboratory
Aeronautical Systems Division
Air Force Systems Command
United States Air Force
Wright-Patterson Air Force Base, Ohio

Report No. 03-63-11

Project No. 4159, Task No. 415906

Prepared under Contract No. AF33(616)-6600
by

TEXAS INSTRUMENTS INCORPORATED
Semiconductor Network Department
Dallas, Texas
Edited by: W. T. Matzen

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ABSTRACT

Part I of this report describes the design and experimental investigation of silicon functional electronic blocks using, primarily, the circuit analog design technique. During the period of investigation under this contract feasibility was established for a number of useful linear circuit functions. Fabrication techniques, a problem in earlier experimental work, have been overcome in most cases. A hermetically sealed package was developed which established a new order of magnitude for practical size reduction.

Part II of this report describes the work done in the exploration of other semiconductor phenomena. Falloff of α at low collector currents in silicon transistors is shown to be due to a shunt-diode current originating at the emitter-base junction periphery; hence improved performance through diffusion and oxidization studies may be possible.

A capacitor with linear voltage-capacitance characteristic and an inductor, utilizing a four-terminal field effect gyrator, have been analyzed and appear promising for silicon FEB's. Fabrication of satisfactory devices will require improved control of epitaxial material.

Thin-film metal-oxide-metal diodes do not have immediate circuit application due to high junction capacitance, which limits switching speed. This restriction may be overcome by reduction of trap densities in the oxide film.

Based on measurements of the piezoelectric properties, GaAs is not an optimum material for use as a resonator or transducer in integrated circuit applications. However, GaAs P-N junctions are efficient sources of infrared radiation and appear promising for electro-optical FEB's.

FOREWORD

This report was prepared by the Semiconductor-Components Division of Texas Instruments Incorporated, Dallas, Texas, on Air Force Contract AF33(616)-6600 under Task No. 415906 of Project No. 4159, "Semiconductor Single-Crystal Circuit Development." The work was administered under the direction of Electronic Technology Laboratory, Aeronautical Systems Division. Captain Lawrence Roesler was the project engineer for the laboratory.

The studies presented began in June 1959 and were concluded in January 1962. The work was carried on under the direction of J. S. Kilby, manager of the Semiconductor Networks Department. Charles Phipps was the program manager.

Although the studies were a group effort, the chief contributors and their fields of interest were: A. E. Evans, design; Dr. J. W. Lathrop, fabrication technology; and Dr. J. R. Biard, device phenomena. The material was compiled and edited by Dr. W. T. Matzen.

This report is a final report and concludes the work on Contract AF 33(616)-6600. The contractors report number is 03-63-11.

This report is unclassified.

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PREFACE

During the decade from 1948 to 1958, semiconductor technology progressed rapidly. Silicon fabrication techniques, particularly those of photolithography and diffusion, allowed precise placement of junction regions, and multiple junction layers to be formed within the bulk semiconductor. Using these techniques, Texas Instruments devised and exhibited to the Air Force late in 1958 operating semiconductor circuits. Subsequently, a research and development program was defined to explore semiconductor circuits or Functional Electronic Blocks (FEB's).

In June 1959, this contract AF33(616)6600, was begun, investigating the use of single crystal semiconductor material for complete circuit functions. The objectives of the program required:

All circuits shall be formed from semiconductor material

The base material must be silicon

Smallness and reliability are primary goals

Circuit functions would be oriented primarily toward airborne electronic equipment applications

Military environmental conditions should be considered for operating requirements.

The particular circuit functions selected in order of priority for investigation were:

Audio amplifiers

Multivibrators

Video Amplifiers

Bandpass Amplifiers

Oscillators

Tunable Amplifiers.

The purpose of the theoretical investigations and experimental fabrication was to establish the practical limitations of such circuit parameters as voltage, current, temperature dependence, and frequency response. In this manner, problem areas requiring a more intensive study could be defined.

Part I of this report describes the investigation, experimental fabrication, and limitations of FEB's for each of the above circuit types. Thereafter, defined tasks exploring other semiconductor phenomena that might overcome these limitations are described in Part II.

PART I

INVESTIGATION OF SILICON FUNCTIONAL ELECTRONIC BLOCKS

SECTION I
INTRODUCTION

The initial design technique devised by Texas Instruments was the use of circuit analogs to define the electrical action within each region of the semiconductor material. In this manner, individual circuit element path effects could be investigated, and the results of this work readily applied to a wide variety of circuit designs.

Because of the need for an active element with an input impedance, orders of magnitude higher than could be achieved with bipolar junction transistors, the unipolar field-effect transistor was investigated. Work in this area led to some useful and interesting field-effect characteristics that could be utilized in both linear and nonlinear circuit functions.

The first part of this report describes the design and experimental investigation of semiconductor circuits, using, primarily, the circuit analog design techniques.

During the period, a functional hermetically-sealed package for FEB's was developed by Texas Instruments, establishing a new order of magnitude for practical size reduction. All of the experimental FEB's were designed for mounting in this package or modular dimensions thereof.

Manuscript released by the editor, 4 March 1963, for publication as an ASD Technical Documentary Report.

SECTION II

CIRCUIT ELEMENTS

2.1 Introduction

Semiconductor networks are designed by relating regions within a wafer of semiconductor crystal to conventional circuit elements. Therefore, it is necessary for the semiconductor network design engineer to understand the relationship between the semiconductor material and circuit elements. Such an understanding requires theoretical and experimental investigation of semiconductor elements.

2.2 Passive Elements

2.2.1 Resistors

Resistors can be formed from single crystal semiconductors either by the bulk material between two contacts or by thin heavily doped layers upon or within the bulk material. Illustrations of these methods are shown in Figure 1. In a. of Figure 1, the resistor is formed by bulk semiconductor material between ohmic contacts a and b. Its value can be calculated from the length, cross-sectional area, and resistivity of the material. Resistors produced in this manner are linear and do not vary with voltage in the range normally used. However, their resistance is a function of temperature. In the resistivity ranges normally used, a typical variation with temperature is shown by curve a in Figure 2. The temperature coefficient of the resistance can be reduced by using material with much higher impurity concentrations (lower resistivity); however, the ratio of the length to cross-section area of the resistor must likewise be increased to maintain a given resistance value. Forming resistors having high impurity concentrations and very small cross-sectional areas is a more feasible method and is shown in Figure 1.b. Thin layers are formed on a semiconductor wafer by a diffusion process. The desired length and width dimensions can be obtained by diffusing through a silicon-oxide mask (Figure 1.b.) The PN junction serves as a barrier, confining the current flow to the diffused region near the surface. Bulk type and diffused layer resistors can be utilized in semiconductor networks.

Diffused resistors having a range of surface impurity concentration, C_S, were prepared to determine the temperature characteristics as a function of C_S. Curve b of Figure 2 shows the temperature characteristics of a typical diffused resistor in which the surface impurity concentration was selected to minimize the resistance-temperature coefficient.

Figures 3 and 4 show the temperature characteristics of P-type and N-type diffused-layer resistors for various values of surface impurity concentration. The characteristics of both types are similar. If the temperature is not too high, the temperature coefficient is seen to be positive at low values of surface impurity concentration and negative at high values of surface concentration

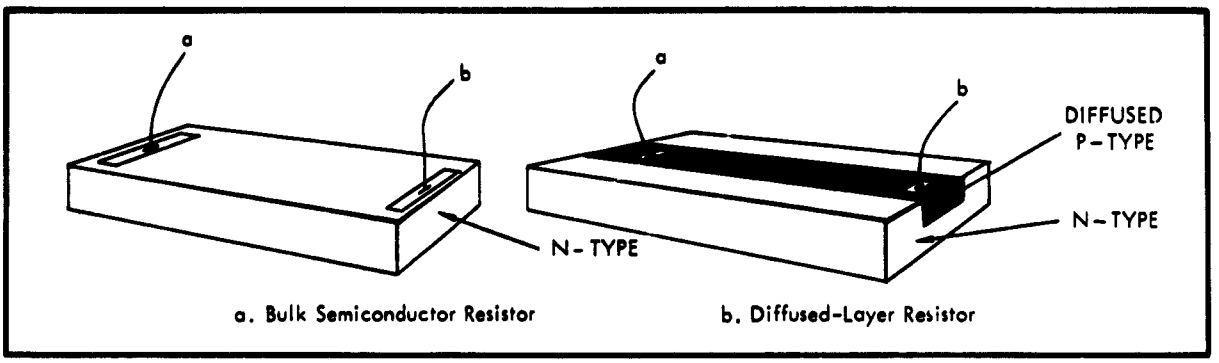


Figure 1. Semiconductor Resistor

Sheet resistance of the diffused layer is a function of diffused impurity surface concentration and diffusion depth. Sheet resistances of 50 to 5000 ohms per square have been obtained.

2.2.2 Capacitors

A reverse-biased PN junction may be used as a capacitor where the depletion region at the junction serves as the dielectric. For a given material, the capacitance is a function of the width of the depletion region and junction area. For silicon, capacitance values of 1.3 pf/mil^2 are possible.

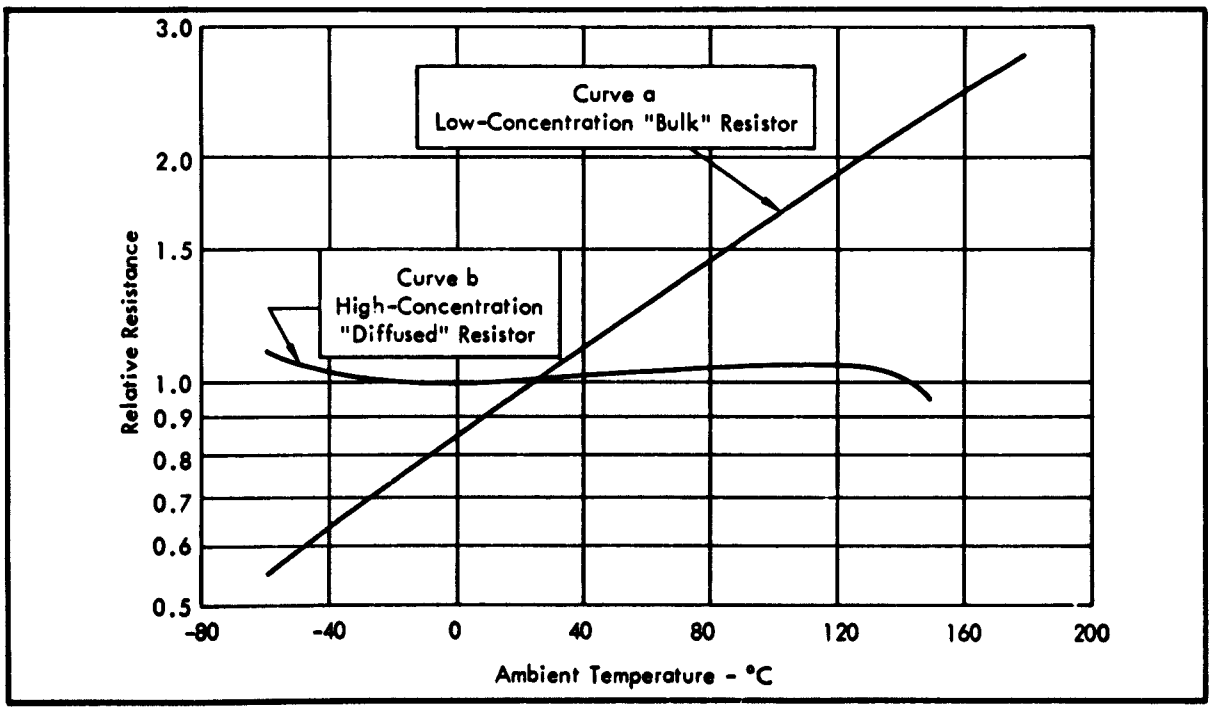


Figure 2. Temperature Characteristics of Silicon Resistors

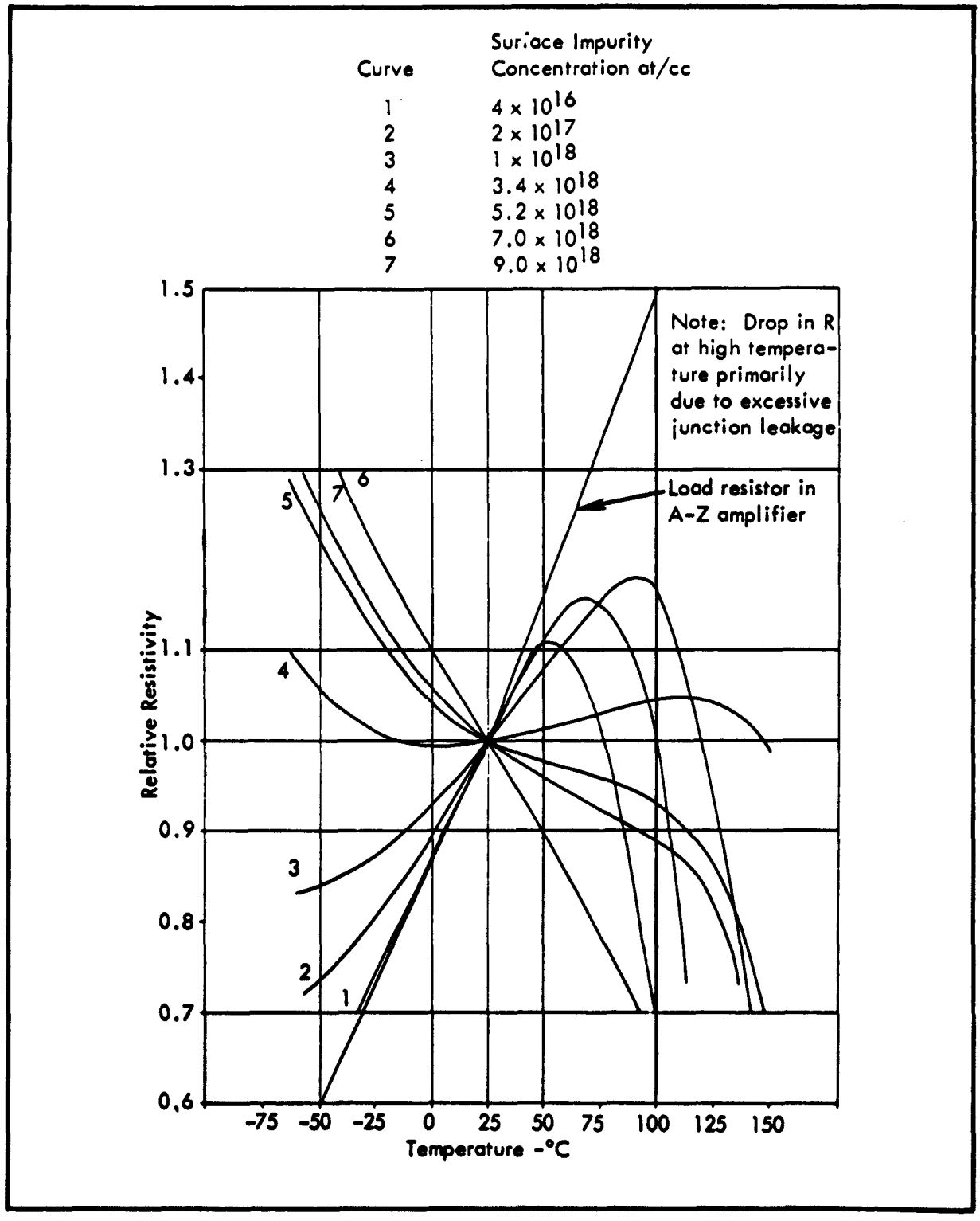


Figure 3. Temperature Characteristics of Gallium Diffused Layer Resistors

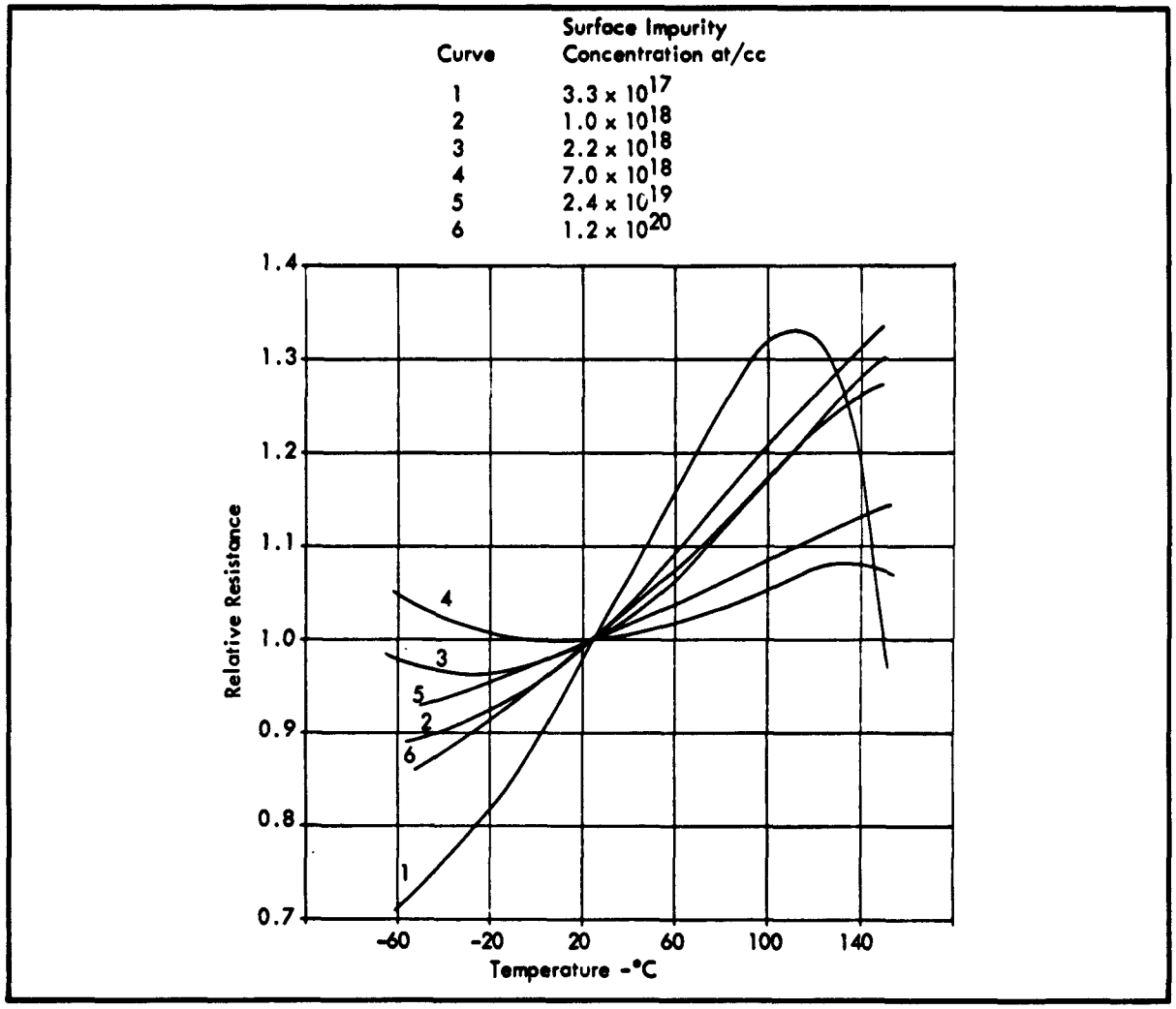


Figure 4. Temperature Characteristics of Phosphorus Diffused Layer Resistors

Breakdown voltages of several hundred volts can be obtained with a low temperature coefficient of capacitance. Since the width of the depletion region changes with applied voltage, a nonlinear response results. Although this effect has been used to advantage in many applications, capacitors of this type are not suitable for high level linear circuits. Also, capacitors are polarized, and must be connected so that the junction is not forward-biased.

For applications where linearity is important, or where reverse bias cannot always be maintained, another type of capacitor can be formed on silicon wafers. The dielectric of these capacitors consists of a silicon-oxide layer formed on the surface of the silicon, as shown in Figure 5. The semiconductor serves as one electrode of the capacitor and a layer of metal is

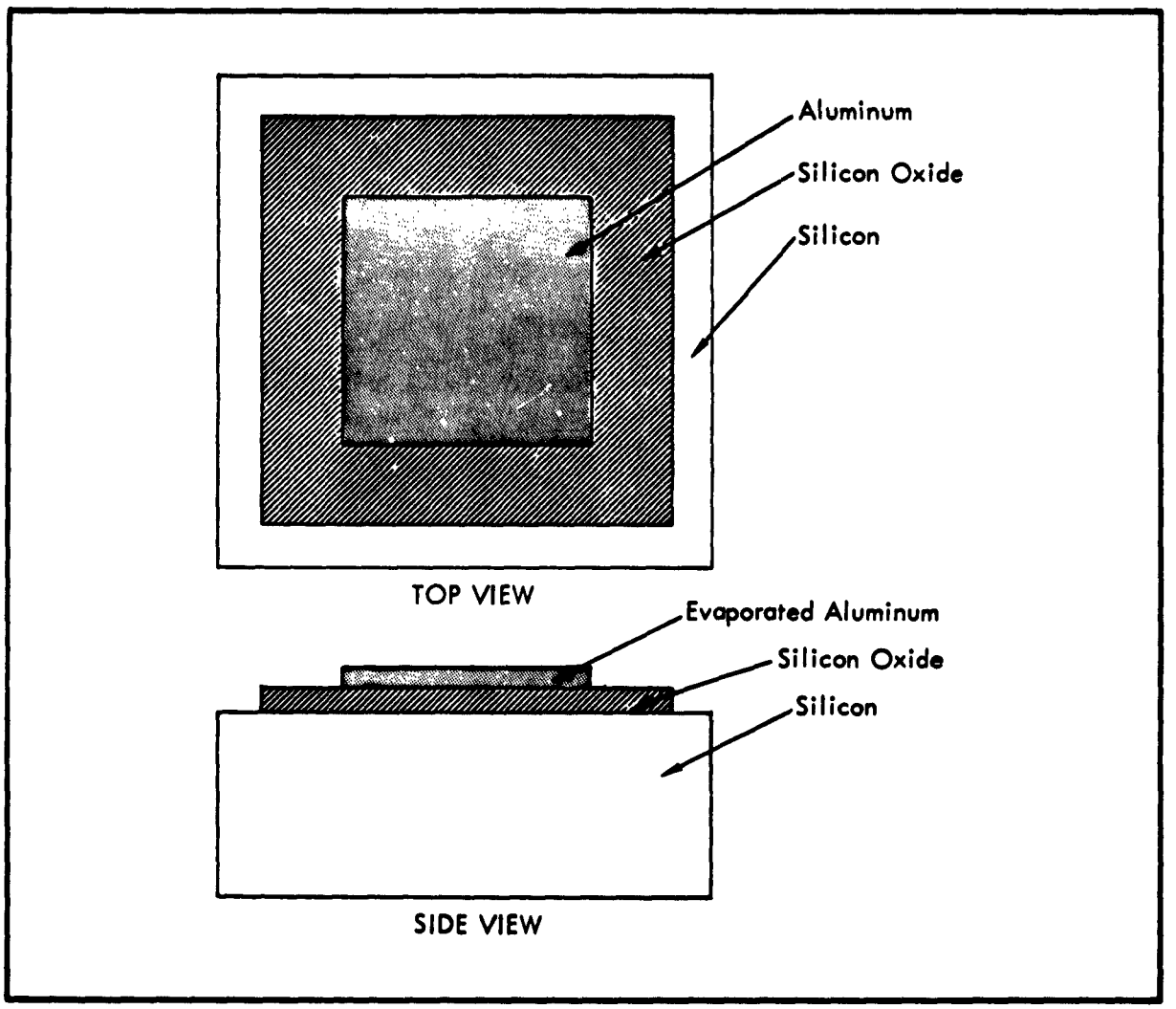
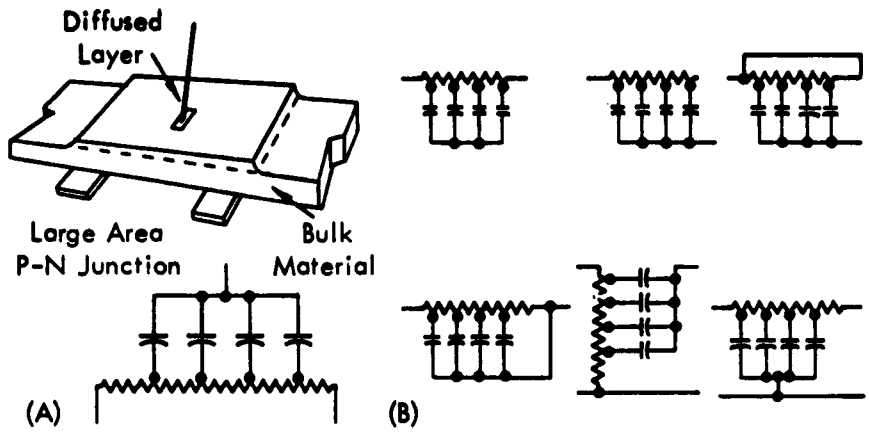


Figure 5. Silicon Oxide Dielectric Capacitor

deposited on the oxide for the counter-electrode. Since the oxide is formed on a single-crystal wafer it is unusually free of defects. Oxide-type capacitors have temperature coefficients well below 100 PPM/°C, low voltage coefficients and excellent stability with time. For 25-volt breakdown ratings, a capacitance of 0.1 pf/mil^2 can be obtained.

2.2.3 Distributed-Constant RC Network

Distributed-constant resistor-capacitor networks are readily formed in semiconductor networks. One type of distributed RC network is shown in Figure 6.a. Several ways to connect its three terminals are shown in Figure 6.b. Such networks have many useful properties, particularly for



Semiconductor distributed-constant R-C networks: (A) distributed network with its equivalent circuit and (B) several possible applications of distributed R-C networks

Figure 6. Semiconductor Distributed-Constant RC Networks

low-pass filters or phase-shift networks. A distributed RC network used as a low-pass filter will have much sharper cutoff characteristics than a three-stage lumped-constant network and will provide more attenuation for a given RC product. Phase-shift networks constructed in this manner have more phase shift for a given attenuation than a lumped-constant equivalent. Because of the layered nature of the structures, distributed-constant networks are easy to fabricate and have been frequently used, particularly in switching networks.

Since the capacitance of a reverse-biased PN junction capacitor is dependent on voltage, a distributed-constant resistor-capacitor network fabricated by this method can be made tunable by varying the bias on the PN junction. Thus, tunable filters and variable phase shift networks can be realized. A distributed RC network may also be made by forming an oxide capacitor on the bulk material. This type would not be tunable as the one using the PN junction capacitor; however, there are many applications where fixed-frequency networks are useful.

2.3 Active Elements

To date several types of active elements have been used in semiconductor networks. These are:

1. Bipolar transistors

2. Unipolar field-effect transistors (UNIFET)*

3. Bipolar field-effect transistors (BIFET)*

4. Diodes.

Other possible devices from semiconductor networks are tunnel diodes, PN-PN switches, varactors, solar cells, and thermoelectric elements.

2.3.1 Bipolar Transistors

The construction techniques used in fabricating double-diffused mesa and planar transistors fit in well with the semiconductor network philosophy. These transistors can be fabricated using diffusion techniques, photographic negatives and photoetching techniques. By controlling the diffusion concentrations, depths, and the geometry of the negatives, many types of transistors can be built (low-level, switching, high frequency or power).

Many times, the optimum diffusion concentration for a bipolar transistor cannot be realized due to constraints placed on the diffusion by resistor values or field-effect devices on the same substrate. However, the mesa and planar transistors are extremely tolerant to wide variations in concentration. Acceptable bipolar transistors have been built with collector regions from 0.5 to 10 ohm-cm and with base concentrations from 10^{16} to 10^{19} impurity atoms/cc. This wide tolerance allows the network designer to optimize the more critical components of the circuit. In cases where acceptable diffusions for the transistors differ from the diffusions required for resistor areas or other component areas, multiple diffusions can be utilized.

2.3.2 Unipolar Field-Effect Transistors (UNIFET)

Initial work under this contract was concentrated on development of techniques to realize audio frequency amplification in semiconductor networks. A literature search and review of the state-of-the-art in transistor circuits indicated the need for an active element with an input impedance a few orders of magnitude larger than realizable with conventional transistors. The UNIpolar Field-Effect Transistor (UNIFET) appeared to offer a solution for this problem. Thus, an investigation of the field-effect structure was undertaken.

The simplified model of Figure 7 shows the regions and critical dimensions of a unipolar field-effect transistor. Figure 8 shows a typical

*An attempt is being made to coin logical abbreviations for the various types of active regions utilized within a semiconductor network. UNIFET is an abbreviation of UNIpolar Field-Effect Transistor and BIFET stands for BIpolar Field-Effect Transistor. These abbreviations will be used throughout this report to aid the readibility of the document and allow clear and concise statements about the types of active regions used.

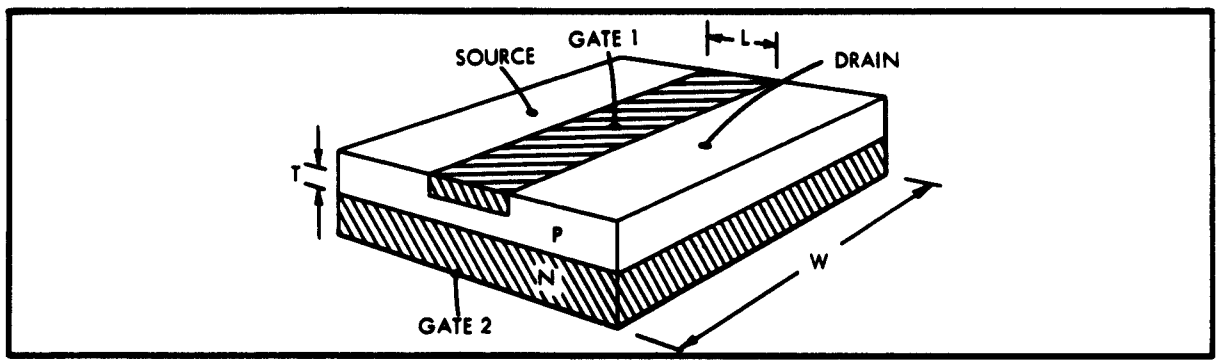


Figure 7. Unipolar Field-Effect Transistor Model

set of drain voltage versus drain current characteristics with gate voltage as a parameter. Critical design parameters are:

V_p = pinch-off voltage

I_{DSS} = channel saturation current

BV_{DGO} = drain-to-gate breakdown voltage

g_{mo} = maximum transconductance.

Design equations for these parameters indicate the need for critical control of the geometry. It may be possible to obtain better control of the

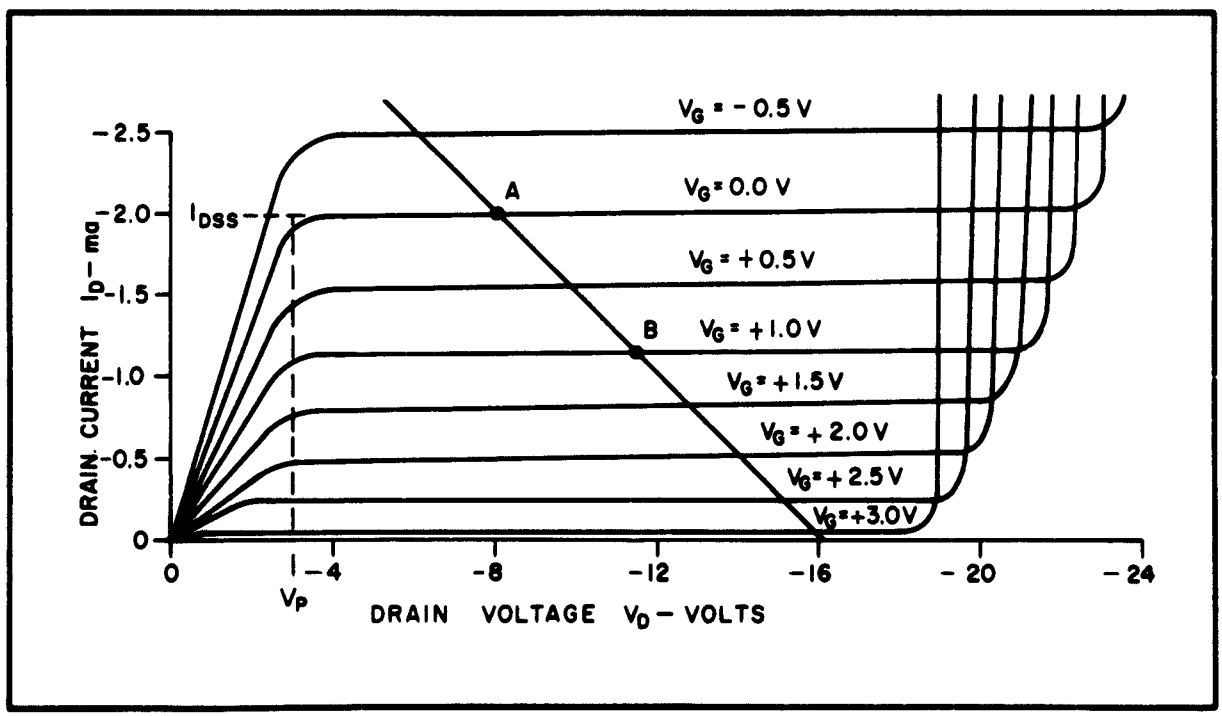


Figure 8. UNIFET Drain Characteristics

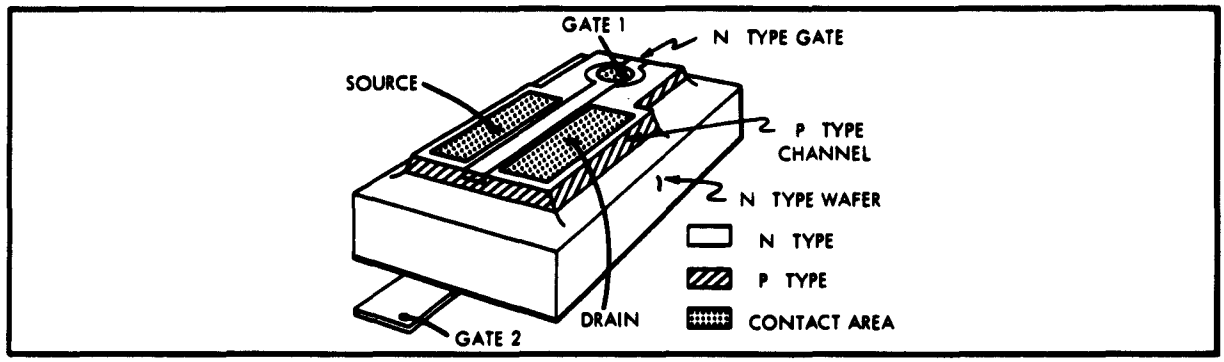


Figure 9. X346-Field-Effect Transistor

channel impurity concentration by using alloyed gates; however, far better control of the length, thickness, and width of the channel can be achieved by using diffusion techniques.

The devices constructed in this program have a diffused structure. Fabrication techniques are similar to those used in making a diffused-base, diffused-emitter bipolar transistor.

The necessary photographic negatives for the three-basic UNIFET designs were completed. These devices were assigned the experimental numbers X-346, X-347, and X-348.

The X-346 structure is shown in Figure 9. Electrical characteristics of some of these units are given in Table 1. The channel width-to-length ratio of this pattern is approximately 30. The diffused gate stripe crosses the mesa and is exposed at each end. This structure has a very short surface path from the Gate 1 to Gate 2, thus increasing the probability of undesired front-gate to back-gate leakage. This particular problem was eliminated in the X-347 pattern.

The X-347 structure is shown in Figure 10. In this pattern the diffused gate region encloses the drain, and is not exposed at the edge of the mesa. Contact areas were reduced to the minimum necessary to provide a low resistance contact to the source and drain regions. The channel width-to-length ratio is 100. Although the mesa area of this unit is no larger than that of the X-346, the g_{mo} is about three times that of the X-346. The characteristics of a few X-347's are listed in Table 1.

Type X-348 was designed to test the feasibility of high-power operation. The pattern, shown in Figure 11, was laid out to give maximum channel width-to-length ratio with minimum complication in construction. No high concentration diffused gate region is employed in this unit. The channel length is 1 mil and the channel width is 850 mils. Analysis indicates that the following characteristics should be realized with this structure.

g_{mo} = 15,000 micromhos $\quad V_P$ = 10 volts

I_{DSS} = 100 milliamperes $\quad BV_{DGO}$ = 100 volts.

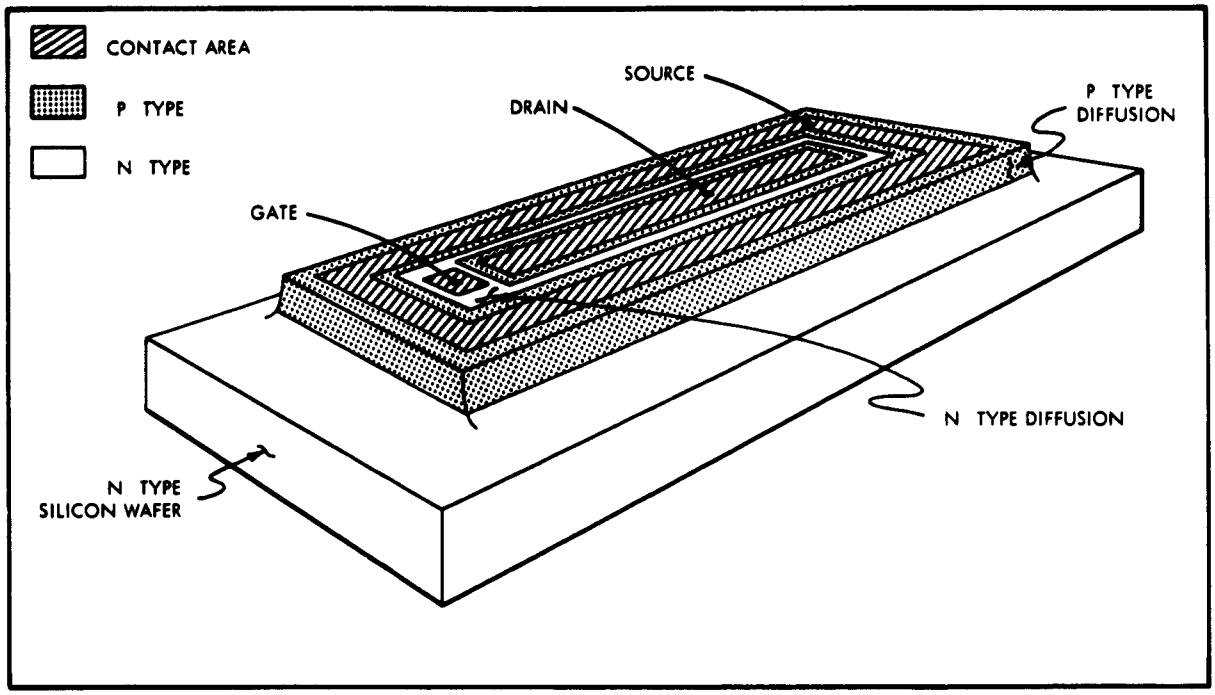


Figure 10. X-347 Unipolar Field-Effect Transistor

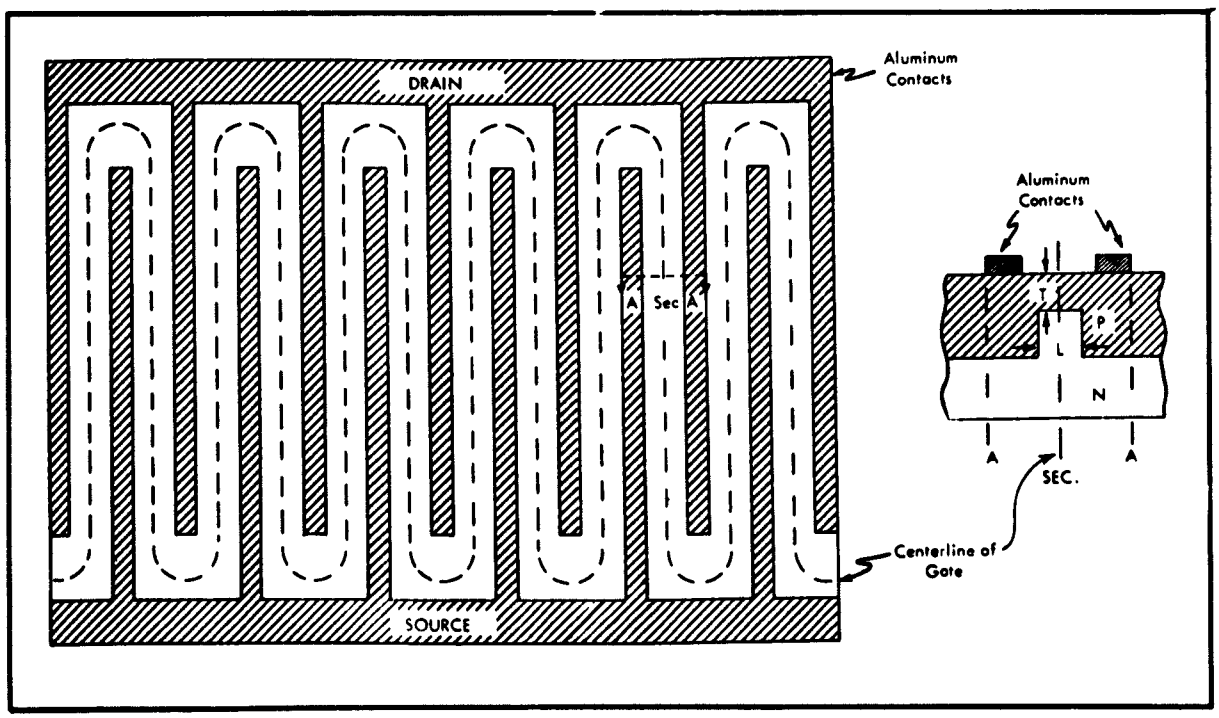


Figure 11. X-348 Field-Effect Transistor

TABLE 1

UNIFET PARAMETERS

Electrical parameters of some of the Type X-346 and Type X-347 UNIFETS are tabulated below:

Device		Diffusion	V_p	g_{mo}	I_{DSS}	I_{GO}	$g_m/V_p I_{DSS}$
Type	Unit No.	Run No.	Volts	μmho	ma	μamps	10^{-3} mho/watt
X-346	1	AF8B	11	4[illegible]	2.6	0.094	1.54
X-346	2	AF8B	11.2	542	2.3	1.45	2.10
X-346	3	AF8B	11.7	418	2.85	1.03	1.25
X-346	4	AF8B	10.3	386	2.02	0.0022	1.86
X-346	5	AF8B	---*	462	2.65	5*	---
X-346	6	AF8B	10.8	435	2.23	0.54	1.98
X-346	7	AF8B	---*	360	2.2	0.03	---
X-347	42	SDE9	2.5	1100	1.3	<1.0	335
X-347	43	SDE9	3.0	1200	1.8	1.0	222
X-347	45	SDE9	3.0	1300	1.75	<1.0	248
X-347	9	SDE9	4.5	900	1.1	<1	182
X-347	19	SDE10	5.0	1800	4.25	<1.0	85
X-347	34	SDE10	5.0	1800	4.8	1.0	75
X-347	38	SDE10	4.5	1800	4.0	<1.0	100

*erratic

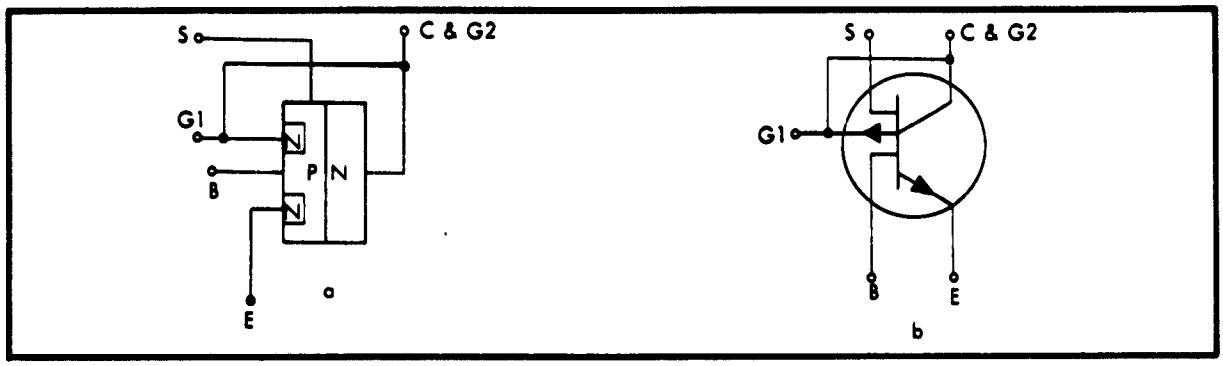


Figure 12. Pictorial and Schematic Symbols for BIFET

2.3.3 Bipolar Field-Effect Transistor (BIFET)

The bipolar field effect transistor was conceived from work on the unipolar field-effect transistor. The BIFET utilizes an electrical field to control the conductance of a majority carrier channel coupled by a junction to an emitter region. The channel separates the emitter region from a surrounding collector region. Useful current results at the collector region that is a function of the majority carrier channel conductance. Internal feedback occurs because the electrical field, due to the bias voltage at the collecting junction, causes the depletion layer to extend into the majority carrier channel, thereby controlling its conductance.

External connections to the internal regions are shown in Figure 12.a. and the schematic of the unit in Figure 12.b. Electrical characteristics can be determined by considering the BIFET a combination UNIFET coupled to a bipolar transistor, as shown in Figure 13.

Figure 14 shows collector output characteristics of a BIFET with source voltage as a variable parameter. This bistable characteristic may be obtained from graphical combinations of the transistor and UNIFET characteristics. Points A and B of the collector characteristic (Figure 14) are the two stable operating points for that load line. The BIFET can be triggered from one state to another with a suitable input at source, S, the base, B, or front gate, G_1.

Regenerative action occurs when it is connected with collector or emitter grounded. Switching times for these configurations are given in ASD Technical Note 61-120.

BIFET structures which were fabricated are shown in Figures 15 and 16.

2.3.4 Induced-Channel Field-Effect Transistor (INDUCHAFET)

The induced-channel field-effect transistor was investigated as a possible component for semiconductor networks. Required coupling capacity for low audio frequencies is easily within the semiconductor network size limitation because of the input resistance (approximately 10^{12}).

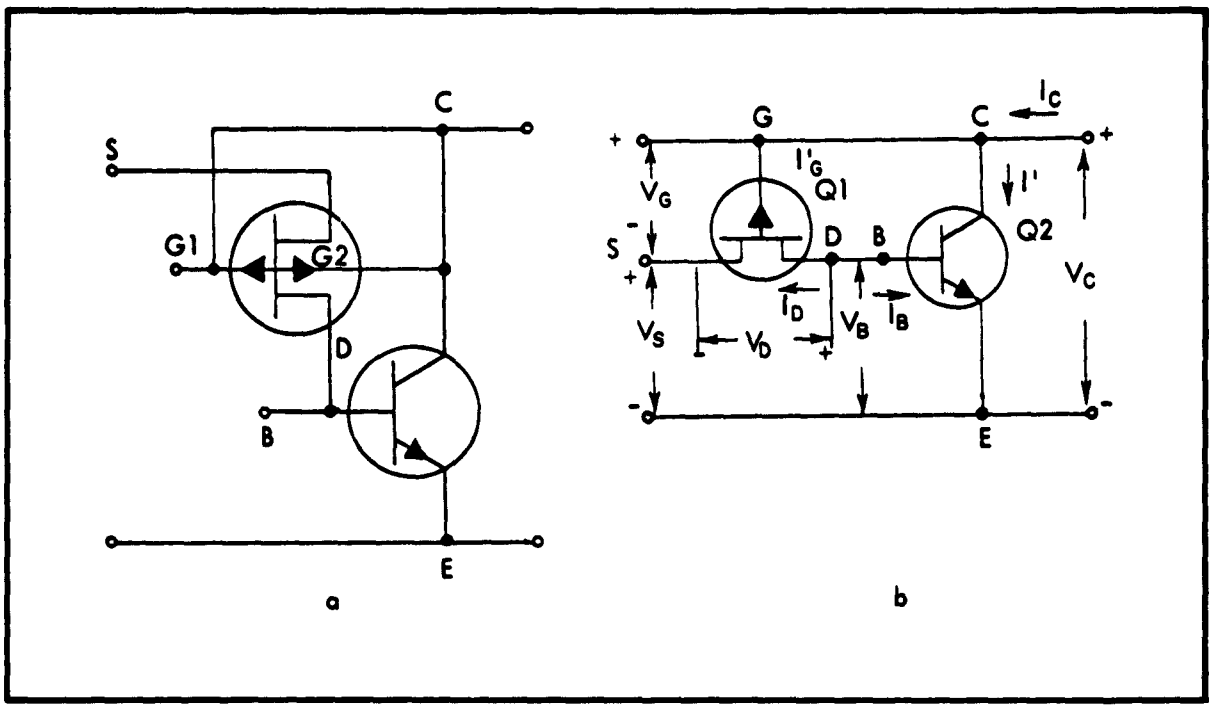


Figure 13. Simulated BIFET Schematic

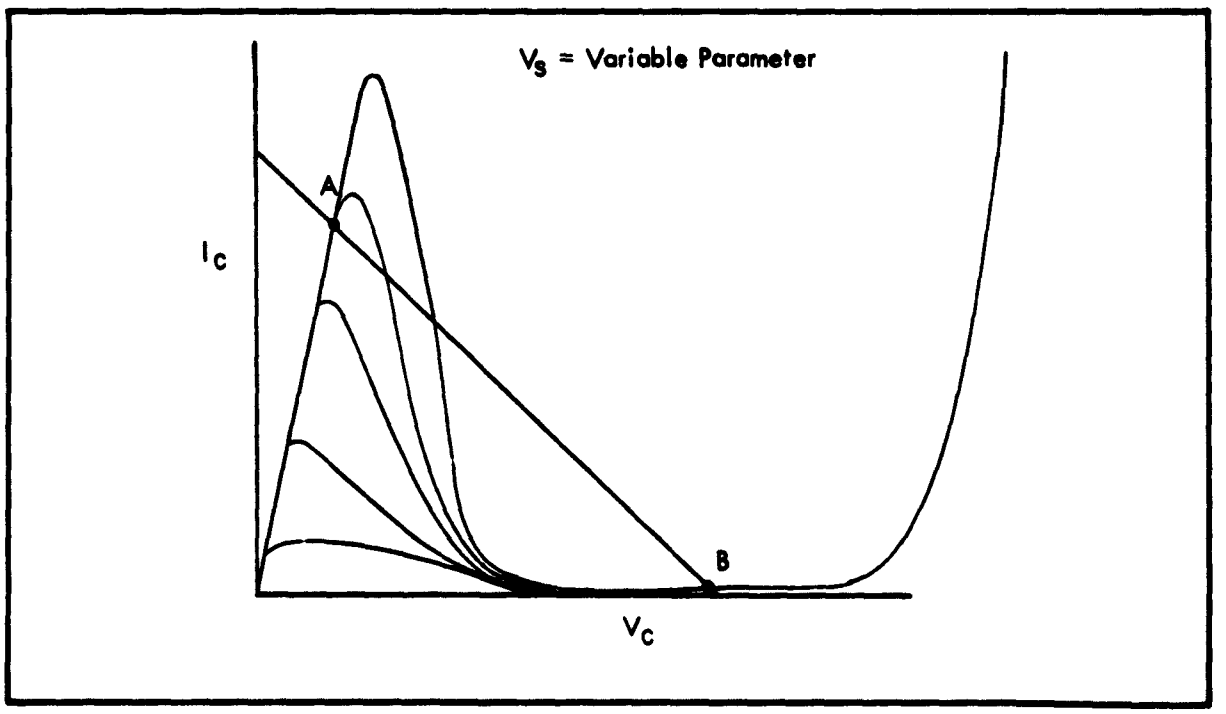


Figure 14. Collector Output Characteristics of BIFET

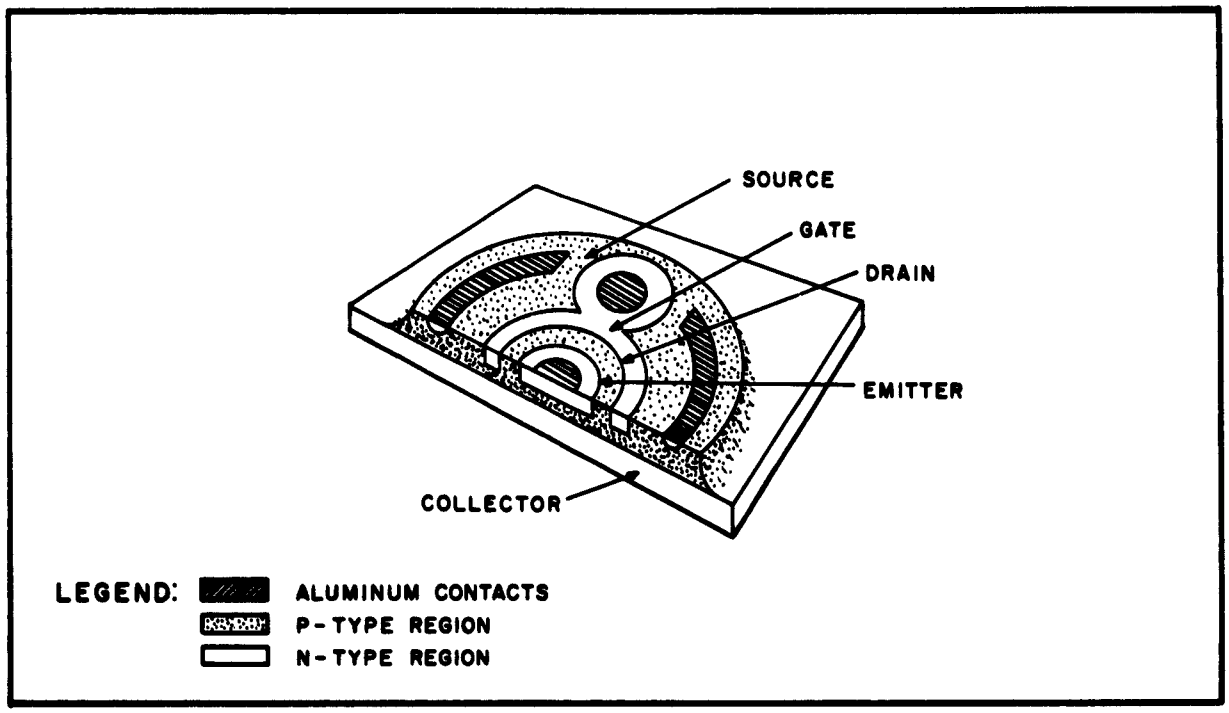


Figure 15. BIFET X-349A

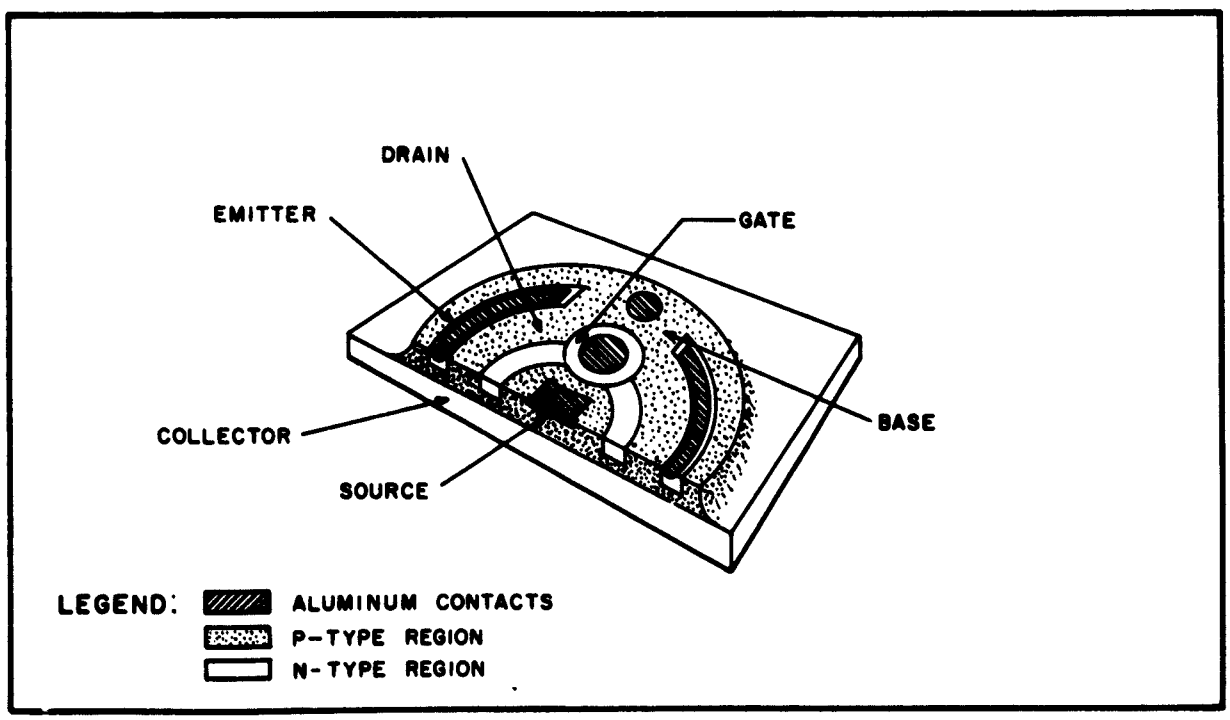


Figure 16. BIFET X-349B

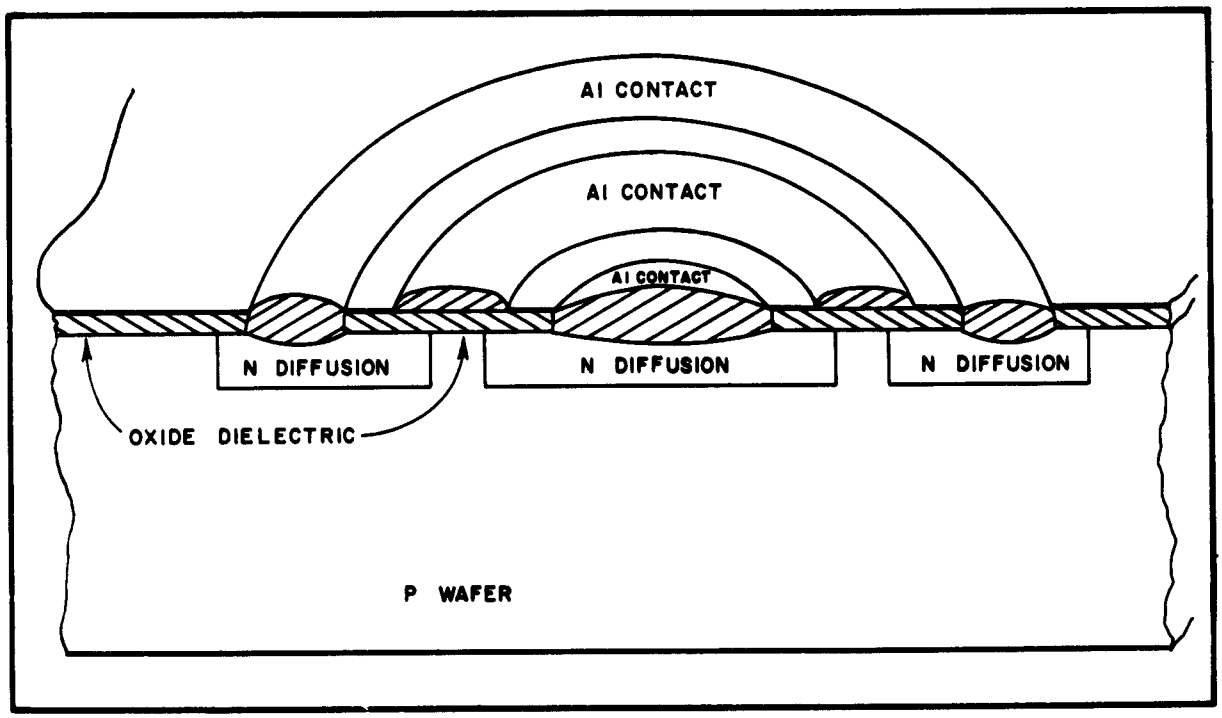


Figure 17. Circular-Geometry, Induced-Channel, Field-Effect Transistor

The starting material can be either P- or N-type. A selective diffusion of the opposite type is then required. Only bulk wafers with no previous diffusions have been used, but it appears that devices can also be fabricated on a diffused layer if necessary for integrated circuits.

Devices have been fabricated using both circular and rectangular geometry. Figure 17 shows a circular device.

The INDUCHAFET differs from the conventional UNIFET in that drain current is ideally zero for zero gate voltage. For a P-type channel, negative gate voltage has no effect; drain current increases with positive gate voltage. In practice an initial channel may be produced during diffusion, allowing an initial current to flow. This will be reduced by negative gate voltages and increased by positive gate voltages. The initial current can be adjusted by applying a potential to the substrate. Improved fabrication techniques are needed for eliminating or controlling this channel.

The dielectric of the INDUCHAFET is very important. It should have high dielectric strength and a high dielectric constant. In addition, it must be formed on or applied to the silicon substrate in an extremely thin, continuous layer. Present fabrication techniques require the selective removal of the dielectric film to make the source and drain contacts. Additional development work is needed on the dielectric.

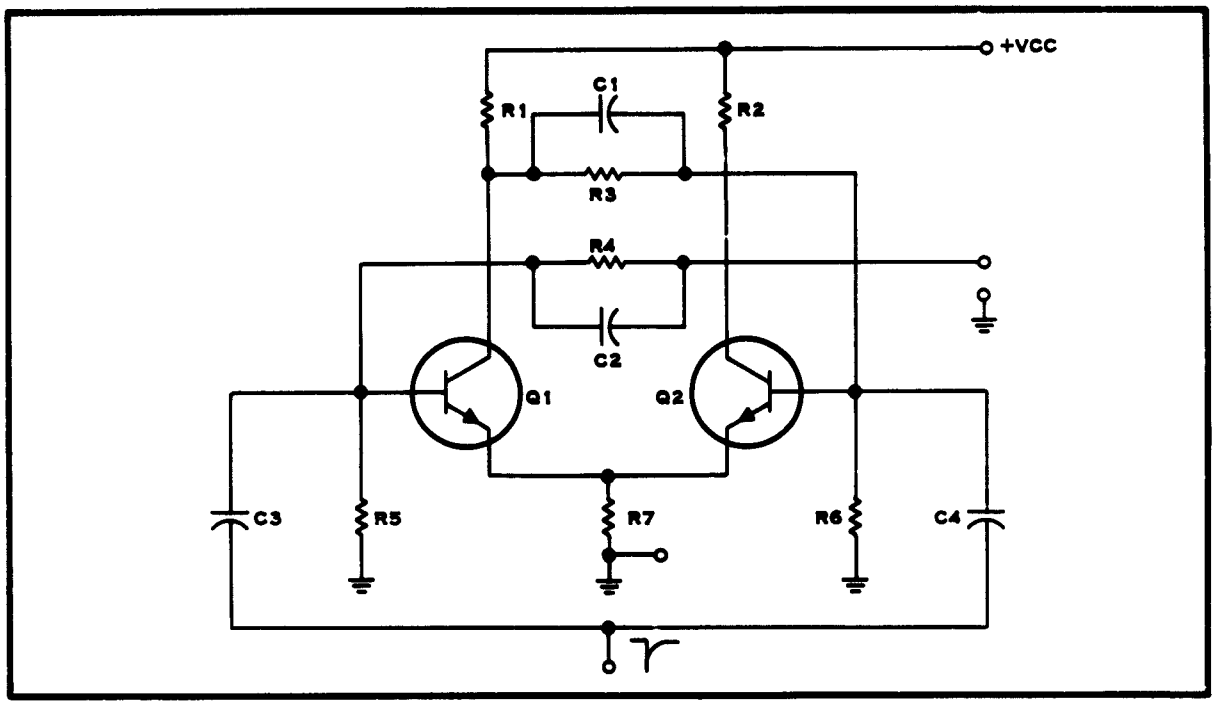


Figure 18. Simple Transistor Flip-Flop Circuit

2.4 Advanced Concepts

2.4.1 Controlled-Field Network

A brief study of memory circuits led to the concept of utilizing controlled fields for circuit functions. In this concept the resistors utilized in a conventional electronic circuit are replaced with a single thin sheet of material having uniform sheet resistance, for example, a thin slab of silicon. Active regions are formed by diffusion at selected locations on the silicon slab. The interaction between the active elements is a function of their location upon the slab. This concept is best explained by an illustration of a circuit function realized in this manner.

The circuit diagram of a simple flip-flop, constructed from conventional components is shown in Figure 18. An approximate equivalent circuit may be constructed by substituting connections, at the proper points, to a single conducting sheet for the resistors. This type of arrangement is shown in Figure 19. Resistors, corresponding to those shown in Figure 18, are indicated in this sketch. In addition, an equivalent resistance exists from each connection on the conducting sheet to all the other connections. This condition is illustrated in Figure 20.

For steady-state conditions (i.e., one transistor in saturation and the other cut-off) and a specified supply voltage, external currents and potentials to the ground plane are determined by the size, shape and conductivity of the sheet and by location and size of the connections to the sheet.

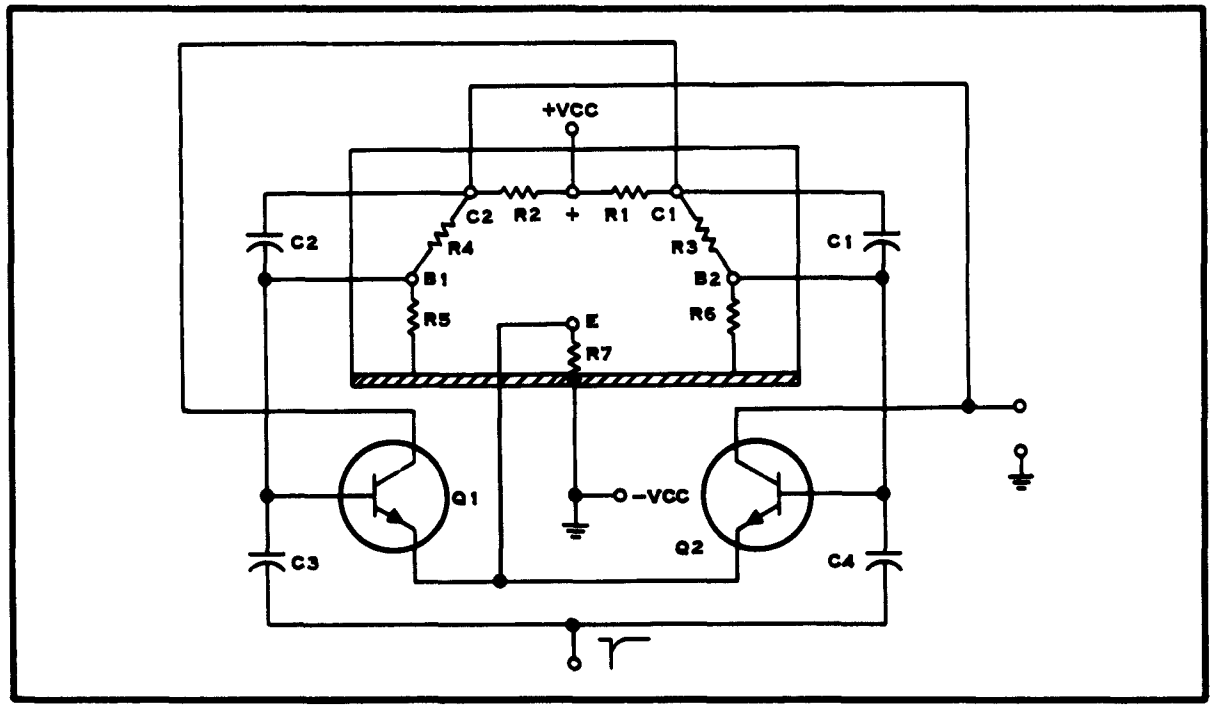


Figure 19. Resistor Connections for a Controlled-Field Flip-Flop

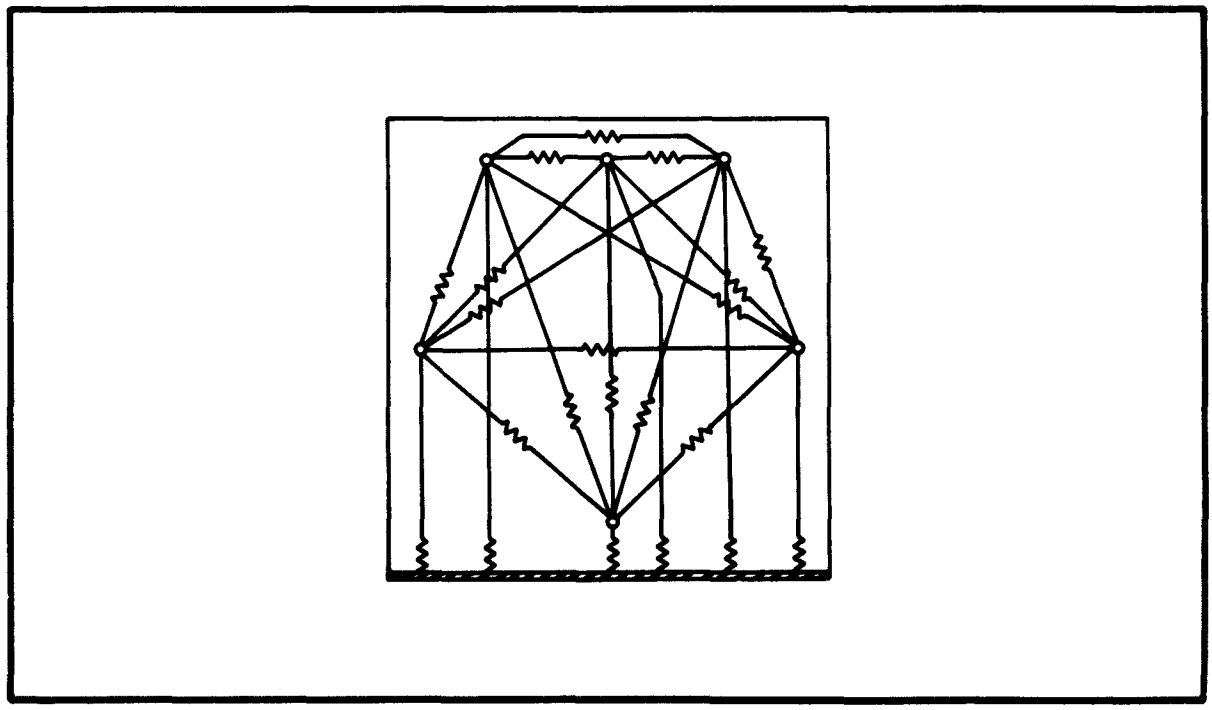


Figure 20. Equivalent Resistances Between Connections for a Controlled-Field Flip-Flop

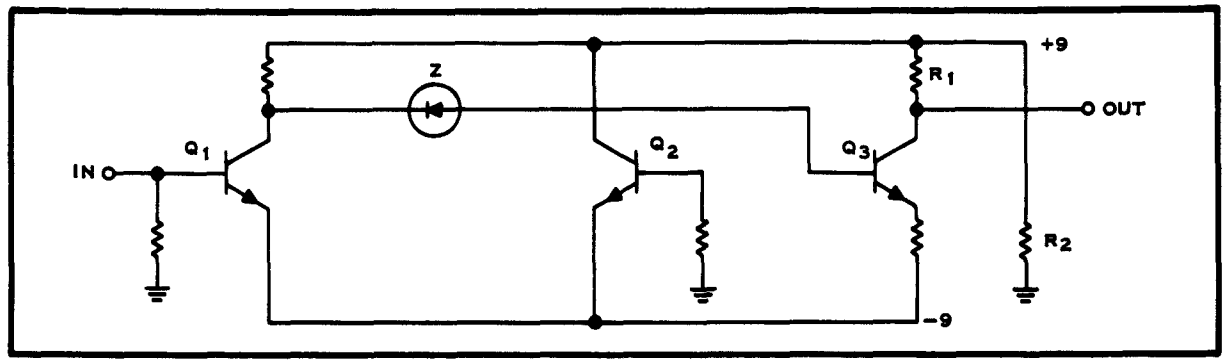


Figure 21. Circuit Using Thermally Generated Voltages to Stabilize the Bias Point

Analytical techniques were developed, using a system of images, to calculate these currents and potentials. The circuit was set up using resistance paper as the conducting sheet. Calculated values were in agreement with values measured on the analogue.

2.4.2 Thermal Feedback

A circuit using thermally generated voltages to stabilize the bias point was tested. This circuit is shown in Figure 21. The differential transistors Q_1 and Q_2 are in thermal contact with R_1 and R_2 respectively but thermally isolated from each other. If for some reason the bias current in the output transistor Q_3 increases, the temperature of R_1 will increase, lowering V_{BE} of Q_1. Since Q_1 is differentially connected to Q_2, this will lower the current in Q_1 and tend to return the output bias to its original value. Resistor R_2 is used to set a thermal reference for Q_2. Thus, if R_1 and R_2 are equal and the V_{BE}'s of Q_1 and Q_2 are matched, the circuit output will be biased at approximately ground potential, allowing maximum output voltage swing. Essentially this circuit has a negative feedback loop around it. However, since the signal through this loop depends on the thermal properties of the material, high frequency signals are attenuated by the thermal capacity of the material. Thus, at dc or low frequencies the negative feedback loop is operative and the bias point is stabilized. At signal frequencies, the feedback is inoperative and the circuit has full open loop gain.

The circuit was tested using the element shown in Figure 22. Response of the amplifier to a 1-cycle square wave is shown in Figure 23. The mid-frequency ac gain is approximately five times larger than the dc gain, or the bias point is stabilized by 14 db of negative feedback. (The mid-frequency gain is proportional to the amplitude of the leading edge of the pulse and the dc gain is proportional to the amplitude of response after the time-constant decay). Since the signal decays with a time constant of 20 milliseconds, the circuit should have a low-frequency break at 50 cycles.

The amount of bias stabilization could be increased by increasing the resistance between the resistor bars and the package.

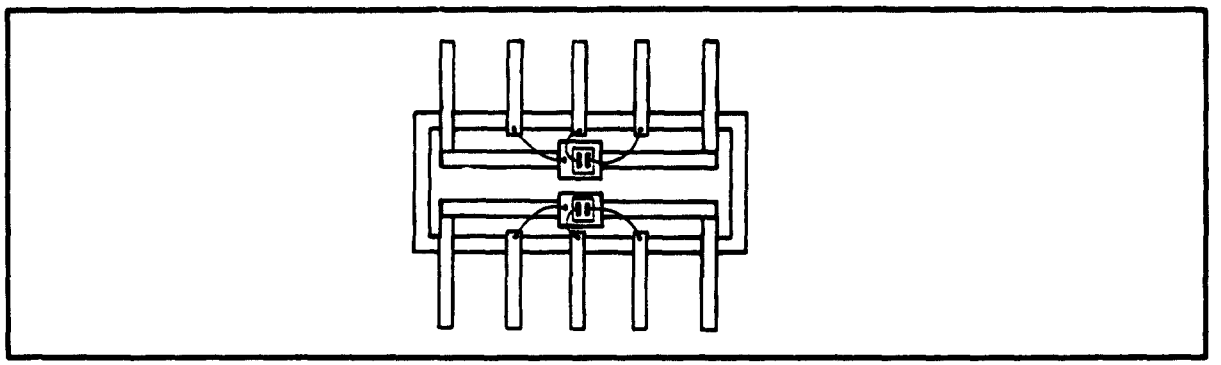


Figure 22. Element Used to Test the Circuit

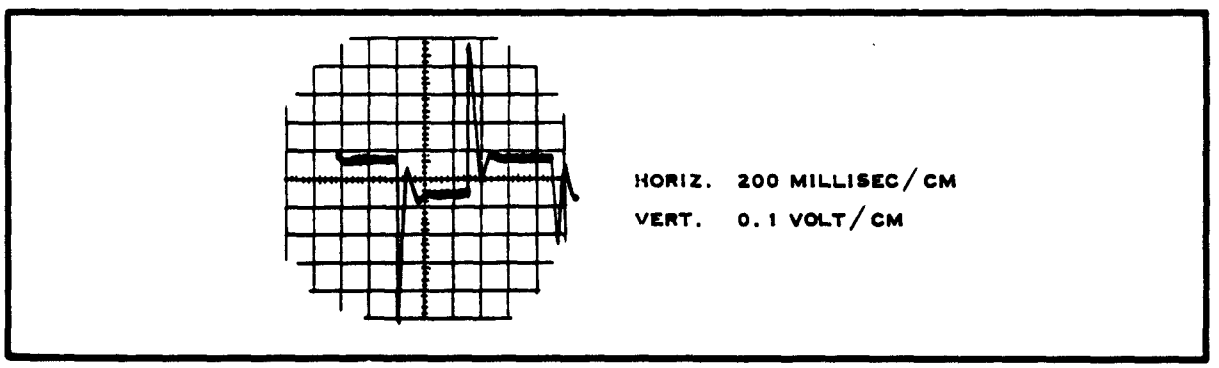


Figure 23. Response of the Amplifier to a 1-Cycle Square Wave

SECTION III

CIRCUIT FUNCTIONS

3.1 Introduction

Design theory and technology have been developed for fabricating a variety of circuit elements from single crystal silicon. These elements were fabricated individually and evaluated as discussed in the preceding paragraphs. However, the main purpose of developing these components was for use in fabricating electronic circuit functions from single crystal silicon. These functional electronic blocks are herein referred to as semiconductor networks.

A listing of the semiconductor networks, and their characteristics, appears in Table 2; Table 3 shows the circuit elements used in each. These networks are discussed further in the following paragraphs.

3.2 Amplifiers

Conventional transistor audio-frequency amplifier circuits are difficult to build as semiconductor networks since they usually employ large bypass and coupling capacitors.

However, with a slight change in circuitry these functions can be performed by other components which fit nicely into the semiconductor network concept. For instance, the inter-stage coupling capacitors can be replaced with zener diodes. Also, emitter resistors, and thus emitter bypass capacitors, are not required for dc stability if dc negative feedback is used around the amplifier. Finally, large input capacitors are not required if the amplifier has a high input impedance.

3.2.1 Audio Amplifier A-1

All three of the above design concepts are incorporated in the amplifier shown in Figure 24, designated as A-1.

The unipolar field-effect transistor (UNIFET) gives this amplifier a high-input impedance. Since the input impedance of this transistor is essentially that of a reverse-biased diode, it should be in the tens of megohm range. Thus, a small capacitor (e.g., 1000 pf) will give a response in the low audio range.

The amplifier has a voltage amplification that is fairly independent of the transistor h_{fe} and the field-effect g_m. Figure 25 shows the calculated A_v of the amplifier as a function of the h_{fe} of the bipolar transistors for various g_m values of the unipolar transistor.

The physical layout of semiconductor network A-1 is shown in Figure 26. All components except the two capacitors are integrated into one silicon bar.

TABLE 2. SEMICONDUCTOR NETWORK DESIGNS

	Function	Type	Frequency	Av (db)	Z_{IN}	Z_{OUT}
AMPLIFIER	Low-level	A-2	100 cps–20 kc	40 db	10 meg	10 k
		A-7	dc–1.5 mc	20 db	10 meg	1 k
	Video	A-9	dc–10 mc	20 db	2 k	20 ohms
	Power	A-6	dc–100 kc	20 db	20 k	2 ohms
	(1 watt)	A-10	dc–20 kc	20 db	2 k	2 ohms
	Bandpass	A-8	500 kc	40 db	1.5 k	1.5 k
OSC	Variable AF	O-2	2 kc–20 kc	Voltage-controlled frequency		
	RF	O-3	200 kc–2 mc	Fixed frequency		
	Variable RF	O-4	500 kc-2 mc	Voltage-controlled frequency		
	Ring counter	PC-1	400 kc			
PULSE	Pulse Gen	PC-2	Pulse width–2μsec-200 μsec–Voltage-controlled Rep. rate–10 kc-100 kc–Voltage-controlled			
	Multibibrator	PC-3	30 kc–70 kc	Voltage-controlled		
	Flip-Flop	PC-4	Up to 1 mc			

TABLE 3. SEMICONDUCTOR CIRCUIT ELEMENTS UTILIZED IN SEMICONDUCTOR NETWORK DESIGNS

Network Design Number	Semiconductor Circuit Element									
	Transistors				Diode	Resistors		Capacitors		Distributed-RC Networks
	NPN	PNP	UNIFET	BIFET		Bulk	Diffused	Oxide	Junction	
A-2			X				X	X		
A-6	X	X				X	X			
A-7	X		X			X	X			
A-8	X				X	X	X	X		X
A-9	X	X				X	X			
O-2	X		X			X	X	X		
O-3	X				X	X	X	X		X
O-4	X				X	X	X	X		X
PC-1	X			X		X	X	X		
PC-2			X	X	X	X		X		
PC-3	X		X							
PC-4	X		X		X	X	X	X		

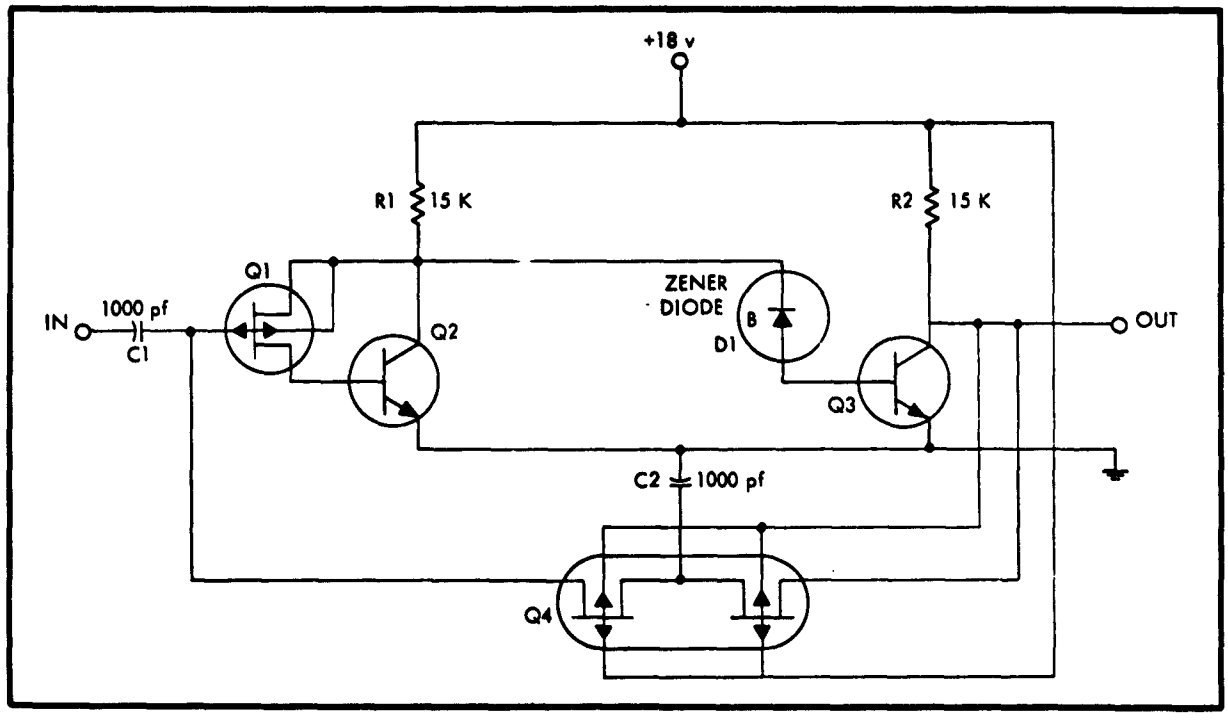


Figure 24. A-1 Audio Amplifier Schematic

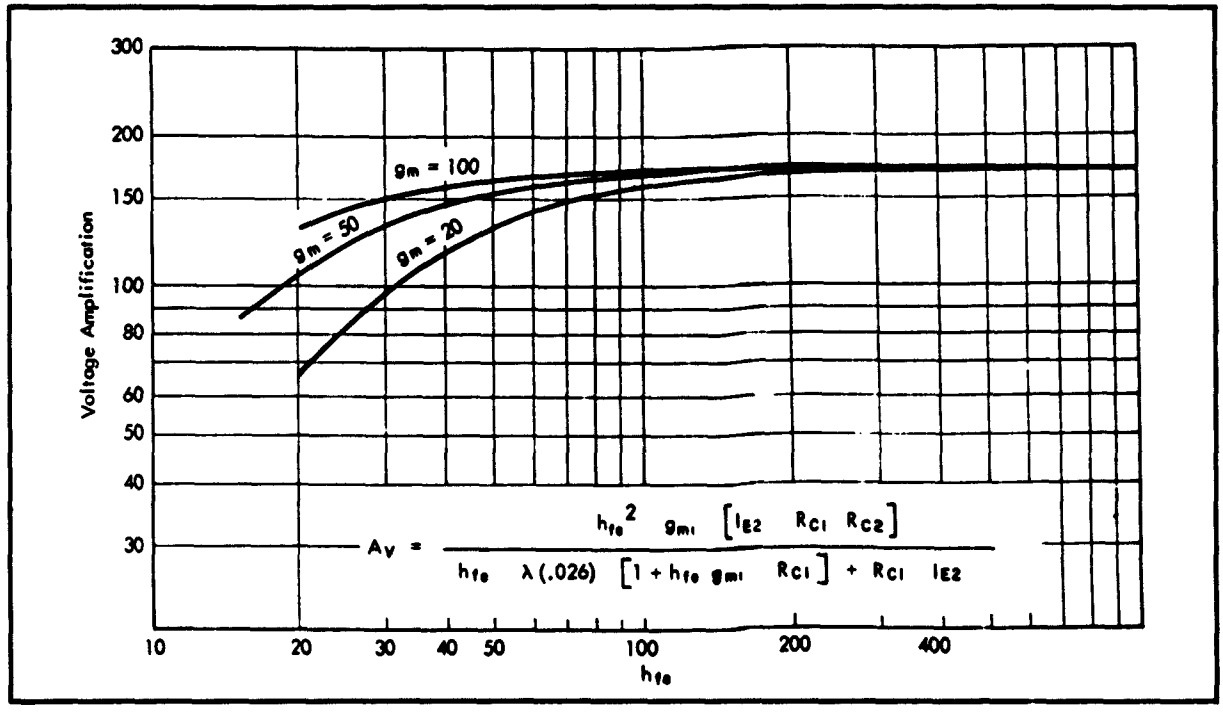


Figure 25. Voltage Amplification of Amplifier A-1

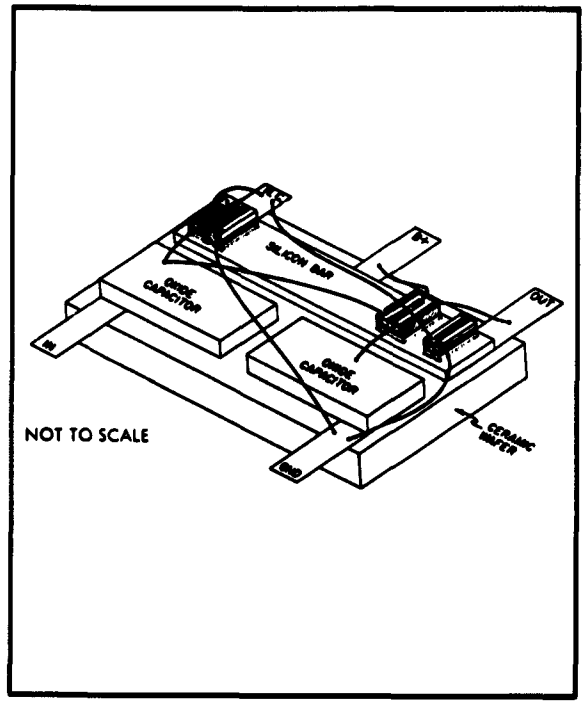


Figure 26. A-1 Semiconductor Network

Several A-1 amplifier bars were processed. For the initial evaluations, a zener diode was patched in externally since the required P-type concentration was not compatible with other diffusions. The amplifier functioned properly except for instability resulting from the feedback loop.

Figure 27 shows a modification of A-1 which has been breadboarded. This circuit was not fabricated as a semiconductor network but appears feasible except for the 0.01 μfd capacitor.

3.2.2 Audio Amplifier A-2

Based on the feasibility of UNIFET (type X-346), a two-stage amplifier using this structure was started. The schematic is shown in Figure 28 and the wafer geometry

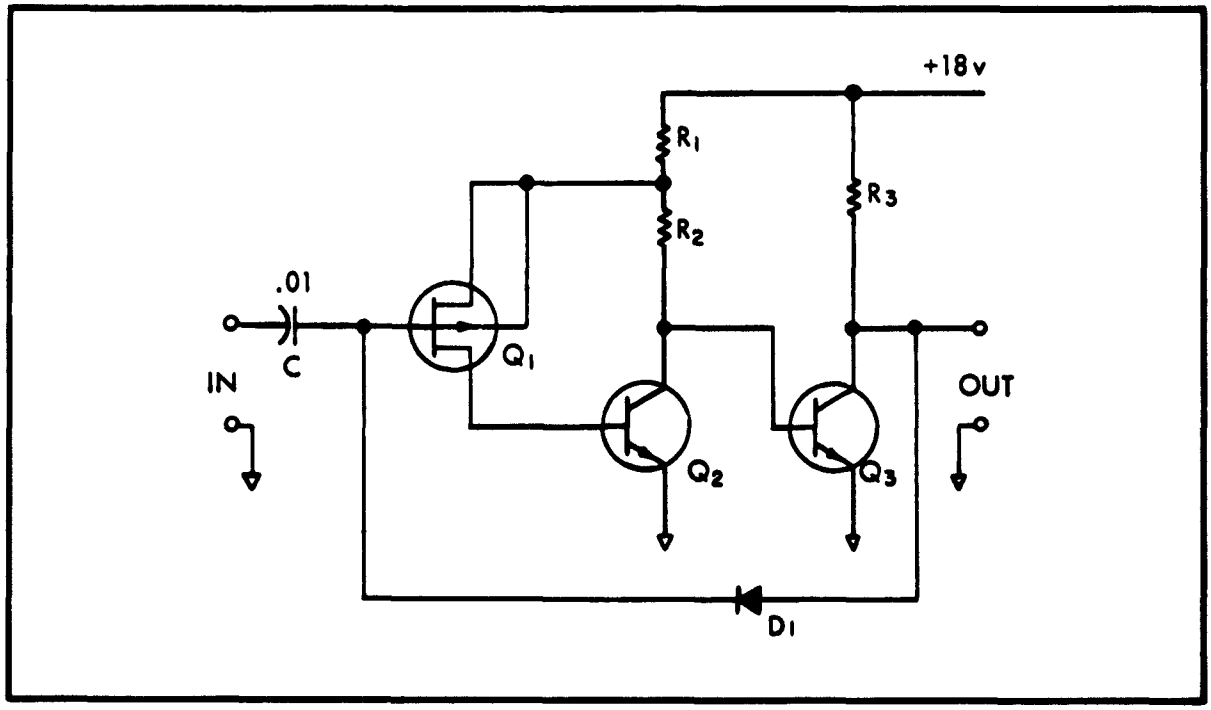


Figure 27. Modified A-1 Schematic

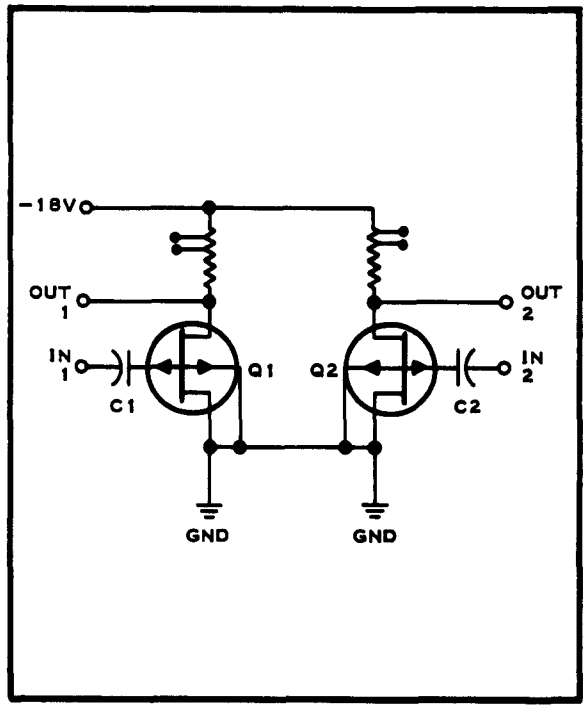


Figure 28. Audio Amplifier A-2

in Figure 29. Figure 30 shows the voltage amplification as a function of frequency for a model of the amplifier, which was delivered to ASD.

No bias stabilization is required for this amplifier; therefore, it is more simple than A-1. This is made possible by formation of the field effect channel and the resistor, in a common P-diffusion, to give temperature compensation.

3.2.3 Power Amplifier A-6

The power amplifier of Figure 31 was designed to give 1-watt output without the use of a transformer or large-value capacitor. Features of the design are

Low zero signal dissipation and high efficiency due to complimentary output.

Low crossover distortion, stable voltage gain, and wide frequency response due to feedback

Low offset voltage due to difference amplifier input.

Feasibility was established when a number of amplifier bars were built which met most of the design specifications. Two were delivered to the Molecular Electronic Branch of ETL/ASD.

3.2.4 Audio-Video Amplifier A-7

This network, shown in Figure 33, is a small-signal, feedback-stabilized, direct-coupled amplifier designed for high-input-impedance preamplifier applications.

Two amplifiers using the layout of Figure 34 were successfully fabricated and delivered to ETL/ASD. Redesign of the circuit should be considered if additional fabrication is contemplated to circumvent problems of diffusion spiking and component tolerance.

3.2.5 Bandpass Amplifier A-8

The schematic diagram for a 500-kc bandpass amplifier is shown in Figure 35. Frequency selectivity is obtained by negative feedback through

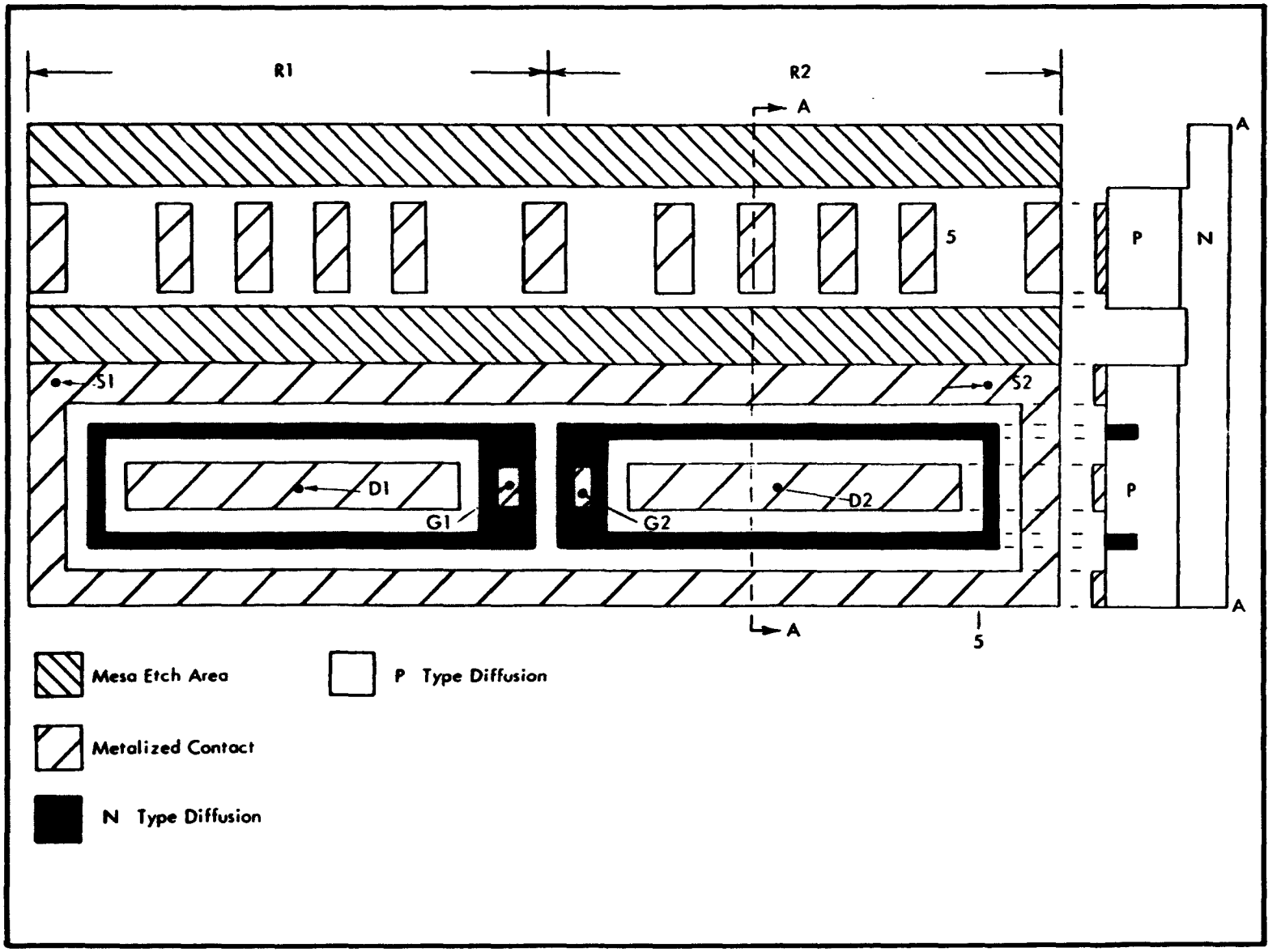


Figure 29. Modified UNIFET Audio Amplifier A-2-A

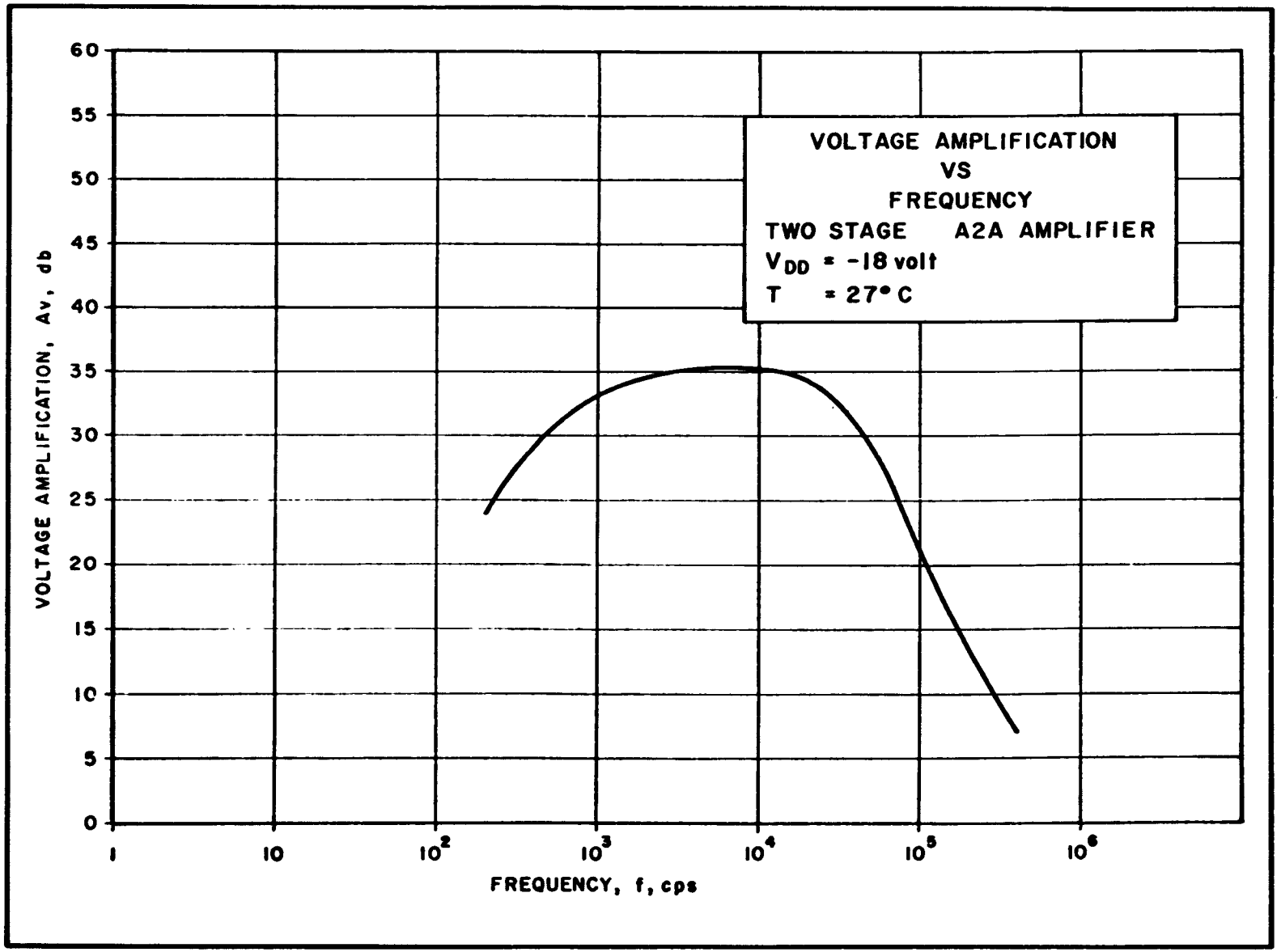


Figure 30. Voltage Amplification Versus Frequency–Two Stage A-2-A Amplifier

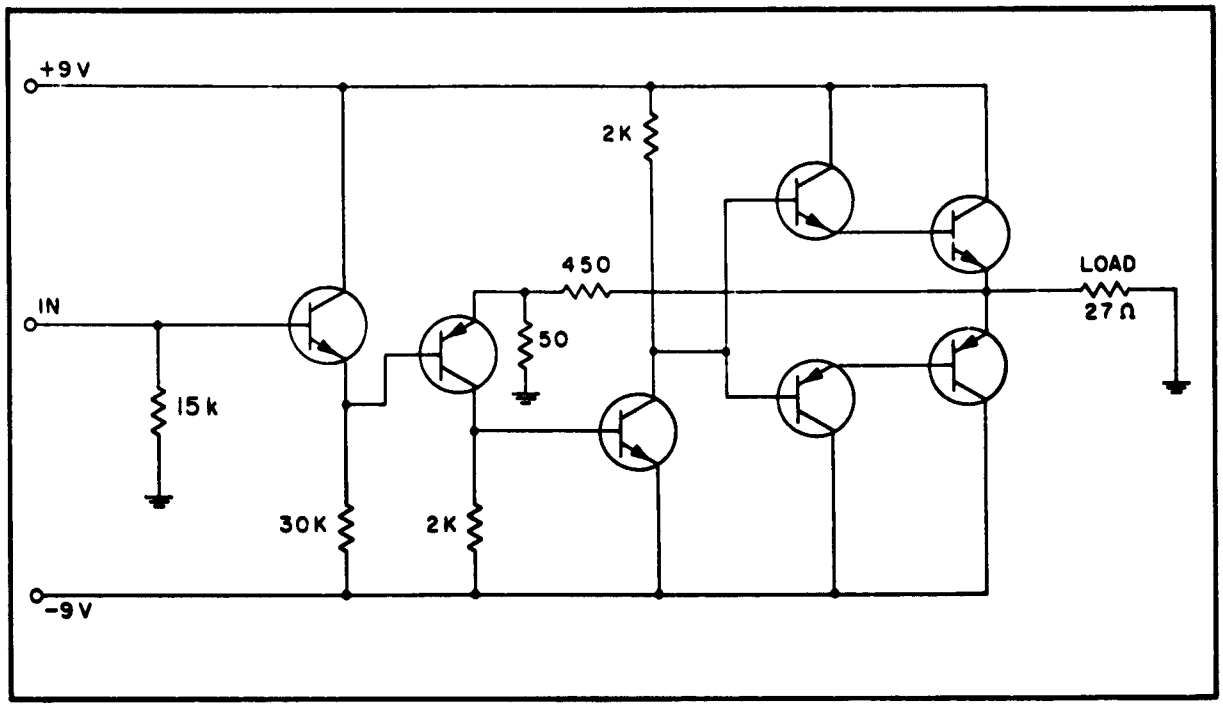


Figure 31. One-Watt Power Amplifier Voltage Gain of 10

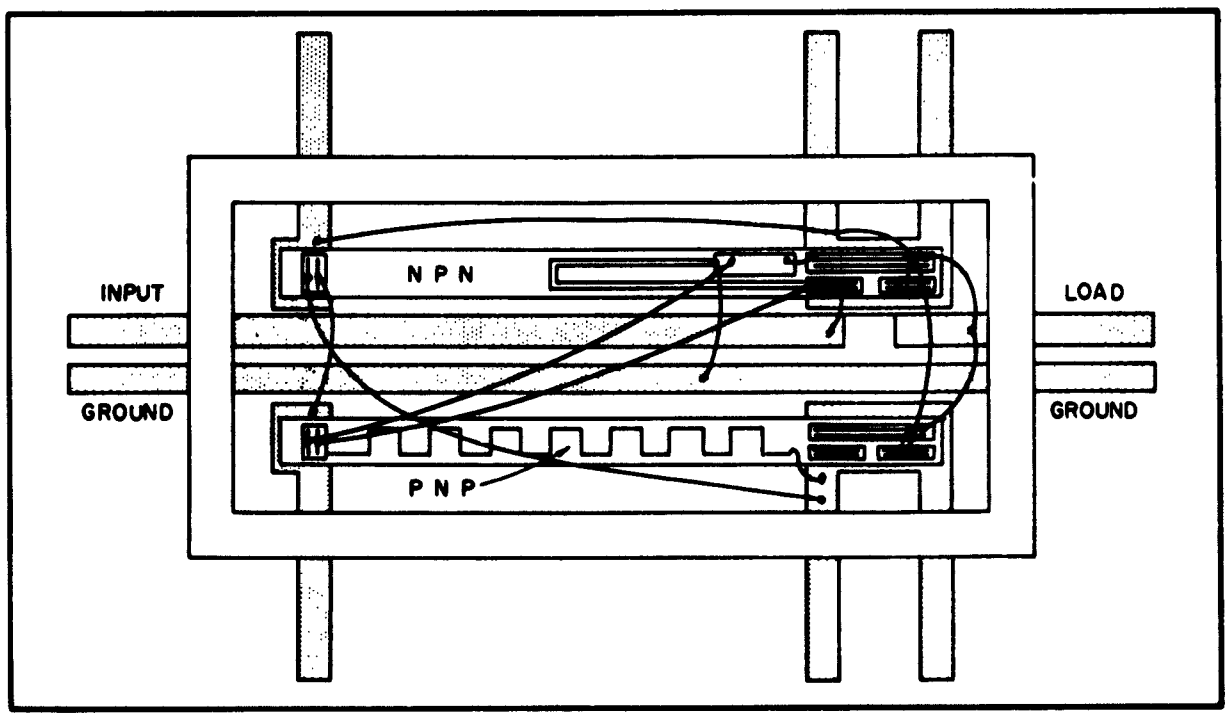


Figure 32. One-Watt Power Amplifier A-6

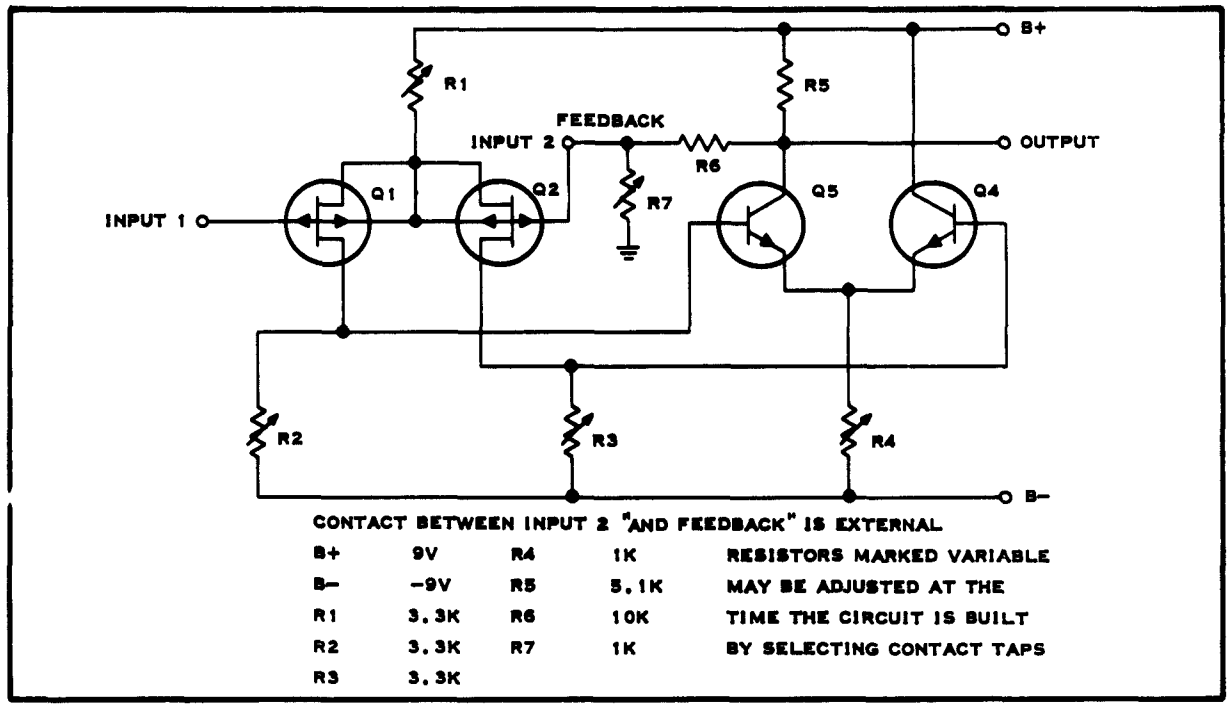


Figure 33. High-Input-Impedance Amplifier Schematic-A-7

a notch filter. The notch filter is contained in one package, shown in Figure 36. The amplifier section is laid out on a single piece of silicon (Figure 37) and mounted in another package. The tuning and input capacitors are mounted in a third package (Figure 38) with all leads brought out for ease of tuning.

A number of good bars of all three types were fabricated. From these an if. strip was fabricated for use in a breadboard radio receiver. Frequency response for the if. strip is shown in Figure 39. Drift of frequency with temperature was attributed to the bulk-resistor notch filter. A gallium-diffused resistor for the notch filter should minimize this problem.

3.2.6 Video Amplifier A-9

A breadboard for a video amplifier was built and tested. The circuit, shown in Figure 40, is very similar to the driving circuit of the A-6. As a semiconductor network, the amplifier would have an NPN bar and a standard production PNP chip.

3.2.7 One-Watt Power Amplifier A-10

This amplifier is an all NPN power amplifier with performance specifications similar to A-6. The circuit is shown in Figure 41 and the physical layout in Figure 42.

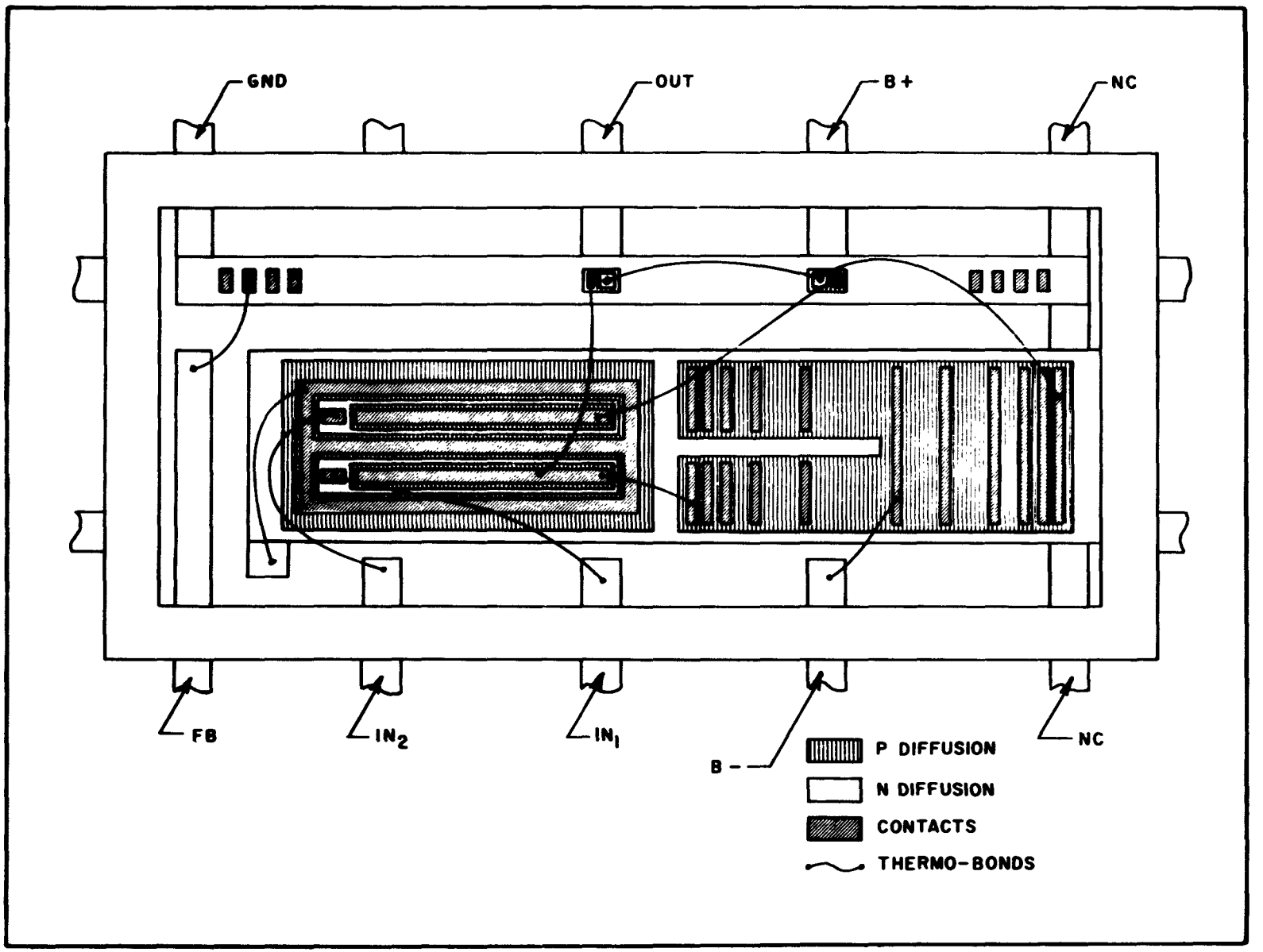


Figure 34. Physical Layout for A-7

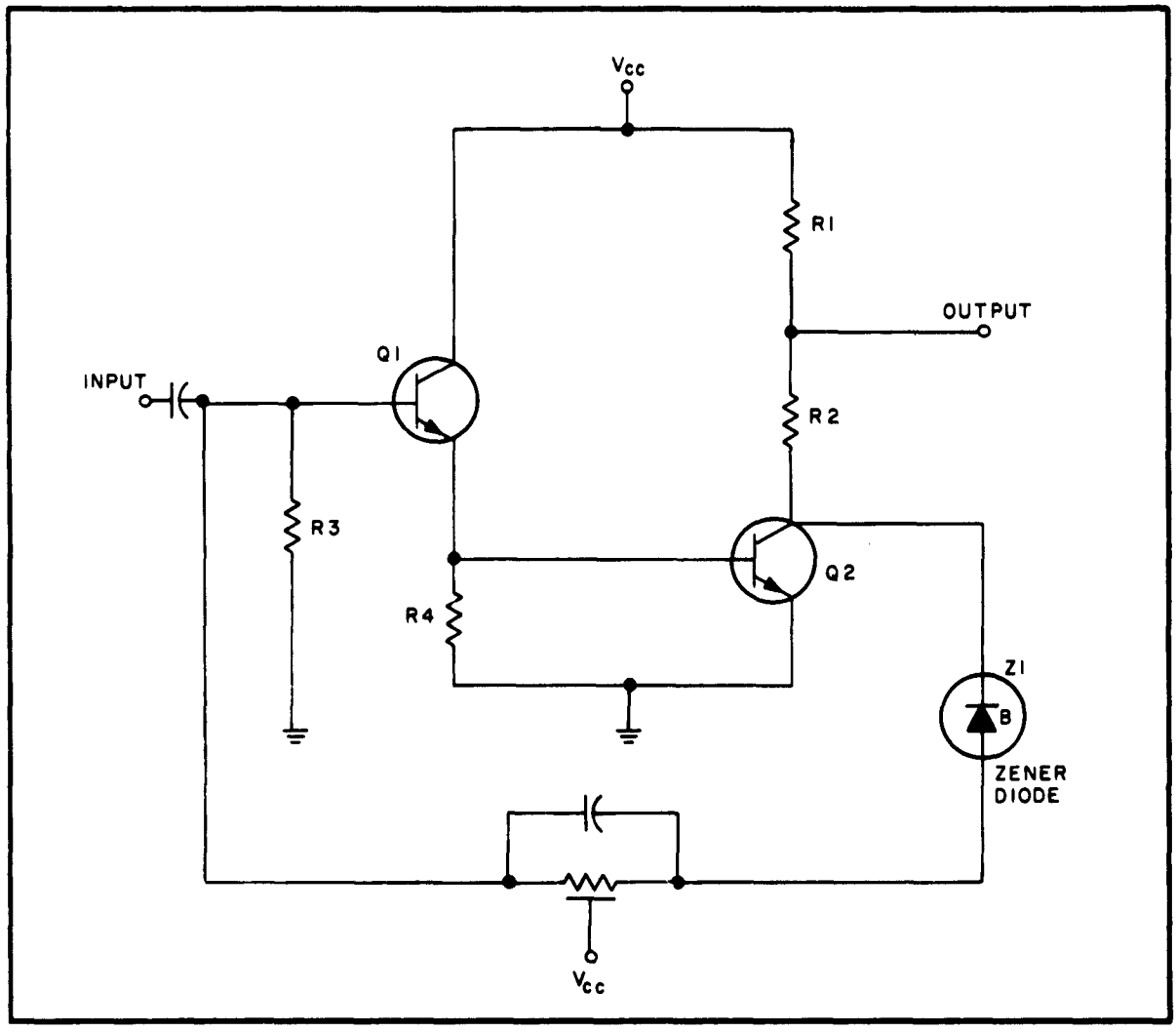


Figure 35. Circuit Diagram of A-8 Amplifier

Characteristics of breadboard models were encouraging. A semiconductor network version has not been constructed; however, it appears feasible using planar and epitaxial techniques.

3.3 Oscillators

Component limitations presently imposed by the fabrication techniques of semiconductor networks restrict the oscillator circuits which may be adapted to this approach. Circuits have been selected which utilize RC circuits for the frequency controlling elements and which require a minimum number of components.

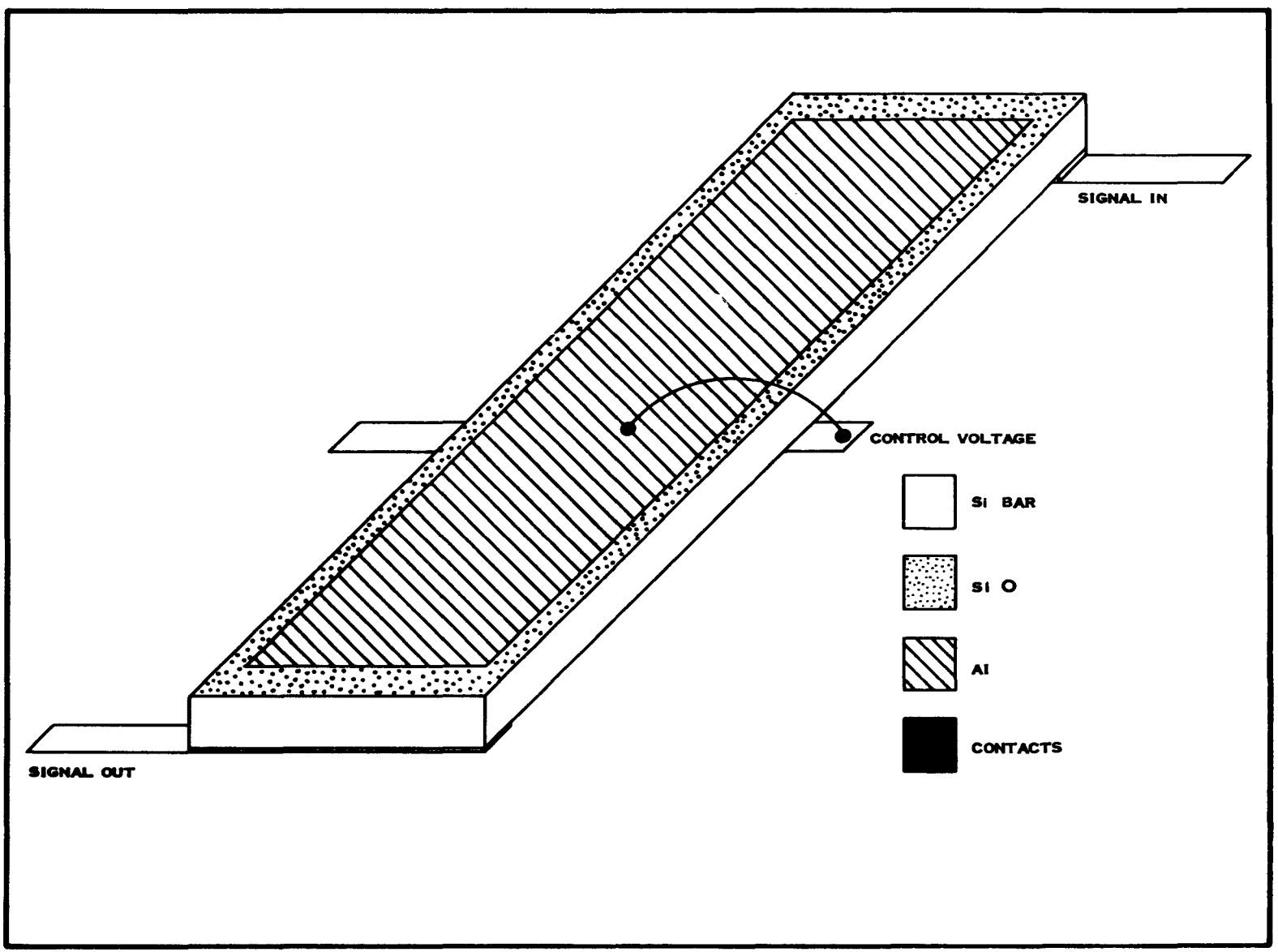


Figure 36. Bulk Resistor Notch Filter A-8 Amplifier Bar

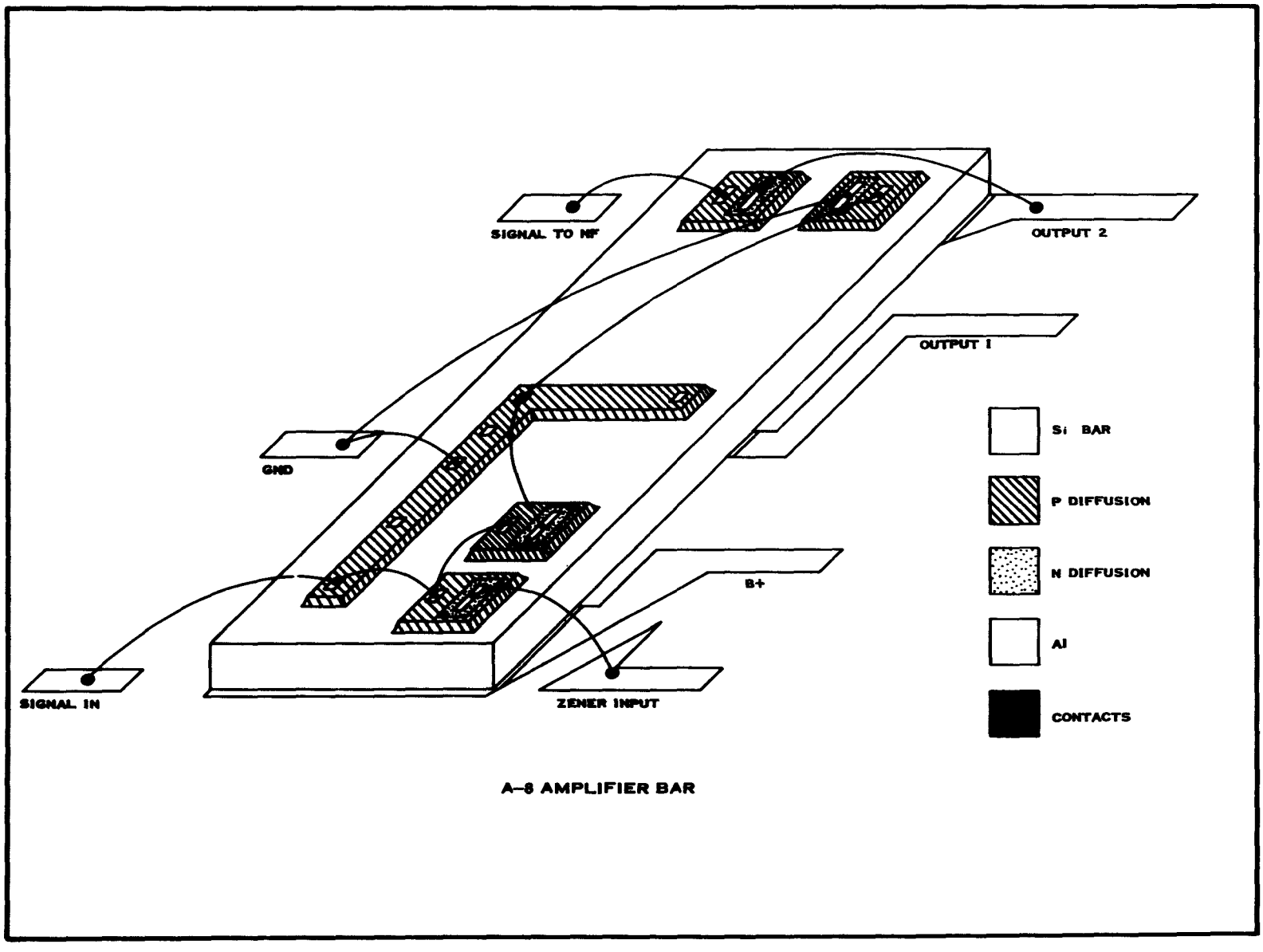


Figure 37. A-8 Amplifier Bar

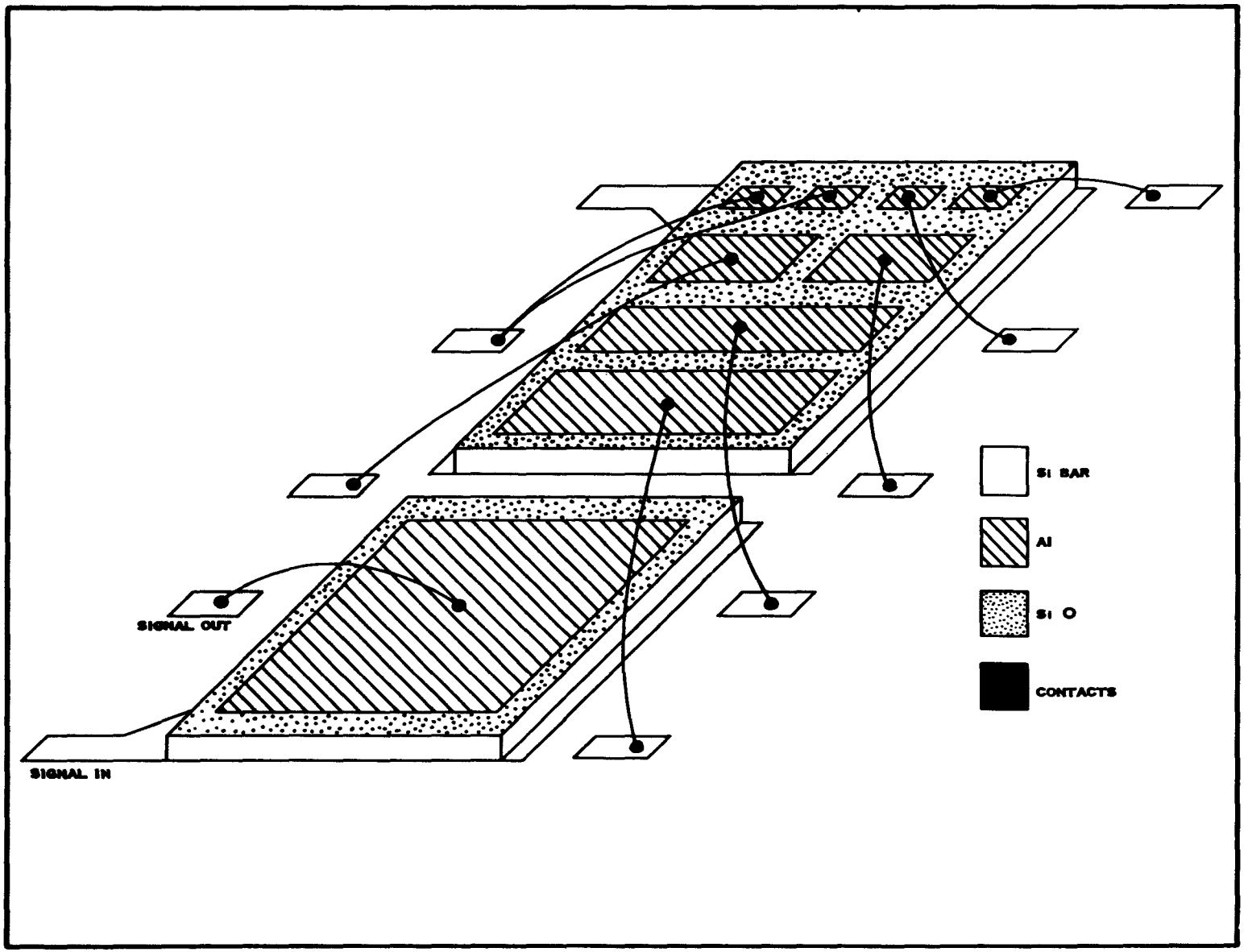


Figure 38. Tuning and Input Capacitor

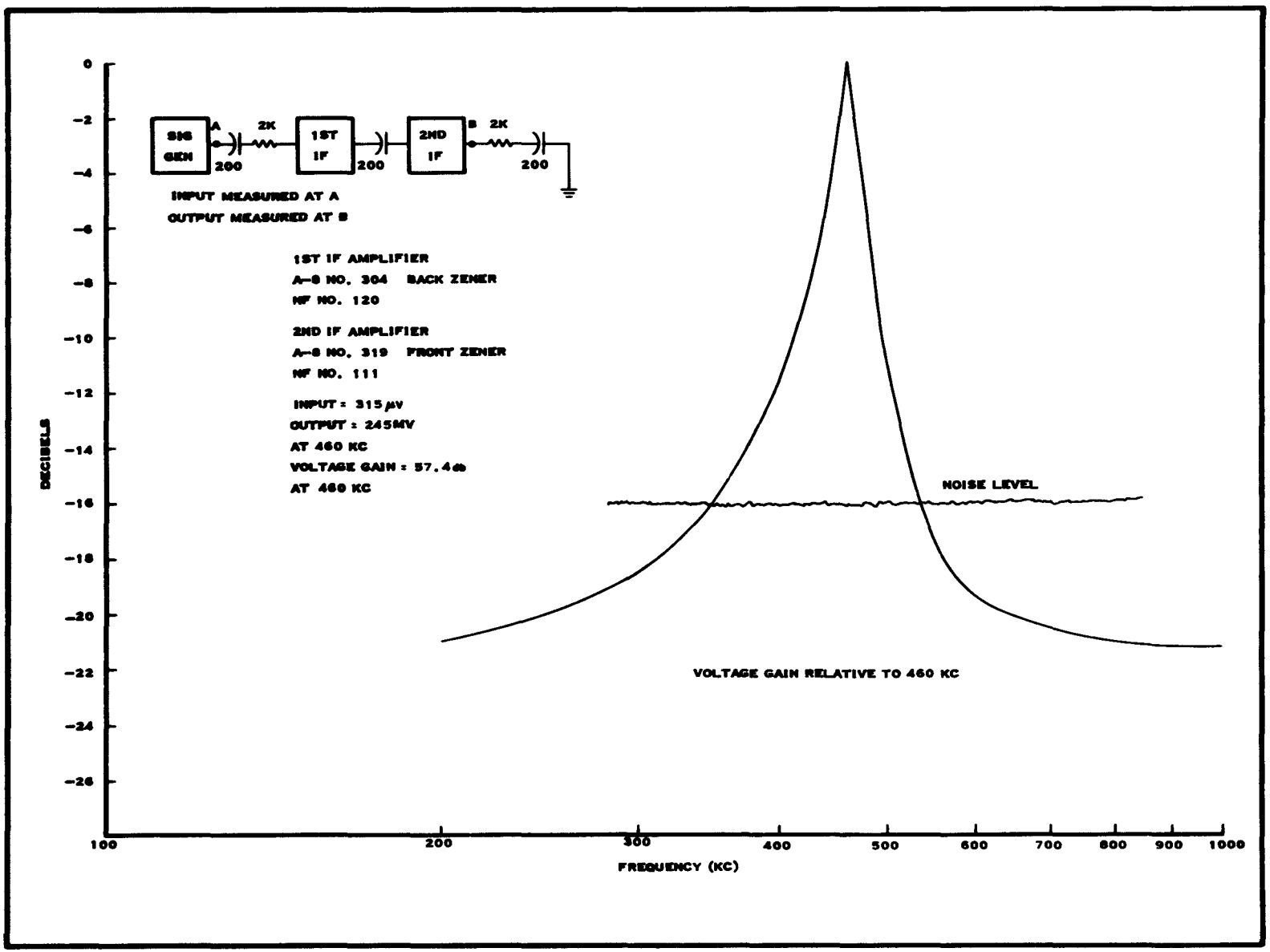


Figure 39. Voltage Gain Versus Frequency

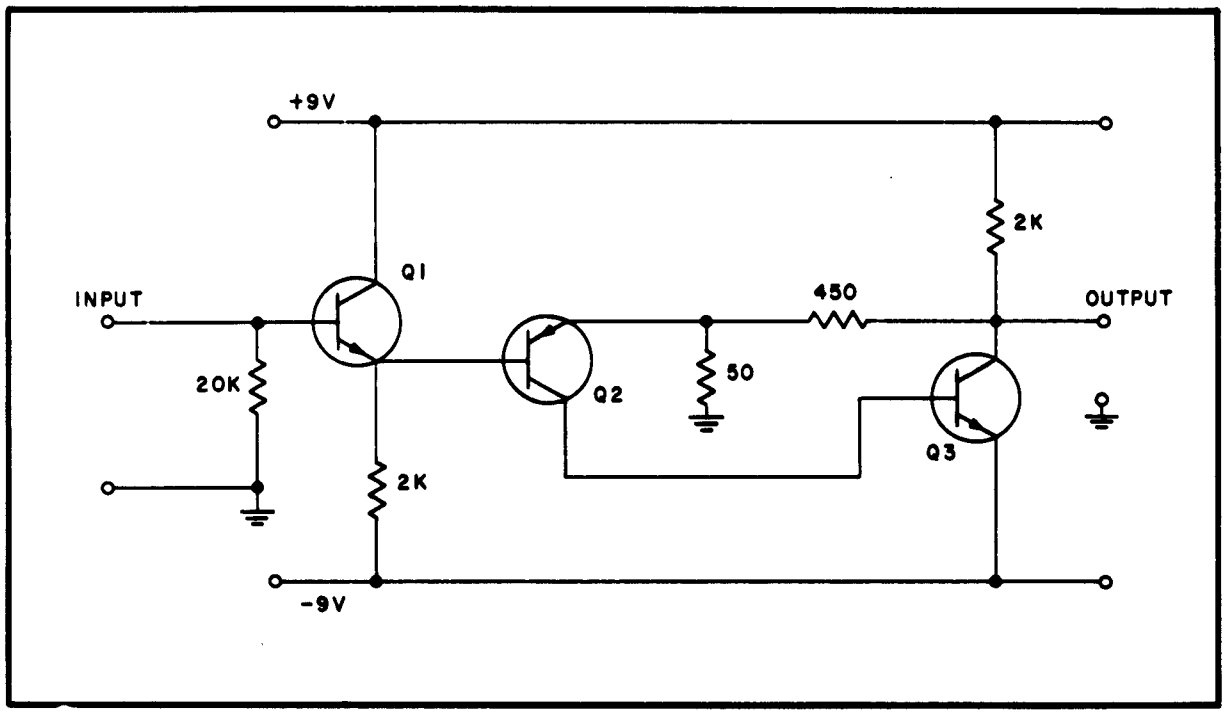


Figure 40. A-9 Video Amplifier

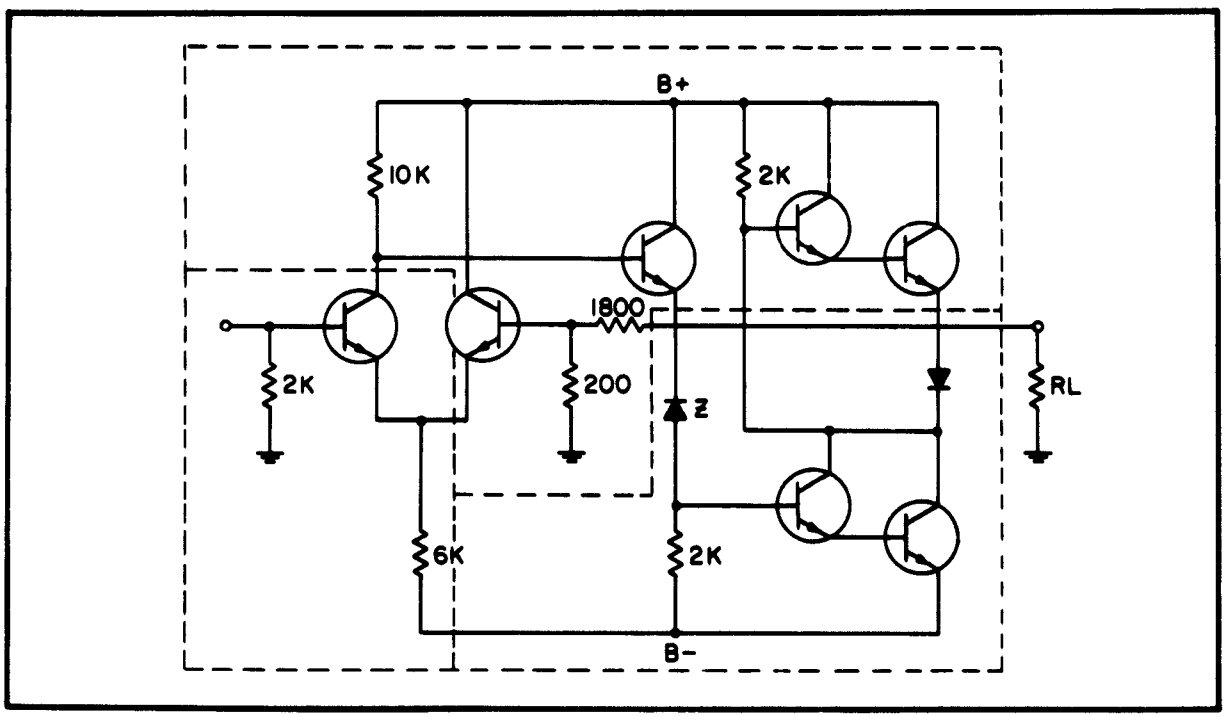


Figure 41. Circuit of A-10 Amplifier

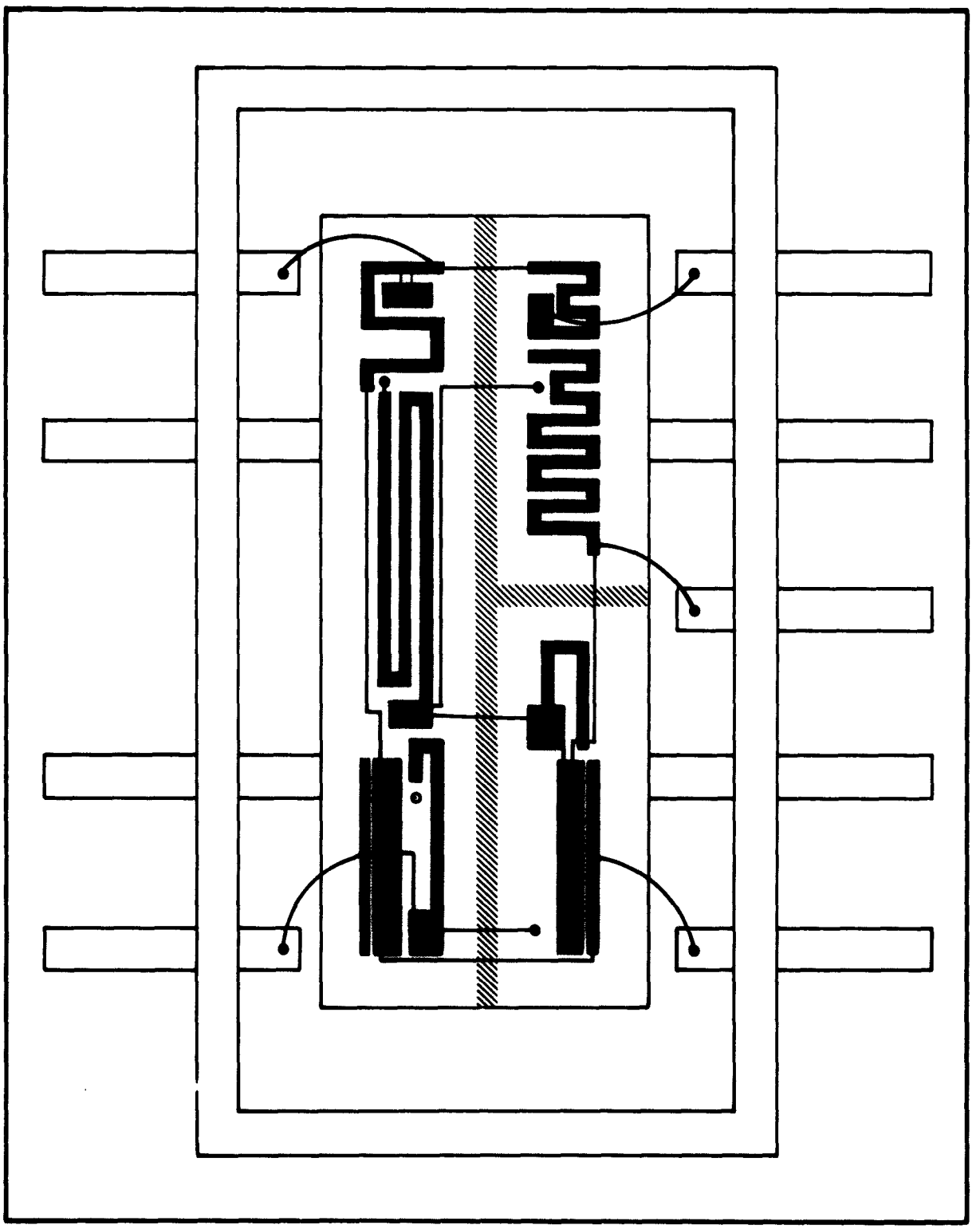


Figure 42. Physical Layout A-10 Amplifier

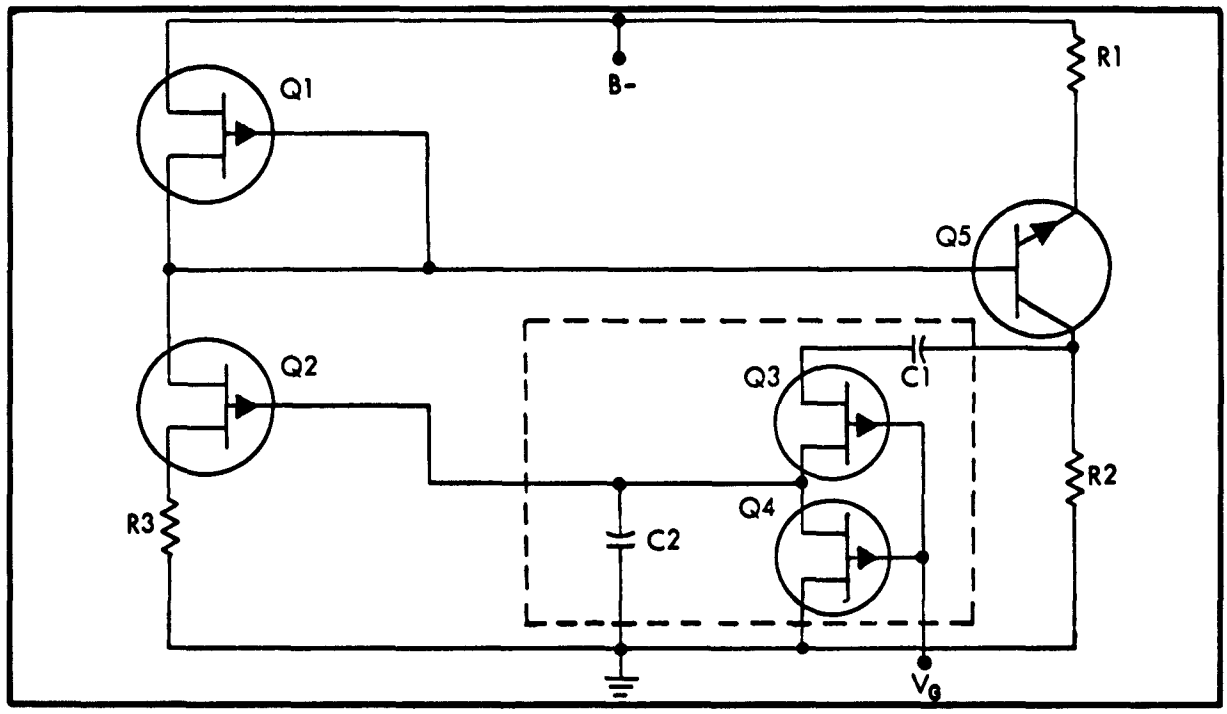


Figure 43. Schematic Diagram of O-2 Oscillator

3.3.1 Variable-Frequency Oscillator O-2

This circuit is a zero-phase-shift oscillator, shown schematically in Figure 43. The field-effect transistors Q_3 and Q_4 are used as variable resistors in the feedback network so that frequency can be controlled by the voltage, V_G. The amplifier section is designed with a UNIFET (Q_2) input for high input impedance so that loading across the feedback network is minimized.

Two diffusion runs were fabricated using the physical layout shown in Figure 44. Parameters for the individual components of the networks were satisfactory except for the ratio of the saturation currents (I_{DSS}) of Q_1 and Q_2.

3.3.2 Fixed-Frequency RF Oscillator O-3

The O-3 has the same schematic diagram as the A-8 and uses the same parts. However, the notch filter is adjusted to provide 180 degrees phase shift at its null frequency. Several O-3's have been fabricated.

3.3.3 Voltage-Controlled RF Oscillator O-4

The O-4 is a variable-frequency oscillator consisting of an amplifier bar and a feedback network. However, in the O-4 the null frequency of the RC network may be varied by changing the bias voltage across the

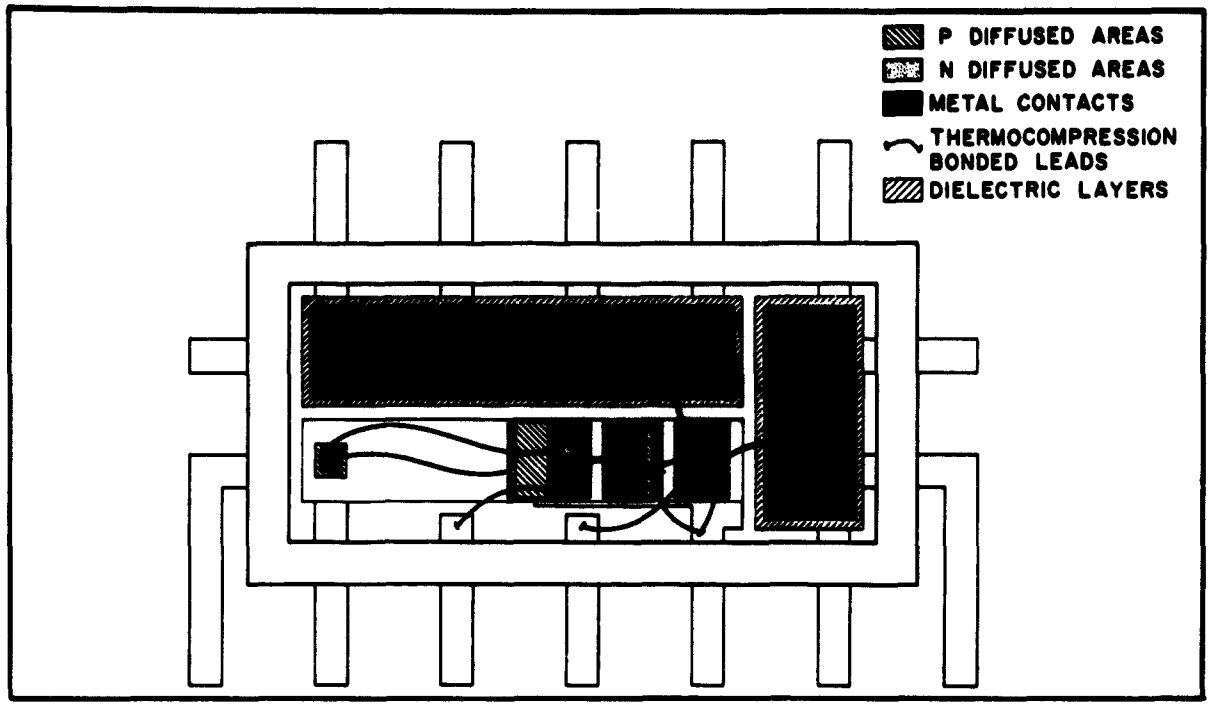


Figure 44. Physical Layout of Variable Frequency Oscillator O-2

depletion layer of the distributed network. An FM transmitter, built from the O-4 was presented to ETL/ASD. A schematic of the transmitter is shown in Figure 45.

One O-4 was completed and had a frequency range of 500 kc to 1 mc for a control voltage of −5 to +5 volts.

3.3.4 Study of a Low-Frequency Oscillator

A study was made of a voltage-variable oscillator using a three-section, RC ladder, phase-shift network with UNIFET devices as the voltage-variable resistors. From measurements of phase shift versus gate voltage, it appears that the RC network can be used with a high-gain amplifier to give a voltage-variable frequency of oscillation over the range 100 to 10,000 cps.

3.4 Pulse Circuits

The negative resistance characteristics of the BIFET are of great interest for semiconductor network pulse circuits. Of special interest are bistable circuits useful in computers with low quiescent and operating power.

3.4.1 Ring Counter PC-1

A ring counter which uses BIFET's as the bistable multivibrator for the individual stages is shown in Figure 46. Power dissipation is minimized

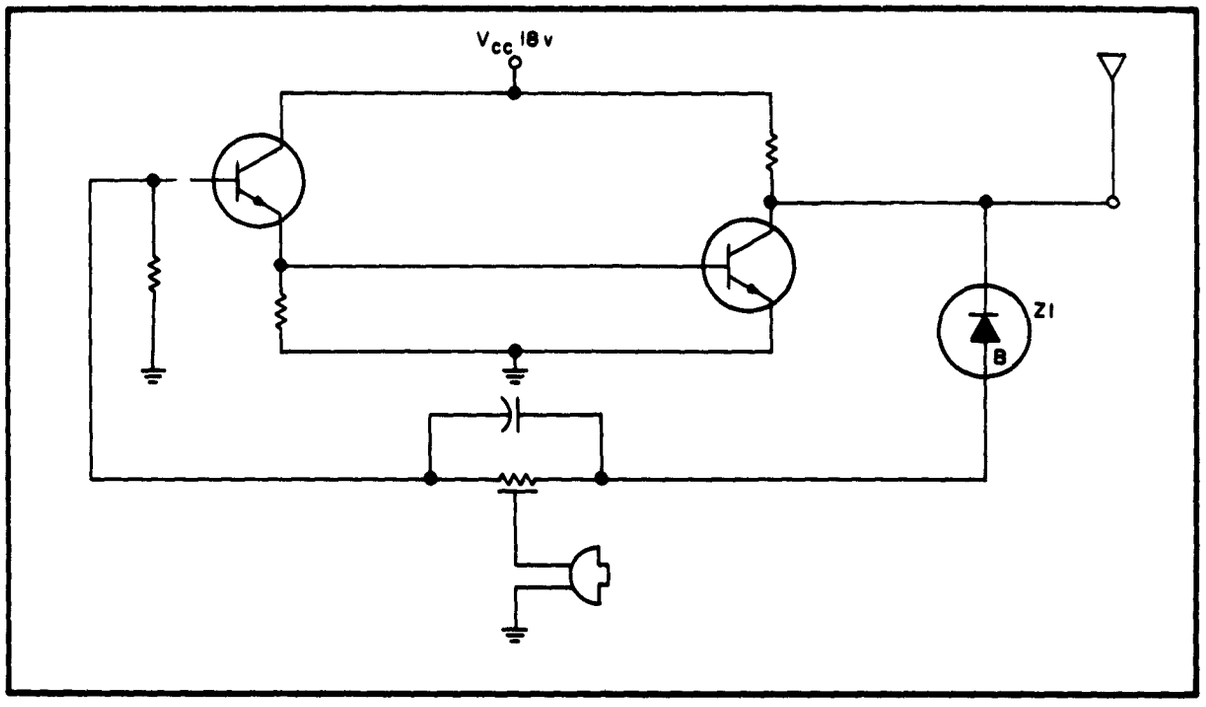


Figure 45. FM Transmitter Employing an O-4 Oscillator

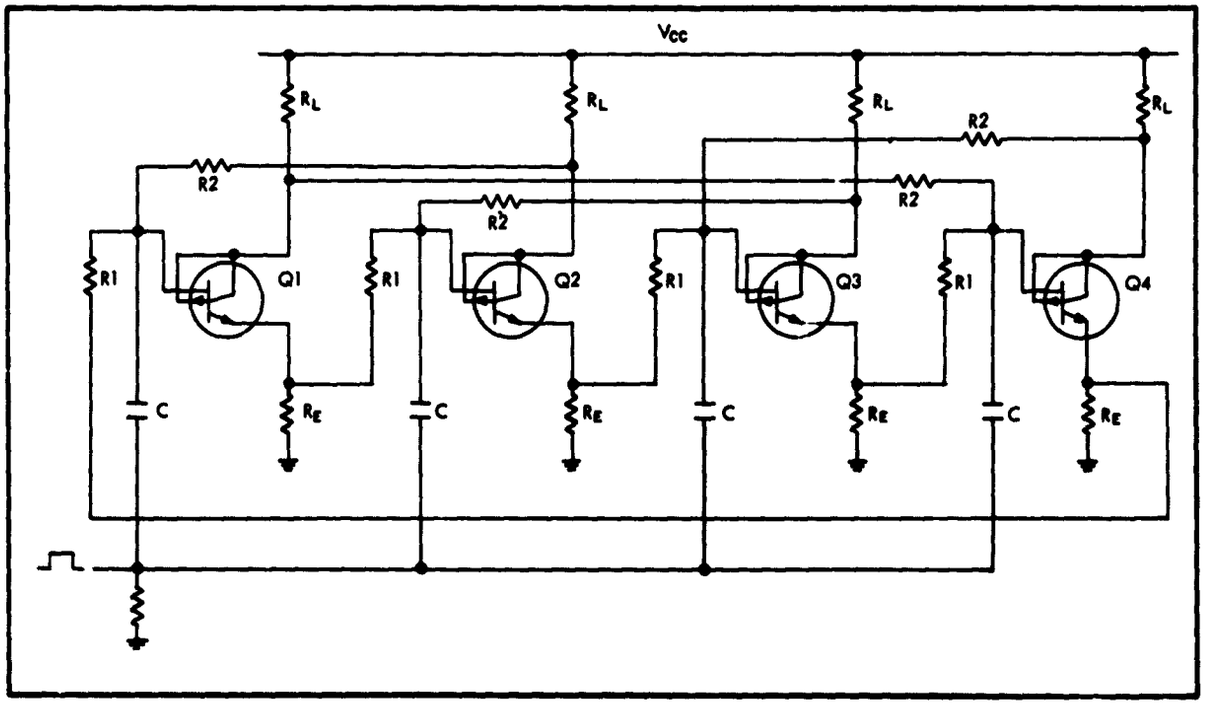


Figure 46. Four-Stage Ring Counter-Source Triggering

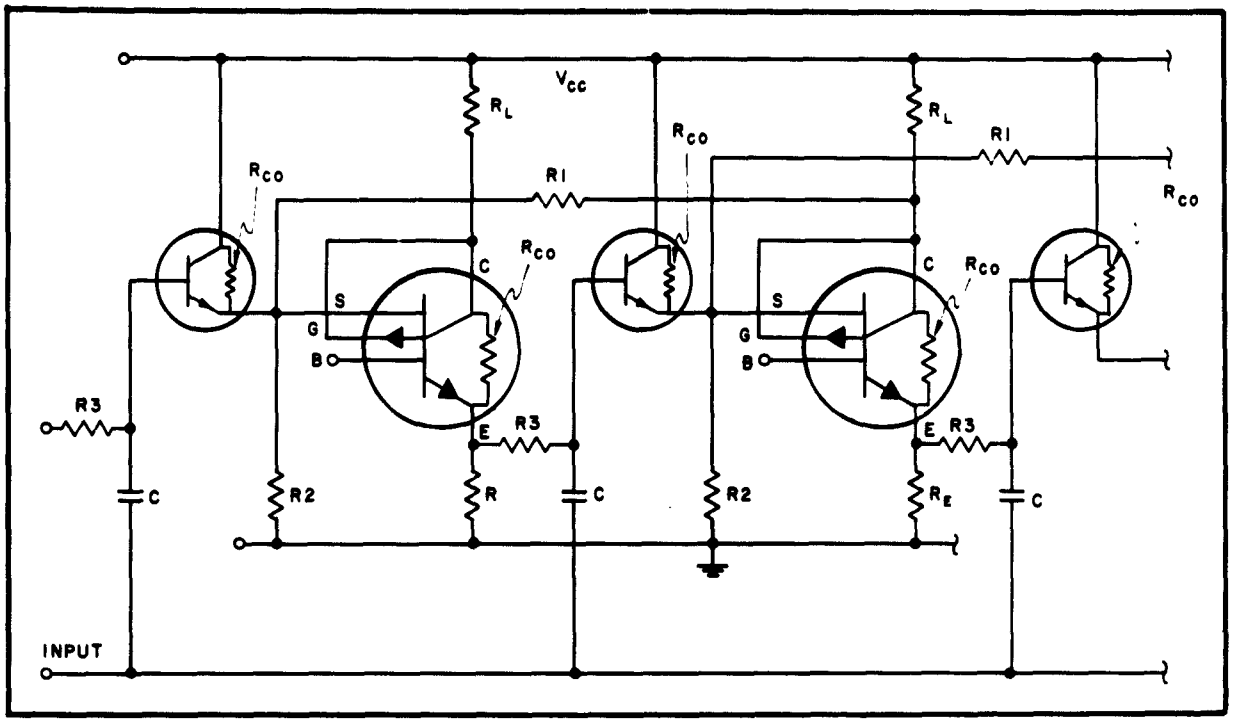


Figure 47. Source-Triggered Ring-Counter Stages

in the BIFET circuit since only one active device is on at any given time. This circuit has been operated with X-349A devices at 200 kc from -40 to 100°C.

A circuit is shown in Figure 47 which uses source triggering and transistor isolation between stages. This circuit allows greater tolerance in fabrication of resistive and active areas. A number of wafers were fabricated which showed bistable characteristics. Attempts to construct a ring counter were unsuccessful due to faulty contacts.

3.4.2 Pulse Generator PC-2

The bistable multivibrator can be made astable by replacing one of the biasing resistors with a capacitor (Figure 48). The repetition rate can be controlled by R_3 and C; the pulse width can be controlled by C, R_1, and R_2.

The pulse generator PC-2, shown in Figure 49, is composed of an astable multivibrator driving a monostable multivibrator. The astable multivibrator is similar to that of Figure 48 except that R_3 is replaced by a UNIFET which acts as a source of constant current to charge the capacitor linearly. The UNIFET also allows external frequency control by adjustment of gate voltage.

The monostable circuit can be made by addition of several components to the astable multivibrator circuit as shown in Figure 49. The UNIFET,

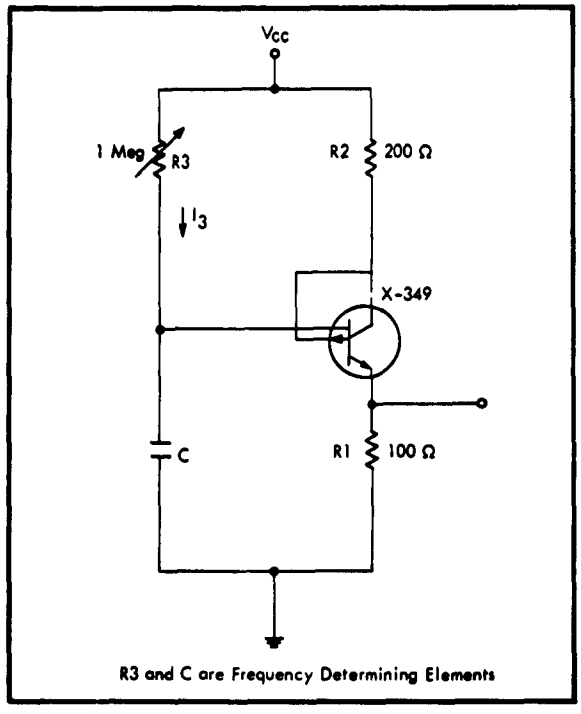


Figure 48. Astable Multivibrator Circuit

Q_3, holds the BIFET in whichever state it is. Resistor divider R_1 and R_2 holds the source voltage below its trigger voltage.

Consider the BIFET, Q_1, to be ON initially. Q_3 supplies current to the BIFET and holds it ON; thus Q_1 and Q_2 cannot function as an astable circuit. If a negative pulse is applied at the base of Q_1, the BIFET turns OFF. Q_3 is also turned OFF because its gates are tied to the collector of Q_1. However, Q_2 is still conducting and charges the capacitor C until the BIFET is triggered ON again.

The channel current of Q_2 and thus the output pulse length are functions of the gate voltage, V_{G2}. Ratios of maximum pulse width to minimum pulse width of 240 to 1 have been obtained.

The monostable multivibrator consists of five bars in a 7-pin semiconductor network package as shown in Figure 50. This same network can be used for the astable multivibrator if Q_3 is disabled by opening the supply voltage to R_1. The complete PC-2 is an assembly of two such packages. A complete PC-2 was fabricated which operated successfully.

3.4.3 Bistable Multivibrator PC-4

A semiconductor network bistable multivibrator with low power consumption, high input impedance and high fan-out can be realized by using the UNIFET as an active circuit element. The circuit should also be less sensitive to nuclear radiation than bipolar transistor circuits. Low-level circuit operation in the 200-kc range is practical with these devices. Figure 51 shows a conventional bistable multivibrator circuit using UNIFET's as the active element.

An improved multivibrator circuit using UNIFET's for load and bias resistors is shown in Figure 52. This circuit has less stringent device requirements; it can be designed for lower power dissipation.

A semiconductor network layout of the circuit of Figure 52 is shown in Figure 53. It is made from two bars of N-type silicon material and is symmetrical around the center line. The electrical connection points are identified to reference them to Figure 52.

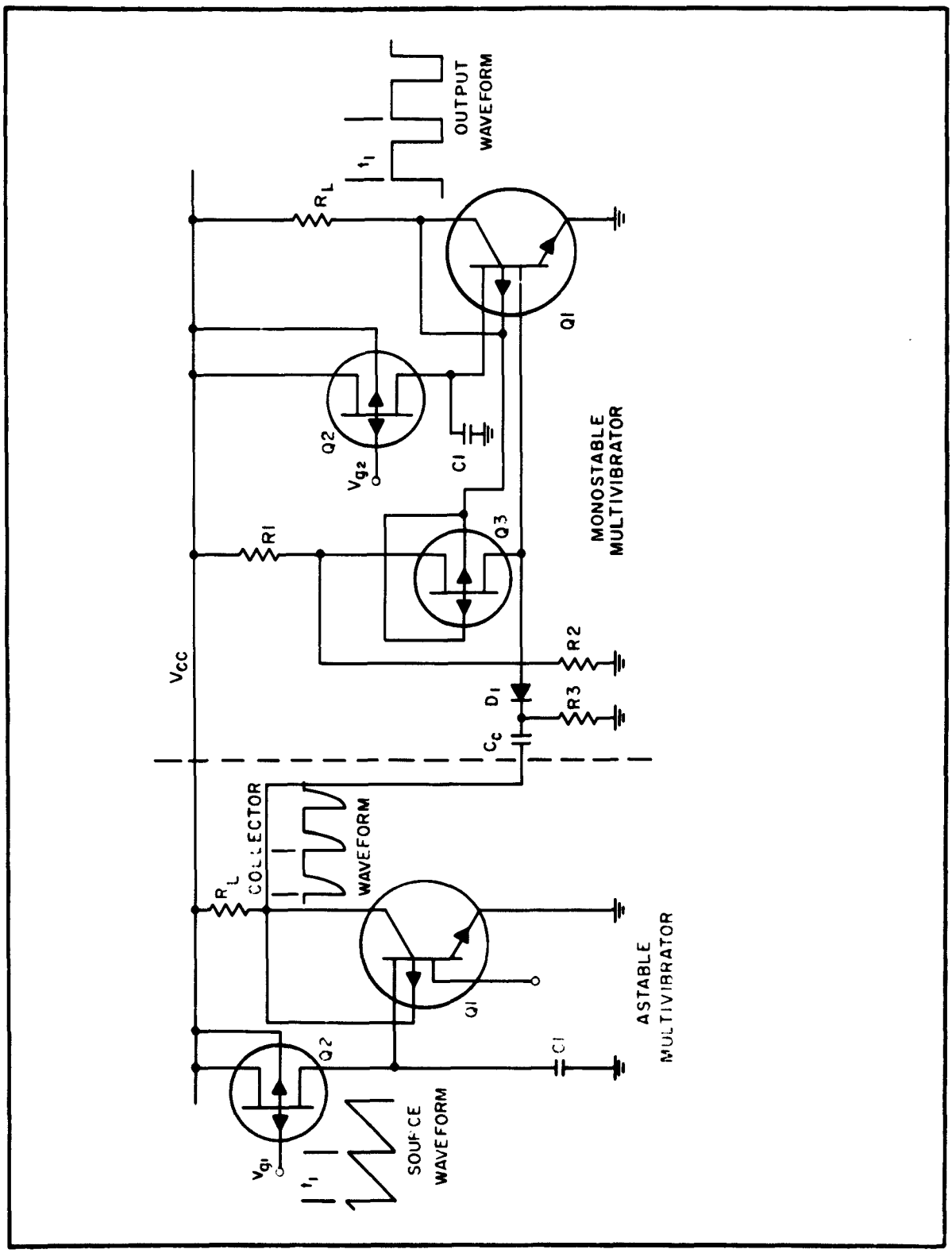


Figure 49. Pulse Generator PC-2

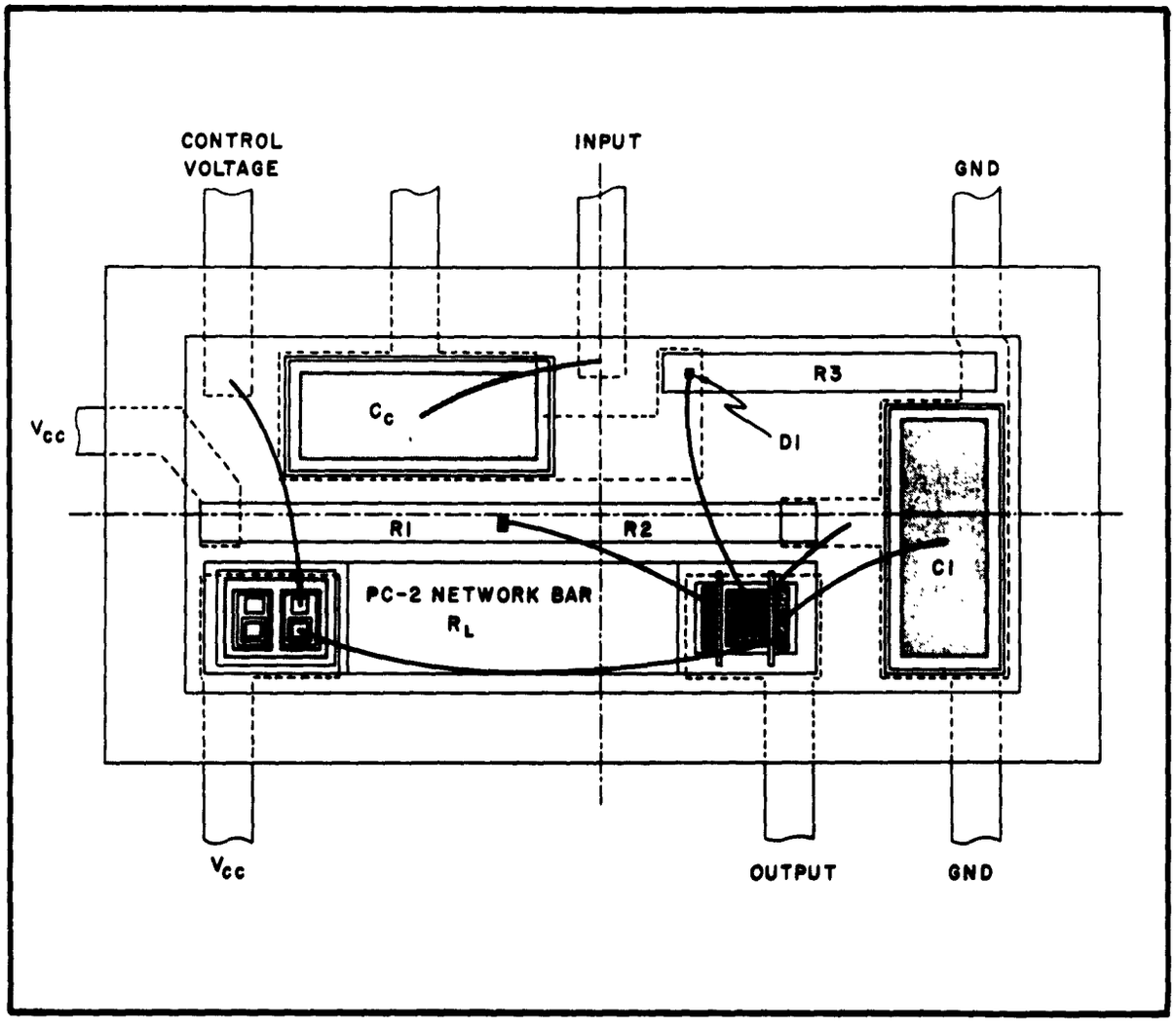


Figure 50. PC-2 Package Layout

A breadboard circuit of Figure 52 responded to trigger pulses at a 200-kc rate. However, the semiconductor network version was not successful due to lack of electrical isolation between components.

The circuit diagram of a bistable multivibrator using four active devices is shown in Figure 54. This circuit will respond to trigger pulses at a 200-kc rate. Figure 55 shows the semiconductor network layout of the circuit.

The multivibrator circuit above has not been fabricated due to diffusion spiking problems in the UNIFET. However, another multivibrator circuit has been designed and evaluated that will operate with devices that are presently being fabricated and have some spiking. The circuit diagram is shown in Figure 56.

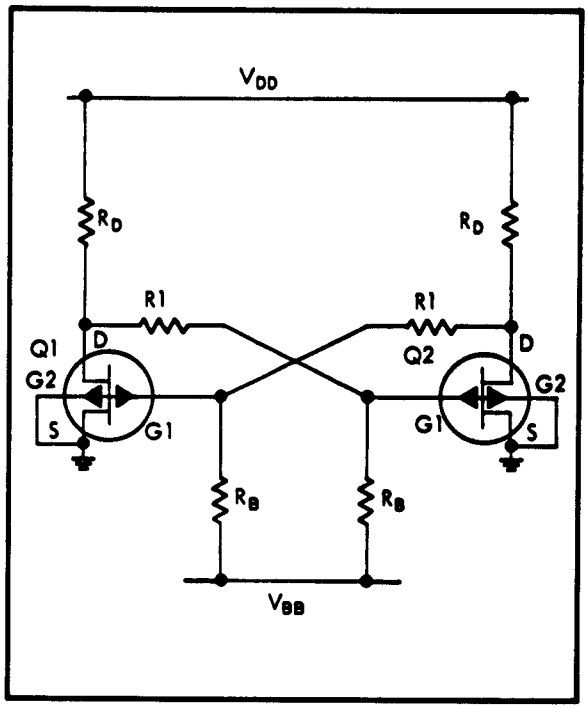


Figure 51. Bistable Multivibrator with Two UNIFETs

This circuit is essentially a conventional bipolar transistor flip-flop with the crosscoupling resistor replaced with UNIFET's. The network required to convert the flip-flop from a set-reset circuit to a binary counter stage is shown by the dashed lines. The cross-coupling UNIFET's permit the use of efficient collector triggering instead of the usual base steering techniques, reducing the number of components required for a counter. The UNIFET's should also provide temperature compensation for the transistors and increase the reliability of the circuit.

Two cascaded breadboard counter circuits have operated as a 1-megacycle counter with a power dissipation of less than 20 milliwatts per stage. The semiconductor network layout of one bar of the PC-4 bistable multivibrator is shown in Figure 57.

3.4.4 Controlled-Field Flip-Flop PC-5

Two controlled-field flip-flops utilizing transistor and diode chips mounted on a small sheet of resistance paper were fabricated and delivered to ASD to demonstrate the controlled-field concept described in Paragraph 2.4.1. The transistors were physically mounted on the sheet at the locations where the collector connections are shown in Figure 58. Diodes were mounted where their cathode connections are shown (external capacitors were used). The equipotential field lines indicate the voltage levels at various parts of the circuit. It can be seen that the base of Q_2, connected to point B, has a bias of approximately +0.25 volt, while the base of Q_1 is ON. If Q_1 is turned OFF, by means of an input pulse, then the field will shift and cause Q_2 to turn ON.

Two of these flip-flops have been built on a single strip of resistance paper and operated as a two-stage counter. Also, a two stage differential amplifier was tested. A voltage gain of two was achieved from the collector of the first stage to the collector of the second stage.

These resistance sheet breadboard models indicate that the controlled-field technique can be applied to semiconductor functional electronic

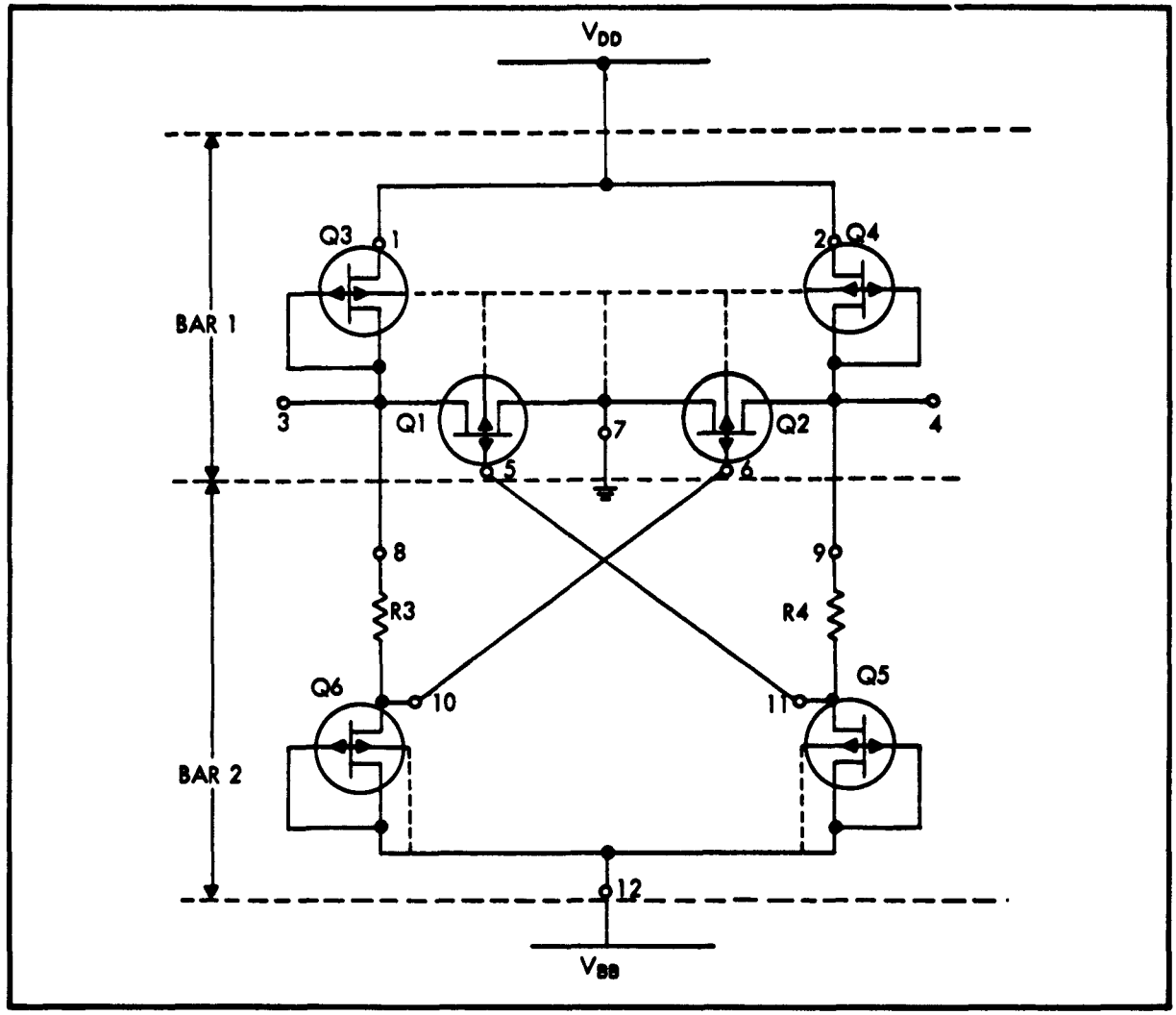


Figure 52. Bistable Multivibrator Circuit Using UNIFET for Drain and Bias Resistors

blocks. Figure 59 shows a possible layout utilizing an epitaxial N-type layer to provide the required sheet resistance.

3.5 Demonstration Receiver

From an inspection of the various circuit functions discussed in the preceding paragraphs, it became evident that a functional electronic block demonstration broadcast receiver could be assembled from these circuit blocks. The only additional circuit function needed was the first and second detectors. A block diagram of this receiver is shown in Figure 60.

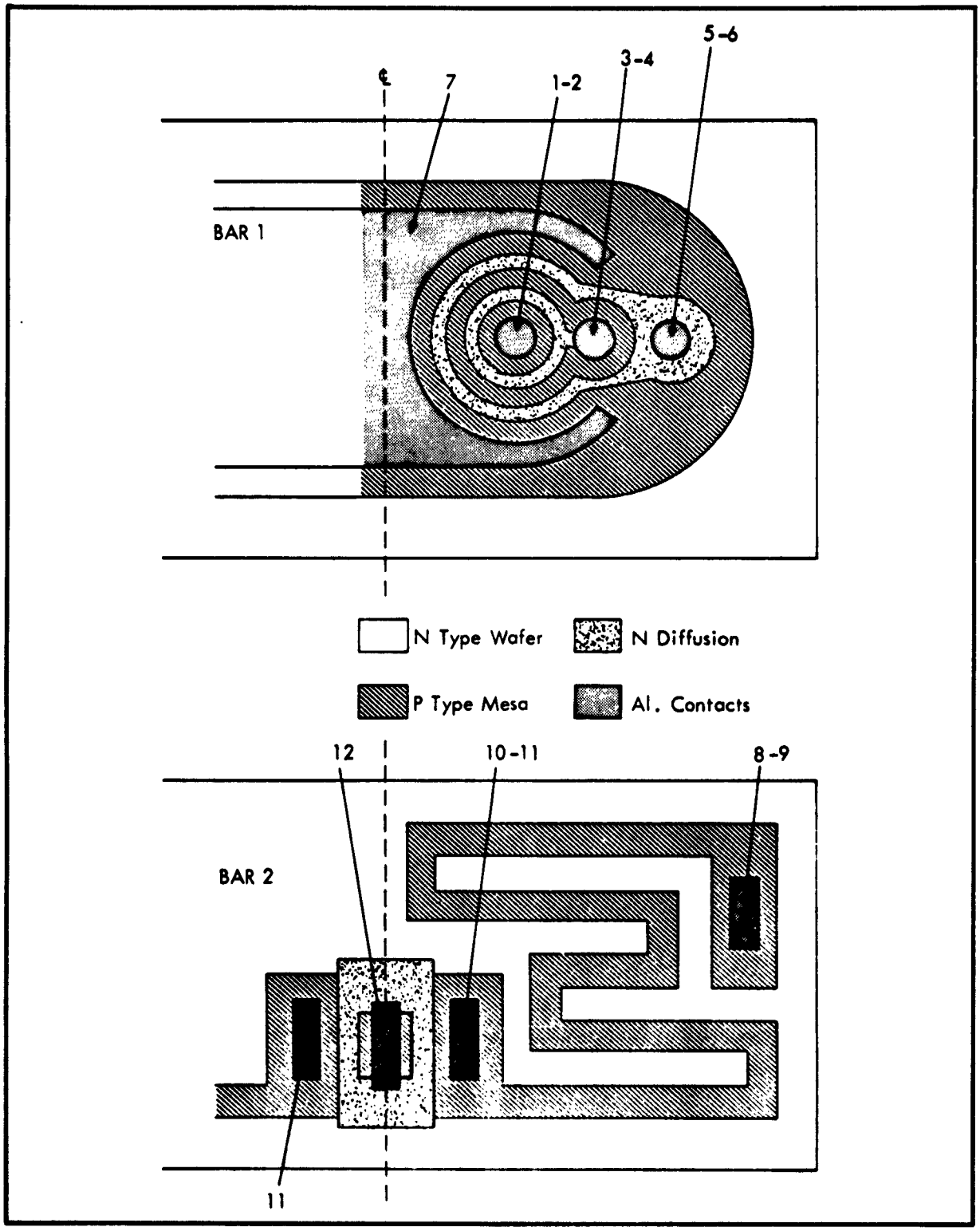


Figure 53. Bistable Multivibrator Layout

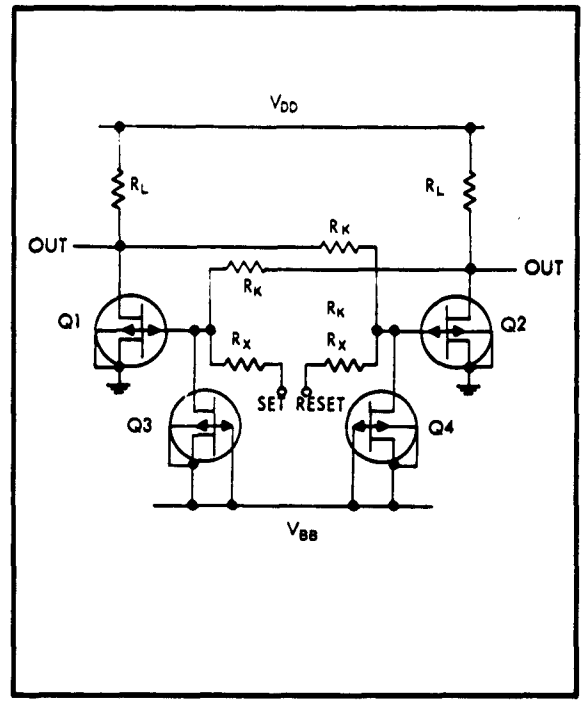


Figure 54. Set-Reset Bistable Multivibrator

The various pieces were assembled, tested, and mounted on a printed circuit board. This receiver was successfully demonstrated to ASD.

Some of the circuits were then redesigned and a receiver was assembled using the stack welding technique.

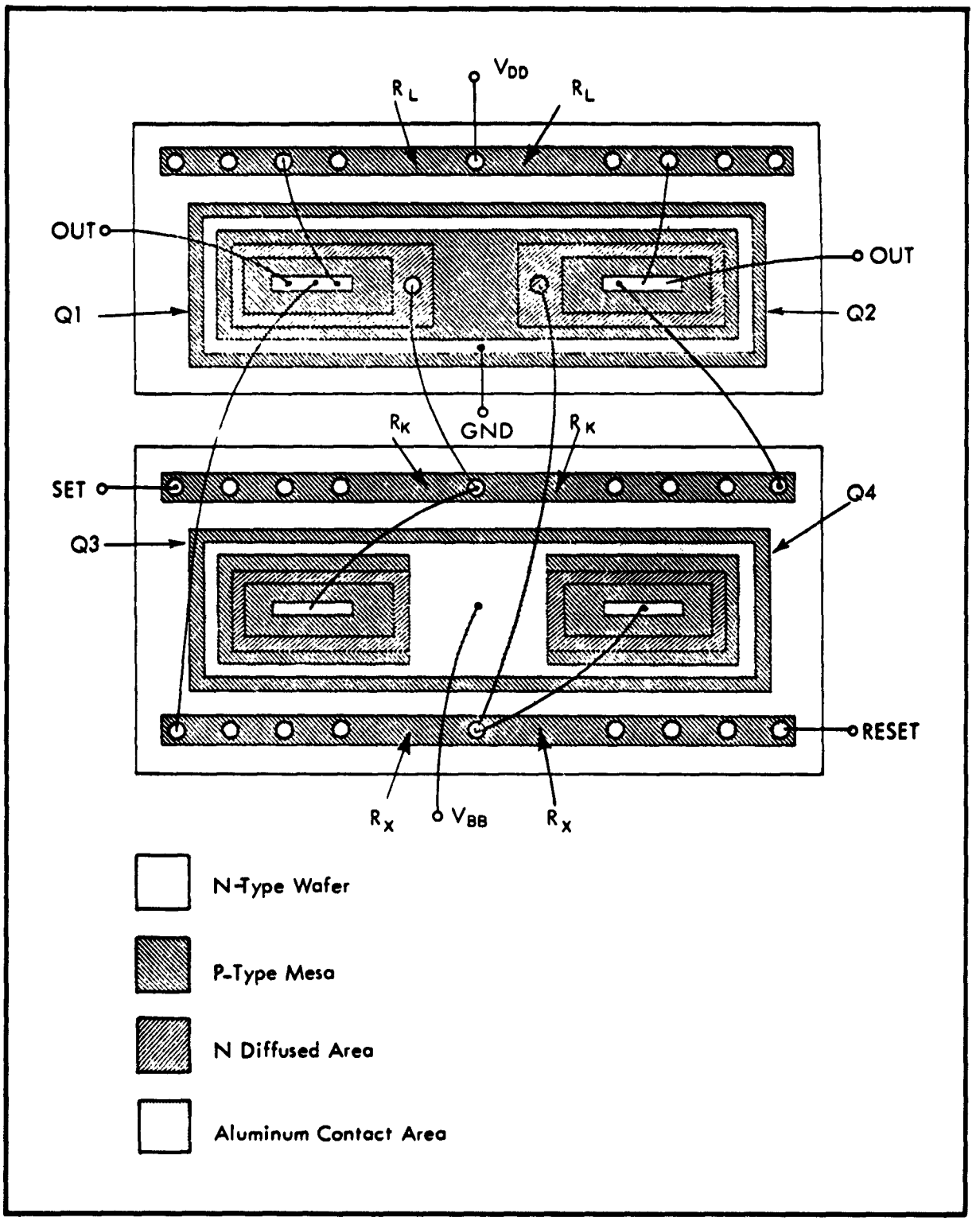


Figure 55. Network Layout for Bistable Multivibrator

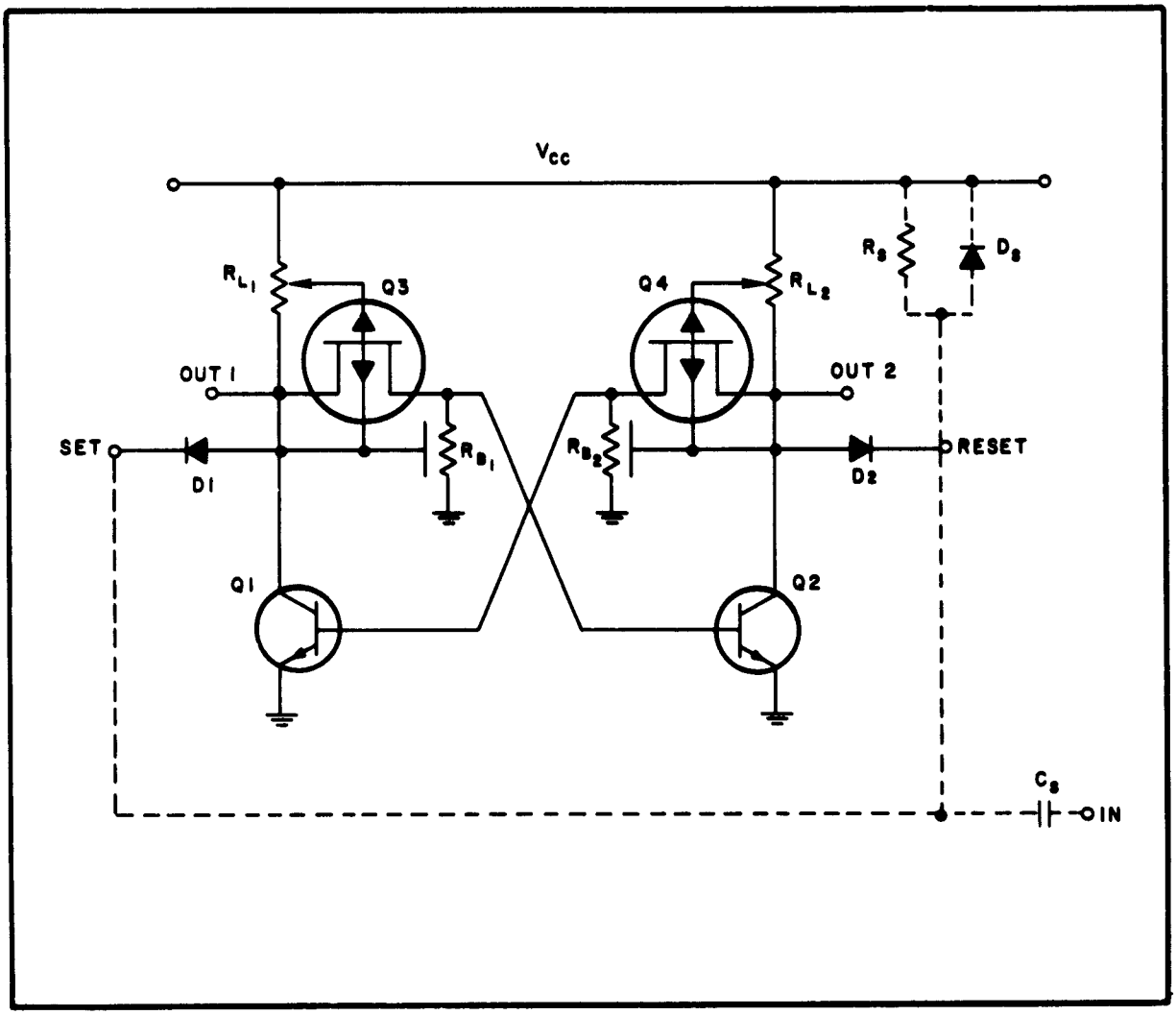


Figure 56. Bistable Multivibrator PC-4

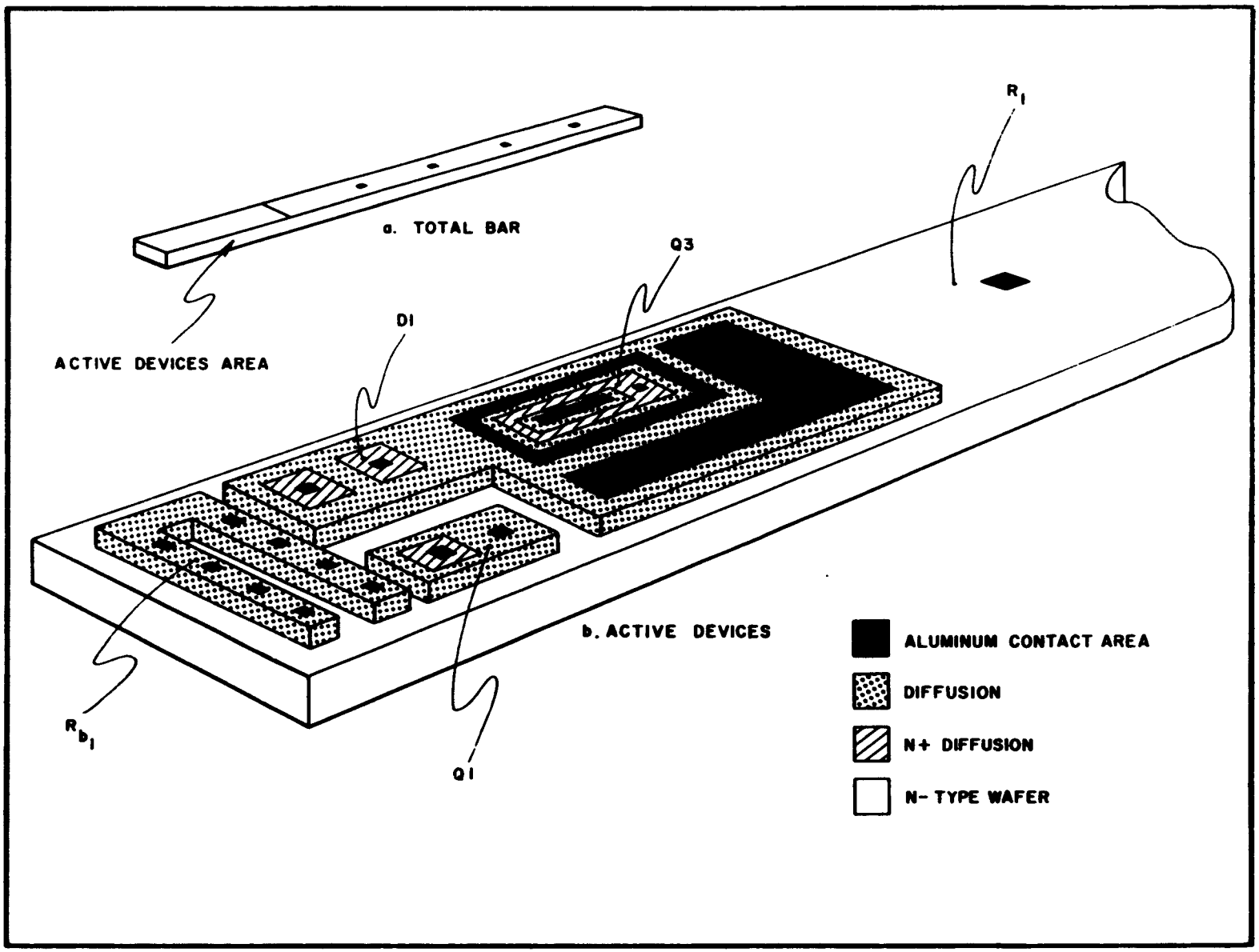


Figure 57. Bistable Multivibrator PC-4 Bar

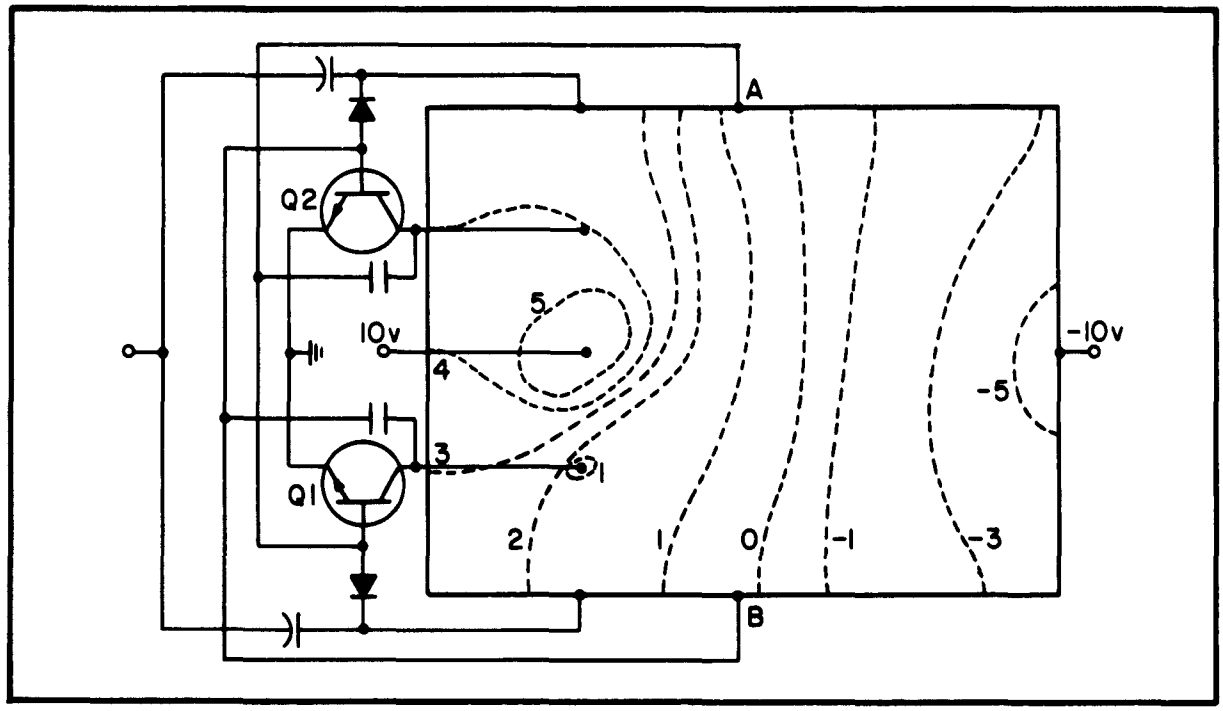


Figure 58. Field Lines Controlled-Field Flip-Flop

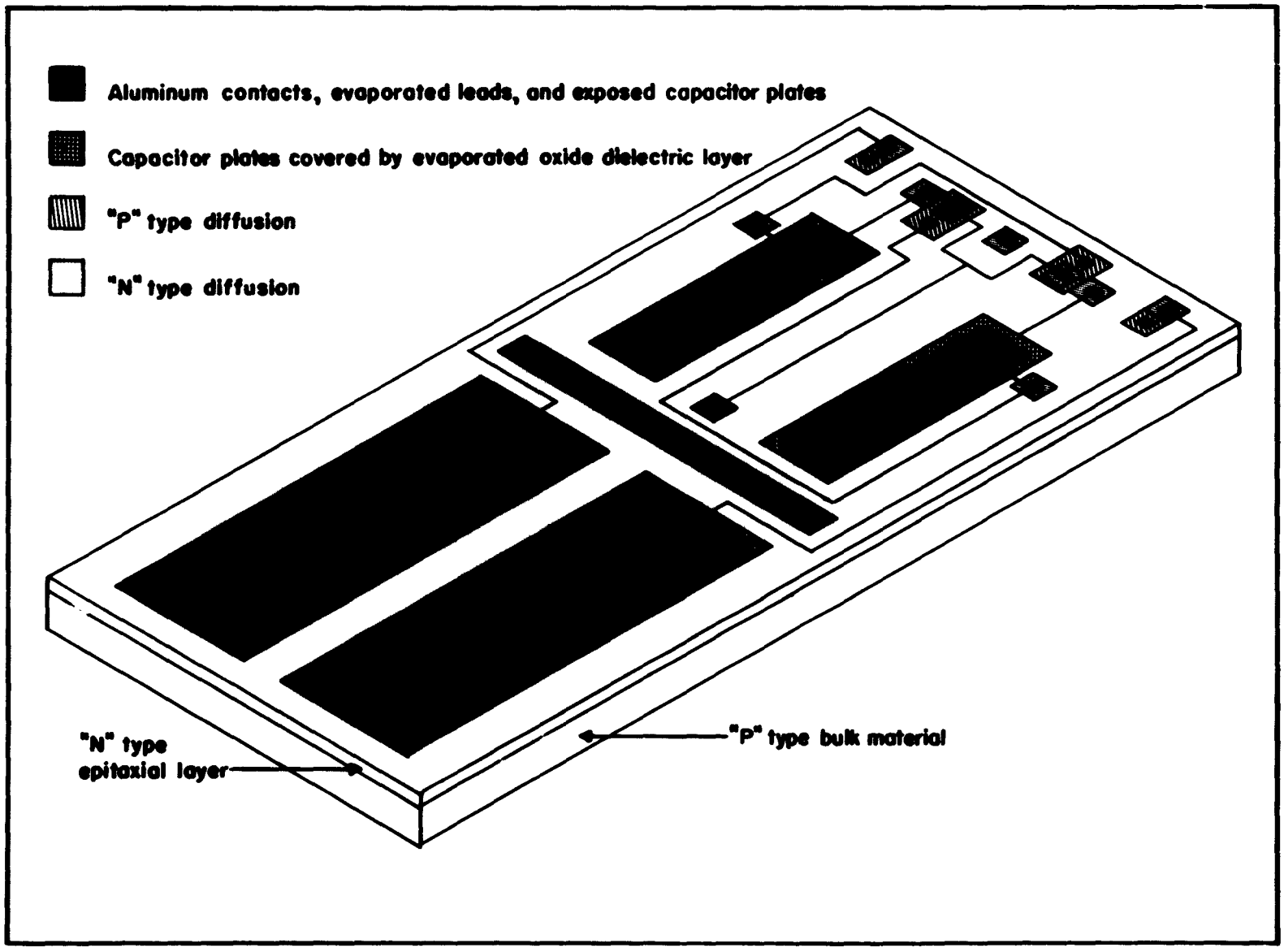


Figure 59. PC-5 Controlled-Field Flip-Flop Semiconductor Network

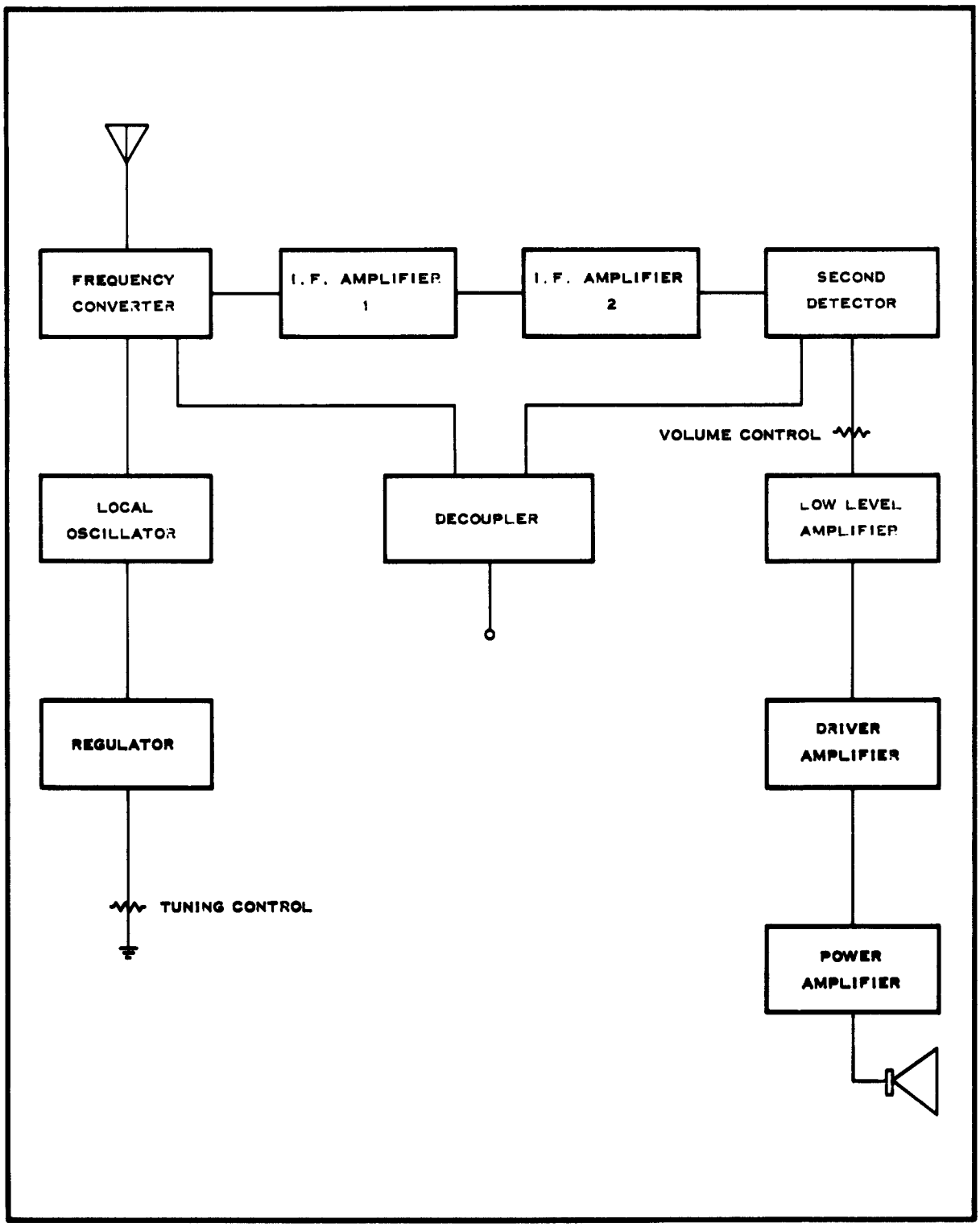


Figure 60. Block Diagram of FEB Receiver

SECTION IV

FABRICATION TECHNOLOGY

4.1 General

The fabrication of semiconductor networks requires many varied processes and skills. Extreme precision is necessary at each fabrication step because of small size and complexity of the networks. Comparable transistor fabrication techniques have been adopted when feasible. In many cases it has been necessary to modify existing processes or develop new processes to conform to the requirements of semiconductor networks.

4.2 Fabrication Procedure for a Typical Network (A-7)

The A-7 amplifier, discussed in Paragraph 3.2.4, is used to illustrate typical fabrication steps for semiconductor networks. As shown in Figure 33, the amplifier utilizes P-channel unipolar field-effect transistors in the input stage. In the second stage, planar NPN bipolar transistors are used. The feedback loop employs passive elements. The amplifier could be fabricated on a single wafer, but would require more complex selective diffusions to meet the requirements of both the unipolar and bipolar transistors.

Planar bipolar transistors are formed on the A wafer (Figure 61); unipolar transistors and diffused resistors are formed on the B wafer (Figure 62). The two types of wafers, when divided into bars, also provide the diffused regions necessary for the differential amplifiers and the feedback network.

Wafers are sawed from grown silicon single crystals and lapped, on both sides, to the desired thickness. Wafers for both bars are N-type. One side is then optically polished to provide a working surface. All transistors and diffused resistors are formed on this surface.

After polishing, the wafers are carefully cleaned prior to thermal oxidation. An oxide layer of sufficient thickness to block phosphorus and boron diffusion is thermally formed on the surfaces of both types of wafers; gallium diffusions are not masked by this oxide.

The B wafers are diffused using a two-zone process with a gallium source. Diffusion depth is measured on a test wafer by interferometric techniques after angle-lapping and staining. Sheet resistance of the diffused layer is measured with a four-point probe. The wafers are then diffused in phosphorus following a selective removal of oxide by photoresist techniques. Another test wafer is evaluated to determine the P-layer channel thickness of the field-effect devices. This is a critical dimension and depends on the difference in depth of the two diffusions.

For the A wafers, a photoresist oxide removal step is used to define areas where a P-type planar diffusion is desired. Boron is then

Figure 61. A-7 A Bar

Figure 62. A-7 B Bar

predeposited and diffused in these areas. An additional oxide forms over the entire wafer as the diffusion takes place.

A test wafer is evaluated at this point. A second photoresist oxide-removal step is now required to limit the N-type phosphorus diffusion to the desired areas. A test wafer is evaluated to determine the base width of the planar transistors, which is also a critical dimension.

After the diffusions are completed, oxide coatings on both types of wafers are removed and the wafers are coated in a high-vacuum evaporator with an aluminum film. The aluminum film is selectively removed, using photoresist, to define the contact areas. Contacts are then alloyed into the silicon. After alloying, the active elements on both types of wafers are spot checked electrically with probes to eliminate improperly diffused wafers.

The unipolar transistors on the B wafers are electrically isolated by a photoresist, mesa etched and probed again. No etch is required for the A wafers because of the inherent isolation of the planar structure.

Channels approximately 4 mils deep which outline the bars on both wafer types are formed using a photoresist deep-etch technique. Actual bar separation is accomplished by lapping the backs of the wafers. Lapping reduces bar thickness to 3 mils.

Contacts are formed by evaporation and alloying gold antimony. Selected bars are mounted in a semiconductor network package with conductive cement. This circuit was designed to allow for adjustment of both bulk-resistor and diffused-resistor values. Resistance values are checked to determine the proper contact points. Connections are made using thermocompression-bonded gold wires. After functional testing, a lid is soldered on the package to form a hermetic seal.

4.3 Fabrication Problems

One of the most critical problems is that of diffusion spiking. This is more serious in the unipolar transistor than in the bipolar transistor because of the small channel thickness, low-channel concentration, and large junction area of the UNIFET. Phosphorus spikes formed in the N-diffusion form a low-resistance shunt path between the front and back gates. The spiking effect has been reduced by using lower temperature phosphorus diffusions and extremely dry carrier gas. Other experiments show that a reduction of gate length reduces spikes due to the smaller area. This also increases g_m and reduces capacitance.

Surface damage during final polishing contributed to irregularities during diffusion. Within the past year slice polishing was changed to chemical etching, which leaves an undamaged surface.

At one time, surface leakage presented a problem for field-effect structures. The use of oxide protection and planar structures greatly lessened this problem.

In general, the varying diffusant concentrations demanded by network design require knowledge and control of impurity levels not normally encountered in the practice of transistor and diode fabrication. This requires a constant effort in diffusion studies for networks, in order to allow fabrication practice to keep pace with design knowledge. Improvements in diffusion together with epitaxial techniques hold considerable promise for extending the design capabilities of semiconductor networks.

Many of the early designs were dependent upon close control of bulk shapes by lapping or etching in order to determine resistance paths. With the increased control of diffusion over a variety of diffusants, diffused layer resistances are used, which lessens many of these processing problems, as well as allowing a more precise control of the resistance's temperature coefficient.

A high degree of geometry control has been regularly achieved through use of the photolithography. In the manufacturing area, production runs are consistently made with diffused lines of 1 mil wide. The small

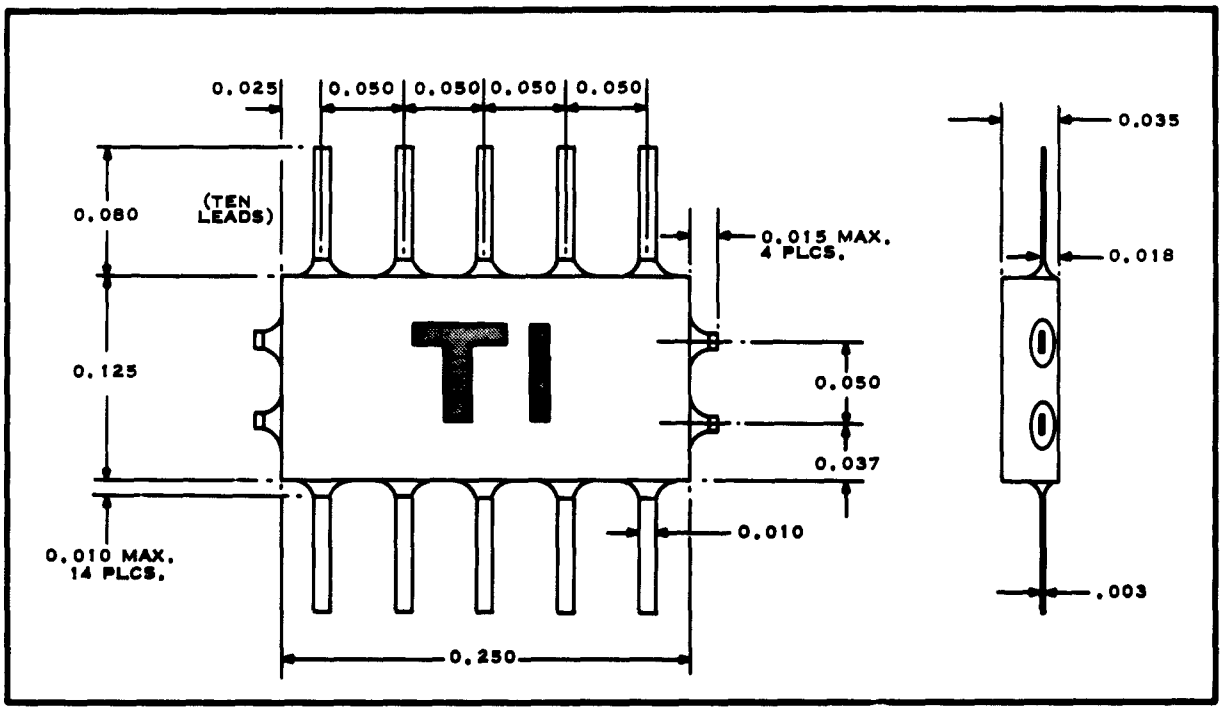


Figure 63. Semiconductor Network Package

package dimensions, allowing a maximum silicon bar size of 0.180 x 0.080 further attest to the degree of fabrication control. These bar dimensions are used for all small signal circuits and are a degree or more smaller than similar circuits made by other manufacturers.

Several of the early designs required more than 20 contacts to be made to the silicon bar. This was tedious and demanding work and has been alleviated by improved design layout and the use of deposited leads.

Although the utility of a package is a lesser problem for the development phase, a functional, hermetically-sealed package has been developed and used for all designs. The early designs required individually tailored lead patterns for each circuit design. With the use of deposited leads and diffused layer resistor paths, all contacts are made to one surface so that a standard package header (Figure 63) can be used.

SECTION V

CONCLUSION

The investigation of circuit analog design techniques for linear silicon functional electronic blocks demonstrates that a number of useful linear functions can be made. These can be expected for

Broadband amplifiers with moderate resistance range

Small values of capacitance

Moderate frequency and power requirements.

Although fabrication techniques at the time of experimentation, 1959 to 1960, presented restrictions, many of these have been overcome. As improved fabrication control is evolved, silicon linear FEB's should become more readily available.

On the other hand, requirements for high impedance, precise frequency shaping or linearity, interstage coupling or isolation, and either very low- or high-frequency functions cannot be solved adequately by the circuit analog design techniques. In order to provide answers for these problems, an exploration of other semiconductor phenomena, such as piezoelectric, photon, and thermal characteristics was undertaken. This work is described in Part II of this report.

PART II

INVESTIGATION OF SEMICONDUCTOR PHENOMENA

SECTION I

INTRODUCTION

Throughout 1959 and 1960, the use of circuit analog design techniques established that nearly all of the digital functions can be realized, and that good audio and video amplifiers and other selected types of circuitry could be designed in this manner.

In many cases, however, a high performance circuit which can readily be adapted to semiconductor functional blocks does not seem to exist. Other components, such as large-value coupling capacitors, transformers, or tuned circuits must be added, greatly reducing the overall effectiveness of the approach.

However, it is not necessary to restrict FEB's to only those circuits which can be fabricated from transistors, diodes, resistors, and capacitors. These elements use only a small fraction of the true potential of semiconductor materials, relying wholly on the principles of charge transport. More important, they do not fully utilize the interactions of this effect with adjacent regions and have not been used at all with outside forces such as heat, light, or mechanical deformation.

In order to broaden the range of FEB capability, investigation of other semiconductor phenomena and their possible application to electronic signal processing was begun under this contract in the spring of 1961. Defined tasks were established to specifically investigate promising areas, with the objective of using these phenomena effects together with circuit analog techniques to accomplish FEB's that are comparable with existing circuitry only at the function level.

Aside from investigating phenomena applicable to new circuit functions, an initial study of low-level diffused structure operation was made to gain an understanding of the requirements for very low-power level silicon FEB's.

SECTION II

LOW-LEVEL PHENOMENA

2.1 Introduction and Objective

This task was directed toward an understanding of the phenomenon which causes fall-off of α at low-currents in silicon diffused structures. This understanding could lead to fabrication techniques for controlling the slope of α with collector current. Aside from allowing extremely low current operation, control of α may also be desirable to provide a steep α slope for certain circuit functions.

Sah, Noyce, and Shockley have attributed α fall-off to recombination in the space-charge region of the emitter-base junction. The resulting recombination current has a voltage dependence of exp (qV/nkT), where $n > 1$, and may be considered to flow through a diode in parallel with the emitter-base junction of a transistor which has a constant current-transfer-ratio α_N. This model is shown in Figure 64. The "excess current" due to this hypothetical diode accounts empirically for the observed variation in α.

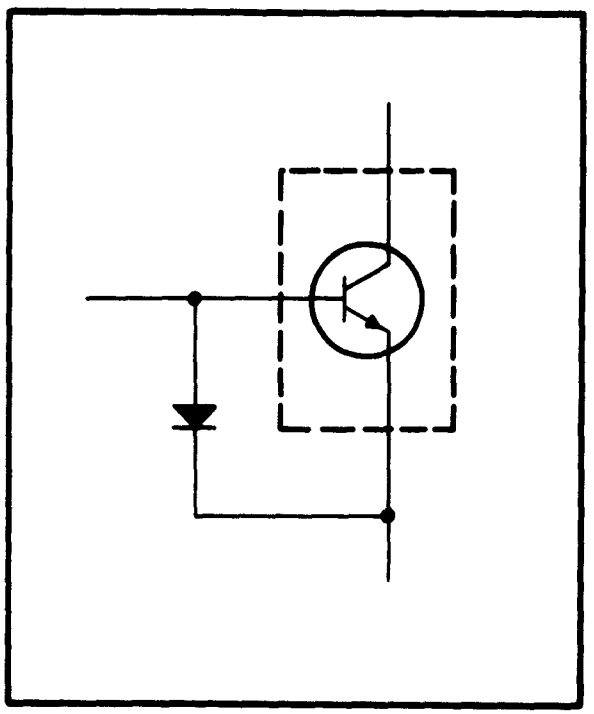


Figure 64. Model for Low Current α Analysis

In the theory of Sah, et al, it is assumed that the recombination centers which produce this excess current are uniformly distributed in the space-charge region of the emitter-base junction. However, in oxide-masked diffused structures, impurity concentrations are higher at the periphery of the emitter-base junction than elsewhere in the space-charge region. Hence, higher densities of recombination centers might be expected at the emitter-base periphery due to mechanical strains or precipitations of impurities.

There is reason, then, to suggest that the excess current may be concentrated at the periphery of the emitter-base junctions. The experiment described in the following paragraphs shows that this is so.

2.2 Theory and Experimental Verifications

The experiment is based on the model shown in Figure 64. The

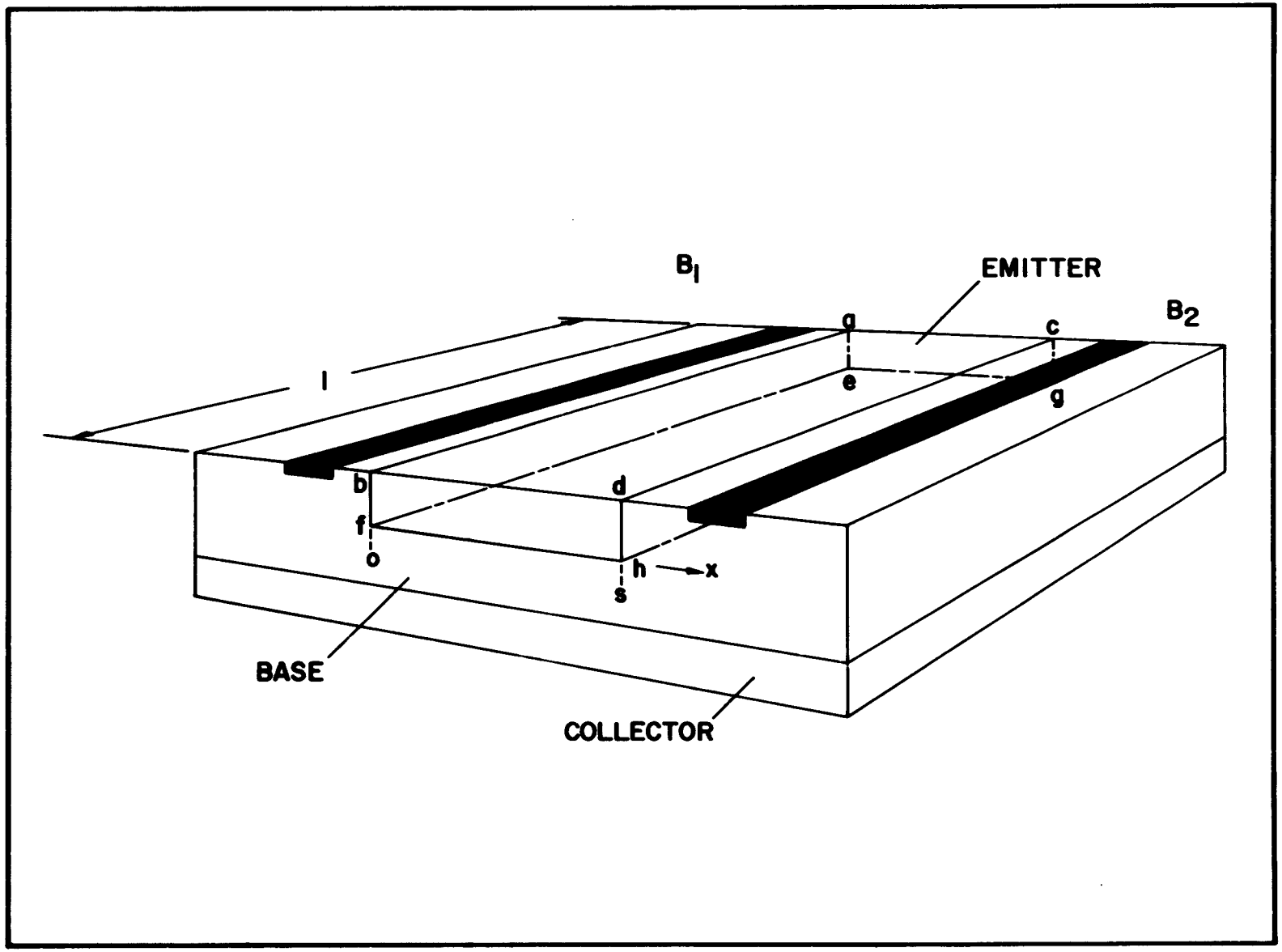


Figure 65. Transistor Tetrode Structure with Linear Geometry

currents in the ideal transistor are assumed to be diffusion currents proportional to exp (qV/KT), where V is the emitter-base voltage. The current density injected into the base is then

$$J_D = j_D e^{\beta V},$$

where

$$\beta = q/KT.$$

The "excess current density is assumed to have the form

$$J_X = j_X e^{\beta V}.$$

Using a tetrode transistor structure (shown in Figure 65), it is possible to vary the collector current distribution by applying a transverse voltage V_T between the two base contacts. The variation of base current with V_T may be calculated; the form of the variation depends upon whether the excess current originates at the surface of the emitter-base periphery or in the bulk.

As V_T is increased, the current is crowded toward one edge of the emitter-base periphery. Assume base current is changed simultaneously to maintain collector current, and therefore diffusion currents in the ideal transistor, at a constant value.

As current is crowded toward one of the peripheries (e.g., ab in Figure 65), the forward bias of the emitter-base junction will be higher at the periphery than in the active portion of the device. Consequently, for constant I_C, I_b will increase if the excess current I_X originates at the periphery.

However, assume I_X originates in the emitter-base junction under the active area of the device (efgh in Figure 65). The crowding due to V_T decreases the effective area of the device. Base current decreases for constant I_C due to increase of α at higher current densities.

Quantitative expressions were developed for the two cases under the following assumptions:

$$I_X >> \frac{1}{1 - \alpha_N} I_C, \text{ so that } I_b \doteq I_X$$

The transverse base current is much greater than I_b so that transverse bias effects of I_b are negligible.

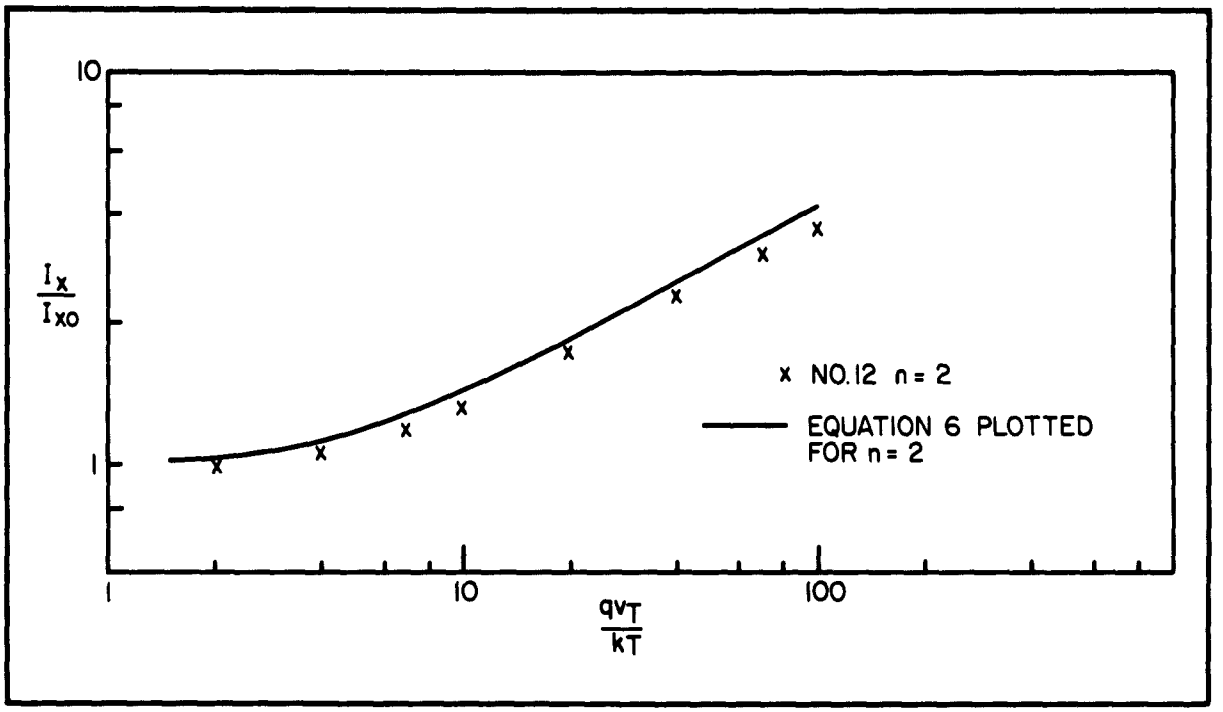


Figure 66. Results of Linear Tetrode

Under these conditions the expressions are:

Case 1: Edge origin

$$\frac{I_X'}{I_{X0}'} = \frac{1}{2}\,(\beta V_T)^{1/n}\left[\frac{\alpha_{N0}}{\alpha_N}\right]^{1/n}\left[\frac{1 + e^{-\beta V_T/n}}{(1 - e^{-\beta V_T})^{1/n}}\right],$$

where the zero subscript refers to the values for which

$$V_T = 0.$$

Case 2: Bulk origin

$$\frac{I_X''}{I_{X0}''} = \left[n\,(\beta V_T)^{[(1/n) - 1]}\right]\left[\frac{\alpha_{N0}}{\alpha_N}\right]^{1/n}\left[\frac{1 - e^{-\beta V_T/n}}{(1 - e^{-\beta V_T})^{1/n}}\right].$$

Measured results agree closely with the curves calculated assuming periphery origin. This comparison is shown in Figure 66.

In the linear tetrode of Figure 65, excess current originating at the low concentration emitter-base peripheries (fh or eg) cannot be distinguished from that originating in the bulk. Circular geometry devices with inner and

outer base rings surrounding an emitter ring were fabricated to avoid this dilemma. Calculated results for the circular geometry (assuming periphery origin of I_X) were also in good agreement with theory.

Minima observed in some of the curves of I_X'/I_{X0}' versus V_T were justified by assuming unequal recombination densities at the two peripheries and using curve fitting techniques.

For all the experimental devices considered, the results are very well accounted for by starting with the assumption that the excess current is concentrated at the surface periphery of the emitter junction. By comparing the experimental results with expressions for the total excess current (i.e., contributions from the edges and from the bulk) it is seen that the edge component is at least five times as large as the bulk component.

2.3 Conclusion

In this work it is shown that the space-charge recombination current (the "excess" component of current responsible for low-current α fall-off) originates at the emitter-base periphery rather in the space-charge region within the bulk of the material. From this result it appears that the excess current is due either to surface states or to recombination centers in the bulk near the surface of the wafer. The latter might result from the high surface concentration of the diffused impurity atoms. It is concluded, therefore, that an understanding of oxidation and diffusion offers the best possibility for a solution to the low-current α problem.

SECTION III

SPACE CHARGE STRUCTURES

3.1 Introduction

The objective of this task was to utilize the depletion region of semiconductor PN junctions to perform useful circuit functions.

The two devices selected for this study were the field-effect tetrode and a PN junction diode having a linear capacitance-voltage characteristic in the reserve bias direction.

3.2 Field-Effect Tetrode

A schematic representation of the field effect tetrode is shown in Figure 67. This device consists of two independent conducting channels of opposite semiconductor type coupled by the depletion region of the PN junction which they form. Operation of the device is dependent on the modulation of channel resistance by the penetration of the PN junction depletion region (shaded area of Figure 67). The current-voltage characteristic of the N channel is shown in Figure 68 for the bias condition illustrated in Figure 67 ($V_2 = V_4 = v_2 = v_4 = 0$).

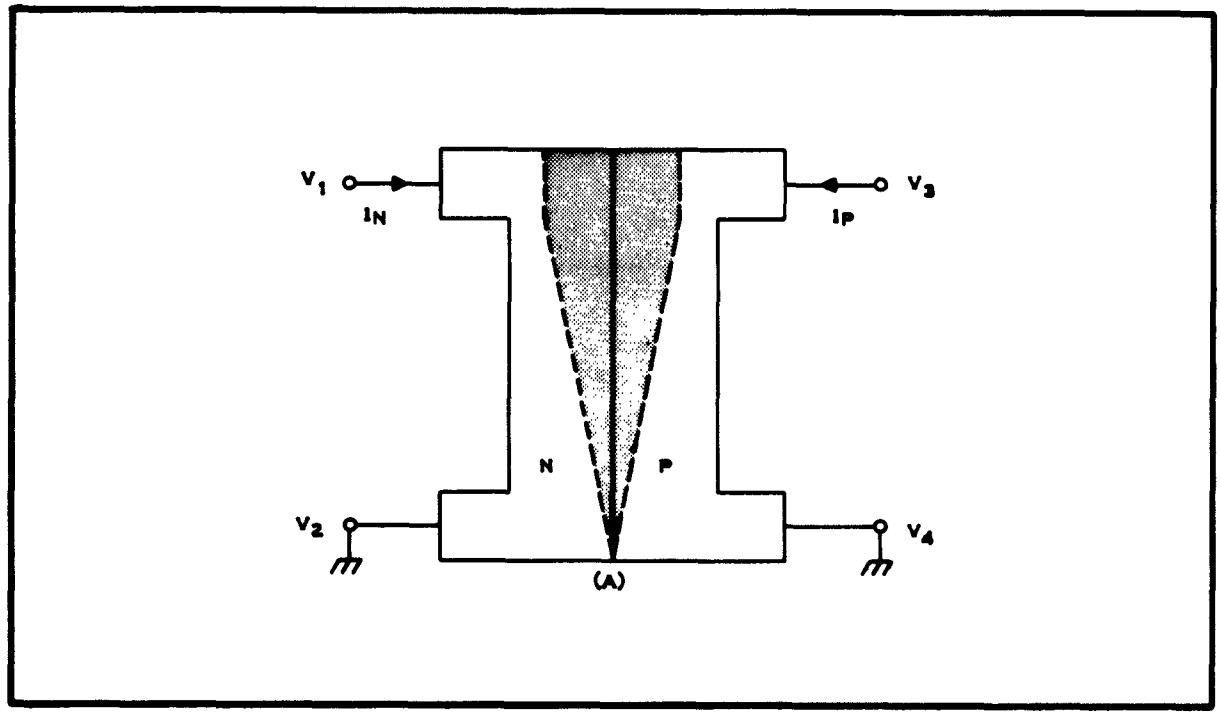


Figure 67. Pictorial Representation of Field-Effect Tetrode

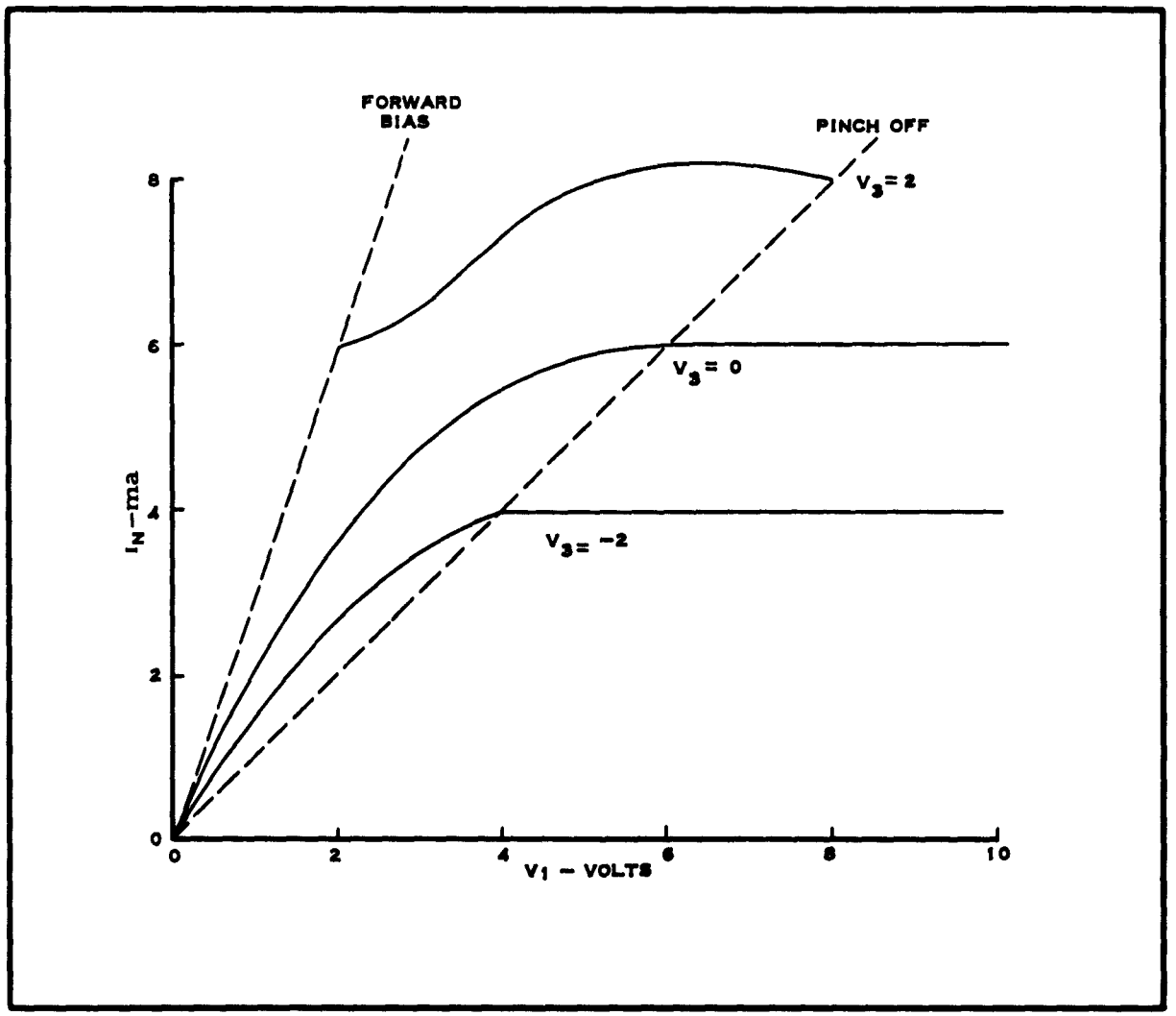


Figure 68. Current-Voltage Characteristics of the N Channel

Small signal "y" parameters as a function of V_1 and V_3 for the bias condition illustrated in Figure 67 were presented in a previous report.

3.3 Applications of the Field-Effect Tetrode

The field-effect tetrode performs the function of a gyrator when biased as shown in Figure 67 with V_1 and V_3 of the same polarity. The input impedance of a gyrator has the characteristics of an inductor when the gyrator is terminated in a capacitor. Thus, the input impedance of the tetrode with a capacitive load C_L will approximate an inductor of magnitude.

$$L = \frac{C_L}{|Y_{12}Y_{21}|}$$

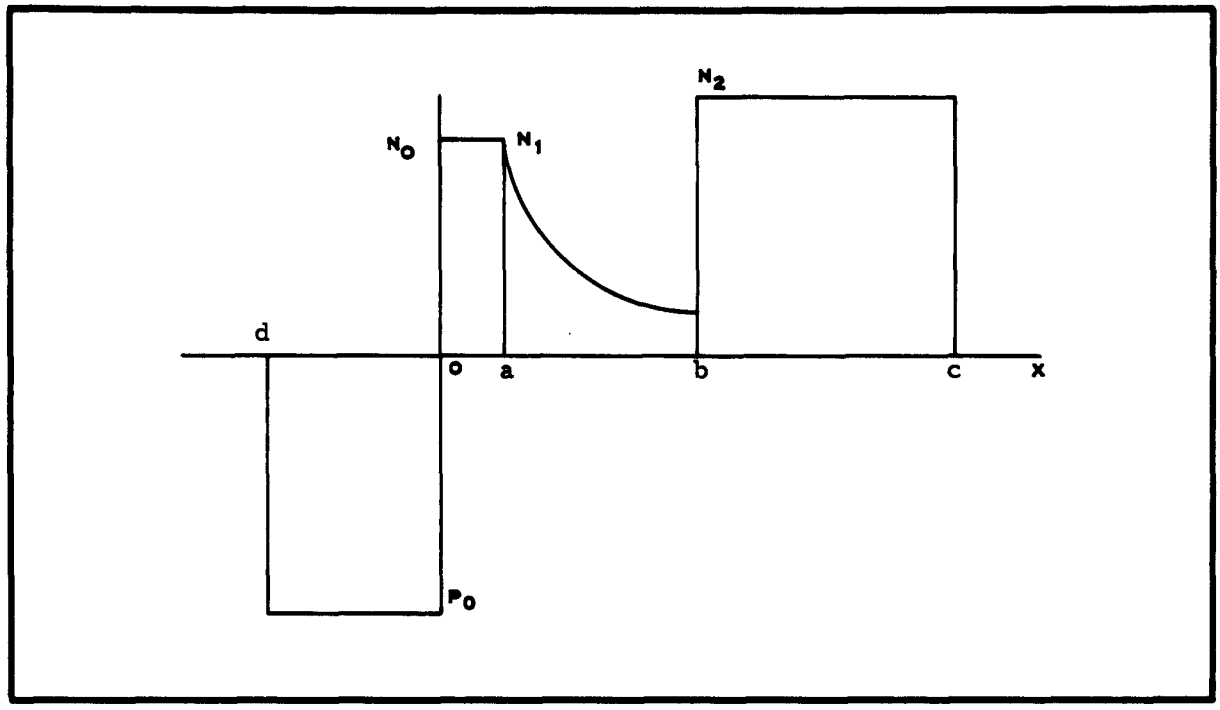


Figure 69. Concentration Profile of a PN Diode

with a Q of

$$Q = \frac{Q_{cap}}{1 + Q_{cap}\left[\frac{Y_{22}}{\omega C_L}\right]\left[1 - \frac{Y_{11}\omega^2 C_L^2}{Y_{22}Y_{12}Y_{21}}\right]} .$$

These input conditions hold with $Y_{12}Y_{21} < 0$ and $Y_{22}/\omega C_L << 1$. The apparent Q of the inductor can be made as large as desired by biasing the tetrode in a region which meets the above requirements and also causes the real part of the input impedance to be negative.

The use of the field-effect tetrode as a reversible isolator, transformer and distortionless modulator, is described in a previous report.

3.4 Linear Voltage Variable Capacitor

A device whose capacitance changes linearly with voltage can be realized with a PN junction diode having the concentration profile shown in Figure 69. The concentration profile as a function of X is given by

Concentration impurity = P_0	$-d > X \leq 0$
Concentration impurity = N_0	$0 \leq X \leq a$
Concentration impurity = $N_1 (a/x)^3$	$a \leq X \leq b$
Concentration impurity = N_2	$b \leq X \leq c.$

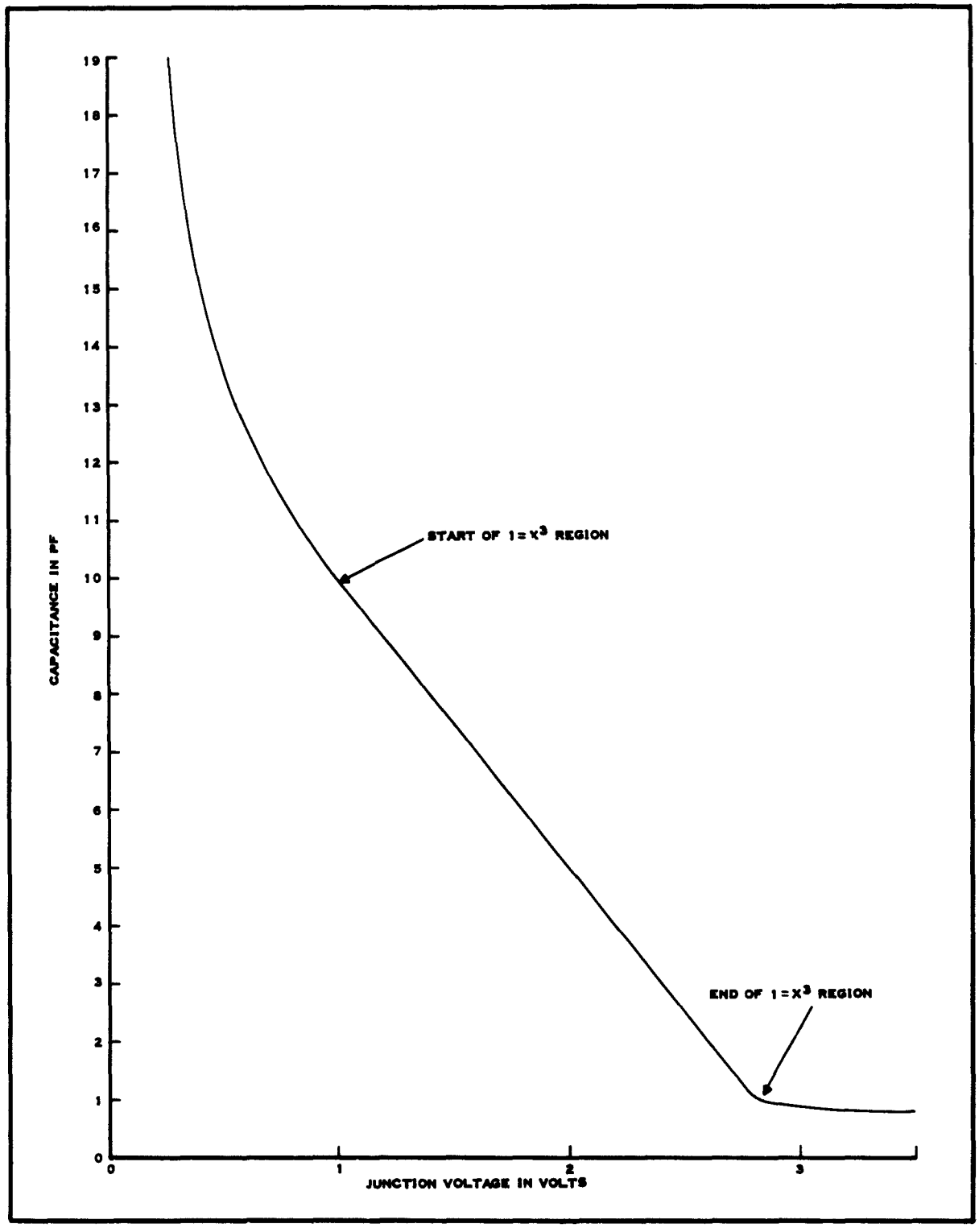


Figure 70. Voltage Versus Capacitance Plot for Junction Shown in Figure 69, $N_0/N_1 = 1$

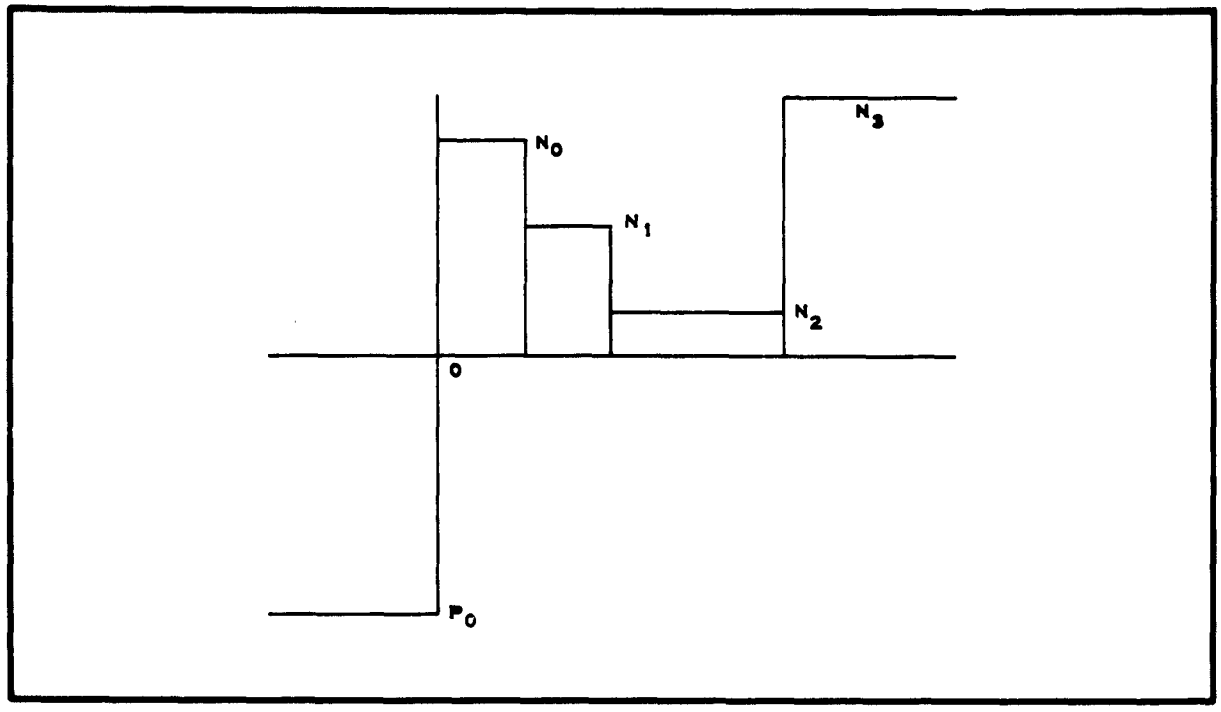


Figure 71. Retrograde Step Junction

For the device P_0 will be much greater than N_0, so the P-side of the junction can be neglected when computing junction voltage and depletion region width. The voltage versus capacitance curve for the junction illustrated in Figure 69 is shown in Figure 70. The curve in Figure 70 illustrates the linear voltage capacitance relation which is realized while the edge of the depletion region is moving through the $1/X^3$ concentration profile. The slope of the capacitance voltage curve in the linear region can be controlled by adjusting N_1 and N_0.

3.5 Experimental Results

Experimental voltage-variable capacitors were fabricated using retrograde step junctions such as that shown in Figure 71 to approximate the $(1/X^3)$ junction of Figure 69. Figure 72 shows a voltage capacitance plot of an experimental device. This device has a 7.6 to 1 capacitance change between zero and six volts reverse bias with a zero bias Q in excess of 300 at 1 mc.

Efforts were made to linearize the voltage-capacitance relation of the experimental devices. Control of the resistivity and thickness of the various epitaxial layers was not sufficient to allow repeatable results.

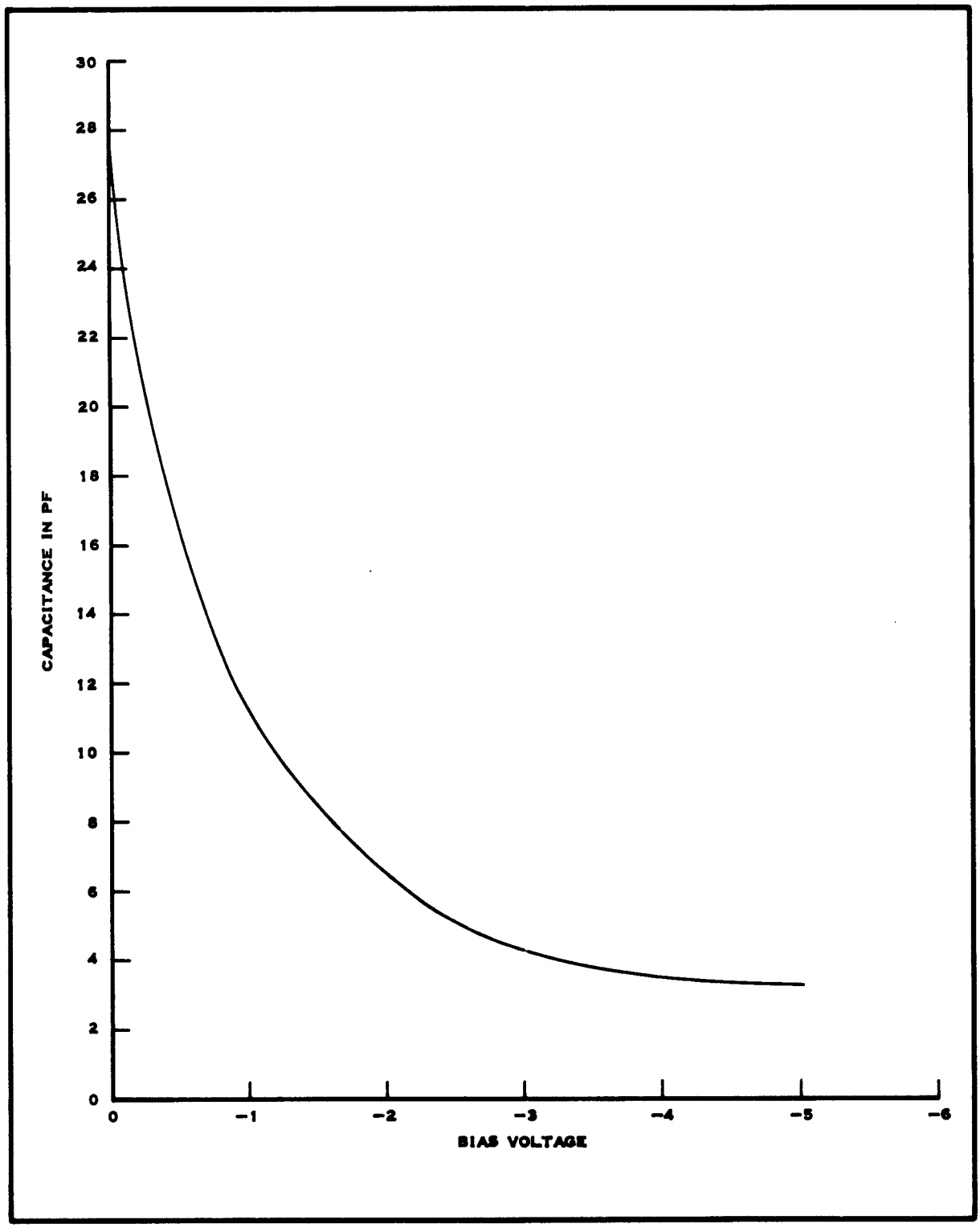


Figure 72. Voltage Versus Capacitance Plot
for an Experimental Voltage Variable Capacitor

3.6 Conclusion

This work has shown that an inductor for semiconductor networks could be obtained from the gyrator action of a field effect tetrode and that a device whose capacitance varies linearly with voltage could be realized with a retrograde PN junction diode having a $1/X^3$ concentration profile.

Effort to fabricate experimental devices has suffered from lack of control of the resistivity and thickness of the epitaxial layers. It has been recommended that further work on the field effect devices be suspended until improvements in technology have been realized which will give a greater probability of success. No further work is planned on these phases of the space charge task.

SECTION IV

PHOTO EFFECTS IN SEMICONDUCTORS

4.1 Introduction

New FEB design tools and functions may result from investigations of the photo effects in gallium arsenide. Two particular effects under study have been the photo-conduction of high resistivity material and the photo-emission of forward-biased, PN junctions.

GaAs can be prepared in a semi-insulating form by introducing impurity levels deep within the "forbidden" energy band[1]. With suitable preparation, samples are highly photoconductive.

Electroluminescence of phosphor films and reverse-biased PN junctions results from the Destriau effect (radiative recombination of excess carrier-pairs generated by impact ionization in high-field regions)[2]. This is an inefficient process, with the power gain limited to about 10^{-3} to 10^{-2} [3].

Offering more promise is electroluminescence resulting from the Lossev effect which, with further development, should have a power gain approaching unity[3]. This effect (radiative recombination of injected carriers of opposite sign)[2], is responsible for the emission from forward-biased PN junctions.

With Lossev emission, both brightness and efficiency should be particularly high using materials for which the conduction-band minimum and valence-band maximum both occur at the same point in momentum space[4]. Also, high efficiency will be most easily accomplished for materials producing emission in the infrared[3]. GaAs satisfies both of the above requirements and is of particular interest because of the present state of material and device technology.

4.2 Experimental Results

A number of photoresistors were fabricated from GaAs material of several megohms-cm resistivity. Units were prepared from a large non-oriented ingot produced by the horizontal Bridgman technique. Various contact arrangements were used. The effect of the contact arrangements on the values of resistances for the samples differed somewhat from that predicted, indicating an inhomogeneity in the GaAs crystal material or surface effects.

Some of the cells exhibited extreme surface sensitivity. Dark currents of some units increased two orders of magnitude overnight after fabrication. The dark current could be reduced to its original value by chemical treatment of the surface. But the change was not permanent and units degraded again with time.

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[1] Refer to References in Section VIII.

Relative photoconductivity was determined using a tungsten lamp producing about 1700 lumens/ft^2 on the sample. The best unit exhibited a dark resistance of 179 megohms and a resistance under illumination less by a factor of 6000.

The speed of response was measured using an arc lamp beam deflected by a rotating mirror. Modulation was displayed on a Tektronix type 545 oscilloscope with a system rise time of 30 nanoseconds. The shape of the observed signal indicated that the decay of the modulation was controlled by two time constants, one about 30 microseconds and the other about 150 microseconds. These numbers are representative of the samples tested. Although these constants are not small, the response may be a function of light intensity and spectral distribution, so that faster performance may be possible with optimum illumination.

4.2.1 Integrated Structure

Light-emitting diodes were formed directly on semi-insulating units to examine the integrated (photoconductive and photoemitting) characteristics. The integrated structure was made by diffusing zinc in on one side of a slice of megohm-cm GaAs to a depth of 0.0005 inch. A tin dot was alloyed into the diffused layer to form a tunnel diode. Contacts were made to the semi-insulating GaAs to form the photoresistor. The most promising structure of this type is shown in Figure 73. Of various contact arrangements, the one shown had least feedthrough of direct electrical signal from the tunnel diode to the photoresistor. Modulation of the resistance with bias of the tunnel diode (in the injection bias region only) was clearly evident.

The P-type material was necessarily removed before forming metallic contacts for the photoresistor. Leaving the P-type material resulted in a rectifying contact under illumination. This is illustrated in the V-I characteristic for several unilluminated resistors shown in Figure 74. For resistor R1, having a P-type layer between each contact and the high-resistivity GaAs, the resistance (V/I) increases with increasing voltage. This indicates the P-type layer forms rectifying contacts.

For resistor R2, having metallic contacts directly on the high-resistivity GaAs, a unity slope is obtained. When such contacts are closely spaced, as for resistor R3, the slope is unity until a voltage is reached for which the current increases rapidly for further increasing voltage. This condition is expected for trap-limited bias regions[5] and indicates ohmic contacts.

Optimizing of the diode emission source is most easily accomplished by separating the source from the photoresistor. Also with the source and detector as separate units, fabrication problems are reduced. Two types of units, combining the emission source and photoresistor as separate structures on the same header, are shown schematically in Figures 75 and 76.

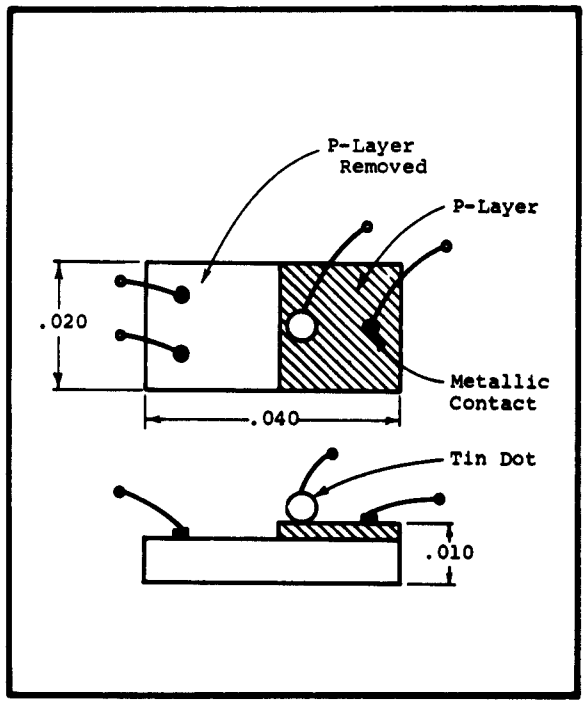


Figure 73. Integrated Structure

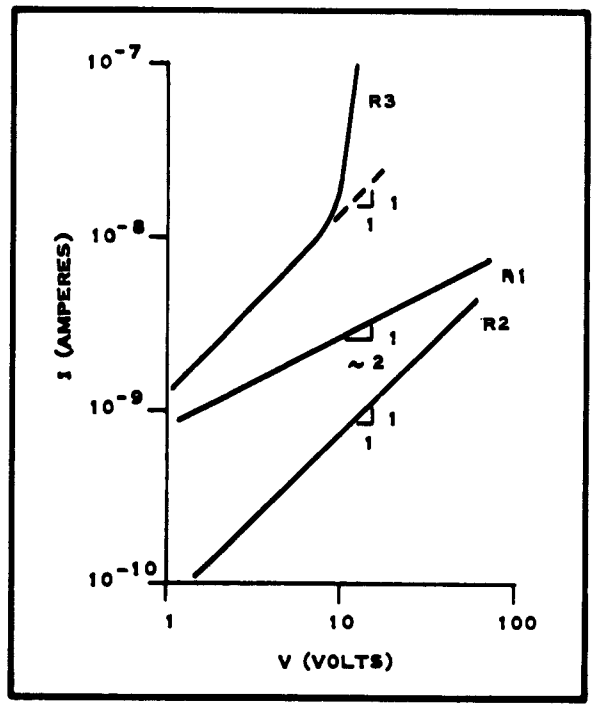


Figure 74. V-I Characteristics of GaAs Photoresistors

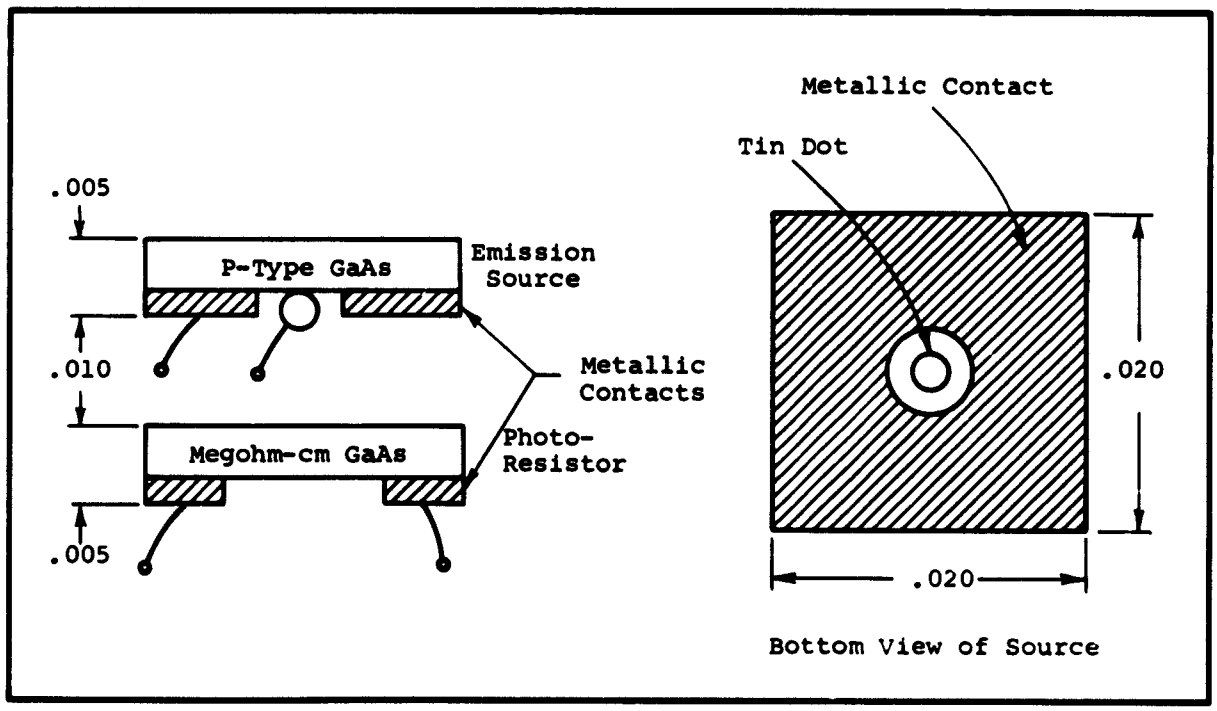


Figure 75. Separated Structures Using Tunnel Diode Emission Source

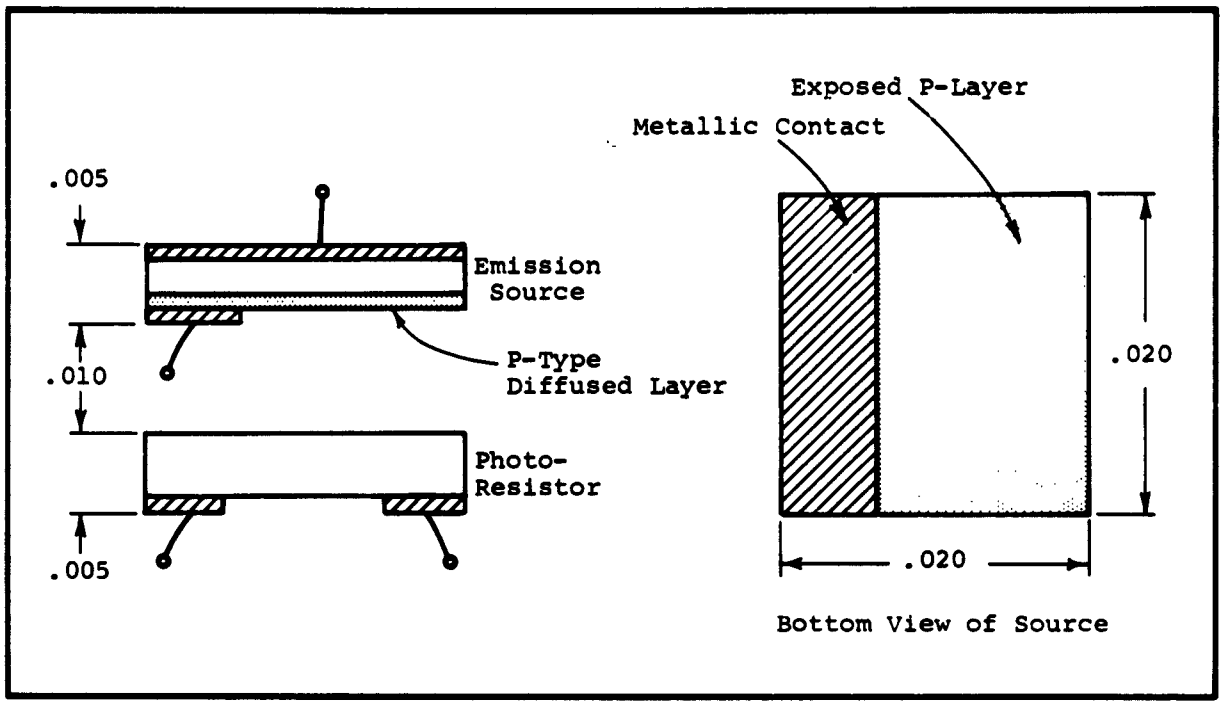


Figure 76. Separated Structures Using Diffused Diode Source

The tunnel diode sources, shown in Figure 75,are similar to those obtained with the integrated structures, i.e., alloyed tin dots on heavily doped ($>10^{19}$/cc) P-type substrates. The resistors are dice of megohm-cm GaAs with two matallic contacts.

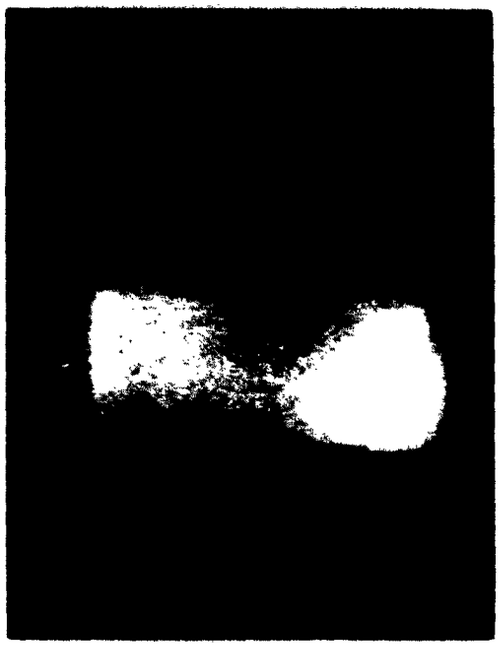
The emission source shown in Figure 76 is made by diffusing a P-type layer into N-type GaAs having a carrier concentration $N_d \approx 10^{17}$/cc.

For the structure (and relative positions) in Figure 75, modulation of the photoresistor was obtained, but it was much less than that obtained with the integrated structure for a comparable level of diode forward current. The tunnel diode structure was positioned as shown because, with an infrared image tube, emission could be detected only from a region extremely close to the base of the alloyed tin dot when viewed from the top. No emission was detected when the source was viewed from the opposite side of the wafer.

For the structure in Figure 73, emission was detected from the entire bar in the area where the P-type layer had been removed. This result indicated that the absorption coefficients for the recombination emission are much greater in the heavily doped P-type material than in the higher-resistivity material.

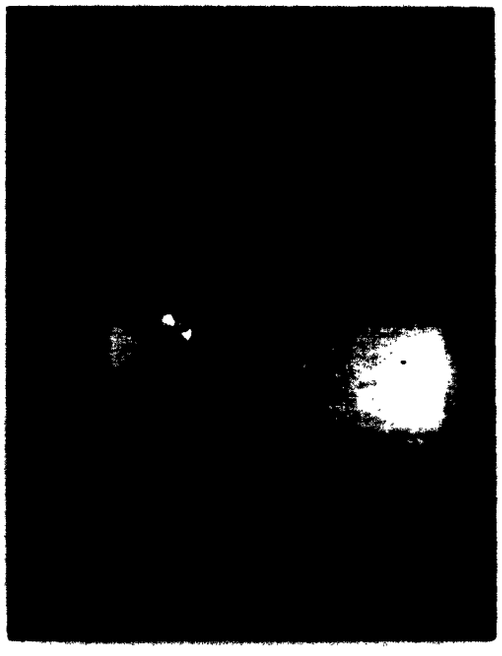
A further experiment confirming this behavior was made by using different types of GaAs as filters for viewing, with the image tube, the emission from a diode of the type shown in Figure 76. As shown in Figure 77, N-type and high-resistivity slices were translucent to the emission, and a P-type slice

Uncovered Surface



Half-Covered by P-Type Slice
2×10^{19} Acceptors/cc, 8 Mils Thick

Half-Covered by N-Type Slice
10^{17} Donors/cc, 10 mils Thick



Half-Covered by Megohm-cm Slice
10 mils Thick

Figure 77. Effects of Conductivity Type on Absorption Characteristics

of the same thickness (approximately 0.010 inch) was opaque. This type of behavior, in which the absorption at a given wavelength increases as the doping progresses from N- to P-type, was reported[6] for GaAs and is confirmed by this simple experiment.

4.2.2 Refining the GaAs Source

To investigate the effect of the contact to the N-type material of the diode source, various configurations of the tab structure shown in Figure 78 were used. Examination of units of the type shown in Figure 78a, with the infrared image tube, revealed a serious debiasing problem, as illustrated in Figure 79. This behavior can be explained with reference to Figure 78a. Current which flows through the junction from the N- to the P-type region at some distance from the edge contact must flow through the sheet resistance of the P-region to reach the contact. This creates an IR drop in the P-region which reduces the voltage available at the junction and thereby the current which flows through the junction. Thus, the effect is more severe with increasing distance from the contact.

Figure 78b illustrates a similar unit with two edge contacts. Emission from a unit of this type, shown in Figure 79, is observed over a large area and is more uniform. Figure 78c illustrates a unit with a "perimeter contact," emission from which is shown in Figure 79. Emission is more uniform than for a unit having two edge contacts.

Also shown in Figure 79 is a smaller area (0.020 inch x 0.020 inch) unit having a single edge contact. Although debiasing is present, the photograph was made with the same total current through the diode as for the larger diode, and the intensity is so great that the debiasing effect is obscured.

Although the perimeter contact was the best of the tab-type contacts, a stripe geometry contact was found to be even more efficient. The stripes consist of small diameter (0.001 to 0.003 inch) wires which are clad with a layer of pure tin. The wires are appropriately spaced on the N-type surface of the diode source, and the structure is heated to form an alloyed-bond between the GaAs and the tin cladding. The small diameter wire results in very little masking of the emitting surface. The final structure, shown in Figure 80 with a photograph of the IR emission, is much more amenable to subsequent etching and cleaning operations than the previously discussed perimeter contact.

The technique also has several advantages over an evaporated stripe technique:

1. Evaporated stripes require extensive jigging and masking but, in addition, have a relatively large sheet resistance requiring an overcoating of additional metal.

2. Leads must be attached to evaporated stripes, whereas the wire contacts are their own leads as seen in Figure 80.

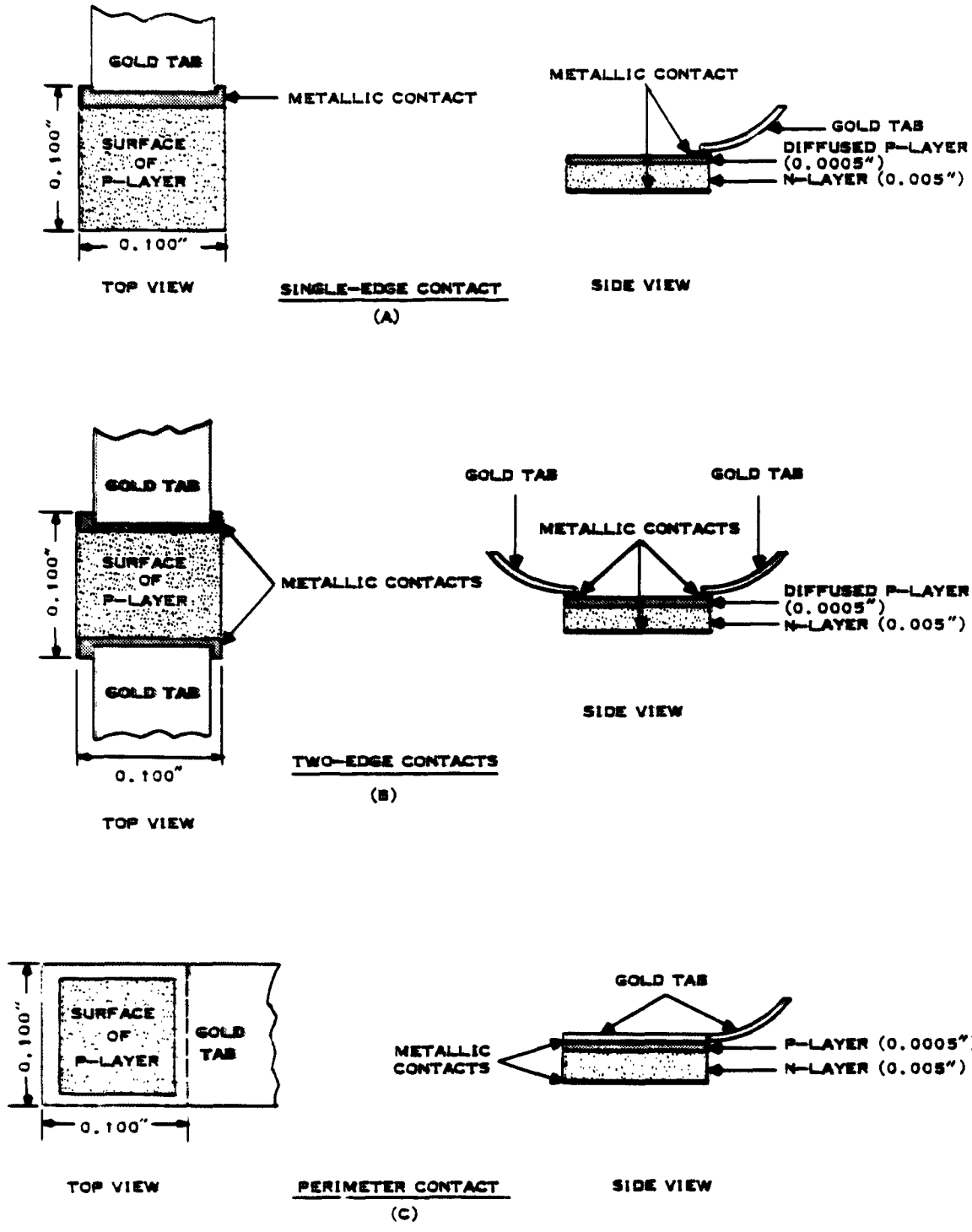
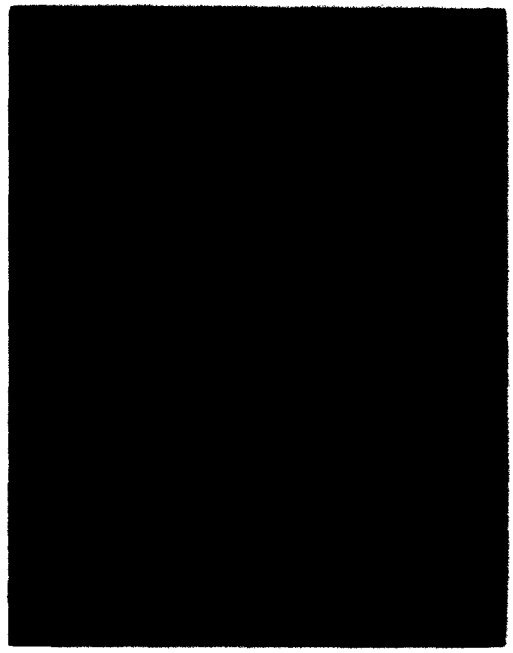
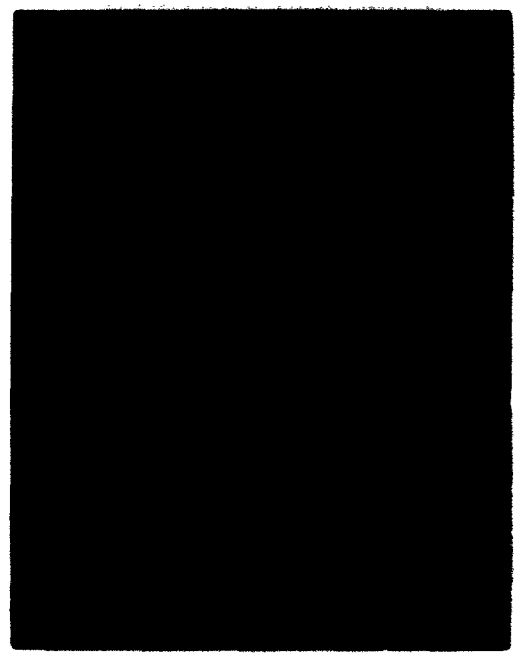


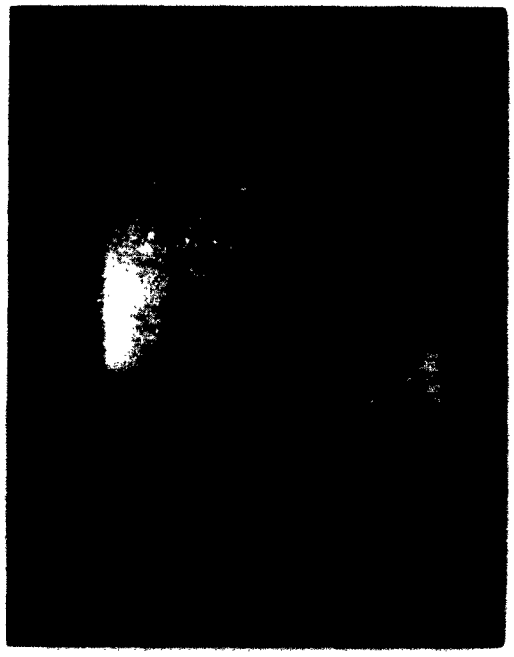
Figure 78. Radiation Source Contact Configurations



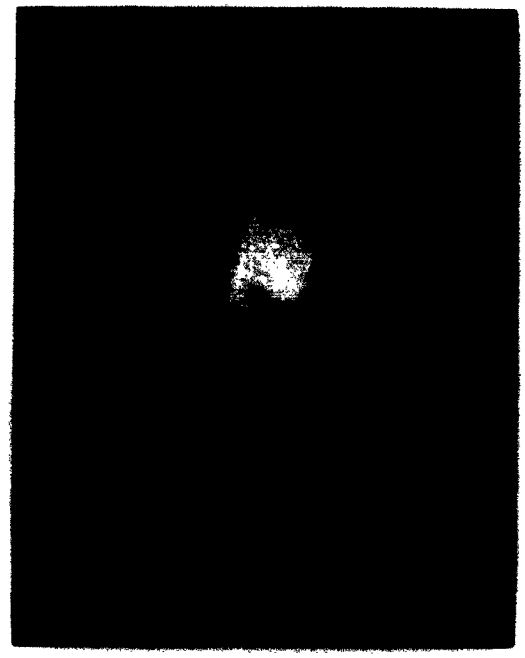
Single-Edge Contact



Two-Edge Contacts



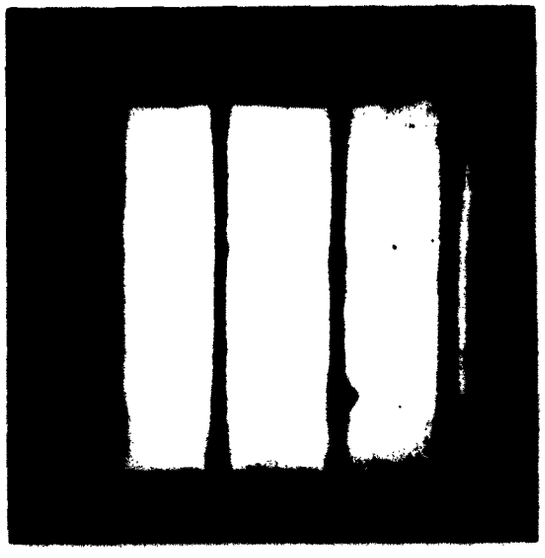
Perimeter Contact



Smaller Unit, Single-Edge Contact

Figure 79. Effects of Contacts and Sheet Resistance

PHOTOGRAPH OF STRUCTURE ILLUSTRATING
USE OF WIRE CONTACTS
DIODE AREA = 75 MILS SQUARE
WIRE DIAMETER = 3 MILS
TO-5 HEADER



INFRARED PHOTOGRAPH OF STRUCTURE ABOVE
WIRES ARE BONDED TO N-LAYER
N-LAYER -0.01Ω-CM, 1.5 MILS THICK
P-LAYER -0.001Ω-CM, 0.5 MIL THICK
DIODE CURRENT = 100 MA

Figure 80. GaAs Diode Infrared Radiation Source

Contacts on these devices have occasionally ruptured during extreme temperature cycling since the thermal expansion coefficient of the wire material does not match that of GaAs. An investigation of other wire materials should lead to a solution.

4.2.3 Emission Diode V-I Characteristics

The forward V-I characteristics, representative of several types of emission diodes, are shown in Figure 81. Except for diodes with tunneling currents, as in diode D13-2 (Figure 81), the V-I characteristics can be described in terms of the three regions indicated in Figure 82. In the low-current region, log I is proportional to the factor qV/2kT. With increasing current, the factor approaches qV/kT, whereupon a series (IR) voltage-drop becomes dominant.

A qV/mkT component (where $m \geq 1$) has been attributed to the effect of recombination of carriers in the space-charge region of the PN junction[7]. The low-current-alpha study by P.J. Coppen and W.T. Matzen[8] indicated that this recombination takes place mainly at or near the junction periphery in certain silicon transistor structures. For the emission diodes, the magnitude of the qV/2kT component has also been found to be strongly dependent on the surface condition, with a thorough cleaning being required to reduce the magnitude to the level shown in Figures 81 and 82.

4.2.4 Emission Spectra

The emission spectra at 25°C representative of several GaAs diodes are shown in Figure 83. Absolute values shown in the figure are those measured at the detector for the best unit, diode D14-2. Measurements were made using a Perkin-Elmer Type 13-U Spectrophotometer. The measuring setup is shown schematically in Figure 84. The responses at about 0.9 micron are due to recombination of carriers from the conduction and valence bands. The "tails" or peaks into the longer wavelengths are due to recombinations from intermediate levels in the "forbidden" band. Selecting, for convenience, a wavelength of 1 micron as separating the band-to-band transitions (N_{b-b}) and the intermediate-level transitions ($N_{i-\ell}$), the respective photon rates at the detector (for I = 100 ma) for several diodes are shown below. Also shown are the diode material thicknesses.

Diode No.	Materials Top/Base	N_{b-b} Photons/Sec	$N_{i-\ell}$ Photons/Sec
D5-3	0.4 mil P+/N	1.1×10^{12}	0.3×10^{12}
D9-2	N/0.4 mil P+	0.4×10^{12}	0.7×10^{12}
D13-2	1 mil N+/4 mil P+	1×10^{12}	0.4×10^{12}
D14-2	1.5 mil N/0.5 mil P+	2.3×10^{12}	1.4×10^{12}

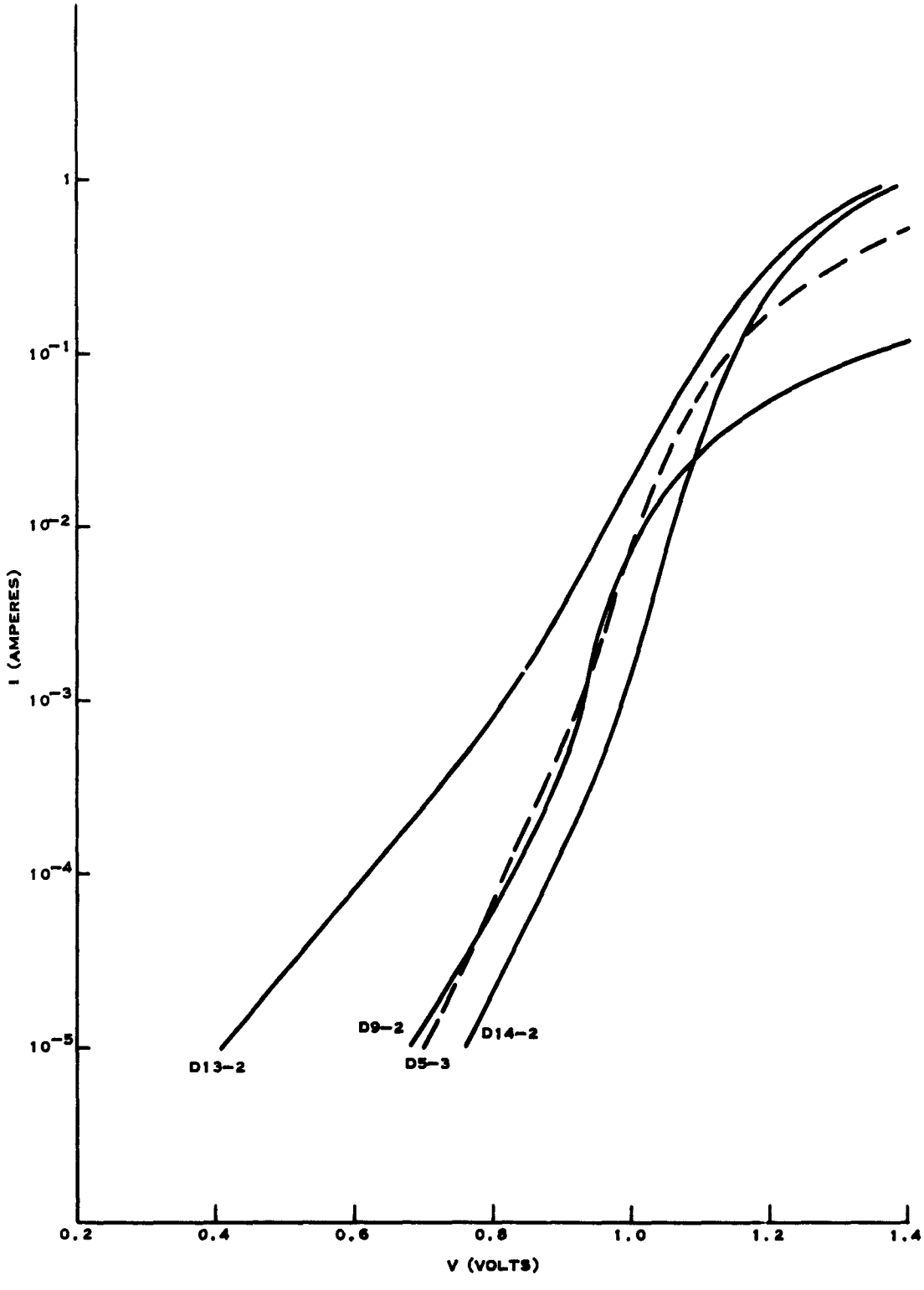


Figure 81. Forward V-I Characteristics for GaAs Diodes

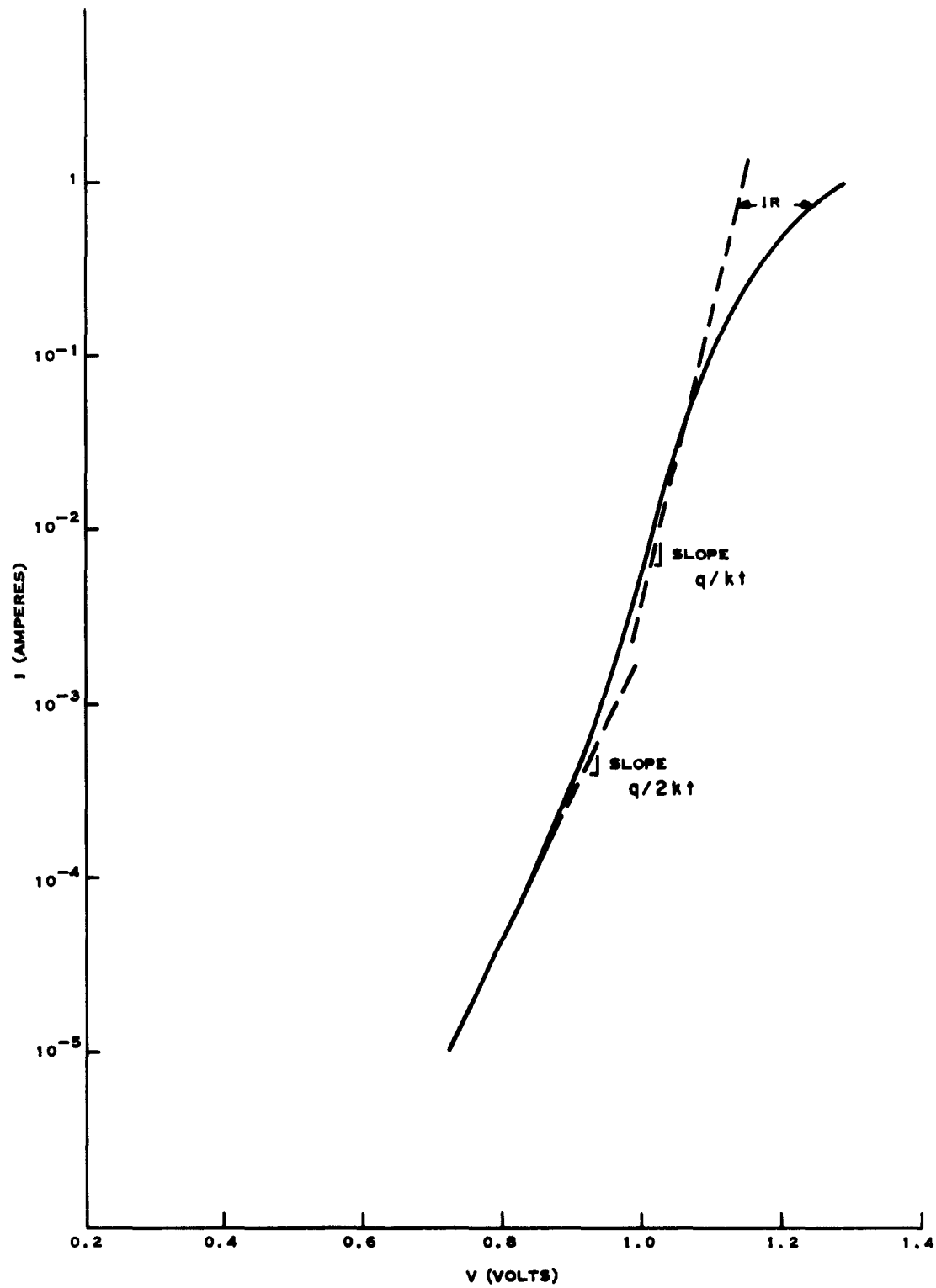


Figure 82. Typical V-I Characteristics

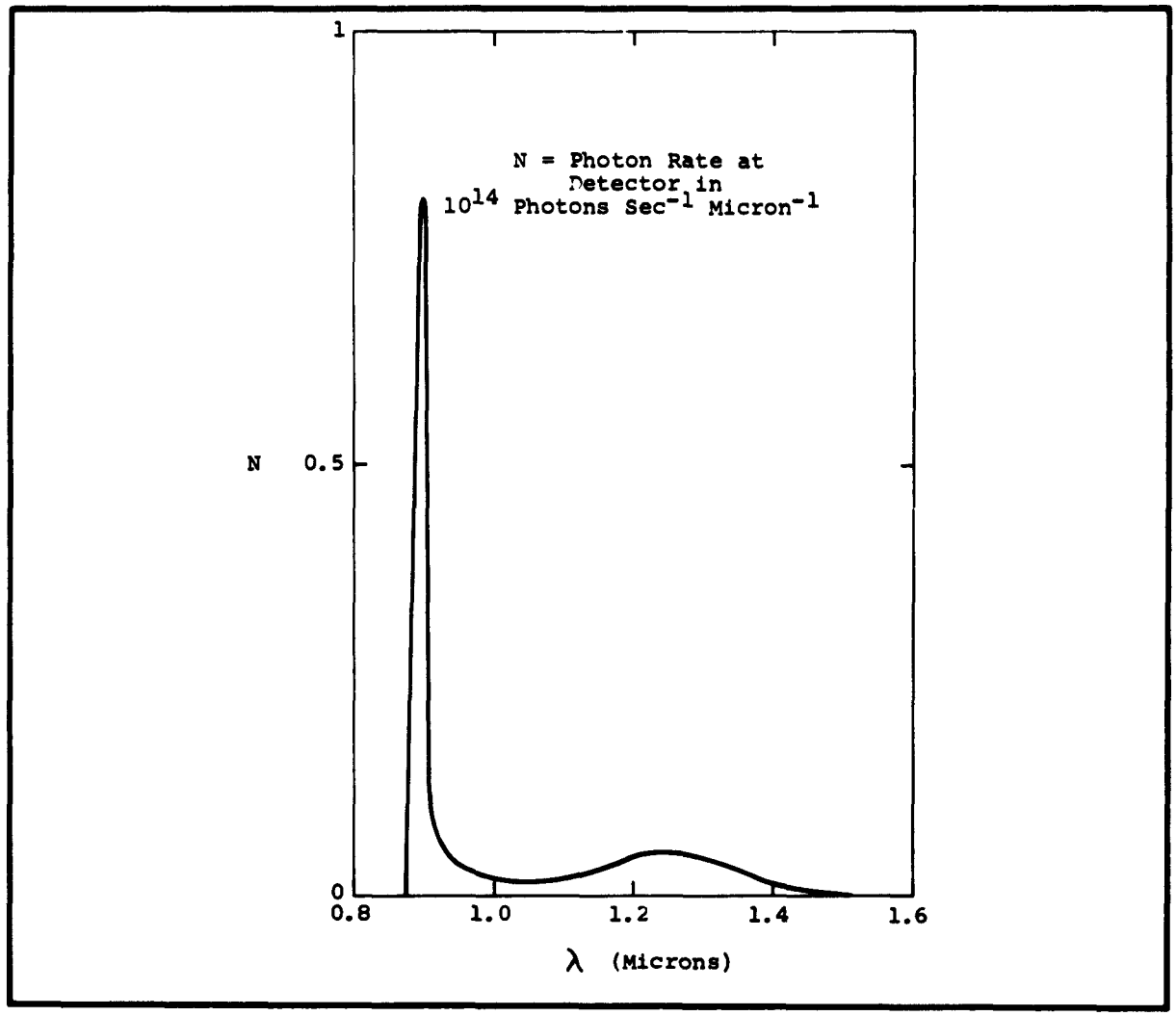


Figure 83. Emission Spectra for GaAs Diode

Preliminary measurements indicate the qV/2kT component of current does not contribute significantly to the emission.

Assuming a simple, semicircular emission intensity pattern, the calculated collection factor to the detector is 0.02. The total photon ratio emitted is then 50 ($N_{b\_b} + N_{i\_\ell}$). For a bias of 100 ma, the minority carrier injection rate is 6.25×10^{17} electrons/sec. For diode D14-2, the quantum efficiency of the external emission is

$$\frac{50\,(3.7 \times 10^{12})}{6.25 \times 10^{17}} \cong \frac{1 \text{ photon}}{3000 \text{ electrons}} .$$

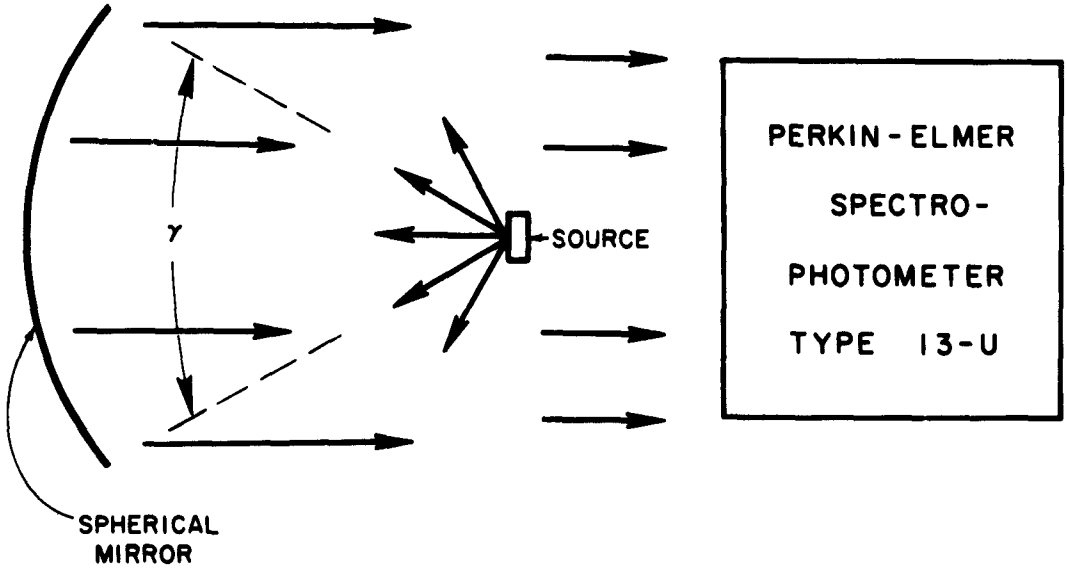


Figure 84. Setup for Measuring Magnitude and Spectrum of Lossev Emission

Due to the GaAs-air interface, only about 1.6 percent of the internally generated emission is coupled into air. The internal quantum efficiency is thus

$$\left[\frac{1}{3000}\right]\left[\frac{1}{0.016}\right] \approx \frac{1 \text{ photon}}{48 \text{ electrons}} .$$

4.3 Conclusion

GaAs is an extremely versatile semiconductor material which should find wide use in future integrated circuits. Not only is this material capable of providing the more conventional bipolar and unipolar transistors and diodes but in its high resistivity form it is a sensitive photoconductor and GaAs PN junctions when forward biased provide efficient generation of infrared radiation. As pointed out in another section of this report, GaAs is also piezoelectric.

Investigation of GaAs should continue with particular emphasis on the PN junction infrared source and its applicability to electro-optic FEB's.

SECTION V

THIN-FILM ACTIVE DEVICES

5.1 Principles of Operation

Impetus for this work was provided by the observation of diode action in metal-oxide-metal (M-O-M) film structures using tantalum and titanium and their oxides (Figures 85 and 86). Forward currents of some

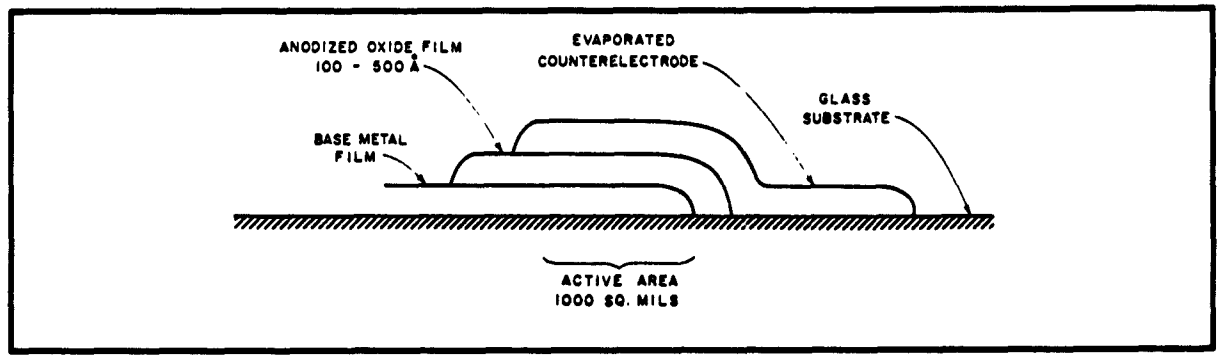


Figure 85. Thin-Film Diodes

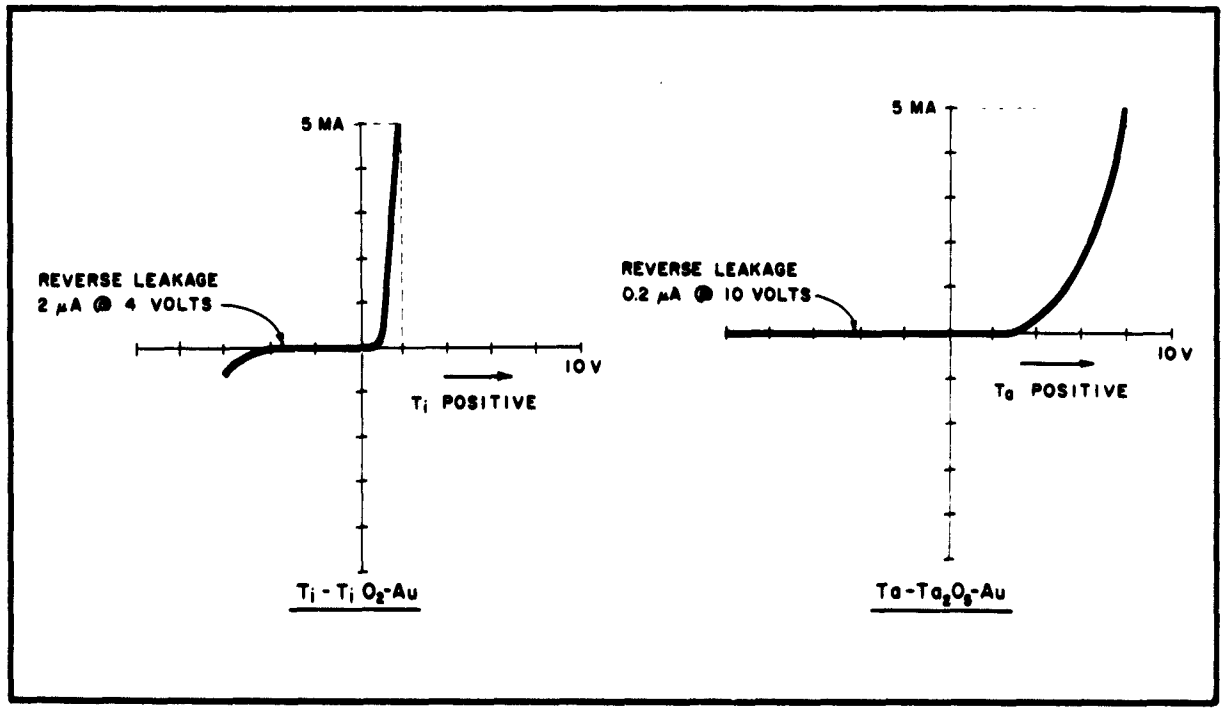


Figure 86. Thin-Film Diodes

tens to hundreds of milliamperes are observed at a few volts bias, with reverse currents in the microampere range, depending on the method of preparation of the device.

Forward current may be explained on the basis of tunneling[9], space-charge-limited current[10], or thermionic emission[11] (Figure 87). Contributions from all three mechanisms probably exist, with the dominant mechanism determined by thickness, ambient temperature, and preparation conditions. In particular, if the oxide is formed anodically, a concentration gradient of tantalum in the oxide is known to exist[12] and should result in a lowering of the effective work function at the tantalum-tantalum oxide interface. Additional evidence for space-charge-limited current is the power-law dependence of current density on field, the slight decay of forward current with time, attributable to the filling of traps in the oxide, and the observation of forward current in relatively thick (1500 Å) oxide films.

5.2 Fabrication of Devices

Tantalum diodes were constructed using both sputtered tantalum films and annealed high-purity sheet as a base material, with oxide coatings formed anodically and by thermal oxidation. Anodic oxide devices had ohmic reverse characteristics up to the formation voltage, at which point destructive breakdown occurred. Thermally oxidized films generally had lower reverse breakdown voltages for equivalent thicknesses, and were electrically noisy. Forward characteristics were similar in both anodic and thermal oxide diodes, with slightly higher current densities observed in the thermally oxidized specimens. Reverse characteristics were quite dependent on the nature of the metal counterelectrode film with reverse current decreasing in the order Ti-Al-Au. This effect may be due partly to work function differences and partly to oxidation of aluminum films in the first phase of evaporation.

Titanium diodes have also been constructed, using the same techniques outlined above. Higher forward current densities are observed for titanium devices than for tantalum devices, for equivalent thicknesses. Thermally formed oxides are known to be more crystalline than those formed by anodization[13], and considerably higher forward current is observed in thermally formed diodes. This result is consistent with the assumption of current limited by space-charge trapped in the oxide layer. Band structures derived from published work functions[14, 15] support the idea that electrons are injected into the oxide at an ohmic contact between titanium and titanium oxide (Figure 88). A very slight forward current is observed in aluminum-aluminum oxide-aluminum structures. Again, the observed characteristics are consistent with an energy-band structure derived from published data.

5.3 Electrical Properties

The above devices unquestionably show stable, reproducible diode characteristics; their immediate application to practical circuits is limited,

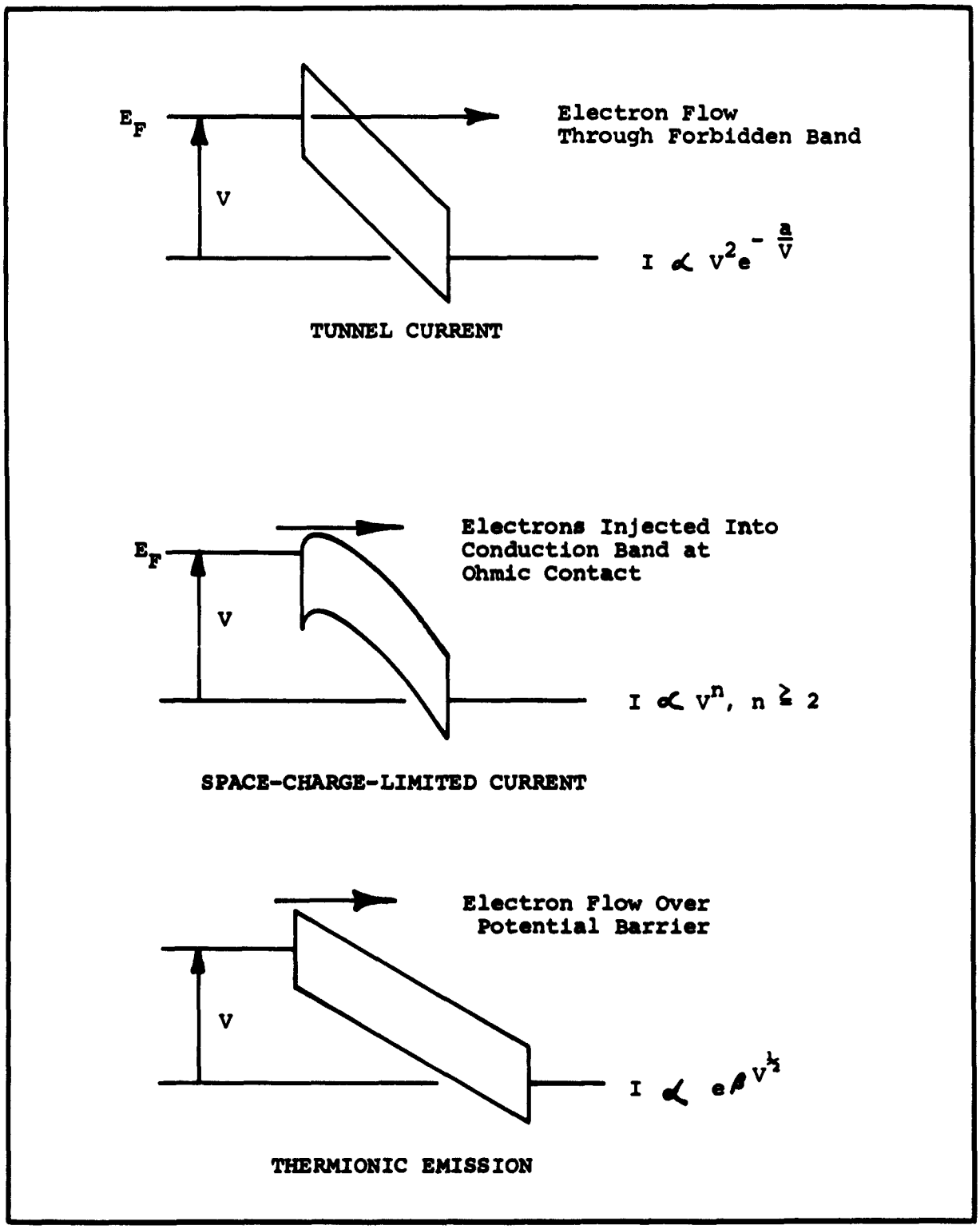


Figure 87. Current Flow Mechanisms

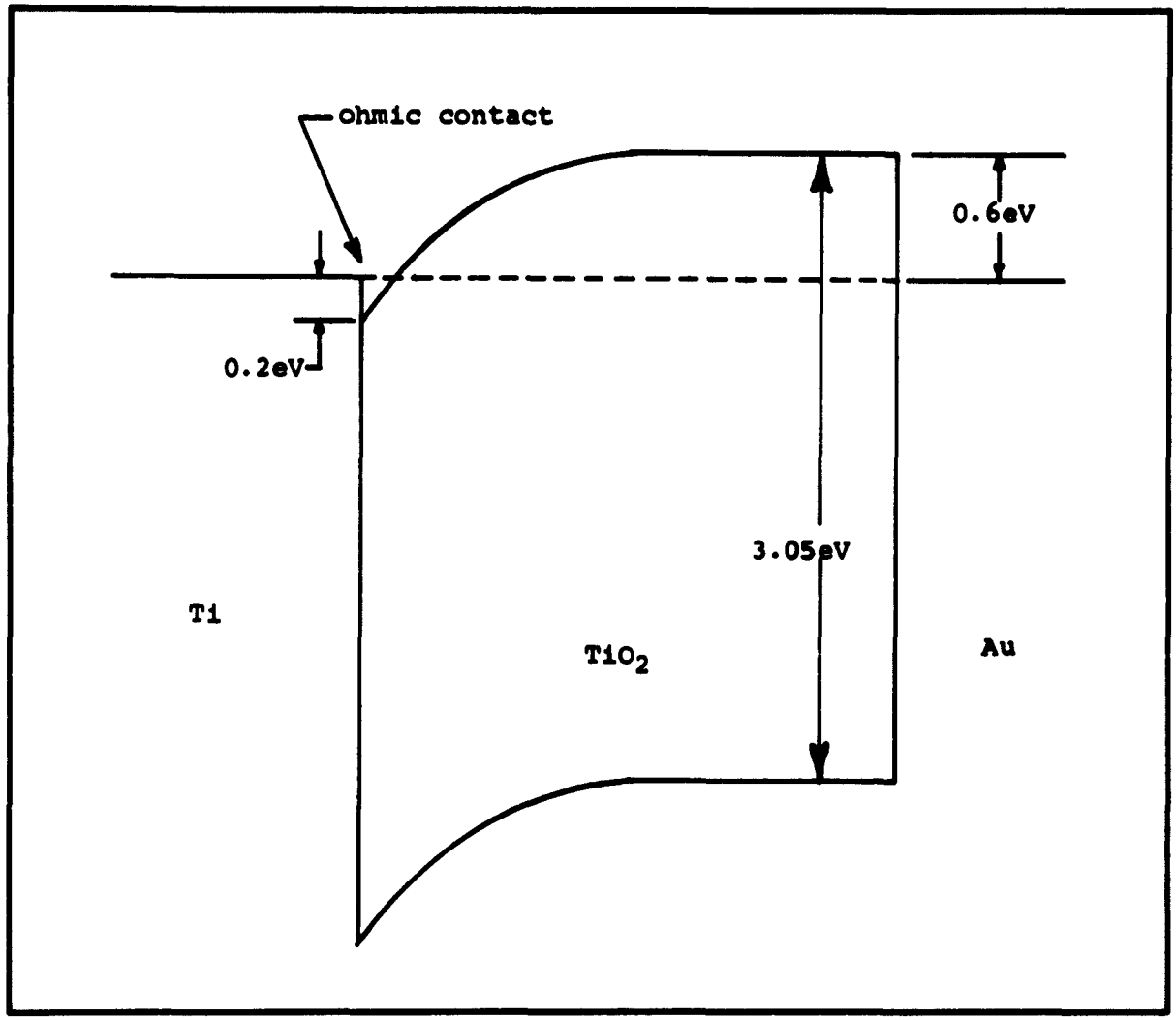


Figure 88. Titanium Diode Energy Diagram

however, by the large capacitance associated with the M-O-M structures. This limitation can be overcome in principle by reduction of electron trap concentration in the oxide layers, which would allow higher current densities to be obtained. As a result, dimensions of practical devices could be reduced with an associated decrease in capacitance. There is evidence that trap densities can be controlled by formation conditions and by doping; these developments will be dealt with below.

Present work on diode structures is designed to improve electrical characteristics of the structures outlined above. In particular, reverse voltage in present Ti-TiO_2-Au structures is limited to approximately 5 volts before conduction occurs. Reverse voltage may be increased by increasing TiO_2 thickness, but only at a sacrifice in forward current. Forward "voltage drop"

for $Ta\text{-}Ta_2O_5\text{-}Au$ structures is undesirably high, of the order of 2 volts or more, depending on oxide film thickness. The most serious obstacle to practical circuit use, however, is the high capacitance density associated with the diode structures. This capacitance combines with external circuit resistance to differentiate input voltage pulses. This effect may be overcome by reduction of trap densities, as shown below.

A figure of merit has been established for thin-film diodes. This figure is:

$$F = \frac{I_F V_R}{C}$$

where

I_F = forward current in mA at 1 volt bias

V_R = reverse breakdown voltage

C = capacitance in pf.

For space-charge-limited forward current, the figure of merit is related to insulator characteristics as.

$$F \propto \frac{1}{tN_t}$$

where

t = dielectric thickness

N_t = density of traps.

The figure of merit neglects the effect of minority-carrier storage since this effect is not expected to occur in the space-charge structure. F is tabulated below for several types of diodes.

Diode	F
TI-6	10
1N660	90
$Ti\text{-}TiO_2\text{-}Au$	10^{-3}
$Ta\text{-}Ta_2O_5\text{-}Au$	10^{-4}.

5.4 Recommendations for Future Work

The density of traps is strongly dependent on purity and crystallinity of the insulator film. Values of N_t range from zero for a perfect single crystal to over 10^{20} cm^{-3} for amorphous material. Present trap concentrations for $Ti\text{-}TiO_2$ structures are probably in the range of 10^{17} to 10^{18} cm^{-3}.

Obviously considerable room for improvement exists in this area. Efforts to decrease trap concentrations consist now of annealing films at high temperature to improve crystallinity, and production of purer starting films by improvements in deposition methods.

Future work on diode structures should be concerned with improvement of the figure of merit F. Several areas of work are envisioned, involving reduction of trapping effects and investigation of high work-function counter-electrode materials.

Reduction of trap concentrations by heat treatment, and consequent improvement in forward characteristics has been shown to be feasible. Optimum time-temperature exposures for various materials have not yet been determined, however. This problem is closely related to that of growing single crystals. One possibility is the use of a swept electron beam for zone recrystallization in situ. This method is attractive in that very high temperature gradients and small penetration depths can be maintained with electron-beam techniques.

The effects of deep traps (traps lying below the quiescent Fermi level) can be reduced by filling these traps with electrons from ionized shallow donors [16]. Thus deep traps are effectively traded for shallow traps. Since shallow traps affect only the magnitude of forward current, while deep traps affect both magnitude and voltage dependence, appropriate doping with shallow donors should measurably improve diode characteristics.

Counterelectrode material and deposition methods have been found to influence both reverse V-I characteristics and capacitance of film diodes. Some of this influence can be explained on the basis of differing work functions between oxide and counterelectrode material, with higher work function materials generally giving rise to lower reverse currents. This effect will be exploited by use of materials which are known to have high work functions against vacuum, such as platinum (5.3 eV), nickel (5.0 eV), palladium (5.0 eV), and copper (4.9 to 5.6 eV). Several of these materials can be evaporated at practical rates with high purity only by electron-beam techniques.

Characterization of film diode structures is at present limited to low-frequency properties, with a few experiments concerned with switching characteristics. High frequency characteristics have been largely unexplored. Typical of high-frequency data needed are variation of rectification ratio and capacitance with frequency. In addition, pulse response characteristics can be used to define trap densities and trap locations in both energy and space [17].

Locations and densities of traps can also be determined by detailed analysis of dc V-I characteristics [10,18]. Variations of diode properties with temperature and bias conditions can be used to elucidate the current transport mechanisms in materials of interest.

In addition to the work on Ta_2O_5 and TiO_2, materials such as BeO, SiO_2, BN, and SiC should be evaluated. The properties desirable for

diode use are:

High electron mobility in the conduction band

Ease of producing low trap-density material

Ease of making ohmic contact to the conduction band

Chemical and electronic stability.

SECTION VI

PIEZOELECTRIC EFFECTS IN SEMICONDUCTORS

6.1 Introduction

Mechanically resonant piezoelectric materials are used routinely as filters, transformers, and to control the frequency of oscillators. Many common piezoelectric materials are insulators for which active device technology is not available. The use of these materials as resonant components for integrated networks would be on a separate package or chip basis.

Piezoelectric resonators fabricated in materials which are semiconductors offer the possibility of a new family of integrated network functions. The series of III-V and II-VI compound semiconductors are known (due to symmetry) to have piezoelectric properties. However, the magnitude of the elastic and piezoelectric constants of these materials is not known.

The following section describes the measurement of the elastic and piezoelectric constants of the III-V compound semiconductor Gallium Arsenide (GaAs). This material was chosen for measurement over other III-V and II-VI compounds because:

High quality high resistivity (>10^7 ohm-cm) GaAs material is available within Texas Instruments.

The technology for the construction of conventional active devices is more advanced for GaAs.

The measurement of the temperature coefficients of the elastic constants and the temperature coefficient of the series resonant frequency is described.

The piezoelectric properties of GaAs are compared to other common piezoelectric materials with respect to mounting characteristics and electromechanical coupling coefficient.

6.2 Elastic and Piezoelectric Properties of GaAs

GaAs is a cubic (isometric) crystal of the zinc blend type. The elasto-piezo-dielectric matrix [19] of this crystal class (Schoenflies symbol — T_d) is shown in Figure 89. The matrix array of Figure 89 shows that GaAs has three independent elastic constants, one independent piezoelectric constant, and one independent dielectric (permittivity) constant. The matrix shorthand of Figure 89 is expanded as a set of simultaneous equations in Figure 90.

Figure 90 describes the elasto-piezo-dielectric properties of GaAs when the coordinate axes (x, y, z) are aligned with the IRE standard [20] crystal axes. The definitions [19] of the symbols used in Figure 90 are given in Table 4.

$$s = \begin{vmatrix} s_{11} & s_{12} & s_{12} & 0 & 0 & 0 \\ s_{12} & s_{11} & s_{12} & 0 & 0 & 0 \\ s_{12} & s_{12} & s_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{44} \end{vmatrix}$$

Mechanical Matrix

$$d = \begin{vmatrix} 0 & 0 & 0 & d_{14} & 0 & 0 \\ 0 & 0 & 0 & 0 & d_{14} & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{14} \end{vmatrix}$$

Piezoelectric Matrix

$$\epsilon = \begin{vmatrix} \epsilon_{11} & 0 & 0 \\ 0 & \epsilon_{11} & 0 \\ 0 & 0 & \epsilon_{11} \end{vmatrix}$$

Dielectric Matrix

Figure 89. Elastic-Piezoelectric and Dielectric Matrices of GaAs, 100 Plane

The absence of elastic constants in the shear-longitudinal cross coupling positions indicates that pure longitudinal or shear modes can be excited in GaAs.

In particular, the equations in Figure 90 illustrate the presence of a pure face shear mode in GaAs which can be excited by an electric field perpendicular to a (100) plane; i.e., a "z" electric field will generate an (x y) face shear.

6.2.1 Rotation of the Coordinate Axes

The characteristics of GaAs (or any other crystal) with the coordinate axes oriented other than along the IRE standard axes can be determined

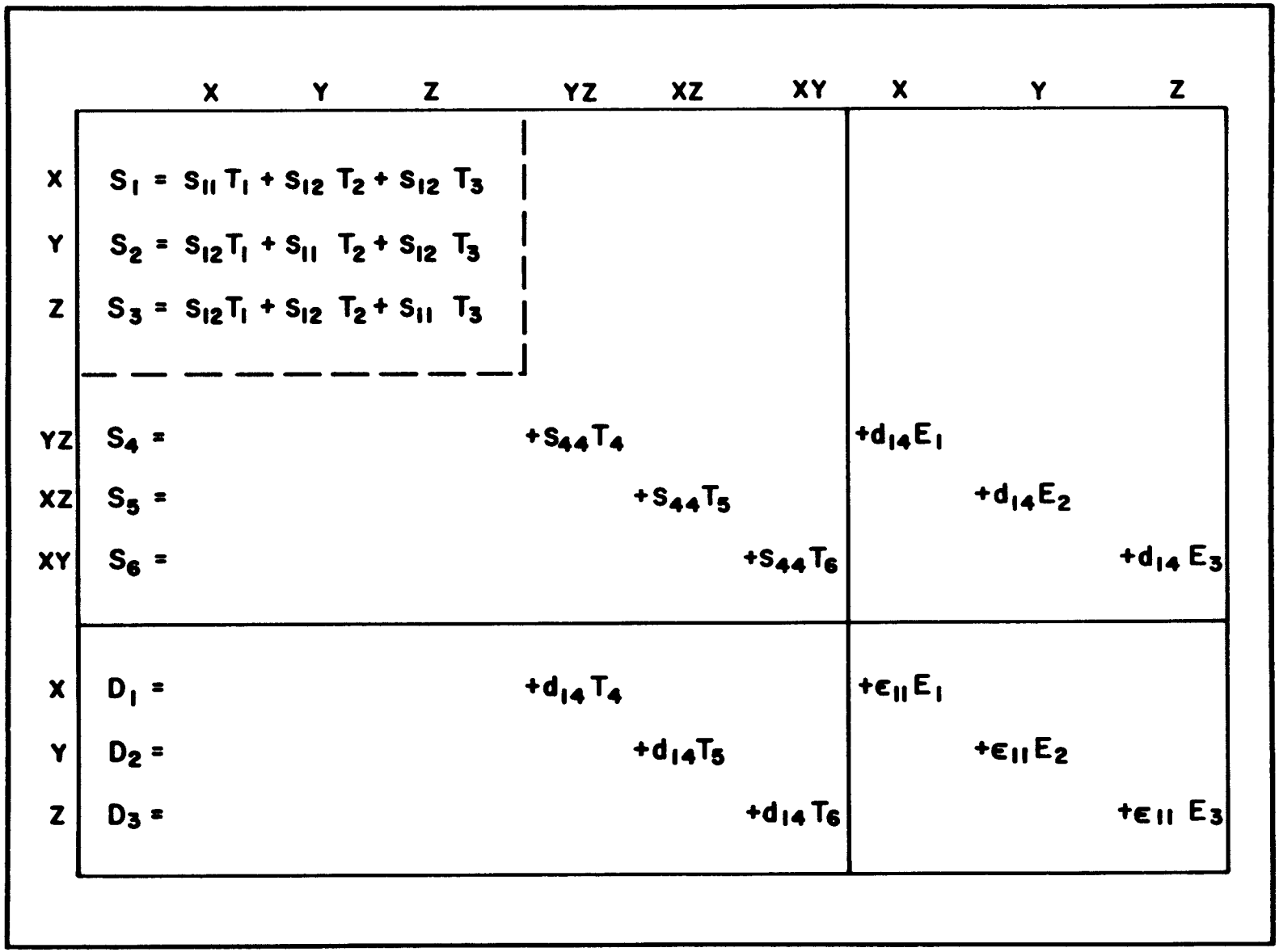


Figure 90. Piezoelectric Relations GaAs

TABLE 4

DEFINITIONS OF SYMBOLS USED IN FIGURE 74

Symbol	Quantity	Mks Units
T	Stress	Newton per (meter)^2
S	Strain ($\Delta \ell/\ell$)	Dimensionless
E	Electric field	Volt per meter
D	Electric displacement	Coulomb per (meter)^2
c^E	Elastic stiffness (E = constant)	Newton per (meter)^2
s^E	Elastic compliance	(Meter)^2 per newton
T	Permittivity (T = constant)	Farad per meter
d	Piezoelectric strain-constant	Coulomb per newton or meter per volt
e	Piezoelectric stress-constant	Coulomb per (meter)^2
k	Coupling coefficient	Dimensionless

by modifying the s, d, and ϵ matrices. This modification is performed by considering the elastic, piezoelectric, and dielectric properties as tensors and calculating the modified constants from the general tensor formula. An alternate approach is to use a matrix multiplication technique suggested by W.L. Bond[21].

The modified s, d, and ϵ matrices (s', d', and ϵ') can be computed using Bond's method from the equations below:

$$s' = [\alpha_T{}^{-1}]\ [s]\ [\alpha^{-1}] \quad (1)$$

$$d' = [a]\ [d]\ [\alpha^{-1}] \quad (2)$$

$$\epsilon' = [a]\ [\epsilon]\ [a_T] \quad (3)$$

where

α^{-1} is the inverse of the matrix "α"

a_T is the transpose of the matrix "a".

The matrices which "α" and "a" represent depend on the desired angular rotation. Forms of "α" and "a" for rotation of the coordinate axis about the x, y, or z axis are given in Reference 21.

Use of Equations (1), (2), and (3) has been facilitated by a computer program which performs the laborious matrix multiplication. This makes the rapid investigation of new orientations possible. The required input data are the elasto-piezo-dielectric constants for some reference position and the desired rotation (or rotations) in three-dimensional space from the reference. The number of successive rotations possible depends on the accuracy of the input data.

The computer program has been used to determine the elasto-piezo-dielectric matrix of GaAs with the (y' z') plane parallel to the (110) or the (111) plane.

Figure 91 illustrates the shape of the GaAs elasto-piezo-dielectric matrix with the (y' z') plane parallel to a (110) plane and the y' axis parallel to a (100) plane. This matrix indicates a pure thickness shear vibration mode in GaAs which can be driven by an x' electric field applied to a "y' z' " plate. The absence of off-diagonal coupling constants indicates that longitudinal modes will not be coupled.

Figure 92 illustrates the elasto-piezo matrix of GaAs with the (y' z') plane parallel to a (111) plane. The computer program was used to compute the matrix constants as the coordinate axes were rotated in small increments about the x" axis. The x" axis had been placed perpendicular to a (111) plane by two previous rotations. The y' axis lies along a (110) direction for zero degrees rotation about the x" axis.

6.3 Measurement of the Elastic and Piezoelectric Constants of GaAs

6.3.1 Measurement of the Elastic Constants

The IRE standards on piezoelectric crystals[19] lists the elastic and piezoelectric constants which can be determined in cubic crystals from the length extensional mode of bars and the contour modes of thin square plates. This list is given in Table 5 on the following page.

Test crystals of high resistivity GaAs (a cubic crystal) were fabricated to be operated in the above modes. The dimensions, crystallographic orientation, and resonant mode of the test crystals are listed in Table 6. Hereafter, the crystal samples will be referred to as the 22.5° bar, 0° plate etc.

The series and parallel resonant frequencies of the test crystals were calculated[22, 23] from the measured frequency of maximum transmission of the circuits shown in Figures 93 and 94 respectively. The calculations were based on the equivalent circuit of the test crystals near resonance shown in Figure 95.

TABLE 5

MODES FOR OBTAINING PIEZOELECTRIC CONSTANTS

Constant	Mode	Crystal Shape
s_{11}	Length extensional	Long thin bar
$(2s_{12} + s_{44})$	Length extensional	Long thin bar
s_{44}	Contour shear	Thin square plate
s_{44}	Contour extensional Mode I	Thin square plate
d_{14}	Length extensional	Long thin bar

TABLE 6

DIMENSIONS, CRYSTALLOGRAPHIC ORIENTATION, AND RESONANT MODE OF TEST CRYSTALS

Sample No.	Crystal Cut	Dimensions in Mils			Resonant Mode
		Length	Width	Thickness	
1	z x t (22.5°)	382	30	20	Length extensional
2	z x t (32.5°)	205	30	20	Length extensional
3	z x t (45°)	401	30	20	Length extensional
4	z x t (0°)	102	102	10	Contour shear
5	z x t (45°)	96	96	10	Contour extensional Mode I
6	z x t (22.5°)	460	40	15	Length extensional
7	z x t (33°)	460	40	15	Length extensional
8	z x t (45°)	460	40	15	Length extensional

The parallel resonant frequency and series resonant frequency of the test crystals computed from the measured frequencies of maximum transmission are presented in Table 7. The following sections describe the use of the series and parallel resonant frequencies in the calculation of the elastic and piezoelectric constants of GaAs.

$$s' = \begin{vmatrix} s_{11}' & s_{12}' & s_{13}' & 0 & 0 & 0 \\ s_{12}' & s_{11}' & s_{13}' & 0 & 0 & 0 \\ s_{13}' & s_{13}' & s_{33}' & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{66} \end{vmatrix}$$

Mechanical Matrix

$$d' = \begin{vmatrix} 0 & 0 & 0 & 0 & d_{15}' & 0 \\ 0 & 0 & 0 & d_{15}' & 0 & 0 \\ d_{31} & -d_{31} & 0 & 0 & 0 & 0 \end{vmatrix}$$

Piezoelectric Matrix

$$\epsilon' = \begin{vmatrix} \epsilon_{11} & 0 & 0 \\ 0 & \epsilon_{11} & 0 \\ 0 & 0 & \epsilon_{11} \end{vmatrix}$$

Dielectric Matrix

Figure 91. Elastic-Piezoelectric and Dielectric Matrices for the GaAs, 110 Plane

6.3.1.1 Calculation of the Elastic Constants

The resonant frequency of the length extensional mode of a long thin bar is given by Equation (4).

$$f_r = \frac{1}{2\ell} \left[\rho\, s_{11}^{E(\theta)}\right]^{-1/2} \quad (4)$$

where

ρ = Density of the material

ℓ = Length of the bar

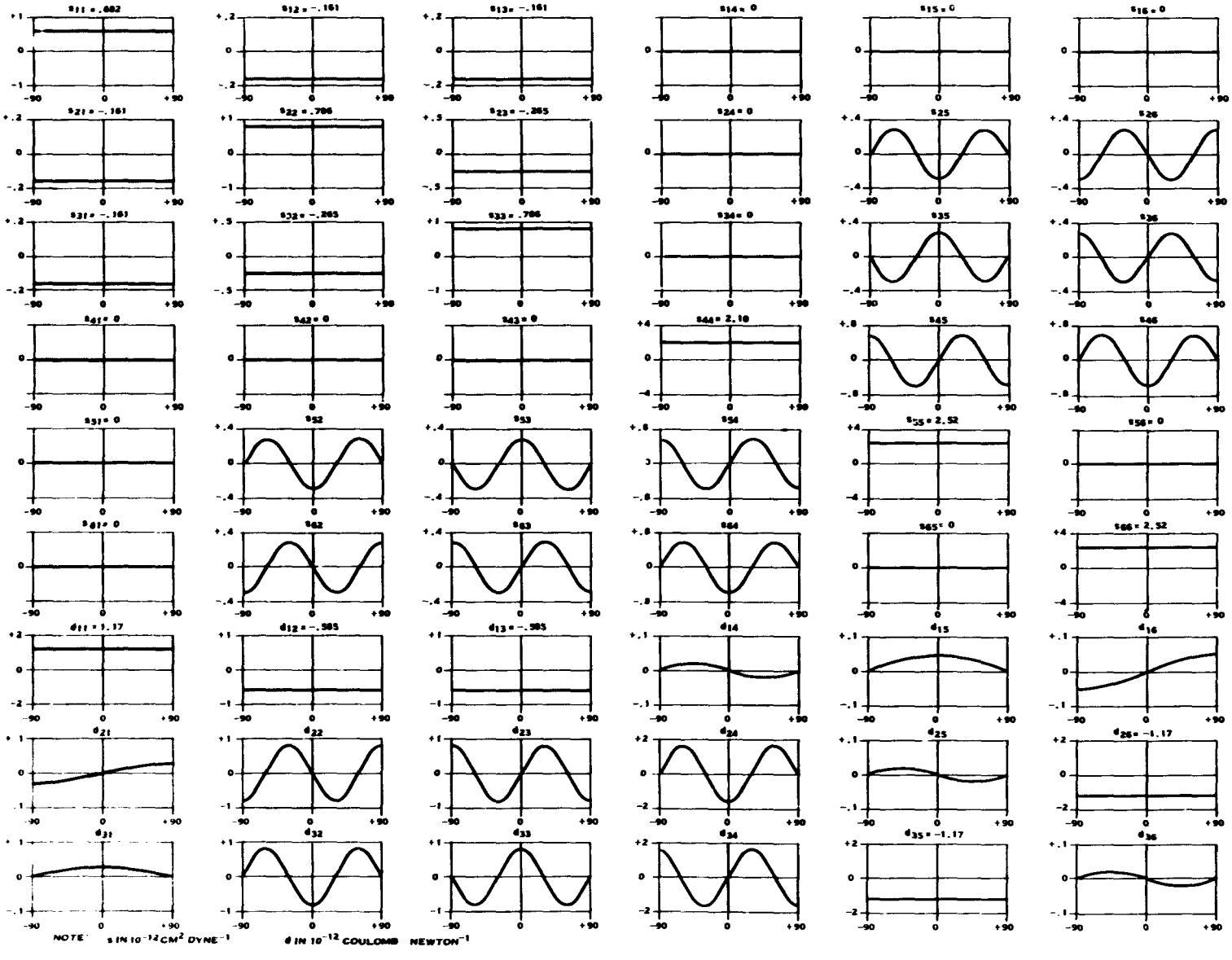


Figure 92. Variations of the Piezoelectric and Elastic Constants of GaAs with Rotation about the X'' Axis

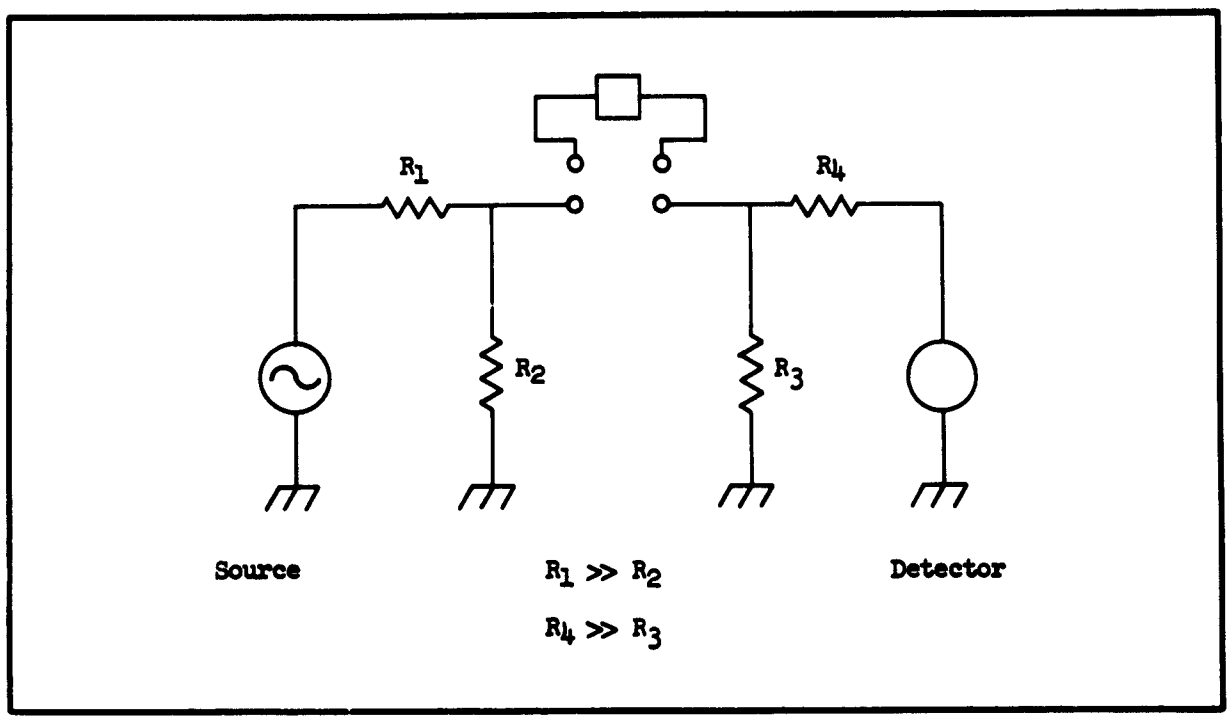


Figure 93. Series Resonance Test Circuit

$s_{11}^{E}(\theta)$ = Elastic strain constant in the direction of the length of the bar. In an anisotropic crystal s_{11}^{E} is a function of crystallographic orientation.*

The face of the test crystals (22° bar, 0° plate etc.) was restricted to lie in the x y (100) plane. This allows $s_{11}(\theta)$ as a function of rotation θ about the z axis to be written as:

$$s_{11}(\theta) = s_{11}(\cos^4\theta + \sin^4\theta) + (2s_{12} + s_{44})\sin^2\theta\cos^2\theta. \quad (5)$$

The constants s_{11} and $(2s_{12} + s_{44})$ can be determined by calculating $s_{11}'(\theta)$ for the 22.5° and 45° bar.

Following from Equation (4) and using the data of Table 7

$$s_{11}' = 1.018 \times 10^{-11} \frac{M^2}{\text{Newton}} \quad \theta = 22.5° \quad (6)$$

$$s_{11}' = 0.835 \times 10^{-11} \frac{M^2}{\text{Newton}} \quad \theta = 45°. \quad (7)$$

*$s_{11}^{E}(\theta)$ is the elastic constant measured at constant field. Throughout the report the superscript "E" will be understood unless specified otherwise.

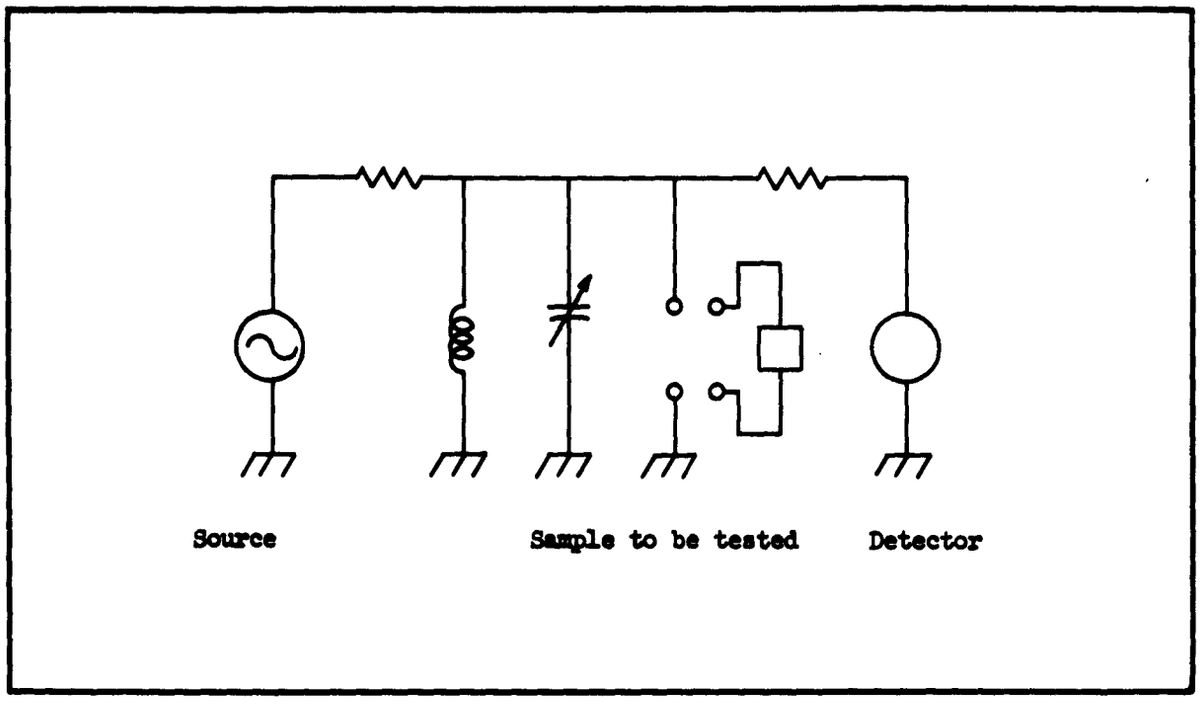


Figure 94. Parallel Resonance Test Circuit

Values of s_{11} and $(2s_{12} + s_{44})$ computed from Equation (5) are:

$$s_{11} = 1.19 \times 10^{-11} \frac{M^2}{\text{Newton}} \tag{8}$$

$$(2s_{12} + s_{44}) = 0.935 \times 10^{-11} \frac{M^2}{\text{Newton}} \ . \tag{9}$$

The elastic constant $s_{11}'(33°)$ calculated from Equation (5) using the values of s_{11} and $(2s_{12} + s_{44})$ previously computed is:

$$s_{11}'(33°) = 0.89 \times 10^{-11} \frac{M^2}{\text{Newton}} \ . \tag{10}$$

This value compares closely to the value for $s_{11}'(33°)$ calculated from the measured resonant frequency of the 33° bar (Table 7). The elastic constant s_{12} was determined by an independent measurement of s_{44}.

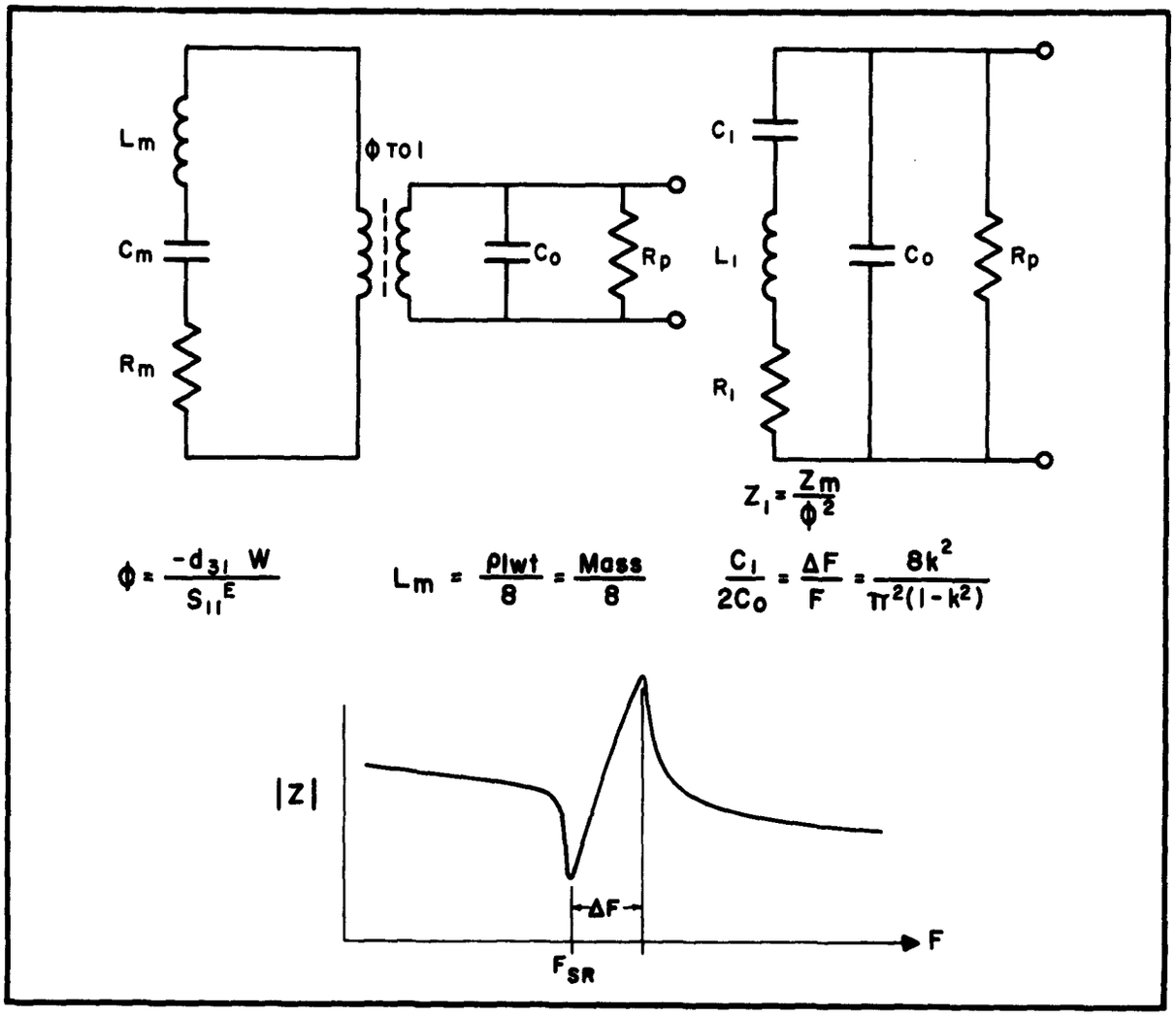


Figure 95. Equivalent Circuit of a Piezoelectric Crystal

TABLE 7

MEASURED ELASTIC AND PIEZOELECTRIC CONSTANTS OF GaAs

Sample No.	Crystal Cut	f_r cps	f_p cps	ρ g/cm³	$s_{11}'(\theta)$ M²/nt	s_{44} M²/nt	k	$d_{31}'(\theta)$ coul/nt	d_{14} coul/nt
6	z x t(22.5°)	183802	183835	5.3	1.018×10^{-11}	–	0.021	0.962×10^{-12}	1.87×10^{-12}
7	z x t(33°)	195316	195385	5.3	0.967×10^{-11}	–	0.0295	0.875×10^{-12}	1.70×10^{-12}
8	z x t(45°)	202904	202985	5.3	0.835×10^{-12}	–	0.0315	0.90×10^{-12}	1.60×10^{-12}
4	z x t(0°)	797750	–	5.3	–	1.80×10^{-11}	–	–	–
5	z x t(15°)	956735	–	5.3	–	1.77×10^{-11}	–	–	–

6.3.1.2 Measurement of s_{44}

The expressions for the resonant frequency of a thin plate are given in Table 8 below:

TABLE 8

RESONANT FREQUENCY OF GaAs CONTOUR MODES

Resonant Frequency	Mode	GaAs Cut
$\frac{0.635}{\ell(\rho s_{44})^{1/2}}$	Contour shear	0° plate
$\frac{0.707}{\ell(\rho s_{44})^{1/2}}$	Contour extensional Mode I	45° plate

The values of s_{44} calculated from the resonant frequency (Table 7) of the contour shear and contour extensional plate are:

Contour shear (0° plate) $$s_{44} = 1.80 \times 10^{-11} \frac{M^2}{\text{Newton}} \quad (11)$$

Contour extensional (45° plate) $$s_{44} = 1.77 \times 10^{-11} \frac{M^2}{\text{Newton}}. \quad (12)$$

Using $s_{44} = 1.735 \times 10^{-11}$ M^2/Newton, s_{12} was determined as

$$s_{12} = -0.425 \times 10^{-11} \frac{M^2}{\text{Newton}} . \quad (13)$$

6.3.1.3 Accuracy of Results

The error in determining the elastic constant (s_{11}') at a known orientation can be calculated from Equation (14) as indicated below:

$$s_{11}' = (4 \ell^2 f_r^2 \rho)^{-1} \pm (2a + 2b + c) \text{ percent} \quad (14)$$

where

(a) = Percent error in determining the length of the bar.

(b) = Percent error in determining the resonant frequency of the bar.

(c) = Percent error in determining the density of the GaAs.

The error from the sum of these causes is expected to be less than 1 percent for the individual elastic constants (s_{11}', s_{44}).

6.3.1.4 Error Due to Orientation

The major error in the measurement of the elastic constants (s_{11}, s_{12}, s_{44}) is the uncertainty in orientation. The single crystal slices from which the experimental bars and plates were cut were oriented by X-ray techniques at the Materials Research Lab to within ±0.25°. Further orientation in our saw section introduced another uncertainty of ±0.1°.

The expected percent errors in the calculated value of s_{11}, s_{12}, and s_{44} can be computed from Equation (5). The expected accuracy of the calculated values of s_{11}, s_{12} and s_{44} is given in Table 9.

TABLE 9

EXPECTED ERRORS ON MEASURED AND REPORTED ELASTIC CONSTANTS

Constant	Measured Value M^2/nt	Reported* Value M^2/nt	% Error in Measured Constant	% Error in Reported Constant
s_{11}' (22.5°)	1.018×10^{-11}	0.998×10^{-11}	±0.7	±1.0
s_{11}' (33°)	0.907×10^{-11}	0.879×10^{-11}	±0.7	±1.0
s_{11}' (45°)	0.835×10^{-11}	0.82×10^{-11}	±0.7	±1.0
s_{11}	1.19×10^{-11}	1.173×10^{-11}	±6.7	±0.98
s_{12}	-0.425×10^{-11}	-0.365×10^{-11}	±28.5	±1.14
s_{44}	1.79×10^{-11}	1.683×10^{-11}	±3.5	±0.14

*Reported Values of the "s" terms were calculated from values of c_{11}, c_{12} and c_{44} reported in Reference 25. In Reference 25, c_{11} and c_{12} are reported with an uncertainty of ±0.14 percent; c_{12} is reported with an uncertainty of ±0.36 percent.

A comparison of our measured results with those reported in the literature is given above in Table 9.

6.3.2 Measurement of the Piezoelectric Strain Constant (d_{14})

The piezoelectric strain constant of GaAs, d_{14}, was calculated from the difference in the electrical series resonant frequency and parallel

resonant frequency of the bars used in the measurement of the elastic constants.

The expression relating the difference in the series and parallel resonant frequency, of a long thin bar plated along its faces, to the piezoelectric strain constant driving the bar is given by Equation (15)[24].

$$[d_{31}'(\theta)]^2 = (\frac{\pi^2}{4})\,[s_{11}'(\theta)]\,[(\epsilon^T{}_{33})]\,(\frac{\Delta f}{f_r})\left[1 + (\frac{4-\pi^2}{4})(\frac{\Delta f}{f_r}) + \text{-----}\right] \tag{15}$$

where

$\Delta f = (f_p - f_r)$ is the difference between the series and parallel resonant frequencies of the bar.

$\epsilon^T{}_{33}$ = the permitivityof GaAs (constant stress)

$d_{31}'(\theta)$ = the piezoelectric strain constant driving the bar.

The piezoelectric strain constant, $d_{31}'(\theta)$, is a function of the orientation of the bar. For the test crystals (orientation restricted to the 100 plane) $d_{31}'(\theta)$ is related to d_{14} by Equation (16).

$$d_{31}' = \frac{d_{14}}{2}\ \text{Sin}\ 2(\theta). \tag{16}$$

The piezoelectric strain constant can be calculated from the data in Table 7, Equations (15) and (16). A sample calculation for the 22.5° bar follows:

$$[d_{31}'(22.5°)]^2 = \frac{\pi^2}{4}\ (1.018)\,(8.85)\,(11)\,(\frac{33}{183})\,(0.99) \times 10^{-26}$$

$$d_{31}'(22.5°) = 0.662 \times 10^{-12}\ \text{coul/nt}. \tag{17}$$

Then from Equation (16), d_{14} is calculated

$$d_{14} = 1.87 \times 10^{-12}\ \text{coul/nt}. \tag{18}$$

The piezoelectric strain constant (d_{14}) computed from the 33° and 45° bars are given in the following equations.

<u>33° Bar</u>

$$d_{31}'(33°) = 0.875 \times 10^{-12}\ \text{coul/nt}$$

$$d_{14} = 1.93 \times 10^{-12}\ \text{coul/nt}. \tag{19}$$

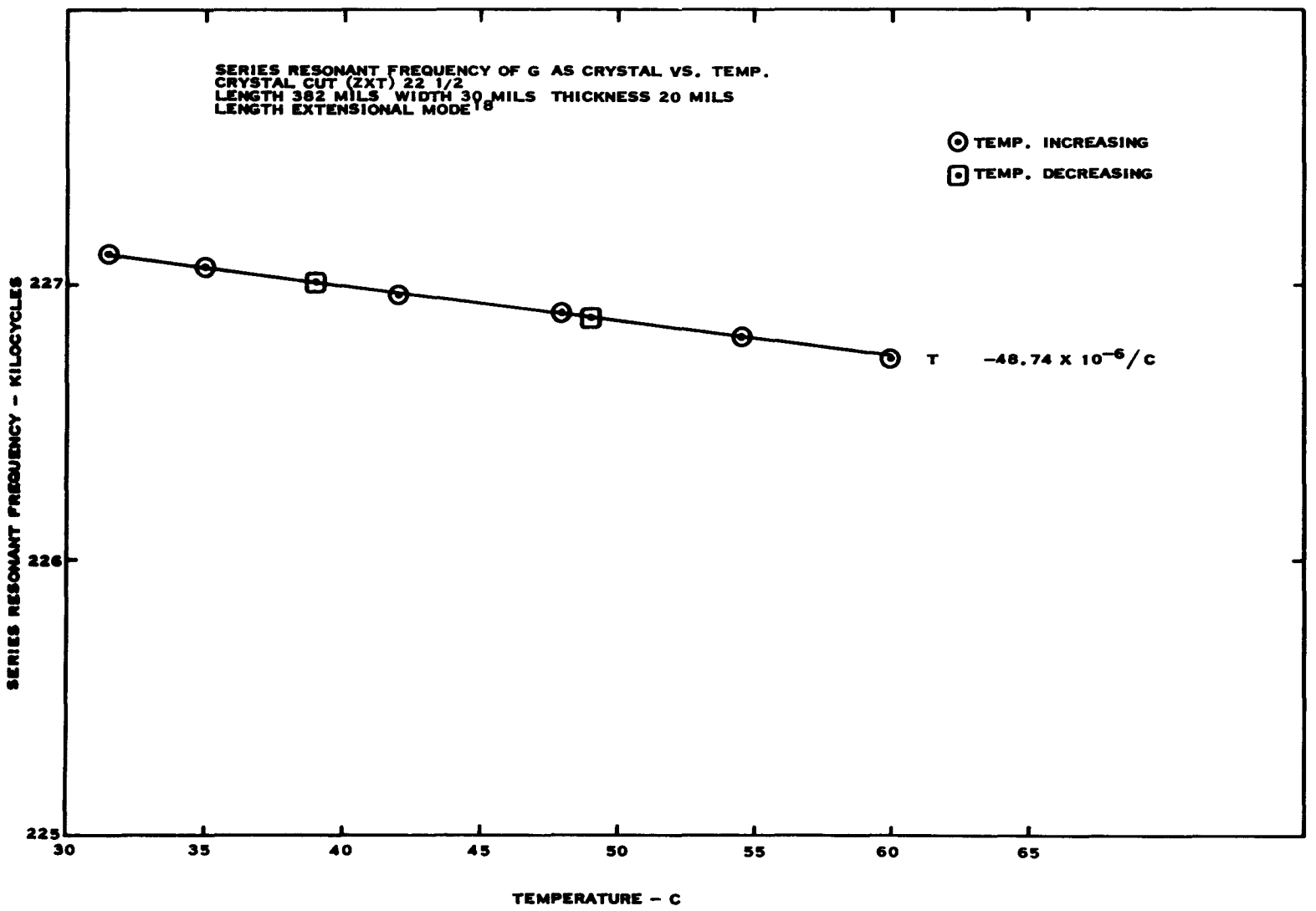


Figure 96. Measured Change in the Series Resonant Frequency of the (22.5° Bar) with Temperature

45° Bar

$$d_{31}\ (45°) = 0.90 \times 10^{-12} \text{ coul/nt}$$

$$d_{14} = 1.80 \times 10^{-12} \text{ coul/nt.} \tag{20}$$

6.3.2.1 Accuracy of Results

The calculated value of d_{14} is expected to be correct within 10 to 12 percent. The bulk of this error occurs in the measurement of the quantity $(f_p - f_r)$, which is about 10 percent. This error reflects an expected error in the measurement of f_p and f_r of

$$f_{meas} = f_r \pm 3 \text{ cps.}$$

The computed values of d_{14} in Table 7 show a maximum spread of roughly 7 percent with an average value of

$$d_{14} = 1.86 \times 10^{-12} \text{ coul/nt.}$$

6.3.2.2 Comparison With Reported Constants

A value for the piezoelectric stress constant (e_{14}) has been quoted[26] in an unpublished report.

$$e_{14} \cong 0.12 \text{ coul/M}^2.$$

The piezoelectric stress constant (e_{14}) can be converted to the piezoelectric strain constant (d_{14}) by Equation (21).

$$d_{14} = e_{14}\, s_{44}$$

thus

$$d_{14} \cong 2 \times 10^{-12} \text{ coul/nt.} \tag{21}$$

This compares favorably to the measured values.

6.3.3 Calculation of the Electromechanical Coupling Factor of GaAs

The electromechanical coupling factor (k) of GaAs for a long thin bar is calculated from Equation (15).

$$k^2 = \left(\frac{\pi^2}{4}\right)\left(\frac{\Delta f}{f_r}\right)\left[1 + \left(\frac{4 - \pi^2}{4}\right)\frac{(\Delta f)}{f_r} + \text{-----}\right] \tag{15}$$

where

$$k^2 = \left[\frac{d_{31}^{\,2}}{s_{11}\,\epsilon_{33}^{\,T}}\right]. \tag{22}$$

The electromechanical coupling factor of a material is a function of orientation. Table 7 lists the values of k, computed from Equation (15), for the 22.5°, 33° and 45° bar. The electromechanical coupling factor for a long thin bar of GaAs (in the 100 plane) is maximum at $\theta = 45°$. Table 10 compares the coupling factor of GaAs ($\theta = 45°$) to typical coupling factors of other piezoelectric materials driven in length extensional modes.

TABLE 10

TYPICAL ELECTROMECHANICAL COUPLING FACTORS OF PIEZOELECTRIC MATERIALS

Material	k
Quartz	0.095
GaAs	0.030
PZT-4	0.30
PZT-5	0.32
CdS	0.20
Ceramic B	0.19

Table 10 points out that coupling factor of GaAs is much smaller than many common materials. The small coupling factor of GaAs makes mounting GaAs crystals more tedious (as will be explained later) and severely restricts the use of GaAs as a wide band transducer material.

6.4 Measurement of the Temperature Coefficients of the Elastic Constants

The temperature coefficient of each of the independent elastic constants ($T_{s_{ij}}$) of GaAs was calculated from the measured temperature coefficient of the series resonant frequency (T_{f_r}) of oriented bars and plates. The measured change in series resonant frequency of the 22.5° bar, 32.5° bar, 45° bar, 0° plate and 45° plate as a function of temperature is presented in Figures 96, 97, 98, 99, and 100. The temperature coefficient of the series resonant frequency is related to the temperature coefficient of the elastic constant controlling resonance by Equation (23).

$$T_{f_r} = \frac{\frac{d f_r}{dT}}{f_r} = \frac{T_\ell}{2} - \frac{T_{s_{ij}}}{2} \qquad (23)$$

where:

$$T_\ell = \frac{\frac{d\ell}{dT}}{\ell} \sim$$ The temperature expansion coefficient of the length. This term has a reported value[26] of $5.9 \times 10^{-6}/°C$ for GaAs at 40°C.

$$T_{s_{ij}} = \frac{\frac{ds_{ij}}{dT}}{s_{ij}} \sim$$ The temperature coefficient of the elastic constant controlling series resonance.

Alternately Equation (25) can be expressed

$$T_{f_r} = 2.95 \times 10^{-6} - \left(\frac{1}{2}\right) \left[\frac{\frac{ds_{11}(\theta)}{dT}}{s_{11}'(\theta)}\right] . \qquad (24)$$

The temperature coefficient of the elastic constant can be computed using Equations (24) and (25) and the data given in Figures 96 through 100. These computed constants are presented in Table 11.

TABLE 11

DATA FOR DETERMINING THE TEMPERATURE COEFFICIENTS OF THE ELASTIC CONSTANTS OF GaAs

Sample No.	Crystal Cut	f_r(40°C) Kilocycles	$s_{11}'(\theta)$ $\times 10^{-11} M^2/nt$	T_{f_r} $\times 10^{-6}/°C$	$T_{s_{11}'}(\theta)$ $\times 10^{-6}/°C$	$\frac{ds_{11}'(\theta)}{dT}$ $\times 10^{-17} M^2/nt-°C$
1	z x t (22.5°)	227.00	0.973	-58.74	123.38	120
2	z x t (32.5°)	451.70	0.855	-58.88	123.66	105.7
3	z x t (45°)	238.38	0.802	-59.05	124.0	99.5
Sample No.	Crystal Cut	f_r(40°C) Kilocycles	s_{44} $\times 10^{-11} M^2/nt$	T_{f_r} $\times 10^{-6}/°C$	$T_{s_{44}}$ $\times 10^{-6}/°C$	ds_{44}/dT $\times 10^{-17} M^2/nt-°C$
4	z x t (0°)	795.75	1.80	-59.2	124.3	224.0
	$\frac{ds_{11}}{dT} = 140 \times 10^{-17} M^2/(nt - °C)$			$T_{s_{11}} = 122.2 \times 10^{-6}/°C$		
	$\frac{ds_{12}}{dT} = -53.6 \times 10^{-17} M^2/(nt - °C)$			$T_{s_{12}} = 123.2 \times 10^{-6}/°C$		
	$\frac{ds_{44}}{dT} = 224 \times 10^{-17} M^2/(nt - °C)$			$T_{s_{44}} = 124.7 \times 10^{-6}/°C$		

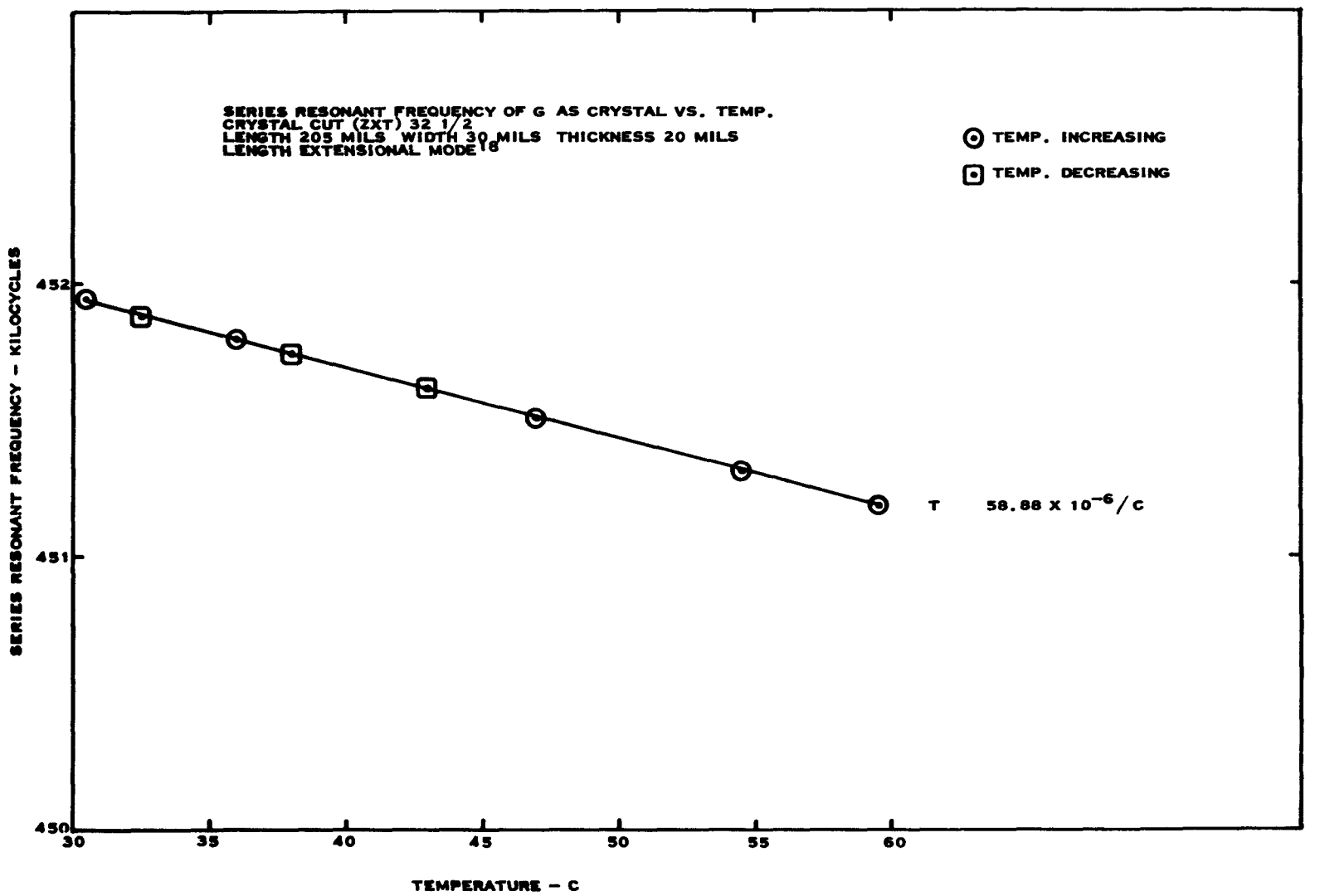


Figure 97. Measured Change in Series Resonant Frequency of the 32.5° Bar

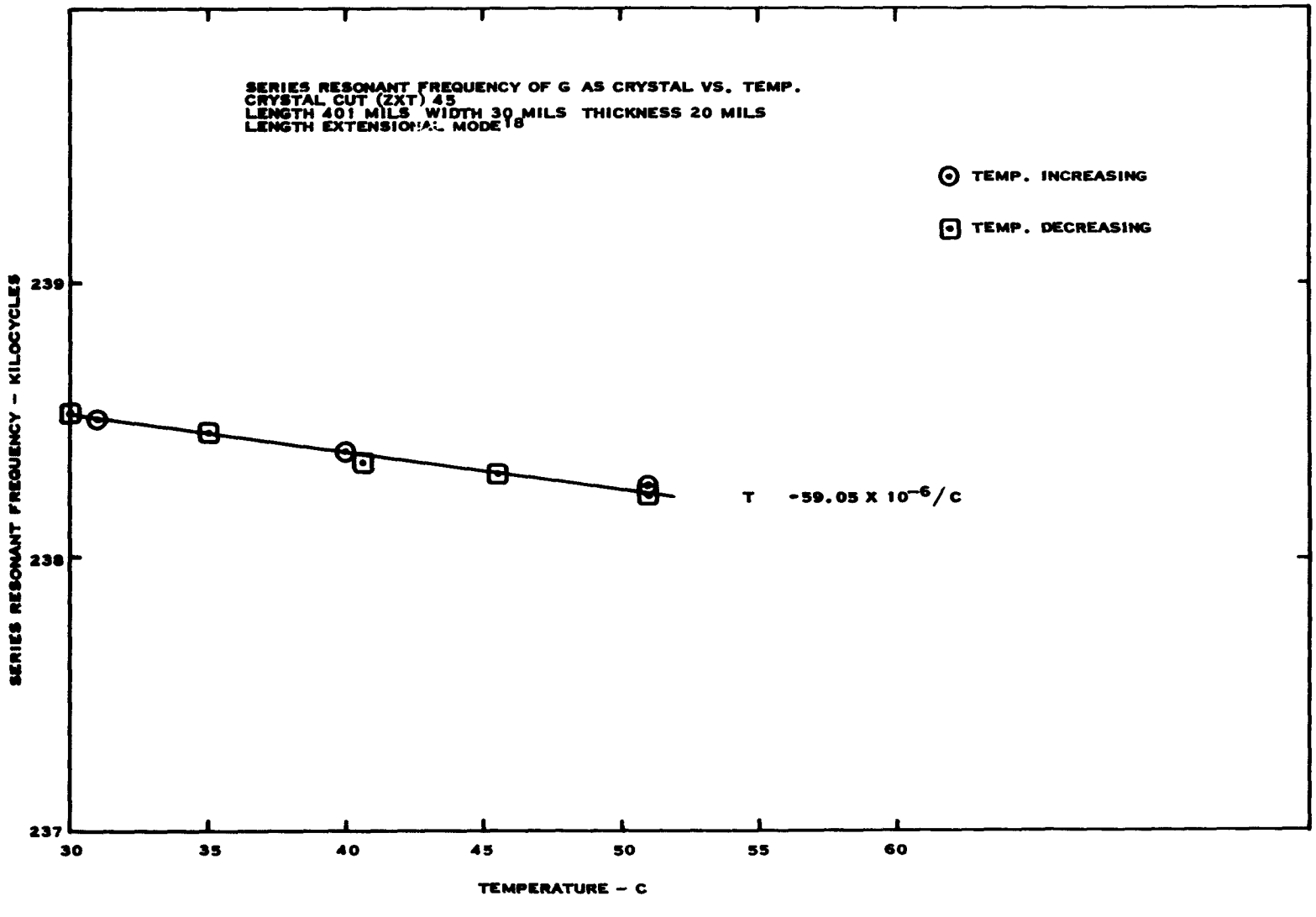


Figure 98. Measured Change in Series Resonant Frequency of the 45° Bar

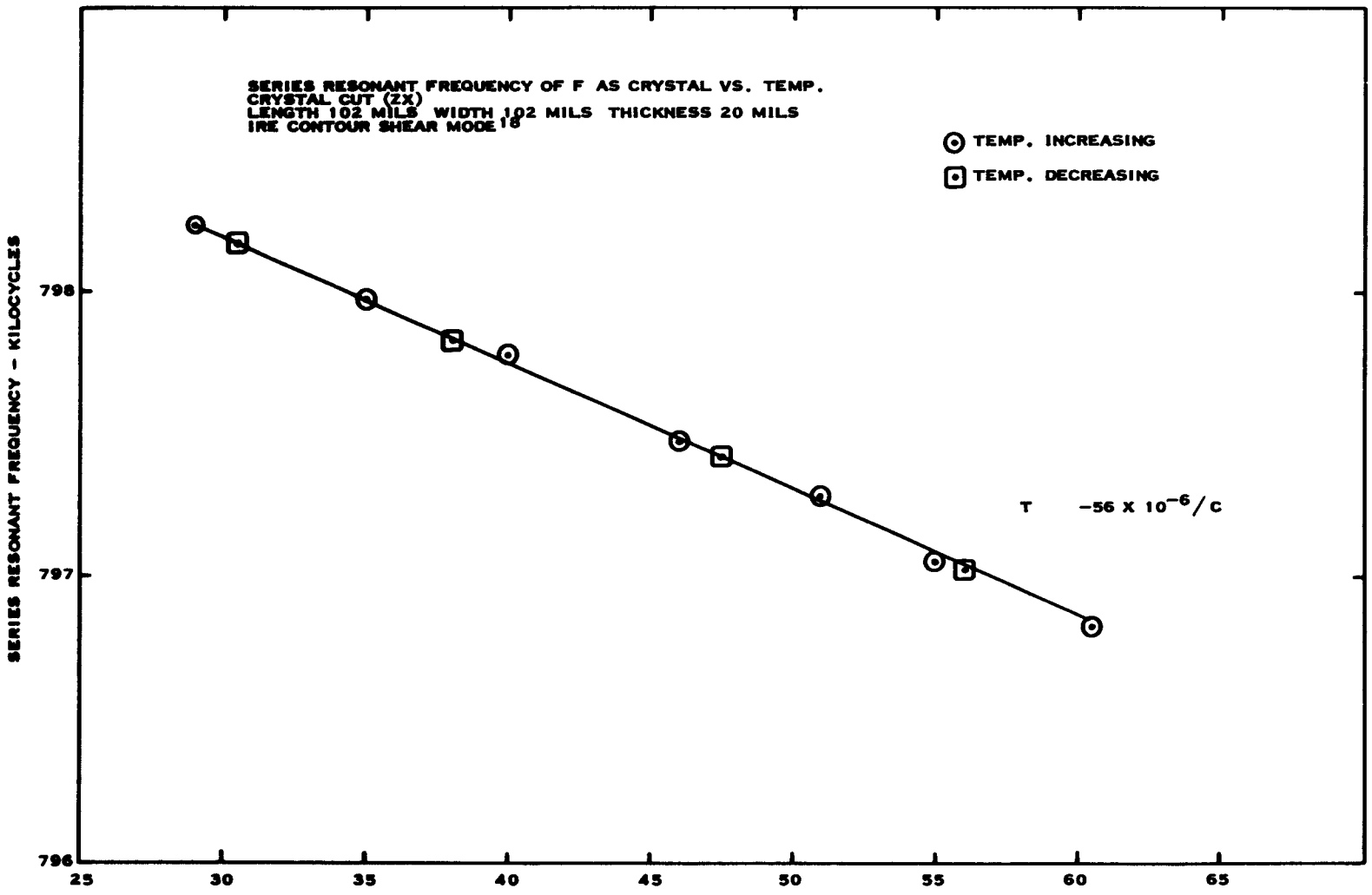


Figure 99. Measured Change in Series Resonant Frequency of the 0° Plate

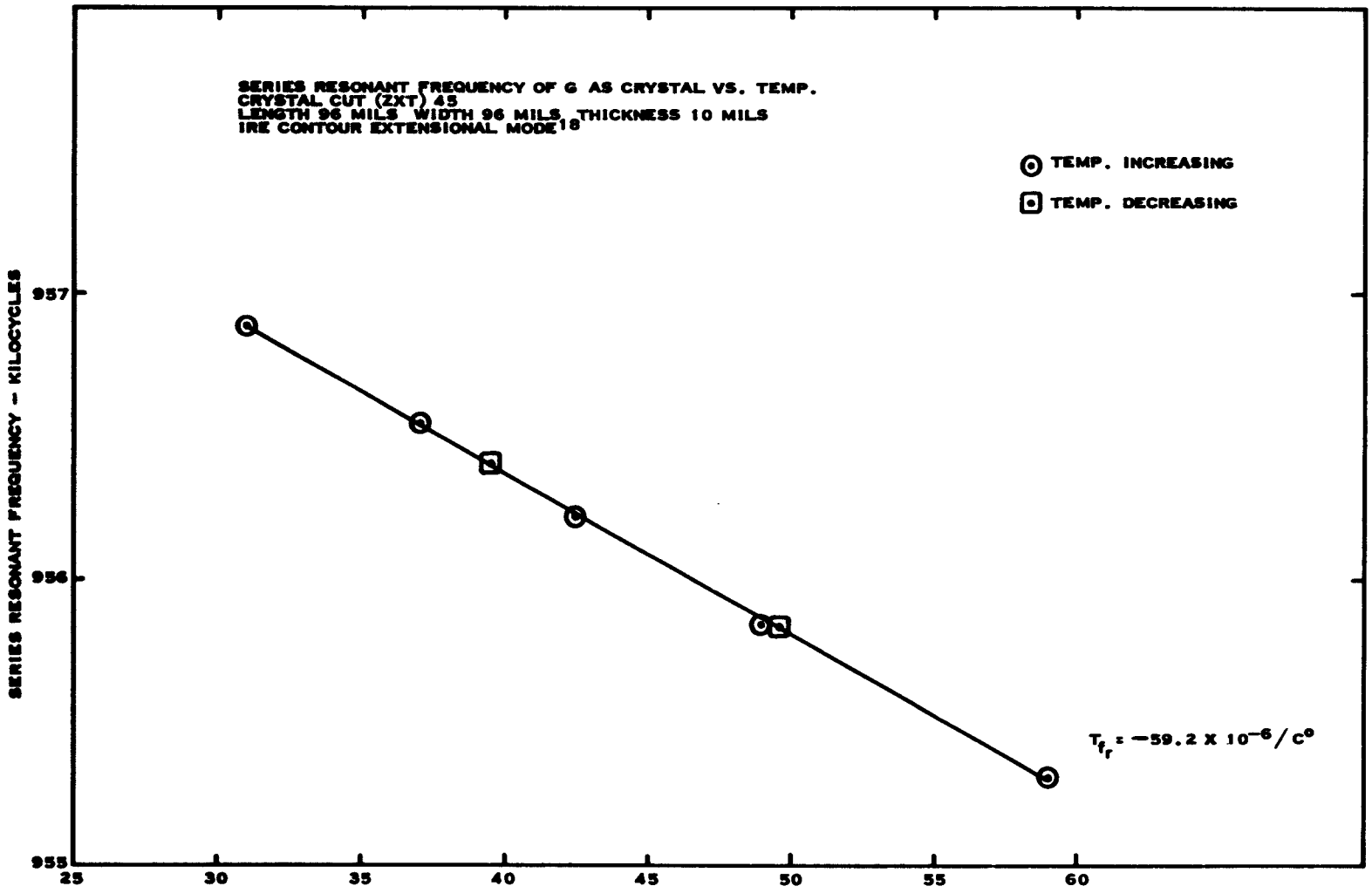


Figure 100. Measured Change in Series Resonant Frequency of the 45° Plate

6.4.1 Zero Temperature Coefficient Orientation

Temperature coefficient of the series resonant frequency of both extensional and contour modes as a function of the independent elastic constants, the crystallographic orientation of the sample, and the derivatives of the independent elastic constants with respect to temperature are given[24] by Equations (25) and (26) below.

Length Extensional

$$T_{f_r} = 2.95 \times 10^{-6} - \left(\frac{1}{2}\right) \left\{ \frac{\left(\frac{ds_{11}}{dT}\right) A + \left[2\left(\frac{ds_{12}}{dT}\right) + \left(\frac{ds_{44}}{dT}\right)\right] B}{(s_{11}) A \quad (2s_{12} + s_{44}) B} \right\} \quad (25)$$

Contour Modes

$$T_{f_r} = 2.95 \times 10^{-6} - \left(\frac{1}{2}\right) \left[\frac{\left(\frac{ds_{11}}{dT}\right) C + \left(\frac{ds_{12}}{dT}\right) D + \left(\frac{ds_{44}}{dT}\right) E}{(s_{11}) C + (s_{12}) D + (s_{44}) E} \right] \quad (26)$$

A, B, C, D, and E in Equations (25) and (26) represent rather complex orientation dependent expressions. The terms contained in A, B, C, D, and E are listed in Reference 24, but are not important in determining the general behavior of the temperature coefficients.

The temperature coefficient of the independent elastic constants has been shown to be approximately equal (Table 11). Thus, the derivatives of the elastic constants with respect to temperature are in approximately the same ratio as the elastic constants (Table 11). The numerators and denominators of Equations (25) and (26) must vary in about the same manner with orientation. It is known that s'_{11} and s'_{44} remain positive regardless of orientation, which strongly suggest that

$$\frac{ds'_{11}}{dT} \quad \text{and} \quad \frac{ds'_{44}}{dT}$$

will remain positive.

These facts lead to the conclusions that the temperature coefficient of the series resonant frequency of simple extensional or contour modes is negative and relatively insensitive to orientation.

A zero temperature coefficient cut of GaAs is not expected for any simple mode controlled by s_{11} or s_{44}. This includes length extensional, contour shear, contour extensional, and thickness shear modes.

Figures 96, 97, 98, 99, and 100 show that the series resonant frequency of GaAs changes linearly with temperature. A GaAs thermometer could be made by controlling the frequency of an oscillator with a GaAs crystal.

6.5 GaAs Resonators

High resistivity GaAs face shear (zx) and contour shear, (zxt) 45°, crystals were mounted in miniaturized holders with the ultimate aim of mounting a GaAs resonant crystal in a network package. GaAs crystals were initially mounted in a commercial holder for quartz crystals (Figure 101). Crystals mounted in this manner set a reference for comparing the mounting losses of miniaturized holders.

GaAs crystals mounted as shown in Figure 101 had the following typical parameters:

C_o = 10.3 pf

C_o/C_1 = 510

R_1 = 900 ohms

Q = 28,000

f_r = 322 kc.

The first approach to miniaturization was to shorten the mounting wires shown in Figure 101 and delete the shock mounting. This type of mounting is illustrated by Figure 102.

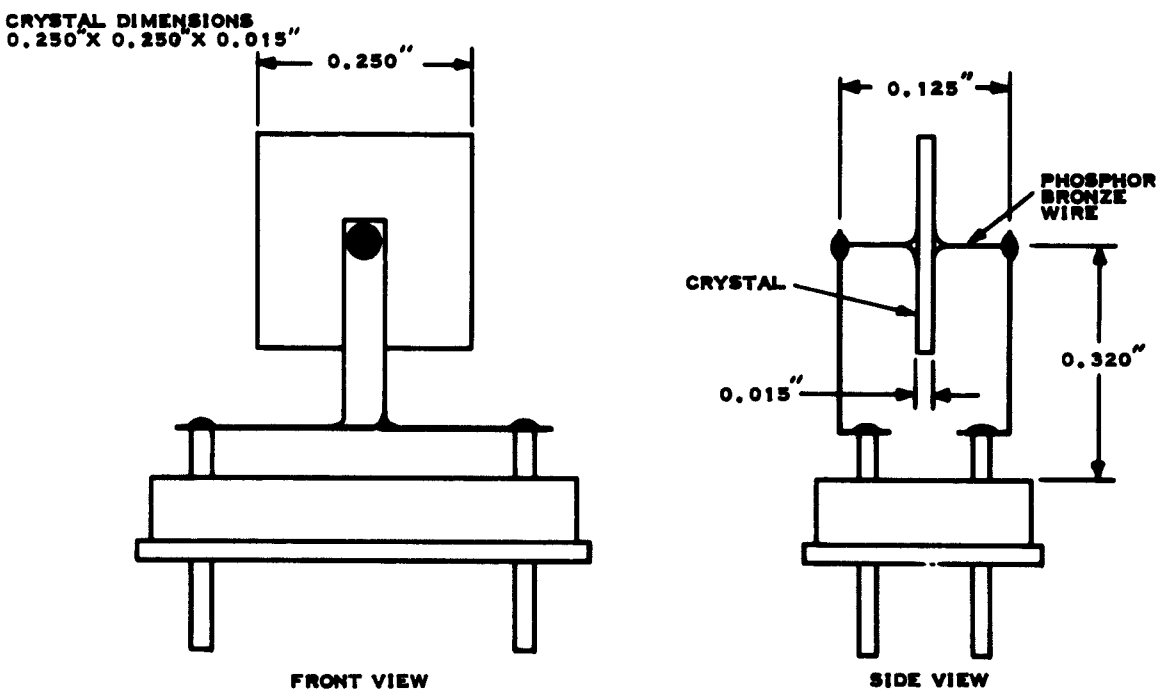


Figure 101. Bliley Type SR-10 Wire Mount

Another approach to miniaturization was to eliminate the mounting wires. Figure 103 shows the GaAs crystal pressure mounted between phosphor bronze springs bearing on the mechanical nodes of the crystal. This mounting was extremely shock sensitive.

The series resistance of crystals mounted as shown in Figures 102 and 103 was slightly higher (1.3 – 1.7K) than crystals mounted as shown in Figure 101. The major effect of the miniaturized mountings was to change the temperature coefficient of the resonant frequency of the crystal and change the series resistance of the crystal with temperature. A GaAs crystal mounted as shown in Figure 101 was used to control the semiconductor network oscillator shown in Figure 104.

GaAs face shear crystals were mounted by several techniques in network packages. Figures 105, 106, and 107 illustrate some of the mounting techniques tried. These crystals had the following typical parameters:

Dimensions: 75 x 175 x 15 mils

f_r = 973 kc

C_o = 2.2 pf

C_o/C_1 = 380

R_1 = 1 – 2 K

Q = 4 – 8000.

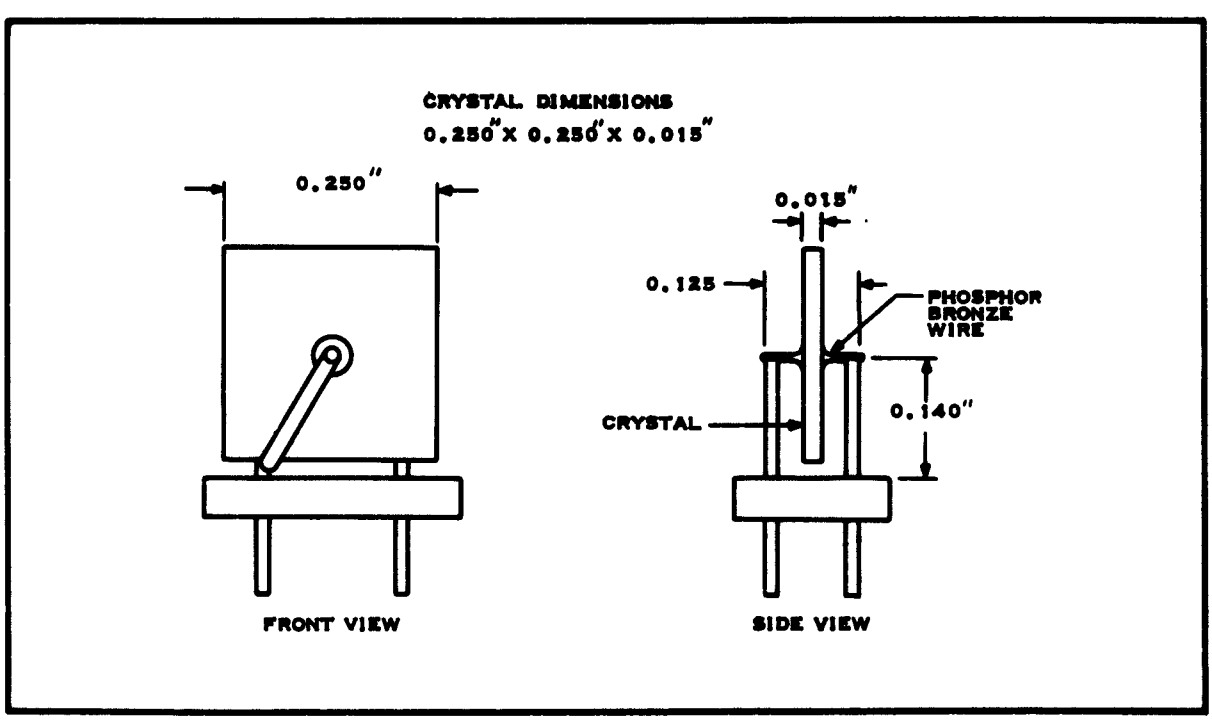


Figure 102. Transistor Header Mount

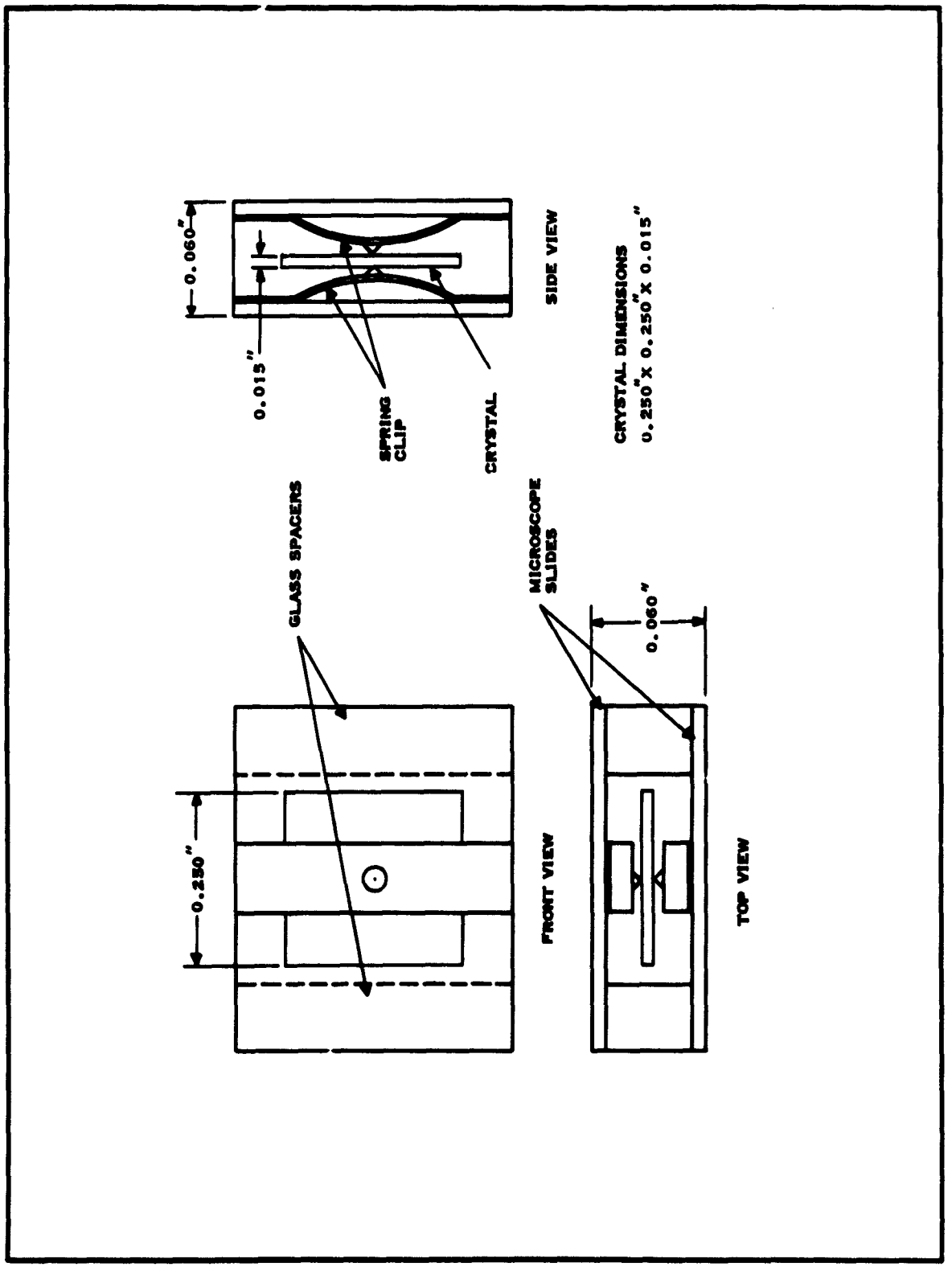


Figure 103. Crystal in Spring Strip Mount

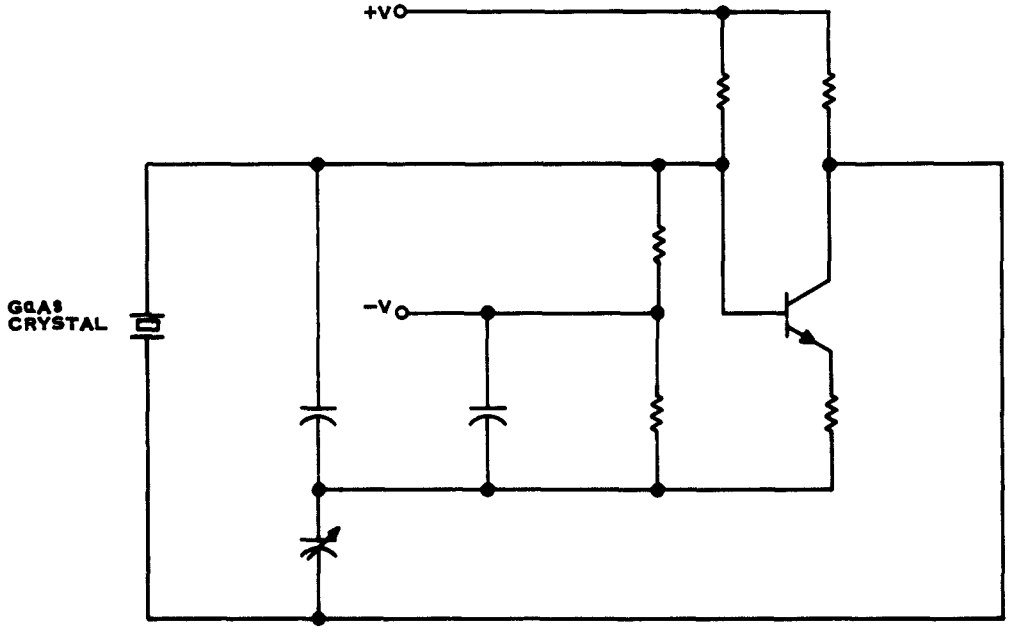


Figure 104. GaAs Crystal Oscillator and Schematic

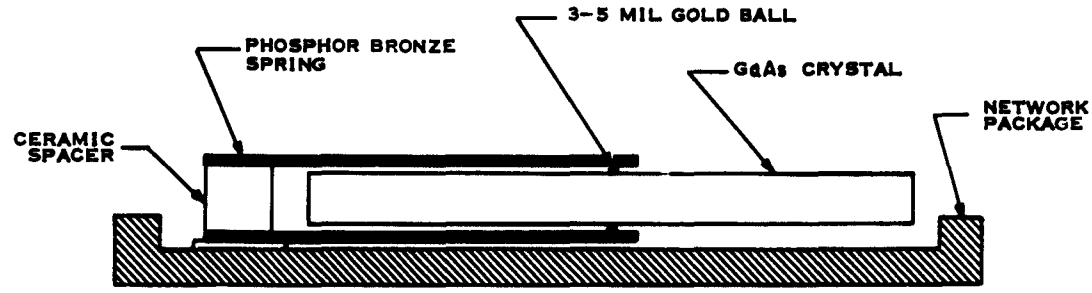


Figure 105. Network Package Mount With Subassembly

The mechanical Q of the crystals shown in Figures 105, 106, and 107 was extremely susceptible to mechanical shock. Some other mounting scheme would have to be developed before GaAs resonators in network packages would be of any practical value.

6.6 Equivalent Circuit of a Piezoelectric Resonator

Electrical performance of a piezoelectric crystal can be determined from the equivalent[24, 28, 29] circuit near resonance shown in Figure 95. The equivalent circuit represents the coupling of the mechanical resonance of the crystal (due to its dimensions, density, and controlling elastic constant) to its electrical terminals with the electro mechanical transformer ϕ. The expression given for ϕ in Figure 95 is for a long thin bar driven in a length extensional mode by a field applied to the face of the bar. The expression for ϕ under other resonant conditions can be found in the literature[29]. The mechanical resonance of the crystal is represented by the motional inductance L_m and the motional capacitance C_m. The effective mechanical Q_m of the crystal is defined in the normal way

$$Q_m = \frac{\omega_r L_m}{R_m} \quad . \tag{27}$$

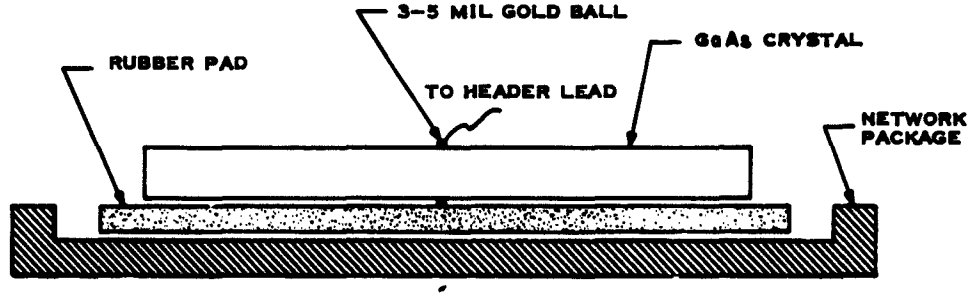
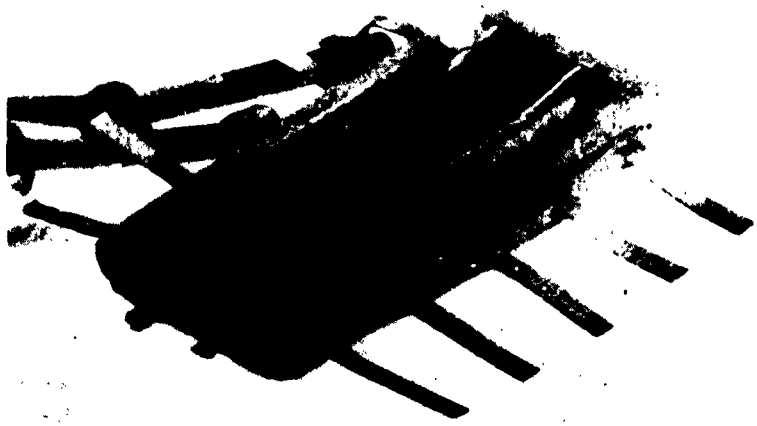


Figure 106. Network Package Mounting With Rubber Pad



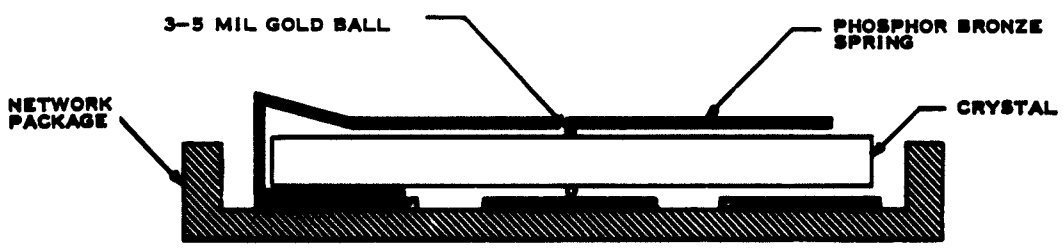


Figure 107. Crystal Mounted in Network Package and Cross Section of Network Mounting

The mechanical loss associated with the crystal is represented by R_m. This loss is generally due to several factors as indicated by Equation (28) below.

$$R_m = R_{air} + R_{material} + R_{mount} \tag{28}$$

where

R_{air} is the real part of the load due to air on the ends of the crystal. This mechanical resistance has a value of 430 Kg/(M^2 – Sec) for radiating areas with effective diameters greater than six-tenths of a wave length (λ). For the long thin bars compared in Table 12, the effective diameter of the radiating area is less than 0.04λ. R_{air} has an approximate value of 25 Kg/(M^2 – Sec) for this condition.

$R_{material}$ is the internal loss of the crystal expressed as a load on the ends of the crystal. This parameter depends on the material Q_{mat} of the crystal and is given by

$$R_m = \frac{\pi}{8} \frac{Z_o}{Q_{mat}} .$$

R_{mount} is the loss associated the mounting reflected to the ends of the crystal. This parameter is minimized by mounting the crystal at its mechanical nodes [30, 19] or by capacitive coupling [31] techniques.

TABLE 12

SERIES RESISTANCE OF LENGTH EXTENSIONAL BARS

$$\frac{t}{w} = 0.5 \qquad \ell = 10\ w$$

Material	Crystal Cut	k	R_1 in Ohms Due To R_m			Nominal Material Q	R_m (material) Nominal Q	$\left(\frac{d_{31}}{s_{11}}\right)^2 \left(\frac{Coul}{m^2}\right)^2$
			Air $R_m \cong 25$	Material R_m Nominal Q	Mounting R_m Assumed 100			
Quartz	X cut	0.095	250	88.8	1K	6×10^5	8.88	0.025
GaAs	zxt (45°)	0.037	328	—	1.53K	—	—	0.016
PZT-4	—	0.30	0.08	51.5	0.318	600	1.62×10^4	80.0
PZT-5	—	0.318	0.07	322.0	0.274	75	1.18×10^5	89.0
Ceramic B	—	0.185	0.21	169.0	0.85	500	1.99×10^4	45.3
Cd S	zxt (0°)	0.085	207	—	830	—	—	0.030

R_1 – Electrical Series Resistance In Ohms

R_m – Effective Mechanical Load in $\frac{Kg}{m^2\ Sec}$

The electrical resistance reflected from the mechanical circuit at resonance is a function of the turns ratio (ϕ) of the electro mechanical transformer. The ratio of electrical to mechanical resistance for several common piezoelectric materials driven in length extensional modes (t/w) = 0.5 is given below:

$R_1 = 10\ R_m$ X cut quartz

$R_1 = 15\ R_m$ zxt (45°) GaAs

$R_1 = 3.2 \times 10^{-3} R_m$ PZT-4

$R_1 = 8.5 \times 10^{-3} R_m$ Ceramic B.

These numbers reflect the high (d_{31}/s_{11}) ratio of PZT and Ceramic B. The effect of mounting losses, material losses, and air load on the series resistance of GaAs, Quartz, PZT-4, PZT-5, Ceramic B, and CdS extensional bars is compared in Table 12. For materials with relatively low mechanical Q (PZT, Ceramic B) the series resistance is dominated by material losses which are represented by an effective mechanical load of approximately

$$10^5 \ \frac{Kg}{m^2\ Sec}.$$

The series resistance of single crystal material such as quartz is dominated by losses due to air load and mounting. GaAs and CdS are single crystal materials and should have a relatively high material Q. Their series resistance should be dominated by air load and mounting losses.

Table 12 illustrates the electrical series resistance caused by an assumed mounting loss of 100 Kg/m^2 Sec. This value of mounting loss yields a computed series resistance comparable to that measured with GaAs resonators. Note that GaAs, Quartz, and CdS have similar series resistance due to mounting. The series resistance caused by this loss in PZT and Ceramic B is considerably less than that due to internal material losses.

The elements C_o and R_p represent the electrical capacitance and resistance of the crystal

$$C_o = \frac{A\epsilon^T}{t} \tag{29}$$

$$R_p = \frac{\rho t}{A} \tag{30}$$

where

ρ is the resistivity of the crystal

ϵ^T is the permeability at constant stress.

Piezoelectric materials such as quartz, PZT and Ceramic B are insulators with resistivities so high that R_p can be neglected. Piezoelectric semiconductors such as GaAs and CdS may or may not have a resistivity high

enough to allow R_p to be neglected. Also, since both GaAs and CdS are photo. conductive, R_p will be sensitive to light intensity and could shunt the effect of the mechanical resonance.

Table 12 illustrates the separation of the series and parallel resonant frequencies of the crystal. This separation is a function[22] of the electromechanical coupling coefficient as given in Equation (31) following.

$$\left[\frac{f_p - f_r}{f_r}\right] = \frac{4}{\pi^2} \left[\frac{k^2}{1 - k^2}\right]. \tag{31}$$

This separation of series and parallel resonant frequencies reflects a capacitance ratio C_1/C_o as given in Equation (32) below:

$$\frac{C_1}{C_o} = \frac{8}{\pi^2} \left[\frac{k^2}{1 - k^2}\right], \tag{32}$$

It has been shown that the maximum percent bandwidth which can be obtained from lattice filters using piezoelectric resonators as elements is:

$$\text{Percent BW} = 80 \left[\frac{k^2}{1 - k^2}\right]. \tag{33}$$

This excludes the use of external inductance.

Thus for filters with a wide passband a material with an electromechanical coupling factor approaching unity is required.

6.7 Application of Piezoelectric Materials to Integrated Networks

The possibility of using the piezoelectric properties of the materials listed in Table 12 to realize resonant elements for integrated networks can be evaluated from knowledge of the device technology available for the material, the mounting characteristic of the material, and the electromechanical coupling factor of the material.

The ceramic materials (PZT-4, PZT-5, and Ceramic B) have the high electromechanical coupling factor which is necessary for the realization of relatively wide bandpass filters. For example PZT-5 driven in a thickness extensional mode has an electromechanical coupling factor of 0.675, allowing a bandpass of about 50 percent to be realized. The high d_{31}/s_{11} ratio coupled with the low material "Q" should make the performance of these materials less sensitive to mounting than quartz. Active devices cannot be made in these materials and network applications would be on a separate package basis. The dielectric constant of these materials is high (12-1300) and therefore restricts the maximum frequency of operation.

Resonant quartz crystals have been widely used to control oscillators because of the physical stability and the zero temperature

coefficient of the resonant frequency. The use of quartz crystals in networks would be restricted to a nonintegrated basis since active devices in quartz are not possible. Bandpass filters with a 1.6 percent passband can be realized with quartz resonators. This is not wide enough to make quartz crystals attractive for most bandpass filter applications. The mounting loss associated with quartz crystals would need to be minimized to obtain maximum performance.

The electromechanical coupling factor of CdS is roughly twice that of quartz. The thickness extensional mode of CdS has an electromechanical coupling factor of about k = 0.2, allowing a filter with a bandpass of about 3.5 percent to be realized. Some active devices (field effect) can be realized in CdS making it possible to realize an active device with about a 3 percent bandwidth. In order to achieve this maximum performance the mounting losses associated with the CdS crystal would have to be minimized. CdS resonators could be used for realizing crystal controlled oscillators. The temperature characteristics of a CdS controlled oscillator would depend on the unknown temperature coefficients of CdS. CdS has a relatively high electromechanical coupling coefficient and would make efficient transducers for driving acoustic delay lines. The insertion loss on an acoustic delay line driven with CdS transducers would be less than that of a line driven with similar quartz transducers.

The electromechanical coupling factor of GaAs is less than 0.05 for all modes. The maximum bandpass which could be realized with a GaAs filter would be approximately 0.2 percent. This is too narrow to be useful for most applications. GaAs resonators could be used to control the frequency of an oscillator. However, the lack of a zero temperature coefficient mode would be a serious disadvantage. The properties of GaAs as a delay medium for acoustic delay lines are listed in Table 13. GaAs would not be an attractive delay medium because the delay time does not have a zero temperature coefficient.

TABLE 13

UNTRASONIC DELAY LINE CHARACTERISTICS OF GaAs

Parameter	Value	Remarks
Acoustic Velocity	0.41 to 0.53 cm/μsec 0.27 to 0.34 cm/μsec	Longitudinal waves (orientation dependent)
Temperature Coefficient	+58 to +60 ppm/°C	Longitudinal and Shear Waves (slightly orientation dependent)
Rate of Change of Temperature Coefficient	±1.6 ppm/°C^2	Scatter in present data does not permit a more accurate determination

6.8 Conclusions and Recommendations

The piezoelectric materials considered which have the best capability for controlling oscillators (quartz) and realizing bandpass filters (the ceramics) cannot be made into active devices. There is some possibility that an integrated CdS active field effect resonant device could be realized at frequencies near 1 megacycle. However, it would have to be shown that this device would out perform a silicon active device and an externally packaged resonator or filter fabricated of a more optimum material.

The piezoelectric properties of GaAs do not indicate that an integrated GaAs resonant structure would be desirable at the present time.

With the present state of the art best performance could probably be realized with a silicon active device and a separably packaged resonator or filter. If the piezoelectric properties of the semiconductor materials are to be useful in networks they must be exploited in a manner which makes fuller use of their piezoelectric, photo conductive and semiconducting properties to perform a function which cannot be done with material having only piezoelectric or semiconducting properties.

One such function is the recently reported ultrasonic amplification phenomena in II-VI and III-V piezoelectric semiconductors[32]. It is recommended that a study into the ultrasonic amplification phenomena be initiated. The first material to be studied should be CdS because it is available in high resistivity single crystal form and has a relatively high electromechanical coupling coefficient.

SECTION VII

GENERAL CONCLUSION

Investigations and experimental fabrication conducted under AF33(616)-6600 from June 1959 through January 1962, defined and established the possible application of silicon Functional Electronic Blocks (FEB's) to linear functions and suggested potential design techniques requiring the use of other semiconductor phenomena.

The initial experimental work formed the basis for subsequent programs, allowing specific development and application of linear FEB's. Linear functions, generally, place greater stress on the designer for ingenuity and upon fabrication controls used in forming silicon blocks. It is principally through the availability of linear FEB's that the major impact will be made on Air Force equipments, because the linear function has been the most abundant of circuit functions and the most widely understood by equipment designers. As linear blocks are made available, there is an acceptance of silicon FEB's by equipment designers that could not be accomplished by the availability of only digital FEB's. As a result of this contract and other similar programs, linear FEB's are available today, proving the utility of silicon FEB's.

In order to expand the application of Functional Electronic Blocks, phenomena, other than charge transport, was investigated in semiconductor materials. The principal materials possessing a wide range of phenomena are the III-V semiconductor compounds. While these investigations suggest many areas of promise, they must be balanced with the limited material and fabrication knowledge of the compound semiconductors as compared to the highly developed state of the art for silicon. This suggests that these newer techniques, will principally find application as supplements to silicon FEB technology, which will be the principal technology of molecular electronics for many years.

SECTION VIII

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WRIGHT-PATTERSON AIR FORCE BASE OHIO

November 25, 2015

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Attn: Michael Hamilton
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On 30 September 2015 our organization received a Freedom of Information Act (FOIA) request from [redacted], our number 2016-00248-F-ST1, dated 20 October 2015, for Technical Documentary Report ASD-TDR-63-281, entitled "Semiconductor Single-Crystal Circuit Development," dated March 1963. The report is listed in DTIC as report AD0411614. The FOIA requires federal agencies to review records responsive to the FOIA request and release to the FOIA requester and to the public all information not protected from release by a FOIA exemption.

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