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PRINCIPLES OF ACCOMPLISHING LEARNING AND LOGICAL PROCESSES IN AUTOMATIC EQUIPMENT

-East Germany-

/Following is a translation of an article by Dr. Eng. P. Neidhardt, Chamber of Technology, Berlin, in the German-language periodical Die Technik (Technology), Vol 18, No 4, Berlin, April, 1963, pages 277-281./

The following article is concerned with an especially important field of modern cybernetics, namely with the principles of adaptive automated technical systems. These are self-organizing, dynamic systems, capable of learning, which represent the last, still inadequately studied group of cybernetics, which up to now has dealt chiefly with self-regulating and self-stabilizing systems. We present here the ideas of a specialist in the field of information processing, discussing the working principles of the electronic realization of the principle of logical combinations and of the learning process by means of binary and non-digital learning matrices.

1. Introduction to the Problem

The subject to be dealt with here is an important branch of modern cybernetics. The definition of cybernetics designates it as the theory of self-regulating and self-organizing dynamic systems. The most highly developed group of such systems are the organisms, and among them, in turn, man. To cybernetics belong most especially all automated technical systems, of which there are programmatically controlled and adaptive types; by the latter is meant such as are capable of learning.

Two questions arise in this connection: What is a logical combination, and what does a learning process consist of in general? Learning, first of all, includes perception. Coupled with perception is the classification of the information received within a system which may be called a "logical framework." Information theory concerns itself with this logical framework and its structure. Every statistical observation requires a logical framework. Since the informational content of a message is statistically defined, a logical framework is prerequisite to the evaluation of a series of symbols. The classification process is thus a step in the learning process.

A further step is storing the information in accordance with prior classification within the logical framework. This performs the function of a memory. A conditional connection is thus set up. This is followed by determination of extreme values, which leads to control of what has been learned. This will be gone into in more detail in later sections. Independent of these basic formulations there are a number of additional specialized processes which lead to various types of learning. There are important relationships here with the precepts of information theory, which characterizes the learning process as redundancy-generating. The redundancy of a message is defined as the number or the percentage figure that indicates by how much the quotient of the information entropy of the message by the maximum information entropy possible with the number of message characters used differs from the value 1 (or 100%). The information entropy, as the logarithmically measured mean of probability of the occurrence of the individual symbols (e.g. letters), serves to characterize an information source. Thus for

example the partial or complete repetition of the particulars of a message in oral or written communication is counted as redundancy. It may be said that that is redundant which is already known.

Two important concepts in information theory are redundancy and relevancy. That part of a signal is relevant which refers to the subject; that is irrelevant, by contrast, which does not refer to the subject. Only what is relevant is interesting. From the point of view of information theory parts of a message or the message itself may have four characteristics. They may be

1.1 not redundant, but relevant,

1.2 redundant and relevant,

1.3 not redundant and not relevant.

1.4 redundant and not relevant.

The process of learning undoubtedly has 1.2 as its goal; the information learned, according to the learning process, or in the can phase, is to be both redundant (i.e. adequately known) and also relevant (bearing on the subject). The learning process is of extraordinary interest to technology, because on its proper technological realization depends in a large measure what the life of mankind will be like in the foreseeable future. The accomplishment of learning and logical processes in machines leads to instruments and installations which themselves optimize their manner of reacting to external influences. The learning process improves the course of the reaction.

It is hardly necessary to point out that this takes us to the most important chapter in cybernetic research and development, namely the building not only of self-regulating and also self-stabilizing dynamic systems, but most especial-

ly of self-organizing systems.

2. Fundamentals of the Algebra of Logic and of the Principle of Logical Combination

The development of an algebra of logic stems from the mathematics professor Boole (1815-1864). Mathematical logic has in the course of time developed into an independent mathematical discipline, making use of so-called bivalent "truth functions," which reflect specific conditions of objective reality as statements. The algebra involved is also known as "Boolean algebra." It is important in this connection that between electrical circuits and the propositions of Boolean algebra there exists a fundamental analogy, on the basis of which the best known exponent of information theory, C. E. Shannon, in 1938 developed an algebraic method of designing circuits which made it possible to set aside the previous empirical method. Moreover this new method is just as valid for circuits which use not mechanical switches but tubes and semiconductor components.

If we are to discuss here the principles of accomplishing logical processes in machines by electronic means, we must begin with the bivalent truth functions and their rules of operation.

2.1 Negation or Inversion

The logistic negation of a proposition "T" (or, say, "not T," Latin "non") is represented by

$$\text{not } T = \overline{T} = F ,$$

where T means true and F false.

The output value in the corresponding logistic electronic circuit occurs only when the input value is not present.

2.2 Conjunction

The logistic product of two propositions X and Y is

the proposition for the truth of which it is required that X and Y be true. It is called "conjunction," and is represented by:

X = T; Y = T; X&Y = truth T (2)
X = T; Y = F; X&Y = fallacy F (3)
X = F; Y = T; X&Y = fallacy F (4)
X = F; Y = F; X&Y = fallacy F (5)

The ampersand (&) in logistic algebra is pronounced "et" (Latin "and"). Conjunction corresponds to a logistic multiplication of two propositions, and is therefore true only when both propositions (logistic variables) are true. The output quantity in the corresponding logistic electronic circuit occurs only in the case where all input quantities are present.

2.3 Alternative or Disjunction

The logistic sum of two propositions X and Y is the proposition for the truth of which it is sufficient for one of the propositions to be true. It is called disjunction and is represented by:

X = T; Y = T; XVY = T (6)
X = T; Y = F; XVY = T (7)
X = F; Y = T; XVY = T (8)
X = F; Y = F; XVY = F (9)

The sign V is pronounced as "vel" (Latin "or") in logistic algebra. Disjunction corresponds to a logistic addition of two propositions, and is consequently true only if at least one proposition (logistic variable) is true. The output quantity in the corresponding logistic electronic circuit occurs whenever at least one input quantity is present.

2.4 Implication

All logical relationships may be reduced basically to conjunctions, disjunctions, and negations. Nevertheless, as one of three additional logistic operations "implication" has been introduced. Implication, with the sign $\rightarrow$, is false only when the first logistic variable, X, is true and the second, Y, false. In all other cases it is true. The sign $\rightarrow$ in logistic algebra is pronounced "seq" (Latin abbreviation of sequentia = the consequence), i.e. "conditioned." Implication is represented by:

$$X = T;\ Y = T;\ X \rightarrow Y = T \qquad (10)$$
$$X = T;\ Y = F;\ X \rightarrow Y = F \qquad (11)$$
$$X = F;\ Y = T;\ X \rightarrow Y = T \qquad (12)$$
$$X = F;\ Y = F;\ X \rightarrow Y = T \qquad (13)$$

Implication is used for describing the relationships between complicated functions.

2.5 Equivalence

Equivalence is used in order to shorten the written form of logistic equations. It is represented by:

$$X = T;\ Y = T;\ X \sim Y = T \qquad (14)$$
$$X = T;\ Y = F;\ X \sim Y = F \qquad (15)$$
$$X = F;\ Y = T;\ X \sim Y = F \qquad (16)$$
$$X = F;\ Y = F;\ X \sim Y = T \qquad (17)$$

The sign $\sim$ in logistic algebra is pronounced "eq" (abbreviation of equivalent). Equivalence is true only when both variables are of the same value. It corresponds to the opposite of logical negation.

2.6 Antivalence

Antivalence, too, is used to shorten the written form of logistic equations. It is represented by:

$X = T;\ Y = T;\ X \neq Y = F$ (18)

$X = T;\ Y = F;\ X \neq Y = T$ (19)

$X = F;\ Y = T;\ X \neq Y = T$ (20)

$X = F;\ Y = F;\ X \neq Y = F$ (21)

The sign $\neq$ in logistic algebra is pronounced "ant" (abbreviation of antivalent, i.e. not equivalent). Antivalence is true only when the two variables possess opposite values. It corresponds to logistic negation.

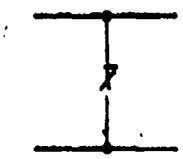
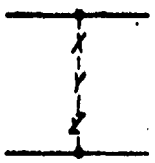
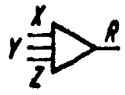
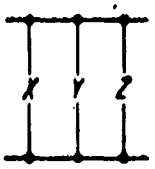
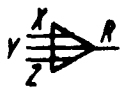
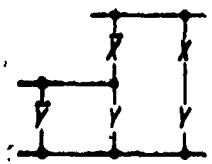
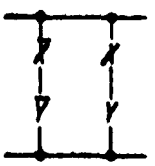
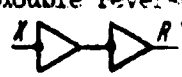
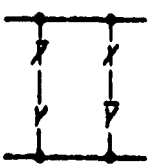
The logical relationships mentioned here may be represented electronically or merely electrically by means of switches. For automation the corresponding basic circuits, of which there are numerous variations, are of the greatest importance. In Table 1 the six different logistic truth functions and their electrical representation are diagrammed.

A certain duality exists between conjunction and disjunction, which may be expressed as follows: Conjunction with reference to positive logistic variables represents disjunction with reference to zero of all logistic variables. In the same way a disjunction with reference to positive logistic variables represents a conjunction with reference to zero of all logistic variables. Disjunction and conjunction may be basic functions of any degree, i.e. may be related to any number of variables.

These remarks are of course intended only to report on the bases of accomplishing logical relationships in automatic machines, but it may be useful to introduce a facetious toy problem and indicate its solution by means of logistic algebra before going on into the electronic components which serve for the automatic solution of such problems of automation.

Let us assume that children regularly tell the truth,

Table 1

Truth function	Substitute circuit	Wiring symbol
1. Negation		 Reverse switch $R = \overline{X}$
2. Conjunction		 And-gate $R = X \cdot Y \cdot Z$
3. Disjunction		 Either-or-gate $R = X \vee Y \vee Z$
4. Implication		No wiring symbol $R \longrightarrow X$
5. Equivalence		Corresponds to double reverse  $R = X$
6. Antivalence		 Reverse switch $R = \overline{X}$, $R \neq X$

since life has not had sufficient opportunity to get them away from this attitude inculcated in their parents' home. On the other hand let it be assumed that adults lie. The problem is this: Seven persons, A to G, are involved. It is known that A and B are children. The problem states that a person C who describes someone called D as already grown. /Translator's note: the sentence in the source seems to be incomplete./ It is further known that a person E states that it is affirmed by A that C asserts that D claims that B can not be dissuaded from the notion that F is unwilling to believe that G is still a child. It now suddenly becomes known that E is 25 years old, and the question arises of how many adults there are in this problem.

One would certainly have some difficulty in finding the correct answer without making use of the formulae of logistic algebra. In the toy problem the adults are to be indicated by letters without a horizontal stroke and children by letters with a horizontal stroke. The first statement made in the problem runs:

$$\bar{A} \,\&\, \bar{B} \tag{22}$$

It is further known that

$$C \bullet D \tag{23}$$

This is based on the fact that either C is still a child and does not lie and consequently his statement that D is already grown is true, or C is an adult and lies, in which case D is still a child. In either case there is antivalence between C and D.

The remaining statements are also antivalent, giving

$$E \bullet (A \bullet \{C \bullet [D \bullet (\bar{B} \bullet (F \bullet G))]\}) \tag{24}$$

The fourth condition given in the problem is simply E, i.e. E is adult. (25)

These four conditions can be related to each other by conjunction. There is consequently a logistic function

$$y\ (A,B,C,D,E,F,G)$$

of the logistic variables A to G. The solution runs:

$$\begin{aligned} y = {} & (\bar{A} \,\&\, \bar{B} \,\&\, C \,\&\, \bar{D} \,\&\, E \,\&\, F \,\&\, \bar{G}) \vee \\ & (\bar{A} \,\&\, \bar{B} \,\&\, C \,\&\, \bar{D} \,\&\, E \,\&\, \bar{F} \,\&\, G) \vee \\ & \vee(\bar{A} \,\&\, \bar{B} \,\&\, \bar{C} \,\&\, D \,\&\, E \,\&\, F \,\&\, \bar{G}) \\ & \vee(\bar{A} \,\&\, \bar{B} \,\&\, \bar{C} \,\&\, D \,\&\, E \,\&\, \bar{F} \,\&\, G) \end{aligned} \qquad (26)$$

It will be seen that in every part of the disjunction there are four children and three adults. For lack of space it is impossible here to present the entire computation, not to mention all the rules of operation of the algebra of logic; for this we must refer to the relevant literature (1,2,3,4,5). /Translator's note: This article is not accompanied by a bibliography. The references are presumably to a bibliography to be published with the sequel./

The electronic means by which these logical relationships can be controlled is discussed below.

2.7 Reverse Switches with Triodes, Transistors, and Ferrite Cores (Negators)

Reverse switches embody equation (1) and serve in electronic implementation for polarity reversal of impulses, with which logistic circuits normally work for reasons of operational speed. The triode negator shown in Figure 1 is blocked by the negative initial grid voltage $-U_g$ across R_1. Then the output potential is $U_a/2$, because the resistances are purposely so dimensioned that

$$R_4 = R_2 + R_3 \,. \qquad (27)$$

The triode is opened by a positive impulse at the

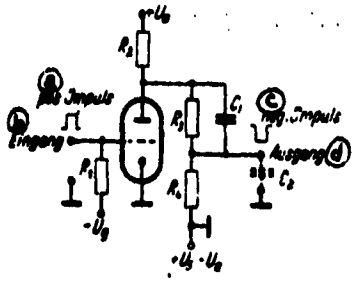


Figure 1. Triode negator.

Legend:

a. positive impulse; b. input; c. negative impulse; d. output.

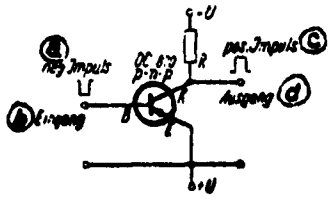


Figure 2. Transistor negator.

Legend:

a. negative impulse; b. input; c. positive impulse; d. output.

input, the potential at the connecting point of R_2 with R_3, or in other words the anode, drops, and consequently the potential at the connecting point between R_3 and R_4, i.e. the output, also drops, and the desired negative impulse occurs. C_1 is a compensating capacity and is intended to compensate the output capacity. The time constants are also set equal:

$$R_3C_1 = R_4 \cdot C_2 \qquad (28)$$

Generally cathode followers are used in connection with such triode negators, so that the high-resistance voltage divider $R_2 - R_3 - R_4$ is not one-sidedly loaded through the

input resistance of the following stage at R_4.

Figure 2 shows a transistor negator with a p-n-p transistor. The letters p and n, of course, indicate the conductive properties of the zones of which the junction transistor is composed, n referring to the negative charge of the electrons which condition the electrical conductivity in the zone in question and p to the positive hole conduction, since the holes from which freed electrons in the lattice have broken away carry a positive charge. The holes are also movable and represent a second mode of conduction of the charge in the semiconductor. A transistor can be built either as a p-n-p semiconductor triode or as an n-p-n semiconductor triode. Lastly, p-n-p-n semiconductor tetrodes are known, consisting of four alternately p and n conductive zones. Thus for example the junction transistors OC-810, OC-830, OC-870, and almost all other GDR transistors are of the p-n-p type, while junction transistors of the n-p-n type (Sylvania types 2 N 35 and 2 N 94) are rarer and serve special purposes. With n-p-n transistors all voltages and currents must be reversed in polarity as compared to p-n-p transistors.

The circuit in Figure 2 works in much the same way as the tube circuit of Figure 1. The negative input impulse reverses the basis from an inverse voltage to a forward voltage, and the collector voltage, or output, rises almost to zero. In the circuit diagram B indicates the base, K the collector, and E the emitter of the transistor.

Another possibility of constructing negators consists in the use of ferrite cores, which are of great importance in the technology of information processing. By ferrites are meant magnetizable materials of very low electrical conductivity, so that magnet cores made of ferrites usually

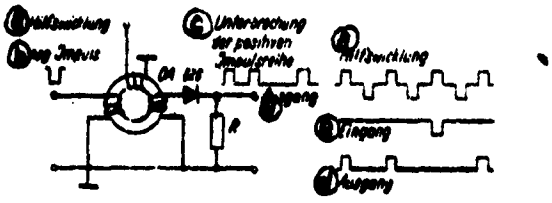


Figure 3. Ferrite core negator.

Legend:

a,a auxiliary winding
b negative impulse
c interruption of the series of positive impulses
d,d output
e input

do not need to be laminated and still show very slight eddy-current losses. Ferrites are produced ceramically, and consist of crystals of spinel structure of iron oxide (Fe_2O_3) with one or more oxides of bivalent metals, chiefly manganese, nickel, zinc, copper, cobalt, or magnesium. Ferrimagnetism differs from ferromagnetism in the type of orientation of the atomic magnetic forces and in the composition of the material. Ferromagnetism occurs in iron (not iron oxide, as in the case of ferrimagnetism), and also in nickel, cobalt, and the corresponding alloys. Hard magnetic ferrites generally deviate approximately by a parallelogram curve from the field intensity; we speak of a "rectangular" hysteresis loop.

A ferrite-core negator as in Figure 3 works as follows:

In contrast to Figures 1 and 2, the object is not to reverse the polarity of impulses, but to generate two conditions at the output of the negator, namely that in the one condition impulses occur and in the other they do not. This

can of course be accomplished with tubes, too (most conveniently with pentodes). Into an auxiliary winding is fed a series of positive and negative impulses, to bring the core back each time to its initial state of magnetization, and into the input is fed the individual impulse that is to blank (cancel) one impulse out of the series. The diode serves only to block voltage impulses of opposite polarity. Whenever the input impulse occurs it and the opposite impulse cancel each other out and the impulse is lacking at the output. This corresponds to a negation of the input information.

2.8 And-Gates as the Electronic Realization of Conjunction in Logistic Algebra

AND-gates realize equations (2) to (5), and they, too, can be constructed with tubes, semiconductor components, and ferrite cores. Four different basic possibilities are briefly described here; there are also numerous variations.

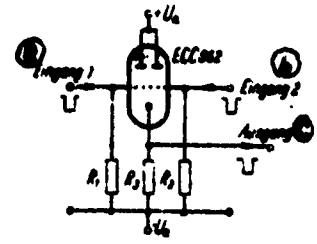


Figure 4. AND-gate with double triode.
Legend:
a input 1; b input 2; c output.

Figure 4 shows a double triode with two inputs and one output. Both triodes are open in a state of rest, so that at the common cathode-resistance R_3 ($R_3 \gg 1/S$, where S is the mutual conductance of the system) the voltage is high. Nor does this condition change when a negative impulse occurs

at one input, because in spite of the blocking of one system which then occurs, the load current at the output is hardly changed. Only when both inputs are supplied with sufficiently high impulse amplitudes does the load current at the output drop practically to zero, i.e. a negative output impulse occurs according to (2).

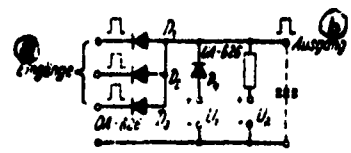


Figure 5. AND-gate with semiconductor diodes.
Legend: a inputs; b output.

The corresponding circuit variation with semiconductor diodes is shown as an AND-gate in Figure 5. Gates are electronic switches which at a specific signal permit the passage of impulse series or block it. They possess an analog in biophysics and neurology in the synapses, which are situated between two neurons and have the function of sending on the electrical action potentials of the nerves, when a certain magnitude is reached, from one neuron to the next by electrolytic conduction. In the circuit of Figure 5 will be seen three inputs, in the lines of which are three diodes D_1, D_2, and D_3. U_2 is a grid voltage working positively across the resistance R, so that the diodes conduct and the output is kept approximately at voltage zero provided

$$R \gg R_i + R_D \,. \qquad (29)$$

In this expression R_i is the internal resistance of an impulse generator at input 1 or 2 or 3 and R_D the resistance of a diode in the forward direction. As soon as all the

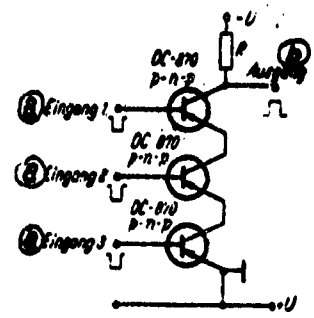


Figure 6. AND-gate with transistors.
Legend: a,a,a input; b output.

diodes are blocked by the occurrence of positive impulses at the three inputs, a positive impulse occurs at the output, but this does not occur if even one diode remains active because it has not received an input impulse. The additional diode D_4 serves to suppress interference impulses at the output when the input pulses do not coincide; its grid voltage U_1 must be so regulated that in case of imperfect coincidence the output voltage stays at U_1 independent of the number of input impulses.

A variant of the AND-gate with transistors is shown in Figure 6. The base voltage is adjusted in such a way that in a state of rest all the transistors are open. An output impulse occurs only when all inputs are simultaneously blanked out, or blocked, by the input impulses. The output impulse is positive, giving a reversal of polarity.

A last variant of the AND-gate with a ferrite core is shown in Figure 7. An impulse occurs at the output only in the case when two positive impulses occur simultaneously, which change the magnetization of the ferrite core via the semiconductor diodes (to avoid retroactive effects on the

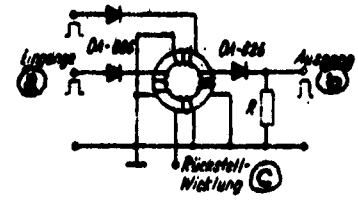


Figure 7. AND-gate with ferrite core.
Legend: a inputs; b output; c reset winding.

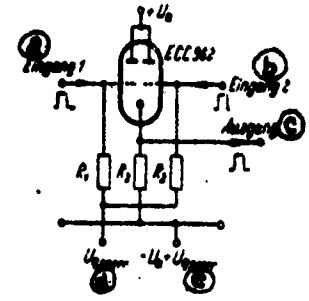


Figure 8. OR-gate with double triode.
Legend: a input 1; b input 2; c output; d U_g (block); e $-U_a+U_g$ (block).

inputs). The reset winding always returns the core to its initial state of magnetization.

2.9 OR-gates as the Electronic Realization of the Disjunction of Logistic Algebra

OR-gates implement equations (6) to (9), and like AND-gates they can be constructed with tubes, semiconductor components, or ferrite cores. As has already been pointed out, a certain duality exists between AND-gates and OR-gates. Both functions, conjunction as well as disjunction, sometimes combine several conditions into one statement (and can therefore be of the nth degree). Figure 8 shows the basic circuitry of an OR-gate with a double triode. Both systems of the double triode are blocked by the voltage

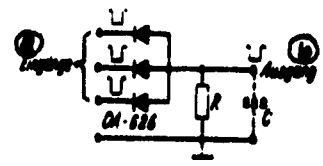


Figure 9. OR-gate with semiconductor diodes.
Legend: a inputs; b output.

U_g, so that the output has the voltage zero. As soon as a positive voltage occurs at input 1 or 2 or at both inputs, the output also becomes positive. Although admitting impulses at both inputs does increase the cathode current, the effective outer resistance drops to about half, so that the output impulse is almost exactly as great as if only one input had carried an impulse. Again we must have $R \gg I/S$.

With semiconductor diodes as in Figure 9 the OR-gate works as follows: For every input one diode is used; the circuit design is quite simple. A negative impulse on one of the diodes makes the latter effective, and provided its forward resistance is small as compared to the working resistance R, the input resistance appears full strength at the output. This provides a negative initial voltage for the other diodes, thus practically switching off their inputs, so that no reaction between the inputs can occur. If the input impulses are of different strength, the one that is strongest takes effect.

Figure 10 shows an OR-gate with p-n-p type transistors. In a state of rest the blocking voltages are effective at the inputs and the output is at the potential of the feeding current U. The transistor on whose base an impulse of negative polarity occurs becomes effective and the output

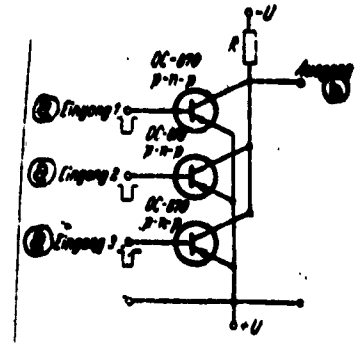


Figure 10. OR-gate with transistors.
Legend: a,a,a inputs; b output.

voltage rises from the negative feeder voltage to zero. The emitter circuit effects a reversal of the impulse. The load resistance must be large compared to the quotient of voltage between emitter and collector by the collector current, so that when several impulses occur at the same moment the output impulse will not be materially changed.

The circuitry of an OR-gate with a ferrite core does not differ from that of the AND-gate. Only its operation is somewhat different. The circuit shown in Figure 7 is used. The more or less parallellogram-shaped curve of the well-known ferrite hysteresis loop requires the generation of a minimum field strength by a minimum current strength in the winding, so as to get from the negative remanence to a positive value. In the AND-gate the process is accomplished by both windings carrying the input current and thus tipping the balance toward a positive remanence value. In the OR-gate the circuit is so dimensioned that one impulse is strong enough by itself that the change-over occurs. Thus in the OR-gate there is no output impulse only in the case

where both inputs are at rest. Here, too, the reset winding serves to bring the core back each time to its normal negative state with a sufficiently strong impulse.

(To be continued.)

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