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RADC-TDR-63-207

April 15, 1963

FINAL TECHNICAL REPORT
FOR
HIGH POWER SOLID-STATE SWITCH STUDY

Westinghouse Electric Corporation
Electronics Division
P. O. Box 1897 Baltimore 3, Maryland

Contract No. AF 30(602)-2602

Prepared
for

Rome Air Development Center
Research and Technology Division
Air Force Systems Command
United States Air Force

Griffis Air Force Base
New York

Copy ___ of ___

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ABSTRACT

This report describes the study, the design, and the development of a high power solid-state radar modulator operating into a resistive (dummy) load. All of the work described was performed on RADC contract AF30(602)2602. Specifically, the report describes the study and experimentation performed on the individual inductive and solid-state components. The seriesing of Trinistors, as well as Trinistor characteristics are described in considerable detail. Finally, the modulator breadboard is described and evaluated. The breadboard develops 5 Mega-watts of peak power and operates at 300 pps. The pulse width is approximately 5 micro-seconds.

Title of Report RADC-TDR-63-207

PUBLICATION REVIEW

This report has been reviewed and is approved.

Approved: Paul H. Babbum for L+Col USAF
ARTHUR O. FROHLICH
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Directorate of Aerospace Surveillance & Control

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Director of Aerospace
Surveillance & Control

FOR THE COMMANDER: Irving J. Gabelman
IRVING J. GABELMAN
Director of Advanced Studies

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I. INTRODUCTION

This report describes, in detail, a solid-state radar modulator breadboard and the components used in the breadboard. This modulator generates 5 Mw peak power and operates at 300 pps. The pulse width is approximately 5 microseconds. The use of Trinistors in a modulator with this capability is unique. Every effort has therefore been made to evaluate Trinistor performance in this high power application. The Trinistor®, however, is inherently a high efficiency device so that the power dissipated in the Trinistor switch is far below the device dissipation capability. Hence, the major modulator design considerations are not Trinistor power capability but Trinistor current and voltage capability. For example, the Trinistor has a voltage rating of 700 volts, average current rating of 70 amperes, and peak current capability of well over 1000 amperes. The peak output voltage and current of the modulator, however, are 50 KV and 100 amperes respectively. A 1:10 output pulse transformer was used, therefore, to utilize the high current capability of the Trinistor and allow it to switch 1000 amperes. Twenty Trinistors were connected in series to achieve the voltage rating required for the primary circuit of the transformer. The Trinistors are used in a manner which fully utilizes both their voltage and their current capabilities.

The adaptation of the Trinistor to the present application constitutes the major design achievement of the program, namely, the capability to reliably series a number of Trinistors and to reliably switch peak currents far in excess of the average current rating of the device.

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II. FINAL BREADBOARD

The prime objective of this contract was to design and construct a breadboard model of a five-megawatt solid-state modulator. This has been successfully done and the details of this modulator follow:

A. SYSTEM DESCRIPTION

Figure 1 shows the block diagram of the 5-megawatt solid-state modulator. The modulator is a line type modulator using resonant charging. Twenty series-connected Trinistors are used to discharge the PFN to generate the 5.0 microsecond pulse. These Trinistors are rated at 700 volts and 70 amperes. To insure that the Trinistor junctions are completely "on" during the peak pulse of current, a saturable reactor delays the output pulse 20 microseconds. A ten-to-one step-up output transformer produces a 50-KV pulse across the 500-ohm dummy load resistor.

The Trinistor switch is driven by a transistor trigger amplifier. The trigger pulse driving the trigger amplifier is obtained from an external pulse generator operating at 300 pps.

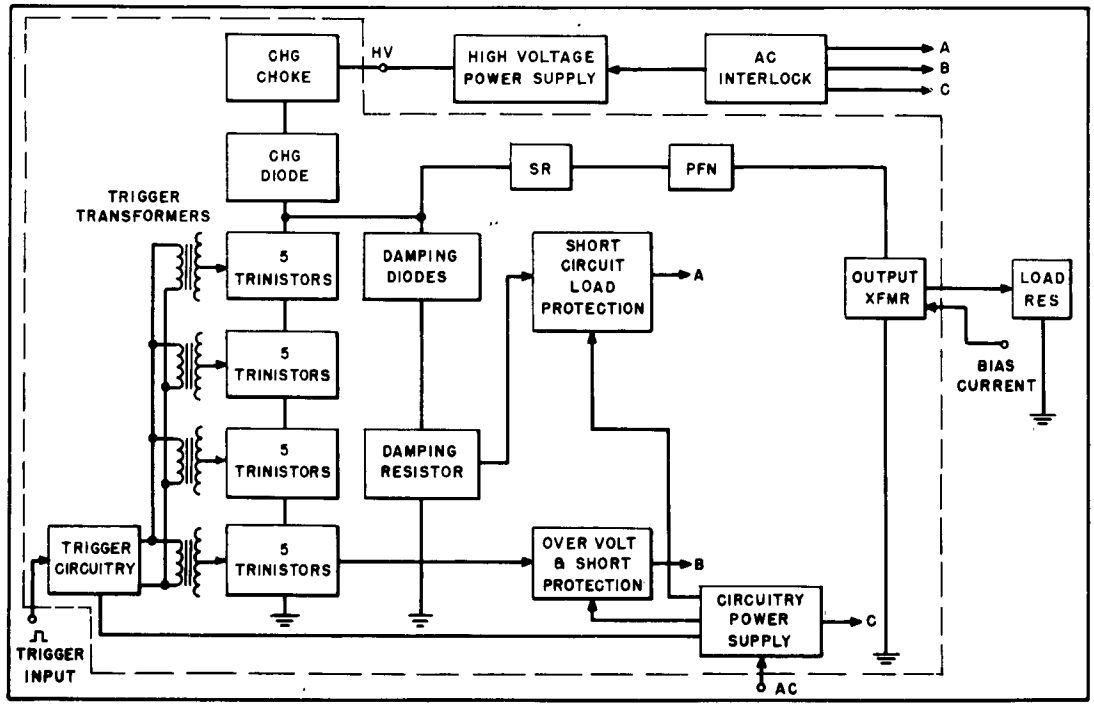


Figure 1. Block Diagram of Modulator

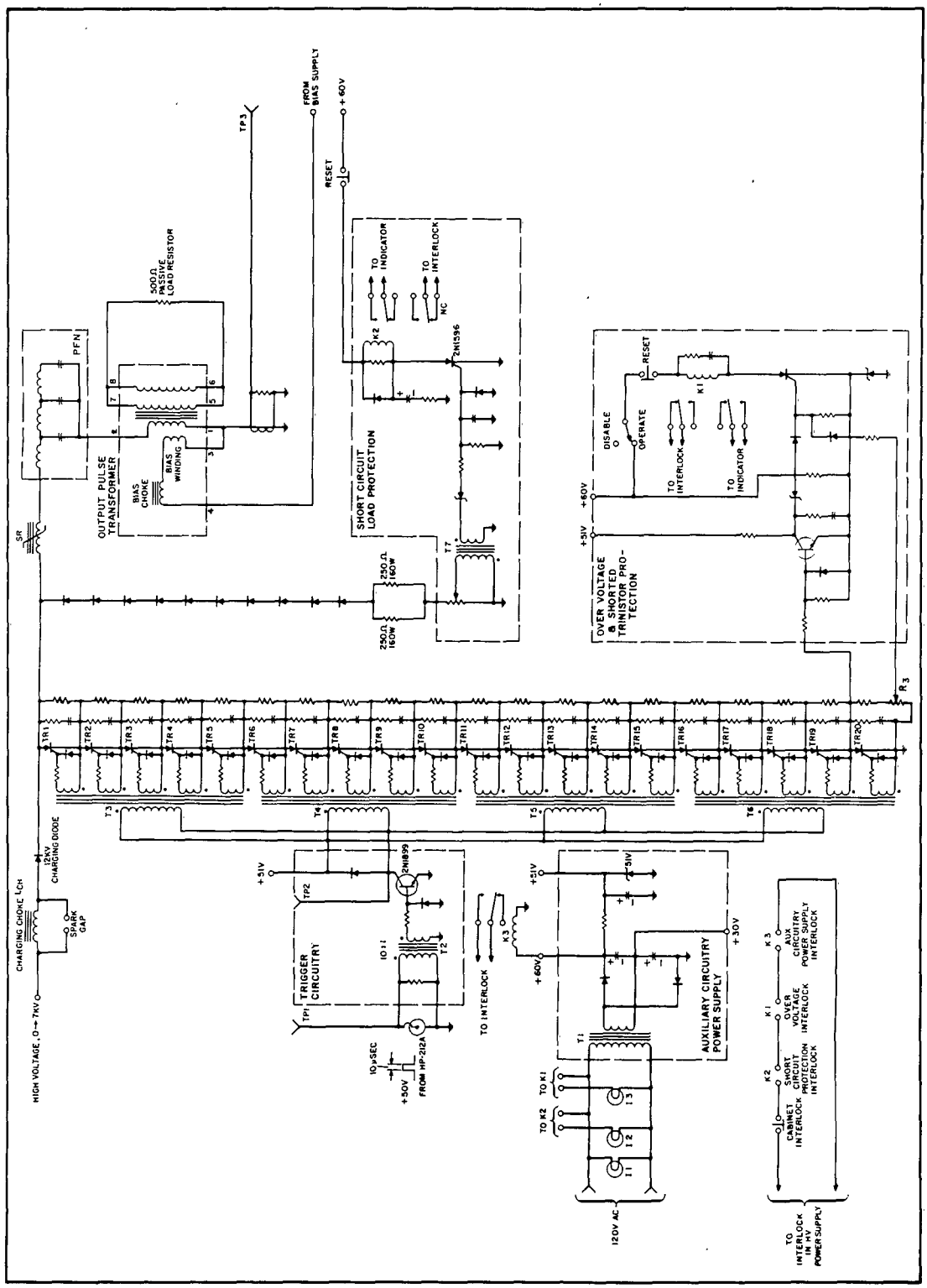


Figure 2. Schematic Diagram of Modulator

Protection circuitry is incorporated to detect abnormal circuit conditions. This circuitry detects and protects the modulator from a short-circuited load, excessive Trinistor voltage, or a shorted Trinistor. The load resistor is designed to present a resistance to the PFN which is 5% lower than the PFN characteristic impedance. This mismatch results in a negative reflection which turns off the Trinistors and resets the saturable reactor core. The negative reflection due to the impedance mismatch is absorbed by the damping diode and damping resistor.

Figure 2 shows the circuit diagram of the breadboard modulator. The sections of this modulator are discussed below:

B. BREADBOARD COMPONENTS

1. Charging Choke

The charging choke for the breadboard charges the PFN to twice the supply voltage. The inductance of this choke is 1.8 henries at 1.73 amperes DC. The resistance of the winding is 8.7 ohms.

The overall dimensions of the charging choke are 8-3/8" H by 8-3/8" W by 8-3/8" D. The charging choke weighs 42 pounds and uses class "S" insulation.

A spark gap is connected across the charging choke to protect the choke. If the high voltage circuit breaker disconnects the power supply from the modulator during the charging cycle, very high voltage can develop across the choke due to the rapidly collapsing current. The spark gap limits this voltage to approximately 18 KV.

2. Charging Diode

The charging diode consists of ten 1200-volt, 12-amp diodes connected in series. These diodes are avalanche type and therefore need no equalizing resistors when connected in series. The ten units in series are rated at 12 KV, which is the maximum voltage that appears on the PFN. This gives a two-to-one safety factor over the voltage which normally appears across the diode assembly.

3. Trinistor Switch

Twenty 700-volt, 70-ampere Trinistors are connected in series for the switching assembly used to discharge the PFN. These Trinistors switch peak currents of 1000 amperes at the full power capability of the modulator.

To insure equal voltage-sharing by each Trinistor in the series string, an equalizing network is shown in figure 3. It consists of a resistor in parallel with the Trinistor and a series R-C network also in parallel with the Trinistor.

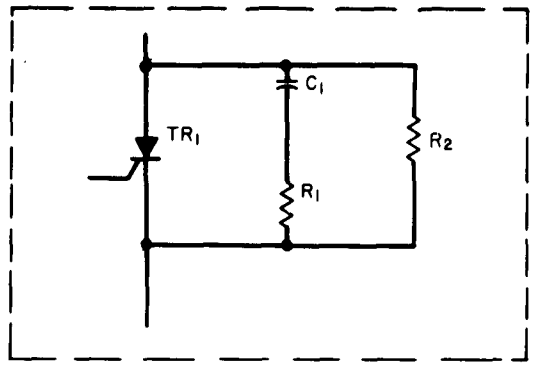


Figure 3. Trinistor Equalizing Network

The parallel resistor insures equal DC voltage-sharing by the Trinistors. The series RC network serves two purposes: The first is to provide AC and transient voltage equalizing and the second is to equalize the turn-on time of the Trinistors. The resistor in series with the capacitor limits the discharge current when the Trinistors switch on.

This entire equalizing network could be replaced by a single Zener diode with equally satisfactory results. This was done early in the testing of the solid-state modulator but the zener diodes supplied for this application were faulty and because of lack of time had to be replaced by the network shown in figure 3.

4. Trinistor Heat Sink Assembly

The Trinistor heat sink assemblies are shown in figure 4. This assembly was designed with five objectives in mind. These are:

1. Use standard, inexpensive, commercial heatsinks
2. Provide adequate cooling
3. Permit use of short interconnecting leads
4. Provide adequate high-voltage insulation
5. Permit easy access to Trinistors.

A forced convection type of heatsink was selected to provide a compact assembly. An individual heatsink is used for each Trinistor. These heatsinks are stacked in four columns with five heatsinks in each column. The four "stacks" are mounted adjacent to each other to form a rectangular assembly. The forced convection is provided with two fans. One fan is mounted at each end of the assembly.

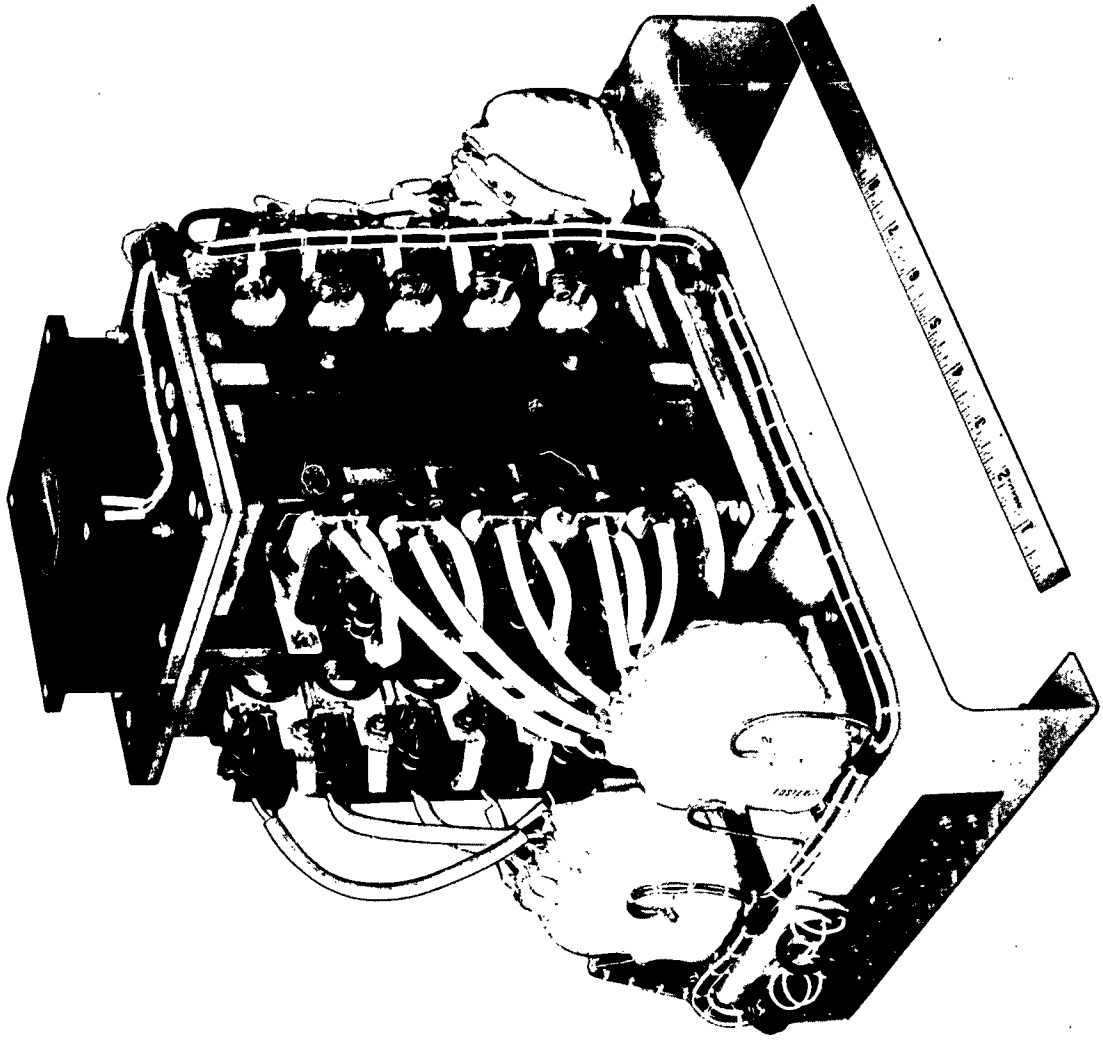


Figure 4. Trinistor Heat Sink Assembly

5. Saturable Reactor

The saturable reactor provides 30 microseconds delay when blocking 12 KV and the current through it just prior to switching is less than 20 amperes. The dimensions of this reactor are 20 inches O. D. and 12 inches I. D. It is 4-1/2 inches high and weighs 106 pounds.

The original specification of the saturable reactor was to provide 20 microseconds delay. This unit introduces 30 microseconds delay, which is greater than necessary. By proper choice of material and designing for 20 microseconds delay, the saturable reactor size can be significantly reduced.

The switching time of the saturable reactor after the delay is approximately three microseconds. The saturable reactor can be made to switch significantly faster by using squarer loop core material. This would result in a more rectangular output pulse from the modulator.

6. Pulse Forming Network

The specifications of the pulse forming network are as follows:

Type: 3 Mesh "E"
Pulse Width: 5 microseconds, at 70% points
Rise Time: 0.8 microseconds, 10% to 90%
Repetition Rate: 300 pps
Ripple: 5% maximum
Characteristic Impedance: 5.25 ohms, -2% +5%
Working Voltage: 11.5 KV
Peak Pulse Current: 1000 amperes
Weight: 140 pounds
Dimensions: 6.25" W x 30" L x 15" H (Bushings extend 2.65" beyond top).

The PFN has been supplied with the first inductor omitted. This inductance is distributed in the saturable reactor and circuit inductance.

The required mutual inductance for the first inductor is provided by a link tightly coupled to the second inductor. The turns in this link are approximately 5 percent of the total number of turns required for the first inductor.

7. Output Transformer

A very compact and lightweight design output transformer has been achieved by using the reset-core type of design. In this type of design, the core consists of an uncut

toroid. This requires the use of a bias winding to prevent saturation of the core and to allow maximum utilization of the core material B-H characteristics. A bias supply is used to reset the core for flexibility in testing, but the pulse reflection or charging current could be used to reset the core in later models.

A small choke is required to isolate the bias winding from the bias source. This choke is mounted in the same container with the output transformer. The output transformer is oil-filled.

The specifications of the transformer are as follows:

Pulse Width	=	5.0 microseconds
PRF	=	300 pps
Primary Voltage	=	5 KV peak
Secondary Voltage	=	50 KV peak
Secondary Load	=	500 ohms
Primary Current	=	1000 Amp peak
Secondary Current	=	100 Amp peak
Rise Time	=	0.5 microseconds
Fall Time	<	1.5 microseconds
Droop	=	3% maximum.

8. Damping Diode Assembly

The damping diode assembly consists of ten 1200-volt, 12-amp diodes connected in series. These diodes are avalanche type and therefore need no equalizing resistors when connected in series.

The resistor in series with the damping diode is 125 ohms and rated at 320 watts. For the short-circuited load condition, where the reflected voltage is equal to the voltage to which the PFN is charged, the peak damping diode current is 96 amperes.

9. Trigger Transformers

Four multiple, secondary, trigger transformers are used to turn on the twenty series-connected Trinistors. Each of the trigger transformers has a single primary and five secondaries. The transformer rise-time is less than one microsecond with less than 10 percent droop for a ten-microsecond pulse. These transformers are insulated for 750 volts between adjacent secondaries and 15 KV to the frame. The dimensions of each transformer are 3" W by 3" D by 3.5" H. Each trigger transformer weighs approximately 1 1/4 pounds.

C. DRIVE CIRCUITRY

The schematic of the drive circuitry for the twenty series-connected Trinistors is shown in figure 5. The circuit consists of a single transistor grounded emitter amplifier which directly drives the Trinistor trigger transformers. The amplifier is driven by a 10-microsecond, 15-volt, positive pulse from an external pulse generator. The amplifier input impedance is 51 ohms and the peak collector current is 3.3 amps. This will supply 500 ma peak drive into each Trinistor gate.

The drive circuitry is built on the "auxiliary circuitry" chassis. The four trigger transformers are mounted separately from the drive circuitry, adjacent to the Trinistor heat sinks.

D. PROTECTION CIRCUITRY

Protection circuitry is incorporated in the breadboard modulator design to sense abnormal circuitry conditions. This protection circuitry detects a short-circuit load condition, a Trinistor over-voltage condition, and a shorted Trinistor condition. If any of these conditions occur, the high voltage power supply interlocked is opened, removing power from the modulator.

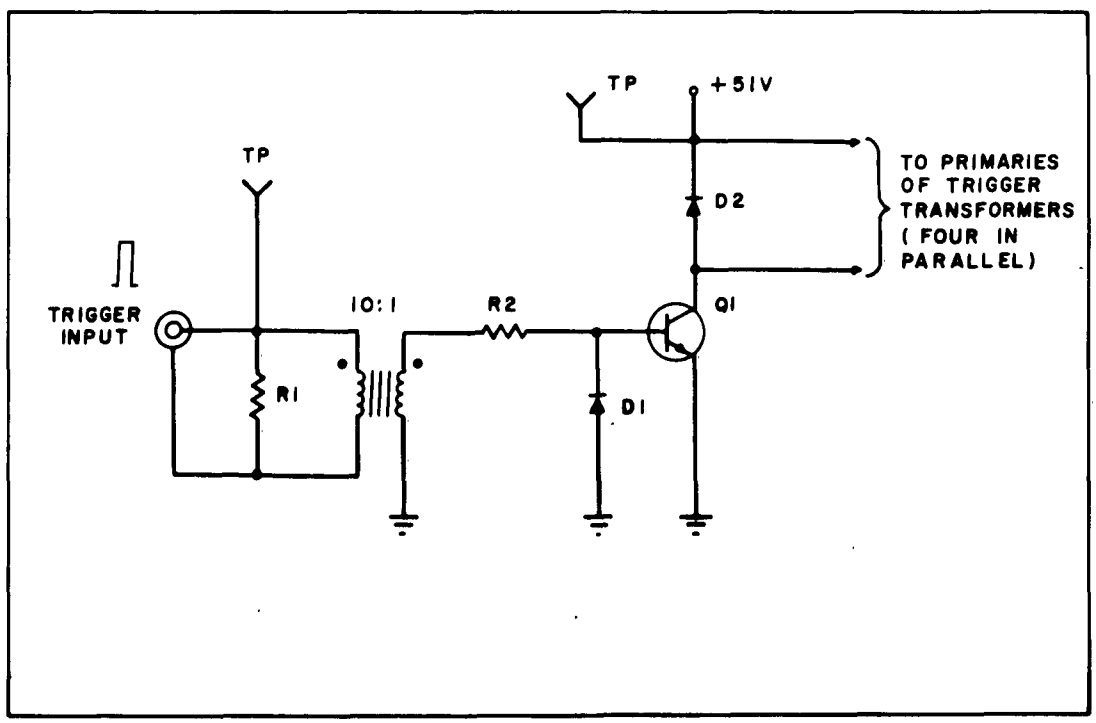


Figure 5. Schematic of Trigger Amplifier

Figure 6 shows the circuit diagram of the short-circuit load protection circuitry. This circuit detects the large voltage reflection that appears across the damping resistor when the modulator is operating into a short-circuit load. This is inverted and stepped down through the input transformer of the detection circuit. The resulting positive pulse at the secondary of the input transformer is coupled through a Zener diode to the gate of a low power silicon-controlled rectifier (SCR). The Zener diode determines the trigger threshold of the SCR. When the SCR is triggered, the relay in the anode circuit is energized and the power supply interlock is opened. The SCR will remain in the conducting state, holding the relay closed, until its anode current is interrupted by the reset switch.

Figure 7 shows the block diagram of the Trinistor over-voltage and Trinistor short-circuit detector. The connections to the Trinistor string are also shown. It senses both for an over-voltage condition of any Trinistor and a short circuit condition across the last Trinistor (TR_{20}) in the string. The over-voltage condition will cause an abnormally high voltage across resistor R_S. This will occur if either the supply voltage is too high or any of the first 19 Trinistors short from anode to cathode. If TR_{20} should short, however, a voltage will not appear across R_S. It is necessary, therefore, to sense for a short across TR_{20}.

Figure 8 shows the schematic of the over-voltage and short detector. The over-voltage detector portion of the circuit is a silicon-controlled rectifier (SCR) with its cathode biased at 24 volts. It will then fire when the gate voltage exceeds 24 volts and close relay K_1. The diodes D_3 and D_4 form an "OR" circuit so that the SCR can be triggered either by the voltage developed across resistor R_S in figure 7 or by the short detector.

The short detector senses the voltage across TR_{20} as previously shown in figure 7. Referring to figure 8, it can be seen that this voltage will turn on the transistor Q_1 and keep the capacitor C_1 discharged. During the interval of the modulator pulse TR_{20} turns on and Q_1 turns off. Capacitor C_1 will begin to charge. Its time constant is such that its charge will never exceed 2 or 3 volts before voltage appears across TR_{20} again and causes it to discharge. If for some reason, TR_{20} should short or remain turned on longer than 2 milliseconds, capacitor C_1 will charge up to 5 volts and fire the SCR, actuating the cut-out relay. The SCR will remain in the conducting stage, holding the relay closed, until its anode current is interrupted by the reset switch.

A "disable" switch is included to remove the anode supply voltage from the SCR. This will allow the modulator to be turned on initially and be operated at reduced voltages. Also, it will be necessary to disable this circuit if it is desired to operate the modulator at very low repetition rates for test purposes.

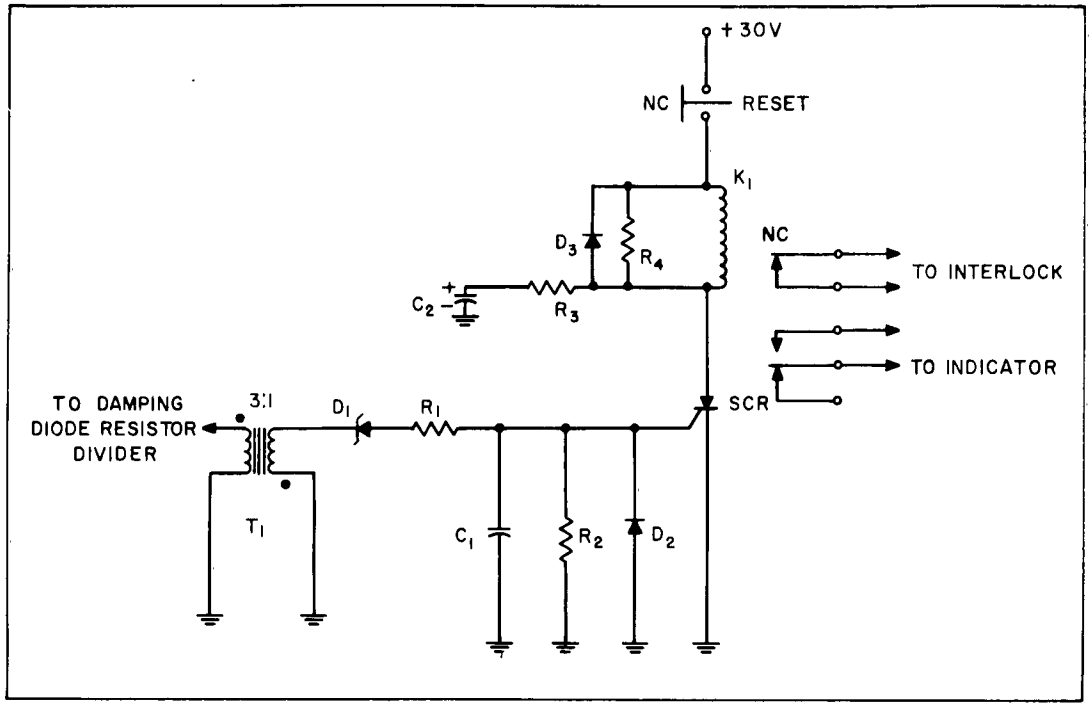


Figure 6. Short Circuit Load Protection Circuitry

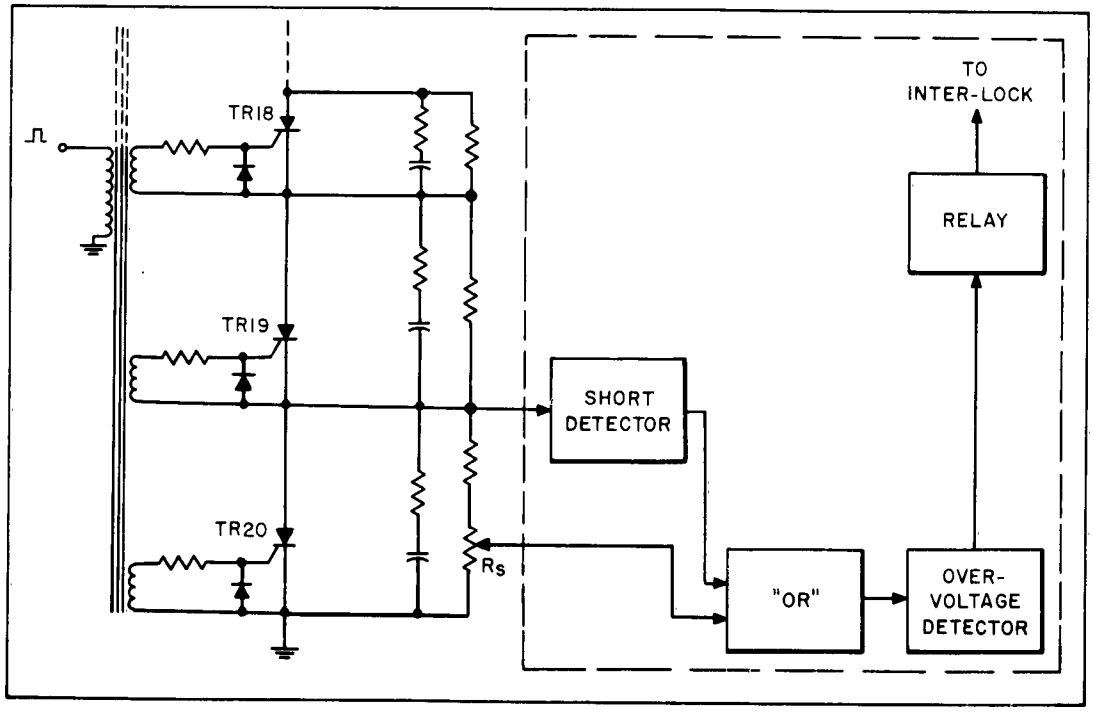


Figure 7. Over Voltage and Short Detector Block Diagram

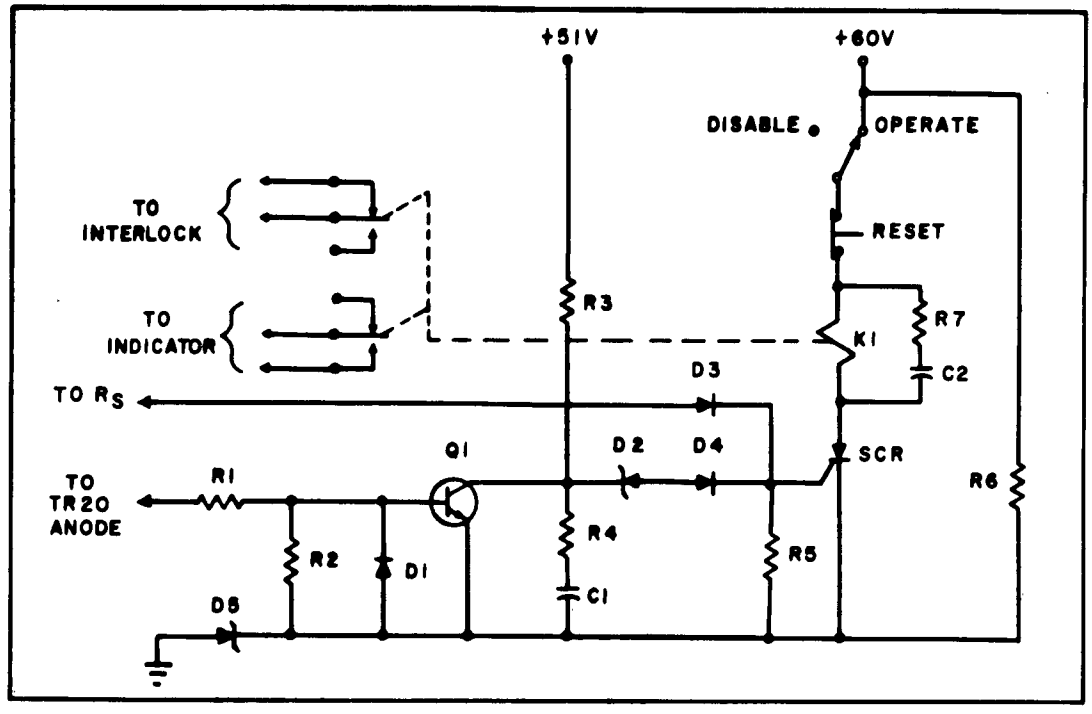


Figure 8. Over Voltage and Shorted Trinistor Detector

E. HIGH VOLTAGE POWER SUPPLY

The schematic of the high voltage power supply and control circuitry is shown in figures 9A and 9B. A photograph of the power supply is shown in figure 10A. The power supply operates from a four-wire, three-phase 60-cps AC, 208-volts RMS source. Other specifications of the power supply are given below:

Output: Zero to 7.0 KV DC, adjustable
Average Load Current: 1.8 amperes maximum
Peak Load Current: 2.7 amperes
Output AC ripple: 1% RMS maximum
Output Voltage variation due to charging PFN: 5% maximum.

The DC voltage is adjustable by means of a three-phase variac, T_1 (see figure 9A). K_1 is a three-pole thermal cutout. The stepped up AC voltage is full-wave rectified by Xenon rectifiers, V_1 through V_6. The AC output ripple is reduced to less than 1% by the choke input filter, L_1 - C_1. The bleeder resistor, R_4, discharges the filter capacitor when AC power is removed. In the event on an over-current situation, the vacuum cutout switch, K_2, removes the DC power from the modulator.

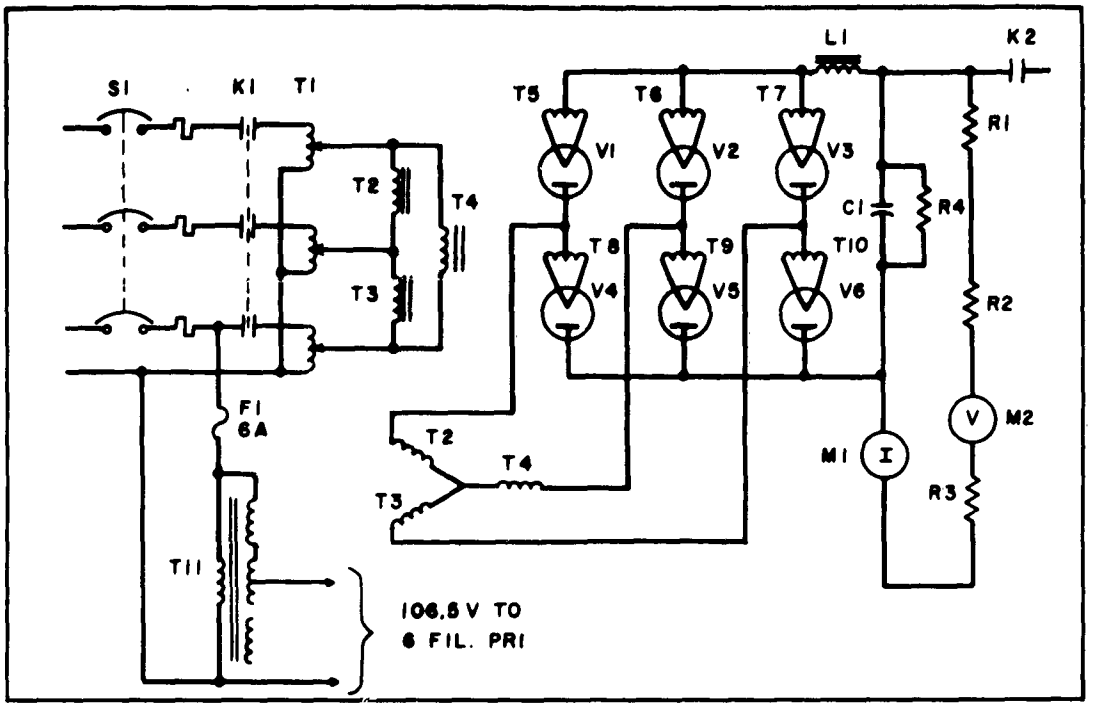


Figure 9A. High Voltage Power Supply

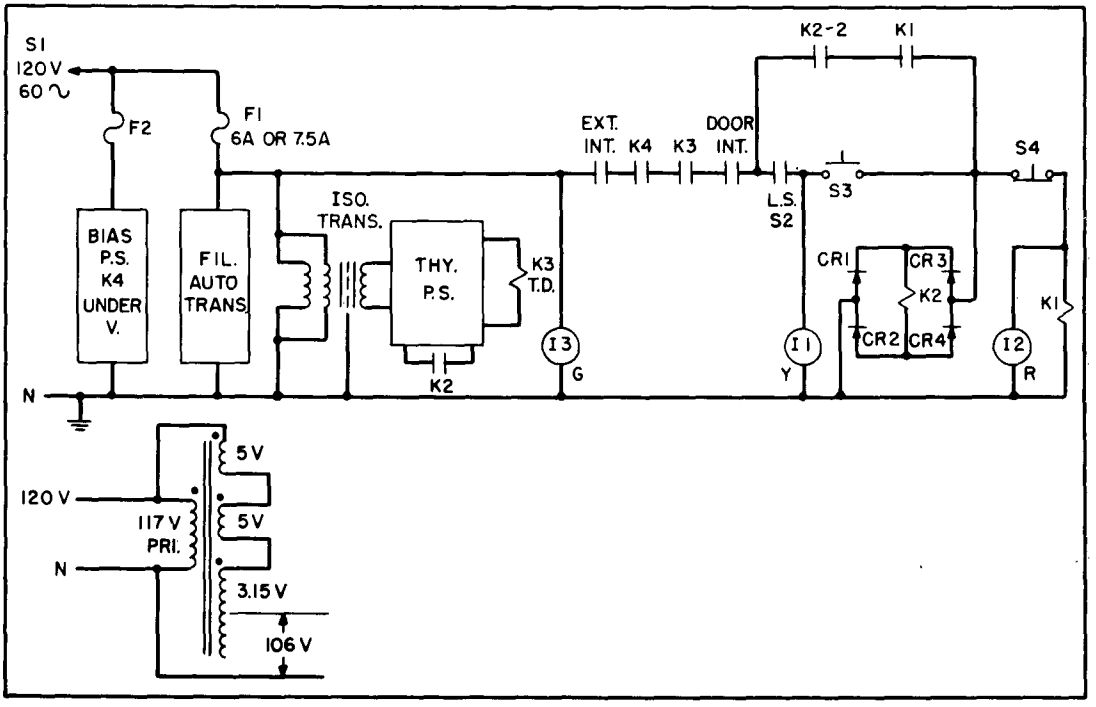


Figure 9B. High Voltage Power Supply Control Circuitry

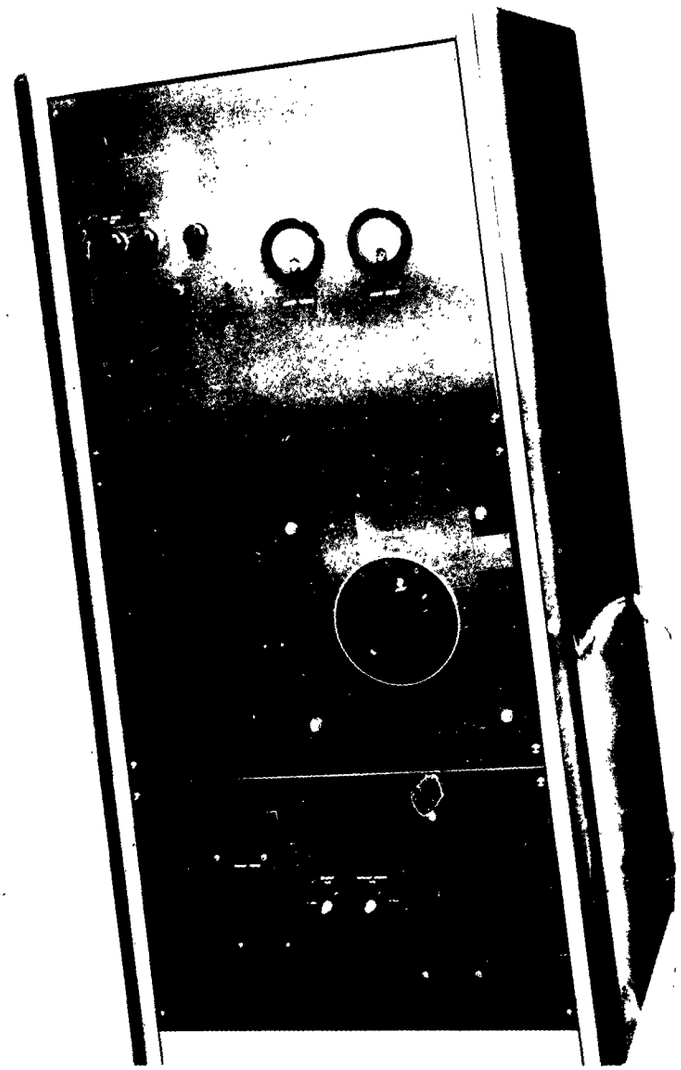


Figure 10A. Power Supply Cabinet

The control circuitry for the high voltage power supply is shown in figure 9B. The interlock system prevents the high voltage from being turned on until the following conditions are satisfied:

1. The door on the power supply is closed.
2. The Xenon rectifier filaments are at operating temperature.
3. The high voltage vacuum cutout switch is closed.
4. The variac is set at zero.
5. Current is flowing from the bias supply through the bias winding of the output transformer in the modulator.
6. All interlocks in the modulator are closed.

Three indicator lights are provided on the power supply cabinet. The green light is "on" when the input circuit breaker is closed. The yellow light indicates that all interlocks are closed and that the high voltage may be turned on. The red indicator light shows when the high voltage is turned on. A DC voltmeter and DC ammeter are also mounted on the front panel of the power supply. These meters monitor the output voltage and current respectively.

Included in the Power Supply Cabinet is a bias supply to provide 6 amperes DC current for the bias winding of the pulse output transformer. Figure 10B shows the schematic of the bias supply. Relay K_1 is a current-controlled relay which will open the power supply interlock if there is insufficient current flowing through the bias winding of the output transformer.

F. DUMMY LOAD

The dummy load required for the 5-megawatt modulator must have a resistance of 500 ohms and be capable of dissipating 7.5 kw of average power continuously. Figure 11 shows the dummy load.

Fifty 250-ohm, 225-watt, non-inductive, wire-wound resistors are connected in a series-parallel arrangement to give the resultant 500-ohm resistance. A compact mounting arrangement was devised, using tinned copper straps and ceramic pillars, so that no single insulator will have more than 20 KV across it.

The cabinet is designed to provide an electrically safe housing for the load resistor. Cooling of the resistors is provided by two fans mounted in the base of the cabinet. Each fan is capable of moving 650 cubic feet of air per minute. This will keep the temperature of the resistors well below their maximum rating and also remove the heat from the work area.

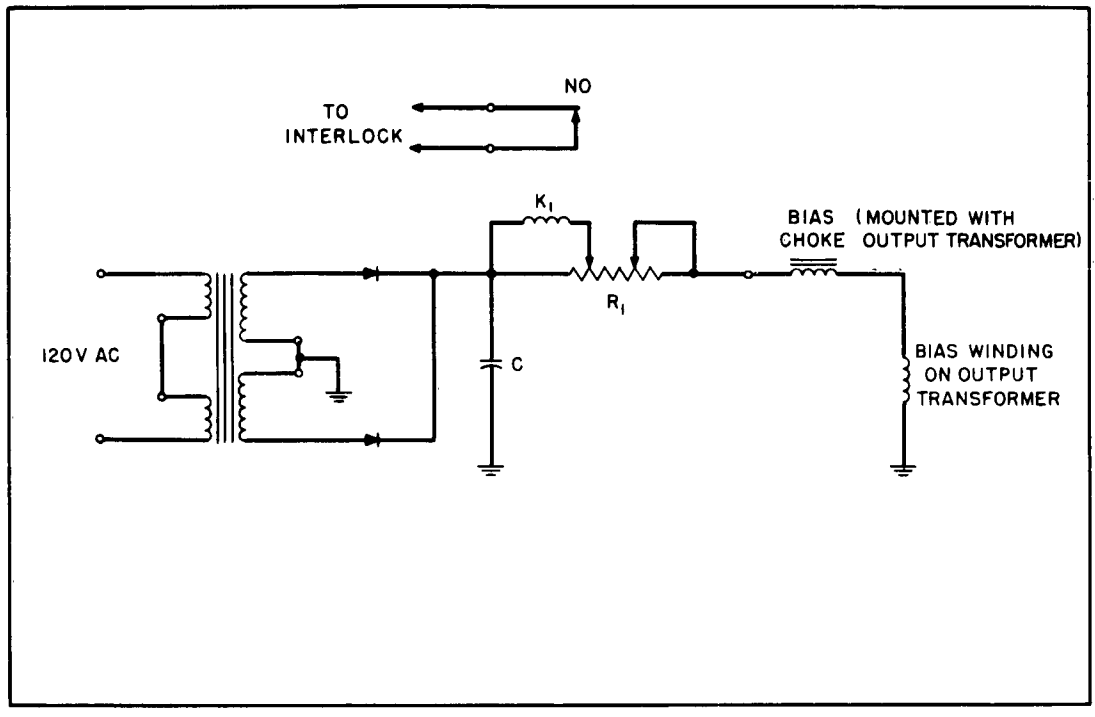


Figure 10B. Bias Supply Schematic

G. MODULATOR CABINET LAYOUT

The top view of the modulator cabinet is shown in figure 12. A photograph of the interior is shown in figure 13. The components were located for minimum lead lengths in the high current path. This was accomplished by placing the Trinistors, the saturable reactor, the pulse-forming network, and the output transformer in a closed loop.

The charging choke is mounted in front of and above the pulse transformer. These two components are cooled by a single blower mounted below the charging choke. The charging diode is mounted adjacent to the charging choke.

The auxiliary circuitry chassis is located on the right side of the cabinet. This chassis contains the protective circuitry, and the power supply for this circuitry.

The connections from the high voltage power supply terminate at the back of the modulator cabinet. The 120 VAC for the indicator lights and auxiliary circuitry power supply, the bias current for the output transformer, and the interlock connections are connected to the modulator through an eight-prong plug. The high voltage wires, from the power supply, pass through the back panel through a rubber grommet.

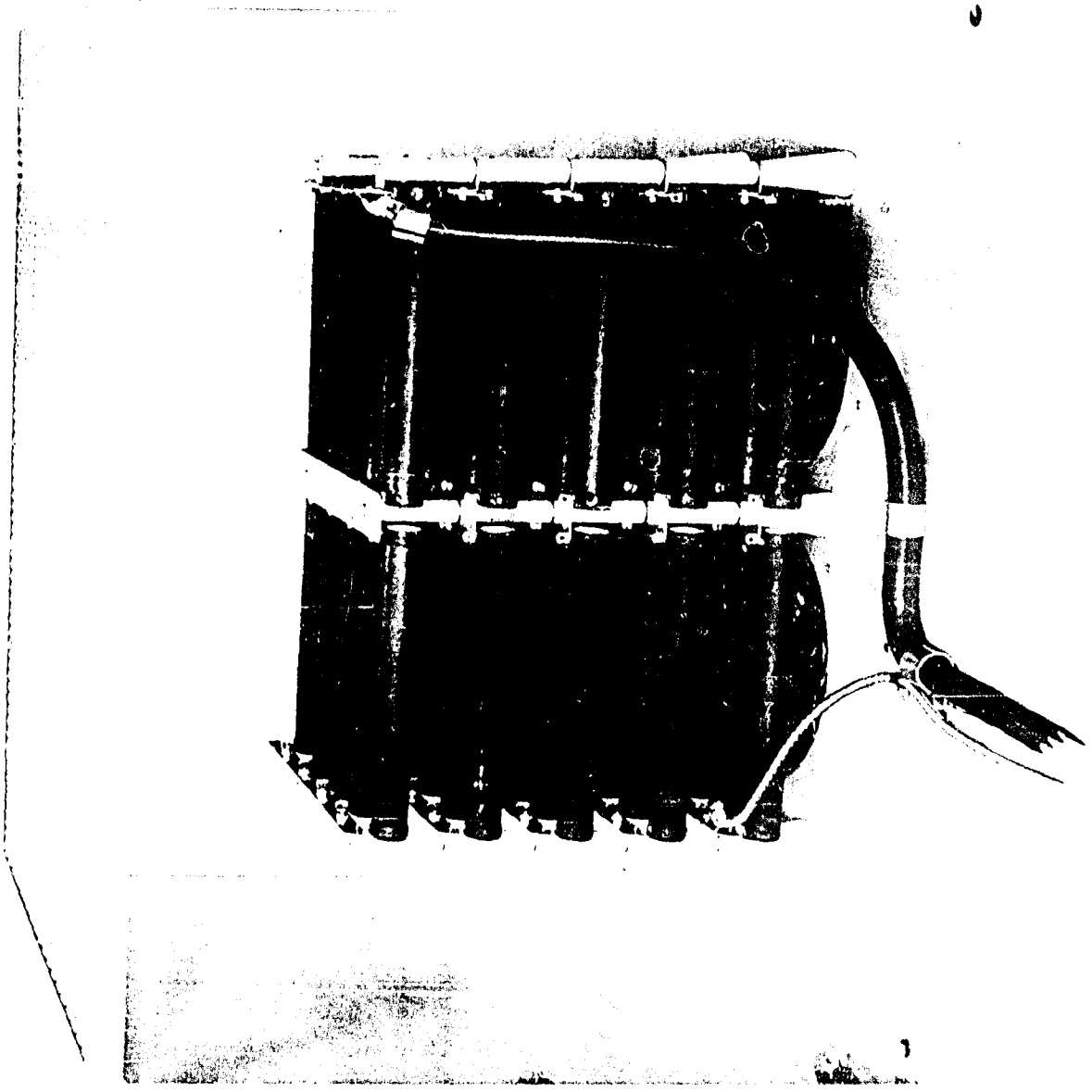


Figure 11. Dummy Load

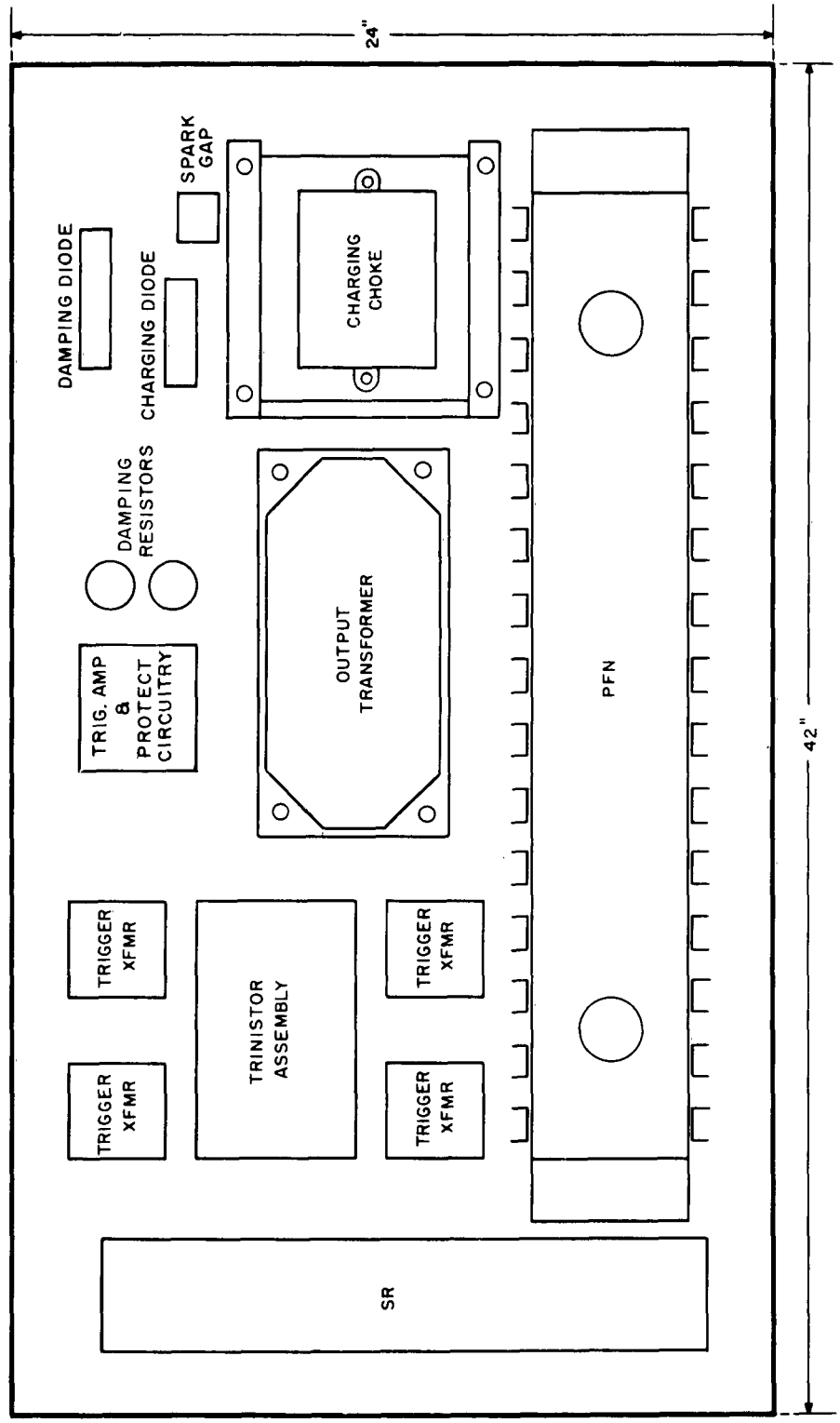


Figure 12. Top View of Modulator Cabinet

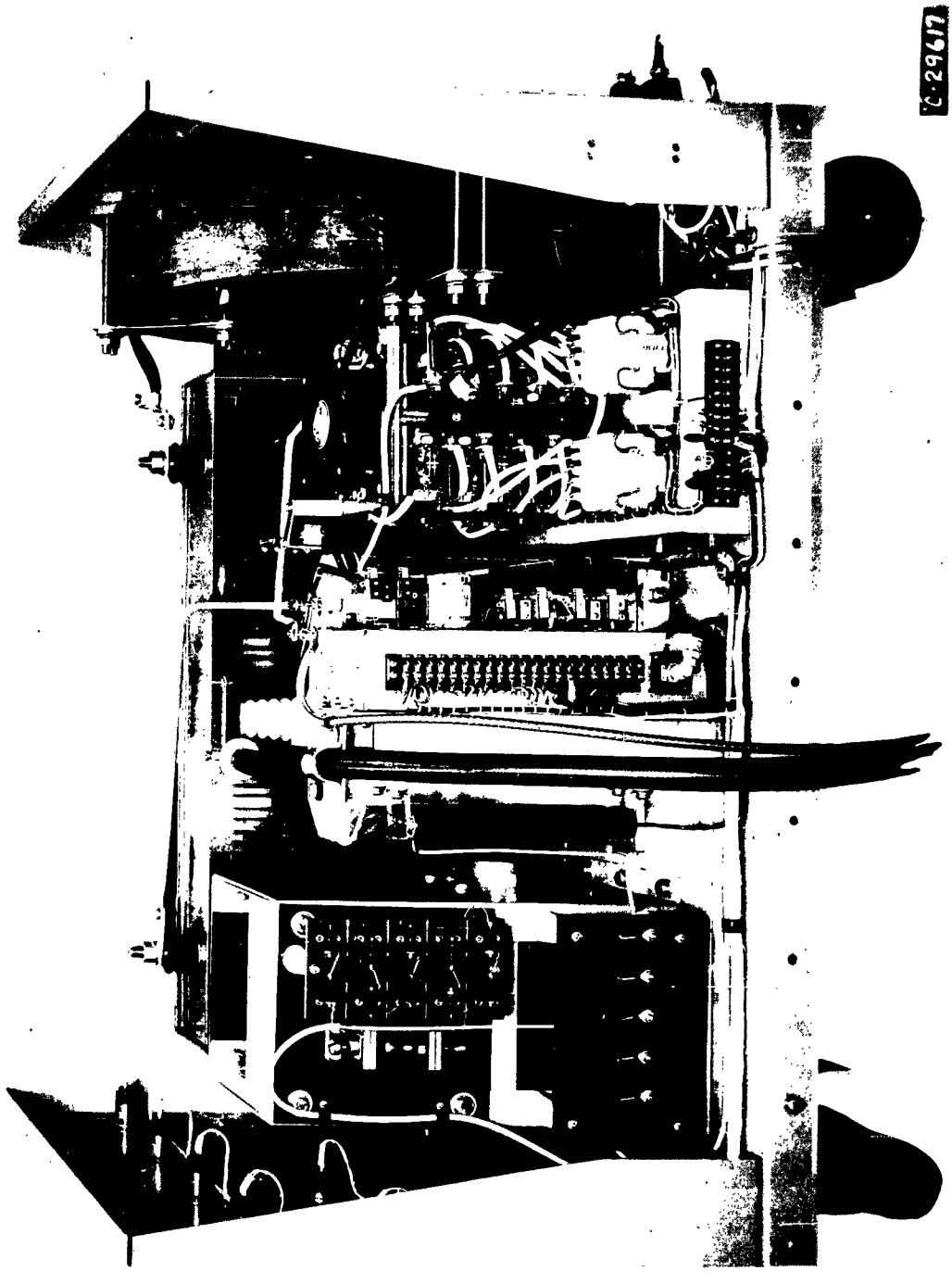


Figure 13. Interior of Modulator Cabinet

The layout of the modulator front panel is shown in figure 14. Four indicator lights are mounted at the top of the panel. One light indicates when the AC power is on. A second light indicates high voltage power. The other two indicator lights turn on if the protective circuitry has tripped the interlock because of a short circuit load condition or an over-voltage or shorted Trinistor condition. Two push-button switches are mounted on the front panel to reset the respective protective circuitry if an interlock is tripped.

Two BNC connectors are mounted on the front panel. One connection is for the trigger input. The other connector is for the output of the current probe which monitors the current through the primary of the pulse transformer. There is also a connector on the front panel to a thermocouple mounted on one of the Trinistors. Additional terminals are on the front panel to monitor the waveshape at the collector of the trigger amplifier and to provide a sync output for an oscilloscope.

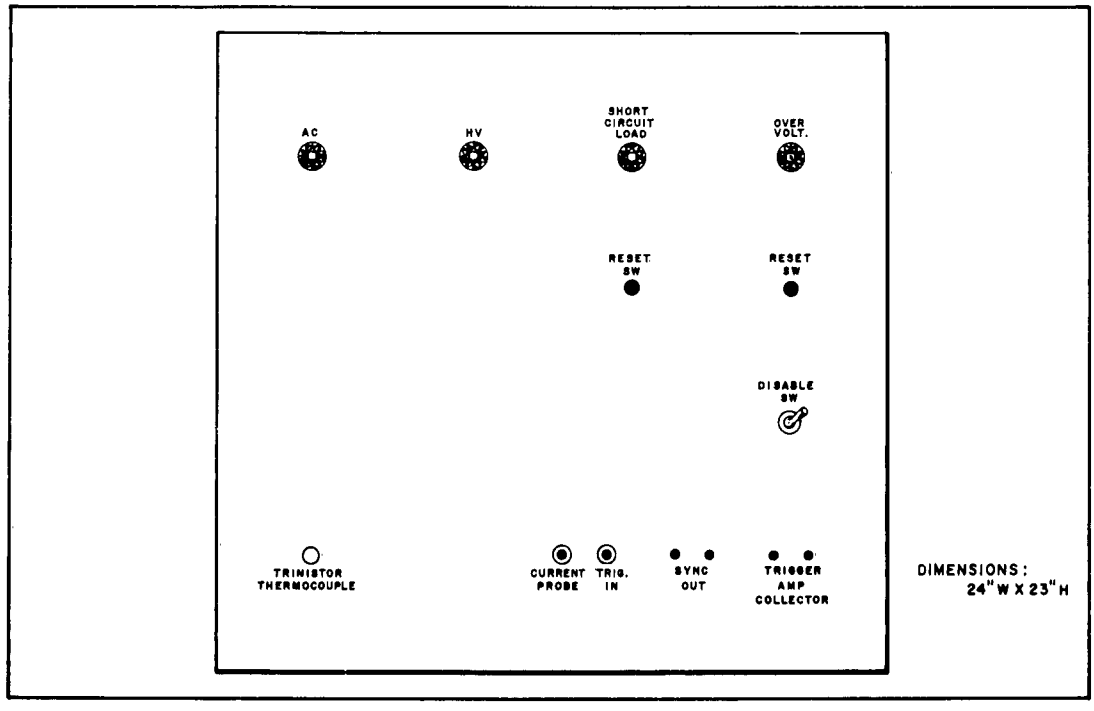


Figure 14. Modulator Front Panel

III. TECHNICAL INFORMATION

A. TRINISTOR CHARACTERIZATION

Initially, seven 700-volt, 70-ampere Trinistors were purchased for evaluation. These Trinistors were characterized to prepare for the design and construction of the high power breadboard modulator. Later on, during the contract, twenty more Trinistors were purchased for use in the actual modulator. These twenty were selected from a group of forty after they were individually tested for forward voltage drop. A representative quantity of them were also tested for leakage current.

All of the Trinistor tests and measurements were designed to provide the most meaningful data for the specific breadboard radar modulator. The parameters measured were leakage current, turn on time, delay time, time jitter, and forward voltage drop. In addition, the inductance of the Trinistor was calculated from the forward voltage drop measurements.

1. Leakage Current Measurements

The leakage current of the seven Trinistors was measured at the full rated anode voltage of 700 volts at 25°C and 105°C. The circuit used for these measurements is shown in figure 15. The measured leakage currents appear in figure 16. Note that at 105°C the leakage current ranged from 0.26 ma to 1.05 ma. This is considerably below the manufacturer's maximum specification of 4.0 milliamperes at 125. C junction temperature.

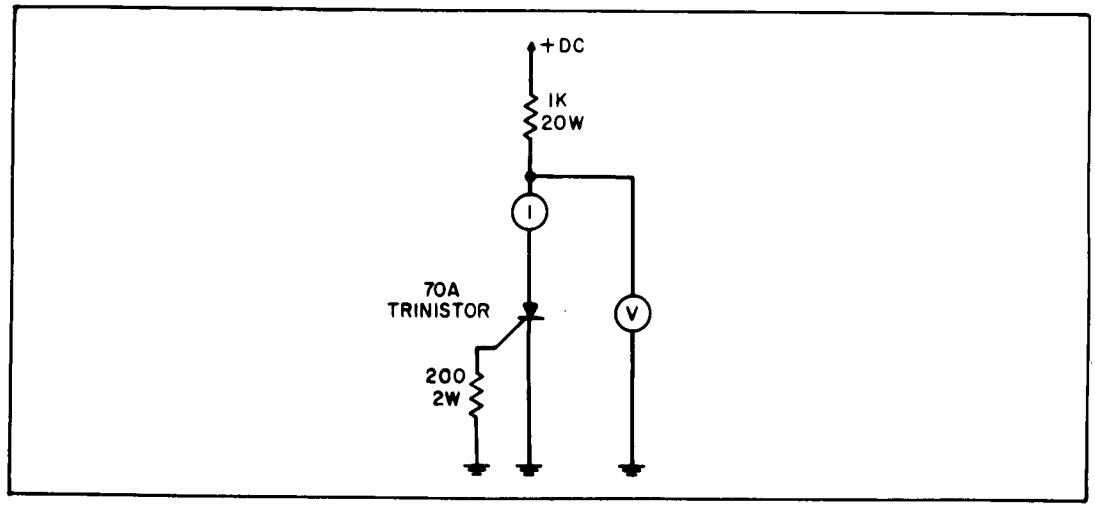


Figure 15. Leakage Current Test Circuit

LEAKAGE CURRENT - MILLIAMPERES at 700 VDC

Trinistor Number	1	2	3	4	5	6	7
Temp - 25°C	.043	.074	.018	.082	.32	.004	.33
Temp - 105°C	.42	.465	.43	.26	.85	.49	1.05

Figure 16. Leakage Current Versus Temperature

The leakage current of twelve more Trinistors was measured at a later date. These twelve Trinistors were selected at random from the group which were obtained for use in the modulator.

The circuit used to measure the leakage current was the same as shown in figure 15 except that the resistor between gate and ground had a value of 24 rather than 200 ohms. This value was used since it was the same as the series gate resistor in the breadboard modulator. The measurements were repeated at 25, 100, and 125°C. Figure 17 shows the results of the measurements. It can be seen that the leakage increases with temperature and voltage, as expected. The leakage values, however, are relatively uniform with a maximum variation of 2 to 1 between Trinistors. The maximum value of leakage at 125°C and 700 volts for any Trinistor was only 1.5 milliamperes.

Trinistor Number	Leakage Current, I Microamperes			
	t = 24°C V= 600 V	t = 100°C V= 600 V	t = 125°C V= 600 V	t = 125°C V= 700 V
22	1.50	280	980	1550
31	0.51	110	530	800
32	1.40	190	820	1250
36	9.00	142	590	1000
37	1.40	118	470	850
38	0.52	138	670	1100
42	0.70	175	680	1150
43	6.20	280	960	1350
45	0.42	135	620	900
46	0.59	175	790	1300
52	1.30	140	590	1000
59	0.14	135	680	1050

Figure 17. Trinistor Leakage Current

2. Turn-on Time Measurements

The actual switching time of the seven Trinistors was measured as a function of load current. Figure 18 shows the circuit used for these measurements. The turn-on times were measured at the anode of the Trinistors. The times measured were from the 10 percent to 90 percent values of the anode voltage change. The turn-on times of the seven samples versus current appear in figure 19. The turn-on times ranged from 0.022 microseconds at 10 amps load current to 0.165 microseconds at 70 amps load current. Note that the Trinistors consistently switched faster at the lower currents than at the higher currents. Figure 20 shows the anode waveform of one of the Trinistors switching 50 amperes.

3. Trinistor Turn-on Delay Measurements

The delay time between application of gate voltage and anode switching was measured on the seven samples. Figure 21 shows the circuit used for these measurements. The delay time was measured as a function of load current. The delay time was measured from the 50 percent amplitude point of the trigger waveform to the 50 percent amplitude point of the Trinistor anode waveform.

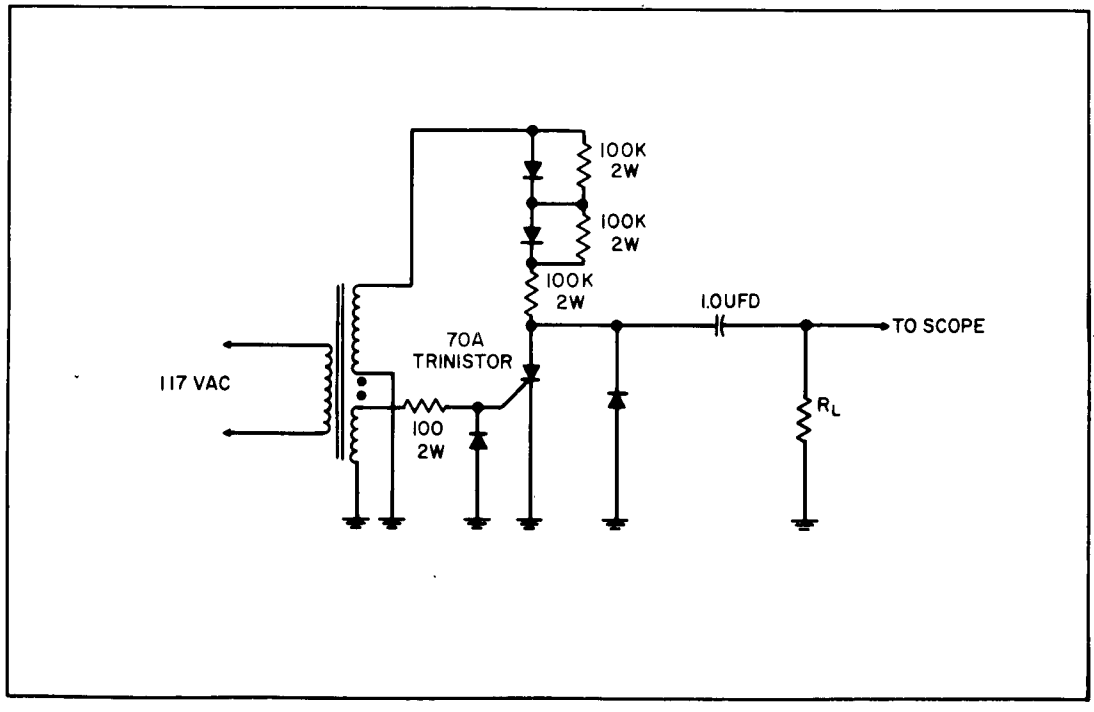
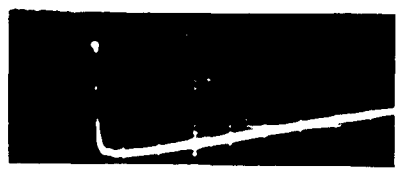


Figure 18. Turn-On Time Test Circuit

TURN-ON TIME - MICROSECONDS

Trinistor Number	10 amps	20 amps	50 amps	70 amps
1	.042 μsec	.070 μsec	.160 μsec	.165 μsec
2	.026 μsec	.042 μsec	.110 μsec	.120 μsec
3	.030 μsec	.036 μsec	.115 μsec	.125 μsec
4	.036 μsec	.040 μsec	.130 μsec	.155 μsec
5	.026 μsec	.032 μsec	.130 μsec	.150 μsec
6	.022 μsec	.030 μsec	.095 μsec	.110 μsec
7	.026 μsec	.032 μsec	.090 μsec	.115 μsec

Figure 19. Turn-on Time vs Switched Current



200 v/cm

t = 1 μsec/cm

Figure 20. Anode Waveform of Trinistor Switching 50 Amps

Figure 22 lists the measured delay times. The shortest time delay occurred when the Trinistors were switching the largest currents. The delay times varied from 0.88 microseconds at 10 amps load current to 0.43 microseconds at 70 amps load current. Figure 23 shows a photograph of the time delay between gate trigger and anode switching waveforms for one of the Trinistors switching 20 amps.

4. Time Jitter Measurements

The time jitter of the anode switching waveform of the seven Trinistors was measured for a load current of 20 amps. The same circuit used for the time delay measurements, shown in figure 21 was used for the time jitter measurements. The actual measurements of time jitter are shown in figure 24. The total jitter ranged from 6 nanoseconds to 18 nanoseconds. Figure 25 is a time exposure showing the time jitter in the anode switching waveform of one of the Trinistors.

5. Trinistor Forward Voltage Drop Measurements

The forward voltage drop across the Trinistor, while conducting, was investigated. This voltage drop is defined as the voltage appearing between anode and cathode of the Trinistor when it is in the "on" state and conducting current.

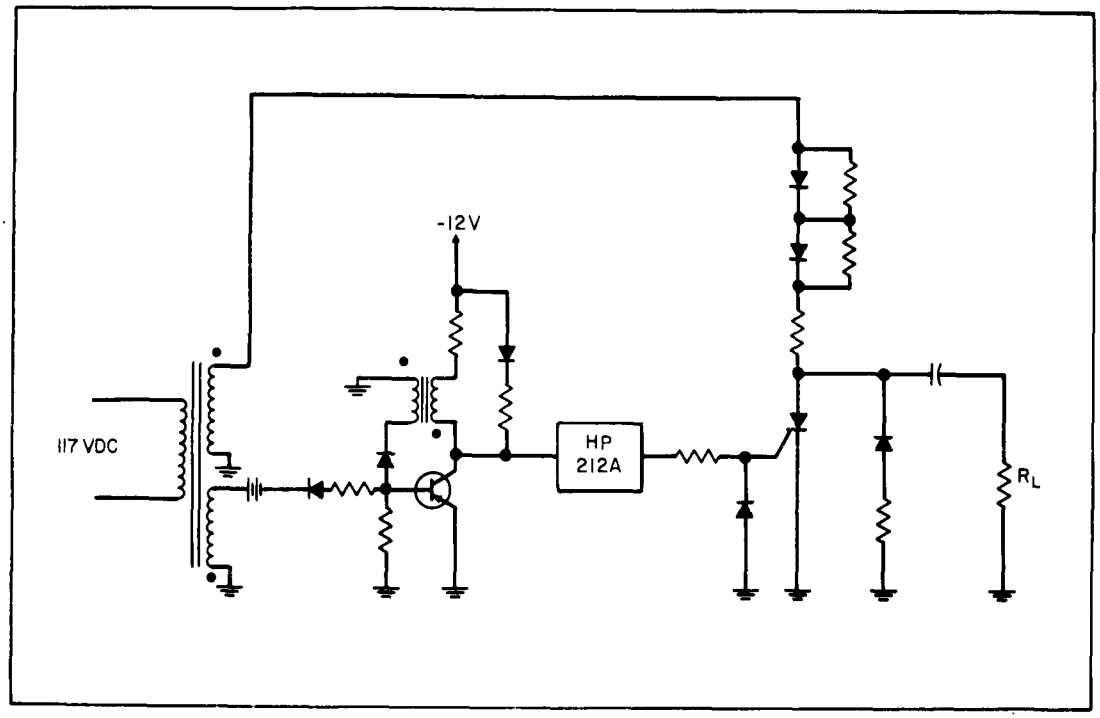
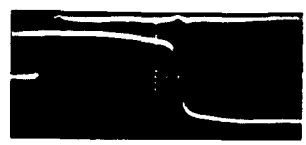


Figure 21. Turn-On Delay Test Circuit

DELAY TIME - MICROSECONDS

Trinistor Number	10 amps	20 amps	50 amps	70 amps
1	.88 μsec	.83 μsec	.80 μsec	.77 μsec
2	.59 μsec	.58 μsec	.57 μsec	.56 μsec
3	.46 μsec	.45 μsec	.43 μsec	.43 μsec
4	.52 μsec	.48 μsec	.48 μsec	.46 μsec
5	.58 μsec	.54 μsec	.56 μsec	.55 μsec
6	.44 μsec	.44 μsec	.42 μsec	.43 μsec
7	.46 μsec	.45 μsec	.44 μsec	.45 μsec

Figure 22. Delay Time vs Switched Current

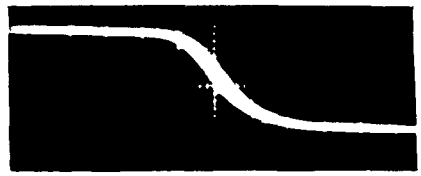


t = 0.1 μsec/cm

Figure 23. Gate Pulse Waveform (Upper) and Anode Waveform (Lower) of Trinistor Switching 20 Amps Showing Time Delay

Trinistor Number	1	2	3	4	5	6	7
Total Jitter (Nanoseconds)	18	9	12	10	9	8	6

Figure 24. Time Jitter of Trinistors



200 v/cm

20 n sec/cm

Figure 25. Time Jitter of Anode Waveform of a Trinistor

The only data available from manufacturers of PNPN controlled rectifiers pertained to either D. C. or half-sine-wave 60-cycle conduction. It was necessary, therefore, to investigate the performance of Trinistors when conducting high pulse currents as would be required in the modulator.

It was found that the forward voltage drop during anode current pulse was dependent upon several factors, such as peak anode current, rate of rise (di/dt) of the current pulse, delay (length of time between "turn-on" at low current and application of the high current pulse), and gate drive. The most significant factors were found to be delay and rate of rise current.

The forward voltage drop of the Trinistors was measured initially using a circuit which pulsed 1000 amps through the Trinistor after the Trinistor was turned on. Figure 26 shows the circuit used. In this circuit, the Trinistor was initially turned on, and held on with a 200 ma. anode current. Relays K1 and K2 are connected in such a manner that upon actuation, the anode current was first stepped up to 20 amperes and then 1000 amperes was pulsed through it. This was done to insure that the entire Trinistor junction was "on" at the time 1000 amperes was applied. Figure 27 shows the peak forward voltage drop for the seven Trinistors initially tested. It can be seen that 19 volts was the typical forward drop under these conditions.

More meaningful measurements of forward voltage drop were made at a later date using a single trinistor in a line-type pulser circuit. These measurements and results are discussed in detail in section C, "Single Trinistor Operation." These measurements include data on forward drop versus delay, initial current, peak current, di/dt, and gate drive.

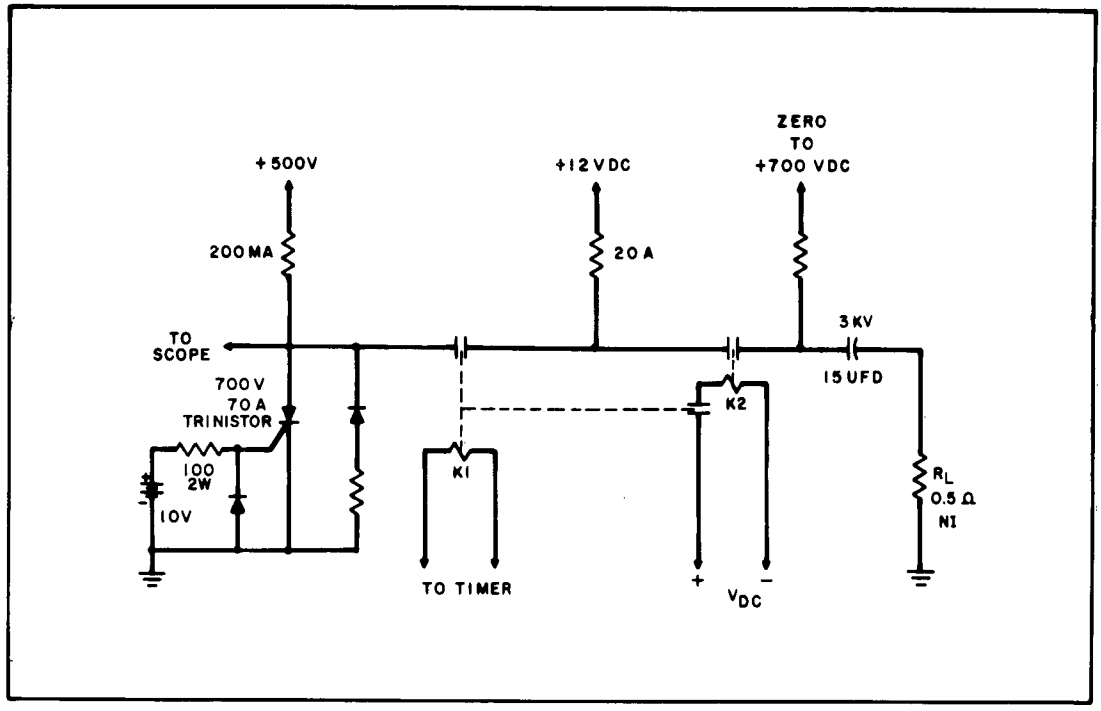


Figure 26. Peak Forward Voltage Test Circuit

Trinistor	1	2	3	4	5	6	7
Peak Forward Voltage Drop	35v	19v	19v	18v	19v	19v	19v

Figure 27. Peak Forward Voltage Drop of Trinistors at 1000 Amps Peak Current

In the selection of the twenty Trinistors used in the breadboard modulator, forty 700-volts, 70-amp, Trinistors were measured for forward voltage drop under a particular set of conditions. The twenty with the lowest forward drop were used; the remaining units were returned to the supplier. Figure 28 shows the test circuit used.

In this circuit, the Trinistor forward voltage drop was measured under the following conditions.

Peak Pulse Current: 300 amperes
Pulse Current Rise Time: 2.5 microseconds (10% to 90%)
Pulse di/dt: 96 amps/microsecond (240 amp/2.5 μsec)
Output Pulse Width: 6.5 microseconds at 50% pts.
Pulse repetition frequency: 50 pps
Peak anode voltage: 215 volts

(more)

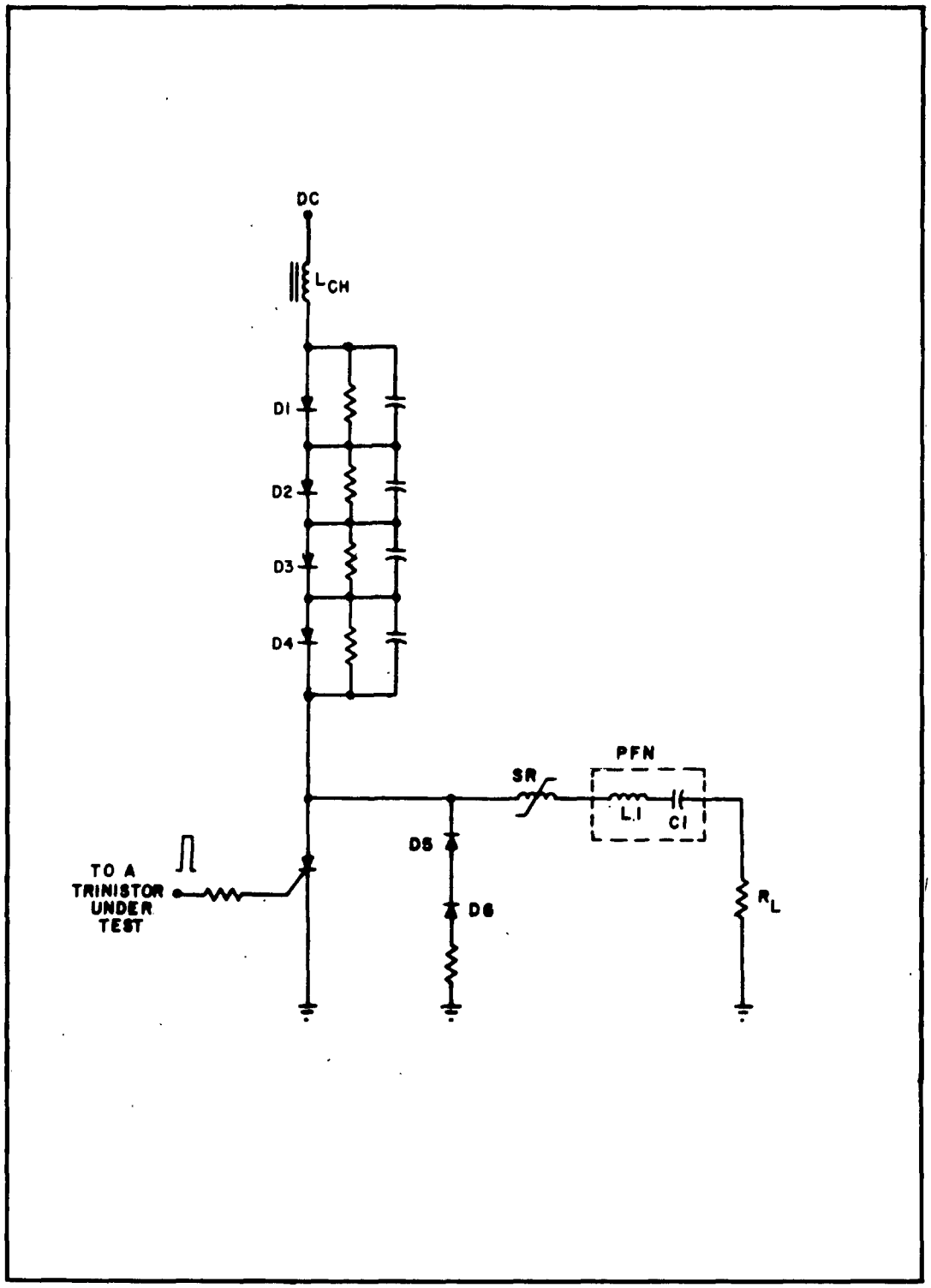


Figure 28. Forward Voltage Drop Test Circuit

Saturable Reactor Delay Time: 8.4 microseconds
Current required to switch Saturable Reactor: 6 amperes
Peak Gate Current: 500 milliamperes
Gate Pulse Width: 10 microseconds.

Figure 29 shows a graph of the number of units versus forward voltage drop. It can be seen that 34 of the 40 units measured between 4.5 volts and 10 volts drop. The six units which measured between 14 volts and 65 volts were considered unacceptable for the solid-state modulator and were rejected.

B. TRINISTOR POWER DISSIPATION

The power dissipated within the Trinistor when switching pulse currents was found to vary as a function of the delay in the current pulse. Figure 30 shows the circuit used to investigate this effect. It will be seen that it is a modified line type pulser. The normal load resistor is replaced by a short circuit so that the high currents desired could be obtained at reasonable voltages. Also, since the main object was to investigate the current, power, and voltage in the Trinistor, rather than the load, the load would be superfluous. Most energy stored in the PFN is dissipated in resistor R_1. A small amount of this energy, of course, is dissipated in the Trinistor.

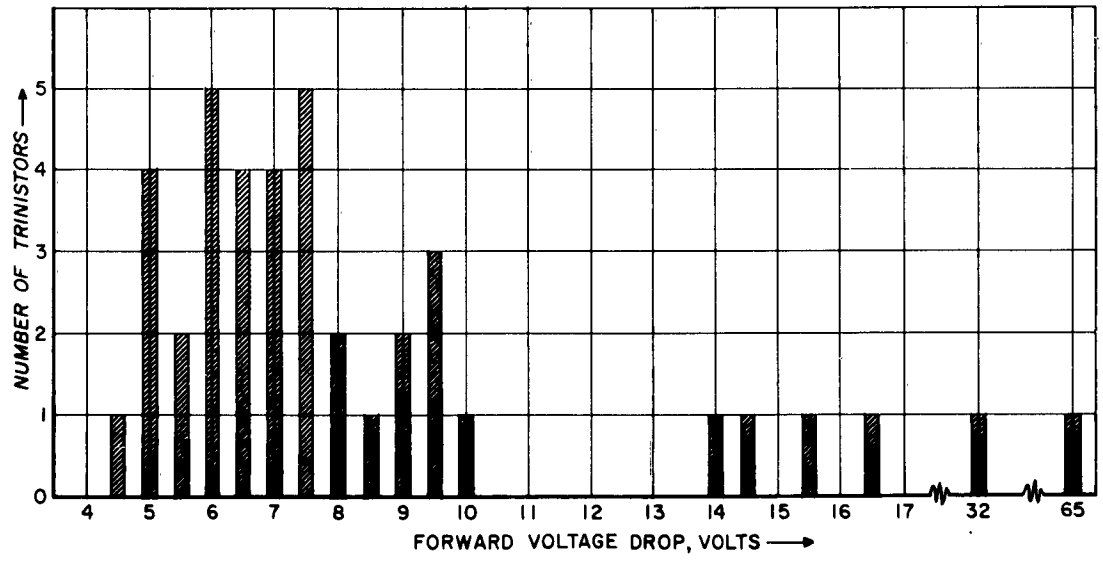


Figure 29. Number of Trinistors Versus Forward Voltage Drop

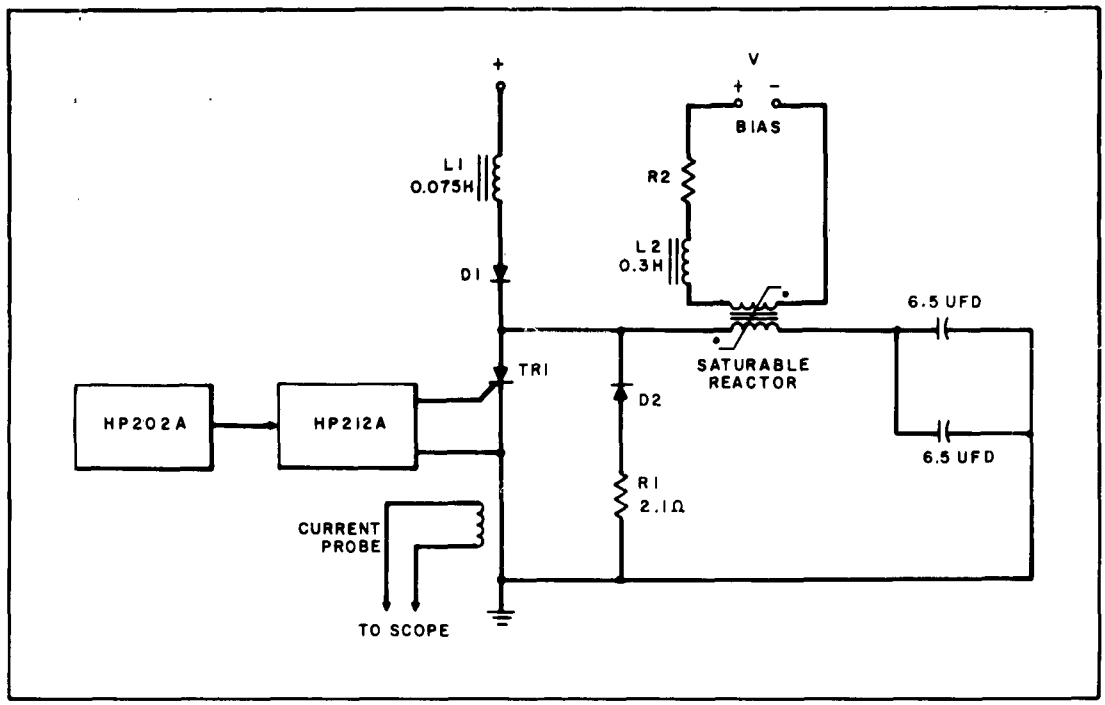


Figure 30. Variable Delay Test Circuit

The delay introduced by the saturable reactor was varied by biasing the core of the reactor. This was done by placing an additional winding on the reactor. The choke, L_2, serves to isolate the winding from the bias supply for pulse currents. With this arrangement, the saturable reactor delay is decreased by increasing the bias current.

The pulse current through the Trinistor was observed on the oscilloscope through a toroidal current transformer placed in the Trinistor cathode lead. The forward voltage drop was measured by connecting the oscilloscope probe to the Trinistor anode and cathode terminals. These connections were made at a point as close as possible to the body of the Trinistor to eliminate introduction of errors due to voltage drops across the anode and cathode connecting leads.

The power dissipated in the Trinistor was measured indirectly by calibrating the Trinistor heat sink. A 4" x 4" x 1/8" aluminum plate with black enamel finish was used for the heatsink. This was calibrated in terms of Trinistor stud temperature versus power dissipated by passing D. C. through an "ON" Trinistor. The current and the voltage across the Trinister were used to calculate the power being dissipated. The temperature at which the heatsink stabilized was proportional to a given amount of power for the given set of conditions. Figure 31 shows the calibration curve for this particular heatsink. When

operating the Trinistor under pulse conditions, the temperature at which the temperature stabilized was noted and the power read from this curve.

Figure 32 shows the data taken on a 70-ampere Trinistor where:

I_p = peak anode current

V_p = peak voltage on PPN

di/dt = rate of rise of current pulse

t_d = delay due to saturable reactor

V_{PF} = peak forward drop from anode to cathode

P_d = power dissipated in Trinistor.

Data was taken for peak pulse currents of both 1000 and 1500 amperes. The equipment did not permit a 30 μsec delay at 1500 amperes and a 6 μsec delay was not attempted. It can be seen that, at 1000 amperes, the power dissipated increased from 8.7 watts to 13.0 watts as the delay was changed from 30 μsec to 6 μsec. At 1500 amperes it can be seen that, for a given delay, the power has increased approximately as the square of the current when compared to the 1000 ampere data. A plot of the peak forward voltage drop and power dissipated for a 1000 ampere pulse versus the delay is shown in figure 33.

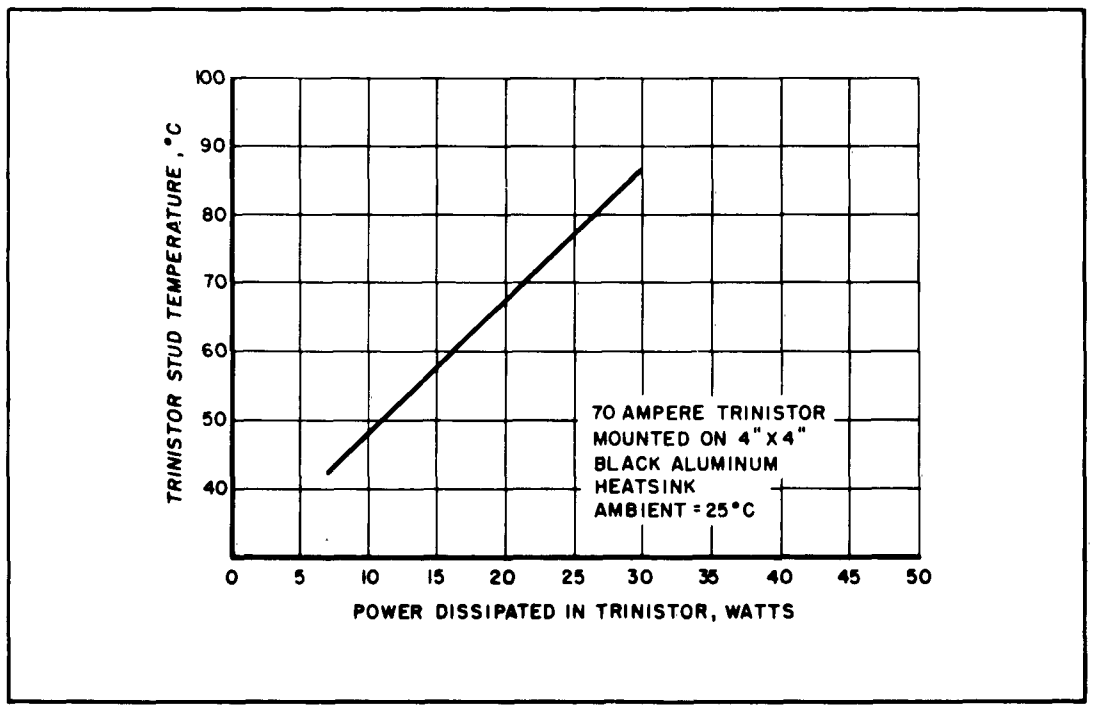


Figure 31. Trinistor Temperature Versus Power Dissipated

PULSE WIDTH = 6.6 μsec (at 50% pts)
PULSE RISE TIME = 3.1 μsec (10-90%)
REPETITION RATE = 300 PPS
AMBIENT TEMP. = 25°C

I_P Amperes	V_P Volts	di/dt Amp/μsec	t_d μsec	V_{PF} Volts	Stud Temp °C	P_d Watts
1000	280	323	30	11.8	45	8.7
1000	265	323	20	13.5	47	9.5
1000	265	323	10	14.5	51	11.5
1000	255	323	6	17	54	13.0
1500	390	473	20	20	64	18.0
1500	390	473	10	24	72	22.5

Figure 32. 70 Ampere Trinistor Pulse Current Data

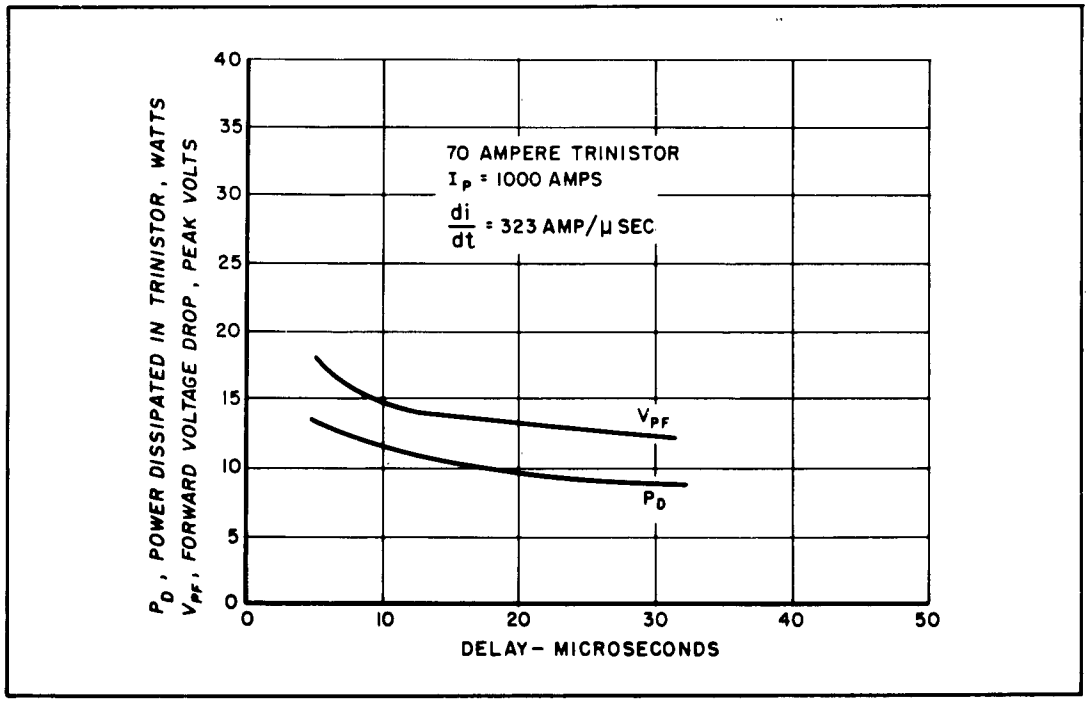


Figure 33. Trinistor Forward Voltage Drop and Power Versus Delay

C. SINGLE TRINISTOR OPERATION

Figure 34 shows a single Trinistor line-type pulser. This was used to investigate Trinistor forward voltage drop as a function of gate drive and pulse width. The operating characteristics of the circuit were as follows:

Pulse repetition rate	=	400 pps
Peak pulse current	=	475 amps
Saturable reactor delay	=	4 μsec
Pulse width	=	5 μsec (at 50% pts).

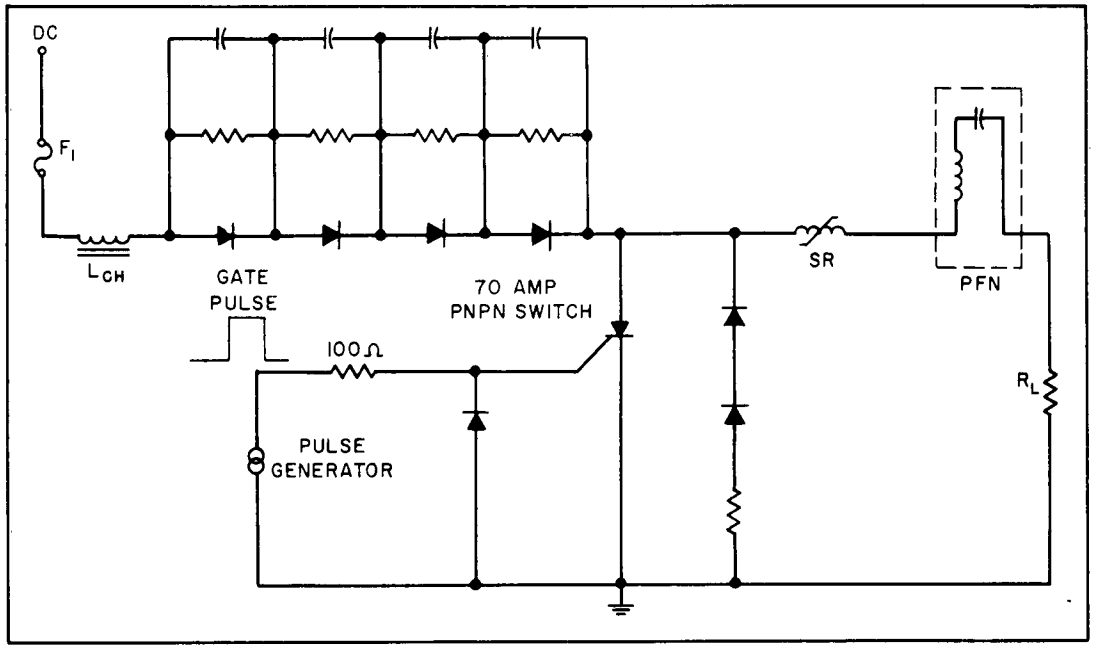


Figure 34. Single PNPN Switch Modulator

Representative waveforms of the anode current and the forward voltage drop across the Trinistor are shown in figures 35 and 36.

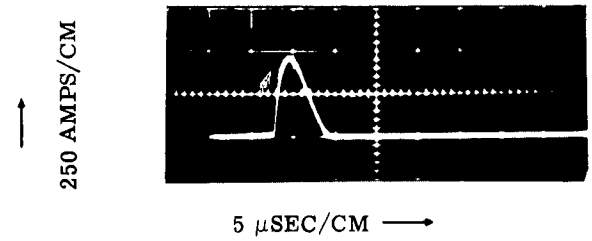


Figure 35. Output Pulse Current Waveform

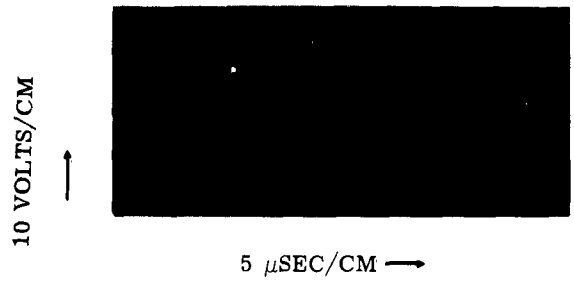


Figure 36. PNPN Switch Forward Voltage Drop

1. Gate Drive

The PNPN switch forward voltage drop was measured as a function of gate drive level. The gate pulse was 10 microseconds wide and the amplitude was varied from 60 ma peak to 800 ma peak. The forward voltage drops measured are shown in figure 37. The voltage drop for three samples of PNPN switches varied from 25 volts at 60 ma gate drive to 16 volts at 800 ma gate drive. The circuit of figure 34 was used for these measurements with the PNPN switch switching 475 amps peak. The saturable reactor delay was 4 microseconds.

PEAK GATE DRIVE (10 μsec pulse)	70 AMPERE PNPN SWITCH FORWARD VOLTAGE DROP		
	UNIT #2	UNIT #4	UNIT #6
60 MA	30v	36v	29v
100 MA	28v	34v	25v
190 MA	25v	32v	24v
300 MA	24v	32v	23.5v
400 MA	23v	32v	23.5v
500 MA	22v	32v	23.5v
600 MA	22v	32v	23v
800 MA	22v	32v	22.5v

Figure 37. Forward Voltage Drop Versus Peak Gate Drive

2. Gate Pulse Width

The PNPN switch forward voltage drop was measured as a function of gate pulse width. The peak gate drive was held constant at 500 ma. The circuit of figure 34 was used and the peak current switched was 475 amps. The saturable reactor delay was 4 microseconds. The forward voltage drops measured for the three samples are shown in figure 38. The forward voltage drop varied from 34 volts at 0.2-microsecond gate pulse width to 16 volts at a 10-microsecond gate pulse width. The peak gate drive was 500 ma.

Figure 39 shows the voltage and current waveforms at the gate of the 70-amp PNPN switch. A 10-microsecond gate pulse width is shown in these waveforms. Figure 40 shows gate voltage and current waveforms for a 2-microsecond gate pulse width.

GATE PULSE WIDTH	70 AMPERE PNPN SWITCH FORWARD VOLTAGE DROP		
	UNIT #2	UNIT #4	UNIT #6
10 μsec	22v	32v	23.5v
4 μsec	23v	32v	23.5v
1 μsec	24v	32v	24v
0.5 μsec	26v	32v	26v
0.2 μsec	(does not trigger)	34v	28v

Figure 38. Forward Drop Versus Gate Pulse Width

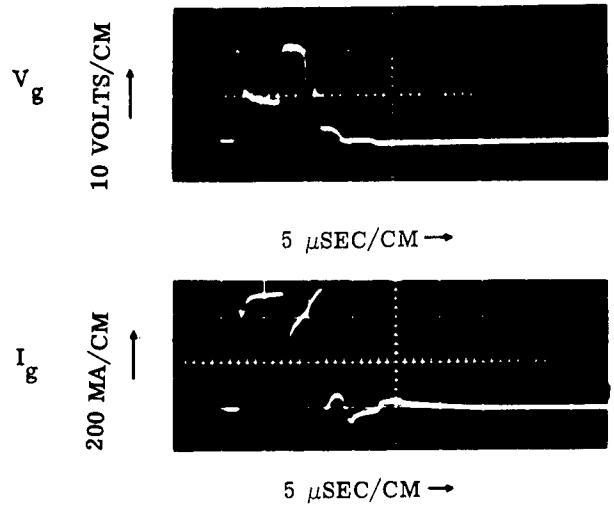


Figure 39. Gate Voltage and Current Waveforms - 10 μsec pulse

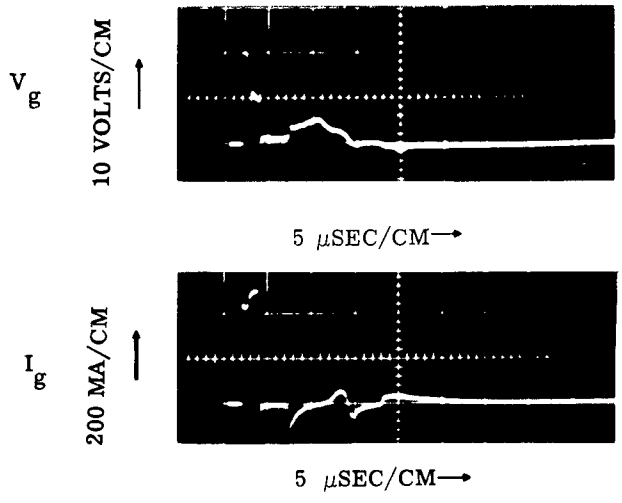


Figure 40. Gate Voltage and Current Waveforms - 2 μsec pulse

3. Current Delay

The PNPN switch forward voltage drop was measured as a function of delay time between anode switching and the peak output pulse current. The circuit of figure 41 was used for these measurements. The circuit is similar to the single PNPN switch modulator circuit, with the exception of the addition of a second PNPN switch. The second PNPN switch, a 400-volt, 200-amp Trinistor, allows the 70-ampere PNPN switch under test to be turned on at any predetermined time prior to the application of the peak pulse of current. A saturable reactor with a delay of 4 microseconds is used in the circuit for the protection of the 200-ampere Trinistor. The current in the 70 ampere PNPN switch is a 3 amps prior to switching on the 200-amp unit.

The peak forward drop across the PNPN switch at 475 amps peak varied from 6.5 volts at 150 microseconds delay to 16 volts at 7 microseconds delay. The measured data appears in figure 42. Figure 43 shows a plot of this data. The peak gate drive was 300 milliamperes and the gate pulse width was 10 microseconds. The output pulse width was 6.8 microseconds. These measurements of peak forward voltage drop versus delay time indicate that the PNPN switch junction is not fully on with a delay as short as 4 microseconds.

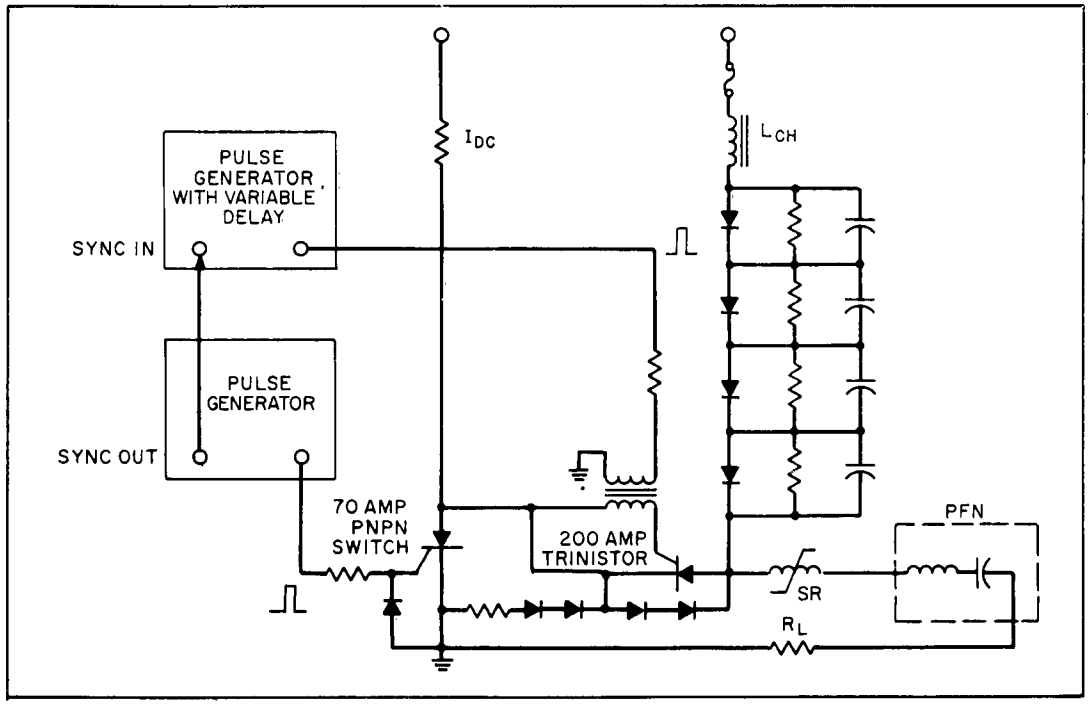


Figure 41. Forward Voltage Versus Delay Test Circuit

DELAY	70 AMPERE PNPN SWITCH FORWARD VOLTAGE DROP		
	UNIT #2	UNIT #4	UNIT #6
7 μsec	9.5v	16.0v	10.5v
8 μsec	9.0v	15.0v	10.0v
10 μsec	8.5v	14.0v	9.7v
15 μsec	7.9v	12.0v	8.7v
20 μsec	7.5v	10.2v	8.2v
25 μsec	7.2v	9.2v	8.0v
30 μsec	7.0v	8.5v	7.7v
40 μsec	6.9v	7.7v	7.2v
50 μsec	6.6v	7.5v	7.0v
100 μsec	6.5v	6.7v	7.0v
150 μsec	6.5v	6.5v	6.7v

Figure 42. Forward Voltage Drop Versus Delay Data

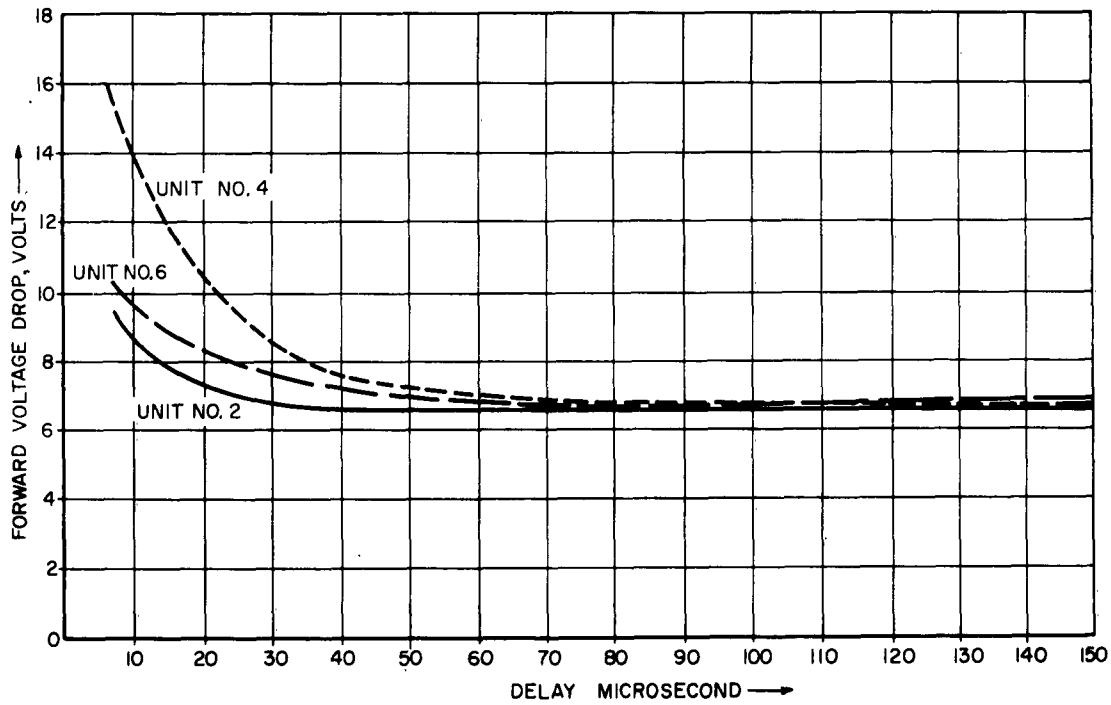


Figure 43. Plot of Forward Voltage Drop Versus Delay

The total PNPN switch forward voltage drop, with 150 microseconds delay and 475 amps peak current is about 6.5 volts. Three volts of this voltage drop is due to the PNPN switch lead inductance. The remaining 3.5 volts drop across the junction is in good agreement with the manufacturer's published data.

4. Anode Current Prior to Output Pulse

The forward voltage drop of three 70-amp, 700-volt, PNPN switches was measured with the anode current prior to discharge of the PFN as the variable. The circuit shown in figure 44 was used for these measurements. A 400-volt, 200-ampere Trinistor was used for discharging the PFN through the 70-amp PNPN switch under test. Note that the 70-ampere PNPN switch under test is always on. This is to insure that the PNPN switch junction is fully on.

The data of forward voltage drop versus initial DC current appears in figure 45.

The PNPN switch forward voltage varied from 11.0 volts with an initial anode current of 200 milliamperes to 7.5 volts with an initial DC current of 3.0 amps. The peak anode current was 475 amps. The 70-amp PNPN switch gate drive was 300 milliamperes.

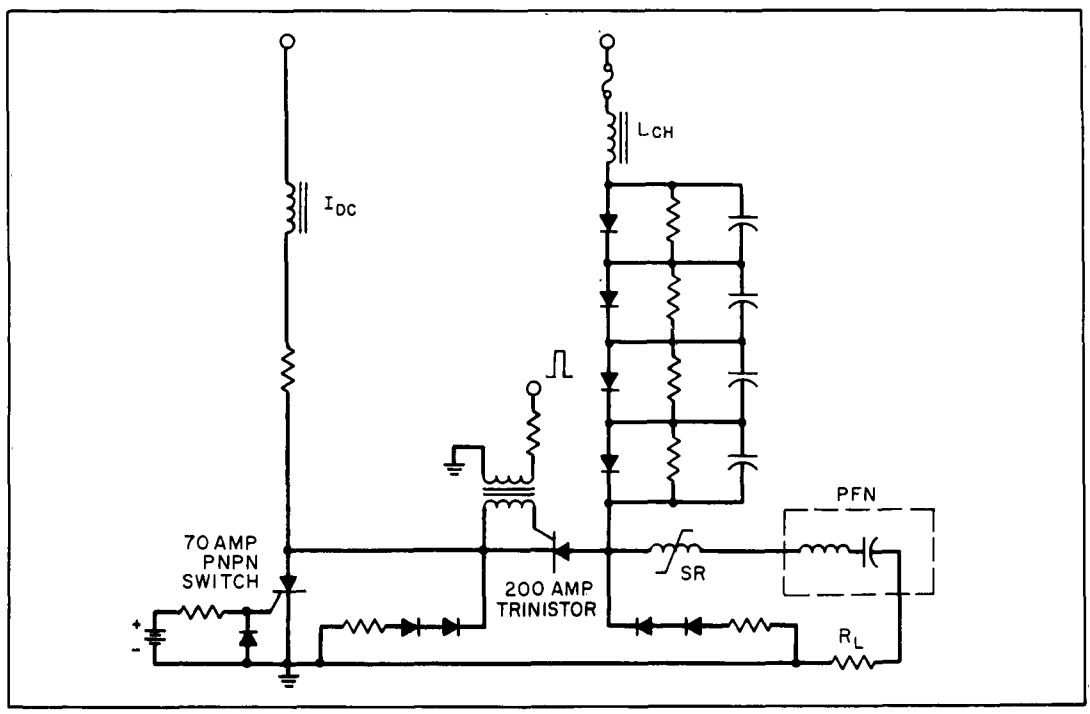


Figure 44. Forward Voltage Drop Versus Initial Anode Current Test Circuit

INITIAL ANODE CURRENT	70 AMPERE PNPN SWITCH FORWARD VOLTAGE DROP		
	UNIT #2	UNIT #4	UNIT #6
200 MA	11.0v	9.8v	10.5v
500 MA	10.0v	8.8v	9.5v
1 AMP	9.0v	8.5v	8.5v
1.5 AMPS	8.5v	8.2v	8.0v
2.0 AMPS	8.2v	8.0v	8.0v
3.0 AMPS	7.8v	7.8v	7.5v

Figure 45. Forward Voltage Drop Versus Initial Current

5. Conclusions

The forward voltage drop across the PNPN switch depends largely on the percentage of the junction which is conducting or "on". The forward voltage drop is lower with more of the junction conducting.

It takes a finite time, on the order of microseconds, for the "on" condition to spread across the junction. The rate at which this "on" condition spreads is dependent on many circuit conditions. The primary circuit condition appears to be the delay time between the anode switching and the peak current pulse. A larger percentage of the junction is conducting as the delay time is increased until the entire junction is "on". Increasing the gate drive, the initial anode current, and the gate pulse width (up to a certain point) also increases the spreading of the "on" condition.

The measurements show that to achieve reliable PNPN switch operation, the following circuit conditions are sufficient. The peak gate drive should be at least 300 milliamperes. The gate pulse width should be two microseconds or greater. The saturable reactor delay should be 20 microseconds or greater. The PNPN switch anode current prior to the output pulse should be greater than three amperes.

D. TRINISTOR EVALUATION

1. Short-Circuit Load Investigation

Magnetrons are known to occasionally arc from anode to cathode. This presents a virtual short-circuit load to the modulator. A practical modulator, therefore, must be capable of operating under such conditions without experiencing catastrophic failure. With this in mind, the Trinistors were tested for this type of over-load condition.

Figure 46 shows the equivalent circuit of the modulator when a pulse is being delivered into a short-circuit load. All circuit resistance has been assumed to be zero. This gives the maximum possible short-circuit current. Also, a single section equivalent PFN is used for simplicity.

The value of the discharge current, i, is:

$$i = V_o \sqrt{\frac{C}{L}} \sin \frac{t}{\sqrt{LC}} \tag{1}$$

The maximum current is therefore:

$$i_{max} = V_o \sqrt{\frac{C}{L}} \tag{2}$$

The values of L and C can be calculated from:

$$L = \frac{TZ_o}{2} \tag{3}$$

$$C = \frac{T}{2Z_o} \tag{4}$$

Where T = pulse width in microseconds

Z_o = PFN characteristic impedance in ohms

L = total PFN inductance in microhenries

C = total PFN capacitance in microfarads

For a 5.25-ohm PFN with a 5-microsecond pulse width:

$$L = \frac{(5)(5.25)}{2} = 13.1 \text{ microhenries}$$

$$C = \frac{5}{(2)(5.25)} = 0.476 \text{ microfarads}$$

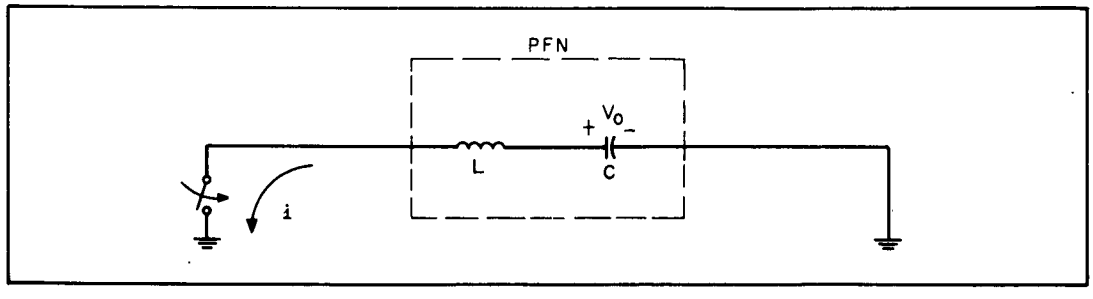


Figure 46. Modulator Equivalent Circuit with Short Circuit Load

Substituting the values for C and L into equation (2) shows the maximum discharge current to be 2200 amperes. A test chassis was built, therefore, to allow a Trinistor to pulse 2200 amperes.

Figure 47 shows the circuit used for this test. The PFN inductance, L, consisted of the saturated inductance of the saturable reactor. A relatively high value of capacitance was necessary for C so that a high peak current could be realized as given in equation (2) above. Two photo-flash capacitors, therefore, with an equivalent capacitance of 58.2 mfd were used for C.

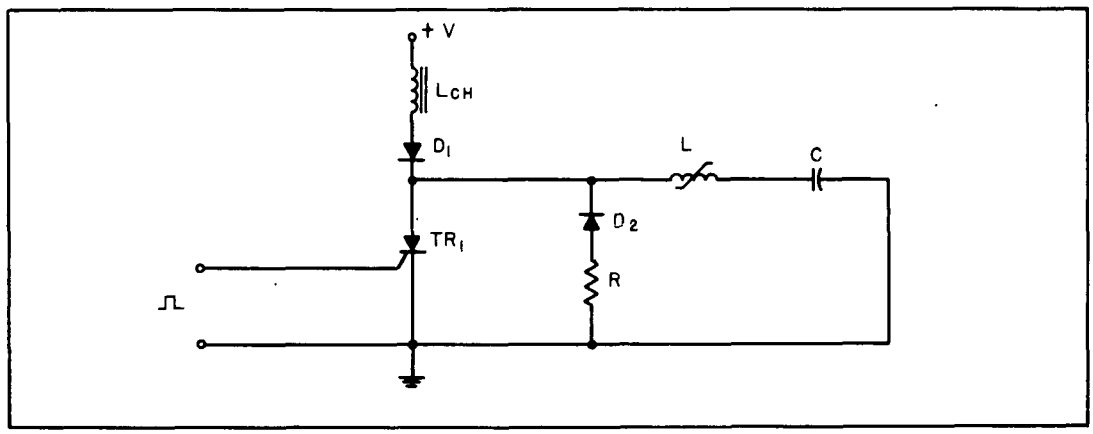


Figure 47. Short Circuit Load Test

Two Trinistors were tested in this circuit. They were initially operated at a relatively low voltage and current while observing the forward voltage drop from anode to cathode. The peak current was then gradually increased to 2200 amperes by increasing the supply voltage. The Trinistors were observed to perform satisfactorily and the peak current was then increased to 2900 amperes without any ill effects.

Figure 48 shows representative anode voltage and current waveforms and defines the symbols. The measured data at 2900 amperes is tabulated below.

Trinistor Sample Number	V_p Volts	I_p Amps	I_s Amps	V_{pf} Volts	t_d μsec	t_r μsec	P_W μsec	di/dt AMP/μsec
X1	400	2900	32	14	23	7	15	415
X2	400	2900	32	16	23	7	15	415

This pulse repetition rate was 10 pps in these measurements. The heating of the Trinistor was found to be barely detectable at this rate.

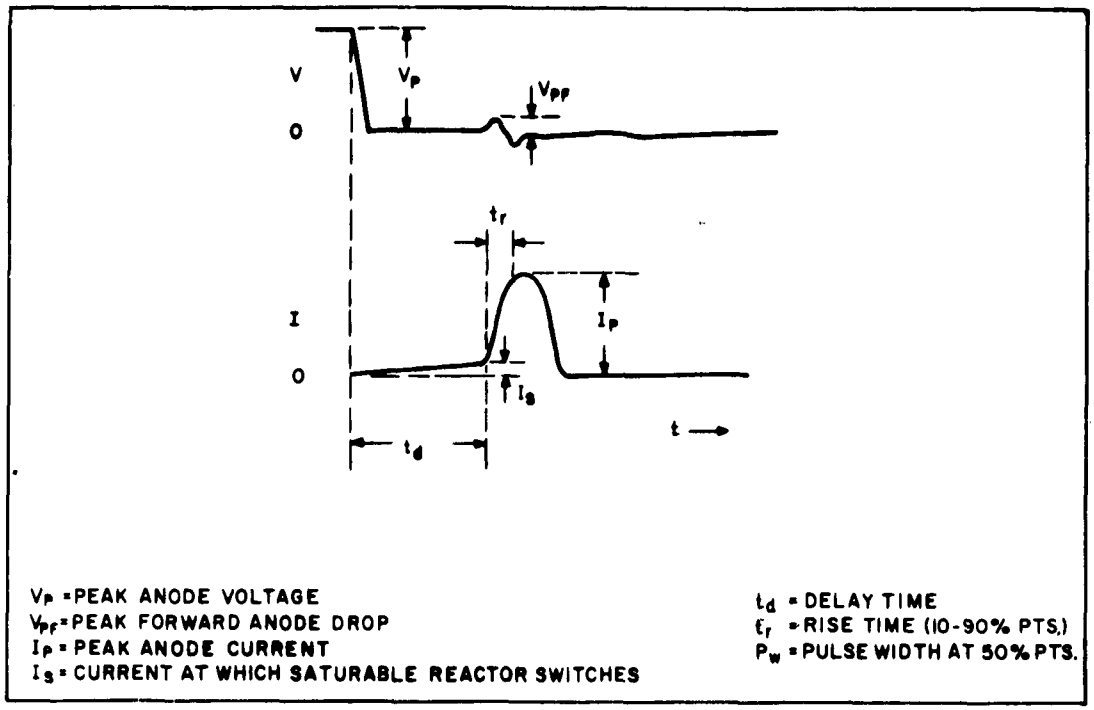


Figure 48. Trinistor Anode Waveforms

The short-circuit load test was also performed on two Trinistors connected in series. Figure 49 shows the diagram of the circuit. The same sample Trinistors (X_1 and X_2) were used. A lower inductance saturable reactor and a lower value of capacitance was used for the pulse-forming network to obtain a narrower pulse and faster rise time. The repetition rate was 10 pps. The measured data is as follows:
(Note: $V_{pf}X_1$ = forward voltage drop across X_1 and $V_{pf}X_2$ = forward voltage drop across X_2.)

V_p Volts	I_p Amps	I_s Amps	$V_{pf}X_1$ Volts	$V_{pf}X_2$ Volts	t_d μsec	t_r μsec	PW μsec	di/dt AMP/μsec
400	1450	34	15	23	24	3.1	6.5	467
600	2200	50	33	35	17	3.2	6.6	690

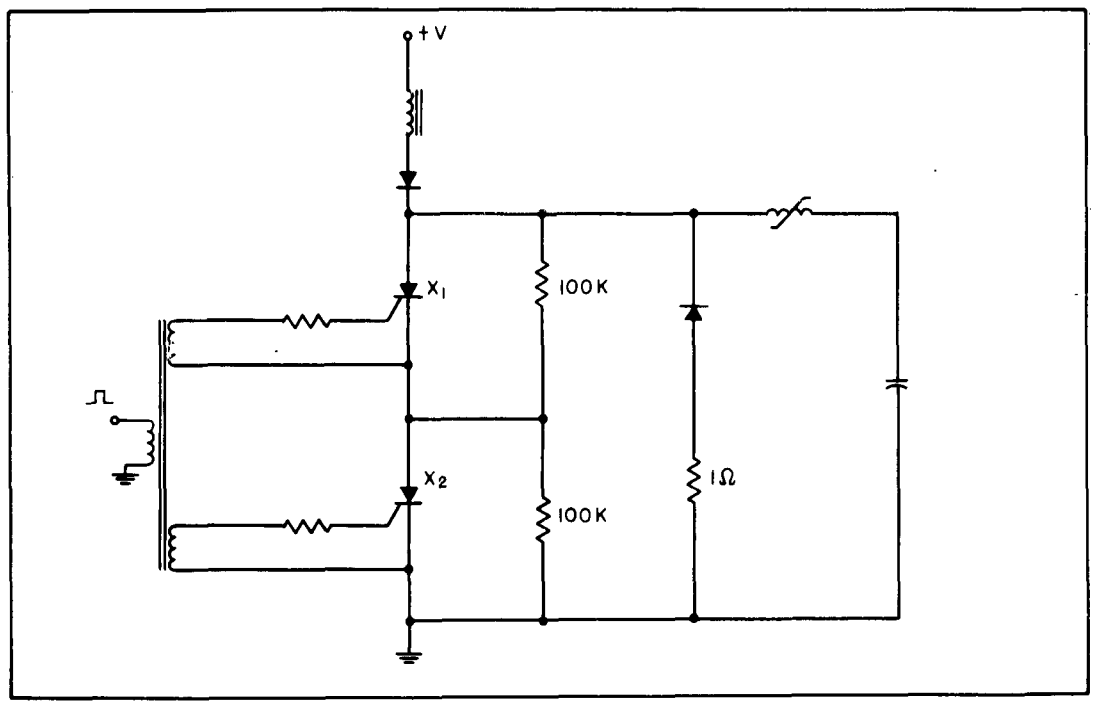


Figure 49. Series-Connected Switch

IV. FINAL BREADBOARD COMPONENT EVALUATION

A. PFN Evaluation

The pulse-forming network was tested at rated voltage and current in the circuit shown in figure 50. The PFN was charged through a resistor and a vacuum relay was used for the switching.

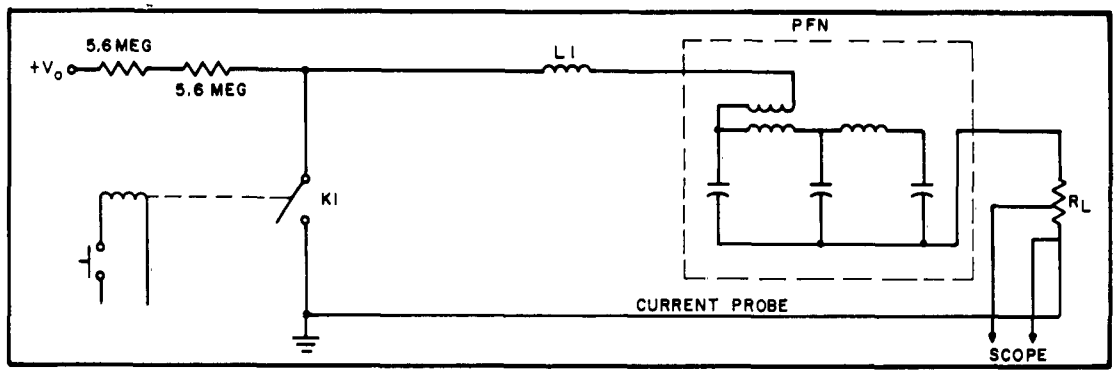


Figure 50. PFN Test Circuit

The PFN was supplied with the first inductor omitted to allow for circuit inductances. This test was conducted using three different values of external inductance: 2 microhenries, 4 microhenries, and 10 microhenries. Photographs of the output voltage across the load resistor for each of these external inductances are shown in figures 51 through 53. It can be seen that with external inductance as large as 4 microhenries, the output waveshape is still very acceptable. There is some degradation of pulse shape using a 10 microhenry external inductor.

$L_1 = 2\,\mu h$ $L_1 = 4\,\mu h$ $L_1 = 10\,\mu h$

5 μsec/cm

Figure 51 Figure 52 Figure 53

Voltage and Current Waveshapes

B. SATURABLE REACTOR EVALUATION

As in the case of the PFN, the saturable reactor was evaluated at rated voltage and current before installation in the breadboard modulator. The circuit used for this evaluation is shown in figure 54. The saturable reactor was tested in conjunction with the PFN to determine if any degradation of the PFN pulse occurred. The PFN was resistively charged and the switch used for discharge was a vacuum relay. The PFN was charged to 10 KV.

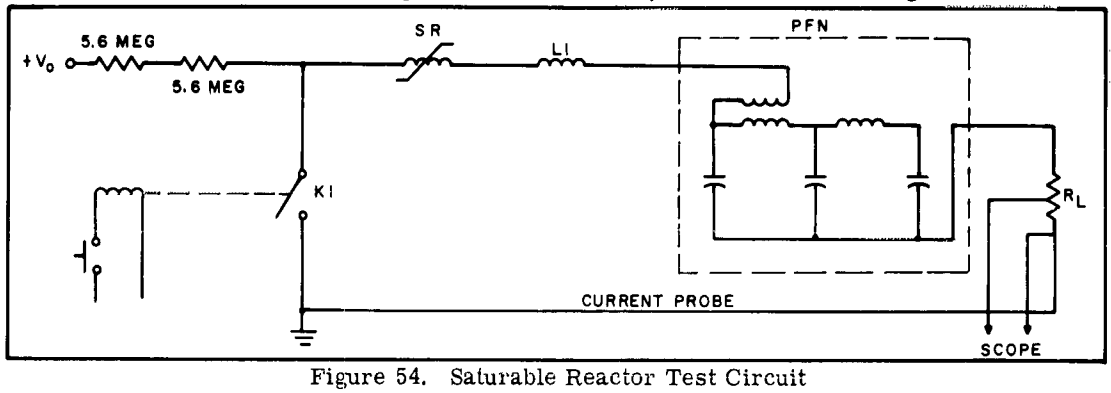


Figure 54. Saturable Reactor Test Circuit

Figure 55 shows the waveform across the load resistor using the saturable reactor and PFN. It can be seen that there is marked degradation of the pulse when using this particular saturable reactor.

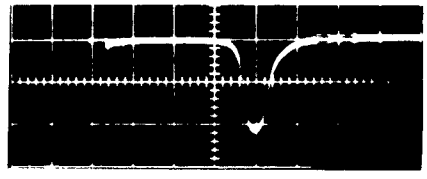


Figure 55. Waveform Across Load Resistor Using Saturable Reactor and PFN

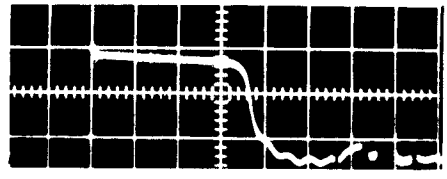


Figure 56. Voltage Waveform Across Saturable Reactor

The reason for the pulse degradation becomes apparent from the waveshape shown in figure 56. This waveshape is the voltage across a one-turn secondary winding through the saturable reactor. It shows the waveshape of the voltage across the reactor. It can be seen that there is voltage across the reactor for approximately 30 microseconds at which time it saturates and switches to a low impedance condition. The transition from high impedance to low impedance, however, takes three microseconds. This slow switching time degrades the net rise time of the pulse generated by the PFN.

This transition time can be significantly shortened by using a superior core material in the saturable reactor. By proper choice of reactor core material, the saturable reactor should introduce no appreciable degradation of the output pulse.

C. OUTPUT TRANSFORMER EVALUATION

The circuit used to evaluate the output transformer is shown in figure 57. The PFN was used in this circuit to simulate the actual pulse shape that was generated in the breadboard modulator. The PFN was resistively charged and a vacuum relay was used for the discharge.

The results of the evaluation of the output transformer were very satisfactory. No apparent degradation of the PFN pulse occurred by using the output transformer compared to directly discharging the PFN into a resistive load.

The output transformer was also tested using the saturable reactor and the PFN to shape the pulse. The results of this test can be seen in the output waveshape in figure 58. The slow rise time is a result of the saturable reactor and not the output transformer. It can be seen that there is no degradation of pulse shape contributed by the output transformer.

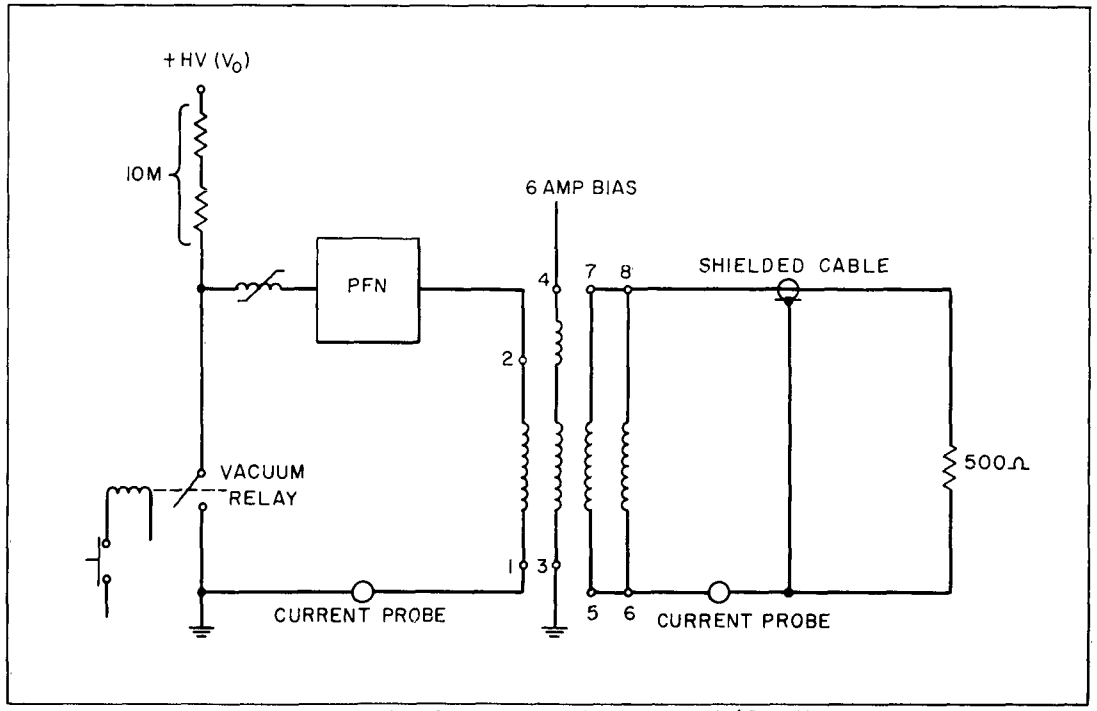


Figure 57. Output Transformer Test Circuit

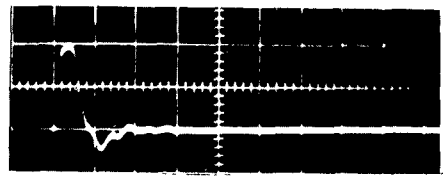


Figure 58. Output Voltage Waveshape

V. BREADBOARD TEST

Upon completion of wiring and construction, the breadboard modulator was operationally tested. The first tests consisted of operating the modulator at 1/3 input voltage. The DC voltage was 2 KV and the average current was 0.66 amperes, yielding an average input power of 1.32 KW.

The trigger and drive conditions are listed below:

Trigger input voltage:	15 volts peak
Trigger pulse width:	10 microseconds
Peak gate current per trinistor:	420 milliamperes
Pulse repetition rate:	300 pps.

With 2 KV DC voltage, the PFN charged to 4 KV.

The output conditions were as follows:	
Peak output transformer primary current:	195 amps.
Peak output transformer secondary current:	17 amps.
Current pulse width at primary of output transformer at 50% pts.:	7.0 microseconds.
Saturable Reactor Delay to 10% amplitude of pulse:	45 microseconds
Peak output power:	136 KW.

No unusual conditions appeared at this power level; therefore, the D.C. voltage was increased to 4 KV. The average current was 1.31 amperes for an input power of 5.24 KW. All trigger and drive conditions remained the same as when 2 KV DC voltage was applied. The output conditions were as follows:

Peak output transformer primary current:	680 amperes
Peak output transformer secondary current:	68 amperes
Current pulse width at primary of output transformer:	7.4 microseconds
Saturable reactor delay to 10% amplitude of pulse:	42 microseconds
Peak output power:	2.04 MW.

All tests at this power level were also satisfactory and the DC voltage was raised to 6 KV. Extensive testing of the modulator was performed at the full power level. The average current to the modulator was 1.87 amps for an average input power of 11.2 KW.

The following output conditions were recorded:

Voltage PFN charged to:	12 KV
Peak output transformer primary current:	1100 amperes
Peak output transformer secondary current:	105 amperes
Primary pulse width at 70% points:	5.2 microseconds
Saturable reactor delay to 10% amplitude of pulse:	30 microseconds
Primary pulse rise time, 10% to 90%:	3.0 microseconds
Primary pulse fall time, 90% to 10%:	6.0 microseconds
Peak voltage across dummy load:	55 KV
Peak output power:	5.8 Mw
Peak negative reflection:	1.3 KV
Saturable reactor switching time after delay, 10% to 90%:	3.5 microseconds

Figure 59 shows the voltage waveshape of the output pulse across the dummy load at full power. Figure 60 shows the current waveshape of the output pulse at full power. Note that there is good agreement in waveshape between the voltage pulse and current pulse.

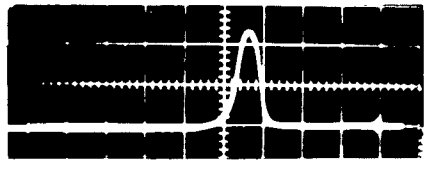


Figure 59. Voltage Waveform Across Dummy Load at Full Power

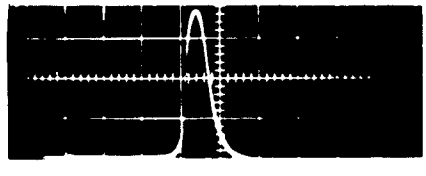


Figure 60. Output Current Waveform at Full Power

The charging waveform at the anode of the "highest" Trinistor is shown in figure 61. It can be seen that this voltage rises to very nearly twice the supply voltage of 6 KV. It can be seen that there is little droop in the peak charging voltage prior to turning on.

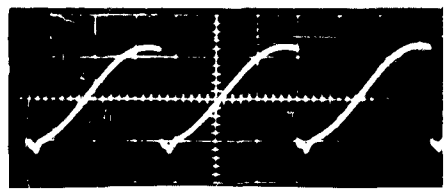


Figure 61. Charging Waveform

Figure 62 shows the Trinistor anode waveform and the primary current pulse waveform on the same scale. It can be seen that there is approximately 30 microseconds delay between the anode switching and the beginning of the current pulse.

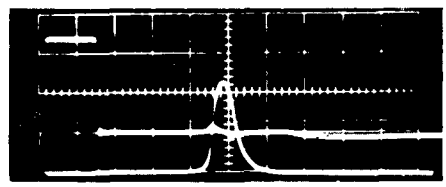


Figure 62. Trinistor Voltage and Current Waveforms

In order to show the delaying and switching action of the saturable reactor, a single turn loop was wound around the saturable reactor. A scope was connected to this single turn loop and the voltage waveshape is shown in figure 63. It can be seen from this photograph that the saturable reactor supports the 12 KV for nearly 30 microseconds after the Trinistors are turned on. Then the reactor core saturates and it switches to a low impedance state, allowing the PFN to discharge into the load. This figure shows the slow switching time of the saturable reactor. As mentioned earlier, this switching time could be significantly improved by the use of better core material in the saturable reactor. Such a core material might be Supermendur.

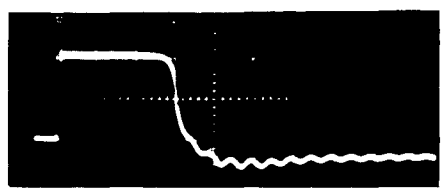


Figure 63. Voltage Across Single Turn Loop on Saturable Reactor at Full Power

The specified impedance of the PFN was 5 percent higher than the load impedance looking into the primary of the output transformer. This was done to insure that the Trinistor would turn off at the end of the pulse by developing the negative reflection across the Trinistors.

A photograph of the negative voltage reflection which is developed across the damping resistors is shown in figure 64. The peak amplitude of this reflection at full power level with 6 KV DC applied is 1.3 KV.

Figure 64. Voltage Reflection Across Damping Resistor

The voltage equalization across the Trinistors was checked with the modulator operating at full power. The equalization was determined by using a DC voltmeter connected across individual Trinistors in the series string. This method yields the average voltage appearing across each Trinistor rather than peak values but is satisfactory for determining voltage equalization. Figure 65 shows the average voltages measured across each Trinistor. It can be seen that the extremes are 290 volts and 350 volts. This is less than ±10% deviation from the center value of 320 volts.

Trinistor	Volts	Trinistor	Volts
1	320	11	340
2	340	12	335
3	290	13	310
4	305	14	340
5	330	15	350
6	338	16	280
7	338	17	350
8	343	18	318
9	295	19	350
10	323	20	345

Figure 65. Voltage Measurements Across Trinistors

An important aspect of the evaluation of the final breadboard modulator was to determine the power dissipation of the Trinistors. The power was determined by measuring the temperature rise of the exhausting air and the air flow. The set-up used for this measurement is shown in figure 66.

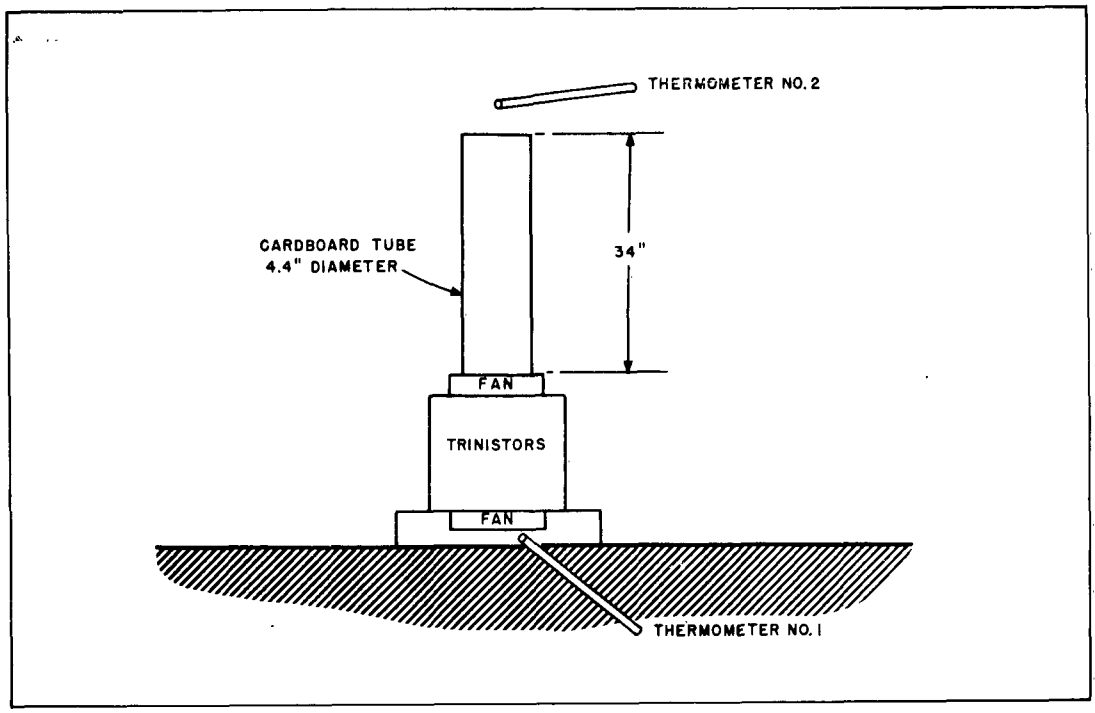


Figure 66. Power Dissipation Measurement Set Up

Using this method, the total power dissipated by the twenty Trinistors was calculated to be 171 watts. This reduces to an average power dissipation of 8. 5 watts per Trinistor. Both the power dissipated and the temperature rise appear to be far below the Trinistor maximum rating. Hence, little degradation in the life of the Trinistor is anticipated.

VI. JITTER AND DELAY

The function of the saturable reactor in the modulator is to delay the output current pulse until the Trinistors have had time to switch completely on. The delay time, t, introduced by the saturable reactor is given by:

$$t = \frac{NAB_t}{V_p}$$

where N = number of turns

A = cross-sectional area of core

B_t = total flux change

V_p = peak voltage applied to PFN.

It can be seen that the delay time is inversely proportional to the peak voltage applied to the PFN. The delay, therefore, will vary as the operating point of the modulator is varied. For example, if the present modulator is operated at half-power (0.707 V_p) the delay will increase from 30 μsec to 42.5 μsec. Also, any ripple in the power supply will cause small variations in delay. These small variations will result in jitter in the output pulse. The amount of jitter for any given amount of ripple, will be directly proportional to the nominal delay. For example, referring to the equation for delay above and assuming NAB_t to be constant, it can be seen that a 1% variation in voltage V_p will cause a 1% variation in delay time, t. If the nominal delay is 30 μsec the jitter will be 300 nanoseconds; whereas if the delay were only 10 μsec there would be only 100 nanoseconds of jitter.

One method of eliminating these effects would be to use a well-regulated, low-ripple power supply and to operate the modulator at a fixed power level. This solution, however, is cumbersome since it reduces the flexibility of the modulator and necessitates a much heavier and costlier power supply.

Another method of decreasing the jitter and variation in delay, due to power supply variations, is to use a compensating circuit for the trigger pulse. This circuit would consist of a variable delay circuit in series with the trigger pulse. The peak voltage on the PFN would be sampled and the trigger delay adjusted accordingly. For example, when the PFN voltage is high, the delay time of the trigger pulse would be increased. When the PFN voltage is low, the delay of the trigger would be decreased.

Circuitry of this type, for automatic compensation of jitter and delay, has been developed and used successfully by the Westinghouse Electronics Division in a magnetic modulator.[1]

Figure 67 shows a plot of percent peak-to-peak power supply ripple versus pulse-to-pulse time jitter for the magnetic modulator. It can be seen that when no compensation was used, for only 1% power supply ripple, the jitter was 170 nanoseconds. The corrective circuitry reduced this to approximately 10 nanoseconds.

In this same magnetic modulator, the pulse position would change 9 μsec from full-power to half-power when no corrective circuitry was used. The corrective circuitry reduced this change to 0.6 μsec.

The results of this work on jitter and delay compensation show that it is practical and with further development can be applied to the high power solid-state modulator.

Another method of compensating for the delay variations due to the saturable reactor would be by biasing the reactor. This would entail an additional winding on the saturable reactor and the delay would be varied by varying the current through this winding as shown in figure 30. The bias would be controlled automatically by circuitry that would sample the charge on the PFN and adjust the bias accordingly. As an alternative, this method could be combined with the gating delay method of compensation discussed earlier. The saturable reactor bias could be varied to compensate for large variations in delay, such as those resulting from operating at half-power while the gating delay circuitry would compensate for small variations as would result from power supply ripple and power line variations.

A third method of delay and jitter compensation involves the charging circuit. The charge on the PFN could be maintained constant by either regulating the "Q" of the charging choke or by diverting the energy from the choke. That is, the voltage to which the PFN is charged would be regulated by regulating the charging circuit. This could be accomplished by several methods. For example, the Q of the choke could be varied by shorting turns on it or inserting resistance. Alternatively, a portion of the energy in the choke could be diverted back into the power supply by using additional windings and switching circuits.

Any one of the above methods may be used to compensate for delay and jitter. It may be desirable, however, to use a combination of two or more methods to realize the best features of each method. For example, varying the delay in the gate pulse would be best for small variations, such as jitter, while varying the bias on the saturable reactor would be

1. Final Engineering Report for Research and Development of a Magnetic Modulator, Westinghouse Electric Corp., Electronics Division, for Navy Dept. Bureau of Ships Electronics Div., Contract No. NObsr-77638, Index No. NE-081500 ST/17.6(20). 12 Feb. 1962, pp. 41-52

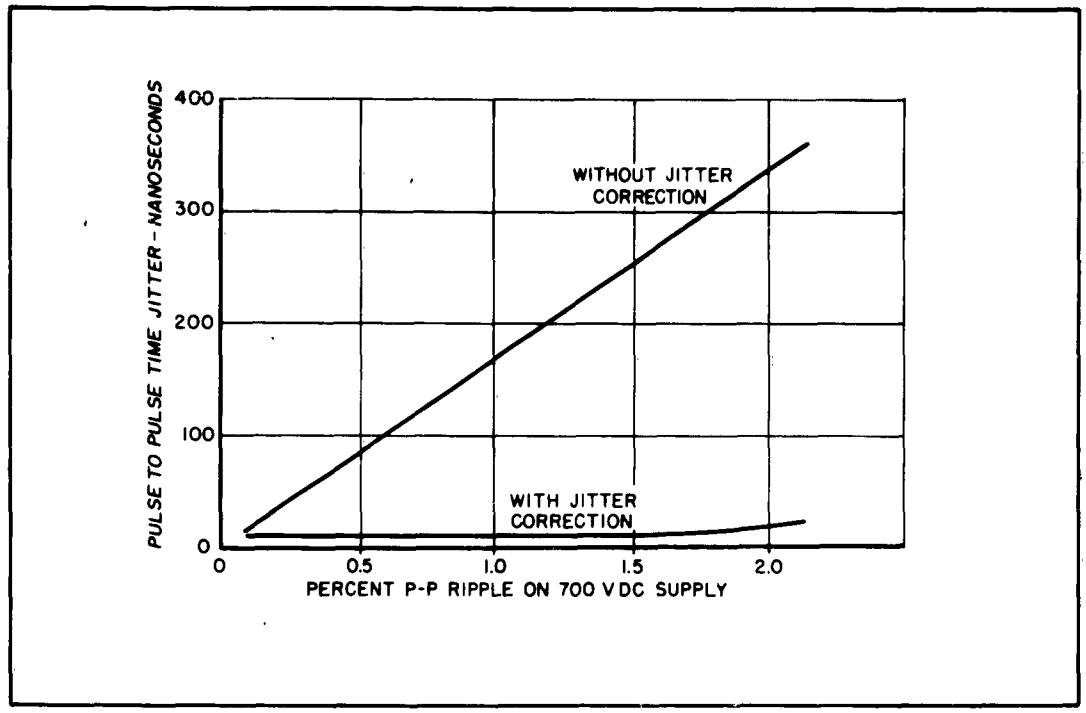


Figure 67. Power Supply Ripple vs. Jitter

best for compensating large delays. A combination of these two methods, therefore, should effectively compensate for all variables in pulse-to-pulse time intervals.

VII. INDUCTIVE COMPONENTS

Because of the experimental nature of the contract, little emphasis was placed on reduction of size and weight of the inductive components. The following sections describe how savings in size and weight could be achieved by using newer types of core material, insulation, and more sophisticated design procedures.

A. SATURABLE REACTOR DESIGN

Among the items discussed in Section II which could be improved is the saturable reactor which can be redesigned to reduce its size, weight, and power dissipation.

The original saturable reactor used in the high power, solid-state modulator was specified to provide 20 microseconds delay when blocking 12 KV. The actual delay turned out to be 30 microseconds. By having the saturable reactor designed by Westinghouse and using the same core material (hipersil) as in the present reactor, but providing 20 microseconds delay rather than 30, the weight can be reduced by 35 percent. By using Supermendur for the core material, the saturable reactor weight can be reduced by 50 percent.

By using improved PNPN switches which will require less current delay (on the order of 10 microseconds) even greater weight savings can be accomplished. Using the same core material, hipersil, the reactor weight will then be 33 percent and by using Supermendur it will be less than 25 percent of the original reactor weight.

Tabel A summarizes the dimensional benefits of redesigning the saturable reactor.

TABLE A

	Present Reactor	Proposed Alternative Reactors			
Delay (μsec)	30	20		10	
Core Material	Hipersil	Hipersil	Supermendur	Hipersil	Supermendur
Diameter (0 D inches)	20	17.5	16	14	12.7
Height (inches)	4	3.5	3.2	2.8	2.5
Weight (pounds)	106	71	53	35	26

There are other reasons for redesign of the saturable reactor besides size and weight reduction. The use of Supermendur for the core material will provide a saturable reactor with a much faster switching time than hipersil. The faster switching time will improve the output pulse shape, providing a more rectangular pulse.

Hipernik V core material would also improve the switching time of the saturable reactor and decrease the size and weight. The improvement in weight reduction derived from Hipernik V core material is not as substantial as that obtained by using Supermendur. Hipernik V however, is less expensive.

B. CHARGING CHOKE AND PULSE TRANSFORMER

By using a new and improved high-temperature wire and insulation, the weight of the present charging choke can be reduced by 25 percent. It can be made smaller by allowing the choke to run at a higher temperature. For example, the maximum operating temperature for the present Class S insulation in this choke is 130°C, whereas the maximum operating temperature for the new materials is 220°C. The new insulation is the result of advanced polymer chemistry at the Westinghouse Research Labs. Although operating temperatures of 220°C have been achieved previously with silicones, the coils were mechanically weak, and were often not reliable because of poor adhesion of silicone enamel to the wire. The new resins are mechanically strong, and are available in the form of solventless varnish, enamel, or paper, and offer the advantage of multiple coil winding with attendant low cost. The new choke would still require a blower. As an alternative, the blower could be eliminated by building a choke similar in size and weight to the present one but using the high temperature insulation. The reduction in weight is greater, however, by reducing the choke size rather than by eliminating the blower. A weight comparison is given in Table B.

TABLE B

	Present Design	Proposed High Temperature Design	
		With Blower	Without Blower
Charging Choke Weight (incl. Blower)	53.6	40 lb.	50 lb.

The present pulse transformer used on the high-power solid-state modulator is considerably smaller than existing pulse transformers. The size and weight of the pulse transformer can be even further reduced, however, by the use of Supermendur for the core material. This should result in a core weight saving of approximately 46%. The smaller core will, in turn, enable a reduction in overall size and a 25% reduction in total weight of the transformer.

In addition to a reduction in size and weight made possible by using Supermendur core material, there should be an improvement in the efficiency of the pulse transformer. With less power dissipation in the pulse transformer, it will run cooler and therefore the overall size can be further reduced.

VIII. CONCLUSIONS

A breadboard modulator delivering 5Mw peak power, operating at 300 pps and pulse width of approximately 5 μsec has been built and tested. The breadboard switching element consists of 20 Trinistor-controlled rectifiers. The breadboard also includes circuitry which will protect the modulator in case of load shorts and detect failure of any one of the Trinistor switches.

In summation, this program has shown that high-power, solid-state radar modulators are both feasible and practical. This has been brought about by developing techniques of (1) seriesing Trinistors and (2) the efficient and reliable utilization of the high current pulse capability of the Trinistor.

It is, therefore, recommended that a program be initiated to test a solid-state radar modulator operating into a live magnetron load.

In addition, it is recommended that a program be initiated to ascertain the reliability of the solid-state modulator. This data can then be compared with reliability data of an existing conventional (tube) modulator design having comparable output characteristics.

APPENDIX

OPERATION AND INSTALLATION INSTRUCTIONS
Solid State Radar Modulator Breadboard

The procedures for turning on and operating the Solid State Radar Modulator Breadboard have been established to provide maximum safety to both the operator and the equipment. It is important that these procedures be followed exactly as listed below.

The procedures have been broken into two groups, namely, installation and interconnection, and operation. DO NOT ATTEMPT TO TURN ON ANY VOLTAGES UNTIL THE COMPLETE INSTALLATION AND INTERCONNECTION PROCEDURE HAS BEEN FOLLOWED!

A. INSTALLATION AND INTERCONNECTION

The breadboard consists of three main units, the modulator cabinet, the power supply cabinet, and the dummy load resistor cabinet. These three units should be interconnected as follows:

1. Remove the right side panel of the modulator chassis.
2. Insert the unshielded high-voltage cable and the separate ground cable through the grommet in the right side panel.
3. Loosely fasten the unshielded high-voltage cable to the clamp in the modulator chassis which is mounted on the auxiliary circuitry chassis.
4. Connect the high-voltage cable to terminal seven of the output transformer.
5. Tighten the high-voltage cable clamp.
6. Connect the separate ground lead which was passed through the side panel grommet to terminal five on the output transformer.
7. Clamp the separate ground lead with an insulated cable clamp to the rear screw holding the high-voltage cable clamp. This should be the screw nearest to the side panel.
8. Connect the ground braid to the ground terminal in the modulator chassis. This terminal is located at the right rear of the modulator chassis. The ground braid exits the modulator between the right side panel and the chassis itself.
9. Fasten the right side panel to the modulator cabinet.
10. Remove the dummy load cabinet side panel.
11. Pass the high voltage cable from the modulator cabinet through the two large cable clamps mounted on bottom panel of the dummy load cabinet. Connect the high-voltage cable to screw A on the upper right hand side of the load resistors.

12. Pass the separate ground cable (insulated) through the small cable clamp mounted on the bottom panel of the dummy load cabinet, and through the center hole of the current probe. Connect this cable to screw B at the lower left corner of the load resistor.

13. Connect the ground braid from the modulator cabinet to the ground screw mounted on the bottom panel of the dummy load cabinet.

14. Fasten the side panel to the dummy load cabinet.

15. Plug one end of the four-wire cable into the socket at the side of the dummy load cabinet. Plug the other end of this cable to the socket at the rear of the modulator cabinet.

16. Connect the eight-wire power supply cable into the plug at the rear of the modulator cabinet.

17. Connect the large white wire (High Voltage Lead) from the power supply cable through the grommet at the rear of the modulator chassis.

18. Insert the small white wire and small black wire from the power supply cable through the grommet on the rear of the modulator cabinet. Connect both of these wires to the ground terminal located inside just beyond the grommet.

19. Connect the four-wire power supply input cable to a three-phase, 208-volt, 60-cps, four-wire line. The wire marked N should connect to the neutral. The other three wires connect to the three phases of the line. The phase of these three wires is not important.

This completes the installation and interconnections.

B. OPERATION INSTRUCTIONS

To operate this equipment, it is necessary that all removable panels be fastened to the modulator cabinet and to the dummy load cabinet. The rear door of the power supply cabinet must be closed. Each of these are interlocked and the equipment cannot be turned on unless these interlocks are closed. All cables must also be connected to allow the equipment to be turned on.

1. Connect a pulse generator to the trigger input connector on the front of the modulator cabinet. This generator should provide a 10-microsecond POSITIVE pulse with a rise-time of 1 microsecond or better. The peak pulse amplitude should be 15 to 25 volts and the repetition rate of the generator should be 300 pps.

2. Switch the over-voltage detector switch on the modulator cabinet to the "off" position.

3. Turn the output voltage control on the power supply fully counterclockwise to the zero position. The high voltage cannot be turned on unless this control is set at zero.

4. Turn on the primary power switch located at the bottom of the power supply front panel. The green lamps on both the power supply and the modulator panel should light.

5. After approximately one minute, the yellow "ready" light on the power supply should come on. This light will not come on if any of the interlocks are open.

6. Press the black start button. The red light on both the power supply and the modulator should come on.

7. Advance the output voltage control to 2 KV as indicated on the panel-mounted voltmeter. The yellow light on the power supply will go out when the voltage control is advanced.

8. Switch the over-voltage detector switch on the modulator to the "on" position.

9. Advance the output voltage control to 6 KV for full power operation. The output current should be approximately 1.87 amperes.
   DO NOT EXCEED 6.5 KV DC FOR NORMAL OPERATION.

10. To turn off the high voltage, press the red stop switch or reduce the output voltage control to zero.

11. If the high voltage has been turned off by pressing the stop switch, the output voltage control must be returned to zero to be able to again turn on the high voltage.

12. The over-voltage detector must be turned off when the HV is reduced to zero. The over-voltage detector should again be turned on when the high voltage is advanced to 2 KV.