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SCIENTIFIC AND TECHNICAL INFORMATION

CAMERON STATION, ALEXANDRIA, VIRGINIA

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RADIO CORPORATION OF AMERICA

TRANSISTOR, VHF SILICON POWER (5W)
REPORT NO. 2
CONTRACT NO. DA-36-039-SC-90797
TECHNICAL REQUIREMENT NO. SCL-2101N
14 JULY 1961
DA PROJECT NO. 3A99-21-002
SECOND QUARTERLY PROGRESS REPORT
1 OCTOBER 1962 to 31 DECEMBER 1962
For
U.S. ARMY SIGNAL RESEARCH AND
DEVELOPMENT LABORATORIES
FORT MONMOUTH, NEW JERSEY
From
RADIO CORPORATION OF AMERICA
SEMICONDUCTOR AND MATERIALS DIVISION
Somerville, New Jersey

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I. PURPOSE

The purpose of this contract is to design and develop a 5 watt, 500 megacycle silicon transistor having minimums of 50% efficiency and 10 db power gain. The device will be constructed in accordance with Signal Corps Technical Requirements NO. SCL-7002/11 dated 23 August 1961. These requirements are summarized below.

MAXIMUM RATING AT 25°C

BV_{CEO}	75 Vdc
BV_{EBO}	5 Vdc
P_c	12 watts at 25°C case temp.
I_c	1.0 Adc
T_j	200°C
T_{stg}	-65°C to + 200°C

GROUP A INSPECTION

Examination or Test	Conditions	Symbol	Min.	Max.	Units
Collector Cutoff Current	V_{CE} = 75 Vdc I_B = 0	I_{CEO}	-	100	μa
Collector Cutoff Current	V_{CE} = 28 Vdc V_{EB} = 0	I_{CES}	-	1	μa
Collector Cutoff Current	V_{CE} = 75 Vdc V_{EB} = 0	I_{CES}	-	100	μa
Emitter Cutoff Current	V_{EB} = 5 Vdc I_C = 0	I_{EBO}	-	100	μa

Examination or Test	Conditions	Symbol	Min	Max	Units
Static Forward Current	V_{CE} = 28 Vdc	h_{FE}	20	60	-
Transfer Ratio	I_C = 357 mAdc				
Base Spreading Resistance	V_{CE} = 28 Vdc	rb'	-	10	ohm
	I_C = 357 mAdc				
Output Capacitance	V_{CB} = 28 Vdc	Cob	-	5	μμf
	I_E = 0				
Small Signal Short Circuit	V_{CE} = 28 Vdc	h_{FE}	12		
Forward Current Transfer Ratio	I_C = 357 mAdc				
	f = 500 mc				
Power Gain	V_{CE} = 28 Vdc	P.G.	10	-	db
	I_C = 357 mAdc				
	f = 500 mc				
	P_i = 0.5 watts				
	$T_c < 55°C$				
Oscillator Output	V_{CE} = 28 Vdc				
	I_C = 357 mAdc	P.O.	5	-	watt
	F = 500 mc				

In addition to the above, a Group B inspection which includes temperature cycling, moisture resistance, shock, vibration, and acceleration tests will be performed. A thermal resistance (θ J-C) requirement of 14.6°C/watt will be met and storage life tests for 1000 hours at 200°C with specified end points will be performed.

II. ABSTRACT

The majority of effort, during this quarter, has been concentrated on experimental studies of the proposed techniques which will be required to produce this device.

The resistivities and diffusion parameters of this device have been determined and have been successfully employed in the diffusion cycles.

Photoresist techniques have been developed which allow excellent definition and registration of the required photoresist patterns in the silicon dioxide, however, improvement is still required in the defining and etching of the aluminum.

In the fabrication of the insulating layer, the main difficulty is one of opening the emitter oxide area after anodizing or silicon monoxide evaporation. The difficulty is inadequate adherence of the defined photoresist to the substrate resulting in lifting during immersion of the wafer in oxide etch. Devices with only a few percent of the emitter areas opened have been fabricated and display excellent diode characteristics. These results indicate the feasibility of the anodized aluminum approach to the fabrication of an overlay structure.

Alternate approaches for producing the insulating layer are being considered. These include metal mask evaporation of a dielectric material only over the base metalling and the use of a second thin metal film over the anodized film, which can be defined and will act as a mask for defining the silicon dioxide.

III. PUBLICATIONS, REPORTS AND CONFERENCES

On 28 November 1962 a conference was held at Radio Corporation of America, Semiconductor and Materials Division, Somerville, New Jersey between representatives of the United States Signal Supply Agency and Radio Corporation of America. The conference discussion included the overlay structure, high frequency measurements on units, and case type required for this unit.

IV. FACTUAL DATA

A. Introduction

Previously, major effort was expended on the development of high power, high frequency devices employing the interdigitated or comb type structure. This structure is composed of a series of emitter stripes connected to a common terminal separated by base stripes attached to a second terminal as shown in Figure (1).

The interdigitated structure is hindered by fabrication technique limitations that make its application marginal at the power output and frequencies required by this contract. Included in these limitations are the attainable ratio of metal thickness to finger width, the ratio of emitter periphery to emitter area, and the inductance associated with the bonding wires and narrow metallized fingers.

B. Overlay Structure

All three of the previously mentioned limitations on the comb type geometry can be overcome by the use of an overlay structure. The outstanding feature of this structure is the concept of complete emitter metallizing over both the base metallizing and the emitter contact areas. See Figure (2) for an example of the overlay structure.

In this structure, the base metallizing grid is defined using photoresist techniques. This is followed by the deposition or formation of an insulating film over the metallized base metal grid. The emitter contact area can then be made as narrow as photoresist and etching techniques permit (0.2 to 0.3 mil). A second metal film is then deposited over the entire wafer and defined over the area containing the emitter and base.

It can be seen that this structure will result in a slight increase in emitter-base capacitance due to the capacitor like construction. However,

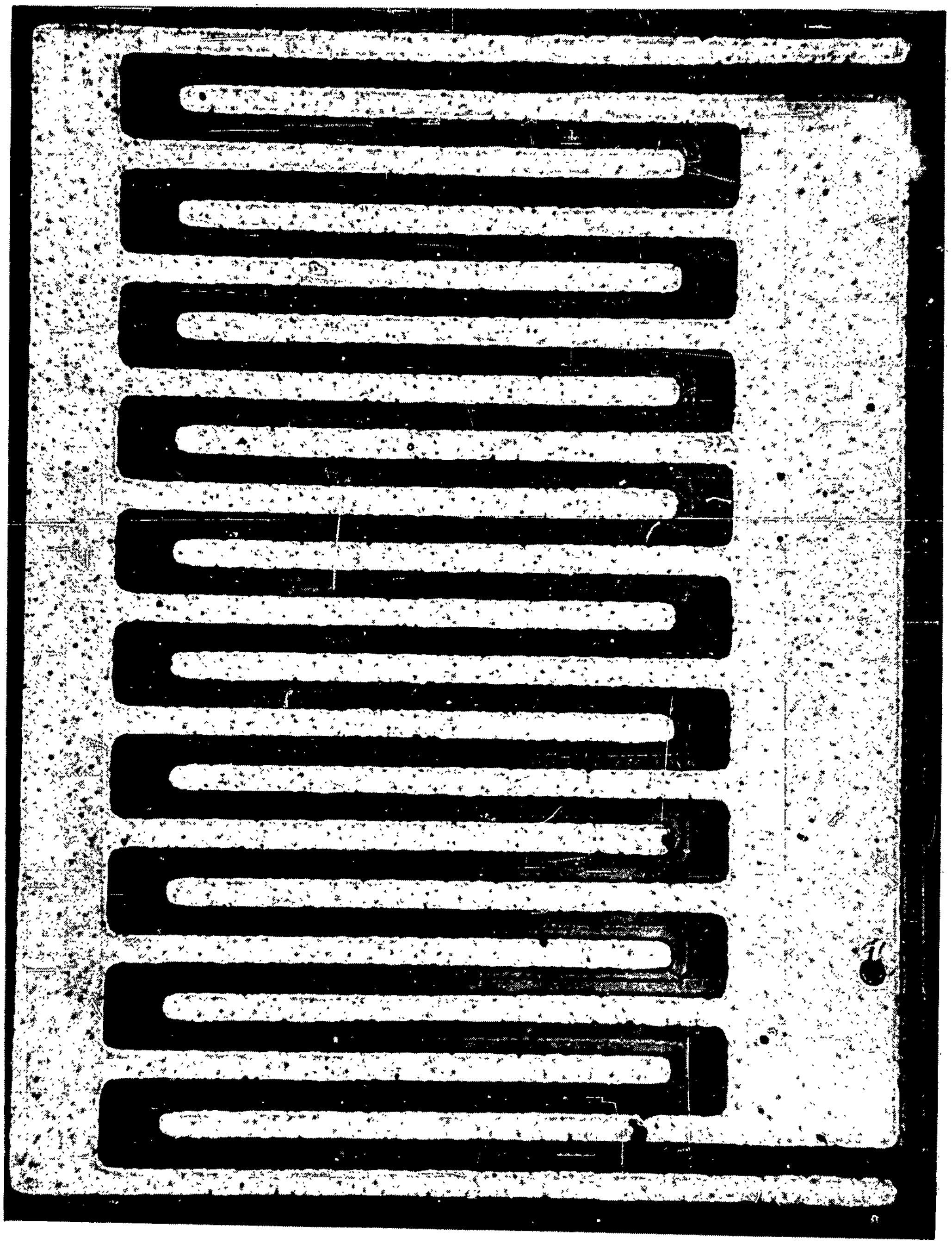


FIGURE 1 INTERDIGITATED (COMB) STRUCTURE WITH INTERLEAVED BASE AND EMITTER FINGERS

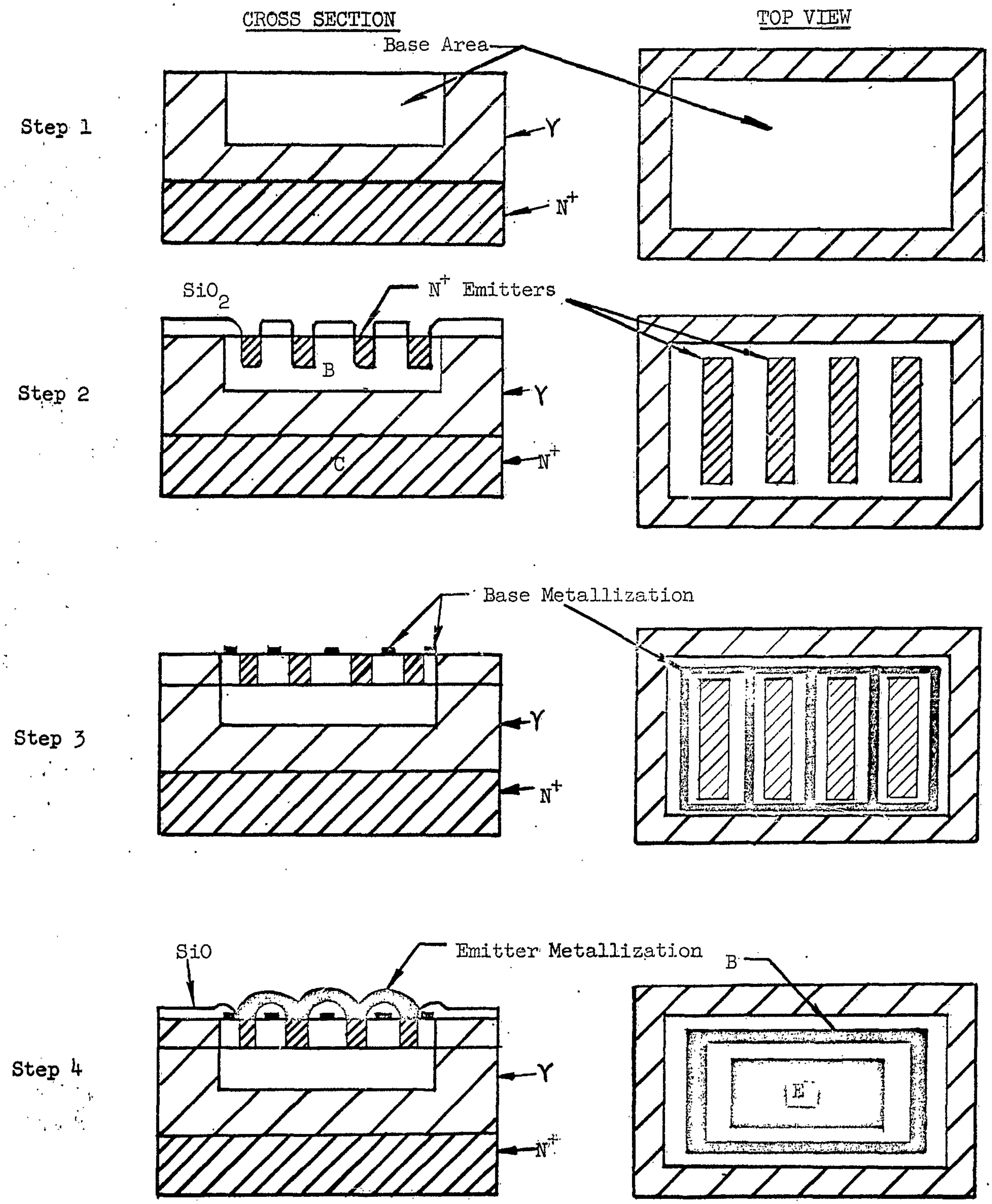


FIGURE 2 EXAMPLE OF OVERLAY APPROACH

since the input resistance to the device is extremely low, the additional input capacitance will not be a problem.

C. Frequency Considerations

In order to obtain the required power gain of 10 db at 500 megacycles, a gain-band figure of merit (K) of approximately 1.6 kmc is necessary. This gain-band figure of merit indicates a maximum total transit time of 2.5×10^{-10} seconds in the device.

To achieve the specified current gain of 12 db, a total transit time of 8×10^{-11} seconds is required which is shorter than the value calculated from the power gain. Hence, the required current gain will be more difficult to attain than the power gain.

Calculations performed using both 20 ohm-centimeter and 6 ohm-centimeter material show the advantage of using the lower resistivity material. As indicated in Table I although the 6 ohm-centimeter material has a higher capacitance, the total transit time is considerably lower than that attainable with 20 ohm-centimeter material.

DEVICE PARAMETER	RESISTIVITY OF STARTING MATERIAL	
	Six Ohm-Centimeter	Twenty Ohm-Centimeter
Collector Depletion Region Transit Time (τ_m)	43×10^{-12} sec.	81×10^{-12} sec.
Base Transit Time(τ_b)	13.9×10^{-12} sec.	7.3×10^{-12} sec.
Sum of τ_m plus τ_b	56.9×10^{-12} sec.	88.3×10^{-12} sec.
Output Capacitance, Common Base Configuration	3.4 picofarads	2.3 picofarads
Emitter Transit Time (τ_e)	4×10^{-12} sec.	4×10^{-12} sec.
Emitter to Collector Transit Time (τ_{ec})	6.0×10^{-11}	9.2×10^{-11} sec.

TABLE I

COMPARISON OF SIX OHM-CENTIMETER AND TWENTY OHM-CENTIMETER MATERIAL FOR THE MORE IMPORTANT PROPOSED DEVICE PARAMETERS AT 30 VOLTS

D. Progress Development

(1) General

The 5 watt, 500 megacycle device will be a triple diffused, NPN, planar transistor. The emitter will be in the form of very small squares or circles arranged in a regular array. The base metallizing will be a matrix of conductors crossing at right angles entirely surrounding the emitter areas. The insulating material used to cover the base metallizing will be either an evaporated silicon monoxide film, an anodically formed Al_2O_3 film or a combination of the two. The dimensions of the device geometry and a comparison of these dimensions to a 3 watt, 200 mc comb type device is shown below.

	Overlay Structure 5w, 500mc	Comb Structure 3w, 200 mc
Total Base Area (BA)	380 square mils	1726 square mils
Emitter Area (EA)	68 square mils	657 square mils
Emitter Periphery (EP)	412 mils	438 mils
Pellet Size	70 x 70 mils	55 x 58 mils
EP/EA	6.05	0.668
EP/BA	1.08	0.255

The ratios EP/EA and EP/BA indicate the relative emitter periphery attainable in a given area. It is apparant that a significant improvement is obtained using the overlay geometry.

(2) Diffusion

The resistivities and diffusion parameters of the device, based on the required transit times and breakdown voltages are stated below:

$X_e = 2 \times 10^{-14}$ cm (0.078 mils)

C_o (emitter $= 3 \times 10^{21}$ atoms/cm^3

$X_b = 2.8 \times 10^{-4}$ cm (0.11 mils)

C_o (Base)= 5×10^{19} atoms/cm^3

$W = 8.38 \times 10^{-5}$ cm (0.033 mils)

Starting material 6 ohm-cm (7.8×10^{14} atoms/cm^3)

Width of starting material in collector body = 1.15×10^{-3} cm (0.45 mils)

C_o (collector contact) = 3×10^{21} atoms/cm^3

$X_{cc} = 1.14 \times 10^{-2}$ cm (4.5 mils)

Diffusion runs having the required surface concentration and diffusion depths have been fabricated.

Experiments on the use of a high doped P layer in the base contact region have been initiated. It is felt that this additional step in the diffusion cycle will result in a decrease in rbb' without adversely affecting the device breakdown characteristics.

(3) Photoresist Techniques

The necessary photoresist masks for the fabrication of this device have been processed and are satisfactory. Because of the very narrow line width and small emitter geometry of this unit, particular attention was devoted to the edge definition, corner radii, emulsion free clear areas and the opaqueness of the emulsion areas.

The extremely small dimensions of this unit also imposed serious limitations on the alignment fixtures and necessitated the redesign of these fixtures so that the wafer position, relative to the mask, could be controlled to within 0.1 mil.

Experiments in the defining of patterns indicated the necessity of a new whirling procedure for the application of the photoresist coating. Using normal whirling techniques, a formation of photoresist, approximately 0.1 mil high, could be seen around the periphery of the coated wafers. This lip of material prevented close contact between the photoresist mask and the coated wafer during exposure. This resulted in a decrease in pattern definition and at times totally inadequate definition as shown in Figure (3). (the difference in definition between wafers with and without this formation).

The procedure for the application of photoresist has been modified and the problem has been eliminated.

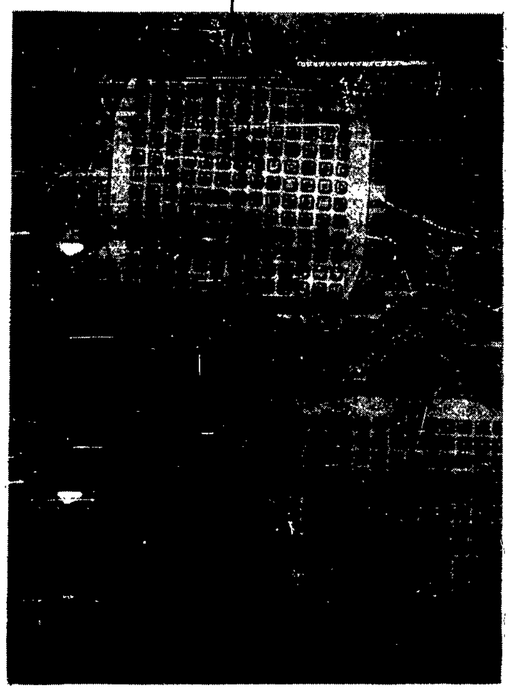
Investigations of photoresist coating techniques, exposure time and developing techniques have resulted in procedures which allow very satisfactory pattern definition.

The degree of pattern sharpness can be seen in Figures (4), (5), and (6). Figure (4) shows a section of the emitter diffusion array, each square being 0.5 mil on a side. Figure (5) shows the defined and etched reverse oxide pattern used to open the silicon dioxide in the emitter and base region prior to metallizing. In this pattern, both the emitter squares and the base matrix are 0.3 mil in width.

In Figure (6), the definition obtained in defining the emitter base metallizing is shown. The metal is approximately 15,000 Å thick and the squares and matrix 0.3 mil in width.

The various registered photoresist pattern prior to metalizing is shown in Figure (7a). In this figure, the outer periphery defines the base area, the darker squares the emitter area, and the small inner squares and matrix the reverse oxide pattern. Figure (7b) shows the unit after definition of 15,000 Å of aluminum in the emitter and base contact areas. Improvements are still needed at this time in the definition and etching of the aluminum film since any imperfection in this will

Pileup of photoresist at edge of wafer. (Note rounded corners of array, loss of definition and presence of completely or partially closed emitter areas).



No pileup at edge of wafer

FIGURE 3 EFFECT OF RIDGE OR PILEUP OF PHOTORESIST AT EDGE OF WAFER ON PATTERN DEFINITION

Magnification 200x

Magnification 400x

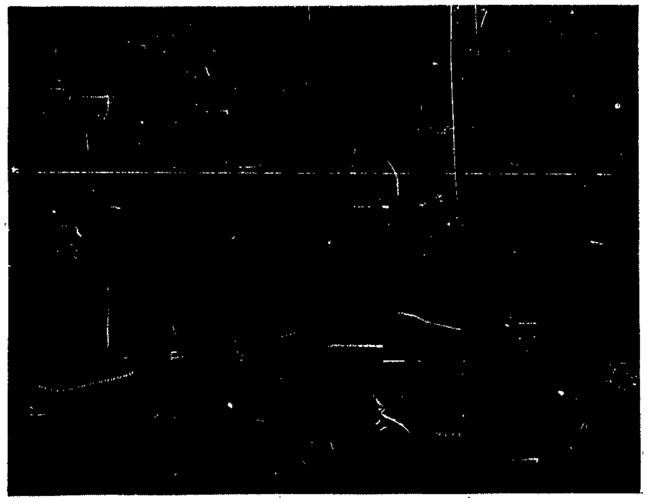
FIGURE 4 EMITTER DIFFUSION ARRAY

Magnification 100x

Magnification 200x

Magnification 400x

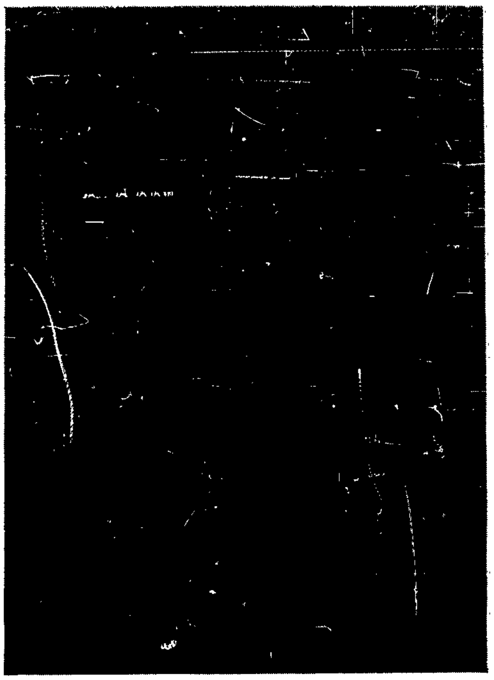
FIGURE 5 ETCHED EMITTER-BASE REVERSE OXIDE PATTERN



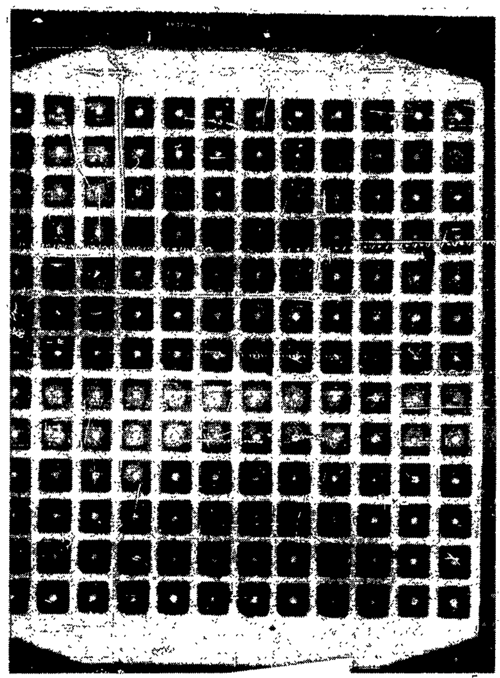
Magnification 200x

Magnification 400x

FIGURE 6 ETCHED EMITTER-BASE METALLIZING PATTERN



a. Pattern Prior To Metallizing



b. Defined Emitter-Base Metallizing Pattern

FIGURE 7 REGISTERED PHOTORESIST PATTERNS-PRIOR TO METALLIZING AND INCLUDING DEFINED EMITTER - BASE METALLIZING result in a short circuit between emitter and base using the anodizing approach to the overlay.

(4) Metallizing

As discussed in Quarterly Report No. 1, calculation of the bias voltage caused by IR drops along the base metallizing matrix indicate that this bias is negligible for films of approximately 15,000 Å. Present metallizing techniques are applicable to the new device geometry and no refinement in this process appears to be necessary.

(5) Insulating Layer

The insulating film over the base metallizing must be free of pinholes, adhere strongly to the substrate, offer very low leakage and be capable of being placed, formed or defined in particular areas.

Initial studies on evaporated silicon monoxide films show that these properties are largely dependent on the evaporation techniques. Further studies indicate difficulty in etching these films in reasonable lengths of time.

In these studies silicon monoxide was deposited over the entire wafer, after the base metallizing had been completed. Photoresist techniques were employed in an attempt to define this insulating material so that the emitter contact areas were free of silicon monoxide while the metallized base matrix retained the monoxide film. All attempts to fabricate a device using this procedure resulted in failure due to an inability to etch out the emitter contact areas. The failure mechanism consisted of a lifting of the photoresist in 1 to 2 minutes in ammondium biflouride etch, a failure of the photoresist to mask at the aluminum, silicon dioxide, silicon monoxide interface or a combination of these two mechanisms. Various substrate cleanup procedures, evaporation conditions and photoresist techniques were employed in unsuccessful attempts to eliminate this condition.

A second approach to the insertion of an insulating layer between the base metallizing and emitter metallizing, is the anodic formation of Al_2O_3 on the aluminum base matrix. This anodized film possesses all the necessary physical properties of the insulating layer.

Initially, a device having an interdigitated structure was used as the vehicle for the experimental work. The metallized emitter and base areas on these units were anodized to 150 volts using a current density of 14 ma/sq in., in a non-solvent forming solution. The anodic layer on the metallized emitter was scribed open exposing the aluminum and a second metal film was deposited over the emitter and anodized base fingers using a metal mask evaporation technique. The anodized base metallizing area which had an emitter metallizing overlay was 1680 square mils, a factor of 15 greater than this device. Measurements of V_{ebo} indicated only 10% of the units had an emitter-base short.

Other experiments on comb type structures modified into an overlay but without the emitters scribed open, showed leakage currents between the metallizing layers of only 5 na at 60 volts.

Recent efforts on insulating layers have been limited to devices designed specifically for this contract. To date these efforts have been largely unsuccessful in so far as fabricating a device capable of the specified operating current. In general the difficulty is in opening the emitter oxide, after anodizing the base metal, so that contact can be made to these areas during emitter metallizing. Specifically, the problem is poor adherence of the photoresist to the substrate due to inadequate surface cleanliness.

Various surface cleanup procedures have been examined with as yet unsatisfactory results.

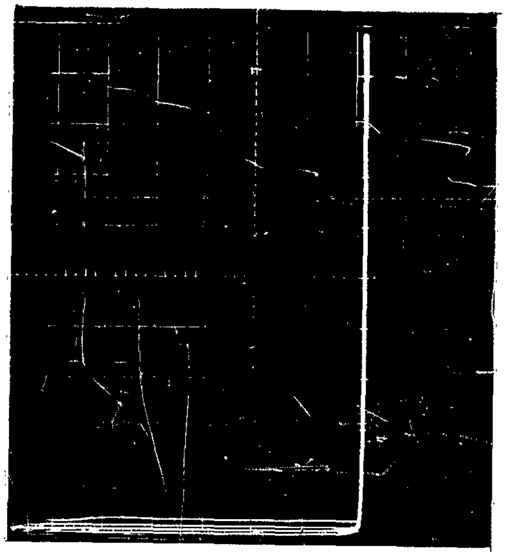
A second possible technique to opening the emitter oxide is the use of a second metal evaporation. This evaporation will take place after forming Al_2O_3 on the base metalizing and will be approximately 2000 Å thick. It is known that this metal film will adhere readily to the substrate with present surface cleanup procedures and that the photoresist will adhere readily to the surface of this film. The photoresist will be defined in the regions over the emitters and the metal film etched using conventional etching techniques. The wafers will then be placed in oxide etch and this thin defined film will be used to mask the remaining areas of the wafers from the oxide etch thereby allowing the opening of the emitter oxide.

A third possible procedure for the fabrication of the overlay will be a metal mask evaporation of silicon monoxide over the base metal after the emitter oxide has been opened. The silicon monoxide will be deposited only over the base metal and no subsequent etching step is required. A metal mask for this technique has been ordered. Due to the grid pattern of base metalizing, two separate evaporations will be needed.

The feasibility of using anodized aluminum as the dielectric material has been shown on this device. Units have been fabricated with several of the emitter areas successfully opened and the device exhibited current gain and excellent emitter-base diode characteristics as shown in Figure (8).

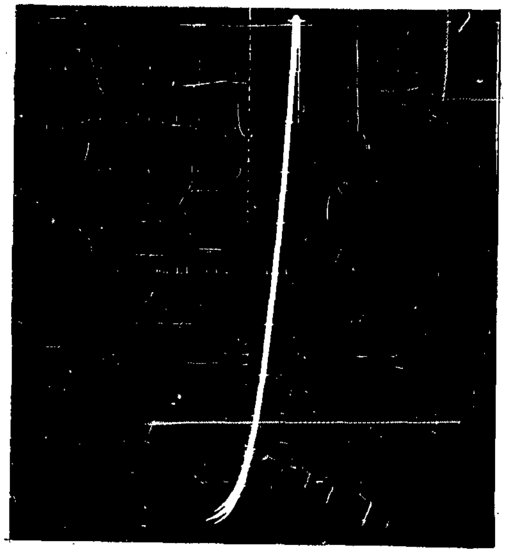
E. Case Design

A high frequency power transistor case has been developed under an RCA



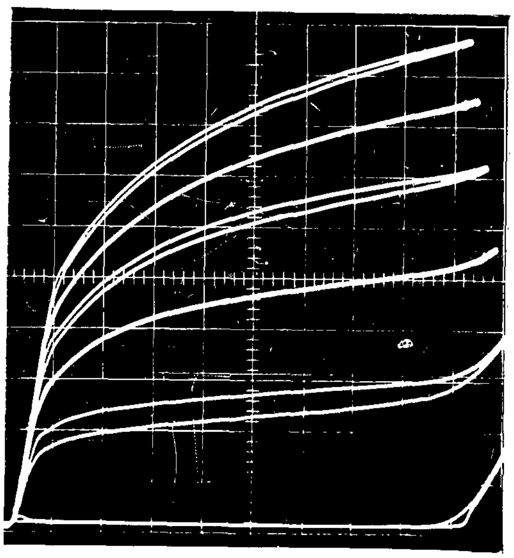
V_{EBF}; V = 0.1 v/division

I = 10 μa/division



V_{EBO}; V = 1.0 v/division

I = 10 μa/division

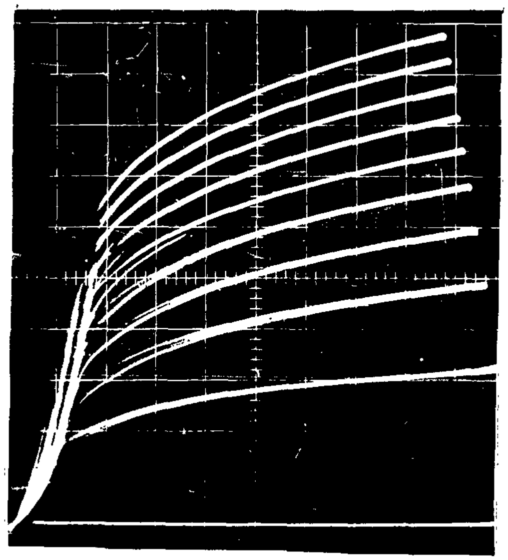


h_{FE} at 2.0 ma; I_C = 0.2 ma/division

I_B = 0.005 ma/division

V = 1 v/division

h_{FE} = 80



h_{FE} at 5.0 ma; I_C = 0.5 ma/division

I_B = 0.04 ma/division

V = 1 v/division

h_{FE} = 14

FIGURE 8 EMITTER-BASE DIODE CHARACTERISTICS AND LOW LEVEL CURRENT GAIN OF THE OVERLAY STRUCTURE program for the 3 watt 150 megacycle device. It is a 7/16 double ended stud package utilizing beryllium oxide to isolate the collector from the case. The thermal resistance is approximately 8°C/W, with a pellet area of 3200 square mils.

The various interelectrode capacitances associated with this case are:

$C''_{cb} = 0.8\ \mu\mu f$

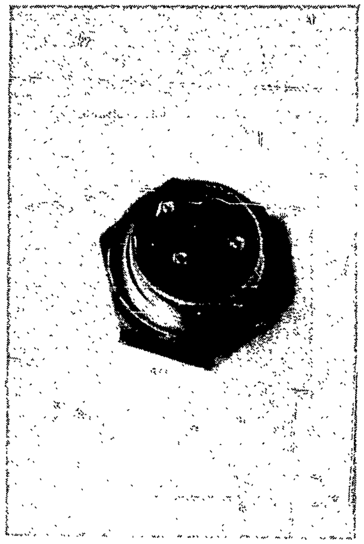
$C''_{eb} = 0.1\ \mu\mu f$

$C''_{ce} = 0.5\ \mu\mu f$

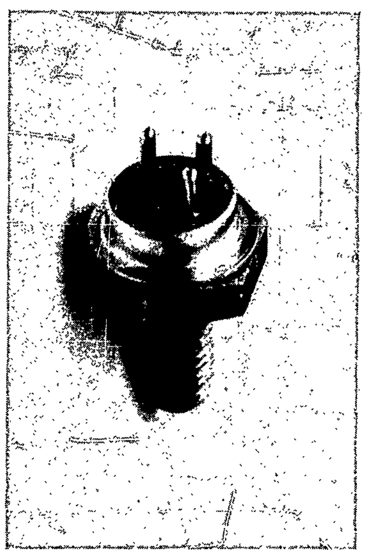
Collector to stud = 2.2 $\mu\mu f$

The emitter lead inductance is less than 3×10^{-9} h.

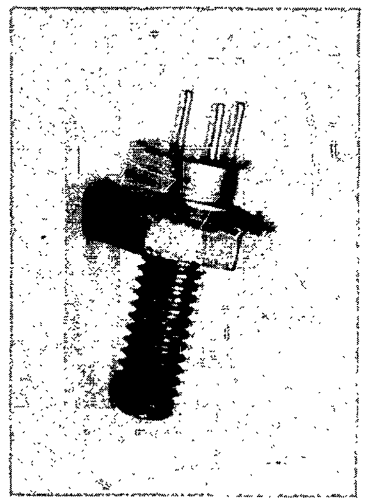
The seal is resistance welded and the leads conform to the 0.200" pin circle of the TO-5 outline. A completed case is shown in Figure (9).



a. Front View



b. Side View



c. Top View

FIGURE 9 HIGH FREQUENCY POWER TRANSISTOR CASE (DOUBLE ENDED STUD-ISOLATED COLLECTOR)

V. CONCLUSIONS

During this quarter, the majority of effort has been expended on investigations of the proposed techniques which will be required to produce this device.

At the present time, photoresist definition on silicon dioxide is excellent and the required dimensions can be readily obtained.

The main area of difficulty in producing an insulating layer by the anodic formation of Al_2O_3 on the base metallizing, is the problem of opening the emitter areas after anodizing. Various surface cleaning procedures have been employed in an attempt to increase the adherence of the photoresist to the substrate with as yet unsatisfactory results.

The feasibility of producing an overlay structure by the anodizing technique has been shown repeatedly by the fabrication of capacitors, the modified comb structure experiments, and the partial successes realized on this device.

Further work will be performed in an effort to improve the adherence of the photoresist to the substrate after anodizing. This work will include evaluation of various surface cleanup procedures and the use of defined thin metal films to act as a mask during the opening of the emitter oxide.

VI. PROGRAM FOR NEXT INTERVAL

During the next reporting period, major effort will be devoted on continued development of the overlay structure. This effort will include attempts to eliminate the difficulties associated with the anodic layer approach and the use of metal mask evaporations of silicon monoxide over only the base metallizing matrix.

Effort will also be expended on the design of the necessary high frequency circuits for the measurements of these devices. These circuits will be designed around low power high frequency comb type units having the same diffusion cycles and cases as the proposed device.

VII. PERSONNEL AND MAN HOURS

Table II below shows the man hours expended during the second quarter of this contract.

ENGINEERS	OCTOBER	NOVEMBER	DECEMBER	TOTAL
J. Bibby	40	48	-	88
D.R. Carley	68	48	30	146
J.H. Cavitt	44	32	38	114
J.F. O'Brien	84	84	76	244
P.L. McGeough	132	120	105	357
TOTAL	368	332	249	949
TECHNICIANS	404	334	284	1022
ALL OTHERS	65.5	49.5	8	123
TOTAL MAN HOURS	837.5	715.5	541	2094

TABLE II

MAN HOURS EXPENDED IN THE SECOND QUARTER

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Radio Corporation of America, Somerville, New Jersey
Silicon 5 watt, 500 mc Transistor
D.Carley, W.Freeman, P.McGeough, J.O'Brien, J.Cavitt
Second Quarterly Progress Report
Signal Corps Contract DA-36-039-SC-90797
Project No. 3A99-21-002, Unclassified

A review of the overlay concept and a comparison of this structure with the comb type geometry is presented. The results of experimental studies of the proposed fabrication techniques including diffusion, photoresist and insulating layers are discussed.

Silicon 5 watt, 500 mc
Transistor

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Signal Corps Contract DA-36-039-SC-90797
Project No. 3A99-21-002, Unclassified

A review of the overlay concept and a comparison of this structure with the comb type geometry is presented. The results of experimental studies of the proposed fabrication techniques including diffusion, photoresist and insulating layers are discussed.

Silicon 5 watt, 500 mc
Transistor

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