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TECHNICAL MEMORANDUM

(TM Series)

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COMMAND SYSTEMS DEPARTMENT

CRT OSCILLOSCOPE DISPLAY

by

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10 April 1963

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SANTA MONICA

CALIFORNIA

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INTRODUCTION

At the request of the Command Systems Department, the Engineering Department has assembled an experimental display system to be used with the Q-32. Data derived from the DATOR drum of the Q-32 will be processed in a display buffer and viewed on a 5 inch Cathode Ray Tube Oscilloscope in the form of dots. The display system will be evaluated, then disassembled.

This document describes system requirements, design considerations and includes detailed logic design of the display buffer and associated components. Alignment and calibration procedures are furnished as part of the document.

I. SYSTEM REQUIREMENTS

System requirements as described by the Command Systems Department are:

1. Build a temporary display buffer using components available in the Engineering Laboratory whenever possible.
2. Use DEC Laboratory digital modules as basic building blocks (a large assortment of DEC modules are in our laboratory stock).
3. Use Engineering's Textronix Type 536 x-y Oscilloscope as the display device.
4. Display a series of dots on the oscilloscope, positioned from data sent from the Q-32's Display Register.
5. Only display a dot when the positioning data is accompanied by a BUSY or DISPLAY bit sent from the Display Register.
6. Use eight bits of vertical positioning data and eight bits of horizontal positioning data.
7. Be able to respond to the standard Q-32 pulses that carry the positioning data and DISPLAY bit from the Display Register.
8. Connect to the Display Register through an IBM connector.
9. Supply the wire necessary to connect the display buffer to within ten feet of the Display Register's connector.

II. COMPONENTS SUPPLIED FOR THE BUFFER DISPLAY SYSTEM

DEC LABORATORY DIGITAL MODULES

- 4 - Type 103 Six Inverter
- 31 - Type 201 Flip-Flip
- 1 - Type 301 Delay (one shot)
- 3 - Type 302 Delay (one shot)
- 2 - Type 401 Clock
- 3 - Type 610 Pulse Amplifier

DEC SYSTEM DIGITAL MODULES

- 1 - Type 4676 Intensity Amplifier
- 4 - Type 4677 Single-Ended Bridge
- 1 - Type 1563 Digital-to-Analog Converter

OTHER DEC EQUIPMENT

- 6 - Type 901 Mounting Panel
- 6 - Type 750 Power Cable
- 1 - Type 1906 Patchcord Mounting Panel
- 2 - Type 721 Power Supply
- 1 - Special Extender Module
- 1 - Type 911 Patchcords, Large Assortment

OTHER POWER SUPPLIES

- 1 - Kepco Model SC-18-4M, AF/F 17995
- 1 - Nobatron Model T50-1.5, AF/S 3901

2 - Filter Capacitor 5,000 μfd, 50V

CRT OSCILLOSCOPE EQUIPMENT, TEKTRONIX

1 - Type 536 Oscilloscope, AF/S 3735

1 - Type 53/54 G Plug-In Unit, AF/S 5002

1 - Type 53/54 K Plug-In Unit, AF/S 3741

1 - Type 310 Oscilloscope, AF/S 4417

1 - Type 53 "Scope-Mobil" Cart, S-2805

1 - Polarized Viewer

1 - Set Of Probes

BREADBOARD EQUIPMENT

2 - RC Network Boards

1 - Transmission Line Cable and Connector

3 - Shielded Lines For The Display

1 - 19" Relay Rack, 6 Foot

III. PHYSICAL DESCRIPTION

The display buffer is mounted in a standard 19-inch rack, 6 feet high. The rack contains all DEC digital modules for the buffer, the test generator, and the calibration system. The physical position of each module and it's individual function is shown in figure 2. Patchcords are used to wire the DEC modules. Spare modules and patchcords are provided for maintenance, and to facilitate minor alterations in the system. The power supplies are mounted above and below the digital modules. Two DEC power supplies provide the normal voltages for the DEC modules. The Kepco power supply provides the -10 volts reference voltage, and the Nobotron power supply provides the -45 volts for the intensity amplifier.

The Textronix 536 Oscilloscope is located adjacent to the buffer rack and may be located on either side. A Type G Differential Amplifier Plug-In Unit is inserted into the right hand slot of the 536.

IV. WIRING NOMENCLATURE

The DEC Laboratory digital modules do not have pin numbers to define patchcord wiring. To help wire the patchcords to the modules, the following system is used:

First Item = the module row, lettered from top to bottom (A thru F).

Second Item = the module columm, numbered from left to right on the patchcord side.

Third Item = modifiers to define the particular point on the selected module.

- First Modifier = location of logic circuit in module (T = circuit on top, M = circuit in the middle, B = circuit on the bottom).
- Second Modifier = location of logic circuit in module (L = circuit on the left, R = circuit on the right).
- Third Modifier = any other word that might clarify the point.

For example, the descriptor B6-MR-base means that the module is located in row B, columm 6. This module is a Type 103 Inverter. The desired inverter is in the middle and on the right side of the module. The connection is to the inverters base.

The logic diagrams are drawn using the standard DEC notation and Symbols as presented in the DEC Digital Modules Catalog.

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V. DISPLAY BUFFER SYSTEM

The display buffer system block diagram is shown in figure 1. The CRT spot on the display oscilloscope is positioned from voltages derived from the digital-to-analog (D/A) converter. A DEC Type 1563 D/A converter module consisting of two, eight-bit ladder networks is used*. The D/A converter has a settling time of 1 μsec. and the four most significant bits of each ladder network are adjustable. It has a temperature coefficient of ±20 PPM/°C. Single-ended bridges (Dec modules Type 4667) are used to drive the ladder networks. The single-ended bridges convert the unregulated standard -3 volts DEC signals into -10 volt referenced levels. They have a delay of approximately 0.3 μsec. The single-ended bridges are driven from a 16 flip-flop buffer register (DEC modules 201) which are set from the data pulses sent by the XD1A. The transition time of the Type 201 flip-flop is about 0.15 μsec.

Adding transition and settling times, stabilized display data is presented to the CRT Oscilloscope approximately 1.5 μsec. after the arrival of the XD1A data pulses. The 1.5 μsec. calculation assumes that the -10 volt reference supply remains clean during positioning. Positioning from all zeros to all ones creates a current impulse of over one-half ampere. Voltage spikes and ringing are inevitable on the -10 line due to its inherent inductance and capacitance. To reduce the time of this disturbance to less than 3 μsec., a 5,000 μfd capacitor is connected across the single-ended bridges at their reference voltage input.

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*For further information on the DEC modules, refer to the DEC Digital Modules Catalog.

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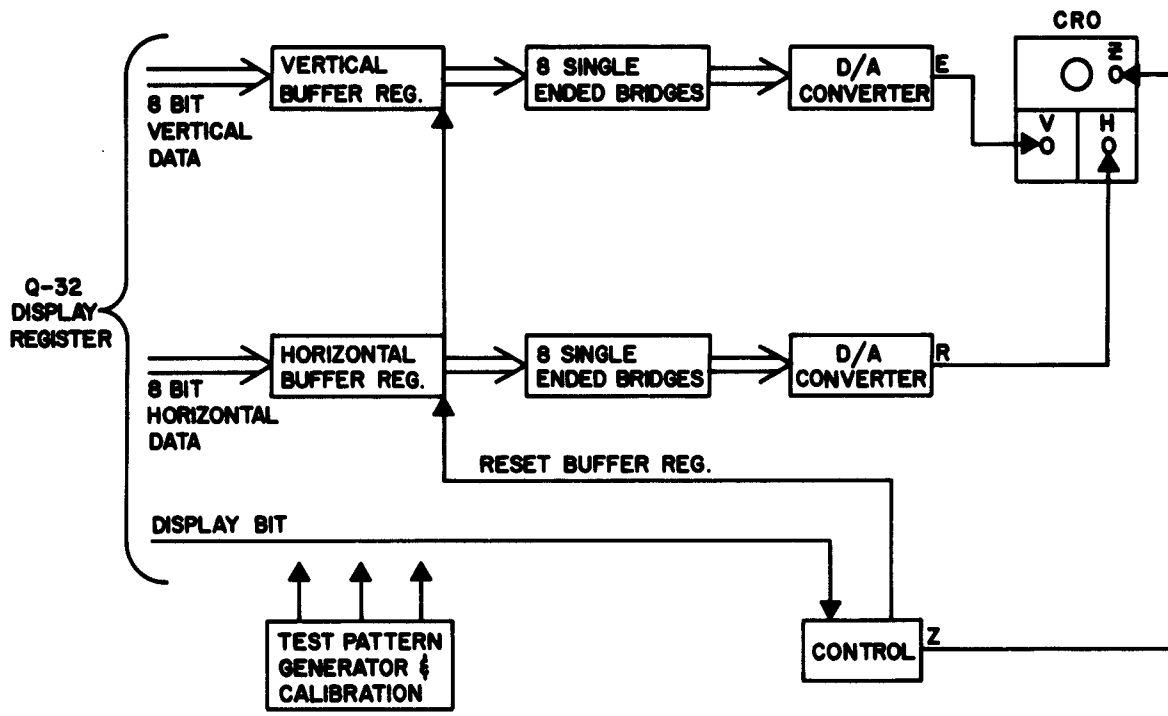

Figure 1 System Block Diagram

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COLUMN

ROW	1	2	3	4	5	6	7	8	9
A									
B					5000 μf	INV CAL.	FF CAL.	FF SWEEP GEN.	FF
C		SINGLE ENDED BRIDGES COL. 7, 8, 10, 11 D/A CONVERTER COL 9						INTENSITY AMPL. COL. 20	
D	FF 128 H	FF 64 H	FF 32 H	FF 16 H	FF 8 H	FF 4 H	FF 2 H	FF 1 H	INV
E	FF 128 V	FF 64 V	FF 32 V	FF 16 V	FF 8 V	FF 4 V	FF 2 V	FF 1 V	INPUT P.A.
F	FF 512	FF 256	FF 128	FF 64	FF 32	INV	RESET DMV	Σ MOD. DMV	INPUT DMV
G	FF 16	TEST PATTERN COUNTER FF 8	FF 4	FF 2	FF 1	TEST CLOCK T=22μS	TEST P.A.		

Figure 2 Buffer Layout

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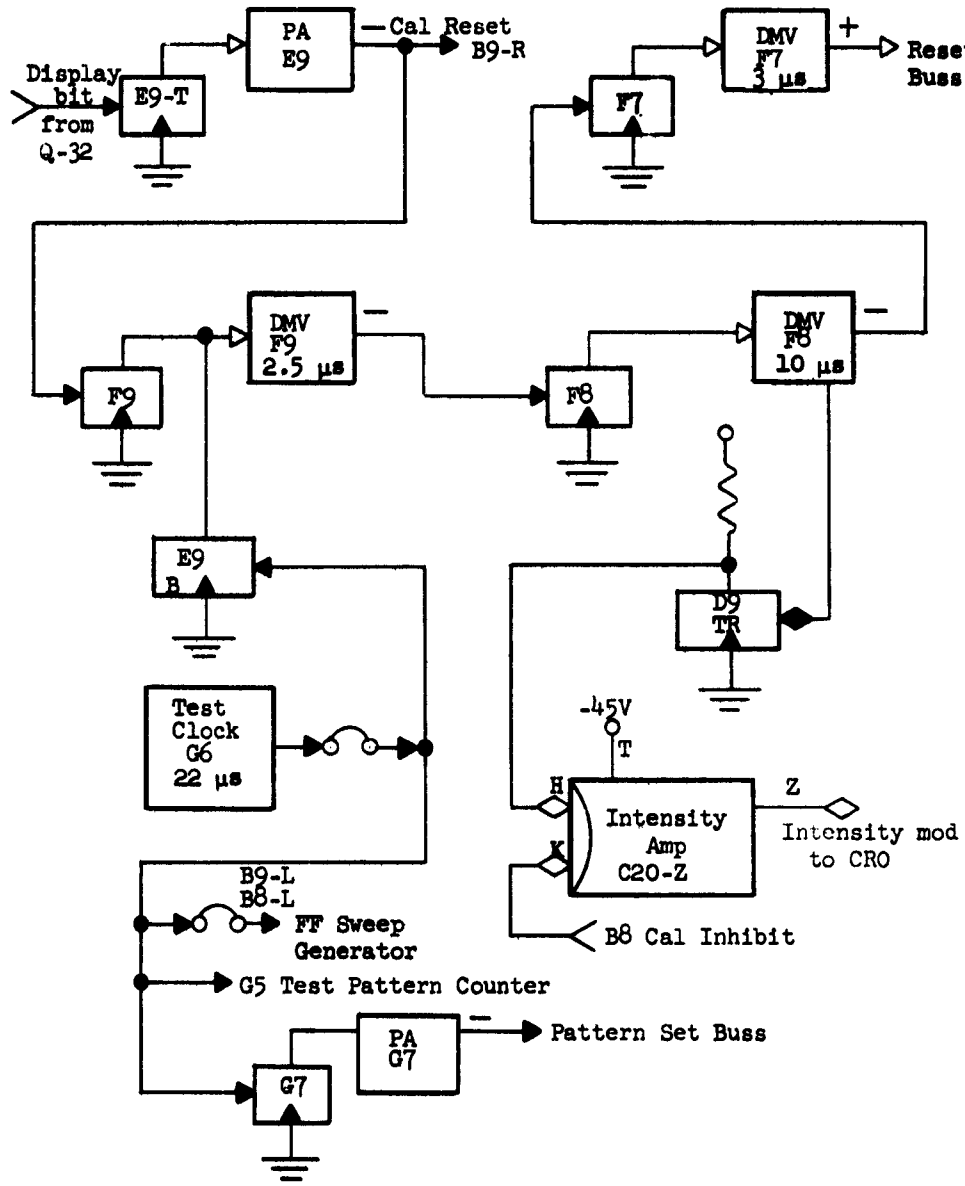

Figure 3 Control

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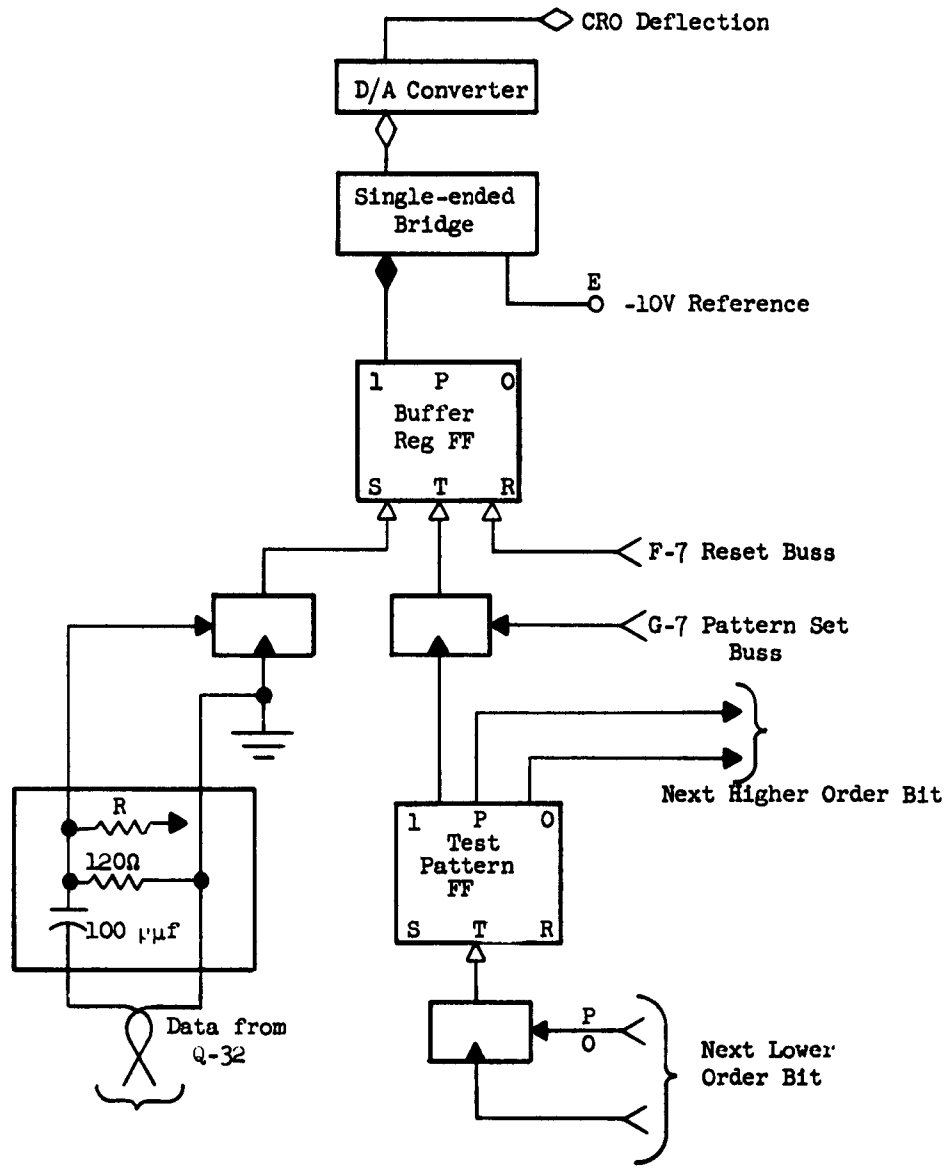

Figure 4 Buffer Register

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DISPLAY REGISTER BIT	DISPLAY BIT	FF POSITION	SINGLE-ENDED BRIDGE		D/A CONVERTER		TEST PATTERN COUNTER	
			Input	Output	Input	Output	FF Pos.	Counter Level
	128 H	D 1	C10 - K	C10 - J	C9 - S	C9 - R	G 1	NOT 16
	64 H	D 2	C10 - P	C10 - N	C9 - T		G 2	NOT 8
	32 H	D 3	C10 - V	C10 - U	C9 - U		G 3	NOT 4
	16 H	D 4	C10 - Z	C10 - Y	C9 - V		G 4	NOT 2
	8 H	D 5	C11 - K	C11 - J	C9 - W		G 5	NOT 1
	4 H	D 6	C11 - P	C11 - N	C9 - X		G 5	NOT 1
	2 H	D 7	C11 - V	C11 - U	C9 - Y		G 5	NOT 1
	1 H	D 8	C11 - Z	C11 - Y	C9 - Z		G 5	NOT 1
	128 V	E 1	C7 - K	C7 - J	C9 - F	C9 - E	F 1	NOT 512
	64 V	E 2	C7 - P	C7 - N	C9 - H		F 2	NOT 256
	32 V	E 3	C7 - V	C7 - U	C9 - J		F 3	NOT 128
	16 V	E 4	C7 - Z	C7 - Y	C9 - K		F 4	NOT 64
	8 V	E 5	C8 - K	C8 - J	C9 - L		F 5	NOT 32
	4 V	E 6	C8 - P	C8 - N	C9 - M		F 5	NOT 32
	2 V	E 7	C8 - V	C8 - U	C9 - N		F 5	NOT 32
	1 V	E 8	C8 - Z	C8 - Y	C9 - P		F 5	NOT 32

Figure 5 Wiring Chart For Data Bits

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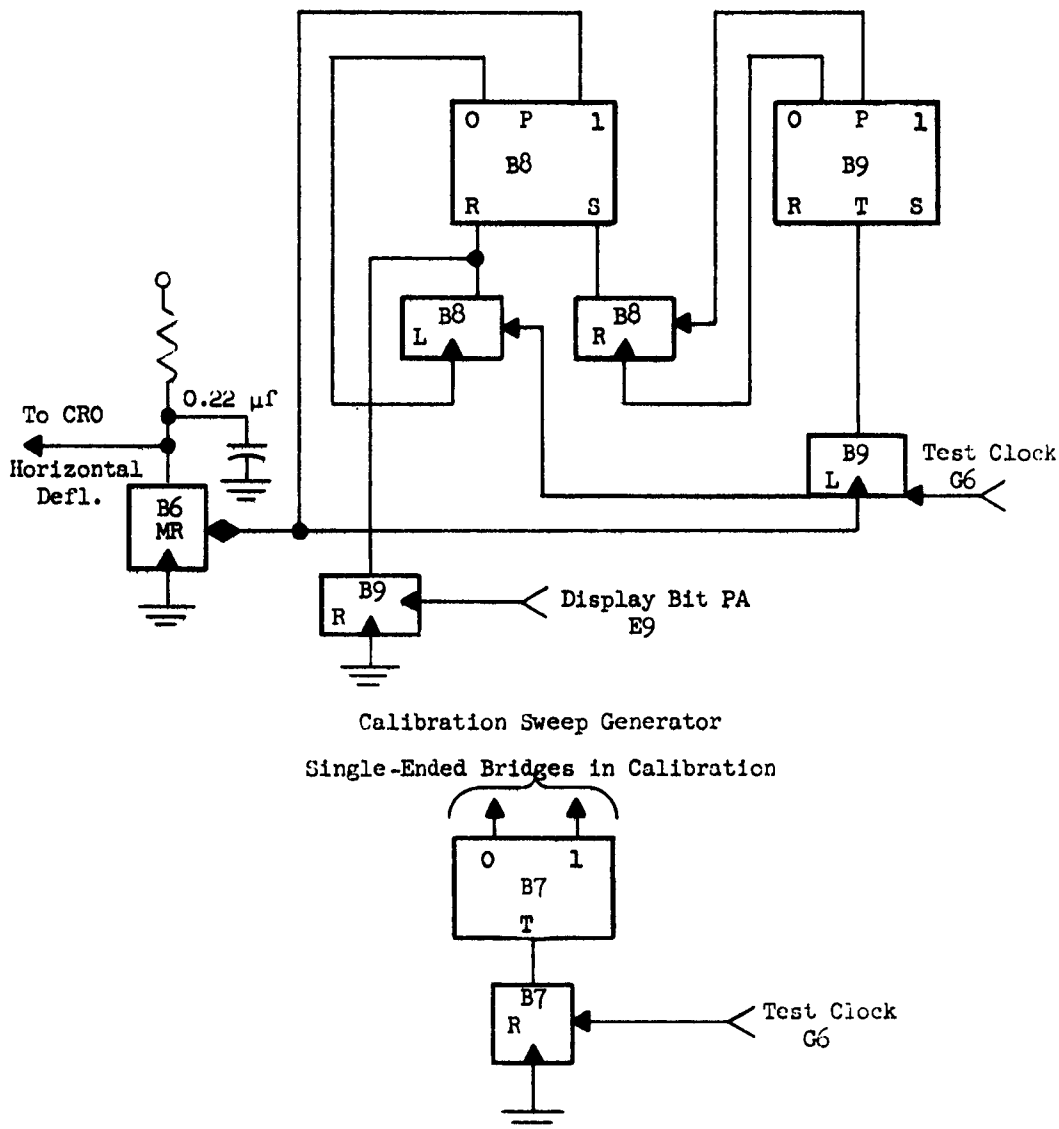

Figure 6 Calibration Flip-Flop

With Type G Amplifier units plugged into the 536 Oscilloscope, a rise time of 35 nanoseconds can be expected with very little overshoot and subsequent ringing.

With the positional data settled on the deflection plates of the 536 Oscilloscope, the CRT electron beam is turned on by applying a positive 45 volt intensity pulse from a DEC Type 4676 intensity amplifier. The input gate and output pulse of the intensity amplifier are shown in figure 10A. The intensity pulse is presently set for a width of approximately 12 μsec.

Visual tests demonstrate that the CRT spot is not noticably brighter with wider intensity pulses. Due to the delay and fall time of the intensity pulse, it will not reach completion until approximately 15 μsec. after the arrival of the intensity gate. The DISPLAY pulse arrives in parallel with the data pulses from the Q-32 and is used to initiate both the intensity pulse and the buffer reset pulse.

The DISPLAY pulse is initially delayed 2.5 μsec. to allow for settling before the input intensity gate is generated (figure 10A). A DEC Type 301 delay unit is used to generate the gate.

Since only ONES signals are transferred to the display buffer from the Q-32, the buffer register must be precleared. The DEC Type 201 flip-flop must be cleared at least 0.2 μsec. before the arrival of the data pulses. On the other hand, the buffer register must not be cleared before the intensity gate to the CRT has been completely removed. A delay unit is triggered at the end of the intensity gate to clear the buffer register after 3 μsec.

VI. LINE TERMINATING NETWORK

The XD1A will be transferring pulse signals to the display buffer, and because of the shape and frequency of the pulses, transmission lines and terminating networks must be used. The cheapest and simplest type of transmission line is the twisted pair. This line can be made up in a laboratory by twisting two lines of regular hookup wire together.

The terminating network is shown in figure 4. The decoupling capacitor prevents any flow of DC current through the circuits in the XD1A. The 100 μμf capacitor loses only approximately 0.1 volt in charging. It is small enough to have low series inductance and a short time constant into the terminating resistor. The terminating resistor is 120 ohms which approximately matches the characteristic impedance of the twisted pair. To minimize ringing and crosstalk, each ground is carried through with its signal lead to its own input module. Ringing may possibly be caused by reflections if our lines do not match the lines in the Q-32. If crosstalk proves to be a problem, it is possible to bias the input modules further "off" by inserting a bias current through R from the positive voltage power supply.

Terminal board construction is used to hold the line terminating components, provide ease of connecting the twisted pair line, provide easy coupling between the terminal points of the line terminating components and the plug cords of the DEC modules, and to keep the buffer neat and clean.

VII. DISPLAY: SCALING, SPOT SIZE, PLOTTING RATE, AND JITTER

SCALING

The ladder network of the D/A converter is referenced to -10 volts. Its maximum output voltage then approaches -10 volts. The minimum voltage change, i.e., the change in voltage due to a change in the least significant bit of the input, is the reference voltage divided by the total number of possible input bit configurations. The eight position-bits of each coordinate point result in an output voltage that varies in 39 millivolt steps from zero to -10 volts ($\Delta V = \frac{10}{2^8} = \frac{10}{256} = 39$ mv).

The 5-inch CRT of the Textronix 536 has a useful diameter of 4 11/16 inches or 11.9 cm. A square with 8.4 cm sides will just fit in the viewing area. The tube face is covered with a graticule marked with one centimeter square divisions, eight in heighth and ten in width.

If the 8 cm per side display is used, one volt from the ladder network corresponds to 0.8 cm deflection on the CRT.

This scaling gives 32 points per cm. To be able to resolve point changes, the spot size must not be greater than 0.3 mm over the viewing area.

SPOT SIZE

The Textronix 536 uses a postaccelerator CRT. This type of CRT has a helix accelerator and provides a high beam current with good focus characteristics. Unfortunately, this focus can not be held over the whole display area. The

focus and astigmatism controls can be adjusted to form the desired spot size on only a portion of the CRT face. If the beam is focused at the center of the CRT face, the beam will form an elongated spot at the edges. The spot will be elongated away from the center of the CRT and will spread up to 7 times the width of the center focused spot.

If the spot is adjusted for the best overall shape, average spot size will be approximately 0.6 mm which only allows a resolution of 7 bits (128 elements).

CRT Oscilloscopes that use a monoaccelerator tube, such as the Textronix 561, can maintain beam focus over the whole display area. However, the beam current is not as high and the display is not as bright.

The 536 uses a P31 phosphor. The P31 phosphor has a green fluorescence and phosphorescence, a medium persistence*, and a relative brightness of 248.** This phosphor gives a bright, sharp image that is principally used in oscilloscope displays in high ambient light.

PLOTTING RATE

To determine the relation between beam duration, spot brightness and focus, subjective tests were performed on the Textronix 536. The tests were performed with a dot pattern recurrent at a 45 cycle rate. The test results were:

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*Relative brightness is taken with a Spectra Brightness Spot Meter, which incorporates a C.I.E. standard eye filter. Representative of 10 K V aluminum screens.

**Persistance is to JEDEC Classification (to 10% level).

1) a beam duration greater than 7 to 8 μsec. does not noticably brighten the display, 2) at durations less than approximately 6 μsec., brightness decreases rapidly, 3) you cannot compensate for a decreased brightness by increasing the beam current without defocusing the beam, 4) I feel that a minimum acceptable display brightness can be accomplished with a beam duration of approximately 4 μsec.

The cycle time required to display a point can be reduced to three sequential timing periods: 1) the time required for settling following the arrival of the data pulses, 2) the time required for the spot to be displayed on the CRT, and 3) the time required to reset the display buffer.

The settling time of the system is approximately 2.5 μsec. and could be reduced to approximately 1 μsec. by employing special techniques. For a bright display, the CRT beam should be on for at least 8 μsec. A 4 μsec. beam duration may give acceptable brightness. It is imperative that the display buffer be reset before the arrival of data pulses. Resetting only required a lead time of approximately 0.3 μsec. but a safety time of approximately 1 μsec. is necessary.

For the display to operate at its full brightness, a point can be displayed approximately every 12 μsec. (2.5 μsec. plus 8 μsec. plus 1.3 μsec.). If a reset pulse precedes the data pulses by approximately 0.3 μsec., the 1 μsec. safety time gap can be recovered. With a slight degradation of the display brightness, a better settling time, and a special reset pulse; a point could be displayed every 5.5 μsec.

JITTER

The display buffer and oscilloscope use 60 cycle power, and to some degree, 60 cycle voltage and currents are present throughout the display system. When the 60 cycle noise is superimposed on the 45 cycle display rate, the display will jitter at a beat rate of 15 cycles. Empirical data shows that people are most sensitive to movement or flicker at 8 cycle rates. Fifteen cycle jitter is very noticable and hard to eliminate.

VIII. CABLE HOOK UP

Connect cabling as follows:

1. Connect C9-E in the buffer rack to the A input of the Type G Unit in the 536 Oscilloscope.
2. Connect C9-R in the buffer rack to the input of the Type K Unit in the 536 Oscilloscope.
3. Connect C20-Z in the buffer rack to the INTENSITY MOD INPUT of the 536 Oscilloscope.
4. Connect the buffer rack common to the 536 Oscilloscope common.
5. Connect the Display Data cable to the Q-32.

IX. TURN ON PROCEDURE

Set up the 536 Oscilloscope as follows:

1. Set gain control to 1 volt/cm on both plug-in units.
2. Set function switch to DC on the Type K Unit.
3. Set function switch to A, DC on the Type G Unit.
4. Set intensity modulation switch to DC.

Turn on DC voltages as follows:

1. DEC supplies ON.
2. -10 volt supply ON.
3. -45 v (intensity voltage) ON.

With the DC voltages ON, the positioning and beam controls are adjusted for a centered display 8 cm square.

The Oscilloscope should have a warm-up period of at least a half hour.

X. DISPLAY TEST AND CALIBRATION

For calibration purposes, a point is needed on each corner of the test pattern for alignment with the display area. Points are also needed along the edges and middle of the test pattern for checking linearity and spot shape. Some form of dot groupings across the display is desirable for checking display resolution. The test pattern should not contain more points than are available from the XD1A display field (1,024)*, and it should have the same display rate (44.4 cps). For Display Buffer check-out and maintenance, the test pattern generator should exercise as much of the buffer as possible in the same way the buffer will operate with the XD1A.

The test pattern shown in figure 7 satisfies the defined requirements and is relatively easy to generate. For clarity, only seven of the actual 17 rows and columns are shown. A corner of the test pattern is expanded to show the fine grain dot pattern.

The test pattern is generated from a 2^{10} binary counter. Counter bit weight 2^0 conditions the setting of the four least significant bits of the horizontal buffer register. Counter bit weight 2^1 to 2^4 conditions bits 2^4 to 2^7 of the horizontal buffer register. Counter bit weight 2^5 conditions the setting of the

*Each drum field has 8,196 slots, of which 8,192 are addressable registers. Every eighth register is to be made available for the CRT Oscilloscope display. A drum field could then contain up to 1,024 display points. It is assumed that the drum register counter in the XD1A is reset at the beginning of every field. If it isn't the contents of a different set of registers will be displayed on alternate drum revolution.

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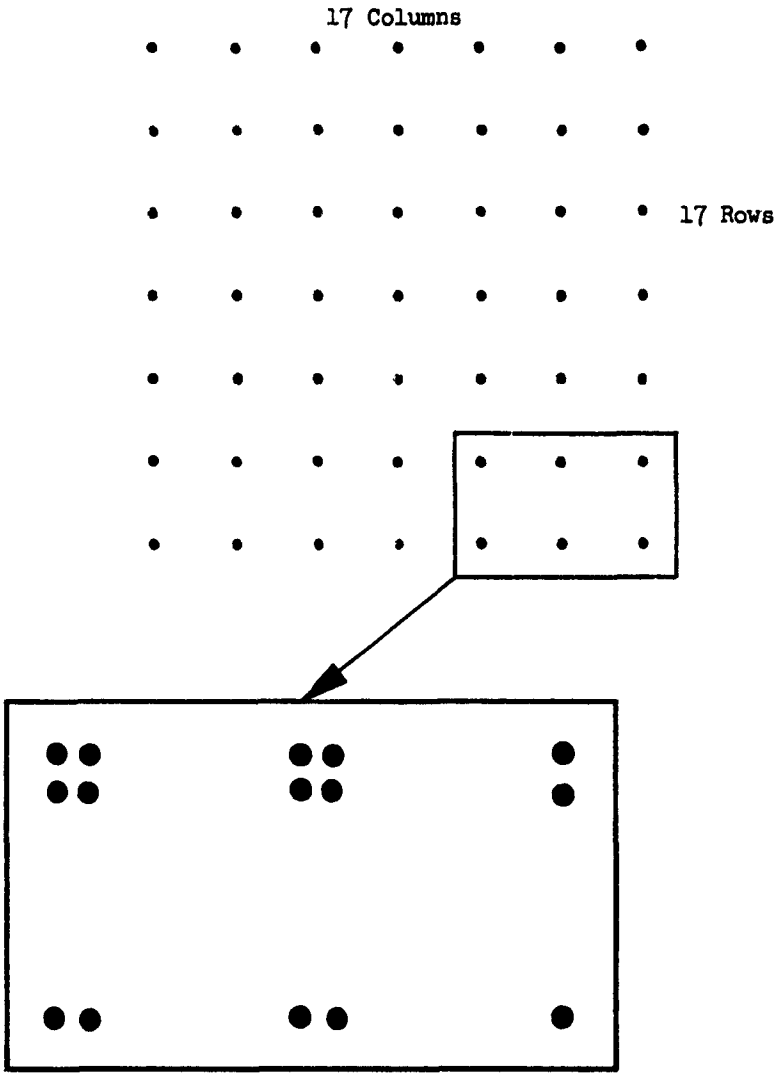

Figure 7 Test Pattern

four least significant bits of the vertical buffer register. Bits 2^6 to 2^9 of the counter complete the setting conditions of the vertical buffer register by connecting to bits 2^4 to 2^7.

The counter pattern is thereby injected into the buffer registers in a sequence that causes the test pattern to be series of horizontal lines that are stepped vertically.

The corner points of the test pattern are realized when the buffer registers contain all ONES or all ZEROS. Conditioning the four least significant bits of each buffer register from the least significant bit of each counter grouping gives a fine grain dot grouping with the dots only one position apart.

The counter is stepped by a test clock running with a period of 22 μsec. (the display period from the XD1A). The test clock also simulates the display bit from the XD1A in initiating the buffer timing cycle. The DATA bits from the XD1A are simulated by the test clock setting the counter level into the buffer register.

DIGITAL-TO-ANALOG CONVERTERS

The DEC D/A converter Type 1563 uses two independent voltage divider (ladder) networks to convert digital inputs into analog voltages. One of the binary ladder networks is shown in figure 8. Each input is weighted in a binary ratio to produce an output voltage reflecting the input digital value. For correct weighting of inputs in the ladder network all of the inputs must be terminated to either ground or a reference voltage. The output of the ladder network must

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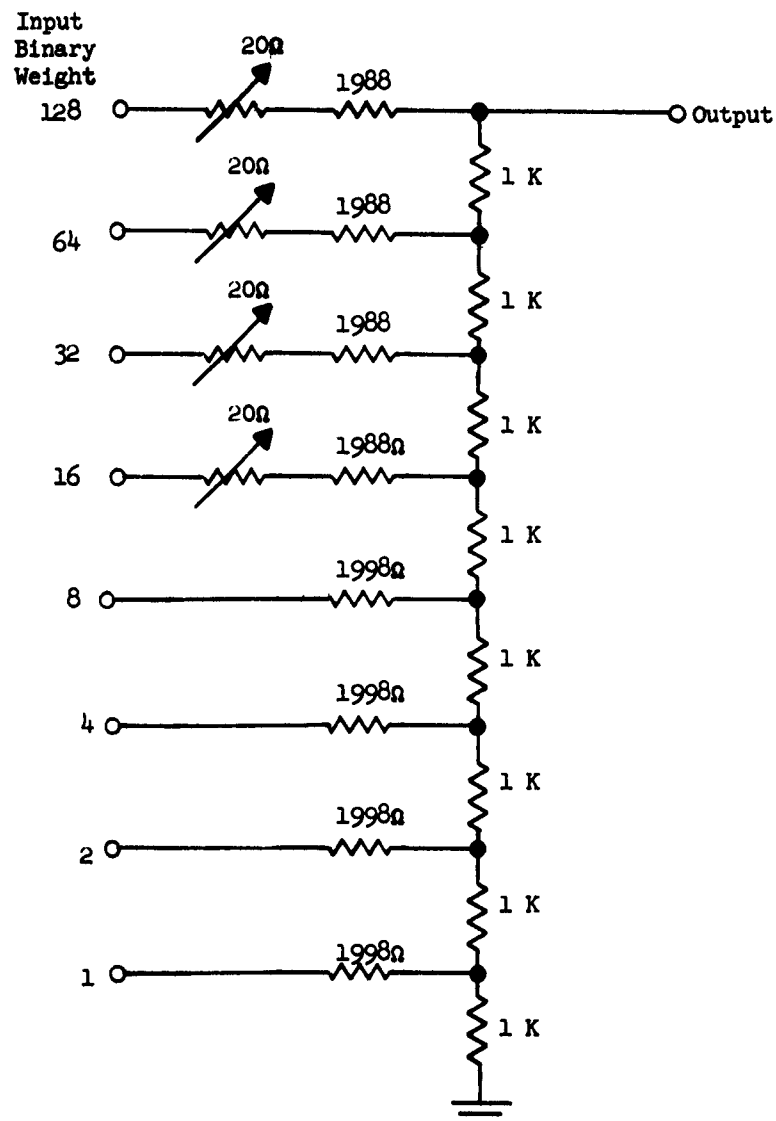

Figure 8 Binary Ladder D/A Converter

not have variable load, and ideally should not be loaded at all.

Small variations in the weighting of the least significant bits of the ladder network have a minor importance since their contributions to the output voltage is small. Even so, the ladder network uses 0.1% wire wound resistors for these bits. Small variations in the weighting of the most significant bits can completely upset the output voltage and precision trimmer resistors are necessary for correction. The accuracy of the D/A converter also depends on the stability and regulation of the reference supply. The impedance and offset voltage offered by the circuits connected to the ladders also effect the D/A converter's accuracy.

CALIBRATION OF THE D/A CONVERTERS

Calibration consists of adjusting the four trimmer resistors on both ladder networks (refer to figure 8). Only the four most significant bits of each ladder network are adjusted.

In the binary weighting sequence, each higher order bit has a weight equal to all the lower order bits plus the weight of the least significant bit. That is, bit weight 16 is equal to the sum of bit weights 8, 4, 2, and 1 plus the bit weight of 1 again. The change in the output of the ladder network due to the change in the least significant bit then becomes the calibration reference.

Calibration is performed by measuring the weight 1 shift when shifting from a higher order weight to the sum of all the lesser order weights. Figure 9 shows a block diagram of the calibration set up. The wiring is shown for adjusting

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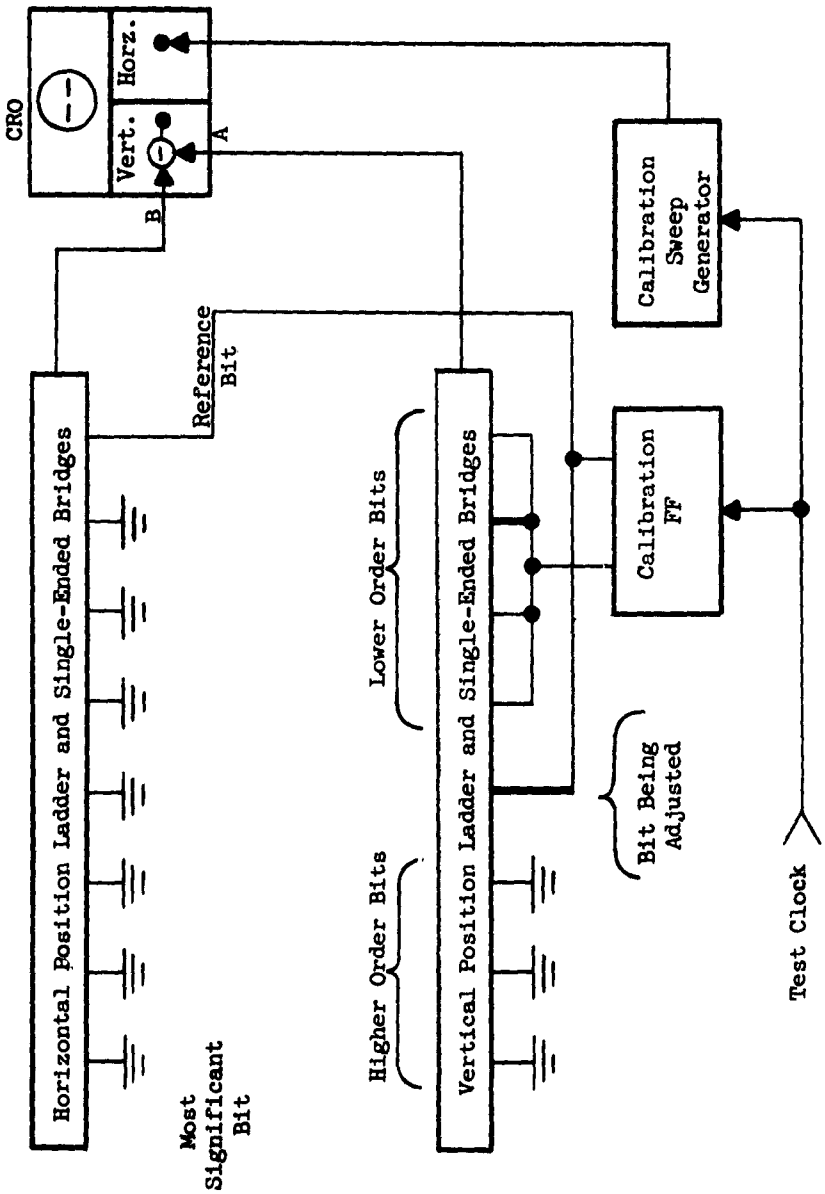

Figure 9 Block Diagram For Adjusting D/A Converters, Wiring Shown For Adjusting Bit Weight 16 Of The Vertical Positioner

bit weight 16 of the ladder network which supplies vertical position. The single-ended bridges are considered as part of the ladder networks for adjustment. The logic diagram of the modules used in the calibration hook up is shown in figure 6.

A -10 volt reference supply was chosen (DEC recommended a reference voltage of -10 volt for the greatest accuracy). It is obtained from a transistor power supply regulated to 0.1% with a ripple of only 1 mv. The voltage is set by an external fixed resistor to prevent change. It is necessary to connect a 5,000 μfd capacitor across the reference voltage input of the single-ended bridges to squelch ringing and other disturbances. Any variation in the reference voltage would be reflected on the output of the D/A converter in proportion to each driving bit weight. The D/A converter requires current to flow both into and out of the reference power supply. Therefore, 0.5 amp source load is connected across the supply to keep it in regulation.

The single-ended bridges supply the reference level signals to the ladder network at a low impedance. Their impedance to ground will fall between 4 and 9 ohms and their impedance to the reference voltage will be 1 to 5 ohms. Since the particular impedance to ground or to the reference voltage varies for each single-ended bridge, the trimmers in the ladder networks are adjusted for each circuit. Changing the positions of the single-ended bridges relative to the ladder network inputs may necessitate recalibration of the D/A converter.

CALIBRATION PROCEDURE

Remove the 16 wires connecting the buffer register to the single-ended bridges at the buffer resistor (reference figure 3). Connect the wires from the inputs to the single-ended bridges as shown in figure 9.

The weight 1 bit of the horizontal position is the reference bit and it is connected to the ONE side of the Calibration Flip-flop (B-7). The first bit to be adjusted is weight 16 of the vertical position and it is also connected to the ONE side of the Calibration Flip-flop (B-7). The lower order bits of the vertical position (weight 8, 4, and 2 and 1) are connected to the ZERO side of the Calibration Flip-flop (B-7).

The rest of the wires are connected to ground. The horizontal position line (from C-9R) is connected to input B of the differential amplifier. The vertical position line (from C-9E) would already be connected to input A of the differential amplifier. Set the amplifier gain to 0.05 volts per cm on both inputs and set input selector switch to AC coupled, A-B.

Connect the calibration sweep generator (B6-MR collector, figure 6) to the input of the Type K amplifier of the Textronix 536 with an auxiliary lead.

Set the gain to 0.2 volts per cm and the input selector switch to AC coupled. Place the D/A converter (C-9) on the extender module. Turn the Textronix 536 around so the screen may be viewed while adjusting the D/A converter trimmers. The test clock should now be connected to the Calibration Flip-flop (B7-BR base) and to the calibration sweep generator (B8-BL base and B9-BL base). Two line

segments should be visible on the screen. As a check, change the gain of either the A or B input on the differential amplifier: each line segment on the screen should split into two vertically displaced lines. Set both gains back to 0.05 volts per cm.

Adjust the differential amplifier Type G Plug-in unit, in the Textronix 536, for common mode rejection. This adjustment may be done by removing the D/A positional lines and connecting the A and B inputs to Calibration Out. With the calibration set to 5 volts per cm, adjust the Differential Balance control to a single merged line. Reconnect the D/A positional lines and the ladder networks are ready to be adjusted.

On the D/A converter module, adjust the first trimmer away from the connector until the two vertical line segments have merged into one. The weight 16 bit of the vertical position has now been adjusted. Notice that the adjustment afforded by the trimmer is very slight. The adjustment becomes more critical as the weight of the bits is increased. The next higher bit is adjusted by transferring the wire from weight 16 vertical position to the ZERO side of the Calibration Flip-flop and replacing it with weight 32 of the vertical position. On the D/A converter adjust the second trimmer away from the connector until the two vertical line segments have merged into one. The third trimmer away from the connector adjusts the weight 64 vertical position and the fourth trimmer away from the connector adjusts the weight 128 vertical position.

The D/A converts horizontal position trimmers are adjusted the same as the

vertical trimmer, except every where "vertical" is used, substitute "horizontal" and vice versa. Weight 16 horizontal position is adjusted by the eighth trimmer away from the connector. Likewise, weight 32 horizontal position is adjusted by the seventh trimmer away, weight 64 by the sixth trimmer, and weight 128 by the fifth.

XI. APPENDIX

DEC AND IBM COMPATABILITY

It was necessary to determine if the interface between the XD1A and the display buffer is likely to cause any problems. If possible, we would like to drive the DEC Laboratory digital modules we have in stock directly from XD1A pulses. The only requirement of the pulses sent from the XD1A is to set a flip-flop register in the display buffer. It is not necessary to transfer signals back to the XD1A from the display buffer.

The XD1A pulses are relatively sinusoidal in their negative excursion and have an amplitude of from -2.5 to -4 volts. Their pulse width measured at the 10% points is 40 ± 5 nanoseconds (figure 10B). The pulse width at the 50% points may be approximated by assuming the waveforms to be sinusoidal. The 10% points then occur at 5° 45' and 174° 15'. The 50% points occur at 30° and 150°. The 50% pulse width is then calculated to be $\frac{120}{168\ 1/2}$ (40) = 28.5 nanoseconds.

The DEC Laboratory digital modules in stock are the DEC 100 series designed to operate from relatively square pulses having an amplitude of -2.5 to -3 volts. Their 50% pulse width is approximately 70 nanoseconds.

DEC respresentatives recommend that the interface use pulse stretching techniques to widen the XD1A pulses. Pulse stretching is accomplished with a 70 nanosecond pulse amplifier that bootstraps its input from its output (figure 12H).

Unfortunately, we do not have the necessary pulse amplifiers in stock and prefer

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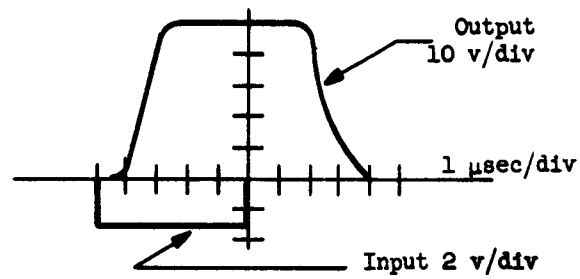

Figure 10A Intensity Amplifier

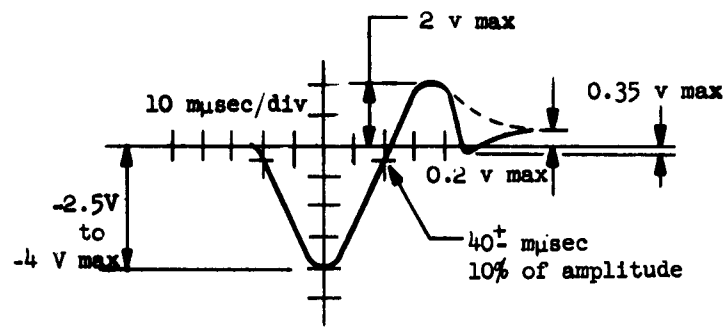

Figure 10B IBM Q-32 Standard Pulses

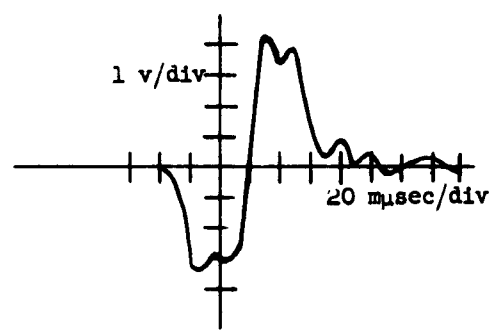

Figure 10C DEC Test Pulse

not to purchase them. A test was then set up to determine if we should gamble on being able to use the DEC 100 series modules without pulse stretching.

Simulating the XD1A pulses proved difficult. Since we do not have a pulse generator capable of generating 30 nanoseconds pulses, we came the closest by using a dual pulse generator of a DEC 5,000 series module. This pulse generator produces relatively square-shaped 40 nanosecond pulses.

The test setup is shown in figure 11. The two 5,000 series pulse generators were connected in cascade to obtain the purest and narrowest pulse. The resultant pulse is shown in figure 10C. Variable pulse amplitude was obtained by inserting a DC level. The two testing flip-flops were selected from an arbitary group of 10 flip-flops to show typical response. Various input networks were tested to determine their merit for use in the interface.

The input networks are shown in figure 12A to 12H. E is the input pulse and E_{min} is the minimum pulse amplitude measured from ground to give reliable triggering.

Conclusions of the test are 1) the flip-flops are relatively easy to trigger, and 2) the single inverter driver should be sufficient as an interface module. The 100 series inverter also triggered the flip-flop as reliably as the higher frequency 5,000 series inverter. The pulse amplifier was the most sensitive to the input pulse and stretching the pulse did not alter the trigger response of the flip-flop. Although these tests do not guarantee operation from the XD1A pulses, they do lend a degree of confidence.

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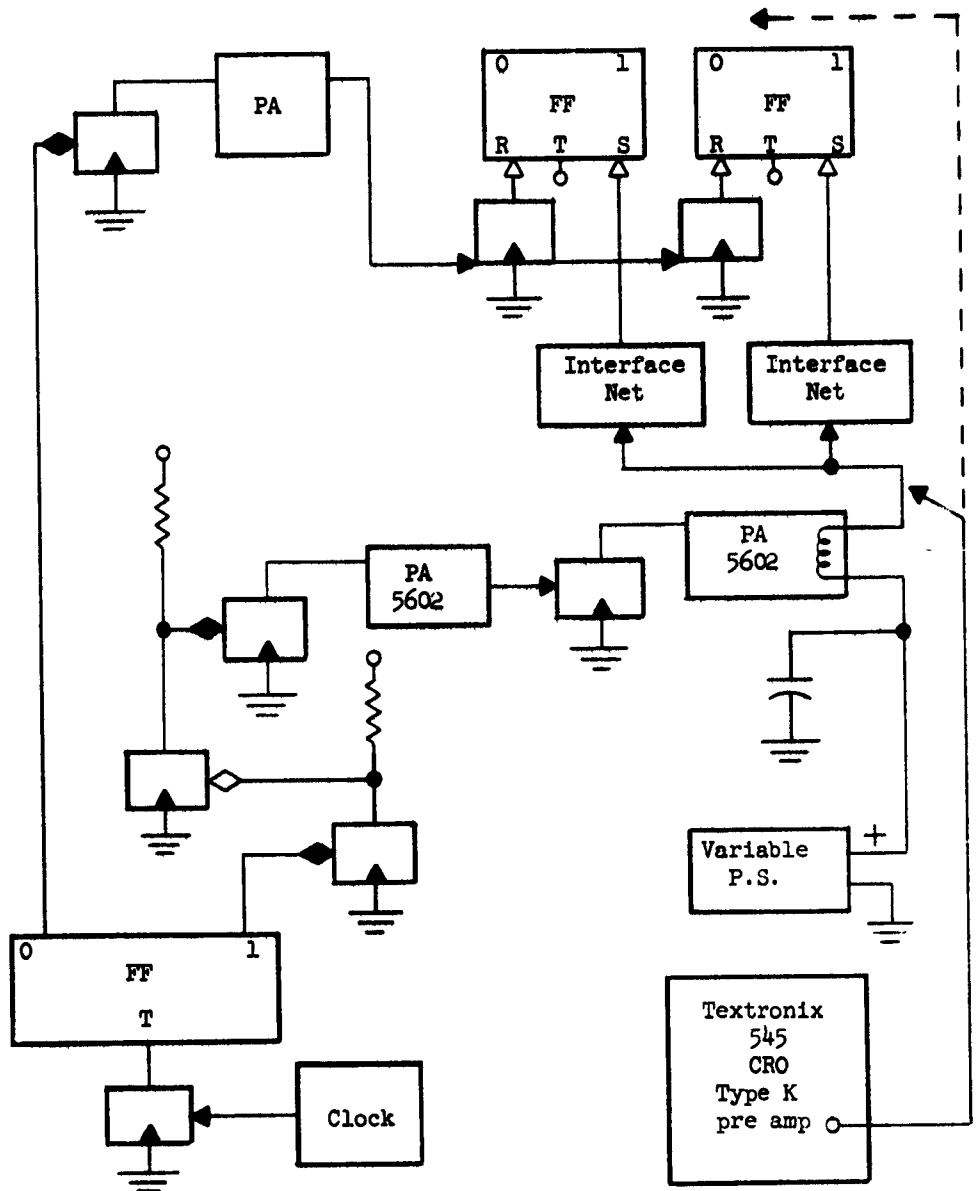
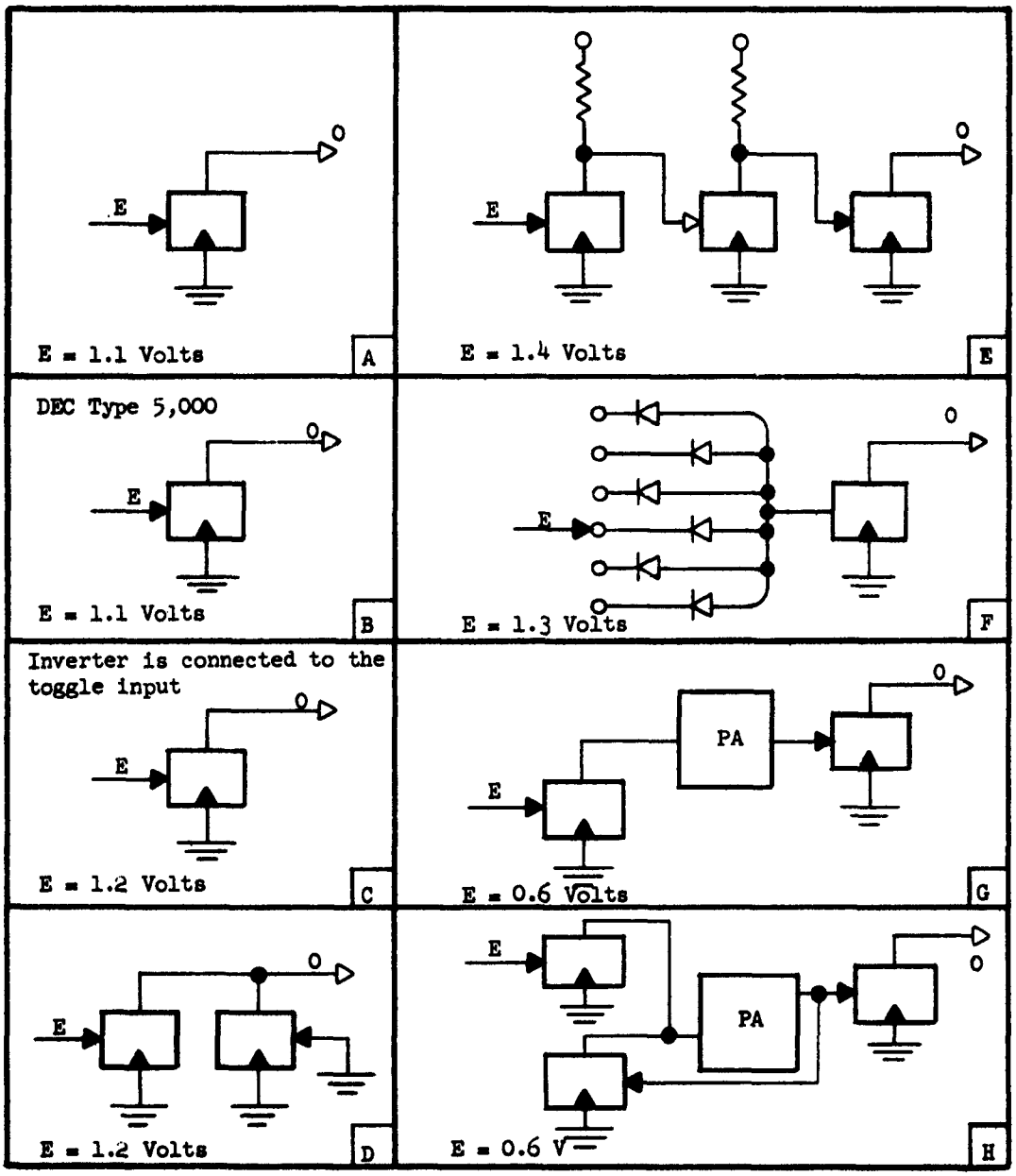


Figure 11 Interface Network Test



E is the minimum pulse amplitude from ground that will reliably trigger the flip-flops.

Figure 12 A-H Interface Networks

10 April 1963

TM-1166/224/00

Distribution List

B. O. Barancik	2110A
P. O. Bemis	8633
J. Brosal	29025
L. Gallenson (5)	1815
L. H. Guthrie	29025
J. N. A. Hawkins	29026
J. Hopper	27020
R. G. Leitner	29012
S. L. Lessler	20021
D. B. Manning (15)	20028
W. K. Overturf	29020
M. H. Selman	29012
R. von Buelow	1815
C. F. Wills	20024

UNCLASSIFIED

System Development Corporation,
Santa Monica, California
COMMAND SYSTEMS DEPARTMENT CRT
OSCILLOSCOPE DISPLAY.
Scientific rept., TM-1166/224/00,
by C. F. Wills. 10 April 1963,
55p., 12 figs.
(Contract ARPA SD-97)

Unclassified report

DESCRIPTORS: Programming (Computers).
Display Systems.

UNCLASSIFIED

Reports that the System Development Corporation's Engineering Department has assembled an experimental display system to be used with the AN/FSQ-32 Computer. Describes system requirements, design considerations and detailed logic design of the display buffer and associated components. Furnishes alignment and calibration procedures.

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