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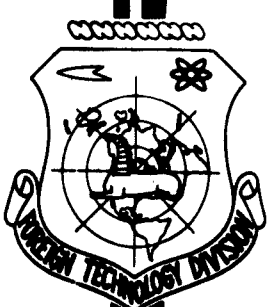
# TRANSLATION

BINARY PARALLEL SUMMATOR WITH THROUGH TRANSFER

By

L. P. Afinogenov and V. G. Kolosov

## FOREIGN TECHNOLOGY DIVISION

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# UNEDITED ROUGH DRAFT TRANSLATION

BINARY PARALLEL SUMMATOR WITH THROUGH TRANSFER

BY: L. P. Afinogenov and V. G. Kolosov

English Pages: 4

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PREPARED BY:

TRANSLATION DIVISION
FOREIGN TECHNOLOGY DIVISION
WP-AFB, OHIO.

# Binary Parallel Summator with Through Transfer

By

L. P. Afinogenov and V. G. Kolosov

We know of binary parallel summators with through transfer utilizing the impedance principle of ferrite work, consisting of paraphase ferrite registers of the first and second addends, connected with census bus-bars for the realization of the logical function of addition according to a "two" modulus with summator ferrites, and census bus-bars, the state of which for obtaining a sum in a given place, transfer and its inversion in the following place passes through the ferrites of the register of the sum and is connected with the inversed and direct yield of the transfer of the preceeding place.

In the summator being described, the realization of the impedance principle of ferrite work is distinguished from what is known by the fact that we introduce compensation bus-bars which insure the census of units and the ferrite needed with simultaneous notation of zero in the remaining (non-working) ferrites.

The described binary parallel summator insures addition and subtraction of two binary digits simultaneously in all places.

The principal place diagram of the binary parallel summator with through transfer is shown in the figure.

Ferrites 1--4 constitute one place of the summator, ferrites 5, 6 -- one place of an algebraic sum, ferrites 7, 8 -- the place of the register of the first addend and ferrites 9, 10 -- the place of the register of the second addend. Addends a and c are given in direct code. The work of the circuit in simultaneous summation takes place in four cycles.

In the first cycle, addend a, given at input 11, is recorded in the register of the first addend (ferrites 7, 8), and addend c, given at input 12, is recorded in the register of the second addend (ferrites 9 and 10). In the second cycle the pulse of the current is given at input 13. Depending on the state of the ferrite of the registers of the addends this pulse passes to bus-bars 14, 15 or 16, reversing the magnetism of the corresponding ferrites of the summator, in addition the pulse of the current not only has its magnetism reversed to state "1" of the corresponding ferrite, but the "0" state is also recorded in the remaining ferrites.

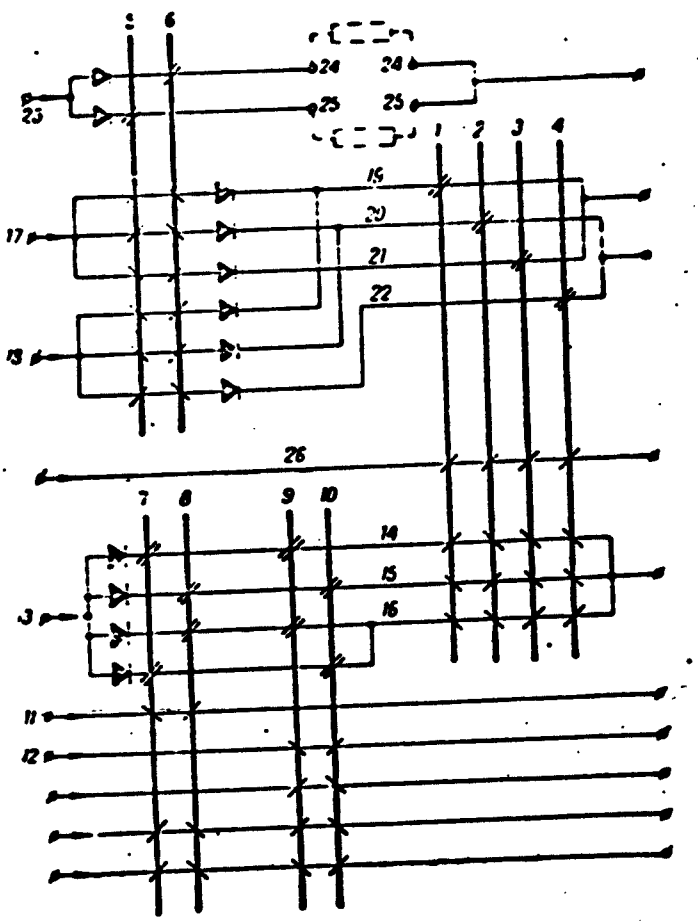
In the third cycle the pulse enters input 17 or 18 depending on the presence or absence of a transfer from the previous place. Depending on the state of the ferrites of the summator the pulse is commuted to bus-bars 19, 20, 21 or 22, recording the corresponding information in the sum register (ferrites 5, 6).

In the fourth cycle we are given a pulse of sum subtraction at input 23. Information corresponding to the state of ferrites 5 and 6 is taken from the output terminals 24 and 25. For improving the amplitude of spurious pulses through the windings of the barrier ferrites of the summator and enlarging the work reliability of the circuit, a compensation bus-bar 26 is introduced.

## Object of invention

A binary parallel summator with through transfer, utilizing the impedance principle of ferrite work, composed of paraphase ferrite registers of the first and second addends, connected by census bus-bars for realization of the logical function of addition according to the "two" modulud with ferrites of the summator, census bus-bars the states of which for obtaining sums in a given place, the transfer and

and its inversion in the following place pass through the ferrites of the sum register and are connected with the inversed and direct output of the transfer of the preceeding place, are distinguished by the fact that for the purpose of enlarging the reliability, through the ferrites of the registers and the summator pass compensation bus-bars.



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