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THEORETICAL AND EXPERIMENTAL RESEARCH TO ASSIST IN  
PREPARATION AND DESIGN OF A HIGH FREQUENCY SILICON  
CARBIDE ACTIVE DEVICE

H. C. CHANG, Principal Investigator

FINAL REPORT

Contract AF 19(604)-8499

December - 1962

Project 4608

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AIR FORCE CAMBRIDGE RESEARCH LABORATORIES  
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by H. C Chang, Principal Investigator

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# Abstract

✓  
For an active device to be usable at temperatures in excess of 500°C, it is necessary that the base material have a large band gap. Of the ~~presently known semiconductors~~, <sup>SiC</sup> ~~silicon carbide~~ appears to be the most feasible material for use as a high-frequency device capable of operation at elevated temperatures.

A unipolar transistor structure has ~~been~~ investigated since a field effect device most nearly fits the peculiar capabilities of ~~silicon carbide~~. <sup>SiC</sup> .

The device requirements are stringent and require a large degree of control over the crystal junction structure. This control is best effected by the epitaxial growth technique. ~~An epitaxial growth reactor has been fabricated and epitaxial layers have been grown on hexagonal silicon carbide seed crystals. The best layers have been shown to possess a high degree of crystalline perfection and are quite pure.~~ <sup>SiC</sup>

A study of the diffusion technique <sup>SiC</sup> ~~has been carried on~~. By varying the various diffusion parameters, the usual complementary error function behavior of the diffusion front ~~has been changed~~.

To fabricate these junction crystals into an operating device required a ~~refinement in the usual lapping, etching and contacting techniques~~. ✓ A gaseous etching technique is described which produces etched surfaces with a uniformity and smoothness previously unattainable. When used in conjunction with various masking techniques, this method appears to be feasible in the production of an active device structure. ✓

Theoretical and Experimental Research to Assist in Preparation  
and Design of a High Frequency Silicon Carbide Active Device

## 1.0 INTRODUCTION

The purpose of this investigation is to develop techniques which indicate the feasibility of fabricating an active silicon carbide device for operation at a frequency of 1 megacycle and at temperatures up to 500°C.

The extreme environmental conditions experienced in aerospace and nuclear research and development have made it mandatory to develop active devices of high performance under severe conditions. Silicon carbide (hereafter SiC) suggests itself for these applications due to its wide band gap. Also SiC is believed to suffer less radiation damage than other currently used semiconductors, and there should be a certain amount of annealing of radiation damage when operated at temperatures of 500° or higher.

The work covered in this report period has been largely devoted to technique development rather than production of an operating device. A firm foundation in the procedures required to prepare active devices must precede the actual fabrication and application of a silicon carbide transistor.

Although device fabrication was not emphasized during this report period, a device structure was designed, so that the fabrication problems in the production of an active element could be better understood. Previous reports have suggested that the unipolar transistor would be the most feasible structure.<sup>(1,2,3)</sup> In this type of device, minority carrier lifetime is of secondary importance. However, because of the high frequency requirements not only the dimensions of the proposed device are quite small, but the fabrication tolerances are extremely close.

For example, the pinch-off voltage, the half-channel thickness and the crystal purity are related by:

$$W_0 = \frac{a^2 N}{2Kq} \text{ where } W_0 \text{ is the pinch-off voltage in volts, } a \text{ the}$$

half-channel thickness in microns and  $N$  the net ionic impurity concentrations in the depletion region. Half-channel thicknesses of 2-20 microns and impurity concentration of  $10^{14}$  -  $10^{16}$  are reasonable experimental values but lead to a somewhat high pinch-off voltage of 20-25 volts. The fabrication of a device capable of operating at  $500^\circ\text{C}$  with such tolerances is expected to be difficult.

The above analysis requires abrupt junctions and a thin high-purity layer together with a close control over the geometrical specifications. The most promising technique to meet these requirements is vapor phase epitaxial growth by the chemical reaction of silicon and carbon containing compounds.<sup>(1,2,3)</sup> This method should have the advantages of easily purified and used starting materials, ease of doping and control of doped growth layer and the lower growth temperature. The latter is especially important since at the temperatures ( $\sim 2500^\circ\text{C}$ ) generally used to grow SiC, diffusion occurs and limits the abruptness of the junction. Therefore, the work reported here is concentrated on a method of thermal reduction, that is, the reacting carbon tetrachloride and silicon tetrachloride with  $\text{H}_2$  at much lower temperatures (in the vicinity of  $1900 - 2000^\circ\text{C}$ ) at the surface of a SiC seed. It is expected that diffusion problems at these temperatures will be considerably reduced.

Studies on the solid state diffusion of impurities into silicon carbide were also required. Although such diffusion studies have been reported previously, the tolerances required in this particular device require refinement of the techniques in order to improve the control both on the junction profile and on the depth of the junction. Studies were also initiated to investigate the feasibility of varying the usual error function junction-profile by varying the parameters during the diffusion.

A large number of problems concerned directly with the final fabrication of the device have been investigated. First there is the difficulty of providing good electrical contacts to SiC capable of operating at junction temperatures above  $500^\circ\text{C}$  and still providing chemical



inertness and electrical stability. A number of subsidiary problems connected with the contacts have been investigated, such as contact geometry and methods of limiting the contact area. Although methods of etching SiC were known prior to the start of this investigation, such etching procedures were known to have insufficient precision for this device, therefore considerable etching work was required. As a final step in the attack of this problem high temperature encapsulations would have to be investigated.

Scientific Report No. 1 and 2<sup>(2)</sup> and Scientific Report No. 3<sup>(3)</sup> on this contract have shown some of the progress made in these areas. In order to obtain good epitaxial films of SiC at comparatively low temperatures, several epitaxial growth reactors have been built and modifications made on them. These reactors are described in more detail later in this report. The gas flow pattern through these reactors has also been studied and altered. The importance of surface preparation was realized early and a detailed lapping and etching program was set up to obtain a suitable surface for epitaxial growth. Previous reports<sup>(2,3)</sup> have given the determination of the growth rate versus temperature.

Outlines of the basic investigations into multi-step diffusion were given earlier<sup>(2,3)</sup>, and the results have indicated that this procedure may lead to better control of the diffusion process.

A tentative device structure has been designed which incorporates the geometrical and electrical requirements of the SiC unipolar transistor. This has been described earlier<sup>(2,3)</sup> along with a number of improved fabrication techniques.

A new precision lapping system was devised and the first investigations on the use of metal masking during molten-salt etching were started. Furnaces have been built for the contact fusion of gold based alloys. These alloys have been previously investigated and were found to produce ohmic contacts to SiC.

At the writing of this final report, we have established that improvements on previously existing technology are feasible. These new

techniques are expected to provide the foundation necessary to produce the device required. Although devices have not been made to date, the techniques developed and reported herein should enable production of the required devices in the foreseeable future, provided that sufficient further effort be devoted to this end.

## 2. Epitaxial Growth of Silicon Carbide

### 2.1 General Discussion

Previous reports<sup>(2,3)</sup> on the epitaxial growth of silicon carbide showed the possibility of growing layers of cubic silicon carbide on a hexagonal silicon carbide substrate. These layers were structurally imperfect because of what we have called "mosaic defects". These defects may be described as islands growing out about 2500Å higher than the main surface of the epitaxial layers. Various changes in the experimental conditions were made but all failed to control the occurrence of these defects. There might be fundamental difficulties in growing cubic SiC (layer stacking ABC ABC) of high perfection on a hexagonal 6H SiC (layer stacking ABC ACB) substrate because of the phase difference between the grown layer and the substrate.

These difficulties could be avoided by growing crystals on a substrate of the same phase. The growth temperature was raised in order to attempt to grow an epitaxial layer of hexagonal silicon carbide.

Initial experiments were discouraging. At substrate temperatures of 1800°C\* no growth occurred and etching of the substrate surface occurred. At substrate temperatures of 1750°C a mixture of cubic and hexagonal silicon carbide grew and the perfection of the layer was poor. A more careful study of the growth mechanism was clearly indicated.

### 2.2 Experimental

#### 2.2.1 Apparatus

The apparatus used for the experiments was essentially that described in the previous scientific reports on this contract<sup>(2,3)</sup> and is reproduced for clarity here. As figure 2.1 shows the reactor is a water cooled quartz tube held vertically. Inside is a graphite block

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\*This temperature, as all other temperatures obtained with a pyrometer, is brightness temperature. Corrections for the light adsorption in the quartz reactor and the emissivity of the sample surface would place the true temperature 100-150°C higher.

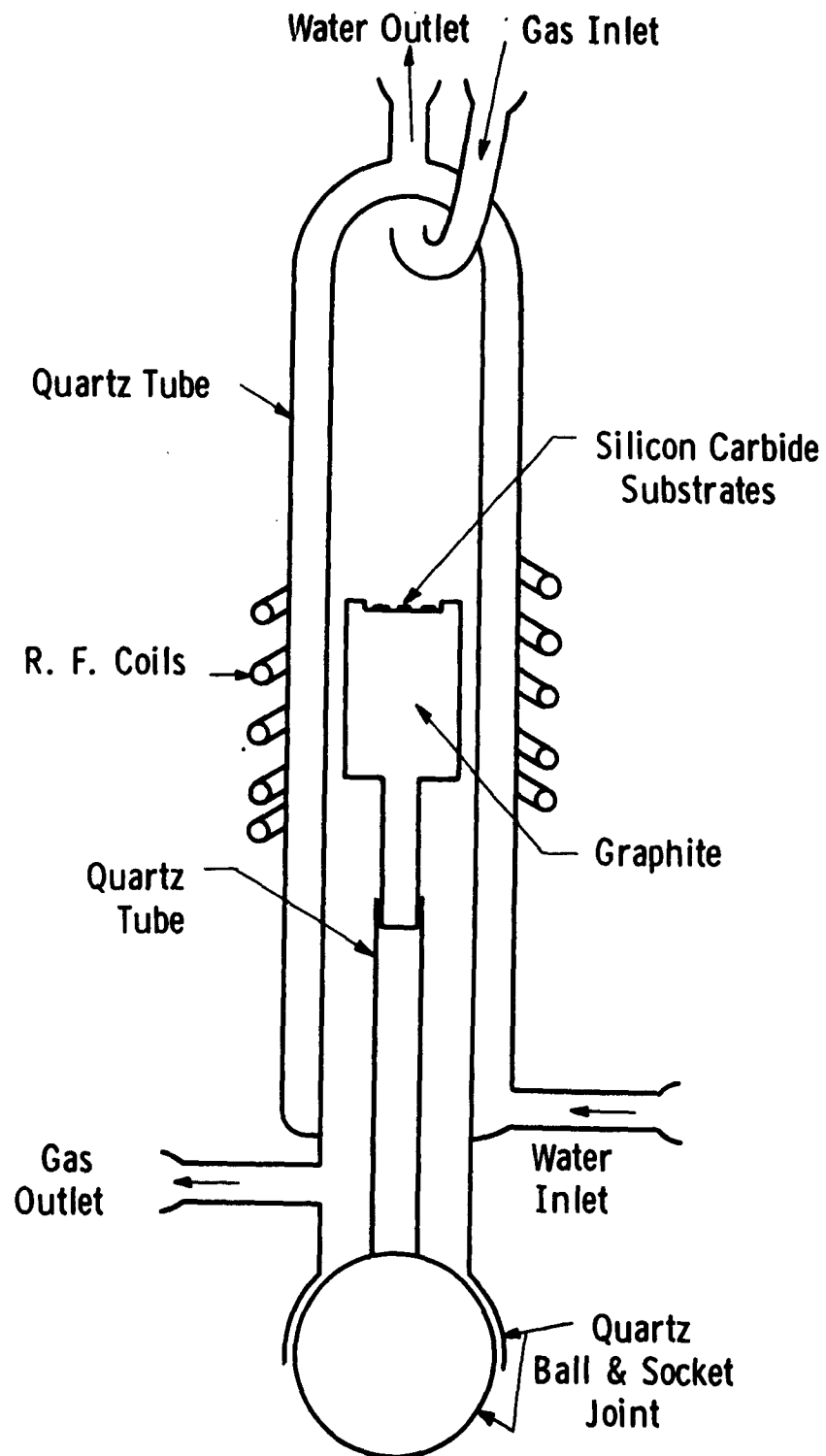


Diagram of epitaxial growth reactor

Fig. 2.1

susceptor mounted in a quartz holder. The SiC substrates are placed on top of the graphite block. Suitable provisions are made for admitting the reactant gases.

#### 2.2.2 Cubic Layers Obtained on Hexagonal Silicon Carbide

In this experiment a SiC crystal was divided into two pieces and cleaned in hydrofluoric acid followed by a methanol rinse. The two pieces were then dried and placed on the graphite heater such that the faces to be grown on were of opposite orientation or polarity, i.e., one was the "silicon" face and the other was the "carbon" face. Figures 2.2 and 2.3 show the surfaces of the grown layers. It was evident that the faces grew differently and it may be assumed that Figure 2.3 shows the growth on the "carbon" face.\* To prove this assumption another crystal was cleaved into two pieces. One piece was etched in molten salt to determine the "carbon" face and thus the polarity of the unetched piece was established.

The unetched "carbon" face was grown on and the growth surface obtained is shown in Figure 2.4. The similarity between Figures 2.3 and 2.4 tends to confirm our previous assumption.

#### 2.2.3 Effect on the Cubic Layer of the Variation of the $\text{SiCl}_4$ to $\text{CCl}_4$

##### Molar Ratio

In normal experiments the molar ratio of  $\text{SiCl}_4$  to  $\text{CCl}_4$  is 1 to 1. This ratio is maintained by control of the flow of hydrogen as gas through the two halide saturators. The increase in molar ratio from 1:1 to 2:1 and to 4:1 was achieved by increasing the flow through the silicon halide saturator.

---

\*The two faces, perpendicular to the "c" axis, are identified as "silicon" and "carbon" faces. The correspondence of these two faces to a silicon carbide crystal has not been proven, however, arbitrarily the rough face obtained after molten salt etching has been designated the "carbon" face.



Fig. 2.2 Layer grown on one face  
a of a divided silicon carbide  
substrate Run 77 230X

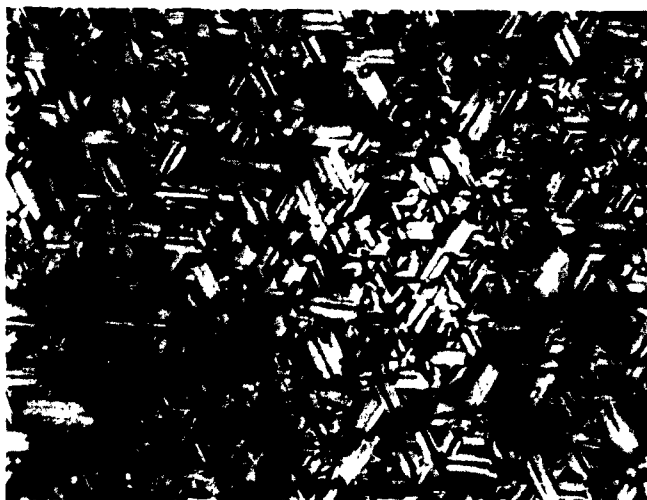


Fig. 2.3 Layer grown on opposite  
face of the other half of the  
silicon carbide substrate Run 77  
230X



Fig. 2.4 Layer grown on a "carbon  
face" Run 78 230X

Because the by-pass hydrogen constitutes the bulk of the gas flow, changing the flow through the  $\text{SiCl}_4$  saturator has little effect on the total gas-flow pattern in the reactor. Figure 2.5, 2.6 and 2.7 show no significant differences. These are the normal mosaic surfaces of the grown layer.

#### 2.2.4 Cubic Silicon Carbide Layers Grown at Fast Growth Rates

A number of experiments were run at accelerated growth rates to determine the effect of this variable on layer perfection.

In these experiments the usual hydrogen gas flow was maintained through both saturators but the temperature of the saturators was increased from  $0^\circ\text{C}$  to  $25^\circ\text{C}$ . The vapor pressures of silicon tetrachloride and carbon tetrachloride are trebled in this temperature range. Figures 2.8 and 2.9 show the surface after growth for 30 minutes at  $1700^\circ\text{C}$ . Figures 2.10 and 2.11 show the surface after growth for 5 minutes. The rate of growth was 1 micron per minute. (Since the top surface of the layer was very irregular, this rate of growth figure is not precise.) In both experiments the surfaces were covered with separated single crystals of cubic silicon carbide. The (111) faces of these crystals were parallel to the (0001) plane of the substrate, as expected for oriented growth, and were oriented in parallel or anti-parallel directions to each other.

Figures 2.12, 2.13, 2.14 and 2.15 show the surface at four times normal growth rate after growth for about one minute. The layer thickness was not measurable and was probably much less than one micron. It may be seen that in Figure 2.15 there are numerous small nuclei. Figure 2.13 gives the clearest indication that the nuclei were not formed randomly but are on helical circles.

#### 2.2.5 Mechanically Polished Substrates

- The work reported in the previous paragraph suggested that nucleation of the first-deposited SiC was occurring at spiral steps in the surface. These steps have been seen in some crystals and are expected to exist in all crystals if the Frank Theory of crystal growth holds.<sup>(9)</sup> This multiple nucleation would tend to produce a very imperfect layer.



Fig. 2.5 Run 79 (115X)  $\text{SiCl}_4$   
Ratio 1 to 1

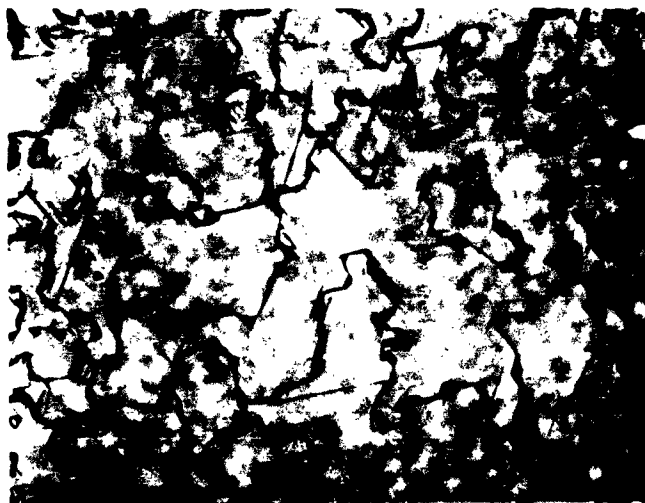


Fig. 2.6 Run 82 (115X)  $\text{SiCl}_4$   
Ratio 2 to 1



Fig. 2.7 Run 84 (115X)  $\text{SiCl}_4$   
Ratio 4 to 1





Fig. 2.8 Grown surface of silicon carbide layer, grown for 30 mins. at four times normal growth rate Run 81 (65X)



Fig. 2.9 As Fig. 2.7 Run 81 (115X)

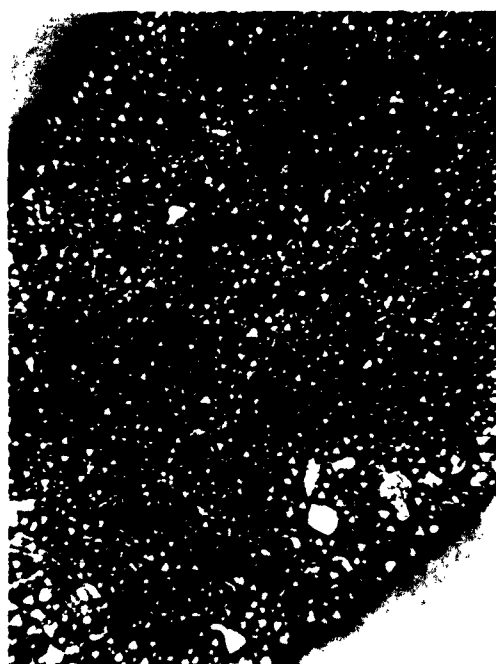


Fig. 2.10 Grown of Silicon carbide layer, grown for 5 mins. at four times normal growth rate Run 83 (65X)

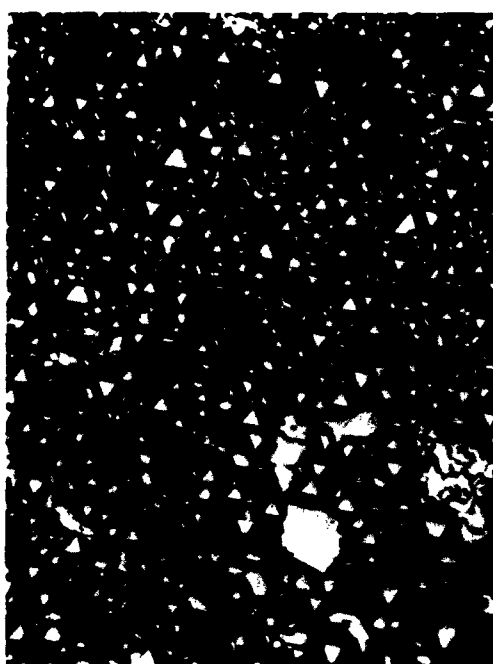


Fig. 2.11 As Fig. 2.9 Run 83 (115X)



Fig. 2.12 Growth surface of silicon carbide layer, grown for 1 minute at four times normal growth rate Run 85 (65X)



Fig. 2.13 As Fig. 2.11 Run 85 (115X)



Fig. 2.14 As Fig. 2.11 Run 85 (230X)



Fig. 2.15 As Fig. 2.11 Run 85 (600X)

A series of experiments were performed, in which the "silicon" face was carefully lapped to remove these spiral steps.

The substrates for these experiments were etched in molten sodium peroxide/sodium hydroxide to reveal the "silicon" face, which was then polished successively on 6 and 0.25 micron diamond powder. Following polishing, the substrate was rinsed in HF, and then in methanol. After drying, the substrate was placed on the graphite heater. A number of runs were made to determine the optimum value of the reaction parameters. The temperature of the substrate must be maintained very close  $1750^{\circ}\text{C}$  ( $\pm 20^{\circ}\text{C}$ ) in order to grow a layer of good crystalline perfection. The gas flow conditions for growth were as follows: total hydrogen  $4 \times 10^{-2}$  gram moles per minute;  $\text{SiCl}_4$  and  $\text{CCl}_4$  -  $1.4 \times 10^{-4}$  gram moles per minute.

Figures 2.16 to 2.19 show the results obtained for Run 87L. Figure 2.16 shows the surface of part of the substrate after diamond polishing. The internal crescent-shaped defect was present in the substrate crystal before polishing. Figure 2.17 shows the growth that took place in the same part of substrate. This growth was hexagonal silicon carbide, since in etching hexagonal etch pits were revealed as is seen in Figure 2.19. Figure 2.18 shows the normal growth on an undamaged portion of the seed.

Figures 2.20 and 2.23 show the surfaces of growth obtained in Run 93. Figure 2.20 shows the surface of growth on an etched substrate while Figure 2.21 shows the surface of growth on a diamond-polished substrate. The improvement in the grown layer using the polished substrate is easily seen.

Figure 2.22 shows the surface of diamond-polished substrate which was not polished towards one edge. Figure 2.23 shows the growth that took place in the same area. It is seen that defective growth spreads out beyond the original defective area.



Fig. 2.16 Substrate 87L after polishing, notice defect in center 115X



Fig. 2.17 Surface after growth Run 87L 115X

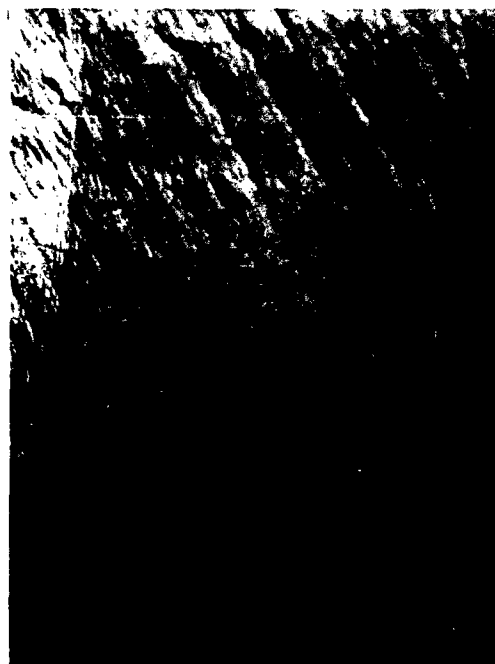


Fig. 2.18 Best used surface after growth Run 87L 115X

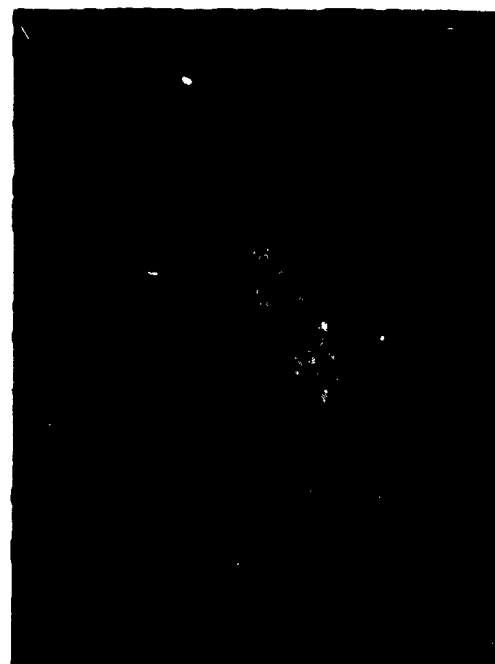


Fig. 2.19 Grown surface Run 87L after etching for 1 1/2 mins. in molten  $\text{Na}_2\text{O}_2/\text{NaOH}$  115X



Fig. 2.20 Grown Surface on etched  
substrate Run 93E (115X)



Fig. 2.21 Grown surface on polished  
substrate Run 93PL (230X)



Fig. 2.22 Surface of substrate, S90L,  
not polished towards crystal edge (115X)



Fig. 2.23 Grown surface on substrate  
S90L Run 90L (115X)

Figure 2.24 shows the damaged area of a substrate which had been diamond polished and then etched in molten sodium peroxide. Etching has revealed the dislocations (presumably caused by the inclusion seen as the heavy black area in the photograph) and also scratches due to polishing. Figure 2.25 shows the surface of the same area after growth, and it is seen that the grown layer has nearly covered the defect. Figure 2.26 shows the surface of the growth taking place on an undamaged area of the substrate.

#### 2.2.6 Growth of Phosphorus-Doped Hexagonal- and Cubic-Silicon Carbide Layers

Phosphorus is expected to be a donor impurity when incorporated into the SiC lattice. There was considerable question, however, if the phosphorus could be conveniently introduced into the growing layer. A volatile P compound might be added to one of the gas saturators but the compound might never reach the growing SiC interface before it was decomposed and lost to the process.

In this experiment the silicon tetrachloride was doped with about ten parts per million  $\text{PCl}_3$ . The substrate used was p-type aluminum-doped silicon carbide. Preliminary results have proved that this layer was n-type and that there was a rectifying junction between the layer and the substrate. Since our process usually produces a p-type layer when the starting materials are not deliberately doped, phosphorus does appear to be incorporated under these conditions.

#### 2.2.7 Properties of Cubic and Hexagonal Layers

The thickness of the grown layer has been determined either by bevelling at a 5 degree angle or by scribing and breaking. Figure 2.27 shows an example of the latter technique. The difference between cubic and hexagonal layers was shown by etching in molten 3:1 sodium hydroxide to sodium peroxide mixture. Figure 2.28 and 2.29 shows the surfaces of an etched cubic layer, and an etched hexagonal layer respectively.

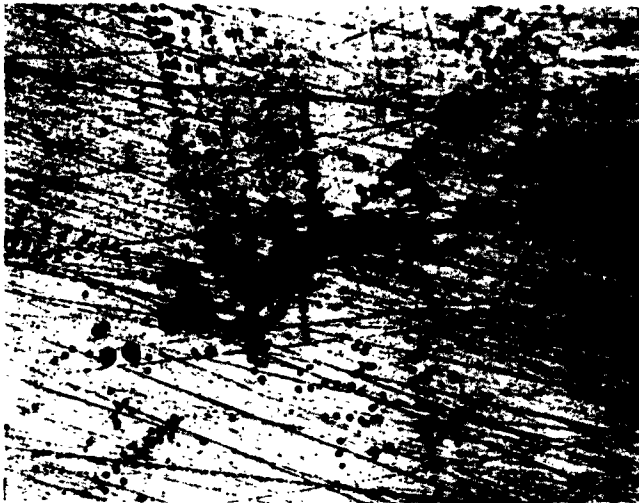


Fig. 2.24 Substrate S94DE polished and etched showing surface of damaged area (115X)



Fig. 2.25 Growth surface on damaged area of substrate S94PE Run 94PE (115X)

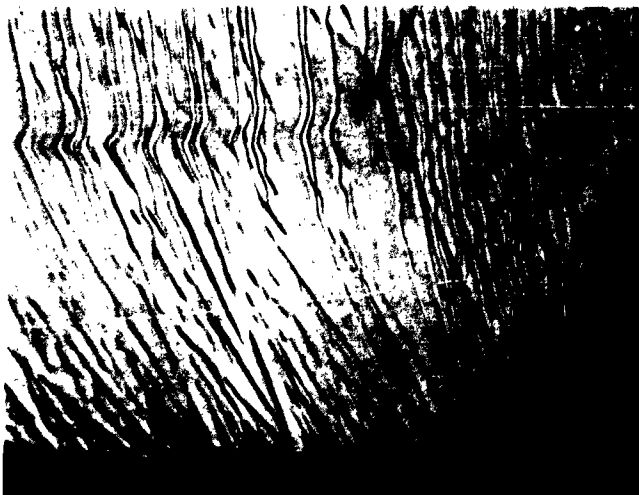


Fig. 2.26 Growth surface on undamaged area of substrate S94PE Run 94PE (115X)

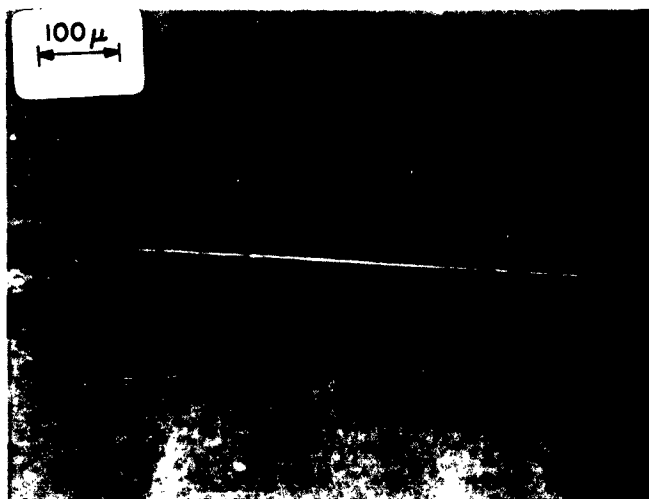


Fig. 2.27 Cross section showing layer and substrate 115X

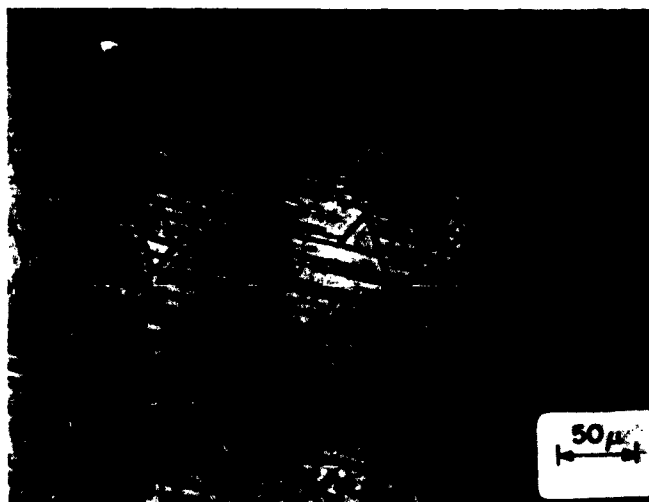


Fig. 2.28 Surface of etched cubic layer 230X



Fig. 2.29 Surface of etched hexagonal layer 230X



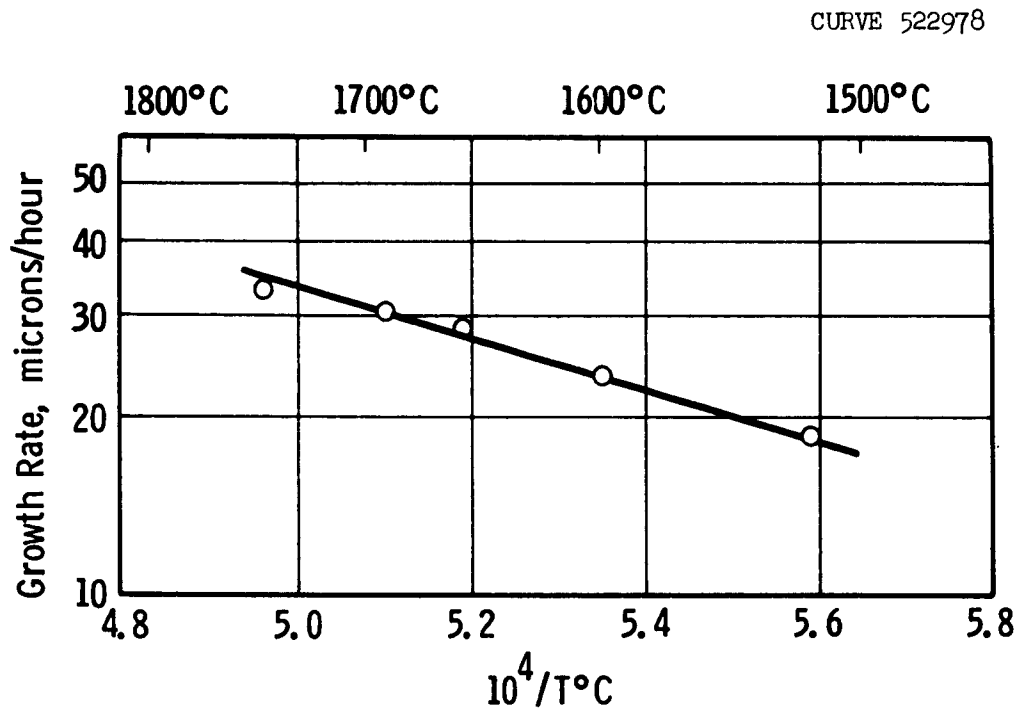
Figure 2.30 shows the variation in growth rate with temperature. It may be noted that the growth rate for the hexagonal layer grown at  $1750^{\circ}\text{C}$  fits the straight line obtained for the growth rate of cubic layers at lower temperatures.

X-ray information obtained either by back reflection or transmission techniques showed that the grown layers were single crystal but did not indicate if the layer was cubic or hexagonal since the substrate reflections interfere.

The electrical properties of the hexagonal layers are described in full detail in Section 5. The layers produced from starting materials which were not deliberately doped have shown p-type conductivity and were of high resistivity. It has been found that a Schottky-type metal-semiconductor rectifier can be made by evaporating a noble metal onto a thin high-purity layer. It has been possible to estimate the approximate concentration of active impurities in the epitaxial layer by measuring the variation in the capacitance of the barrier with the applied reverse voltage at room temperature. The purity of the layers found by this method has been between  $10^{14}$  to  $10^{16}$  carriers per cc. There is some evidence that the concentration of carriers in the layer may be dependent on the purity of the substrate, which would suggest that some diffusion of impurities from the substrate into the growing layer took place.

### 2.3 Discussion of Results

It was shown that there is a marked difference between growth obtained on the "silicon" and "carbon" faces. This result may be compared to the difference seen on etching these two faces.<sup>(4)</sup> The latter difference is believed to be due to the slight ionic character of the silicon-carbon bond, which, because of the orientation of silicon-carbon dipoles in layers, makes the silicon face positively charged with respect to the carbon face. It is possible that the difference observed in growth on the two surfaces is due to greater surface energy on the silicon face because of the greater stability of the bonds within the



Temperature dependence of silicon carbide growth rate

Fig. 2.30

"carbon" face compared to the bonds in the "silicon" face.<sup>(12)</sup>

It is interesting to observe that the growth obtained on the "carbon" face is similar in appearance to that observed in the growth of a silicon layer onto an oxide-coated silicon surface.<sup>(5)</sup> In the latter growth, the presence of oxide interferes with the formation of silicon-to silicon bonds.

The increase in the ratio of silicon tetrachloride to carbon tetrachloride from 1:1 (the usual ratio) to 4:1 showed no marked effect on the mosaic pattern of a cubic layer. There was also no significant change in the growth rate. This indicates that the  $\text{SiCl}_4$  concentration in the reactor is not a rate-determining parameter.\* Since graphite is present in the reactor,  $\text{H}_2$  transport will insure an excess of C. Therefore, it is probable the rate-determining parameter, at constant temperature is diffusion of the reactants across the boundary layer between the growing surface and the vapor phase.

The cubic growth obtained using fast growth rates at substrate temperatures of  $1700^\circ\text{C}$  gave valuable information. When the growth time was reduced to about 1 minute, the nuclei were seen to be forming in concentric circles. These are probably the edges of spiral growth steps on the surface of the substrate. Such edges would provide preferential sites for nucleation as has been found for the nucleation of ice crystals onto the surface of cadmium iodide crystal.<sup>(6)</sup>

Growth spirals are common on the surfaces of silicon carbide crystals but because of the small heights (e.g., A 6H silicon carbide spiral has a step height of  $15 \text{ \AA}$ ) they are visible only with the special

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\* Another key experiment would be to vary  $\text{SiCl}_4$  concentration so that the ratio of  $\text{SiCl}_4$  to  $\text{CCl}_4$  is less than 1. Also the concentration of  $\text{CCl}_4$  should be varied while the  $\text{SiCl}_4$  is kept constant. From the results of these experiments the determining factors in growth rate should be found.

optical techniques, such as phase contrast microscopy.<sup>(7)</sup> Therefore, more work is required to establish a direct connection between the pattern of the nuclei seen after growth for one minute and the growth spirals on the surface of the substrate. The perfection of growth was improved using a mechanically polished surface instead of using an etched surface. This would indicate that the latter surface contains defects that interfere with the growing of a good epitaxial layer.

The theories of epitaxial growth (and growth of crystals from the vapor) have been considered by many workers.<sup>(8-11)</sup> There are two current theories applicable to the growth of crystals from the vapor phase. The theory of Volmer, Becker and others depends upon the formation of a two-dimensional nucleus for the growth of a new crystalline layer. The theory of Frank and others postulates growth with help of a screw dislocation. The dislocation presents a self-perpetuating step at which growth takes place. It has been shown theoretically and experimentally verified that growth by the Frank mechanism is possible with much lower supersaturations than those required by the Volmer mechanism.

The theories on the mechanism of epitaxial growth by Mentzer, Engel, and Frank and van der Mewe<sup>(9)</sup> consider oriented growth of one crystal upon another. As in the theory of vapor growth, the most important problem is the formation of the initial nuclei.

In the case of silicon carbide, two types of nuclei, either of hexagonal or of cubic structure, are possible. Both structures have very similar lattice stabilities but the surface energy of the hexagonal structure is higher.<sup>(12)</sup> This higher surface energy accounts for the high temperatures (greater than 2000°C) normally required for the formation of hexagonal silicon-carbide crystals by the sublimation method. The quoted growth temperature 1750°C used in the present work is as noted the brightness temperature of the substrate. Such a temperature

is apparently high enough to grow epitaxial layers of hexagonal SiC by providing sufficient surface energy to stabilize hexagonal nuclei.

#### 2.4 Conclusions

It is shown in this report that hexagonal layers of silicon carbide of good perfection can be grown. Further work will be necessary to optimize conditions. The undoped layers grown have been of high purity and may be useful for fabrication of a metal-semiconductor rectifier. Preliminary work on doping the grown layer has been successful and further work is planned in order to prepare grown n-p junctions in the epitaxial layer.

### 3. Diffusion

#### 3.1 Introduction

Previous scientific reports<sup>(2,3)</sup> on this program have described the diffusion furnace. This furnace was designed so that the open tube - carrier gas technique could be used. A graphite heater, thinned at the center to permit a higher and more uniform temperature, was used to heat the crystals. The temperature was controlled to  $\pm 2^{\circ}\text{C}$ .

In order to produce as uniform diffusion front as possible, crystal surface must be carefully prepared. A lapping, etching and polishing technique is used for this purpose<sup>(3)</sup>.

When heated to  $2000^{\circ}\text{C}$ , the silicon carbide crystals decompose at the rate of about 0.1 mil/hour. Thus, this decomposition rate may be as great as the diffusion process. To prevent the decomposition, an equilibrium atmosphere of the SiC-Si-C reaction is provided around the crystals by the use of granular SiC.

The crystals are held upright during diffusion in a slotted graphite holder which permits uniform exposure to the flowing gas carrying the diffusant<sup>(3)</sup>.

Junctions are prepared by the diffusion of aluminum into n-type (nitrogen-doped) SiC crystals. This produces a p-n-p structure with the p-region surrounding the n-type core. The distribution of diffused impurity across the junction region (varying from a graded to a nearly step distribution) is controlled by the diffusion process. In the case of the unipolar transistor, we are primarily interested in an abrupt junction and a narrow channel structure.

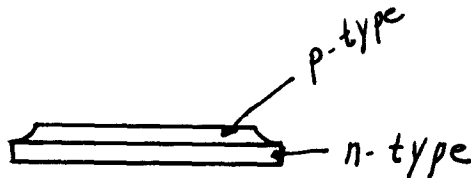
Before describing the diffusion techniques involved in producing the transistor structure, a brief outline of the desired results of the process should be reviewed.

From previous investigations it was found that the unipolar field effect design was the most feasible approach to the fabrication of a silicon carbide transistor. In this device the channel thickness is limited by the desired pinch-off voltage and the purity of the n-type silicon carbide. The pinch-off voltage in turn cannot be greater than

the breakdown voltage and may be further limited by leakage current of the diffused p-n junction. Since as pointed out in Chapter 1 the total channel thickness should be about 10-15 microns, the actual physical thickness of the crystal is limited to a maximum of about 3 mils. Crystals less than 3 mils in thickness are easily fractured and difficult to process.

A knowledge of the diffused junction depth is necessary so that further processing steps can be carried out, and in the case of fabricating a unipolar transistor, this depth should be known quite exactly. An electrolytic etching technique has been developed so that junction depths as shallow as 1-2 microns can be delineated. The procedure is to etch a small hole in the p-type layer using a point probe under forward bias in a dilute alcohol-HF bath. The etching will continue until the n-type material is reached. The junction depth can then be measured with a microscope. A similar experimental arrangement makes it possible to etch a mesa of p-type material on an n-type base.

A sketch of this is shown below.



### 3.2 Two Step Technique

In order to produce the desired thin channel thickness by diffusion from a thick crystal, a two-step process was considered. The first step is a deep diffusion with a minimum of control on the junction depth. The second step is diffusion into the narrow region of pure-n-material in the center. The crystals were initially thicker than 100 microns. The first

deep diffusion produced a p-n-p structure with a junction depth of about 50 microns. Each diffused crystal was examined to determine which junction had the best electrical characteristics. The poorer junction was lapped off and the crystal thinned so that about 20 microns of the pure n-type material was left. From the first diffusion experiment, an average diffusion rate for the crystals was established. This rate was then used to control the depth of second diffusion. The use of the average diffusion rate was justified, since within a given growth run the diffusion coefficient of the crystals were equal to within 5%. The second diffusion was then run to obtain the desired channel thickness.

The initial deep junction was formed by programming the diffusion temperature of the "infinite source method" or constant concentration of aluminum. The crystal temperature was controlled at 1950-1980°C for about 75% of the intended run time (about 30 hours). The temperature was then increased rapidly to 2100-2150°C and held constant for the remainder of the run. There is a strong temperature-dependence of the diffusion coefficient,  $D$ , and the change of  $D$  due to a 200°C increase in temperature is about one order of magnitude.

### 3.3 Results

Testing of the diffused junctions has shown that reverse currents on the order of microamperes are obtained with reverse voltages of 300 volts. The forward voltage is higher than on grown junction crystals due to the higher resistivity base material and a somewhat graded junction.

Crystals which had been diffused by the two step technique were processed into a transistor configuration, using the etching techniques described. However, even in the relatively short diffusion distances with the maximum amount of control of the junction depth, the channel region was overcompensated. In view of these results, this technique was deemphasized, since it appeared the epitaxial growth technique offered a greater feasibility of controlling the junction structure.



#### 4. Device Fabrication

##### 4.1 General Discussion

Theoretical studies, reported in Scientific Reports No. 1.-2 and 3<sup>(2,3)</sup> have shown that a small unipolar transistor with accurate dimensions is a favorable device design. Therefore, techniques which have been established for silicon have been modified for use with SiC. Evaporated metal contacts have been developed. In particular, the use of a Ta-Au contact has been highly successful. If desired, this evaporated contact can be alloyed into the SiC reproducibly, producing a uniform flat surface. During this report period, 1 mil Au wires have been successfully thermocompression--bonded to evaporated contacts.

##### 4.2 Metal Masks for Etching

The controlled etching small regions in the crystals is required to fabricate the high-frequency transistor. Although the chlorine-etch to be described in paragraph 4.3 is a significant advance in the art, a parallel effort has been devoted to methods of masking the already efficient  $\text{Na}_2\text{O}_2$ -NaOH etch. As mentioned in the last report,<sup>(3)</sup> the only masking material discovered to date is Zirconium (Zr). Although Zr is attacked by the salt etch, its relative inertness lends hope to the supposition that it can be used as an etchant mask. Calculations indicate that the Zr masking layer would have to be at least  $1\mu$  thick.

Three methods were investigated for the deposition of Zr on SiC substrates: (i) the evaporation of Zr metal under vacuum,<sup>(16)</sup> (ii) high temperature alloying of the metal to the substrate, and (iii) gaseous decomposition of the vapor of a compound containing the metal.

Evaporation of the metal (i) was attempted in a number of ways as listed in Table 4.1. Multiple filament evaporation achieved the thickest deposition ( $1.1\mu$ ). Patterns were etched in this film by masking portions with "Pyseal" and dissolving the exposed Zr in HF. Subsequent etching in molten  $\text{Na}_2\text{O}_2$  removed the remaining Zr but it left a faint pattern on the substrate. This result showed it might be possible to use Zr to mask

molten  $\text{Na}_2\text{O}_2$ . It also gave some validity to the assumption concerning the minimum deposit thickness. Some doubt still remains, however, whether Zr evaporated from a W filament is contaminated with W. The extent of this contamination (if present) has not yet been determined, but if W were present in the film, it very likely would render the film more susceptible to attack by the etchant. None of the other evaporation methods produced a film of sufficient thickness.

Table 4.1

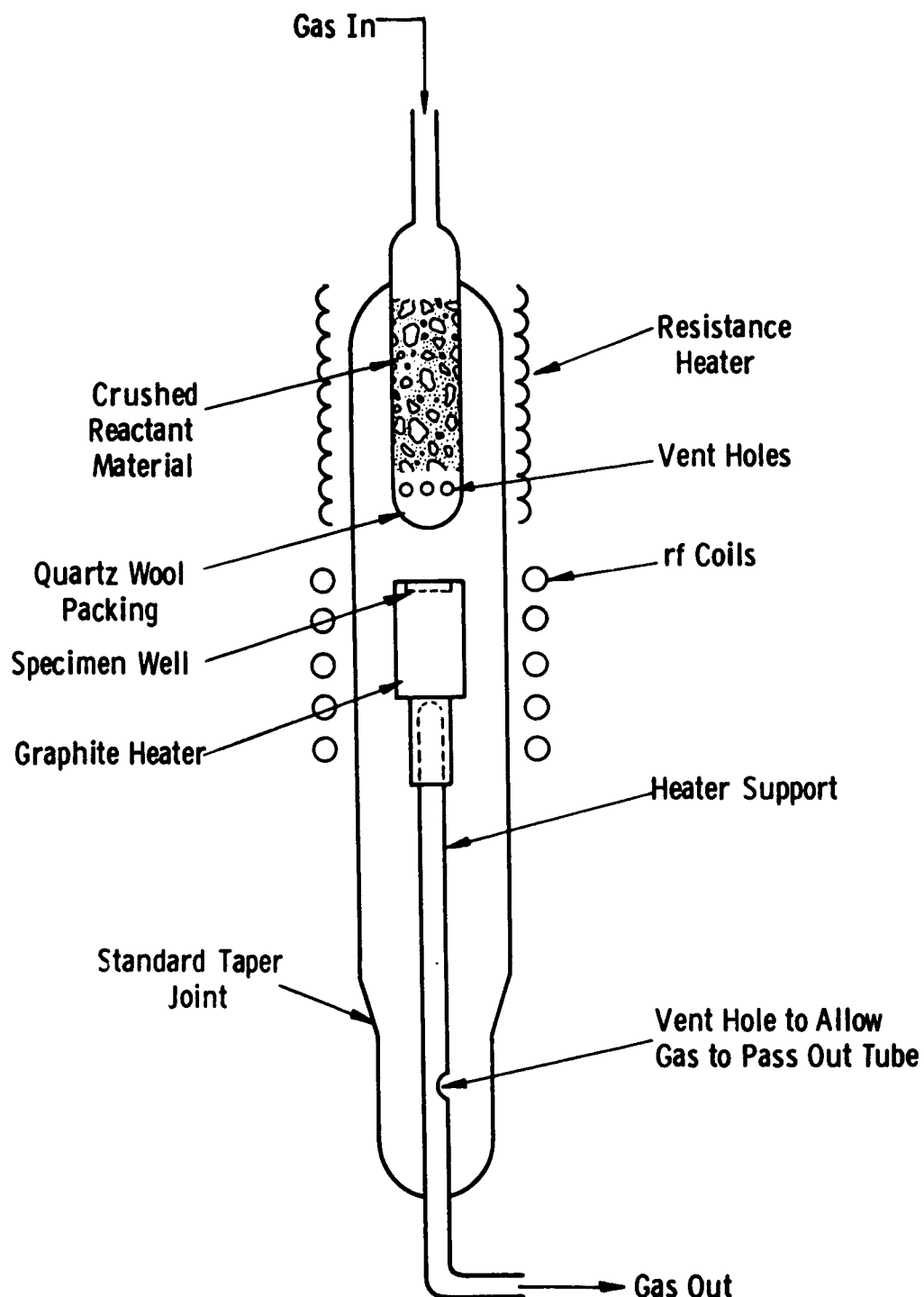
<u>Method</u>	<u>Source of Heat</u>	<u>Thickness</u>
Tungsten Filament, Single	Resistive Heating of Filament	0.2 $\mu$ or less
Tungsten Filament, Multiple	Resistive Heating of Filament	about 1.1 $\mu$
Zr Metal in $\text{ZrO}_2$ Crucible	Resistance Element Around Crucible	less than 0.2 $\mu$
Graphite Crucible	Electron Bombardment	less than 0.2 $\mu$
Pendant Drop on Zr Rod	Electron Bombardment	less than 0.2 $\mu$
Molten Zr Pool on Zr Rod supported by $\text{ZrO}_2$ Block	Electron Bombardment	*

\*The  $\text{ZrO}_2$  block shattered when heat was applied.

Two attempts were made to bond Zr to the SiC to the SiC by alloying (ii). A definite interaction between the Zr and SiC was detected, and in spite of excellent wetting of the SiC by the molten alloy, the solid Zr did not adhere well and it could be stripped from the surface with very little effort. This is thought to be due to differences in thermal contraction since the alloying temperature was in the 1800 to 2000°C range. Attempts to etch Zr-alloyed specimens in molten  $\text{Na}_2\text{O}_2$  showed that the alloy would resist the etchant and that the substrate was given somewhat more protection by the Zr in those regions in which the adhesion was better.

Gaseous plating is perhaps the most attractive method for depositing Zr on SiC (iii) Zr deposits produced by gaseous deposition are usually ductile, dense, smooth, and adherent. The temperature of deposition is low enough that one may hope to avoid the difficulties engendered by differences in thermal contraction. Zr is deposited gaseously by the thermal decomposition of  $\text{ZrI}_4$  at 1100-1300°C<sup>(17,18)</sup> or by displacement deposition from  $\text{ZrCl}_4$  at 1200°C on a suitable metal substrate.<sup>(10)</sup> The  $\Delta F^\circ$  values<sup>(15)</sup> for the pertinent chlorides ( $\text{ZrCl}_4$  - 57.5 K cal per mole per valence bond;  $\text{HCl}$  - 37.8 K cal per mole per valence bond; and  $\text{NaCl}$  - 91.8 K cal per moles per valence bond) suggest that  $\text{ZrCl}_4$  cannot be reduced by  $\text{H}_2$  but that one should be able to reduce it by Na vapor. These conclusions may not be valid at the actual reaction temperature since  $\Delta F^\circ$  values are defined at 25°C, but they are indicative.

The apparatus used is shown in Figure 4.1  $\text{Zr}$ ,  $\text{ZrI}_4$ , or  $\text{ZrCl}_4$  was put in the inner glass tube and reacted with or sublimed into a gas, Ar, containing  $\text{I}_2$  or  $\text{H}_2$  as the reaction required. The specimens were put in the well on the graphite element which was heated by an rf generator. Deposition was attempted by thermal decomposition or hydrogen reduction of  $\text{ZrI}_4$ . The  $\text{ZrI}_4$  was prepared in two ways. In the first three runs,  $\text{I}_2$  was sublimed into the carrier gas and passed through Zr sponge. The reacting Zr and  $\text{I}_2$  was heated in a closed tube for a long period of time. The product was quite impure. In one run, it was used as made and in the other run, it was further purified by sublimation. In only one of these runs was Zr deposited and then a very poor product was obtained. Table 4.2 gives data on the Zr deposition runs.



Apparatus for zirconium deposition

Fig. 4.1

Table 4.2

## Zirconium Gaseous Deposition Runs

Entry No. (11)	Run Time	Temperature		Reactant Materials	Remarks
		Resistance Heater	Graphite Heater		
36/2	2.5 hrs.	300°C	1650°C	ZrCl <sub>4</sub> +H <sub>2</sub>	No Zr
38/2	1 hr.	250-300°C	1400°C	Zr+I <sub>2</sub>	No Zr
38/4	about 2.5 hrs.	300-450°C in 50° increments over	1300°C	Zr+I <sub>2</sub>	Some very impure Zr deposited. Much reddish brown deposit on quartz. I <sub>2</sub> heated to 60-80°C.
39/3	about 2.5 hrs.	400°C	1300°C	Zr+I <sub>2</sub>	Reaction zone flooded with light, no Zr.
40/3	1.5-2 hrs.	400°C	1300°C	Crude ZrI <sub>4</sub>	No Zr, H <sub>2</sub> O droplets in inner quartz tube.
41/1	first hr. second hr.	300°C 400°C	1300°C 1400°C to 1500°C 1550°C	sublimed ZrI <sub>4</sub>	No Zr on speci- mens or heater or residue from ZrI <sub>4</sub> .

The results obtained in trying to deposit Zr are discouraging but they are included here since with a good commercial source of  $\text{ZrI}_4$ . This method may be useful. Preparing good material in a sufficient quantity would have required an extended investigation. Optimum conditions were not approached in any of the runs since in every run a large excess of  $\text{I}_2$  was present. This excess inhibited the reaction,  $\text{ZrI}_4 \rightarrow \text{Zr} + 2\text{I}_2$ . It is believed that with a purer  $\text{ZrI}_4$  and more effort, Zr that is thick enough and sufficiently adherent to be used as a maskant for  $\text{Na}_2\text{O}_2$  etching could be deposited by this method.

#### 4.3 Etching Studies

##### 4.3.1 General Discussion

A basic process in the fabrication of most semiconductor devices is that of controlled etching, i.e., an etching process which has a reproducible rate and is capable of being confined to specified areas. With the majority of semiconducting materials, these conditions are easily met by standardized methods. Silicon carbide, however, does not lend itself well to any of the standard techniques as it is a very inert substance, being attacked chemically by only a few etchants at elevated temperatures.<sup>(4)</sup> It can be electrolytically etched as discussed below but only if a supply of holes is available. With n-type SiC, the only effective hole supply is a forward-biased p-n junction. Due to these difficulties, the controlled etching processes for SiC which have been attempted in the past were not notably successful.

##### 4.3.2 Electrolytic Etching

Considerable research has been done on the electrolytic etching of SiC. Previous reports<sup>(1,2,3,4)</sup> give the details; therefore, only a summary will be given.

It has been shown that in reality there are two types of electrolytic etching encountered with SiC, (i) the etching of thick p-regions where the p-n junction plays no part. (ii) the etching of thin p-layers on thin n-material with the attendant difficulties brought on by the nearby

p-n junction. The former type has been used with standard masking techniques to produce patterns on substrates and to obtain deep etching with a minimum of lateral attack.<sup>(2)</sup> It is not very useful, however, since it cannot be used to prepare the needed active device structure. The latter type of electrolytic etching has been used most often. This p-n junction configuration in an active device is difficult to obtain because of the rate control problem.<sup>(3)</sup> n-type material will not etch unless it receives holes from an outside source. Therefore, as n-type material is exposed, the current which normally would be distributed over the entire area flows through the p-region that remains. This increases the current density on the p-region and, of course, the etch rate as well. This effect can cause the etch rate to increase exponentially. The use of standard masking techniques cannot be used with such etching as the mask would be undermined in a few moments. Both types of etchings are complicated in that the electrolytic etching of SiC is difficult to duplicate from specimen to specimen, due to differing physical properties of individual crystals.

A further important difficulty encountered is the "milky layer attack," a phenomenon in which the SiC is attacked but not completely dissolved. It appears that one atomic species is selectively removed from the lattice, leaving a mechanically unstable material. While a specimen is being etched, no change in the SiC is noted; but when removed from the solution and dried, certain regions appear milky. This milky region can be easily broken with a probe, which reveals a much larger attacked area than expected from the current density and time. That is, it appears to have a current efficiency greater than 100%. Some success in eliminating this phenomenon has been attained by changing the composition of the etchant, but the results have not been satisfactorily reproducible.

#### 4.3.3 Chemical Etching

Due to simplicity, a chemical method is attractive for etching semiconductors. Ideally, it is capable of etching both n-type and p-type

materials, it is not affected by the structure of the crystal, and it may be used with masks of various types to produce intricate patterns on the substrate. In SiC technology, two general methods of chemical etching (molten reagent etching and gaseous etching) are available; but the molten reagents fall somewhat short of achieving all the requirements above.

Sodium peroxide, the most commonly used molten reagent, falls short of being an ideal etchant in that no mask yet investigated has been adequate. The simplicity of the process, however, has caused a search for such as mask. For a number of reasons, particularly the ease of deposition and the adherence of the deposits, this interest has centered around metal masks. The only metals yet investigated that offer any hope of success are gold and zirconium as mentioned in Section 4.2.

#### 4.3.4 Gaseous Etching

Gaseous chlorine will attack SiC at temperatures of 900-1100°C<sup>(1)</sup> and considerable work has been done on such etching at the Westinghouse Materials Laboratories.<sup>(19)</sup> Since it was not a suitable etchant to achieve the objectives of this earlier program, the emphasis was placed on other etching systems. However, with our requirements the process may be feasible if a suitable mask is found.

SiO<sub>2</sub> in the form of fused quartz is nearly resistant to attack by Cl<sub>2</sub> at temperature as high as 1100°C - 1200°C. Thus if a mask of SiO<sub>2</sub> is deposited on SiC, the masked surface should also be protected from attack by Cl<sub>2</sub>.

A preliminary experiment showed that SiC specimens were extensively attacked by Cl<sub>2</sub>. Also selective etching due to the polar nature of SiC was noted. In succeeding runs, attempts were made to obtain a layer of SiO<sub>2</sub> on SiC surfaces. The SiO<sub>2</sub> was prepared by oxidizing previously deposited Si or SiO. These runs were not completely successful because of poor adhesion of the SiO<sub>2</sub> and preferential etching by the Cl<sub>2</sub>. The results did suggest, however, that a satisfactory film could be prepared by oxidizing the SiC surface.



The initial experiments were done with SiC specimens oxidized for 1-3 hours at 1000°C. The results were erratic and somewhat confused by the effect of crystal polarity on the etching process. Consequently, a number of specimens, some unetched and some etched in molten  $\text{Na}_2\text{O}_2$ , were oxidized for 57 hours at 1200°C in an atmosphere of water vapor saturated oxygen. The oxide layer produced was believed to be from 1000 to 2000 Å thick. Specimens treated in this way were prepared for  $\text{Cl}_2$  etching by masking one end of each crystal with wax, leaving the other end exposed. The  $\text{SiO}_2$  was removed from the exposed end with HF. After removing the wax, the specimens (now with one end masked with  $\text{SiO}_2$ ) were etched three hours at 1000°C in  $\text{Cl}_2$ . Argon was used to flush the system before and after the run and a small amount was added to the  $\text{Cl}_2$  so that the flowmeter would not be contaminated. The data on this and other  $\text{Cl}_2$  etching runs is given in Table 4.3.

The results of this procedure are shown in Figure 4.2. On this figure, A designates the region coated with an  $\text{SiO}_2$  film, B the region from which the  $\text{SiO}_2$  film was removed by HF. As shown in the figure, the B region has a smooth surface where it was etched by the  $\text{Cl}_2$ . One result of the  $\text{Cl}_2$  etching is the formation of a carbon layer over the etched area. In the figure, region C has been etched, but the carbon layer has not been removed. The formation of this carbon layer has been previously reported;<sup>(19)</sup> and was present after all experiments in this series. The layer may be removed by scraping (as was done on the specimen in Figure 4.2) but it is more convenient to remove it by oxidation at elevated temperatures.

The effect of the polar nature of SiC was shown in these experiments. As has been described previously, when a SiC crystal is etched in molten  $\text{Na}_2\text{O}_2$ , one face becomes smooth while the other becomes rough and "wormy". The smooth face has been arbitrarily designated as the silicon face. In this experiment, the silicon face was only slightly attacked, the etch rate being about one micron per hour. The attack in the carbon face and in the lateral directions was greater. The carbon

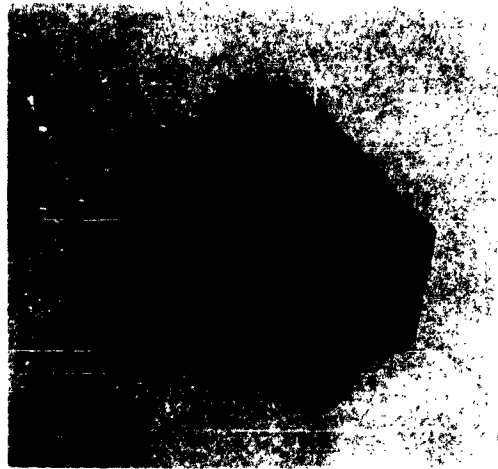


Figure 4.2 Chlorine-Etched SiC Crystal

- A. Surface Masked with  $\text{SiO}_2$
- B. Etched Surface with Carbon Removed
- C. Etched Surface with Carbon Remaining



Figure 4.3 SiC Crystal Etched in Chlorine and Oxygen

- A. Surface Masked with  $\text{SiO}_2$
- B. Etched Surface

Table 4.3

Run	Temp. (°C)	Atmosphere	Time (hr)	Type Specimen	Carbon Residue	Remarks
1	960	< 5% Cl <sub>2</sub>	1	grown junction (n-surface)	yes	* rf furnace; Face I not etched; Face II etched on both crystals; one Face II up, one Face II down.
2	940	1-1 Cl <sub>2</sub>	0.5	grown junction (n-surface)	yes	rf furnace; SiO film oxidized to SiO <sub>2</sub> ; poor adhesion; some substrate oxidized and not affected by Cl <sub>2</sub> .
3	930-1040	Cl <sub>2</sub>	1	grown junction (n-surface)	yes	Specimens from Run 2; scratched in area exposed during oxidation; Face I etched by Cl <sub>2</sub> at scratches; rf furnace.
4	930-1040	Cl <sub>2</sub>	0.5	grown junction (n-surface)	yes	Si-covered and plain SiC specimens, previously oxidized; plain SiC specs. protected against attack; Si-covered specs. not fully oxidized, oxide layer stripped off by preferential attack on Si; rf furnace.
5	900-950	Cl <sub>2</sub>	0.75	grown junction (n-surface)	yes	Change to resistance heated furnace; Face I exposed, attack only at dislocations.
6	950	Cl <sub>2</sub> +<5% Ar	2	grown junction (n-surface)	yes	Resistance furnace; specs. from Run 5; Face II exposed, attack observed there.
7	940-970	Cl <sub>2</sub> +<5% Ar	2.5	grown junction (n-surface)	yes	Oxide layer too thin, general attack where possible.
8	1000	Cl <sub>2</sub> +<5% Ar	3	grown junction (n-surface)	yes	Thick oxide film; Face I etched < 3μ; Face II etched 87μ; lateral etching 99μ; excellent masking by oxide.

Table 4.3 (Continued)

Run	Temp. (°C)	Atmosphere	Time (hr)	Type Specimen	Carbon Residue	Remarks
9	1015-995	Cl <sub>2</sub> + 5% Ar	1	grown junction (n-surface)	yes	Preparation for epitaxial growth; carbon scraped off, small specks removed in NaOH + Na <sub>2</sub> S <sub>2</sub> O <sub>8</sub> ; specs. etched briefly in Cl <sub>2</sub> while in epitaxial growth furnace; single crystal growth on Face II achieved.
10	1014	Cl <sub>2</sub> + O <sub>2</sub> + Ar	ca. 1.5	grown junction (n-surface)	no	Excellent etching; excellent masking by oxide; Face I etched 4-7μ; Face II etched 99-101μ; lateral etching 65-66μ.
11	1000	Cl <sub>2</sub> + 5% Ar	5/60	grown junction (n-surface)	yes	Carbon burned off in O <sub>2</sub> (5 min.); clean surface remaining.
12	1000	Cl <sub>2</sub> + 5% Ar	5/60	diffused	yes	Etched to determine Face II; subsequently oxidized; p-surface.
13	1000	Cl <sub>2</sub> + O <sub>2</sub> + Ar	ca. 0.25	grown junction	no	Step-etched to denote Face II; single crystal epitaxial growth on etched step.
14	1000	Cl <sub>2</sub> + O <sub>2</sub> + Ar	ca. 0.25	grown junction	no	Step-etching to identify Face II; single crystal epitaxial growth on etched areas; ambient may have been contaminated with H <sub>2</sub> O, SiO <sub>2</sub> formed on surface during etching.

\* Face I - Silicon Face } Defined on Page 7  
 Face II - Carbon Face }

face was etched at about 29 microns per hour while the lateral directions etched at a rate of about 33 microns per hour. In the figure the carbon face is shown.

The presence of the carbon layer after the  $\text{Cl}_2$  etching is a major problem since it can cause contamination and interfere with subsequent treatment. The most obvious solution to the problem would be to prevent its formation during the etching process.

It is expected for a priori reasons that the addition of oxygen to the chlorine would prevent the formation of the carbon layer.

To test this approach, several specimens were prepared in the same manner as those shown in Figure 4.1. These specimens were then etched in a mixture of  $\text{Cl}_2$ ,  $\text{O}_2$  argon for 1-1/2 hours at  $1000^\circ\text{C}$ . The composition of the gases was varied from 40-70%  $\text{Cl}_2$ , 10-30%  $\text{O}_2$  and 5-10% Ar. The data on these experiments are also given in Table 4.3. The results of this etchant are shown in Figure 4.3. The region of the crystal covered with the oxide mask is marked A and the etched surface is marked B. As noted in previous experiments using only  $\text{Cl}_2$  and argon, the carbon face etched more rapidly than the silicon face. The silicon face etched at a rate of 3-5 $\mu$  per hour while attack on the carbon face and in the lateral directions occurred at rates of about 66 $\mu$  per hour and 44 $\mu$  per hour respectively. The etching was quite uniform over the exposed surface, and no difference could be seen in two specimens etched at the same time. The carbon face is shown in Figure 4.3.

Although neither etchant attacks the "silicon" face appreciably in the as grown state, both have strong rates of attack on the damaged layer of this face after lapping or at dislocations intersecting the surface. A characteristic common to both types of etching is the ability of the grown  $\text{SiO}_2$  film to resist the attack of the etchant. The film is apparently impervious to the etchants and substantially without defects. The sharp line of demarcation between the etched and masked region of the specimens indicates that the film is firmly adherent and that there is no tendency for preferential attack to occur along the  $\text{SiC} - \text{SiO}_2$  interface.

Both etchants give favorable ratios of lateral to vertical attack. The ratio for chlorine etching was  $99\mu/87\mu$  or 1.1, and for chlorine and oxygen etching it was  $66\mu/100\mu$  or 0.66. The latter value is exceptionally low and suggests that such etching might make it possible to resolve masked patterns in a substrate with much better precision than has been observed with any prior system.

#### 4.3.5 Applications of Chlorine and Chlorine and Oxygen Etching

Since this etching is strongly preferential to the carbon face and success in obtaining epitaxial growth on this face had been lacking in the past, experiments were designed to determine the reason for this lack of success and to achieve good epitaxial growth on the carbon face. The results of these experiments were not entirely conclusive, but it was found that etching with chlorine and oxygen produces a good surface for subsequent epitaxial growth. Most of the crystals so prepared, had single crystal growth in the etched regions with some polycrystalline growth in the masked areas. Several had some polycrystalline regions in the epitaxial layer due to crystal imperfections that were not obvious until after etching.

The applications of this method in the field of pattern etching are obvious, but other uses can be conceived. Thinning a crystal would possibly be easier with this type etching than with lapping, particularly when the thicknesses are to be made less than  $50\mu$ . No masking would be needed since only the carbon face is attacked appreciably. A further advantage of such a thinning process would be the lack of a damaged layer which would complicate further processing. Edges of crystals can be removed and junction depths delineated by oxide masking the surface and exposing the edges. In this way, no surface damage would be introduced by such procedures as lapping or sandblasting.

#### 4.3.6 Polarity of Silicon Carbide

One interesting result of this etching is the difference in etching rates on the two sides, caused by the polarity of the SiC. To clarify the meaning of polarity, the crystal lattice of SiC, when viewed

in a direction perpendicular to the basal plane, is made up of alternating layers of silicon and carbon atoms in a sequence beginning with a (000 $\bar{1}$ ) face made up of silicon atoms and ending with another (0001) face made up of carbon atoms. This arrangement gives a significance to the manner in which a SiC crystal is attacked.

Effects of polarity are seen with other etchants as well, and it is conceivable that the erratic results that have been seen in electrolytic etching may also be a result of crystal polarity.

It is interesting to question which surface contains the carbon atoms and which the silicon atoms. Prior to this work, it has been generally believed on somewhat arbitrary grounds that the face which etches smooth in molten Na<sub>2</sub>O<sub>2</sub> contains the silicon atoms. The results with the chlorine etching tend to contradict that opinion. Chlorine is a strongly electronegative element. Silicon is also known to be more electropositive than carbon; this is also true for a SiC lattice as well, since at temperatures in the range of 0-200°K the electrons tend to be associated with the silicon atoms and the holes with the carbon atoms.<sup>(20)</sup> At the temperatures of gaseous etching, ca. 1270°K, this distribution would be overwhelmed by thermal generation of carriers and should not affect the etching. The polarity, however, should tend to keep the same relative direction. An electronegative etchant would be expected to attack more readily at the more electropositive site in the crystal lattice. This would mean that the face which is more readily attacked by the Cl<sub>2</sub> should be the face with the silicon, i.e., the rough face after NaO<sub>2</sub> etching may be the silicon face.

## 5.0 Evaluation of the Properties of the Epitaxial Layers

### 5.1 Undoped Layers

The electrical properties of several epitaxial layers which were grown by vapor deposition using the techniques described in this report, have been determined. All the layers which have been examined were grown on p-type substrates.

For thin, high-resistivity epitaxial layers grown on low-resistivity substrates, the conventional methods used to determine the conductivity type and the average resistivity are not suitable, since the presence of the substrate may seriously affect the measurements. Accurate measurements of the electrical properties of the epitaxial layers, therefore, were not possible. It has been possible, however, to obtain some information about these properties, using the measurements which will be described.

#### 5.1.1 Point-Probe Rectification

Before making any electrical measurement, the edges of the specimens were cleaned, either mechanically or electrolytically, to remove the imperfect material that often grows in these regions. A tungsten plate, acting both as a mechanical support and as an electric contact, was then alloyed to the substrate side of specimen using Au-Ta-Al pellets, which produce ohmic contacts to the p-type substrate.

The first electrical measurements were made on the epitaxial layer by using simple pressure point-probe contacts. The measurement of the I-V characteristics were made by means of a Tektronix transistor curve tracer. As shown in Fig. 5.1 these point contacts have unusually good rectifying properties, i.e. better than is usually observed for point-contacts on conventional SiC crystals.

The reverse leakage current was practically undetectable, (less than  $10^{-6}$  A), at 200 V PRV.

Such a result suggested the possibility that the rectification was due to a p-n junction present between the epitaxial layer and the substrate,





Figure 5.1 Characteristics of point probe contact at room temperature.

- a. Forward. Horizontal, 1 v/div.; Vertical, 10 $\mu$ a/div.
- b. Reverse. Horizontal 20 v/div.; Vertical, 10 $\mu$ a/div.



Figure 5.2 Characteristics of evaporated contact at room temperature.  
Origin to right.

- a. Forward. Horizontal, 0.5 v/div.; Vertical, 10 $\mu$ a/div.
- b. Reverse. Horizontal, 20 v/div.; Vertical, 10 $\mu$ a/div.

the epitaxial layer being n-type, as the direction of the rectification was the same that can be expected for this case (forward conduction with the point negatively biased.) Such an interpretation, however, was ruled out because the I-V characteristics measured between two point probes placed onto the same epitaxial layer exhibit reverse characteristics in both directions.\* It was therefore concluded that the epitaxial layer was p-type and that the rectification effects observed were due only to metal-SiC contact.

#### 5.1.2 Evaporated Contacts

To better understand the results obtained from the measurements performed with point-probes contacts on the epitaxial layers, similar measurements were performed with evaporated metal contacts.

A Au-Ta film was therefore deposited by vacuum evaporation onto the surface of the epitaxial layers, using the technique described in Scientific Report No. 3 on this project.<sup>(3)</sup> The metallized surface was then masked with Apiezon wax and chemically etched, leaving only two small metallized areas to be used as electric contacts.

The results obtained with evaporated contacts were qualitatively similar to those obtained using the simple point-probe contacts. The forward and reverse characteristics between the two contacts on one of the specimens examined are shown in Fig. 5.2.

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\* This result alone could be explained in a different way. If the layer is n-type and the observed rectification is due to a p-n junction between the epitaxial layer and the substrate, this result can be expected if the resistivity of the layer is so high that the current flowing directly between the two probes is smaller than the reverse current of the junction. From the results of measurements and the geometrical dimensions of the specimens it was possible to calculate that this could be true if the resistivity of the layer is at least as high as several thousand ohm-cm. Although such a value of the resistivity is not theoretically impossible (the theoretical intrinsic resistivity of SiC being of the order of  $10^{21}$  ohm-cm at room temperature), this interpretation does not seem to be very convincing, particularly in view of the results obtained from the capacitance measurements which will be described later.

The contacts, not being alloyed, are simply metal-semiconductor contacts of the so-called surface-barrier type. Therefore the electrical properties depend not only on the semiconductor properties but also on the properties of the metal (in particular on the value of its work function). The metal in this case is Ta, the gold protecting the thin Ta film from oxidation and damage. As the Tektronix curve tracer has inadequate sensitivity, the measurement of the reverse saturation current was also attempted on a X-Y recorder having a maximum sensitivity of  $10^{-8}$  A per division. The reverse currents were undetectable even on this instrument, showing that the current at low reverse voltages is lower than  $10^{-8}$  A.

The properties of the contacts were also measured at high temperatures. As expected, the forward characteristic improves considerably as the temperature increases, while the reverse characteristic deteriorates. The results of the measurements are shown in Fig. 5.3. Particularly interesting is the fact that the I-V characteristics did not change after the heating cycle.

#### 5.1.3 Capacitance Measurements

The evaporated contacts, whose electrical properties have been described in the preceding paragraph, allowed, through capacitance measurements, an evaluation of the doping level of the epitaxial layer.

The relationship between the capacitance of a surface-barrier contact and the reverse applied voltage can be easily calculated for a uniformly doped semiconductor, from the relationship between the width  $d$  of the space-charge layer and the applied voltage  $V$ :

$$V + V_0 = \frac{q}{2\epsilon} N d^2 \quad (5.1)$$

where  $V_0$  is the height of the metal-semiconductor barrier,  $N$  is the net impurity concentration,  $q$  is the electronic charge ( $1.5 \times 10^{-19}$  coulombs) and  $\epsilon$  the dielectric constant ( $.9 \times 10^{-13}$  for SiC).



If A is the contact area, the capacitance is given by:

$$C = \frac{A\epsilon}{d} \quad (5.2)$$

Therefore, from the equation (5.1), we obtain:

$$C = \frac{q\epsilon N A^2}{2(V + V_0)} \quad (5.3)$$

and

$$N = \frac{2(V + V_0)}{q\epsilon A^2} C^2 \quad (5.4)$$

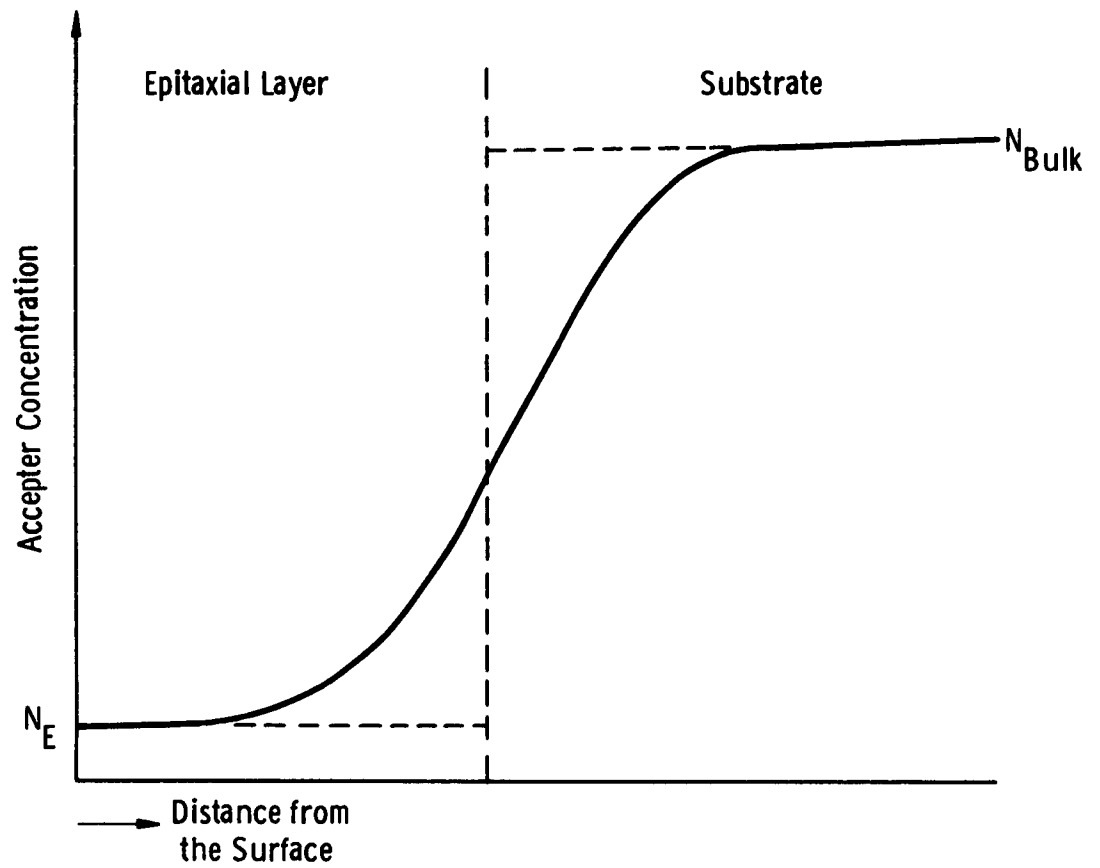
These expressions, however, are only valid if the semiconductor is uniformly doped in the region near the surface, inside the space-charge layer. For the epitaxial layers under consideration the most probable impurity distribution is the one qualitatively shown in Fig. 5.4. The transition between the highly doped substrate and the less doped epitaxial layer is probably gradual, due to solid state diffusion which occurs during the growth process.

Equations 5.1, 5.3 and 5.4 will give a reasonable approximation to the true values only when the space-charge layer width is much smaller than the thickness of the epitaxial layer.

When the space-charge layer width is of the same order or larger than the thickness of the epitaxial layer, equations 5.1, 5.3 and 5.4 will no longer be true, and the capacitance will change with the voltage at a rate substantially smaller than that predicted by the equation 5.3.

For small applied voltages, however, if the value of d deduced by the equation 5.2 is much smaller than the thickness of the epitaxial layer, equation 5.4 can be used as a reasonable approximation to calculate the impurity concentration,  $N_E$ , near the surface of the epitaxial layer. This is, of course, only an order-of-magnitude approximation of the impurity concentration N. It must be also pointed out that the value of  $V_0$ , the height of the metal-semiconductor barrier, is not known. In the following calculations it is assumed,  $V_0 = 2$  volts. Such an

CURVE 565098



Probable impurity profile in the SiC epitaxial layer

Fig. 5.4

assumption is rather arbitrary, but it should not produce an error larger than  $\pm 50\%$ . As we are presently interested only in knowing the order of magnitude of the impurity concentrations, this may be considered satisfactory.

The capacitance measurements just described were performed on some of the specimens examined. Figure 5.5 shows a representative sample with the contacts. The results for three of these specimens are illustrated in the curves of Figs. 5.6, 5.7 and 5.8. As can be seen, specimens 1 and 2 gave similar results, while the specimen No. 3 seems to have a much higher doping level.

The substrate of the specimen No. 3 was actually different from the substrates of the specimens No. 1 and 2, which were grown during the same growth run, and was probably more heavily doped. This seems to indicate, therefore, that the doping of the epitaxial layer may be affected by the impurities present in the substrate.

It can be pointed out, in this respect, that the thickness of the examined layers (about  $10\mu$ ) was small enough to allow for the possibility of a solid-state diffusion during the epitaxial growth from the substrate.

## 5.2 Doped Layers

To investigate the possibility of doping intentionally the epitaxial layers, a few growth runs were made during which a volatile phosphorus compound was introduced in the apparatus used for the growth. The substrate was p-type.

Only one specimen of this run has been examined. The layer grown was cubic silicon carbide. Due to the introduction of the phosphorus, the layer was expected to be n-type. Actually the specimen appeared to have properties very different from those of the previously examined specimens. The measurements with the point probes did not give any useful information, because the characteristics obtained with the transistor curve tracer were erratic and did not show definite rectification. Two Au-Ta evaporated contacts were subsequently put onto the surface of the

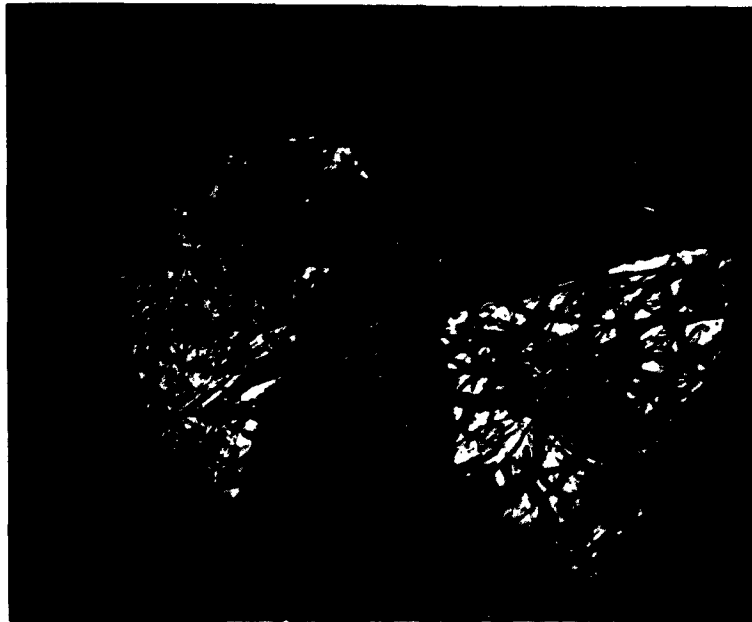
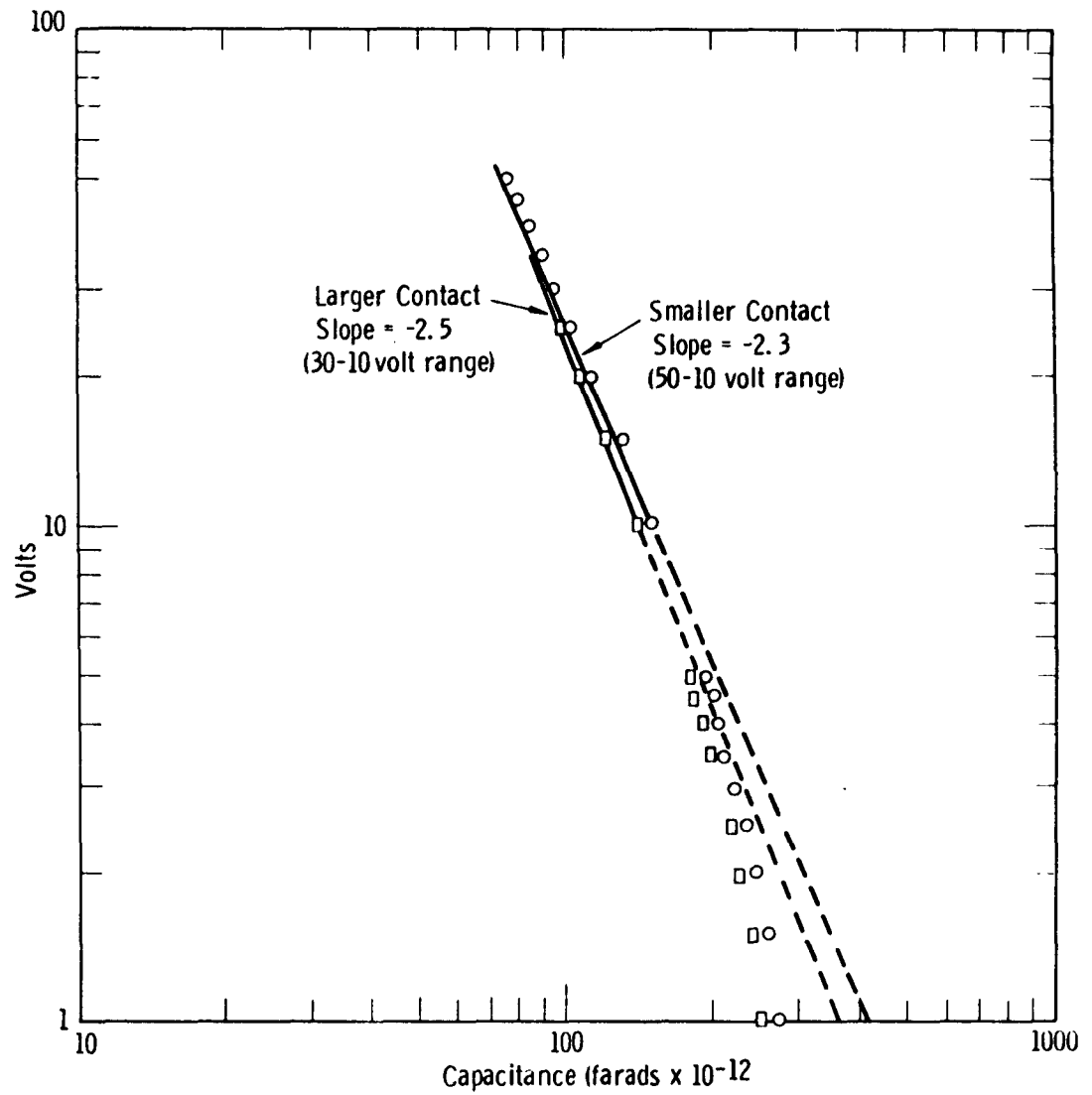


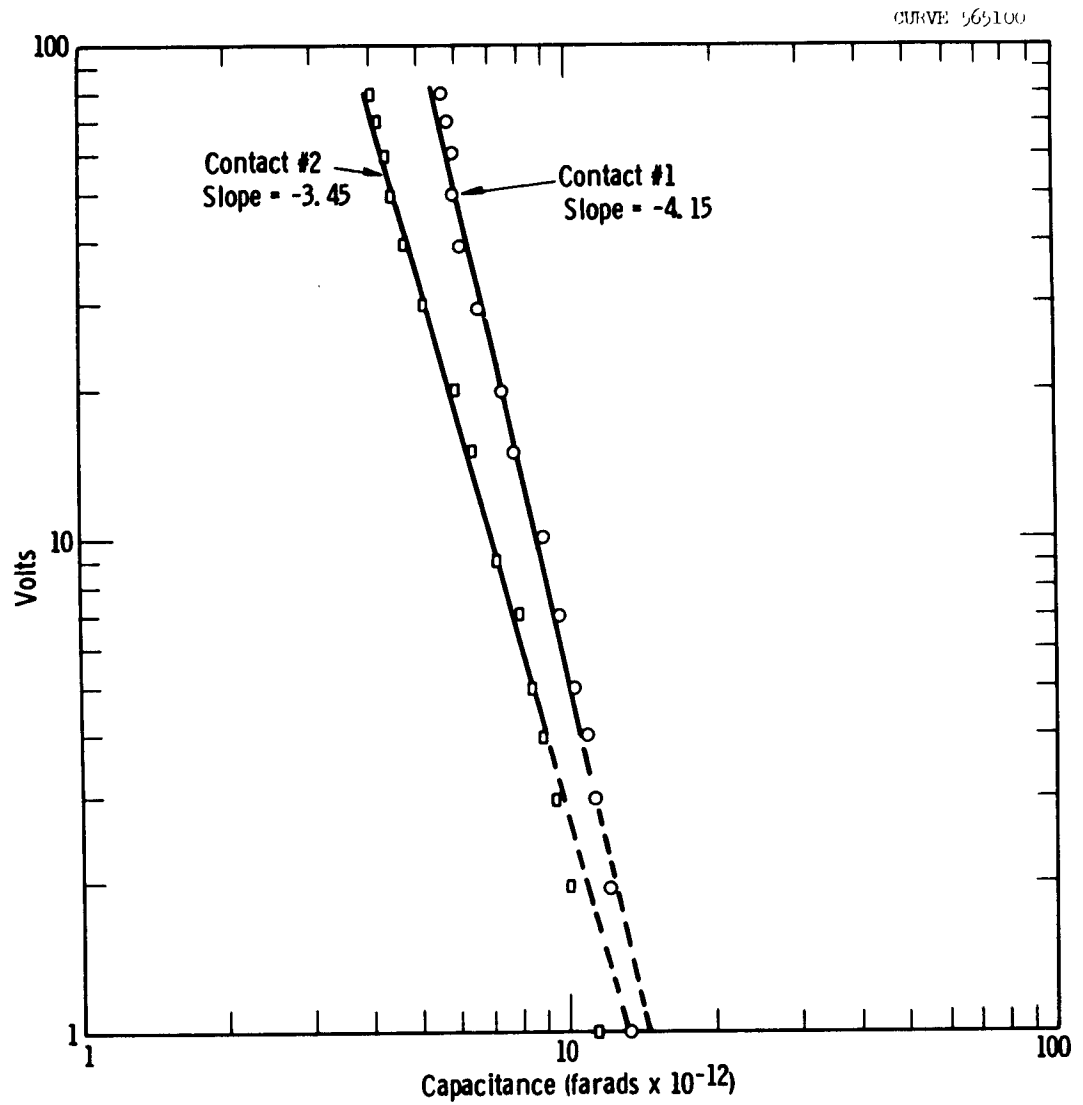
Figure 5.5 Evaporated surface barrier contacts, used for capacitance measurements. Contact No. 1 to right, No. 2 to left.





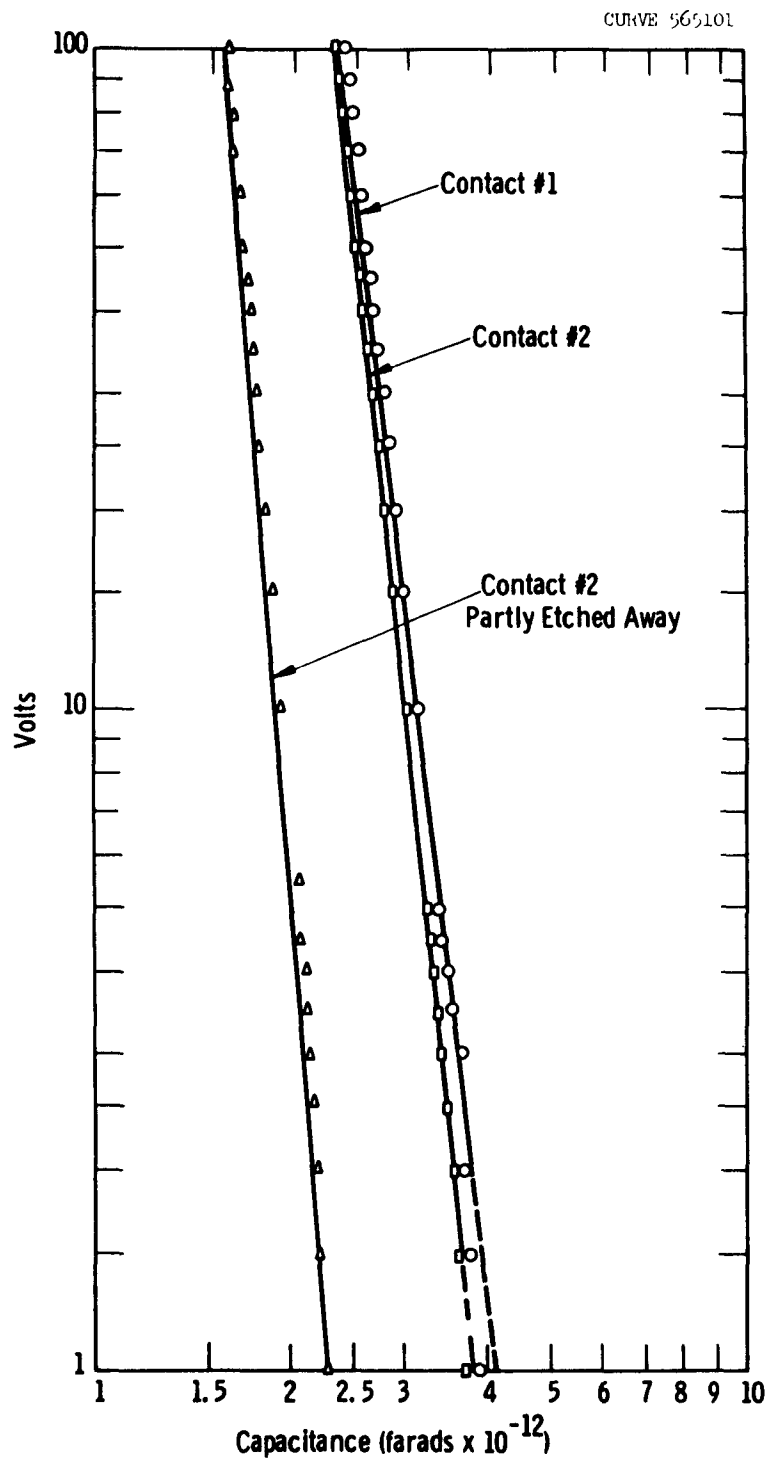
The variation of capacitance with reverse bias

Fig. 5.6 Specimen #1



The variation of capacitance with reverse bias

Fig. 5.7 Specimen #2



The variation of capacitance with reverse bias

Fig. 5.8 Specimen #3

epitaxial layer (the substrate, as for all the specimens previously examined, was alloyed with Au-Ta-Al onto a tungsten tab). The two contacts were alloyed to produce ohmic connections to the epitaxial layer, which was suspected to be n-type. After the application of the contacts the specimen was electrolytically etched and was then given a very short chemical etch in molten  $\text{Na}_2\text{O}_2$ .

The I-V characteristic measured between one of the contacts to the epitaxial layer and the contact to the substrate, which initially did not indicate any real rectification, showed a definite rectification after several molten salt etches.

The I-V characteristic measured between the two contacts applied to the epitaxial layer was almost perfectly ohmic. It was therefore concluded that the rectification was, in this case, due to a p-n junction between the p-type substrate and the epitaxial, which was therefore n-type.

The properties of this junction are poor. It is possible that this result may be partially attributed to insufficient etching. The etching time was limited by the lack of masking to protect the contacts from the action of the molten  $\text{Na}_2\text{O}_2$ .

From the measurement of the ohmic resistance between the Au-Ta contacts, the value of the resistivity at room temperature may be calculated and is probably between 1 and 10 ohm cm. This calculation must take into account possible sources of error such as contact resistance and irregular specimen geometry.

## 6.0 Conclusions

The work in this report attempted to develop some practical technological process suitable for the controlled fabrication of SiC devices. The results can be summarized as follows:

6.1 Epitaxial layers of hexagonal and cubic SiC have been grown on hexagonal SiC platelets using a vapor phase-thermal reduction method. The crystal perfection of the cubic SiC is relatively poor due to mismatch between the cubic and hexagonal phases. At temperatures above about  $1700^\circ\text{C}$  the hexagonal phase was formed. A final mechanical polish was used to obtain growth of high perfection.

6.2 A technique has been developed for the fabrication of an evaporated metal contact. By evaporating and alloying Au-Ta or Au-Ta-Al films, ohmic contacts having controlled geometry can be made to SiC crystals. This evaporation process can also be used, in some cases, to produce rectifying surface-barrier contacts.

6.3 The problem of controlled machining and etching of SiC specimens has been carefully examined. Controlled lapping, and electrolytic etching, masking procedures for etching in molting salts and controlled gaseous etching has been taken into consideration.

The deposition of Zr films to be used as protective masks during the etching in molten  $\text{Na}_2\text{O}_2$  has been investigated, Zr having been selected because of its relatively good resistance to molten  $\text{Na}_2\text{O}_2$ . The results have not been satisfactory because of the difficulty of depositing a thick, adherent Zr film onto the SiC surface. After improving the techniques for the Zr deposition, this method may become practical.

Recent developments, show that high temperature gaseous etching with chlorine and oxygen is a more satisfactory procedure. This technique is especially suitable for device fabrication since an efficient mask of  $\text{SiO}_2$  is easily prepared.

6.4 The electrical properties of a few SiC crystals having a vapor-phase grown epitaxial layer have been examined. Although the results cannot be considered definitive, due to the small number of specimens examined and to the uncertainty of the measurements, the following indications have been obtained:

1) High purity p-type SiC epitaxial layers can be grown epitaxially. Impurity concentrations of the order of  $10^{14} \text{ cm}^{-3}$  have been measured.

ii) By adding a phosphorus compound to the gaseous phase during the growth of the epitaxial layer, an n-type layer has been produced. This result seems to suggest that doping agents can be intentionally introduced in the epitaxial layers.

iii) A rectifying p-n junction has been observed between the p-type substrate and the n-type epitaxial layer.

iv) With thin, high purity, p-type layers grown onto heavily doped p-type substrates good rectifying surface-barrier contacts can be obtained.

Combining the epitaxial growth techniques with a suitable technology for contact fabrication and controlled etching, the production of SiC transistors of controlled quality comes nearer to fruition.

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