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Page

20. Substitute Enclosure (1), which corrects data for $P_n(\epsilon)$ in Table 1.

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TABLE 1. Experimental and Theoretical Data for the Linear Matched Filter and Shift Register Recognizer

Sync pattern = 11-bit Barker (11100010010); sampling aperture = 10 μs, signal = NRZ plus noise filtered at 150 kc; number of errors allowed (ε) = 0.

S/N	p	Linear Matched Filter				Shift Register Recognizer			
		$P_n(\epsilon)'$		$F_n(\epsilon)'$		$P_n(\epsilon)$		$F_n(\epsilon)$	
		Exp.	Theoretical	Exp. x 10^{-3}	Theoretical x 10^{-3}	Exp.	Theoretical	Exp. x 10^{-3}	Theoretical x 10^{-3}
2.11	0.001	0.97	0.74	2.60	2.36	0.996	0.989	0.466	0.474
1.96	0.003	0.95	0.73	2.50	2.76	0.955	0.968	0.457	0.474
1.64	0.01	0.94	0.69	3.92	4.17	0.89	0.89	0.464	0.474
1.40	0.02	0.93	0.67	5.33	6.45	0.78	0.80	0.455	0.474
1.15	0.05	0.92	0.64	11.09	10.94	0.54	0.57	0.441	0.474
0.95	0.09	0.90	0.61	19.93	18.63	0.36	0.34	0.465	0.474
0.85	0.12	0.89	0.60	24.10	26.30	0.25	0.25	0.442	0.474

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TECHNIQUES FOR SYNCHRONIZING PULSE-CODE-MODULATED TELEMETRY

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FOREWORD

This report presents a summary of the theoretical and experimental investigation of synchronization methods for PCM telemetry that was originally undertaken by the Instrumentation Division of the Naval Ordnance Laboratory, Corona, California, in April 1959. The initial phase of the work, concluded in September 1960, was sponsored by the Air Force on MIPR (33-616) 59-29 under Appropriation 57X3600, Task 82188. The work was continued under Navy sponsorship and was authorized by Bureau of Naval Weapons WepTask RMWC52-036/211-1/F009-13-01.

The information contained herein represents the contribution of many individual members of the Instrumentation Division. E. R. Hill, who authored the report and directed the investigations, was assisted by J. L. Weblemoe and J. R. Campbell, who were major contributors to the project. Acknowledgment is also made of the contributions of H. H. Mansnerus, who aided in designing the experimental equipment, planning the test procedures, and collecting data. E. H. Hygh, J. W. Battles, and J. J. Berry also provided valuable assistance during the early phases of the program.

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ABSTRACT

A theoretical and experimental study was made of frame synchronization (sync) for non-return-to-zero pulse-code-modulated signals, including conditions where bit sync may not be stable. Criteria for sync pattern selection and for sync mechanization logic are treated for stable and unstable bit sync. Two types of sync pattern detectors are evaluated; the linear matched filter and the shift register recognizer. Techniques for finding sync patterns satisfying a given criterion are described. Effects of data-filter bandwidths on bit sync and bit detection are discussed. The results of a separate study are given, wherein bit sync is aided by an RF carrier coherent with the bit frequency.

CONTENTS

Table

I. INTRODUCTION

This study deals primarily with the frame synchronization (sync) of non-return-to-zero (NRZ) pulse-code-modulated (PCM) signals under conditions of clock instability and signal-to-noise ratio (S/N) that do not necessarily permit continuously stable bit sync. Stable bit sync is assumed to exist when a local oscillator is synchronous with the PCM signal, slippages do not occur, and phase errors are less than ±10 percent of a bit period. Frame sync allows proper decommutation of the data and is usually achieved by proper phasing of a bits-per-frame counter.

As far as possible in this investigation, the theoretically predicted performance is supported by experimental evaluation. For statistical simplicity, the theoretical analysis assumes Gaussian noise, and a Gaussian noise source was used in the signal simulator.

Frame sync information is transmitted by a specially coded sync pattern at frame or subframe rates, or at submultiples of these rates. A frame is defined as one complete sampling of all primary channels. Two types of correlators are analyzed for detection of the frame sync pattern: the linear matched filter (LMF) and the shift register recognizer (SRR). Assigning bits to each word for sync purposes has been shown in a previous report to be undesirable (Ref. 1).

The effect of the following factors on bit sync has been studied: airborne-clock stability, data-filter bandwidths, and phase-lock-loop noise bandwidths. The results of an independent study (Ref. 2) wherein the RF carrier is coherent with the bit frequency are discussed.

Frame sync may consist of three phases: (1) acquisition, (2) verification, and (3) retention. In the acquisition phase, the entire frame is searched in an effort to find a sync indication. If a true sync has been found, it will reoccur at frame intervals with a probability determined by the noise environment. During the retention phase, the output of the sync pattern detector is observed during a narrow time interval, or aperture, in order to reduce the possibility of false-sync indications. If stable bit sync is maintained, this aperture need be only one bit period wide.

During the experimental investigation, it was discovered that voltage-controlled oscillator (VCO) slippages of plus or minus one bit per frame

were a frequent occurrence under conditions of unstable bit sync. Consideration was given to the possibility of using a three-bit aperture, thus permitting rapid detection and correction for these slippages. The three-bit aperture leads to a different criterion for selection of sync patterns than does the one-bit aperture. The use of the three-bit aperture was found to have advantages over the use of the one-bit aperture.

The correlation function for codes selected on the three-bit aperture criterion exhibits two large negative correlation peaks, one on each side of the positive correlation peak (true-sync position). The use of these negative correlation peaks in the sync pattern detection logic results in a somewhat improved relationship between the recognition probability and false-sync probability.

Near optimal frame sync patterns for both the three-bit and the one-bit aperture criteria are given, and techniques for finding them are described. Also, the different properties of each pattern and their effect on frame sync are discussed.

Inasmuch as reference will be made throughout this report to different parts of the communication channel, Figure 1 is included to show the general arrangement of components assumed in this report.

A PCM signal simulator was constructed to produce an NRZ signal with word lengths from 10 to 33 bits. With this simulator, up to 100 words could be placed in each frame, and any desired frame sync pattern could be placed at the beginning of each frame. Fixed bits could be placed at the beginning and end of each word to simulate word sync, if desired. Random bits were generated to fill the other bit positions of the frame. The polarity of these bits was determined by sampling Gaussian noise with an average of zero, thus giving each bit an equal probability of being either a one or a zero. The bit rate employed was 100 kilobits per second.

Special terms used in this report are defined in a special Nomenclature section at the end of the book.

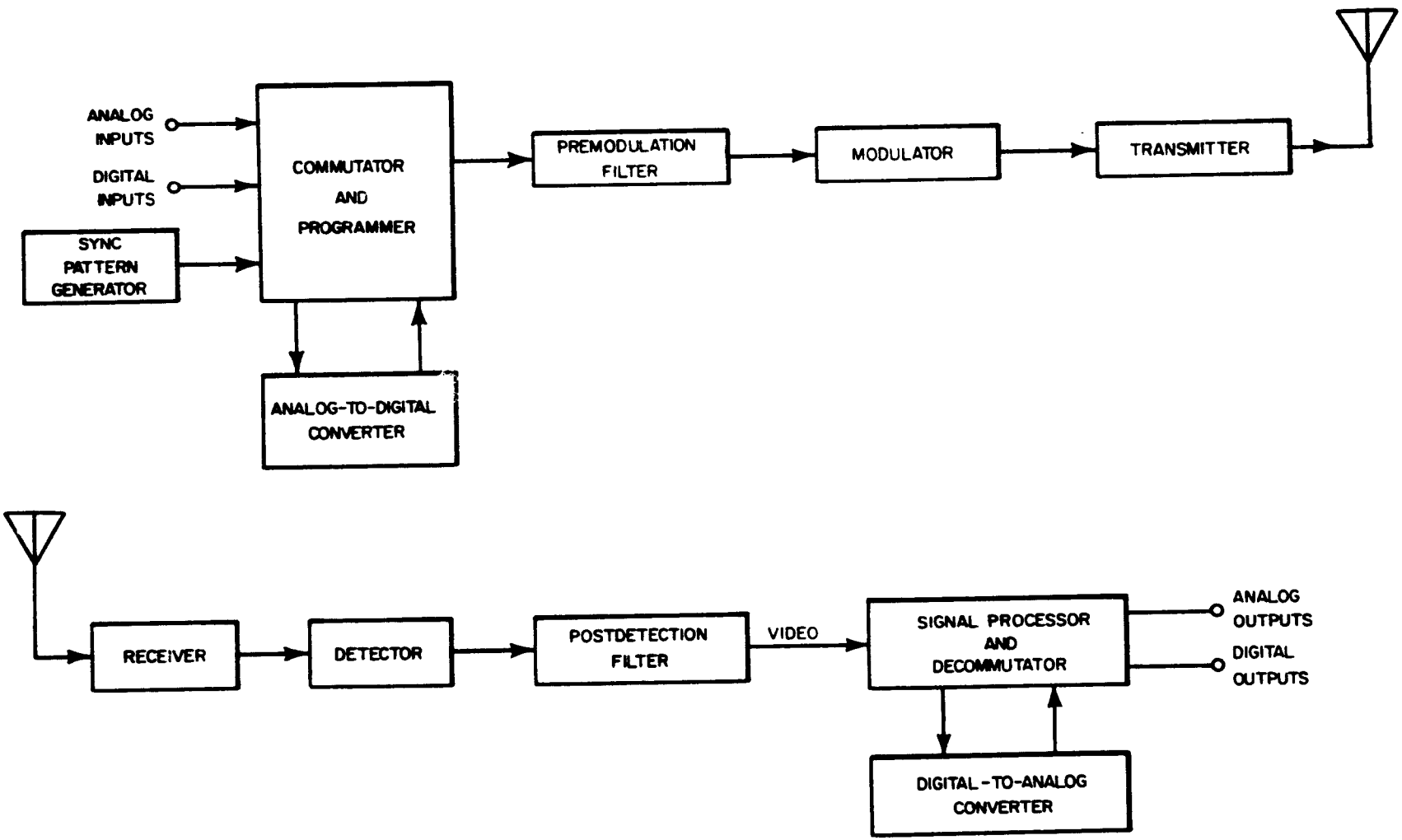


FIGURE 1. Typical PCM Communication Channel

II. BIT SYNCHRONIZATION

A. PHASE LOCK

1. FREQUENCY SPECTRUM OF PCM SIGNAL

a. Non-Return-to-Zero

It is assumed that the PCM signal is of the NRZ type, wherein ones and zeros are represented by discrete levels, and that transitions in the bit stream occur only when there is a change from one to zero, or from zero to one.

Coherent detection of a PCM signal requires an oscillator which is synchronous in frequency and phase with the signal. To obtain the bit sync information from the video signal, a phase-lock oscillator is normally used. The frequency spectrum of a random PCM, NRZ signal filtered at 1.5 times the bit rate appears in Figure 2. The spectrum plot reveals a tendency toward deep nulls at the bit rate and its multiples. The sharp peaks that appear at the bit rate and its multiples would not appear if the rise and fall times were identical, and therefore they are not dependable for sync purposes. The frequency spectrum of an NRZ signal accordingly contains no dependable components at the bit frequency.

b. Spectrum Transformation

(1) Gating techniques. Several gating and integrating-gating techniques have been developed for extracting the bit frequency from an NRZ signal. The people working on these techniques[1] have not yet published the results of their work.

(2) Differentiation and rectification. Transitions in an NRZ bit stream occur at integral multiples of the bit period. The spectrum of an NRZ signal contains no component at the bit frequency. The Fourier analysis of a periodic train of unidirectional pulses contains frequency components at the fundamental pulse frequency and at even and odd harmonics thereof. As might be expected, differentiation and full-wave rectification of an NRZ signal produces a waveform whose spectrum

[1]Some of the companies in California where this work is being done are: Space General Corporation, Glendale; Beckman Instruments, Inc., 2400 Harbor Boulevard, Fullerton; and Telemetrics, Inc., 12927 South Budlong Avenue, Gardena.

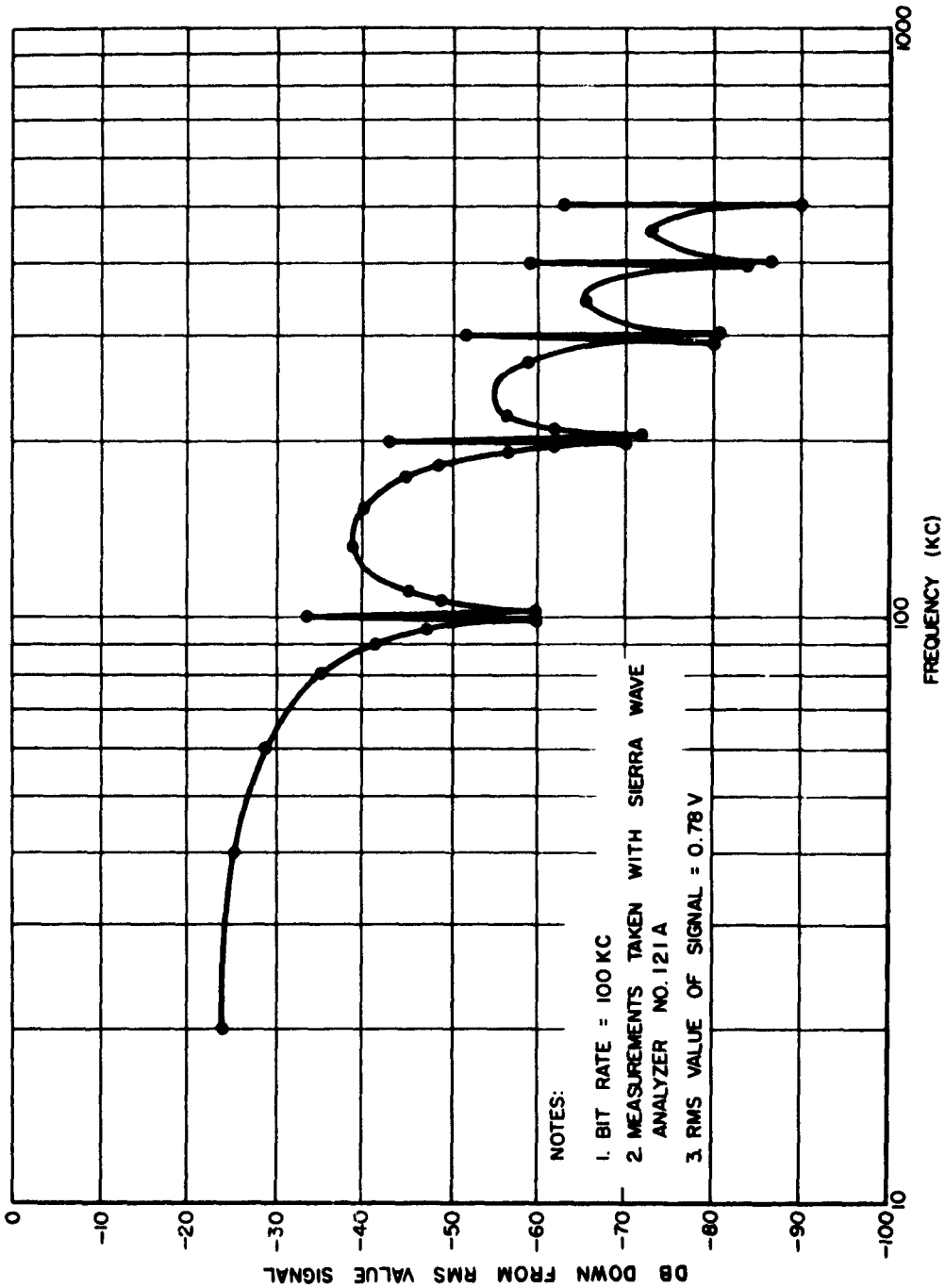


FIGURE 2. Spectrum of a Random NRZ Signal Filtered at 1.5 x Bit Rate

contains a strong component at the bit frequency and at even and odd harmonics thereof.

Figure 3 shows the spectrum of a differentiated and half-wave rectified NRZ signal in which the fundamental at the bit frequency is 20 db above all other frequencies, except harmonics of the bit frequency. Full-wave rectification would normally be employed, since half-wave rectification discards half the transitions and therefore loses half the bit frequency information.

2. PHASE-LOCK NOISE BANDWIDTH

a. Phase Detector

A phase detector is required in a phase-lock loop to detect any change in phase between the VCO and the signal. The usual phase-lock loop analysis assumes a continuous-wave signal. The VCO waveform, therefore, is sampled for half of each period of the incoming signal. For a PCM, NRZ signal, the information relative to the bit frequency is contained in the transitions. For a random bit stream (i.e., ones and zeros, each occurring with a probability of 0.5), the average number of bits between transitions is two. Hence, the probability that the next transition will be n bits away is $(\frac{1}{2})^n$. Because the NRZ signal, as such, is not a satisfactory input to the phase detector, the mechanization employed in the bit synchronizer detects the transitions with a zero-crossing detector and triggers a blocking oscillator with a constant-width output pulse. Since the VCO waveform is sampled for the duration of this pulse, the pulse width must be less than the bit period and usually less than half of this period.

The noise bandwidth of the phase-lock loop is a function of both the width of the sampling aperture and the average sampling frequency. The theory for continuous-wave signals (Ref. 3) shows the noise bandwidth to be a function of three parameters: the gain constant, K, the damping ratio, ζ, and the undamped natural resonant frequency, ω_n. The resonant frequency is a function of K and of the bandwidth-determining time-constant, τ_2:

$$\omega_n = \sqrt{\frac{K}{\tau_2}} \qquad (1)$$

The effect of aperture and frequency sampling upon noise bandwidth can be seen by examining τ_2. The speed of a phase-lock loop's response to an input phase reversal depends on transferring the charge (thus, voltage) to the control network (whose major time constant is τ_2) in each input signal cycle. If a continuous-wave input signal sampling aperture is d_2 and the VCO output is a sawtooth waveform, the time constant,

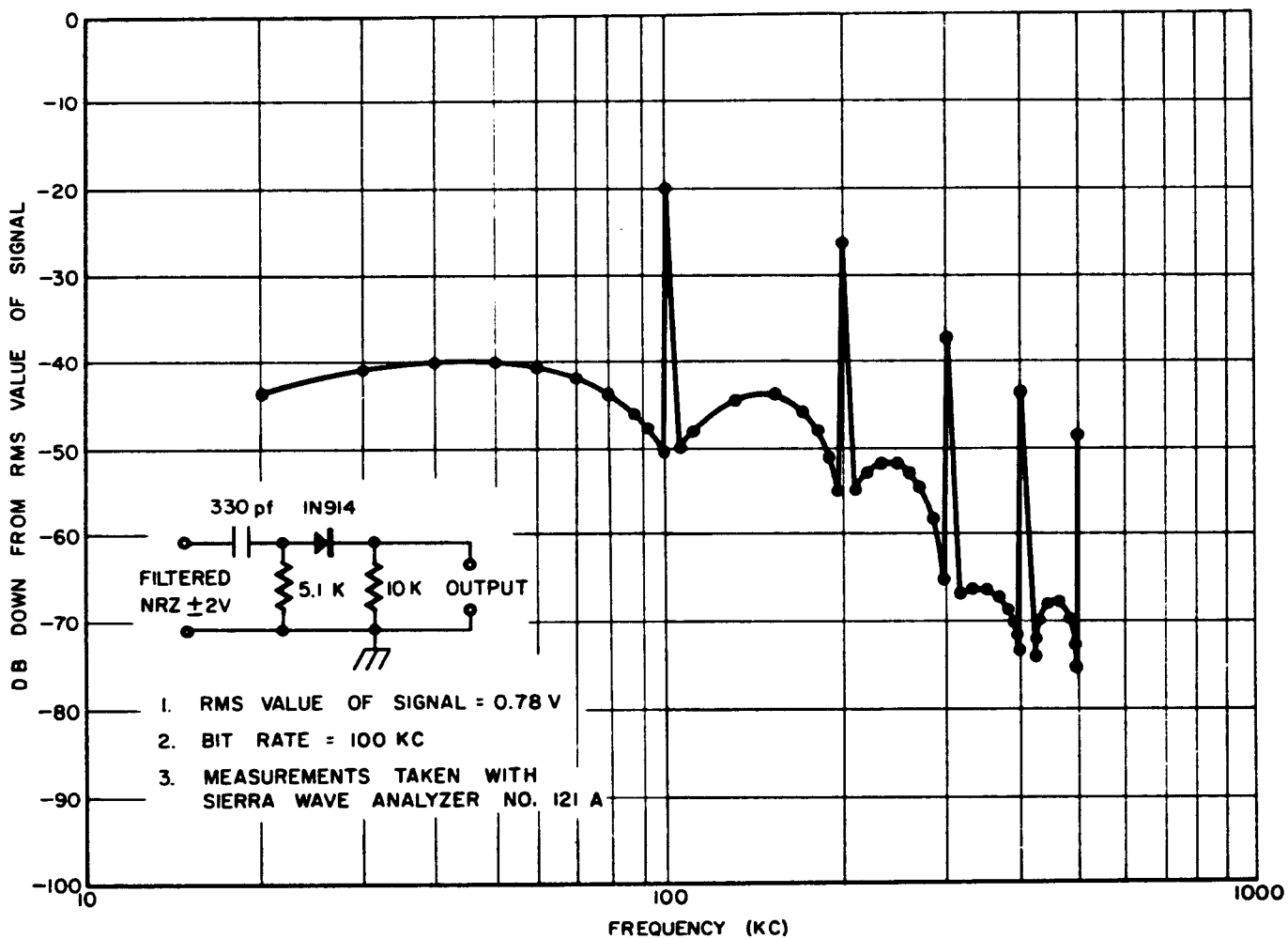


FIGURE 3. Spectrum of a Random NRZ Signal Filtered at 150 kc, Differentiated, and Half-Wave Rectified

τ_2, appears to be changed by the factor (d_2/d_1), where d_1 is the actual sampling aperture. For a multiplier phase detector, d_2 would be equal to half the period of the continuous-wave input. If the average sampling frequency caused by transitions in the NRZ signal is f_1, the time constant, τ_2, is reduced by the factor (f_b/f_1), where f_b is the bit frequency. Thus, the effective time constant, τ_2', is τ_2 changed by the factor $(d_2/d_1)(f_b/f_1)$.

$$\tau_2' \propto \left(\frac{d_2}{d_1}\right)\left(\frac{f_b}{f_1}\right)\tau_2 \tag{2}$$

Therefore, the natural resonant frequency becomes

$$\omega_n' \propto \left(\frac{d_1 f_1 K}{d_2 f_b \tau_2}\right)^{\frac{1}{2}} \tag{3}$$

The noise bandwidth of the phase-lock loop is therefore a function of the factor $(d_1/d_2)(f_1/f_b)$. Although d_1 can be held constant, f_1 is dependent upon the average number of bits between transitions, and thus the noise bandwidth of the phase-lock loop is dependent upon the characteristics of the NRZ signal.

b. Clock Stability

The stability of the bit generator is a primary factor in establishing the minimum allowable noise bandwidth of the phase-lock loop (Ref. 4). For this reason, attempts are made to set limits on the airborne bit frequency stability. The present Standards of the Inter-Range Instrumentation Group's (IRIG) Telemetry Working Group (TWG) (Ref. 5) state that the rate of change of bit rate should not exceed 0.1 percent of the nominal bit rate per second. A proposed revision of the Standards (Ref. 6) states that the spurious time displacement of bit phase in an interval T, relative to the frequency and phase established by an average over the preceding interval, T, shall not exceed 0.1 of the bit period. The interval T shall be taken as 10 times the interval between assured bit transitions.

The Standards also state that the change in frequency shall not exceed 1.0 percent of the nominal bit rate, which limits the long-time drift stability.

The following quotation from another proposal (Ref. 7) is more complete and appears to be better suited to the Standards:

> "A. Rise-Fall Time Jitter: The systematic difference between positive-going and negative-going transitions

shall not exceed 10% of a nominal bit period. This tolerance is in ADDITION to (B) and (C) below.

"B. WOW. The algebraic sum of the transition displacements, excluding systematic jitter, shall not exceed 20% of a nominal bit period over any 32-bit segment. No single transition, excluding jitter, shall be displaced more than 20%. Transition displacement is measured against the nominal extrapolated position from the preceding Standard Frame (2048 bits) and includes drift (if any).

"C. Offset and Drift:
C1. Type 1, 0.1% or less from calibration frequency.
C2. Type 2, 5% or less from calibration frequency.
The deviation is the average over any Standard Frame (2048 bits)."

Standards for bit-rate stability should, if possible, be stated in such a way that appropriate phase-lock-loop noise bandwidths can readily be determined.

3. DATA-FILTER BANDWIDTH

An additional factor to be considered in determining conditions for optimal performance of the phase-lock loop is the data-filter bandwidth. The phase-lock loop performance, as measured by the phase error, was found to be a function of data-filter bandwidth and the probability of transitions in the NRZ signal. One result of an independent study (Ref. 2) made as part of this project was to show that, for a transition probability of 0.5 (random bit stream), the data bandwidth necessary to produce minimum phase jitter was 0.8 of the bit rate. This study assumed square filter pass bands and rectangular NRZ signals.

4. SLIPPAGE OF VOLTAGE-CONTROLLED OSCILLATOR

A phenomenon known as slippage can occur in a phase-lock loop when the phase error between the VCO and the signal becomes sufficiently large for the VCO to slip a full cycle or more and to lock in again an integral number of cycles from its original position.

The characteristics of this phenomenon in NRZ signals differ from those in continuous-wave signals. Clock instability, noise, or a combi-

nation of the two, causes slippage and loss of sync more abruptly in a continuous-wave signal than in an NRZ signal. This is because, in an NRZ signal, long sequences of bits occur without transitions. During these times, the input-signal phase can drift away from the VCO phase, or noise can produce such large perturbations in the VCO phase that the sign of the error signal will reverse, thus producing a phase shift of one full cycle. Therefore, under threshold conditions of bit sync, slippages of plus or minus one bit are a frequent occurrence. In a later section, consideration is given to the mechanization of frame sync, wherein the effects of slippage are reduced.

B. CARRIER LOCK

1. FREQUENCY SYNCHRONIZATION

In telemetry applications, where a very stable bit frequency generator can be employed, an alternative technique (Ref. 2) is available for substantially improving the bit sync in a high noise environment. For this technique, the RF carrier frequency is generated synchronously with the bit frequency by multiplying up from the bit frequency. At the receiving station, the bit frequency is obtained by dividing down by the known factor from the RF carrier frequency.

This approach achieves its great advantage from the fact that a narrow-band phase-lock loop can maintain sync with the continuous-wave RF carrier to signal strengths of 30 db or better below that at which sync can be maintained by differentiation and rectification of the NRZ signal.

2. PHASE SYNCHRONIZATION WITH COHERENT BIT FREQUENCY

As long as sync is maintained with the RF carrier, the bit frequency will be reproduced with great precision. This, however, does not guarantee that the phase of the bit frequency will be properly aligned with the NRZ signal. This phase information must be obtained from the NRZ video signal and at an S/N ratio comparable to that required for sync on the NRZ signal alone. However, once this phase alignment is achieved, bit sync will be maintained as long as sync with the RF carrier is maintained.

The possibility of generating an RF carrier coherent with the bit frequency has become particularly attractive with the advent of solid-

state circuitry capable of frequency synthesis at frequencies in the kMc region. Significant power can now be produced at 2200 Mc by the use of varactor diodes in parametric multiplier circuits. Very simple, reliable, high-frequency dividing circuits can be constructed with tunnel diodes.

III. FRAME SYNCHRONIZATION

A. FRAME FORMAT

Pulse-code modulation is a time-multiplex system and thus consists of a time sequence of bits, representing sync information and data. One complete sampling of all major channels constitutes a major frame. Some data channels may be subcommutated and thus appear in the major frame once in each cycle of the subcommutator; however, this does not alter the structure of the major frame. A frame sync pattern usually appears in every frame to mark the beginning of each frame; however, this may also be subcommutated and appear less frequently. The group of bits representing a given channel is called a word. At one time it was considered desirable to accompany each word with one or more bits for sync purposes. Some existing systems still employ up to three bits per word for this purpose.

The frame format that will be assumed throughout this report appears in Figure 4. A single frame sync pattern of n bits appears at the beginning of each frame, and all other bits are assumed to be random.

B. SYNCHRONIZATION PATTERN DETECTION

1. LINEAR MATCHED FILTER

a. Recognition Probability

Frame sync requires the identification of a specific point or time in each frame. This permits a bits-per-frame counter to be synchronized with the frame, thus allowing identification of each bit in the frame and thereby decommutation of each channel. A suitable frame sync pattern and an appropriate pattern recognizer matched to this code will provide the necessary sync information.

Two types of pattern detectors were investigated in this study: the LMF and SRR. These pattern detectors represent two different detection philosophies. With the LMF, all bits of the sync pattern plus their associated noise are examined simultaneously before a recognition decision is made. The SRR requires that each bit plus its associated noise be examined separately and a corresponding noise-free bit (one or zero) be generated. The sequence of regenerated bits is now examined by the

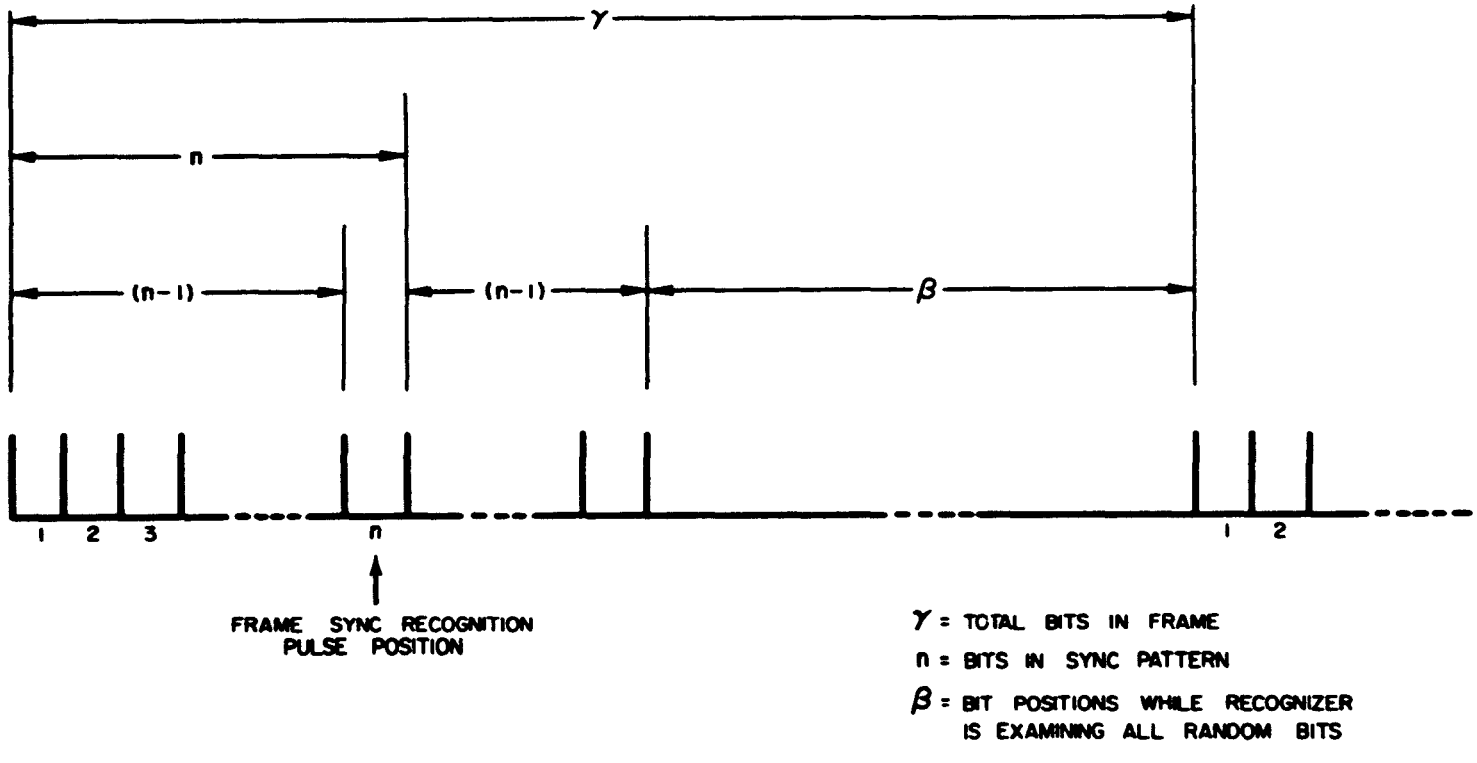


FIGURE 4. Frame Format

SRR. After the bits are detected on a bit-by-bit basis, either the LMF or the SRR could be employed with equal results; however, the SRR offers bit-rate flexibility that the LMF does not have and is therefore the logical choice. The SRR cannot be used satisfactorily on the undetected video signal.

One implementation of the LMF appears in Figure 5, where one-bit delay elements plus inverting (-) and noninverting (+) stages are used to cause all n bits to arrive at the output of the LMF at the same time and in the same phase. This particular LMF is designed to detect an 11-bit sync pattern and is matched to the 11-bit Barker (Ref. 8) code. If each bit passes through the LMF without attenuation or amplification, the output voltage in the absence of noise will be 11 times the peak of the NRZ for the pattern to which it is matched and less for all other patterns. The output voltage will be reduced by twice the peak of the NRZ signal for each bit that differs from the pattern to which it is matched. When every bit within the LMF differs from the matched pattern (i.e., when the complement code is examined), the output will again be 11 times the peak of the NRZ signal but opposite in sign. These voltages are with respect to the midpoint voltage of the NRZ signal, which is usually set at zero volts. For convenience, let it be assumed that the NRZ signal is balanced about ground and that the peak noise-free amplitude is 1 volt. When a noisy signal enters the LMF, all the noise associated with the n bits is superimposed on the output. It has been shown that, with Gaussian noise, the RMS noise at the output is $\sqrt{n}$ times the RMS noise at the input.

$$\sigma_o = \sqrt{n}\,\sigma_i \tag{4}$$

where

σ_i = RMS noise at input to LMF

σ_o = RMS noise at output of LMF

n = number of bits in sync pattern

In the absence of noise, a threshold set midway between the maximum and next-to-maximum outputs will be exceeded only for the code to which the LMF is matched, while the output for all patterns differing by one or more bits will fall below this level. In the presence of noise, the probability that recognition will not occur is given by the probability that the noise will be below the threshold at the time of observation. This probability is given by the area under the normal probability density curve between E_p and infinity.

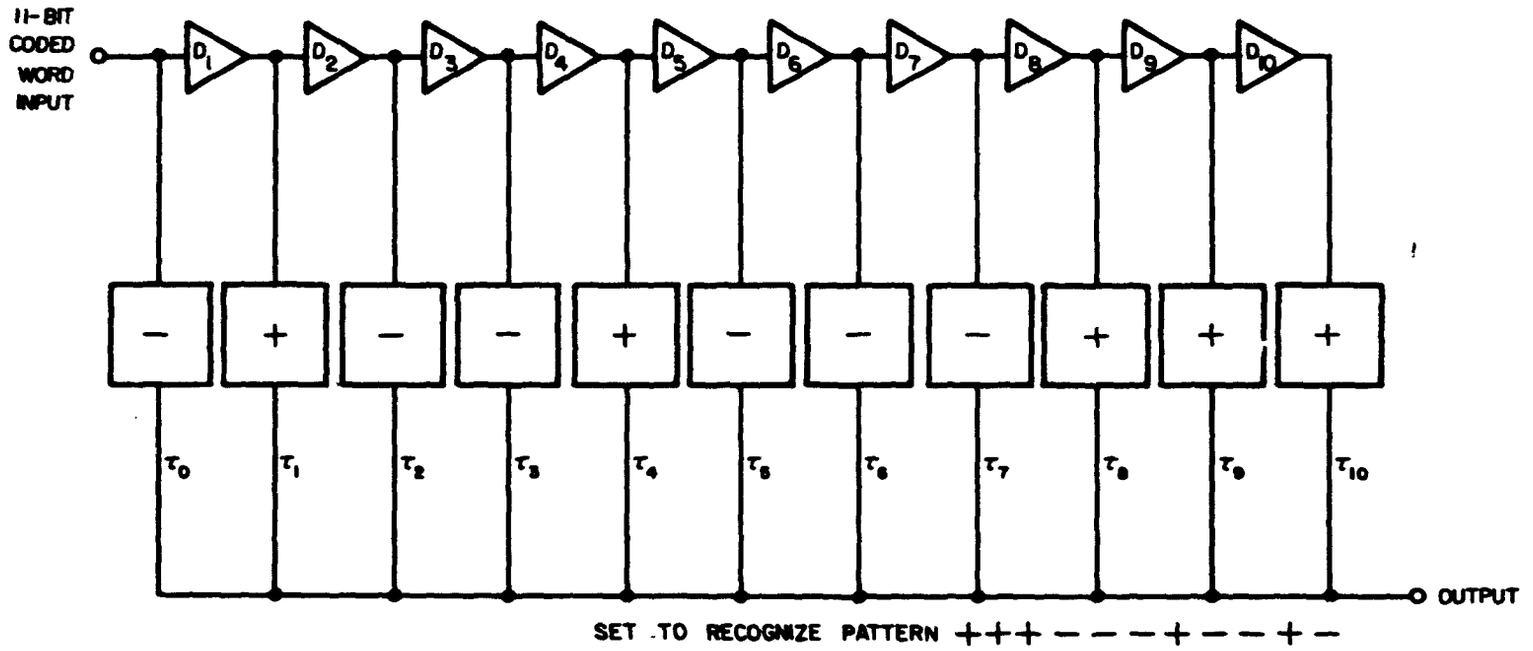


FIGURE 5. Linear Matched Filter (LMF)

$$P(N_o < E_p) = \int_{E_p}^{\infty} \frac{e^{-(N_o^2/2\sigma_o^2)}}{\sqrt{2\pi\sigma_o^2}} dN_o \qquad (5)$$

where

N_o = instantaneous amplitude of the noise at the output of the LMF

E_p = peak amplitude of the NRZ signal

The probability of recognition is given by the probability that the noise voltage will be above the threshold when the correct code is within the LMF and the threshold is set midway between the maximum and next-to-maximum levels.

$$P(N_o > E_p) = \int_{-E_p}^{\infty} \frac{e^{-(N_o^2/2\sigma_o^2)}}{\sqrt{2\pi\sigma_o^2}} dN_o \qquad (6)$$

Written in terms of the error function, which is easily found in mathematical tables, Equation (6) becomes, in more general form,

$$P_n(\epsilon)' = 1 - \tfrac{1}{2} \operatorname{erf}\left[\frac{(2\epsilon + 1)E_p}{\sigma_i\sqrt{n}}\right] \qquad (7)$$

where

$$\operatorname{erf} x = 2\int_x^{\infty} \frac{e^{-(x^2/2\sigma^2)}}{\sqrt{2\pi\sigma^2}} dx$$

$P_n(\epsilon)'$ = probability of recognition. (The prime distinguishes this expression from a similar one for the SRR.)

σ = RMS value of noise

ϵ = multiples of E_p at which threshold is set below maximum noise-free output of the LMF

When ϵ is equal to zero in the absence of noise, only codes agreeing exactly with the LMF will be recognized. When ϵ is equal to 1, all codes differing from the LMF by one or zero bits will be recognized, etc.

Equation (7) is the probability that the signal plus noise will be above a preset threshold at a given instant in time. In actual practice, the output of the LMF is observed through a time aperture of finite width. The probability that a noise waveform will exceed a given threshold at least once during a finite time is clearly greater than the probability for an instantaneous sample. This is related in a complex manner to the bandwidth of the noise spectrum and to the sampling aperture. Experimental and theoretical data for the LMF appear in Table 1. The difference between the theoretical and experimental data for $P_n(\epsilon)'$ is quite large, and it is not known whether or not this can be explained by the use of a finite sampling aperture; it is known, however, that the data are quite sensitive to the sampling aperture width. For the data in Table 1, the aperture was a one-bit period.

b. False-Synchronization Probability

Acquisition of frame sync is dependent primarily upon two quantities: the probability of recognition of the sync pattern as it is scanned, $P_n(\epsilon)'$; and the probability of a false-sync indication between sync patterns, $F_n(\epsilon)'$. It was assumed in this study that the data can traverse all possible code values. Even if the frame sync pattern were made unique with respect to the data, this condition would be maintained only in the absence of noise.

For analysis purposes, a random bit stream is assumed for all bits in the frame other than the sync pattern; i.e., the probability of a transition at the end of any bit period is 0.5. In the absence of noise, n + 1 discrete output levels are possible from the LMF. The probability that any one of these levels will occur can be calculated from one of the fundamental theorems of the Theory of Probability; namely, if p is the probability that an event will occur in a single trial, the probability that the event will occur exactly r times in n independent trials is

$$P_n(r) = C_r^n p^r q^{n-r} \tag{8}$$

where

$$q = 1 - p$$

$$C_r^n = \frac{n!}{r!(n-r)!}$$

Translating this to the problem at hand, if

p = probability that a bit disagrees with the LMF

k = number of bits agreeing with LMF = number assigned to the corresponding output level

then the probability that the kth level will exist at the output of the LMF for any group of random bits (p = 0.5) is

$$p_n(k) = (\tfrac{1}{2})^n C_k^n \tag{9}$$

For the kth level at the output of the LMF, a false-sync indication will occur only if the noise superimposed on the signal is sufficient to exceed the preset threshold. The probability of this occurring is

$$P(N_o > |2n - 1 - 2k - 2\epsilon|E_p) \tag{10}$$

The occurrence of the kth level and the noise exceeding a preset threshold are independent events, and thus the probability of their occurring simultaneously is the product of their respective probabilities.

$$P_n^{\epsilon}(k) = (\tfrac{1}{2})^n C_k^n P(N_o > |2n - 1 - 2k - 2\epsilon|E_p) \tag{11}$$

where

$P_n^{\epsilon}(k)$ = probability for random bits that the code will differ from the LMF by k bits and that the noise will at the same time exceed the threshold set at ϵ

There are $n + 1$ possible values for $P_n^{\epsilon}(k)$, and the associated events are mutually exclusive. Therefore, the probability that some one of them will occur is the sum of their respective probabilities.

$$F_n(\epsilon)' = (\tfrac{1}{2})^n \sum_{k=0}^{n} C_k^n P(N_o > |2n - 1 - 2k - 2\epsilon|E_p) \tag{12}$$

Writing this in terms of the error function, as defined previously, it becomes

$$F_n(\epsilon)' = \frac{1}{2^{(n+1)}} \sum_{k=0}^{n} C_k^n \operatorname{erf} \frac{|2n - 1 - 2k - 2\epsilon|E_p}{\sigma_i\sqrt{n}} \tag{13}$$

The data calculated from Equation (13) are compared with the experimental data in Table 1. Agreement is well within the expected experimental limits. It should be noted that the number of false-sync indications is high: about four per frame at S/N = 2, and about 30 per frame at S/N = 1.

2. SHIFT REGISTER RECOGNIZER

a. Bit Detection

(1) Sampling detector. The alternative approach to that of the LMF, which makes a simultaneous examination of n bits plus their associated noise, is to detect the bits individually and reconstruct the NRZ signal before pattern detection. A certain percentage of these bits will be in error, depending on the S/N, the bandwidth, and the type of detector used. To obtain a reconstructed NRZ signal with equi-period bits requires synchronous detection, and the simplest detector of this type is the sampling detector. This technique makes an individual examination of the video signal at an appropriate point in each bit interval. If the signal-plus-noise voltage is greater than zero, a one-bit is regenerated; if it is less than zero, a zero-bit is regenerated. An error will result if the instantaneous value of noise is greater than and opposite in sign to the signal at the time of sampling. The probability of such an error occurring is dependent upon the ratio of the peak signal at sampling to RMS noise. The peak signal is used here, rather than the RMS value, because the RMS value of an NRZ signal (after filtering) is dependent upon the average number of bits between transitions.

(2) Integrating detector. The sampling detector per se is not usually the optimal bit detector, since S/N can usually be improved by conditioning the video signal prior to sampling. An improved method for conditioning the signal prior to bit detection is to integrate over the bit period. A linear integrating detector is shown in Figure 6. The probability of an error in detection is given by

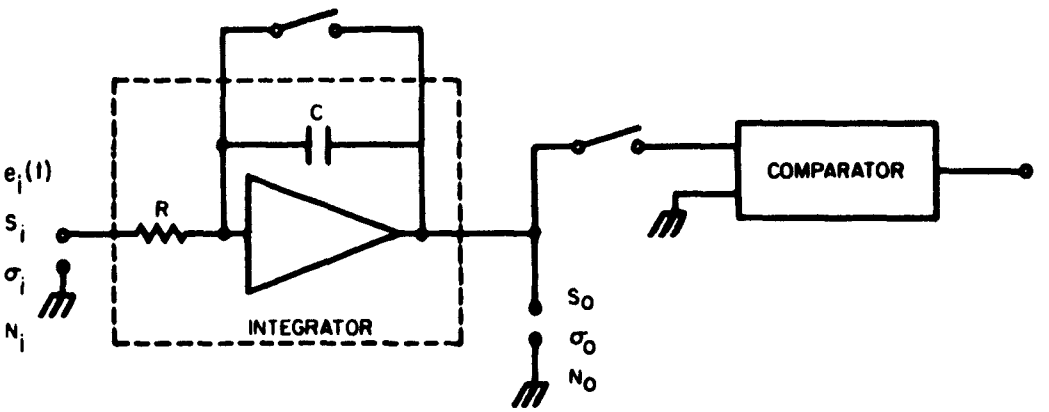
$$P(N_o > S_o) = \int_{S_o}^{\infty} \frac{e^{-(N_o^2/2\sigma_o^2)}}{\sqrt{2\pi\sigma_o^2}} \, dN_o \qquad (14)$$

where S_o is the signal amplitude at integrator output at end of integration period. This probability is decreased as the ratio S_o/σ_o is increased; therefore, it is desirable to maximize this ratio. If the signal energy in each bit period is equal, the probability of an error occurring is the same for all bits. The signal energy in each bit period is not equal,

TABLE 1. Experimental and Theoretical Data for the Linear Matched Filter and Shift Register Recognizer

Sync pattern = 11-bit Barker (11100010010); sampling aperture = 10 μs; signal = NRZ plus noise filtered at 150 kc; number of errors allowed (ε) = 0.

S/N	P	Linear Matched Filter				Shift Register Recognizer			
		$P_n(\epsilon)'$		$F_n(\epsilon)'$		$P_n(\epsilon)$		$F_n(\epsilon)$	
		Exp.	Theoretical	Exp. x 10^{-3}	Theoretical x 10^{-3}	Exp.	Theoretical	Exp. x 10^{-3}	Theoretical x 10^{-3}
2.11	0.001	0.97	0.74	2.60	2.36	0.004	0.011	0.466	0.474
1.96	0.003	0.95	0.73	2.50	2.76	0.045	0.032	0.457	0.474
1.64	0.01	0.94	0.69	3.92	4.17	0.11	0.11	0.464	0.474
1.40	0.02	0.93	0.67	5.33	6.45	0.22	0.20	0.455	0.474
1.15	0.05	0.92	0.64	11.09	10.94	0.46	0.43	0.441	0.474
0.95	0.09	0.90	0.61	19.93	18.63	0.64	0.66	0.465	0.474
0.85	0.12	0.89	0.60	24.10	26.30	0.75	0.75	0.442	0.474



NOTES:

$e_i(t)$ = INPUT SIGNAL AS A FUNCTION OF TIME

S_i = RMS SIGNAL AT INPUT

S_o = SIGNAL AMPLITUDE AT INTEGRATOR OUTPUT AT END OF INTEGRATION PERIOD

σ_i = RMS NOISE VOLTAGE AT INPUT

σ_o = RMS NOISE VOLTAGE AT OUTPUT OF INTEGRATOR

N_i = INSTANTANEOUS AMPLITUDE OF NOISE VOLTAGE AT INPUT

N_o = INSTANTANEOUS AMPLITUDE OF NOISE VOLTAGE AT OUTPUT

FIGURE 6. Linear Integrating Detector

however, when the data filter bandwidths are so narrow that the signal does not recover within one bit period after a transition. In this case, the average bit error probability will be a function of the average number of bits between transitions, as will be shown in the next section. Three cases will be considered where the signal energy in each bit period is constant and each bit consists of (1) a rectangular pulse, (2) a half sinusoid, or (3) a rectangular pulse filtered at 150 kc (i.e., 1.5 times the bit rate). The details for making the necessary calculations will not be given, but the method will be outlined and references cited. It is first necessary to calculate the RMS noise, σ_o, at the output of the integrator for the noise bandwidth at the input, by use of the following equation (Ref. 9, 10):

$$\sigma_o^2 = \int_0^\infty |H(j\omega)|^2 G(\omega)\, df \tag{15}$$

where

$H(j\omega)$ = transfer function of integrator

$G(\omega)$ = noise power spectral density at input to the integrating bit detector

Next, at the end of the integration period, the signal amplitude at the output of the integrator must be calculated from the equation

$$S_o = \frac{1}{RC}\int_0^\tau e(t)\, dt \tag{16}$$

where

S_o = signal amplitude at integrator output at end of integration period

$e(t)$ = time function of input signal

τ = period of bit frequency

Using Equation (14), the bit error probability can now be obtained by substituting the values found in Equations (15) and (16) and referring to mathematical tables of error functions. Six plots of bit error probability (p) versus S/N under different conditions appear in Figure 7. Curve I is a plot of the theoretical p for rectangular bit pulses; and, as would be expected, the p is less for a given S/N than for any of the other plots,

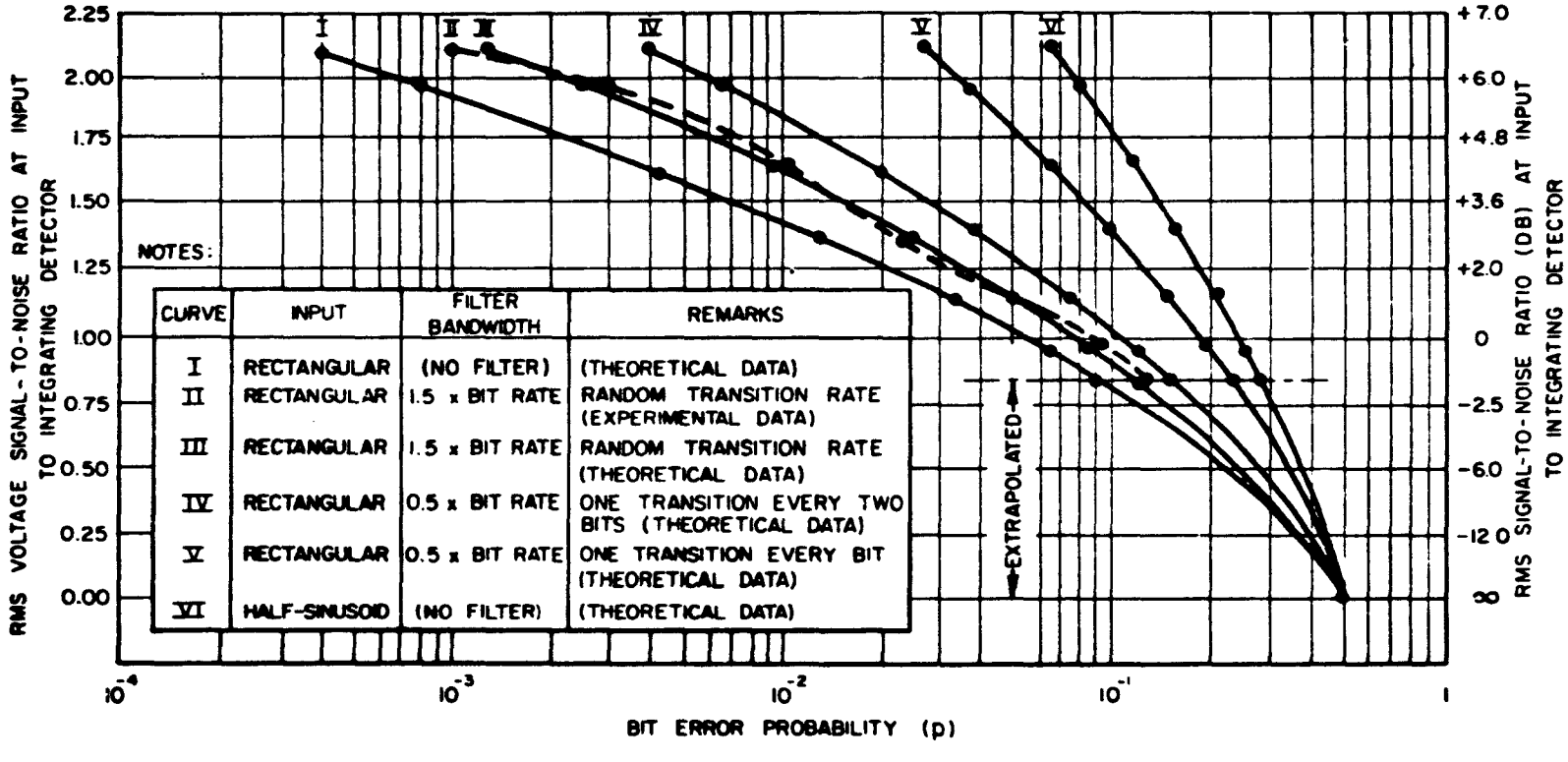


FIGURE 7. Bit Error Probability Versus Signal-to-Noise Ratio

since the signal energy per bit period is the maximum possible. Curve III is a plot of theoretical p for rectangular pulses filtered at 1.5 times the bit frequency. The leading-edge pulse characteristics were assumed to be the first quarter cycle of a sinusoid with a period of 6 ms. The experimental data taken with the 1.5 bit-rate filter appear in Curve II, and the agreement with Curve III is very good. Curve VI shows p for the case where the bit signal pulse consists of a half sinusoid. This curve shows the greatest p for a given S/N because the signal energy per bit period is the least for all signals considered. Actually, in this case, use of the integrating detector does not result in an advantage. If an instantaneous sample is taken at the peak of the half sinusoid, the probability of error would be less than results from sampling the signal at the output of the integrator. It is interesting to note that all the curves in Figure 7, if extrapolated, pass through a common point at S/N = 0 and p = 0.5. This is to be expected, since the weighing influence offered by the signal disappears as the signal approaches zero. With Gaussian noise alone, the bit decision is as likely to be a one as a zero.

(3) Data-filter bandwidths. Narrow data-filter bandwidths produce detrimental effects upon the bit detection process. If the filter bandwidths are such that substantial signal recovery between transitions is not possible, the probability of a bit error becomes a function of the past history of the NRZ signal. That is, the probability of an error in a given bit interval is dependent upon whether there was a transition at the end of the preceding bit interval, or even at the end of two or more bit intervals preceding it. The increased probability of error results from the decreased signal energy in some bit intervals. For a group of fixed bits, such as the frame sync pattern, nearly all errors will occur in a few particular bit positions. This difference was measured experimentally, using two 0.5-bit-rate filters, one simulating the premodulation filter and the other simulating the postdetection filter. The probability of error was found to be four or five times greater for some bit positions than for others. The large variation in p occurs in part because the energy associated with a given bit interval is displaced by an amount dependent upon the past history of the NRZ signal. This displacement precludes optimal phasing of the bit detector, and the best possible compromise is far from optimum for any given bit.

In general, the average p will be a function of the average number of bits between transitions. For the two 0.5-bit-rate filters, the average p was calculated for two cases (see Figure 7). Curve V represents data where a transition occurred at the end of every bit period. Curve IV shows the result of a transition at the end of every second bit period. The large separation between these two curves indicates the high dependence of p upon the average period between transitions for restricted data bandwidths.

Increased understanding of the detrimental effects of filtering at 0.5 of the bit rate can be gained by consideration of the spectrum of an NRZ signal. The highest square-wave frequency that can be produced is at 0.5 times the bit rate; i.e., for a 101010 . . . signal. The Fourier spectrum of a square wave consists of the fundamental and odd harmonics. The amplitude of the fundamental sine wave is 20 percent greater than the amplitude of the square wave. As filtering is imposed on the square wave sufficient to attenuate the harmonics of the spectrum, the fundamental will rise above the level of the square wave. Note that this is not a transient phenomenon but the emergence of the peak of the fundamental, which is normally reduced by the canceling effect of the harmonics. As the 3-db cutoff frequency of the filter is reduced to 0.5 times the bit rate, the peak amplitude of the fundamental frequency diminishes to 10 percent below the peak amplitude of the square wave. The result is that, for filtering at 0.5 times the bit rate, the signal energy per bit interval is reduced not only by the long rise times following transitions, but also by actual attenuation of the signal under the conditions of a transition in every bit period. Increasing the data-filter bandwidths allows the fundamental component to rise above the normal level of the NRZ signal, thus tending to compensate for the loss in signal energy caused by the finite rise times. It was found experimentally that, for data-filter bandwidths in the neighborhood of 0.8 times the bit rate or greater, the dependence of p on the transitions was negligible. The filters used were of the low-pass Butterworth type with bandwidths measured at the 3-db point and with terminal attenuations of 36 db per octave.

b. Recognition Probability

Recognition of the frame sync pattern in the regenerated NRZ signal does not require a linear device, such as the LMF with its inherent inflexibility to changes in bit frequency. The device to be discussed in this section is the SRR, which is composed of n bistable elements arranged in stages. Each element contains one of n sequential bits of the NRZ bit train for one bit period. At the end of the bit period, a new bit is introduced in the first stage and each stage transfers its bit to the following stage, with the nth stage discarding its bit. A block diagram of the SRR appears as Figure 8.

The SRR is so mechanized that each stage can supply a fixed increment of current to a linear summing network, depending upon whether the bit contained in that stage at that period is a one or a zero. Whether the current is supplied for a one or a zero can be predetermined. Thus, if the bit contained within a given stage agrees with that for which the SRR was preset, an increment of current will be supplied to the summing network and a fixed increment of voltage will appear at the output. If all bits agree with the pattern for which the SRR was preset, a voltage of n increments in amplitude will appear at the output; if one stage differs,

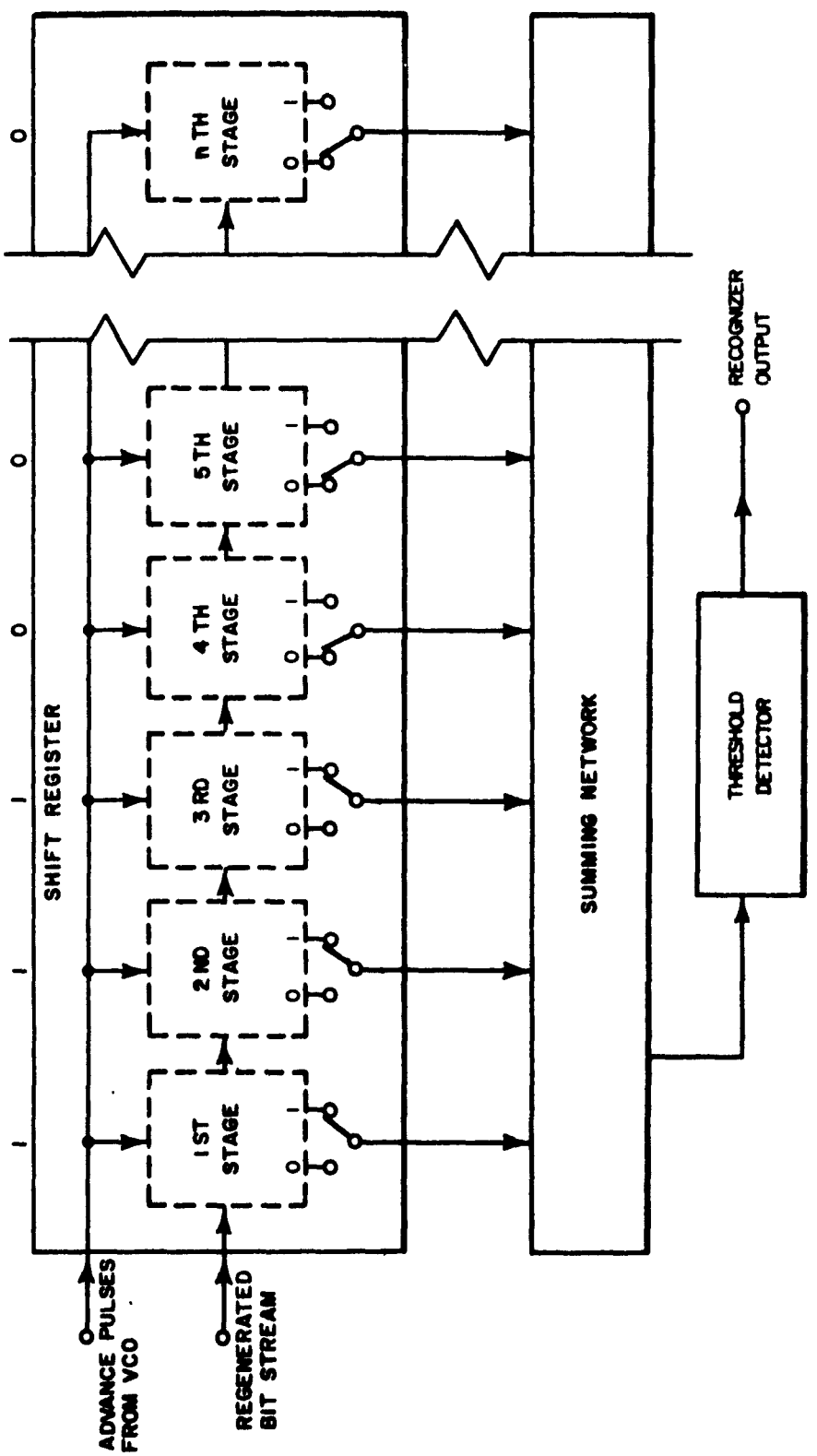


FIGURE 8. Shift Register Recognizer (SRR)

the output will be n - 1 increments in amplitude, etc. Thus, if the frame sync pattern is contained within the SRR, the output will be reduced one increment for each bit error within the frame sync pattern.

The probability that exactly r errors will occur in a particular sync pattern during the detection process is given by Equation (8). If it is predetermined that all patterns with ϵ or fewer errors shall be recognized, then the probability that ϵ or fewer errors will occur is given by the sum of the probabilities for each of these events, since they are mutually exclusive.

$$P_n(\epsilon) = \sum_{r=0}^{\epsilon} C_r^n p^r q^{n-r} \tag{17}$$

where

p = bit error probability

$q = 1 - p$

ϵ = maximum number of errors allowed by the SRR

$P_n(\epsilon)$ = probability that an n bit sync pattern will contain ϵ or fewer errors for a bit error probability of p

By setting the trigger level of a voltage threshold detector between the n and n - 1 levels at the output of the summing network, only sync patterns with no errors ($\epsilon = 0$) will be detected. If the threshold detector trigger-level is set between the n - 1 and n - 2 levels, all sync patterns with one or fewer errors ($\epsilon = 1$) will be recognized, and so on.

The probability of sync pattern recognition, $P_n(\epsilon)$, is a function of three parameters: the number of bits in the sync pattern, the number of errors allowed by the SRR, and the bit error probability. It is not evident from Equation (17) how $P_n(\epsilon)$ is affected by changes in n, ϵ, and p. Figure 9 shows a family of curves of $P_n(\epsilon)$ with n plotted along the ordinate and ϵ along the abscissa while p is held constant and equal to 0.02. $P_n(\epsilon)$ has meaning only for integral values of n and ϵ. The smooth curves in Figure 9 pass through points with $P_n(\epsilon)$ values that are very close to those indicated on the curves. Figures 10 and 11 show plots similar to those in Figure 9, except that p is held constant at 0.1 and 0.2, respectively. Families of curves for constant $F_n(\epsilon)$ also appear on these plots and will be discussed in the next section.

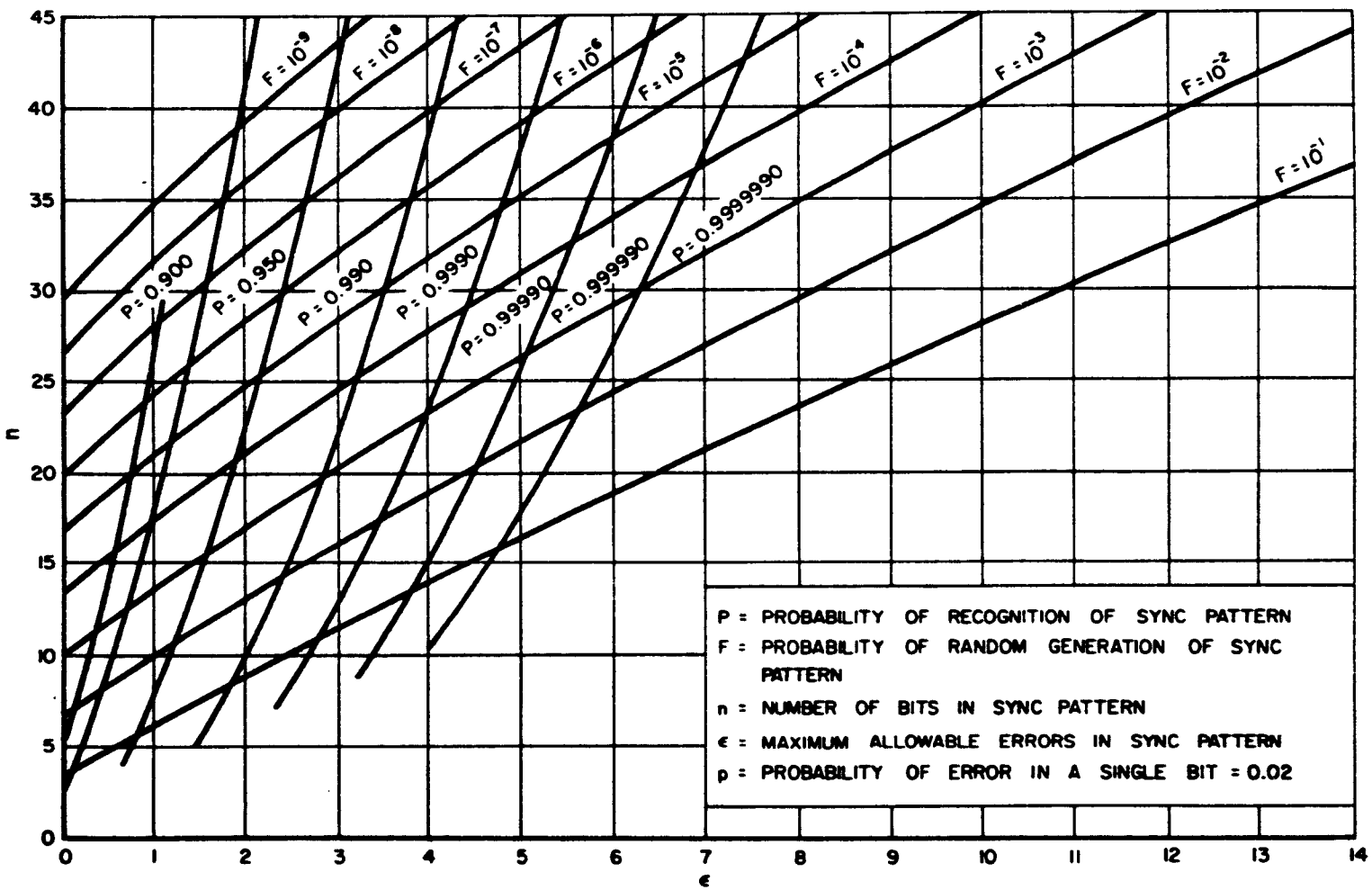


FIGURE 9. $P_n(\epsilon)$ and $F_n(\epsilon)$ Versus n and ϵ for p = 0.02

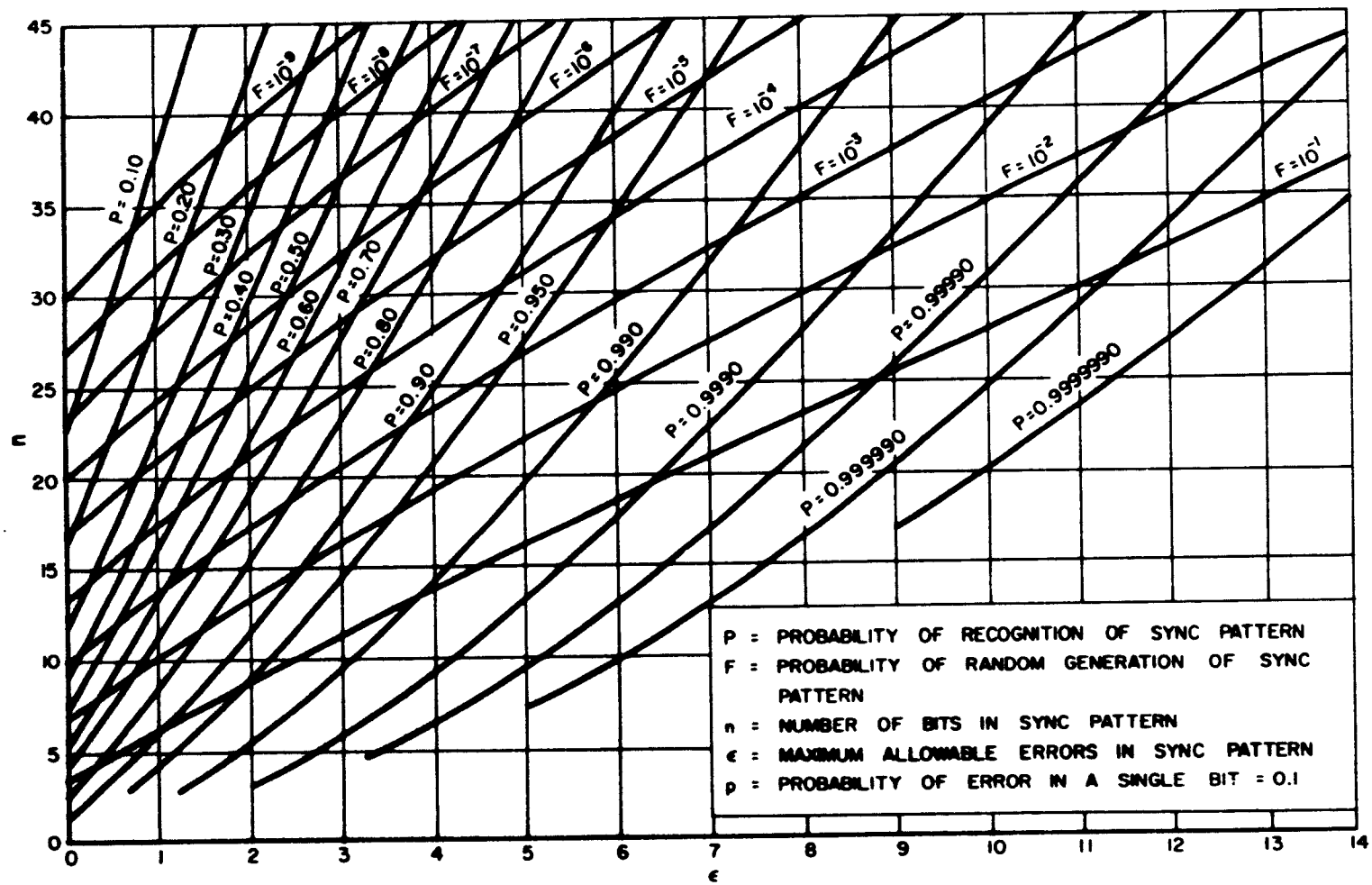


FIGURE 10. $P_n(\epsilon)$ and $F_n(\epsilon)$ Versus n and ϵ for p = 0.1

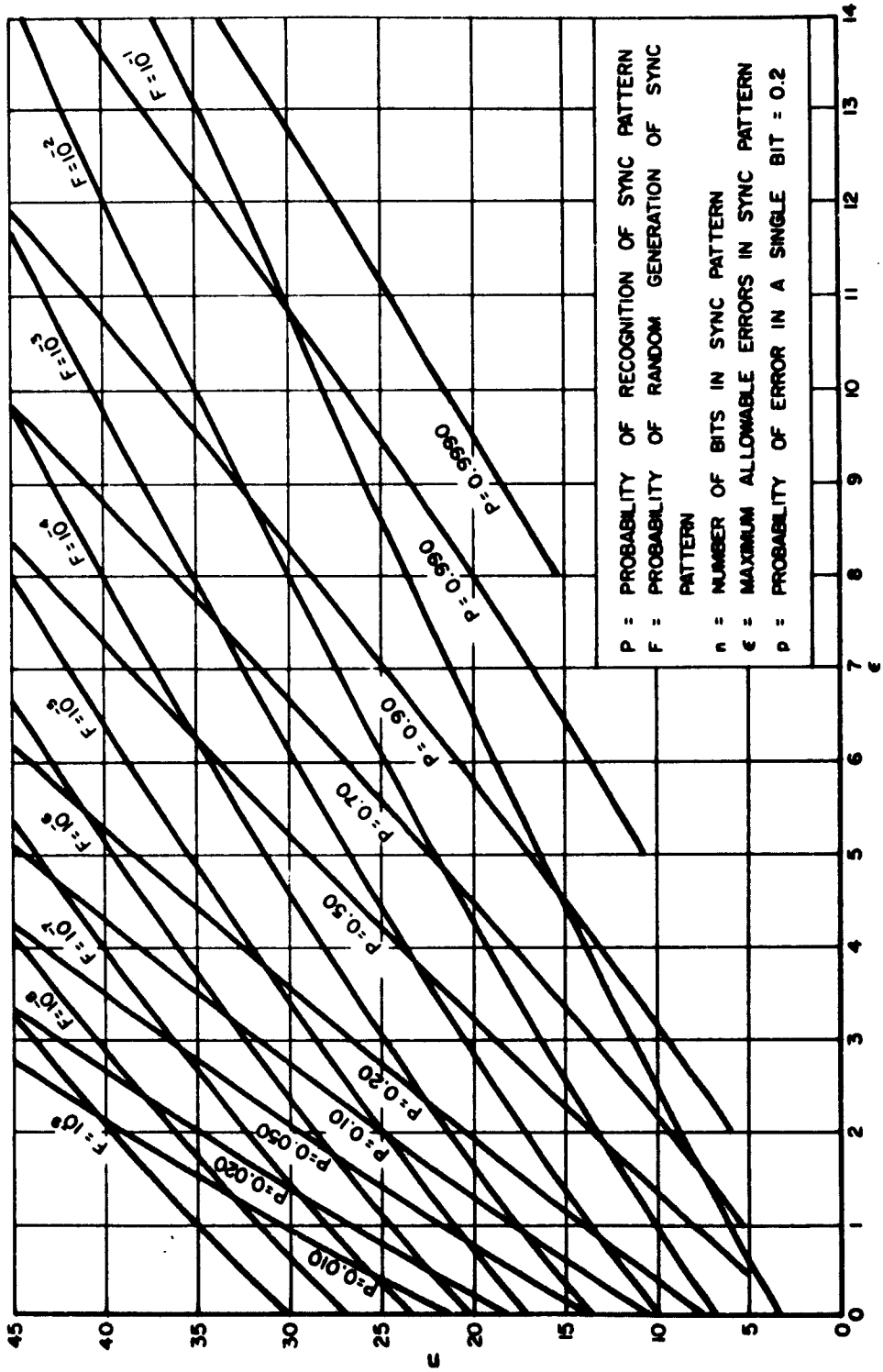


FIGURE 11. $P_n(\epsilon)$ and $F_n(\epsilon)$ Versus n and ϵ for p = 0.2

c. False Synchronization Probability

(1) Random bit stream. There is always a finite probability, in the presence of noise, that a false-sync indication will occur during the data portion of the frame. In this analysis, it is assumed that no attempt is made to exclude the frame sync pattern from the data. In fact, it is assumed that all bits, exclusive of the sync pattern, occur with equal chance of being a one or a zero.

There are two distinct conditions under which false-sync patterns can occur: (1) when the SRR is examining all random bits and (2) when it is examining simultaneously some bits belonging to the frame sync pattern and some random bits.

When the SRR is examining all random bits, the first important question is: What is the probability that a group of n random bits will differ from the frame sync pattern by no more than ϵ bits? This is given by Equation (17), where $p = q = 0.5$, which reduces to

$$F_n(\epsilon) = \frac{\sum_{r=0}^{\epsilon} C_r^n}{2^n} \tag{18}$$

where $F_n(\epsilon)$ is the probability that n random bits differ from the sync pattern by ϵ or fewer bits.

A second important question is: For a given length of frame, what is the probability (H_β) that one or more false-sync indications will occur during the random portion of the frame? The SRR examines β groups of n random bits per frame. If each of these groups were independent (i.e., contained no bits belonging to any of the other groups), the desired probability would be equal to one minus the probability that none of the groups were recognizable sync patterns. These groups are not independent, however, since each contains n - 1 bits of the preceding group. Nevertheless, as shown in the Appendix, the assumption of independence is a good approximation under the indicated conditions. The desired probability becomes

$$H_\beta = 1 - [1 - F_n(\epsilon)]^\beta \tag{19}$$

where

$$\beta \gg n$$

$$F_n(\epsilon) \ll 1$$

H_β = probability that one or more false-sync indications will occur in the random region per frame

(2) Displacement condition. In the previous section, the probability of a false-sync indication occurring when the SRR is examining all random bits was considered. This probability was not a function of the bit-error probability or of the frame sync pattern characteristics. Recognizable frame sync patterns can also occur in the displaced position when the SRR is overlapping the sync pattern and the random region. This latter probability is more complicated and involves the bit-error probability and the characteristics of the frame sync pattern employed.

When the frame sync pattern is contained entirely within the SRR, there is agreement in every bit position in the absence of errors. Recognition will result unless the number of errors within the sync pattern exceeds ϵ. When the bit stream is shifted a few bits from this position, however, there are generally many bits in disagreement with the SRR in the absence of errors in the sync pattern. In fact, the number of disagreements will generally be greater than ϵ; and, in this case, false recognition will never occur in the absence of errors. If, however, the number of disagreements within the sync pattern is less than ϵ, false recognition can occur (even in the absence of errors) by the proper distribution of the random bits within the SRR. In general, for a given displaced position, a false-sync indication can occur in a number of ways, depending upon the occurrence and distribution of errors within the frame sync pattern and the distribution of the random bits within the SRR. The equation that has been derived (and is further explained in the Appendix) is as follows:

$$H_b(\epsilon) = \left(\tfrac{1}{2}\right)^b \sum_{i=E_b-\epsilon}^{E_b} C_i^{E_b} p^i q^{E_b-i} \sum_{j=0}^{\epsilon-E_b+i} C_j^{n-E_b-b} p^j q^{n-E_b-b-j} \sum_{k=E_b+b+j-i-\epsilon}^{b} C_k^b \tag{20}$$

where

$$C_r^n = \frac{n!}{r!(n-r)!}$$

$C_r^n = 0$ when $r > n$ or $r < 0$ because the factorial of a negative number equals ∞ and 1 over ∞ equals 0

$H_b(\epsilon)$ = probability that a false-sync indication will occur for a displacement of b bits and for a code with E_b disagreements within the SRR for that displacement

b = number of bits displaced from the position where the frame sync pattern is entirely contained within the SRR

E_b = number of bits, belonging to the frame sync pattern and contained within the SRR, which are in disagreement with the SRR for a displacement of b bits

p = bit error probability

ϵ = number of errors allowed by the recognizer

q = 1 - p

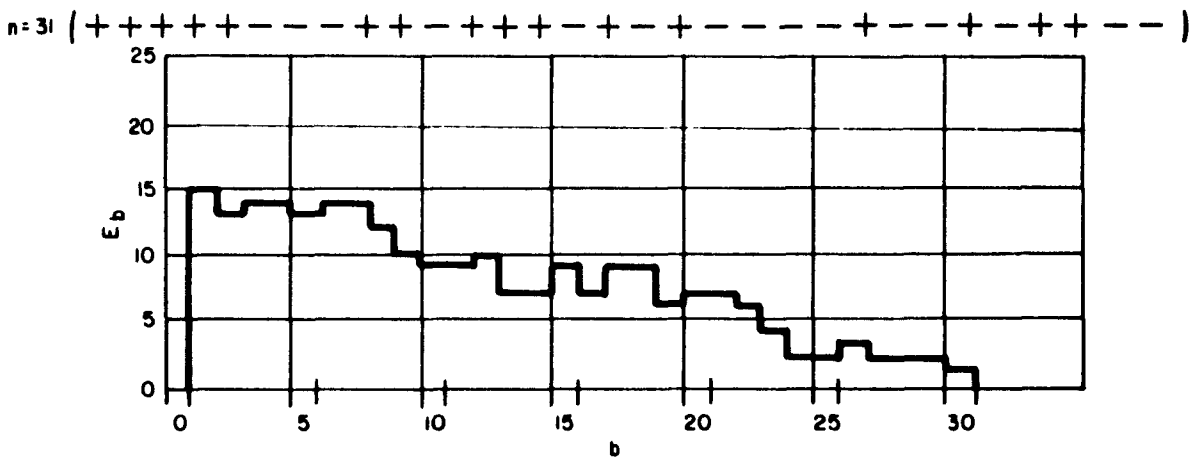
i, j, k = summation indexes

The probability of a false sync occurring as given by Equation (20) can vary greatly for the various displacement positions, depending upon the characteristics of the sync pattern. Figure 12 shows a plot of E_b versus b for a particular 31-bit sync pattern that will be discussed in a later portion of this report. A plot of the correlation function A_b also appears in Figure 12. This function is defined as the number of agreement bits minus the disagreement bits belonging to the sync pattern and contained within the SRR for each displacement position.

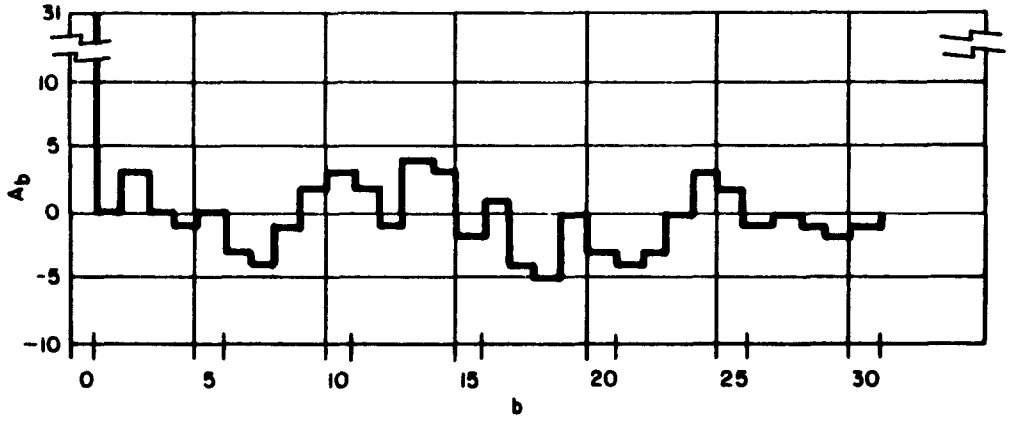
A probability that will be required in later developments is that one or more false-sync indications will occur in the n - 1 displacement positions on either side of the true sync position H_δ (refer to Figure 4). The probability that a false-sync indication, in a given displacement position, will occur is given by Equation (20). There are 2(n - 1) displacement positions for each scan of the frame sync pattern. The occurrences of false-sync indications in the displacement positions are not independent as justified in the Appendix; however, the assumption of independence results in a good approximation. Therefore, the probability of one or more false-sync indications in the 2(n - 1) displacement positions, to a good approximation, is given by

$$H_\delta \cong 2 \sum_{b=1}^{n-1} H_b(\epsilon) \qquad (21)$$

This equation can assume a wide range of values for a given length of pattern, depending upon the criterion under which the sync pattern was selected.



NUMBER OF ERRORS (E_b) IN PATTERN REQUIRED TO DISPLACE n-BIT PATTERN (b) BITS



AUTOCORRELATION FUNCTION $A_b = n - b - 2E_b$

FIGURE 12. Code 1 (One-Bit Aperture)

(3) Total false synchronization probability. The probability of one or more false-sync indications occurring during the data or random bit portion of the frame is given by Equation (19). The probability that at least one false-sync indication will occur during the overlap or displacement region of the frame is given by Equation (21). The events represented by these probabilities are independent; accordingly, the probability that one or the other or both will occur in any single frame is

$$H_\gamma = 1 - (1 - H_\beta)(1 - H_\delta) \tag{22}$$

Thus, H_γ is the total probability that one or more false-sync indications will occur in each frame.

C. FRAME SYNCHRONIZATION LOGIC

1. ACQUISITION

a. Choice of Synchronization Pattern

After bit sync is obtained, the time to acquire frame sync is dependent upon two independent events: the occurrence of false-sync indications and recognition of the correct frame sync pattern.

False-sync indications can occur in two distinct regions of the frame: the displacement (or overlap) region and the random region. The probability of false-sync indications in the random region is independent of the choice of sync pattern; and the probability of one or more such indications per frame is given by Equation (19). The probability of at least one false-sync indication in a displaced position is given by Equation (21) and is a definite function of the choice of codes. For some very poor choices of codes (such as all ones, all zeros, or alternating ones and zeros), H_δ can be large compared to H_β. On the other hand, there are in general many codes for a given length such that H_δ is small compared to H_β.

If H_δ is small compared to H_β, the probability of a false-sync indication is almost entirely dependent upon H_β, as can be seen from Equation (22). If a code chosen is such that this condition is satisfied, then the acquisition of sync becomes dependent only upon H_β and the probability of recognition $P_n(\epsilon_1)$. The condition that H_δ is small compared to H_β is assumed to be satisfied in the following development.

b. Acquisition Time

Frame sync is herein defined as the synchronizing of a bits-per-frame counter with the frame rate. This is accomplished when the bits-per-frame counter is reset at the time of frame sync recognition, either by the frame sync pulse or by reset pulses generated within the counter. From the recognizer, there is a continuous sequence of sync pulses, each of which is indistinguishable from the others on an individual basis. The true-sync pulses are distinguishable from the false-sync indications only by the fact that the true-sync pulses occur only at integral multiples of the frame rate while the false-sync pulses occur in a random manner. If the bits-per-frame counter were reset by every output pulse from the recognizer, frame sync would be lost every time a false-sync pulse occurred, and it would never be known with any certainty whether the system was "in sync" or "out of sync." As a means of avoiding this difficulty, the output of the recognizer is inhibited from resetting the bits-per-frame counter for one full frame after the receipt of a sync pulse. The output of the recognizer is again observed for one bit period at the end of this frame period. If the first pulse were a true-sync pulse, the probability of a second pulse occurring exactly one frame removed from the first is high for a true-sync pulse and low for a false-sync pulse. This is because, for reasonable values of bit error probabilities, $F_n(\epsilon_1)$ is low and $P_n(\epsilon_1)$ is high. In the presence of noise, the probability of recognizing the frame sync pattern is less than unity, so it may be desirable to observe the recognizer output for more than one frame period after the initially received recognizer pulse. The particular acquisition logic employed is dependent upon additional factors and will be discussed later.

Initial acquisition time is defined as the average number of frames occurring after bit sync and before the first true-sync pulse resets the bits-per-frame counter. The expression for initial acquisition time will be derived in the section that follows.

The probability that an individual sync pattern will be recognized is $P_n(\epsilon_1)$. Therefore, on the average, $1/P_n(\epsilon_1)$ sync patterns must be scanned for each one that is recognized and henceforth will be denoted by α_0.

$$\alpha_0 = 1/P_n(\epsilon_1) \tag{23}$$

The subscript (1) on ϵ refers to the acquisition phase and distinguishes it from the retention phase to be discussed later.

Let it be assumed that bit sync is acquired, on the average, in the middle of a frame. (This assumption is valid, since it is as likely to occur at one point in the frame as at another.) Starting in the middle of

a frame, $(\alpha_0 - \frac{1}{2})$ frames must be scanned in order to observe α_0 sync patterns. Therefore, if no false-sync pulses were present, exactly $(\alpha_0 - \frac{1}{2})$ frames, on the average, would be required for frame sync. However, when false-sync pulses are present, one full frame is gated out (by the inhibiting gate on the recognizer) for each false-sync pulse received. As expressed in Equation (18), $F_n(\epsilon_1)$ is the probability that any group of n random bits will assume a recognizable sync pattern in the acquisition phase; hence, the expected number of false-sync pulses encountered in scanning $(\alpha_0 - \frac{1}{2})$ frames is $\beta(\alpha_0 - \frac{1}{2})F_n(\epsilon_1)$, since there are β groups of random bits per frame. Thus, the average number of frames required for initial acquisition of frame sync is

$$\alpha_1 = (\alpha_0 - \tfrac{1}{2})[1 + \beta F_n(\epsilon_1)] \tag{24}$$

where $F_n(\epsilon_1) << 1$. Equation (24) was derived on the assumption that the gate inhibiting the recognizer was open at the time that bit sync was acquired. This is a good assumption, provided that the number of false-sync pulses per frame is small compared to unity. When frame sync is lost after initial acquisition, the average number of frames necessary to reacquire frame sync is derived in the same manner as for Equation (24), except that the inhibit gate is closed initially. The acquisition time after loss of frame sync is therefore:

$$\alpha_{01} = \alpha_0 + \tfrac{1}{2} + \beta(\alpha_0 - \tfrac{1}{2})F_n(\epsilon_1) \tag{25}$$

which is seen to be one more frame than for Equation (24).

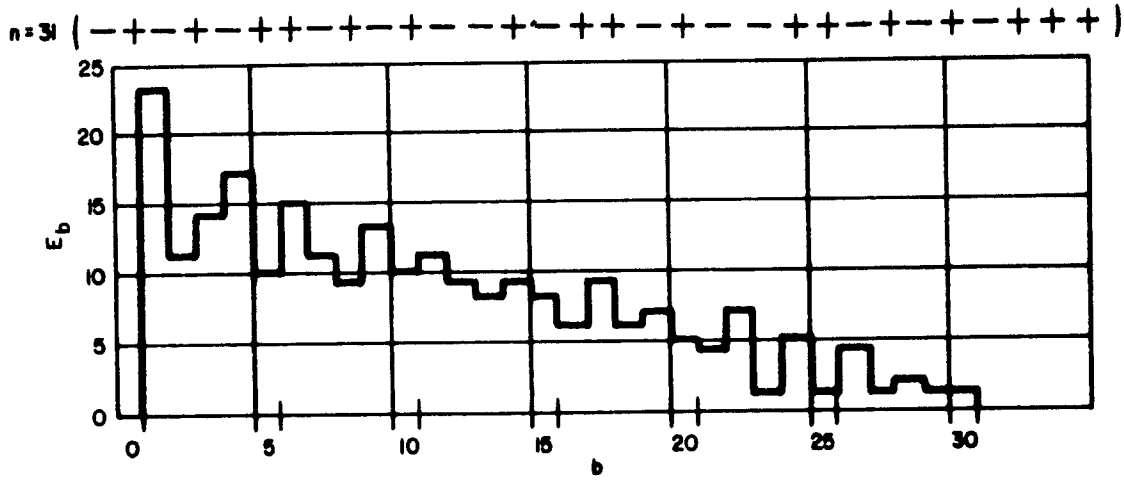
c. Recognition Probability Versus False Synchronization Probability

(1) Length of synchronization pattern. As indicated in Equation (24), for a given frame length, the time to acquire frame sync is a function of two quantities: the probability of recognition and the probability of random generation of the sync pattern. Equation (24) assumes that $H_\delta << H\beta$; and, under this assumption, the acquisition time is independent of the particular code selected for frame sync. Examination of Equation (24) reveals that the minimum possible value of α_1 is one-half frame, which is achieved when $P_n(\epsilon_1)$ equals unity and $\beta F_n(\epsilon_1)$ is small compared to unity. Normally, it will not be desirable to approach this limiting value; but reasonably short acquisition times may be achieved by proper choice of parameters. Nonetheless, the acquisition time can be made almost any value by proper choice of parameters. Once the frame length and

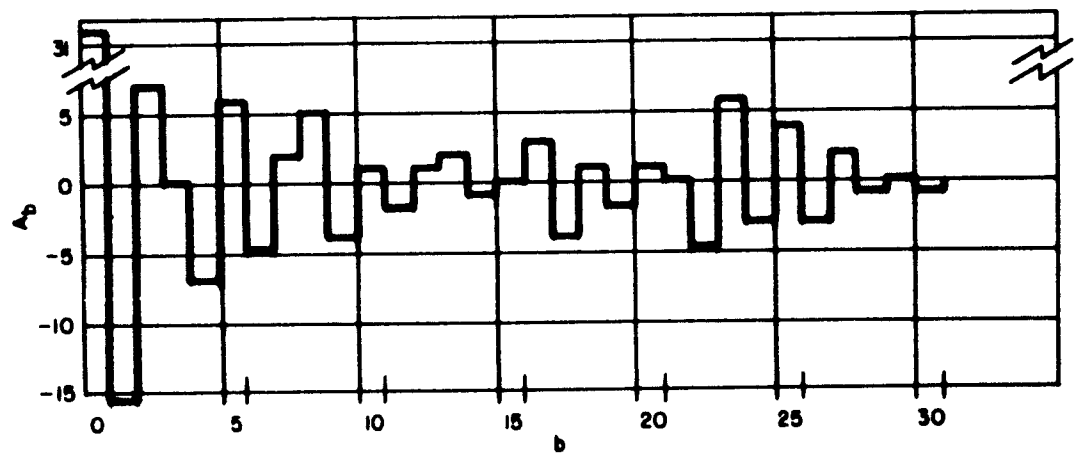
bit error probability are established, the only remaining parameters are the length of sync pattern and the number of allowed errors. A plot such as that shown in Figure 10 is very useful in selecting desired values for these parameters. For a given value of n, it is possible to make $P_n(\epsilon_1)$ as near unity as desired by increasing ϵ_1. However, $F_n(\epsilon_1)$ becomes very large if this is carried too far, canceling the benefit resulting from the increase in $P_n(\epsilon_1)$. Equation (24) shows how α_1 can become very large if $\beta F_n(\epsilon_1)$ becomes large compared to unity, e.g., if $F_n(\epsilon_1)$ increases. As Figure 10 shows, all $P_n(\epsilon_1)$ and $F_n(\epsilon_1)$ curves intersect for some value of n and ϵ_1, so proper choice of n and ϵ_1 will give almost any desired value of $P_n(\epsilon_1)$ and $F_n(\epsilon_1)$. Theoretically, α_1 could thus approach its minimum as closely as desired, but such practical considerations as n dictate a compromise.

(2) Multiple correlation peaks. Satisfactory acquisition time is dependent upon a favorable relationship between recognition probability and false sync probability. The detection criterion employed thus far requires that the positive correlation peak exceed some preset threshold level, which is determined by the number of errors, ϵ_1, allowed by the recognizer. The level of the positive correlation peak is determined by the number of errors in the frame sync pattern or, in general, by the number of bits that disagree with the code for which the recognizer was set.

Examination of the correlation function of a three-bit aperture code, such as the one plotted in Figure 13, shows that the positive correlation peak is preceded and followed by a large negative correlation peak. The possibility of incorporating these negative correlation peaks, as well as the positive peak, into the detection logic has been suggested. The amplitude of the negative correlation peaks is determined by the number of bits within the recognizer that are in disagreement when the sync pattern is displaced by one bit from the recognition position. The amplitude of the negative correlation peak preceding the positive correlation peak is closely related to the one following; and, for this discussion, the use of only one peak will be considered. In the absence of errors, when the correct pattern is displaced one bit, there generally will be n_d bits in disagreement and n_a bits in agreement with the stored pattern in the recognizer. For a one-bit displacement, one sync pattern bit has been shifted out of the recognizer and one random bit has been shifted in. Therefore, the sum of n_d and n_a is one less than n. In the presence of bit errors, some of the errors will occur among the n_d bits and some among the n_a bits. The amplitude of the negative correlation peak will be decreased for an error among the n_d bits and increased by an error among the n_a bits. Thus, for a given number of errors in the sync pattern, the amplitude of the negative correlation peak will depend upon the distribution of errors among the original agreement and disagreement bits. Hence, for a given number of errors within the sync pattern, a number



NUMBER OF ERRORS (E_b) IN PATTERN REQUIRED TO DISPLACE n-BIT PATTEN (b) BITS



AUTOCORRELATION FUNCTION $A_b = n - b - 2E_b$

FIGURE 13. Code 2 (Three-Bit Aperture)

of different amplitudes of the negative correlation peak will be possible. Paraphrased, for a given amplitude of the positive correlation peak, a number of different amplitudes of the negative correlation peak will be possible. It is apparent, therefore, that the negative correlation peak contains information in addition to that carried by the positive correlation peak.

The detection logic necessary to incorporate both the positive and negative correlation peaks can be mechanized by the use of two threshold detectors: one to detect the positive peak and one to detect the negative peak. Recognition is achieved only when the negative peak falls below a preset negative level and is followed one bit period later by the positive peak rising above a preset positive level.

Under these assumptions, theoretical expressions were derived for the recognition probability and false sync probability. Experimental data were taken to verify the theoretical data, and the results appear in Table 2. The probabilities incorporating the negative peak, as distinguished from those for the positive peak only, are designated by the capital letter N suffixed to the quantity. The parameter, ϵ_1, has the usual meaning and establishes the threshold of the positive correlation peak detector. The quantity, ϵ_3, establishes the setting of the threshold detector for the negative correlation peak. When the number of bits in disagreement within the recognizer is ϵ_3 or more, the negative correlation peak will extend below the negative threshold level. The agreement between the theoretical and experimental data is sufficient to warrant confidence in the results.

The recognition and false sync probabilities for the positive correlation peak alone are also given in Table 2. For the code employed in taking these data, the number of disagreements in the absence of errors, ϵ_1, is 16. For low values of ϵ_1 and for ϵ_3 equal to 16 or less, there is little change resulting from incorporation of the negative correlation peak, as is to be expected. However, as ϵ_1 is increased, both $P_n(\epsilon)N$ and $F_n(\epsilon)N$ decrease relative to $P_n(\epsilon)$ and $F_n(\epsilon)$. The percentage of reduction in $P_n(\epsilon)$ is about the same as for $F_n(\epsilon)$.

The reduction in $F_n(\epsilon)$ is beneficial; however, the reduction in $P_n(\epsilon)$ is not desirable. The true measure of the value of these changes is in their effect upon quantities such as the acquisition (α_4) and the fraction of frames out of sync (λ_D). These quantities were discussed in detail for Dual-Mode System, Equations (34) and (40), and were calculated for the conditions stated in Table 2. It was found that no improvement resulted in acquisition time, and that improvement in λ_D was less than 15 percent. The recognition logic for the retention mode assumed use of the positive correlation peak only.

TABLE 2. Comparative Negative Correlation Peak Data

Length of pattern (n) = 22; number of disagreements in the negative correlation peak with no errors in the pattern (E_1) = 16; binary sync pattern = (10101001010110010011001).

ϵ_1	ϵ_3	Positive and Negative Peaks				Positive Peaks Only	
		Theoretical		Experimental		Theoretical	
		$P_n(\epsilon)N$	$F_n(\epsilon)N$ x 10^{-6}	$P_n(\epsilon)N$	$F_n(\epsilon)N$ x 10^{-6}	$P_n(\epsilon)$	$F_n(\epsilon)$ x 10^{-6}
0	16	0.098	0.24	0.10	0.5	0.098	0.24
1	16	0.25	3.5	0.25	3.1	0.339	5.48
1	15	0.33	5.4	0.32	4.9	0.339	5.48
1	14	0.33	5.4	0.34	5.7	0.339	5.48
2	16	0.37	2.7	0.29	28.0	0.620	60.5
2	15	0.53	4.3	0.51	41.1	0.620	60.5
2	14	0.60	5.7	0.58	55.1	0.620	60.5
3	16	0.43	1.5	0.63	172	0.828	428
3	15	0.64	2.4	0.60	231	0.828	428

Under the conditions of this investigation, incorporating the negative correlation peak into the recognition logic appears to result in no significant advantage. The results are presented here only because they suggest the possibility of significant advantage with the use of more complex sync pattern recognition logic. It is possible that codes can be found which, when used with a special recognition scheme, would lead to improved sync performance.

d. Static Data Problem

For purposes of mathematical analysis, it has been assumed that all bits not assigned to the frame sync pattern are random. Under this condition, the probability of two false-sync pulses separated by one frame period in two successive frames is very small, and the probability of several false-sync pulses occurring at the frame rate in successive frames for random bits is too small to be considered.

The low probability of false-sync pulses occurring at the frame rate for random bits results from the statistical independence in the bit distributions from frame to frame. In practice, this independence does not necessarily exist, since some data channels may change very slowly, thus perpetuating essentially the same bit distribution for many successive frames. Since ϵ_1 errors are allowed in the sync pattern during the acquisition phase, any group of n bits that differ from the frame sync pattern by no more than ϵ_1 bits will be recognized. It is not feasible to exclude all recognizable patterns from the encoded data. Therefore, if a frame sync pattern is placed in every frame, it is impossible to distinguish it from a group of data bits that by chance assume a pattern within ϵ_1 errors of the sync pattern. Any system designed to synchronize on a frame sync pattern in every frame can also sync on slow moving data, thus preventing the acquisition of proper frame sync for long periods of time.

Several techniques are available for making the frame sync pattern sequence distinguishable from the data. Replacing the sync pattern with its complement in alternate frames is a satisfactory alteration of format to permit this distinction. The recognizer output then will reveal positive and negative correlation peaks alternating at the frame rate. For such a format, the frame sync logic must be designed to detect this positive-negative sequence and to ignore peaks that are not alternately positive and negative at the frame rate. The chance of a data word alternating between a given code and its complement in alternate frames is extremely small.

The beginning of a subcommutated frame is usually marked by a second sync pattern. An alteration of the above technique that provides the subcommutation marker without the addition of a second sync pattern is to inhibit the alternation of the major frame code-complement in the

major frame in which the subcommutated frame begins (Ref. 7). Note that this produces a 180-deg phase shift in the frame sync pulse sequence (e.g., code, complement, code, code, complement, code, complement, etc.).

Another format that permits discrimination between data and frame sync information is to insert a sync pattern in every other frame (Ref. 7). Thus, the frame sync pulses will occur at half the frame rate while false-sync pulses from slow moving data will occur at the frame rate. The frame in which the subcommutation frame begins can also be marked by repeating the sync pattern in two successive frames.

2. VERIFICATION

If transition from the acquisition to the retention phase is made falsely, the conditions imposed by the latter may imply too great a time loss before the system could return to the acquisition phase. For this reason, a verification phase usually is desirable after acquisition. Such a verification phase precludes entering the retention phase until there is a high probability that the system is in frame sync. A simple verification condition is to require that a predetermined number of consecutive recognizer pulses occur at the frame interval. Several such criteria will be discussed later.

3. RETENTION

The retention phase is a period of operation when it is believed that the system is in frame sync, this being known with a probability dependent upon the frame sync logic employed. Once in the retention phase, the system will remain there until the retention phase criterion is no longer satisfied; such failure to satisfy the retention criterion reverts the system to the acquisition phase. Rather stringent conditions are imposed in the retention phase; and for this reason, a verification phase may be used to avoid entering retention falsely.

Failure to satisfy the retention criterion can result from two conditions: (1) failure to recognize the frame sync pattern and/or (2) loss of the frame sync. The first condition is termed a "false alarm" because it may or may not involve a loss of frame sync.

a. Single-Mode System

A single-mode system is one in which the frame sync logic does not employ a change in the recognition probability between the acquisition and verification phases on the one hand and the retention phase on the

other. For the implementation employed in this experimental investigation, the retention phase is represented by a gate that inhibits the output of the recognizer for one full frame. The system enters the retention phase on the first pulse from the recognizer with no attempt to identify it as true or false. One frame after the pulse is received, the inhibit gate opens and the system will remain in the retention phase only if a recognizer output occurs at this time to reset the inhibit gate. A block diagram of the single-mode frame sync system appears in Figure 14.

The single-mode system can lose frame sync in any one frame if the following two conditions are satisfied: (1) failure to recognize the sync pattern, which allows the inhibit gate to open; (2) the occurrence of one or more false-sync pulses in that frame. The simultaneous occurrence of these two events allows the bits-per-frame counter to be reset in an improper phase. These two events are independent; thus, the probability that they will occur in the same frame is the product of their individual probabilities. The probability that the frame sync will not be recognized is $[1 - P_n(\epsilon)]$, and the probability that at least one false-sync pulse will occur in the frame is H_γ. Therefore, the probability that frame sync will be lost in any given frame is

$$L_\gamma = [1 - P_n(\epsilon)]H_\gamma \tag{26}$$

Since H_β is usually large compared to H_δ, it is seen from Equation (22) that, under these conditions, Equation (26) becomes approximately

$$L_\beta = [1 - P_n(\epsilon)]H_\beta \tag{27}$$

Thus, the system is intermittently in and out of sync in a manner dependent upon the distribution of false-sync pulses and recognition pulses. Equation (25) gives the average number of frames necessary to reacquire sync each time it is lost. A measure of the performance of the system is given by the ratio of the average number of frames that the system is out of sync to the total number of elapsed frames:

$$\lambda_s = \frac{\alpha_{01}}{1/L_\beta + \alpha_{01}} = \frac{\alpha_0 + \frac{1}{2} + \beta(\alpha_0 - \frac{1}{2})F_n(\epsilon)}{1/L_\beta + \alpha_0 + \frac{1}{2} + \beta(\alpha_0 - \frac{1}{2})F_n(\epsilon)} \tag{28}$$

where $F_n(\epsilon) << 1$. Under the conditions that $P_n(\epsilon) >> \beta F_n(\epsilon)$, Equation (28) can be simplified to the approximate equation:

$$\lambda_s = \frac{\alpha_0 + \frac{1}{2}}{1/L_\beta + \alpha_0 + \frac{1}{2}} \tag{29}$$

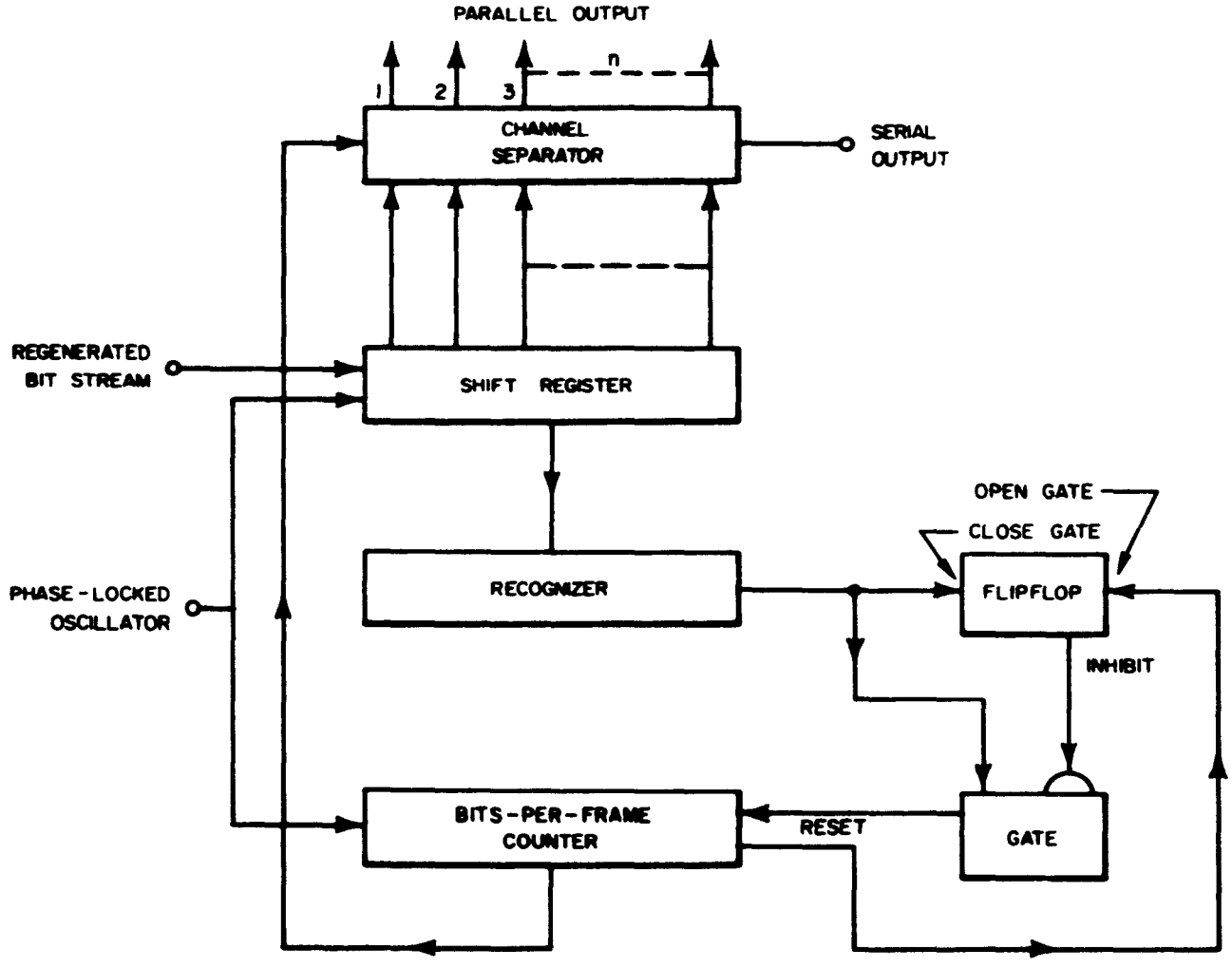


FIGURE 14. Single-Mode Frame-Synchronization System

Performance of the single-mode system can be improved by imposing a more restrictive condition for remaining in the retention phase. One method by which this can be done is to require that α consecutive frames elapse without a recognition, before the system returns to the acquisition phase. The probability that α successive frame sync patterns will be examined without a recognition is

$$X = [1 - P_n(\epsilon)]^{\alpha} \tag{30}$$

Therefore, under this condition for remaining in the retention phase, the approximate average number of frames between false alarms is

$$\alpha_5 = \frac{1}{[1 - P_n(\epsilon)]^{\alpha}} \tag{31}$$

Each time the system enters the retention phase on a false-sync pulse, α frames are required before the system determines this fact and returns to the acquisition phase. The verification criterion should be sufficiently restrictive to ensure that the probability is small of entering the retention phase on a false-sync pulse. A verification criterion that is usually sufficiently restrictive is to require reception of two recognizer pulses that are separated by an integral multiple of the frame interval. The verification phase extends from the end of acquisition to the time that the system enters the retention phase. Assuming the above criterion for verification, the average number of frames required for this phase of operation is

$$\alpha_2 = \alpha_0 + \beta(\alpha_0 - 1)(\alpha_1 + 1)F_n(\epsilon) \tag{32}$$

For each false alarm, the system switches back to the verification phase, and sometimes sync is lost before the retention phase is reacquired. The average number of frames required to get back into the retention phase after each false alarm is

$$\alpha_3 = \alpha_0[1 + \beta(\alpha_1 + 1)F_n(\epsilon)] \tag{33}$$

For those times when sync is lost after a false alarm, the average number of frames out of sync before sync is reacquired is

$$\alpha_4 = 1 + (\alpha_0 - \tfrac{1}{2})[1 + \beta F_n(\epsilon)] \tag{34}$$

Therefore, the ratio of frames out of sync to total elapsed frames for the improved single mode of operation is

$$\lambda_{sc} = \frac{1 + (\alpha_0 - \tfrac{1}{2})[1 + \beta F_n(\epsilon)]}{\left[\frac{1}{1 - P_n(\epsilon)}\right]^{\alpha} + \alpha_0[1 + \beta(\alpha_1 + 1)F_n(\epsilon)]} \tag{35}$$

which reduces to approximately

$$\lambda_{sc} = \alpha_0[1 - P_n(\epsilon)]^{\alpha} \tag{36}$$

when $P_n(\epsilon) >> \beta F_n(\epsilon)$.

b. Dual Mode System

(1) Digital filter. The single-mode system is improved by imposing the condition that α consecutive frames elapse without a recognition before leaving the retention phase. This reduces the percentage of frames out of sync due to false alarms; however, it suffers from the disadvantage that, once sync is lost, α frames are required before this loss of sync can be determined.

The same improvement gained by the frame counting technique can be achieved by increasing the probability of recognition during the retention phase. One method for achieving this is by use of the digital filter (Ref. 11). This device employs two counters. Once the retention phase is gained, a bit-by-bit examination of the sync pattern is made for errors. One counter stores the bits in error and the other the correct bits. If the counter storing the correct bits overflows first, both counters are reset and the accumulation is started over. If, however, the counter storing the false bits overflows first, a failure-to-recognize is indicated. Using this method, the probability of recognition can be increased to nearly any desired value by adjusting the counter capacities.

The digital filter is restricted to the use of a one-bit aperture in the retention phase because a distinction between correct and incorrect bits is impossible if a phase slippage occurs in the local oscillator. If errors are bunched within the frame sync pattern, the digital filter can make a decision of nonrecognition after examining a small part of the sync pattern. A technique that examines the entire sync pattern before making a decision would appear to make better use of the available information.

(2) Increasing allowed errors. A second method of increasing the retention probability is to increase the number of errors allowed by the recognizer upon entering the retention phase. Examination of Figures 9, 10, and 11 shows that for a given length of sync pattern, n, the recognition probability, $P_n(\epsilon)$, increases rapidly with increases in the allowed

errors, ϵ. The false-sync probability, $F_n(\epsilon)$, also increases with ϵ; however, this is of no great concern in the retention phase, since the output of the recognizer is examined only during a narrow aperture once each frame.

The number of errors allowed by the recognizer during the acquisition and verification phases will be designated by ϵ_1, and during the retention phase by ϵ_2. If a false alarm is indicated by failure to recognize the sync pattern in the retention phase, then the probability of returning to the verification phase is $1 - P_n(\epsilon_2)$. If the verification criterion is the same as indicated in the section on the single-mode system, then the probability that at least one false-sync pulse will be encountered before the retention phase is re-established is $1 - [1 - F_n(\epsilon_1)]^{\alpha 0 \beta}$. Therefore, the probability that frame sync will be lost in any frame, π, is given by the product of these two independent probabilities.

$$\pi = [1 - P_n(\epsilon_2)]\left\{1 - [1 - F_n(\epsilon_1)]^{\alpha 0 \beta}\right\} \tag{37}$$

when $H_\beta(\epsilon_1) >> H_\delta(\epsilon_1)$. The probability that sync will be maintained in any one frame is given by one minus this probability.[2]

The block diagram of one mechanization of the dual-mode frame sync system appears in Figure 15. The dual-mode system differs from the single-mode system in that the probability of recognition of the frame sync pattern is increased in the retention mode for the dual-mode system. The timing sequence diagram for this system is shown in Figure 16. The individual waveforms are identified by capital letters that also appear on the block diagram in Figure 15. In Figure 16, Part a shows a typical sequence of events leading from the beginning of acquisition through verification to retention. In Figure 16, Parts b and c are expansions of waveforms at the beginning of the retention phase for the single-bit and three-bit aperture conditions, respectively.

Understanding of the frame sync logic mechanized in Figure 15 will be enhanced by a detailed description of the sequence of events depicted in Figure 16, Part a. It is assumed that bit sync is acquired in the middle of the first frame appearing in Figure 16, Part a. All gates are enabled by the positive state of any waveform. Waveforms B and F are both in the positive state at this time. This will usually be the case, since waveform C sets flipflops 1 and 2 to the enabling state and C is

[2] The probability that frame sync will be lost in any given frame where $H_\delta(\epsilon_1)$ is significant is given by

$$\pi' = [1 - P_n(\epsilon_2)]\left\{1 - [1 - H_\delta(\epsilon_1)]^{\alpha 0}[1 - F_n(\epsilon_1)]^{\alpha 0 \beta}\right\} \tag{37a}$$

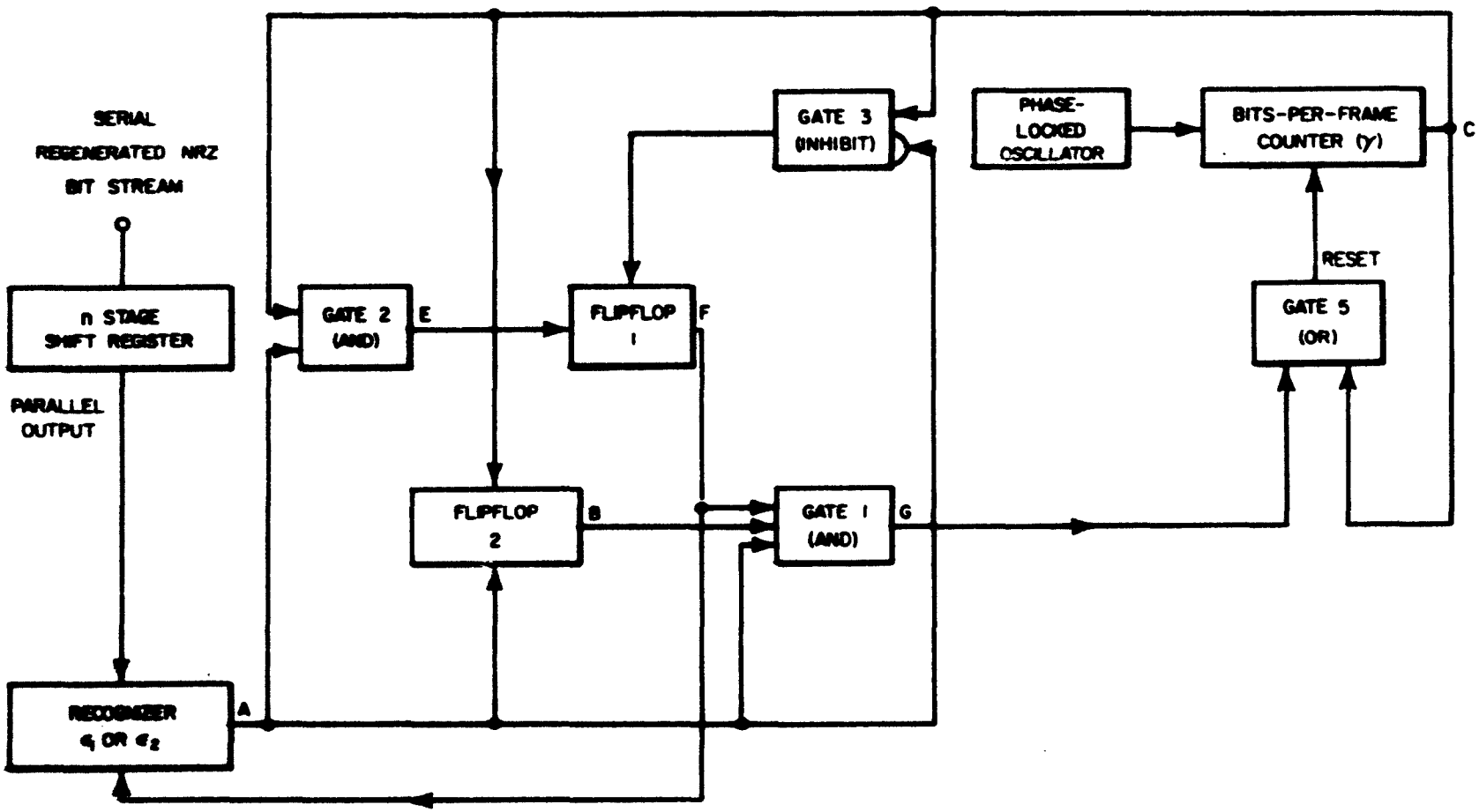
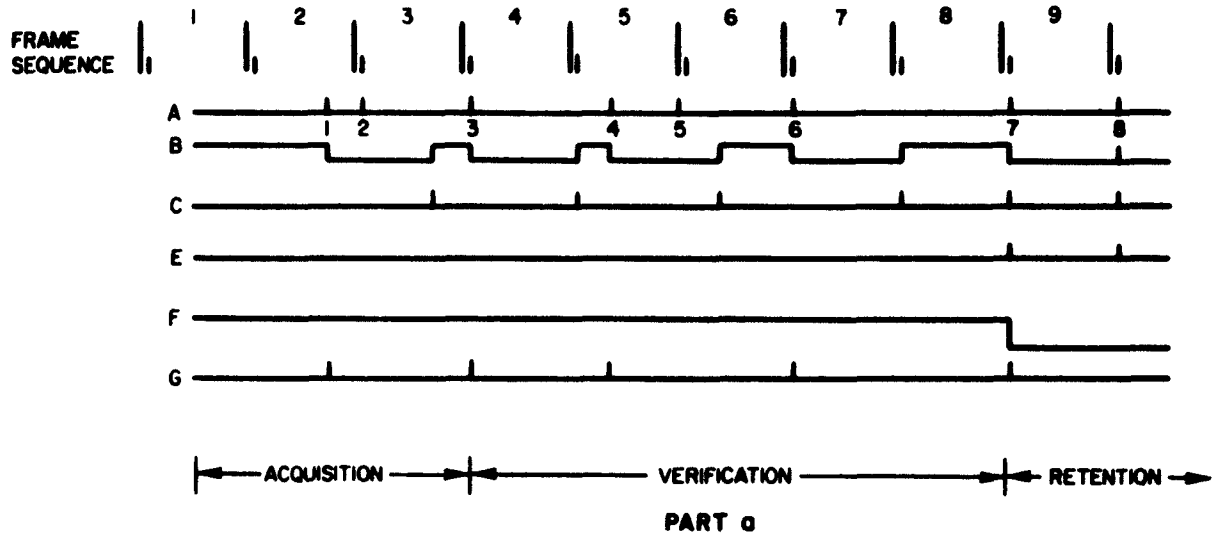
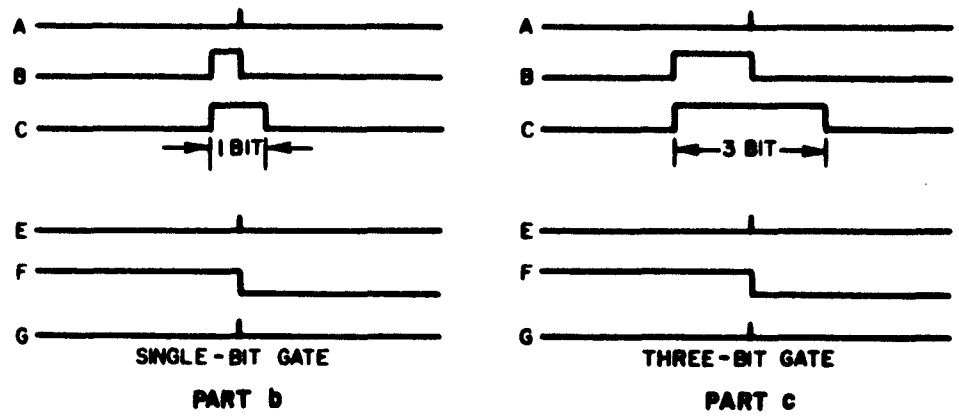


FIGURE 15. Dual-Mode Frame-Synchronization System





NOTES:

1. GATES ARE ENABLED BY POSITIVE LEVEL OF WAVEFORMS
2. PARTS b AND c ARE WAVEFORM EXPANSIONS OF PART a AT BEGINNING OF RETENTION
3. POSITIVE IS UP

FIGURE 16. Dual-Mode Timing Sequence

generated once per frame by the bits-per-frame counter, even before bit sync is obtained. With waveforms B and F in the enabling state, the first recognizer pulse will pass through AND Gate 1 and OR Gate 5, and then the pulse will reset the bits-per-frame counter. This event occurs during the latter part of frame 2 in the timing sequence diagram of Figure 16, Part a. The recognizer pulse, waveform A, also resets flipflop 2, returning waveform B to the disabling state, where it remains for one full frame. Flipflop 2 can be reset only by waveform C, which occurs each time the bits-per-frame counter fills up. If the bits-per-frame counter resets before it reaches full capacity, the spacing between pulses on waveform C may be greater than one frame. A correct recognition occurs at the beginning of frame 3 but is lost, since waveform B is in the disabling state at this time. Waveform C resets the bits-per-frame counter during the latter part of frame 3, thus returning waveform B to the enabling state. A correct recognition pulse occurs at the beginning of frame 4, thus resetting the bits-per-frame counter to the correct phase. The system is in frame sync at this time; and, by definition, this ends the acquisition phase and marks the beginning of the verification phase. The verification criterion requires that a recognition pulse must coincide with a pulse on waveform C. This condition could be satisfied at the sync position at the beginning of frame 5; however, a recognition is not received, waveform B returns to the enabling state, and the system remains in verification. The bits-per-frame counter is reset internally and the system remains in frame sync. A false recognition pulse occurs during the first part of frame 5, thus resetting the bits-per-frame counter out of phase and causing loss of frame sync. A correct sync pulse occurs at the beginning of frame 6, but is excluded by waveform B. Waveform B returns to the enabling state at the first part of frame 6. No false-sync pulses occur during the remainder of frame 6, and a correct sync pulse occurs at the beginning of frame 7, thus re-establishing frame sync. The sync pattern at the beginning of frame 8 is not recognized; however, no false-sync pulses occur in frames 7 and 8, so the system remains in frame sync. At the beginning of frame 9, a correct recognition is received, which coincides with waveform C, thus satisfying the verification criterion. Coincidence between waveforms A and C causes an output pulse to be generated by AND Gate 2, thus resetting flipflop 1. Waveform F returns to the disabling state, blocking AND Gate 1 and at the same time switching the number of errors allowed by the recognizer from ϵ_1 to ϵ_2. The system thus enters the retention phase at this time and will remain there as long as flipflop 1 remains in the proper state to disable AND Gate 1. The system will remain in the retention phase as long as the recognition pulse is received in each frame during the narrow aperture of waveform C.

The recognition pulse, waveform A, and waveform C act as inputs that inhibit Gate 3. Waveform C passes through Gate 3 to reset flipflop 1 when the recognition pulse is not coincident with it. For a 31-bit sync

pattern, typical values of ϵ_1 and ϵ_2 might be 4 and 10, respectively. From Figure 10, it is seen that for a bit error probability of 0.1 the recognition probabilities are 0.80 and 0.99990, respectively, which fact greatly increases the retention probability without resorting to the frame counting techniques. The principal limitations on the magnitude of ϵ_2 are the values of $F_n(\epsilon_2)$ and $H_b(\epsilon_2)$, which increase rapidly with increasing ϵ_2. This must be considered, since a phase slippage of the bits-per-frame counter while in the retention phase causes the narrow aperture C to coincide with the overlap region or the random bit region. The probability that a recognition pulse will be received in any one of these positions can be calculated for $F_n(\epsilon_2)$ or $H_b(\epsilon_2)$. The probability that the system will remain out of sync for α frames before the switching back to acquisition is

$$M = [(F_n(\epsilon_2)]^{\alpha} \tag{38}$$

for the random region, or

$$N = [H_b(\epsilon_2)]^{\alpha} \tag{39}$$

for the overlap region. For the verification criterion implemented in Figure 15, the probability that the retention phase will be acquired falsely cannot exceed

$$K = 1 - [1 - F_n(\epsilon_1)]^{(\alpha_1+\alpha_2)} \tag{40}$$

A useful measure of retention capability is the ratio of frames out of sync (because of false alarms) to the total elapsed frames

$$\lambda_D = \frac{\alpha_4}{1/\pi + \alpha_4} = \frac{1 + (\alpha_0 - \frac{1}{2})[1 + \beta F_n(\epsilon_1)]}{1/\pi + 1 + (\alpha_0 - \frac{1}{2})[1 - \beta F_n(\epsilon_1)]} \tag{41}$$

which reduces to

$$\lambda_D \cong \pi(\alpha_0 + \tfrac{1}{2}) \tag{41a}$$

when $P_n(\epsilon_1) >> \beta F_n(\epsilon_1)$ and $1 - P_n(\epsilon_2) << 1 - P_n(\epsilon_1)$.

D. OPTIMIZATION OF SYSTEM PERFORMANCE

1. CRITERIA FOR SYNCHRONIZATION PATTERN SELECTION

a. One-Bit Aperture

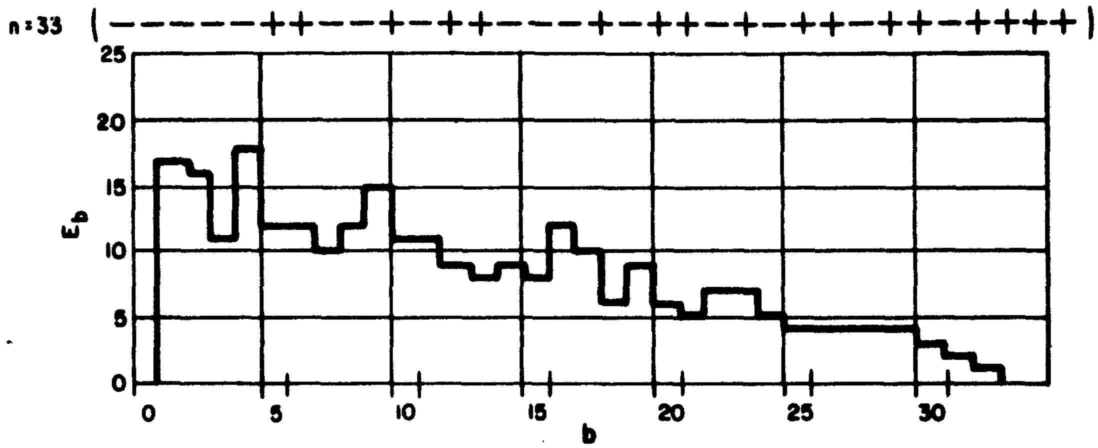
The recognition probability, $P_n(\epsilon)$, and the false-sync probability, $F_n(\epsilon)$, are functions of the number of bits, n, in the sync pattern and the number of errors, ϵ, allowed by the recognizer; however, these probabilities are independent of the particular pattern that is selected. Pattern selection is possible only when criteria are available for determining the desired correlation properties of the sync pattern. The correlation properties can also be stated in terms of the probabilities of a recognition in the various displacement positions as given by Equation (20).

In general, criteria for acquisition and/or verification may dictate the selection of the frame sync pattern. In the acquisition and verification phases, the only condition determining the selection of the sync pattern is the magnitude of $H_\delta(\epsilon_1)$, the total probability of a false-sync indication in the displacement region, as shown in Equation (21). Theoretically, $H_\delta(\epsilon_1)$ could be minimized in the absence of other criteria; however, a point of diminishing returns is reached when $H_\delta(\epsilon_1)$ becomes small compared to $H_\beta(\epsilon_1)$. Therefore, the criterion for sync pattern selection in the acquisition and verification phases can be stated as

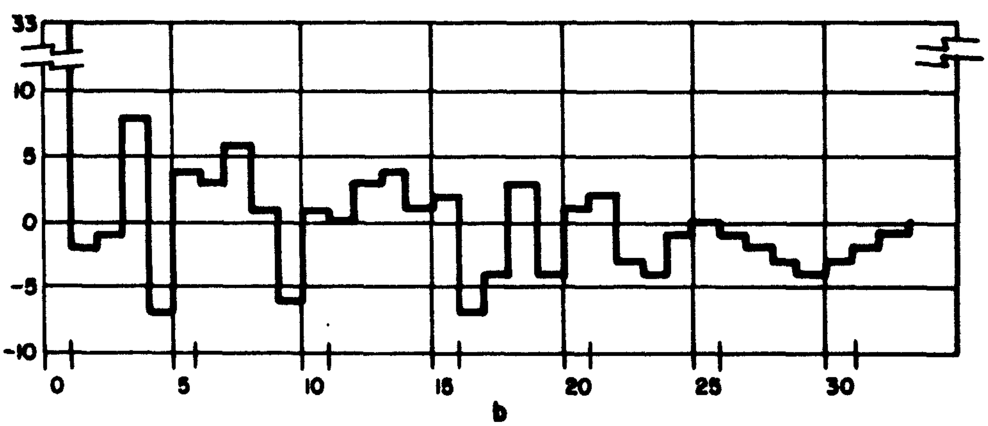
$$H_\delta(\epsilon_1) << H_\beta(\epsilon_1) \tag{42}$$

In the retention phase, when the sampling aperture (waveform C in Figure 16, Part b) is one bit-period wide, all criteria for code selection are satisfied by minimizing $H_\delta(\epsilon_1)$. The one-bit aperture allows examination of the recognizer output only at the time that recognition is expected; and the probability of recognition, $P_n(\epsilon_2)$, is independent of the choice of sync patterns. This assumes that frame sync is maintained and that bit slippages do not occur. Even if bit slippages do occur, the only requirement that could affect the choice of the sync pattern is the need to keep the probability of a displaced false-sync pulse low, compared to unity. Sync patterns that do not satisfy this requirement do not have low values of $H_\delta(\epsilon_1)$. Therefore, the only criterion determining the selection of sync patterns for the single-bit sampling aperture is the minimization of $H_\delta(\epsilon_1)$.

Figures 12, 17, and 18 are plots of sync patterns with low values of $H_\delta(\epsilon_1)$. The upper plot in each case shows the disagreement bits in

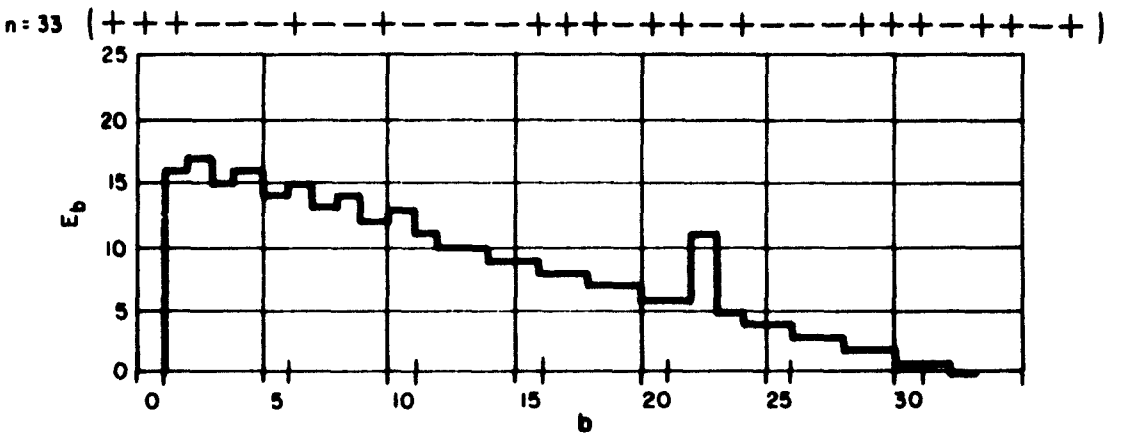


NUMBER OF ERRORS (E_b) IN PATTERN REQUIRED TO DISPLACE n-BIT PATTERN (b) BITS

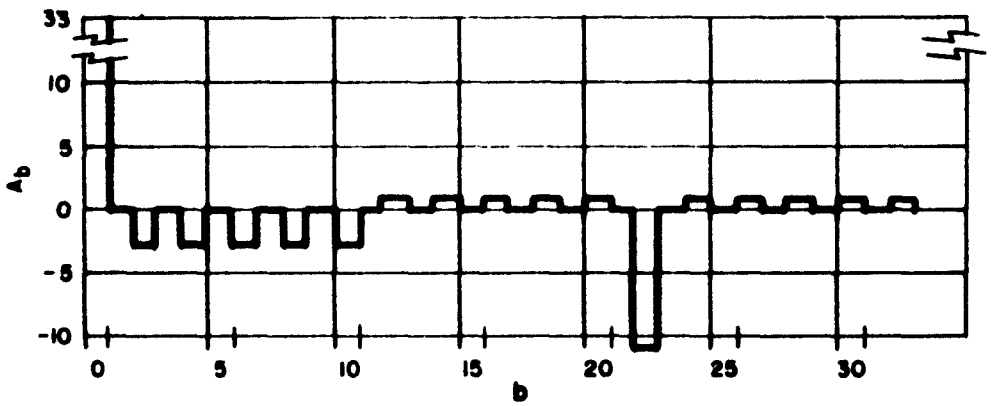


AUTOCORRELATION FUNCTION $A_b = n - b - 2E_b$

FIGURE 17. Code 4 (One-Bit Aperture)



NUMBER OF ERRORS (E_b) IN PATTERN REQUIRED TO DISPLACE n-BIT PATTERN (b) BITS



AUTOCORRELATION FUNCTION $A_b = n - b - 2E_b$

FIGURE 18. Code 5 (One-Bit Aperture)

the overlap region versus the displacement position. The lower plot shows the autocorrelation function, A_b, which is defined as the agreement bits minus the disagreement bits for each overlap position.

b. Three-Bit Aperture

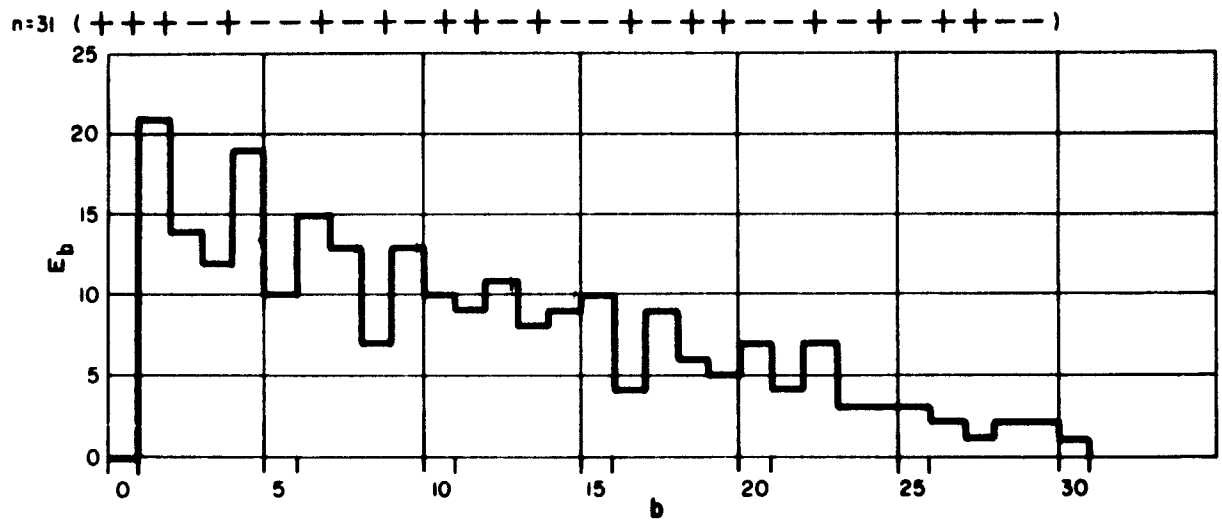
As the threshold of bit sync is approached, slippages begin to occur between the VCO of the phase-lock loop and the signal. Slippages of plus or minus one bit per frame are much more frequent than slippages of larger amounts. When the sampling aperture (waveform C of Figure 16, Part a) is one bit wide, recognition will be missed for a slippage of one or more bits. However, if the sampling aperture is three bits wide, centered at the normal recognition position, recognition is still possible for slippages of plus or minus one bit per frame. Accordingly, with the three-bit aperture and slippages of plus or minus one bit per frame, the condition for remaining in the retention phase is satisfied and the bits-per-frame counter can be reset to the proper phase without recourse to acquisition.

The three-bit aperture, however, also permits false-sync pulses, displaced by plus or minus one bit, to enter the system and falsely reset the bits-per-frame counter. To offset this, a sync pattern (to be suitable for use with the three-bit aperture) should satisfy the condition that the probability of a false-sync pulse displaced by one bit should be small compared to the probability of a false alarm:

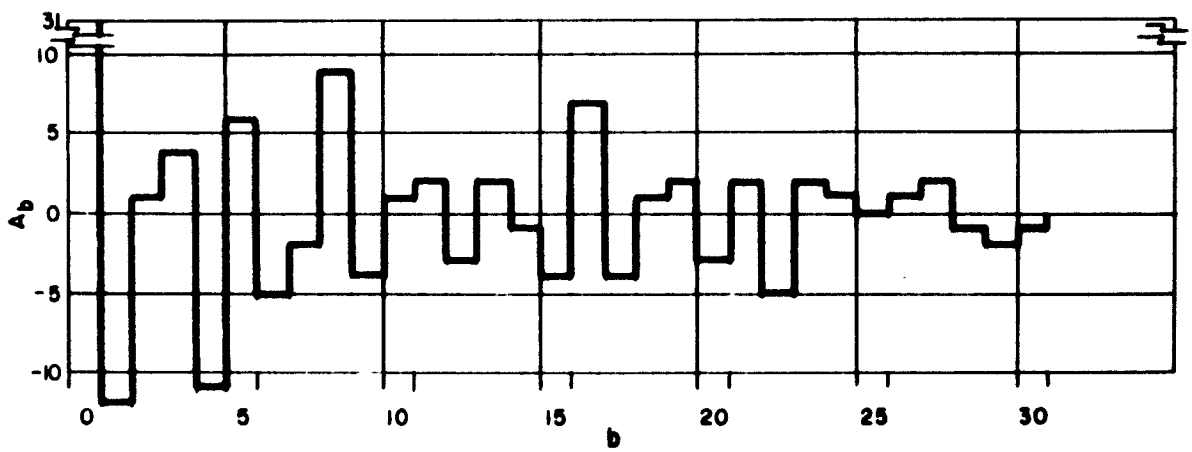
$$H_1(\epsilon_2) << 1 - P_n(\epsilon_2) \qquad (43)$$

$H_1(\epsilon_2)$ is calculated from Equation (20) for the case of b = 1.

An examination of the one-bit aperture codes, which tend to minimize $H_\delta(\epsilon_1)$, reveals that they do not satisfy the condition expressed in Equation (43). There are, however, codes that do satisfy this requirement and at the same time satisfy the acquisition criterion stated in Equation (42). Two codes selected on the three-bit aperture criteria are plotted in Figures 13, 19, and 20. The differences between the plots of the three-bit and one-bit aperture codes should be noted. Most notable is the very large negative correlation peak at the first displacement position exhibited by the three-bit aperture codes. In general, the autocorrelation functions of the three-bit codes exhibit a greater dispersion from the zero line than do the similar functions of the one-bit codes. This characteristic of the three-bit aperture codes results in increased values of $H_\delta(\epsilon_1)$. Table 3 shows the relative values of the important parameters in the selection of sync patterns. For some of the three-bit aperture codes, $H_\delta(\epsilon_1)$ exceeds by more than an order of magnitude the $H_\delta(\epsilon_1)$ for some of the one-bit aperture codes, yet the condition imposed by Equation (42) is still satisfied for all of the codes in the table.

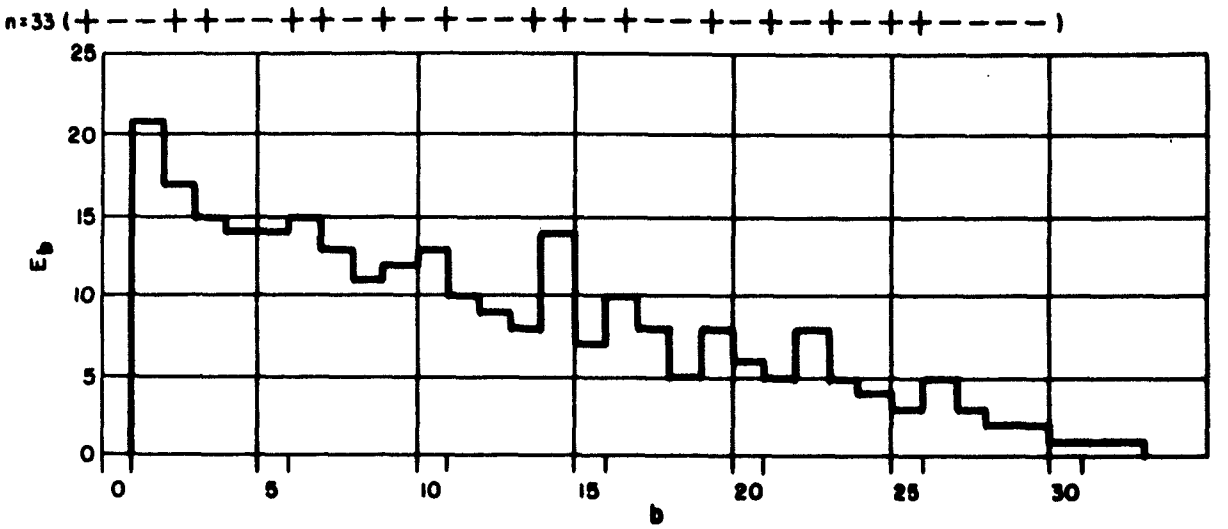


NUMBER OF ERRORS (E_b) IN PATTERN REQUIRED TO DISPLACE
n-BIT PATTERN (b) BITS

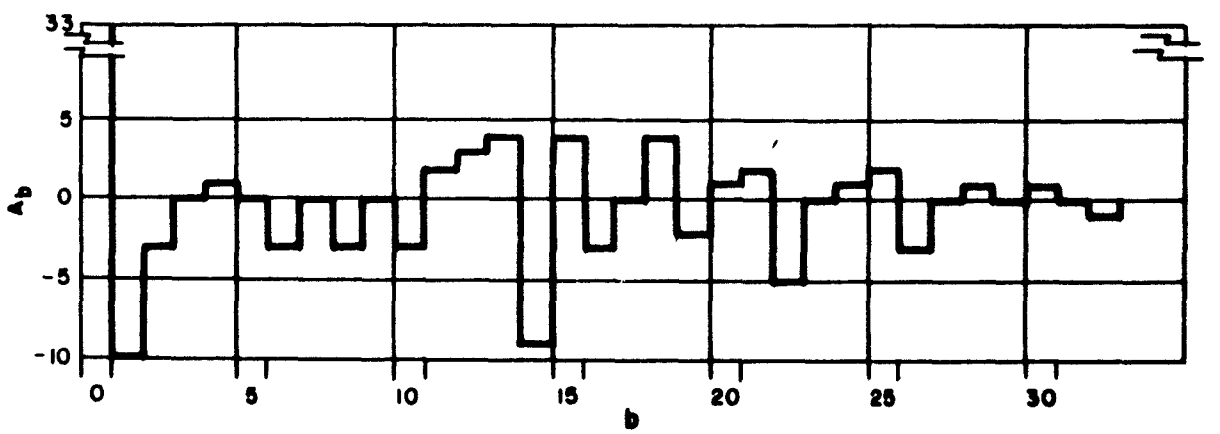


AUTOCORRELATION FUNCTION $A_b = n - b - 2E_b$

FIGURE 19. Code 3 (Three-Bit Aperture)



NUMBER OF ERRORS (E_b) IN PATTERN REQUIRED TO DISPLACE
n-BIT PATTERN (b) BITS



AUTOCORRELATION FUNCTION $A_b = n - b - 2E_b$

FIGURE 20. Code 6 (Three-Bit Aperture)

TABLE 3. Calculations Comparing Codes Selected on the Basis of Different Criteria

$\beta = 1000$; $p = 0.1$.

Binary Code[a]	n	Aperture	ϵ_1	ϵ_3	$H_\beta(\epsilon_1)$ x 10^{-3}	$H_\delta(\epsilon_1)$ x 10^{-6}	H_γ x 10^{-3}	$H_1(\epsilon_2)$ x 10^{-6}	$1 - P_n(\epsilon_2)$ x 10^{-6}
1	31	1	4	10	17.0	162	17.15	2029	126.2
2	31	3	4	10	17.0	665	17.64	0.0118	126.2
3	31	3	4	10	17.0	432	17.43	0.3125	126.2
4	33	1	4	10	5.46	18.6	5.48	113	238.3
5	33	1	4	10	5.46	60.5	5.51	455	238.3
6	33	3	4	10	5.46	63.0	5.52	0.258	238.3

[a] 1 = 111110001101110101000010010110 0

2 = 101010010101101001011001010100 0

3 = 111010010101101001011001010110 0

4 = 111110011010011101001010010010000

5 = 111000100100001110110100011101101

6 = 100110011010100110100101010110000

The three-bit aperture code gains its advantage over the one-bit aperture code under conditions of bit slippage of the phase-lock oscillator. When the slippage is no more than plus or minus one bit per frame, the bits-per-frame counter can be reset at the end of that frame, thus reducing the total frames out of sync. Table 4 shows comparative data taken with the one- and three-bit apertures with a near-optimum code selected for each. The data in the first row were taken under conditions where a slippage was occurring on the average of once per second. Slippages were induced by frequency-modulating the clock (bit rate) with Gaussian noise. With the one-bit aperture, the system was out of sync 22 percent of the time. When the three-bit aperture was employed under the same conditions, this was reduced to 8 percent. When the slippage rate was increased to about 3.5 per second, the system was out of sync 32 percent of the time with the one-bit aperture and 17 percent with the three-bit aperture.

TABLE 4. Relative Performance of System With One- and Three-Bit Aperture Codes

Signal-to-noise ratio was measured at input to phase-lock loop and bit detector. Slippages were induced by Gaussian noise frequency-modulating the clock. $n = 22$ bits; $\epsilon_1 = 3$; $\epsilon_2 = 7$; $\gamma = 880$ bits per frame; $f_b = 100$ k-bits per second; $f_f = 113$ frames per second; RMS S/N = 1.0.

Average Slippages per Second	Fraction of Data Lost (λ_D)	
	One-Bit Aperture Code	Three-Bit Aperture Code
1.0	0.22	0.083
3.5	0.32	0.17

c. Techniques for Pattern Finding

For a given length of sync pattern, n, there are 2^n possible patterns from which to choose. When sync patterns of thirty bits or more are used, the number of possible codes is several billion. When criteria are established for determining desirable code characteristics, the next questions to be answered are:

1. For a given number of bits assigned to the sync pattern, is there one optimum pattern for these criteria or are there perhaps many that are equally good or nearly so?

2. For a given length of sync pattern, how can the optimum sync pattern or optimum sync patterns be found?

For given criteria, such as for the one-bit aperture, a straightforward approach might be as follows: First, calculate $H_\delta(\epsilon_1)$ from Equation (21) for all possible 2^n patterns. Second, select the pattern with the minimum value of $H_\delta(\epsilon_1)$, and this would be the best possible sync pattern for a one-bit aperture. For the longer sync patterns, this procedure is prohibitive in both cost and time, even for a large-scale high-speed computer. Approximation methods have proven more fruitful for the selection of sync patterns.

Examination of the E_b versus b plots reveals a great deal about the characteristics of a code, once experience is gained in code selection. For example, codes that have small values of $H_\delta(\epsilon_1)$, such as in Figures 12, 17, and 18, have the general characteristic that E_b increases roughly monotonically as b decreases. However, this property is more important for large values of b (as exhibited by the code in Figure 17, which is the best one-bit aperture code of the three). The realization that the E_b versus b plot allowed a trained observer to predict a great deal about a code inspired the construction of a device that would display the E_b versus b plot on the face of an oscilloscope. Switches were made available to control each bit in the pattern individually. The change in the E_b versus b plot is immediately revealed to the operator when he makes any change in the code by reversing the position of one or more of the switches. With a reasonable amount of experimenting, a trained operator can select a near-optimum sync pattern for a given criterion. For example, in the selection of a one-bit aperture code, the largest contributors to $H_\delta(\epsilon)$ are the $H_b(\epsilon)$ values for small overlap positions, i.e., small values of b.

A computer program was written for the individual $H_b(\epsilon)$ terms, Equation (20), and their summation $H_\delta(\epsilon)$, Equation (21). This program permits rapid calculation of these complex expressions, once the E_b values are known. How near a given code is to optimum for a given criterion can only be determined by comparing these calculated parameters with those for codes of the same or nearly the same number of bits. As data are accumulated for a number of consecutive code lengths, a great deal concerning the degree of optimality can be determined by plotting a given parameter against the code length. It was found that, for near-optimum one-bit aperture codes, the value of $H_\delta(\epsilon)$ decreased monotonically as n increased. In fact, if $H_\delta(\epsilon)$ is plotted against n on semi-log paper, the points fall on a straight line for near-optimum one-bit aperture codes, as shown in Figure 21. During the search for near-optimum one-bit aperture codes, it was found that when the value for $H_\delta(\epsilon)$ was above this line, for a given code length, it was always possible by additional searching to find a code with a value of $H_\delta(\epsilon)$ closer to or

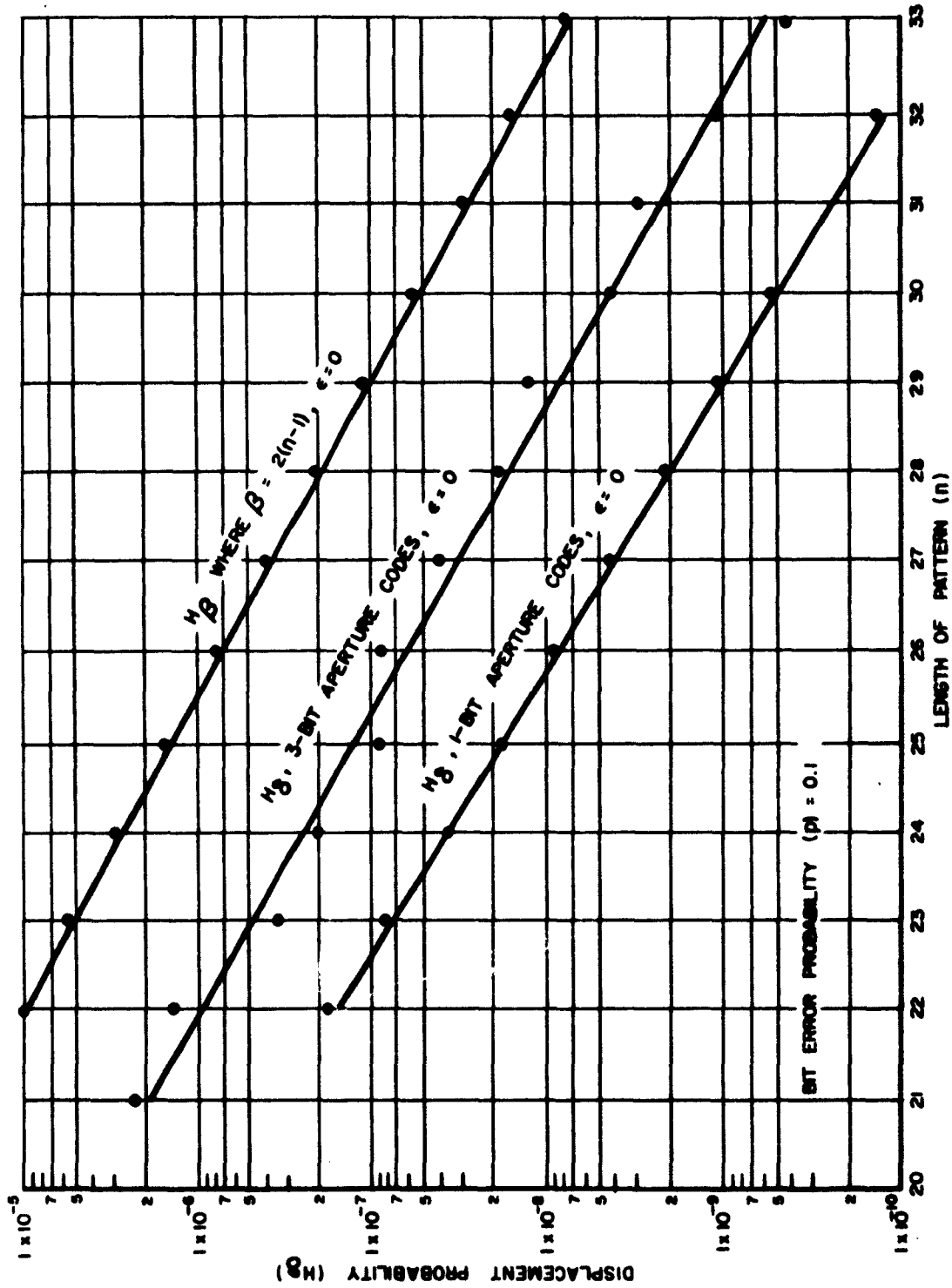


FIGURE 21. Displacement Probability, H_δ, Versus Length of Pattern, n, for $\epsilon = 0$

on this line. However, no code has yet been found with a value of $H_\delta(\epsilon)$ below this line. On this basis, it is assumed that codes with values of $H_\delta(\epsilon)$ on this line are near-optimum one-bit aperture codes. The codes that are plotted in Figure 21 are listed in Figure 23. It is not known whether any of the one-bit aperture codes listed in Figure 23 are truly optimum; however, it is felt that the difference between these near-optimum codes and the optimum codes would be only of academic interest. It should be stated that this technique assumes the number of allowed errors, ϵ, to be zero, and the codes appearing in Figure 23 were selected on this assumption. The values of $H_\delta(\epsilon_1)$ for $\epsilon_1 = 3$ are plotted in Figure 22. The points now do not all lie on a straight line. There is some evidence that codes which are optimum for one value of ϵ are not optimum for another; however, it appears that the improvement to be gained from selecting codes for each value of ϵ is slight.

Figure 23 also includes a list of three-bit aperture codes selected by the above technique. The selection was guided by the criteria stated in Equations (42) and (43). The values of $H_\delta(\epsilon_1)$ for $\epsilon = 0$ and $\epsilon = 3$ are plotted in Figures 21 and 22, respectively, as was done for the one-bit aperture codes. The points do not lie on a straight line as for the one-bit aperture codes, since the primary consideration is not the minimization of $H_\delta(\epsilon)$. These values, however, as shown in the upper curve, are all well below the probability of a false-sync indication, H_β, in an equal number of random bits. This comparison with an equal number of random bits is a good rule-of-thumb for the merit of a code; however, the criterion stated in Equation (42) is a sufficient requirement for normal applications.

2. PARAMETER SELECTION

a. Length of Synchronization Pattern

For a given frame format, the answer to questions regarding optimal system performance are very difficult to find. For example, the fraction of frames out of sync for the dual-mode system, λ_D, Equation (41), is a very complex function of n, ϵ_1, ϵ_2, β, and p. The problems of selecting parameters is aided somewhat by the fact that n, ϵ_1, and ϵ_2 can assume integral values only. Minimization of a quantity, such as λ_D, is not usually desirable because other quantities, such as the acquisition times, may assume impractical values. In general, parameter selection involves a compromise between two or more factors. Understanding of system performance under worst conditions is usually desired; therefore, the maximum expected value of p is assumed. Synchronization can be improved by assigning more bits to the frame sync pattern. Increase in n, however, must always be accompanied by an increase in ϵ, as was seen in Figure 10, if either $P_n(\epsilon)$ or $F_n(\epsilon)$ is to be maintained constant.

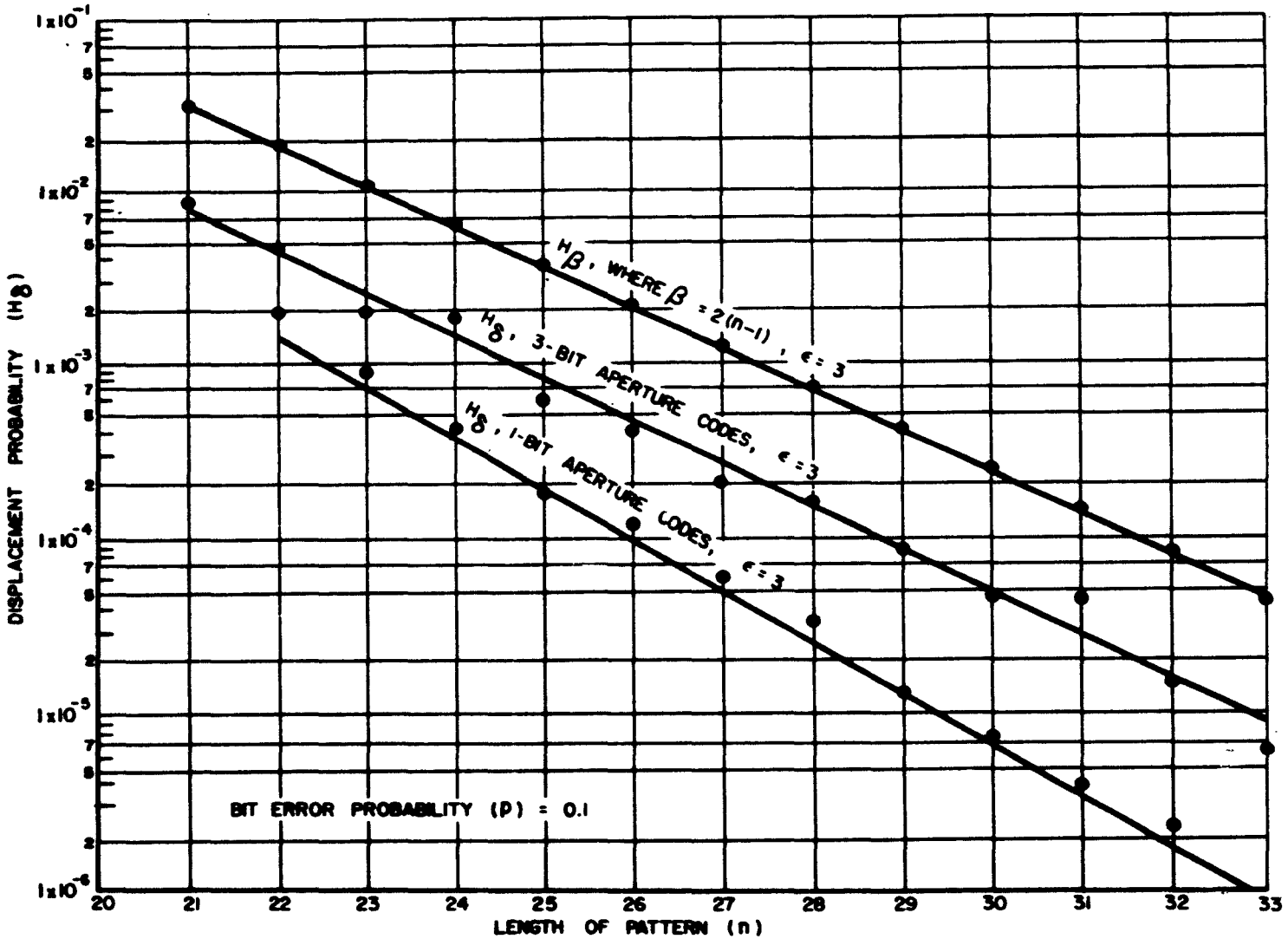


FIGURE 22. Displacement Probability, H_δ, Versus Length of Pattern, n, for $\epsilon = 3$

ONE-BIT APERTURE CODES		THREE-BIT APERTURE CODES	
n	BINARY CODE	n	BINARY CODE
		21	110101010010010011100
22	1111101100101000010000	22	101010010101100101 1001
23	1111011011000101000000 0	23	1010101011011011000 1100
24	1111011101010000110000 00	24	1010101011011011100 11100
25	1111110110010100011000000	25	1010101001011010011001100
26	1111110110010100011000000 0	26	1010101001011010011001 1001
27	1111111011001010011100000 00	27	1010101001011010011001 10011
28	1111100100111001010000000 00	28	1101010101100100101001001100
29	1111111101000111000010100 1000	29	1110010001100101010110100 0101
30	1111110111001110100010100 10000	30	1110010001100101010110100 11010
31	1111111001101111110101000 0100000	31	1110100101011010010110010101100
32	1111111001101011001010000 01000000	32	1010101010010011001100010010 1100
33	1111101110100111010010100 10010000	33	1001100110101001101001010110000

FIGURE 23. Near-Optimum Codes for One- and Three-Bit Aperture Criteria

It can be seen from Figure 11 that nearly any desired values of $P_n(\epsilon)$ are possible, if a sufficiently large value of n is chosen and an appropriate value of ϵ is selected.

Determination of parameter values providing a desired sync capability can be aided by a series of spot calculations. Table 5 shows the sync capabilities of both the single-mode and dual-mode systems for five different values of n, ranging from 22 to 33 bits. The bit error probability is 0.1, and the frame length is about 1000 bits. In the dual-mode system, the values of ϵ_1 and ϵ_2 are adjusted to maintain $F_n(\epsilon_2)$ equal to 0.1 or less and to keep the initial acquisition time between one and two frames. The improvement in λ_D with increase in n for the dual-mode system is very rapid, but it is not as rapid for the single-mode system. The dual-mode system is seen to be from one to four orders of magnitude better than the single-mode system as measured by λ_s/λ_D, depending on the length of the sync pattern and the value of ϵ chosen.

Practical considerations usually preclude the possibility of operation at very high bit error probabilities; however, there are special situations in which this region is interesting. Considering, for example, the ability of the carrier-lock system to maintain bit sync to very low values of S/N (and hence to large values of p), it is interesting to speculate on the frame sync capabilities under such conditions. The use of redundant coding schemes permits the transmission of useful data at these high bit error probabilities.

The question proposed is: For a given frame length and sync performance, how will the required length of frame sync pattern vary with the bit error probability? The curve in Figure 24 was normalized on the basis of four quantities: $F_n(\epsilon_1)$, $F_n(\epsilon_2)$, α_1, and $\beta + n$, which define the frame sync performance. The values assigned to these quantities appear in Figure 24. The number of bits in the frame sync pattern, n, was calculated for four values of p, 0.1, 0.2, 0.3, and 0.4. The problem was to calculate n, ϵ_1, and ϵ_2 for each value of p under the normalizing conditions. At the four values of p, the frame sync pattern occupies 3, 6, 15, and 60 percent, respectively, of the total frame. The extrapolated curve shows that if p = 0.43, the entire frame would be needed for the frame synchronization. The curve also shows that if p = 0, then $P_n(\epsilon) = 1$ and about 19 bits would be needed for the frame sync. False-sync probability is not a function of p but it does set the value of n when p = 0. Note also that the values of ϵ_1 and ϵ_2 become more nearly equal and also occupy a larger percentage of n as p increases.

Because of the complex nature of the quantities that characterize sync performance, it is difficult to visualize how performance varies with changes in a given parameter. A computer program has been written for the following quantities: $P_n(\epsilon)$, $F_n(\epsilon)$, π, λ_D, $H_b(\epsilon)$, and $H_\delta(\epsilon)$ as

TABLE 5. Comparison of Single-Mode and Dual-Mode Systems for Different Parameter Values

$\beta = 1000$; $p = 0.1$.

n	Single-Mode				Dual-Mode							$\frac{\lambda_S}{\lambda_D}$
	ϵ	α_1	$L_\beta \times 10^{-4}$	$\lambda_S \times 10^{-4}$	ϵ_1	ϵ_2	α_1	α_2	$F_n(\epsilon_2)$	$\pi \times 10^{-8}$	$\lambda_D \times 10^{-8}$	
22	2	1.2	356	719	3	7	1.2	1.7	0.067	35,000	71,200	990
25	2	1.4	83.7	19.5	3	8	1.4	1.9	0.054	4,450	8,350	23.4
28	2	1.7	17.8	47.5	3	10	1.7	2.2	0.092	84.5	161	2,950
31	3	1.1	14.0	29.4	4	11	1.1	1.6	0.075	48.7	82.7	356
33	3	1.1	5.14	11.5	4	12	1.1	1.7	0.081	6.25	10.5	10,900

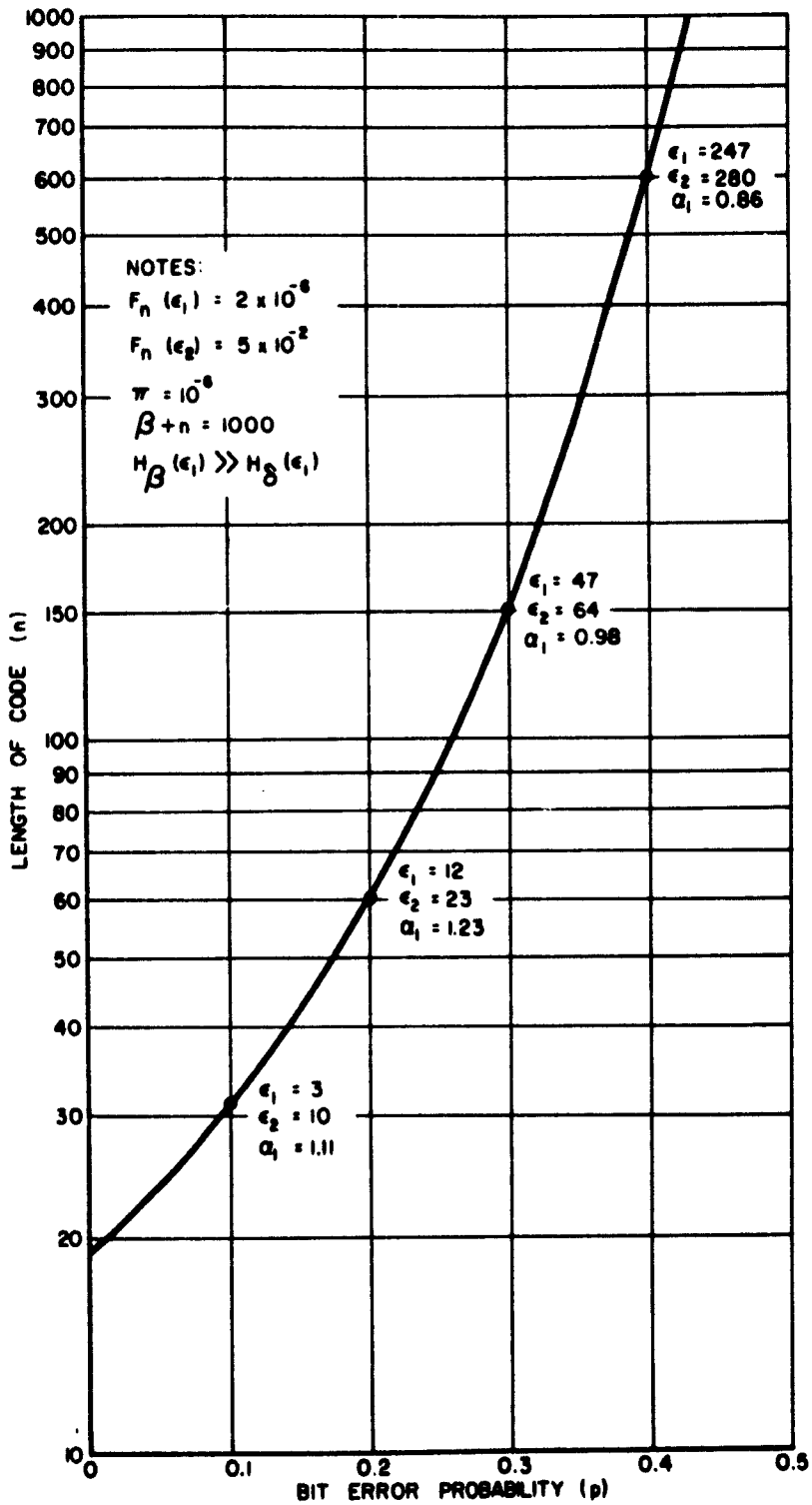


FIGURE 24. Length of Code, n, as a Function of Bit Error Probability, p, for Nearly-Constant Frame-Sync Capabilities

functions of n, ϵ_1, ϵ_2, p, β, and E_b. The computer program makes it possible to rapidly compute the values of these quantities for a large number of parameter values. From these values, a series of graphs can be plotted, which greatly aid one's insight into frame sync performance.

A number of graphs are included to assist the reader's understanding and to help him make appropriate choices of parameter values. In Figure 25, with p fixed at 0.05, λ_D (fraction of time out of sync for dual-mode system) is plotted against n for a number of ϵ_1 and ϵ_2 values. Figures 26 and 27 are the same as Figure 25, except that p = 0.1 and 0.2, respectively. It is interesting to note that, under certain conditions, λ_D is almost independent of n. While $F_n(\epsilon)$ decreases with n, $P_n(\epsilon)$ also decreases with n; and these opposing influences cancel each other in their effect upon λ_D under certain conditions.

It is clear from Figures 25, 26, and 27 that λ_D decreases for increasing values of ϵ_2 and decreasing values of ϵ_1. The limitation on the minimum value of ϵ_1 is determined by the magnitude of the acquisition times, which in general increase with decrease in ϵ_1, especially at large values of p. The average number of frames out of sync each time sync is lost due to a false alarm must be restrained to practical values. Figures 28 through 32 show α_4, plotted as a function of n for various values of ϵ_1 at various values of p. It is seen, as in Figure 28, that α_4 first decreases with increase in ϵ_1; and then, as ϵ_1 becomes larger, α_4 begins to increase. The value of ϵ_1 at which this turning point takes place depends on the value of p, as can be seen in this sequence of plots. Also, α_4 is sometimes an increasing function with respect to n and at other times a decreasing function, depending on the values of ϵ_1 and p. These effects are dependent upon the complex way in which $P_n(\epsilon)$ and $F_n(\epsilon)$ change with variations in parameter values.

Figures 33 and 34 show the manner in which λ_D and α_4 vary with p for fixed, reasonable values of n, ϵ_1, and ϵ_2.

b. Errors Allowed by Recognizer

Control of ϵ, the number of errors allowed by the recognizer, is a powerful means of controlling the frame sync performance. The frame sync capability is primarily dependent upon the recognition probability, $P_n(\epsilon)$, and the false sync probability, $F_n(\epsilon)$. These quantities are both sensitive functions of ϵ, as Figures 9, 10, and 11 clearly show. Functions such as π and λ_D, which involve different values of ϵ (ϵ_1 and ϵ_2), become very complex. However, selection of ϵ_1 and ϵ_2 are enhanced by a series of calculations, as shown in Table 6. These data were calculated for a sync pattern of 31 bits, a bit error probability of 0.1, and a frame length of about 1000 bits. The table shows values for the quantities $P_n(\epsilon_1)$, $F_n(\epsilon_2)$, α_1, α_2, H_β, π, and λ_D. In the first part of Table 6,

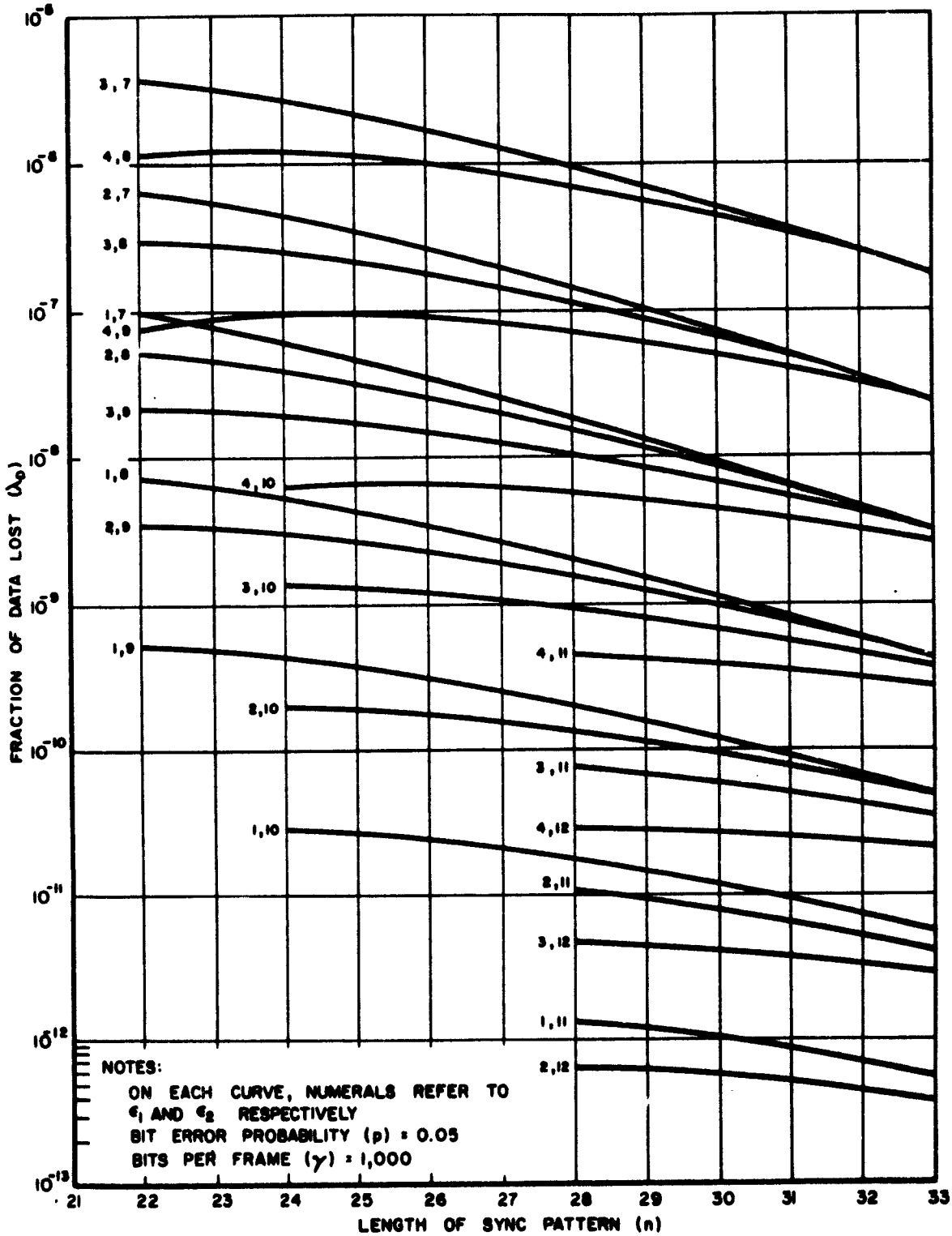


FIGURE 25. Fraction of Data Lost, λ_D, as a Function of Length of Sync Pattern, n, for Various Errors Allowed (ϵ_1 and ϵ_2) for p = 0.05

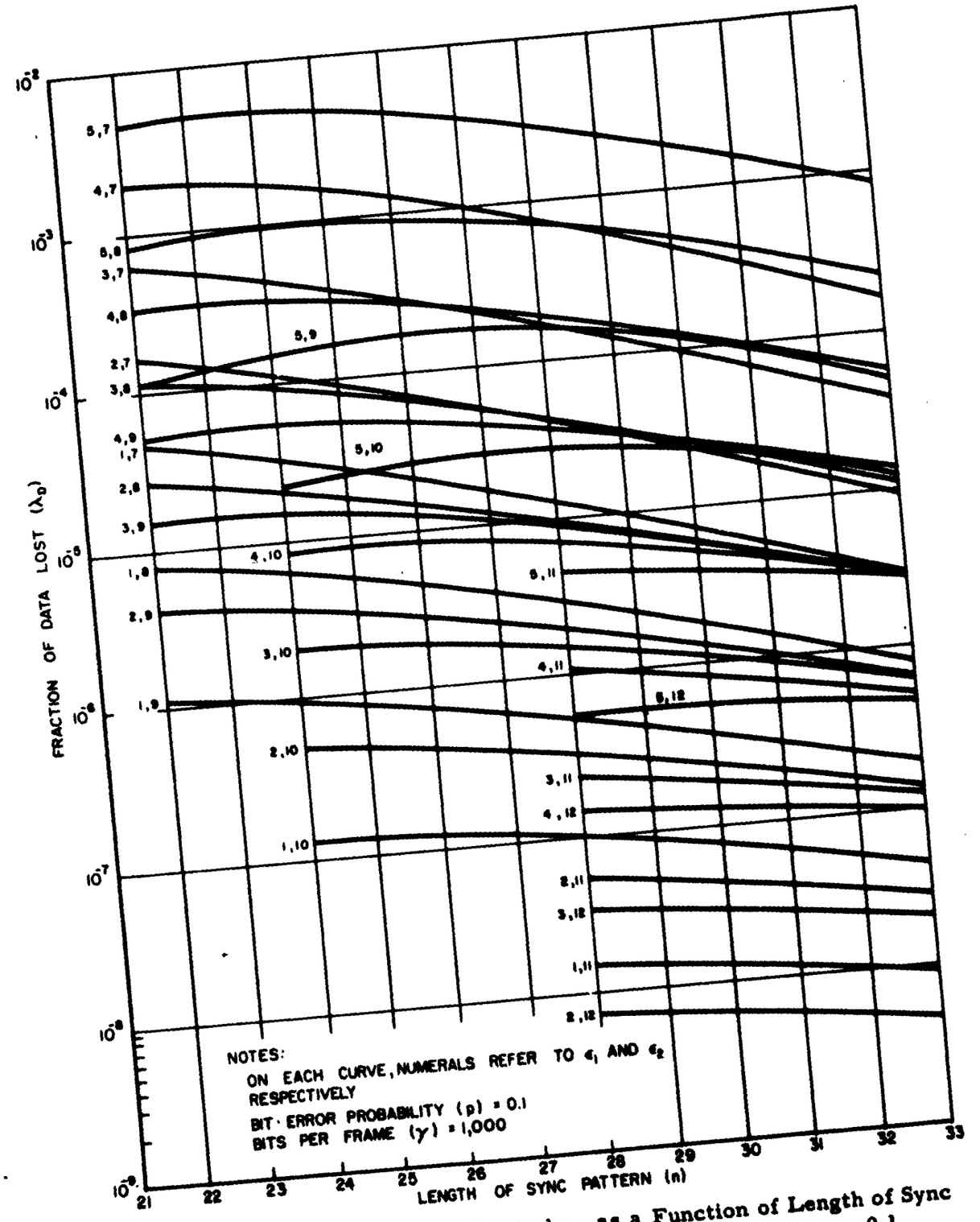


FIGURE 26. Fraction of Data Lost, λ_D, as a Function of Length of Sync Pattern, n, for Various Errors Allowed (e_1 and e_2) for p = 0.1

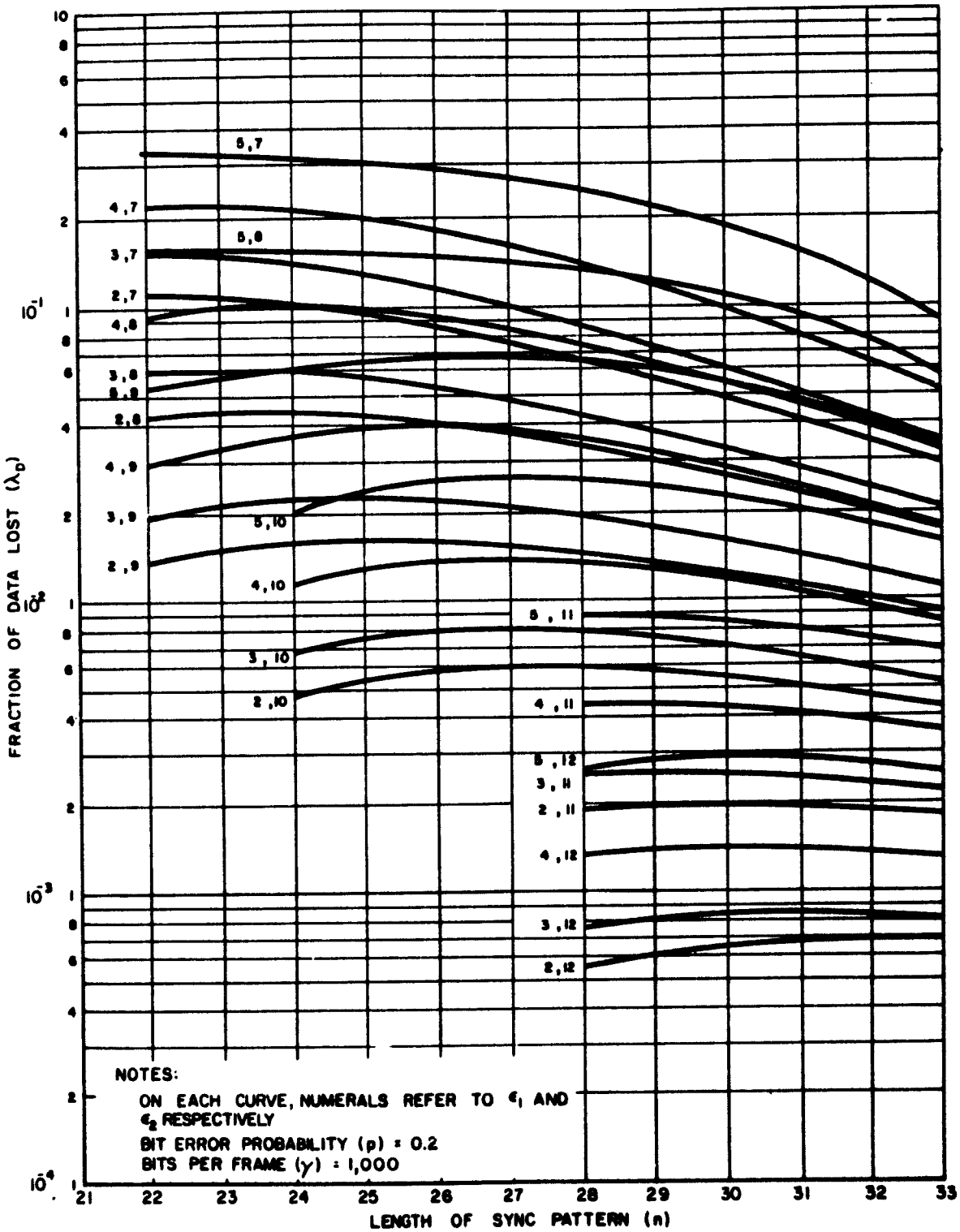


FIGURE 27. Fraction of Data Lost, λ_D, as a Function of Length of Sync Pattern, n, for Various Errors Allowed (ϵ_1 and ϵ_2) for p = 0.2

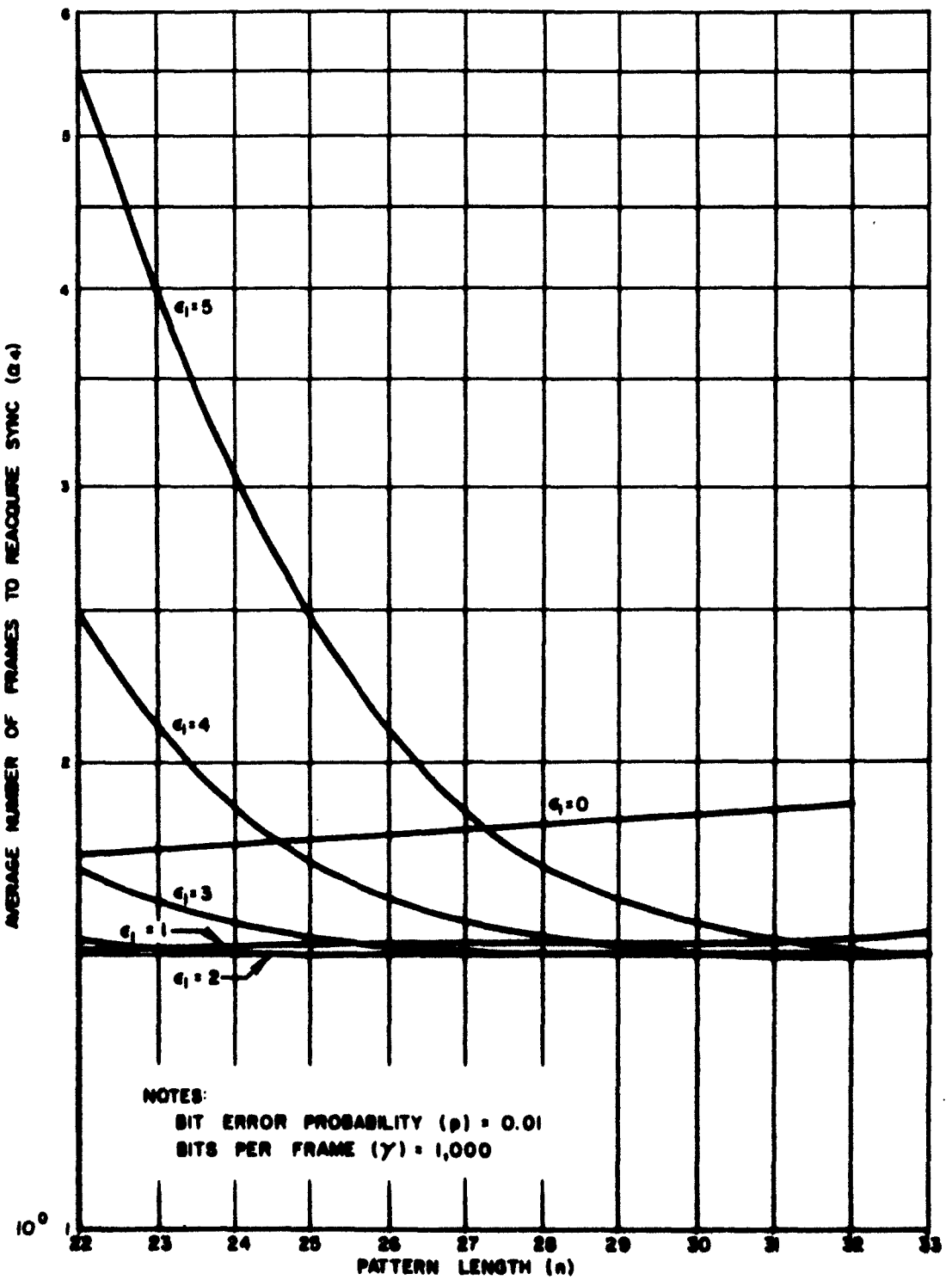


FIGURE 28. Average Number of Frames to Reacquire Sync, α_4, as a Function of Pattern Length, n, for Various Numbers of Errors Allowed (e_1), p = 0.01

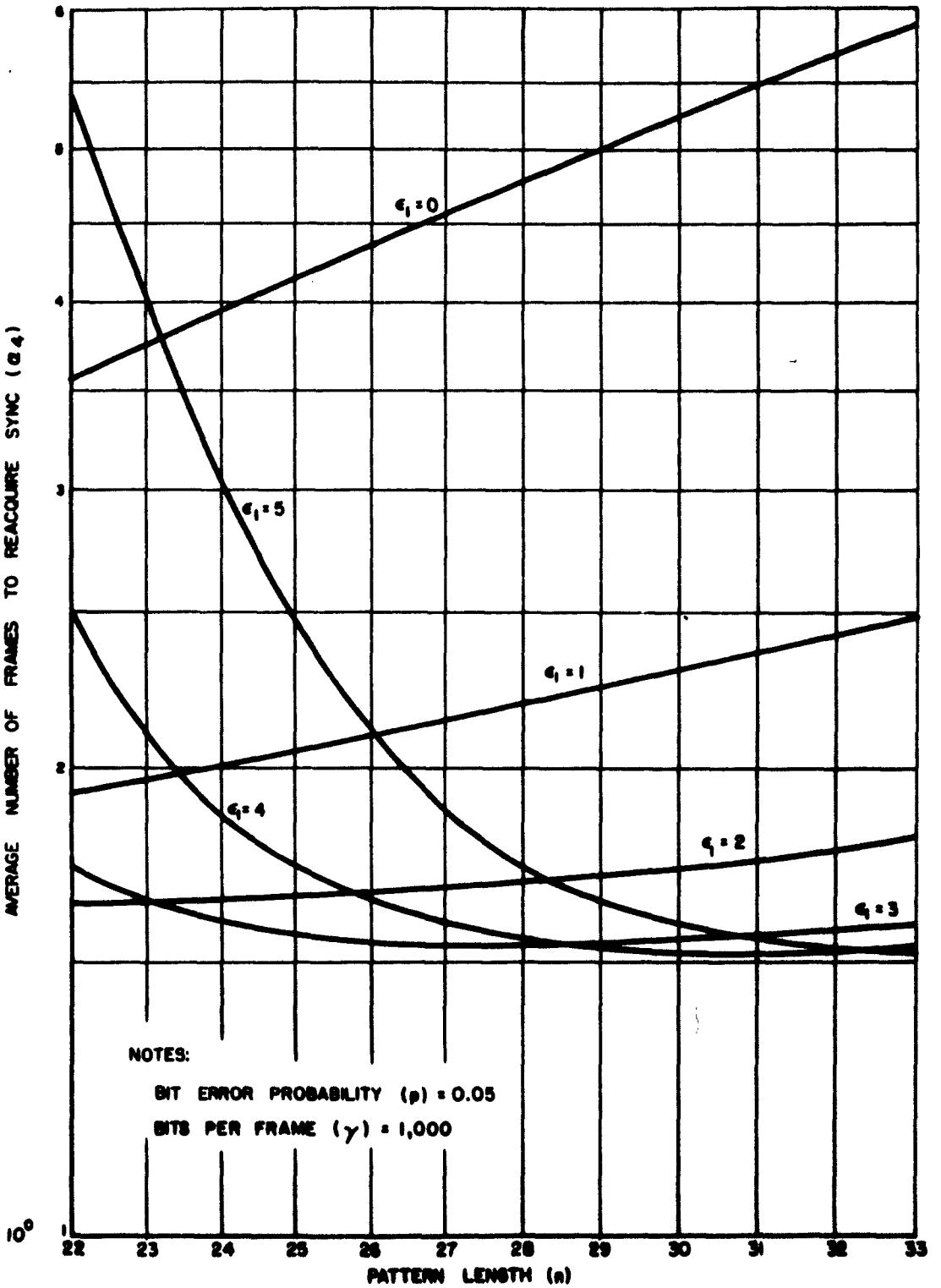


FIGURE 29. Average Number of Frames to Reacquire Sync, α_4' as a Function of Pattern Length, n, for Various Numbers of Errors Allowed (ϵ_1), p = 0.05

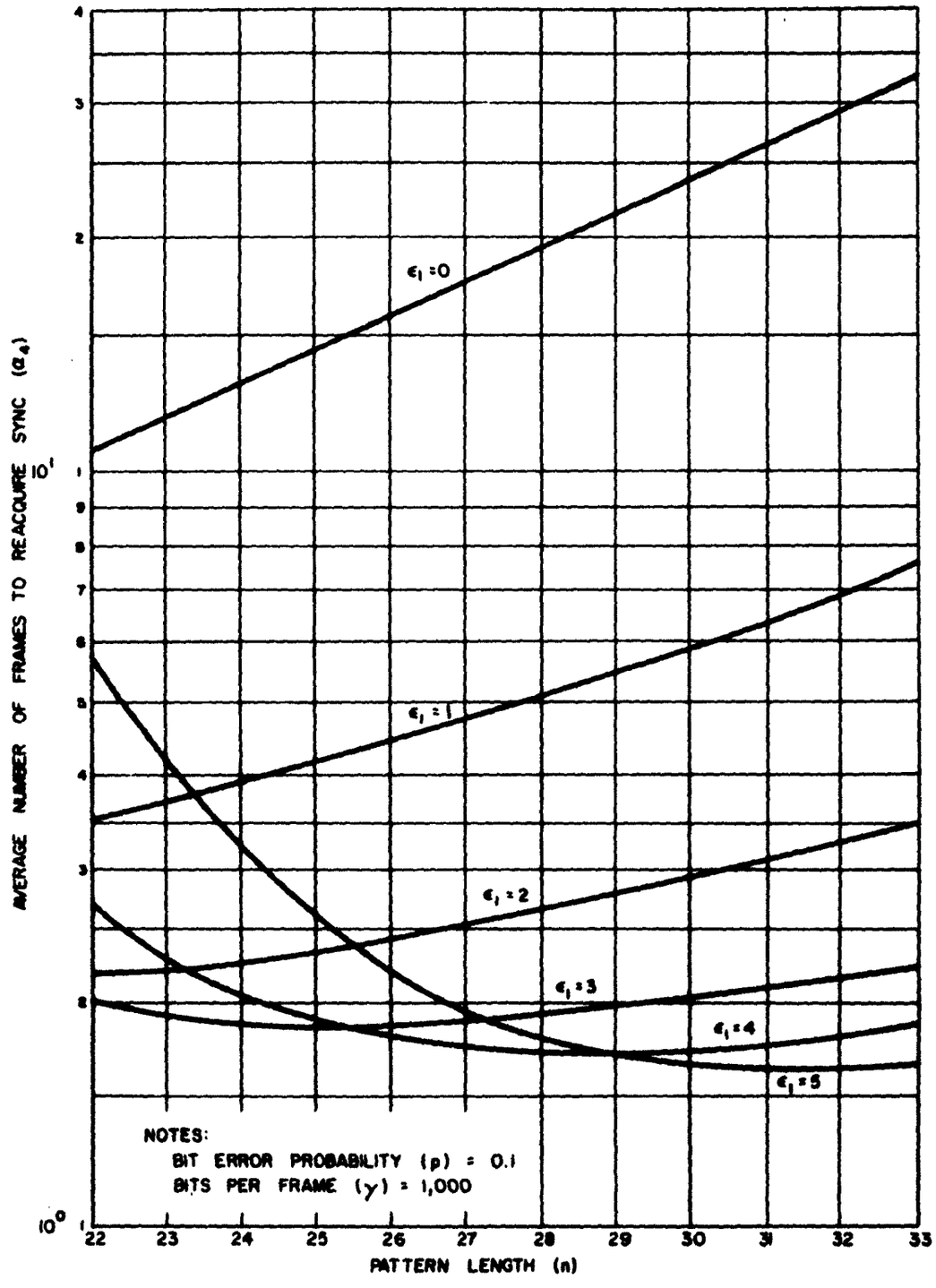


FIGURE 30. Average Number of Frames to Reacquire Sync, α_4, as a Function of Pattern Length, n, for Various Numbers of Errors Allowed (ϵ_1), p = 0.1

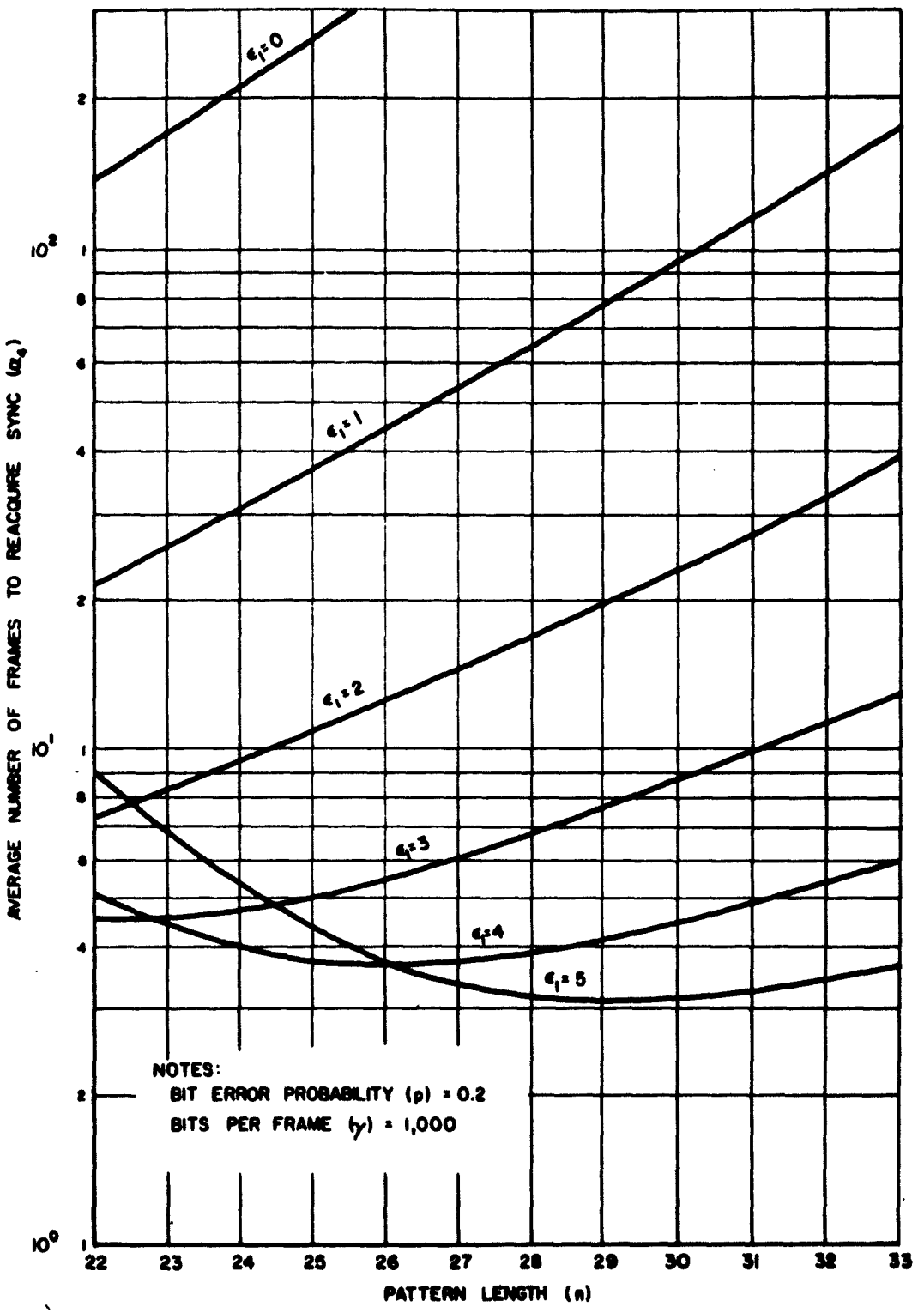


FIGURE 31. Average Number of Frames to Reacquire Sync, α_4, as a Function of Pattern Length, n, for Various Numbers of Errors Allowed (ϵ_1), p = 0.2

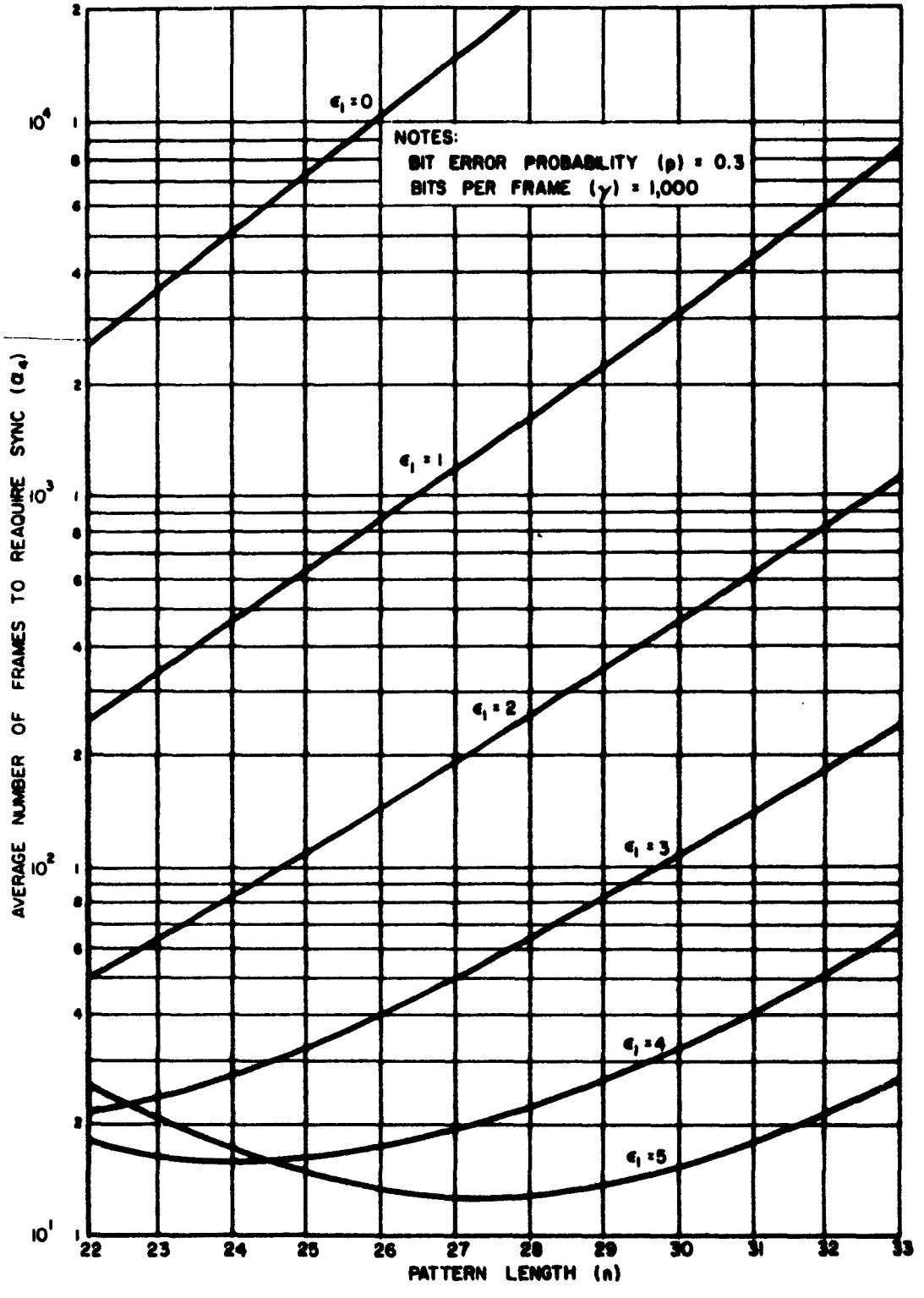


FIGURE 32. Average Number of Frames to Reacquire Sync, α_4, as a Function of Pattern Length, n, for Various Numbers of Errors Allowed (ϵ_1), p = 0.3

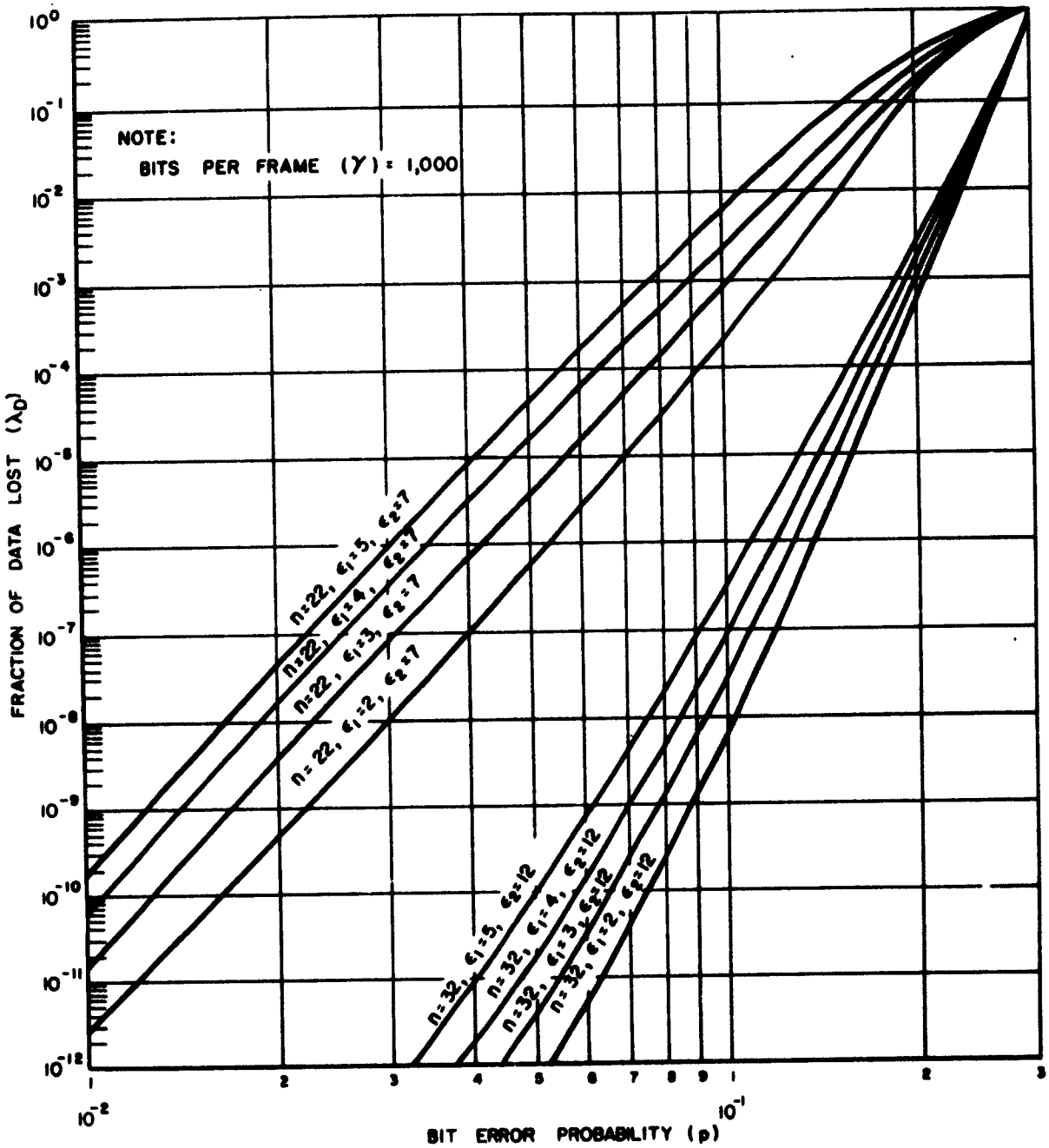


FIGURE 33. Fraction of Data Lost, λ_D, as a Function of Bit Error Probability, p

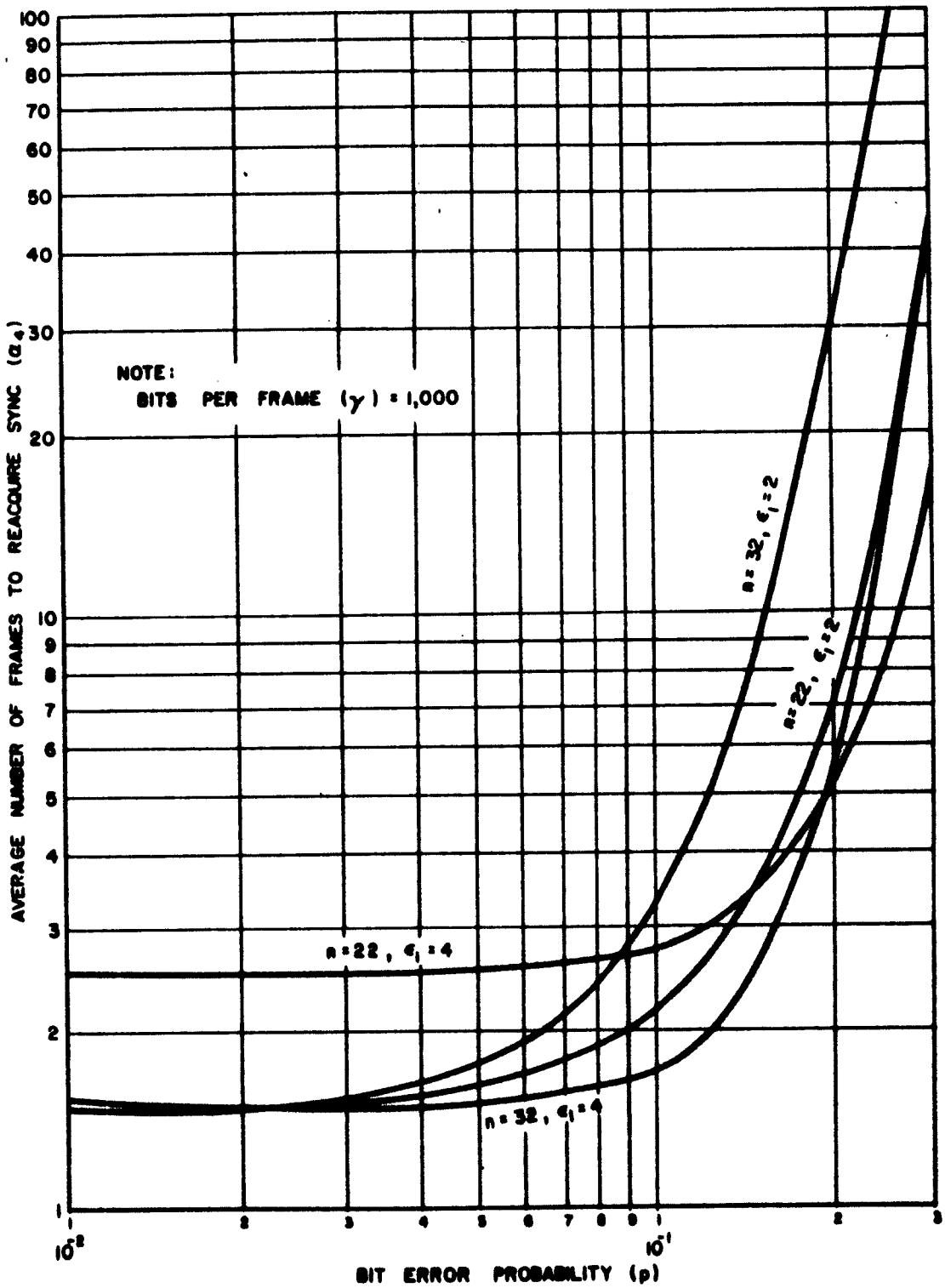


FIGURE 34. Average Number of Frames to Reacquire Sync, α_4, as a Function of Bit Error Probability, p

TABLE 6. Performance of Dual-Mode System for Different Values of ϵ_1 and ϵ_2

$\beta = 1000$; $p = 0.1$; $n = 31$.

ϵ_1	ϵ_2	$P_n(\epsilon_1)$	$F_n(\epsilon_2)$	α_1	α_2	H_β	π	λ_D
1	10	0.169	0.035	5.40	5.90	8.9×10^{-5}	1.1×10^{-8}	7.1×10^{-8}
2	10	0.338	0.035	2.07	2.58	5.9×10^{-4}	7.5×10^{-8}	2.3×10^{-7}
3	10	0.624	0.035	1.11	1.61	2.3×10^{-3}	4.7×10^{-7}	9.8×10^{-7}
4	10	0.807	0.035	0.75	1.25	1.7×10^{-3}	2.6×10^{-6}	4.5×10^{-6}
5	10	0.916	0.035	0.65	1.10	9.2×10^{-2}	1.2×10^{-5}	2.1×10^{-5}
6	10	0.969	0.035	0.72	1.05	3.6×10^{-2}	4.6×10^{-5}	8.1×10^{-5}
7	10	0.990	0.035	0.92	1.02	8.1×10^{-1}	1.0×10^{-4}	2.4×10^{-4}
4	9	0.807	0.015	0.75	1.25	1.7×10^{-2}	1.3×10^{-5}	2.2×10^{-5}
4	10	0.807	0.035	0.75	1.25	1.7×10^{-2}	2.6×10^{-6}	4.5×10^{-6}
4	11	0.807	0.075	0.75	1.25	1.7×10^{-2}	4.7×10^{-7}	8.3×10^{-7}

ϵ_2 is held constant at 10 and ϵ_1 varied from 1 to 7. The initial acquisition time, α_1, is not a sensitive function of ϵ_1, except at low values of ϵ_1. The fractional frames out of sync, λ_D, decrease rapidly as ϵ_1 is decreased. For $\epsilon_1 = 3$, the system is out of sync approximately one frame in every 10^6 frames, yet the initial acquisition time is only a little over one frame. In general, a great reduction in the percentage of frames out of sync can be achieved at a small sacrifice in acquisition time by proper selection of ϵ_1 and ϵ_2.

In the second part of Table 6, where ϵ_1 is held constant at 4 and ϵ_2 is varied from 9 to 11, it can be seen that frame sync performance is improved by increasing ϵ_2. The upper limit on the magnitude of ϵ_2 is determined by the maximum allowable values of $F_n(\epsilon_2)$ and $H_b(\epsilon_2)$ as established by Equations (38) and (39). Graphs such as appear in Figures 9, 10, and 11 can be used to find $F_n(\epsilon_2)$, which is a function of n, ϵ_2, and p. $H_b(\epsilon_2)$ is a function also of the displacement position, b, and is not so easily predictable as $F_n(\epsilon_2)$. The following facts concerning $H_b(\epsilon_2)$ are listed as a guide in the selection of frame sync patterns:

1. $H_b(\epsilon_2)$ at $p = 0.5$ is equal to $F_n(\epsilon_2)$.

2. $H_b(\epsilon_2)$ may or may not be a monotonic function of p.

3. The maximum value of $H_b(\epsilon_2)$ may be greater than $F_n(\epsilon_2)$.

4. For $E_b \leq \epsilon_2$, the value of $H_b(\epsilon_2)$ at $p = 0$ will not be zero; however, it will always be zero for $E_b > \epsilon_2$.

5. The maximum value $H_b(\epsilon_2)$ may occur at $p = 0$, e.g., when $(n - b) > 2E_b$.

IV. CONCLUSIONS

The following are the principal conclusions and recommendations of this investigation:

1. The total data-filter bandwidths (i.e., the net effect of premodulation and postdetection filtering) should not be narrower than 0.8 times the bit rate at the 3-db point with an attenuation of at least 36 db per octave beyond this point.

2. The SRR is preferred to the LMF for two reasons: (a) greater flexibility to changes in bit rate, and (b) an improved relationship between recognition probability and false-sync probability.

3. A dual-mode frame sync scheme is recommended, wherein the retention probability is increased by increasing the number of errors allowed by the recognizer while in the retention mode.

4. For frame lengths up to 2048 bits, frame sync patterns between 22 and 33 bits permit stable frame sync up to a bit error probability of 0.1 or more.

5. The use of word-sync bits assigned to each word of the frame is not recommended because the improvement in sync capability does not justify the added information capacity required.

6. The use of the three-bit aperture in the retention mode, plus a code selected for this criterion, leads to improved performance under two conditions: (a) when phase slippage of the VCO in the phase-lock loop is occurring, and/or (b) when the negative correlation peak (in addition to the positive) is used in the recognition logic. Under good S/N conditions and for a conservatively designed system, the improvement is modest; however, to provide for improved operation under threshold conditions (since the added complexity is slight), the three-bit aperture is recommended. Results of the limited investigation into the use of the negative correlation peak are not sufficient to justify its recommendation.

7. As a means of avoiding the static data problem, one of the following techniques is recommended: (a) replace the frame sync pattern with its complement in alternate frames, or (b) insert the frame sync pattern in every other frame, leaving out the complement (Ref. 7).

8. When sync must be maintained at an S/N ratio much below unity, a carrier-lock system is recommended, wherein the bit rate is coherent with the RF carrier.

APPENDIX

Probability of Sync Pattern Recognition, $P_n(\epsilon)$

Regeneration of the PCM signal by integration over each bit period constitutes a sequence of independent events. The probability p that any given bit is in error is a function of S/N. The probability that exactly r errors occur in an n bit frame sync pattern is given by the binomial distribution

$$C_r^n p^r (1 - p)^{n-r}$$

where the order of occurrence of the errors does not matter. If the pattern recognizer is set to allow ϵ errors, all patterns with ϵ or less errors will be accepted by the recognizer. The occurrence of one sequence of bits excludes all others; therefore the events involved in the binomial distributions are mutually exclusive. The sum of all distributions between r = 0 and r = ϵ is equal to the probability that one of the acceptable patterns will occur, therefore

$$P_n(\epsilon) = \sum_{r=0}^{\epsilon} C_r^n p^r (1 - p)^{n-r} \tag{44}$$

Probability of Random Generation of Sync Pattern, $F_n(\epsilon)$

For purposes of analysis, all bits in the frame other than those in the sync pattern are considered to be randomly generated; that is, each of these bits has a 50 percent probability of being a one or a zero. The probability that any group of n random bits is a recognizable sync pattern is given by Equation (44) where p is defined as the probability that a given bit does not agree with the sync pattern. The probability that n random bits differ from the sync pattern by ϵ or less bits is obtained from Equation (44) when p is equal to one half.

$$F_n(\epsilon) = (\tfrac{1}{2})^n \sum_{r=0}^{\epsilon} C_r^n \tag{45}$$

Probability of One or More Random Sync Pulses per Frame, H_β

The probability that at least one false-sync pattern will occur in the β random bits of each frame is a function of $F_n(\epsilon)$. Let $A_1, A_2, \ldots A_\beta$ be the events representing the occurrence of a false-sync pattern from

the first of the β bits to the last. $P(A_1)$, $P(A_2)$, ... $P(A_\beta)$ are the probabilities of these events occurring. Some of these events are related; thus, a general expression for H_β may be written from the addition theorem

$$H_\beta = \sum_{i=1}^{\beta} P(A_i) - \sum_{i=1}^{\beta} \sum_{j=1}^{\beta} P(A_i A_j) + \ldots \pm P(A_1 A_2 \ldots A_\beta)$$

where

$$i \neq j \neq k \ldots \neq \beta$$

$$i < j < k \ldots < \beta$$

All events separated by more than n bits are independent. For example, events A_i and A_j are independent provided $(j - i) > n$. Therefore when β is large compared to n, the number of events A_i and A_j that are independent is much greater than the number that are related. For two independent events, the probability of their joint occurrence is the product of $P(A_i)$ and $P(A_j)$. With patterns suitable for frame sync purposes, the probabilities of related events $P(A_iA_j)$ are nearly always less than the probabilities for independent events $P(A_i)$,$P(A_j)$. With practical parameters, the probabilities $P(A_i)$ are small compared to unity, which causes the higher order multiple event probabilities to be small compared to the lower order ones. Under these conditions, a good approximation for H_β is obtained when it is assumed that all events A_i, A_j,... A_β are independent.

$$H_\beta = \sum_{i=1}^{\beta} P(A_i) - \sum_{i=1}^{\beta} \sum_{j=1}^{\beta} P(A_i)\, P(A_j) + \ldots \pm P(A_1)\, P(A_2) \ldots P(A_\beta)$$

where

$$i \neq j \neq k \ldots \neq \beta$$

$$i < j < k \ldots < \beta$$

The preceding equation can also be written

$$H_\beta = 1 - [1 - P(A_1)][1 - P(A_2)] \ldots [1 - P(A_\beta)]$$

and since $F_n(\epsilon) = P(A_1) = P(A_2) = \ldots$, this reduces to

$$H_\beta = 1 - [1 - F_n(\epsilon)]^\beta \qquad (46)$$

Probability of Displacement of Sync Pattern, $H_b(\epsilon)$

The general expression for the probability of displacement of the frame sync pattern by b bits is

$$H_b(\epsilon) = \left(\tfrac{1}{2}\right)^b \sum_{i=E_b-\epsilon}^{E_b} C_i^{E_b} p^i q^{E_b-i} \sum_{j=0}^{\epsilon-E_b+i} C_j^{n-E_b-b} p^j q^{n-E_b-b-j} \cdot \sum_{k=E_b+b-\epsilon-i+j}^{b} C_k^b \qquad (47)$$

This equation was developed by the following procedure. For a particular n-bit pattern with ϵ errors allowed by the recognizer, a displacement of b bits was assumed. Then, by inspection, all possible ways in which a recognition could occur were listed. The probability for each of these events was derived by simple probability theory in terms of the bit error probability p. Since these events are mutually exclusive, the sum of their probabilities equals the total probability of the occurrence of a recognition in the assumed displaced position. The summation limits and probabilities were then expressed in terms of the parameters n, ϵ, b, and E_b and the summation indexes i, j, and k.

Probability of One or More Displaced Sync Pulses per Sync Pattern Scanned, H_δ

A general expression for the probability of one or more displaced sync patterns per frame sync pattern scanned can be written from the addition theorem

$$H_\delta = \sum_{i=1}^{2n-1} P(A_i) - \sum_{i=1}^{2n-1} \sum_{j=1}^{2n-1} P(A_i A_j) + \ldots \pm P(A_1 A_2 \ldots A_{2n-1})$$

where

$$i \neq j \neq k \ldots \neq (2n-1)$$

$$i < j < k \ldots < (2n-1)$$

$A_i, A_j, \ldots A_{2n-1}$ are events representing the occurrence of displaced sync patterns from the first bit of the frame sync pattern that enters the recognizer to the last. $P(A_iA_j)$ is the probability that displaced patterns occur in two different positions of the overlap region. With sync patterns suitable for frame sync purposes, the higher order multiple event proba-

bilities are smaller than the lower order ones. This fact allows the following inequality to be written from the preceding equation

$$H_\delta < \sum_{i=1}^{2n-1} P(A_i)$$

The probabilities $P(A_iA_j)$, $P(A_iA_jA_k)$, ... are normally so small compared to the $P(A_i)$ probabilities that the sum of the $P(A_i)$ probabilities is a good approximation to H_δ. Displacement properties are symmetrical about the sync position, hence

$$H_1(\epsilon) = P(A_{n-1}) = P(A_{n+1})$$

$$H_2(\epsilon) = P(A_{n-2}) = P(A_{n+2})$$

.
.
.

A good approximation for H_δ can therefore be written

$$H_\delta \approx 2 \sum_{b=1}^{n-1} H_b(\epsilon) \tag{48}$$

Probability of One or More False-Sync Pulses per Frame, H_γ

The probability that one or more false-sync pulses will occur per frame must include both the probability of displacement, H_δ, and the probability of random generation, H_β. The events involved in these two probabilities are independent. The probability that no displaced pulses occur per frame is $(1 - H_\delta)$ and the probability that no randomly generated pulses occur per frame is $(1 - H_\beta)$. The probability that neither of these events will occur in a given frame is $(1 - H_\delta)(1 - H_\beta)$. The probability that one or the other or both of these events will occur is

$$H_\gamma = 1 - (1 - H_\delta)(1 - H_\beta) \tag{49}$$

Probability of Loss of Frame Sync per Frame in the Dual-Mode System, π

To lose frame sync in the dual-mode system while in the retention phase requires the occurrence of two events. The first event is failure to recognize the frame sync pattern, the probability of which is given by $1 - P_n(\epsilon_2)$. The second event is the occurrence of one or more

false-sync pulses during the time necessary to reacquire the retention mode. The average number of frames required to recognize a frame sync pattern in the acquisition phase is α_0. The number of random bit positions scanned in α_0 frames is $\alpha_0\beta$. From Equation (46) it is seen that the probability of one or more randomly generated false-sync pulses occurring in $\alpha_0\beta$ frames is

$$1 - [1 - F_n(\epsilon_1)]^{\alpha_0\beta}$$

$H_\delta(\epsilon_1)$ is neglected, since it is usually small compared to H_β. The two events necessary for loss of frame sync are independent; thus, the probability of loss of frame sync in a given frame is

$$\pi = [1 - P_n(\epsilon_2)]\left\{1 - [1 - F_n(\epsilon_1)]^{\alpha_0\beta}\right\} \tag{50}$$

If $H_\delta(\epsilon_1)$ is included in the calculation, Equation (50) becomes

$$\pi' = [1 - P_n(\epsilon_2)]\left\{1 - [1 - H_\delta(\epsilon_1)]^{\alpha_0}[1 - F_n(\epsilon_1)]^{\alpha_0\beta}\right\}$$

where the prime is added to indicate that $H_\delta(\epsilon_1)$ is involved. π' is derived by an extension of the development for Equation (50). There are α_0 sync patterns scanned in α_0 frames, and the events associated with $H_\delta(\epsilon_1)$ and $F_n(\epsilon_1)$ are independent.

Average Number of Frames for Search Phase, α_1

The search phase extends from acquisition of bit sync to recognition of the first frame sync pattern. It is assumed that, on the average, bit sync is acquired in the middle of a frame. To recognize one correct sync pattern, α_0 sync patterns must be examined. Thus, if no false-sync pulses are encountered, an average of $(\alpha_0 - \frac{1}{2})$ frames will be scanned for each frame sync pattern recognized. The number of random bit positions scanned in $(\alpha_0 - \frac{1}{2})$ frames is $(\alpha_0 - \frac{1}{2})\beta$. When H_δ is neglected, the number of false-sync pulses expected during the search phase is $(\alpha_0 - \frac{1}{2})\beta F_n(\epsilon_1)$. For each false-sync pulse that occurs, the bits-per-frame counter is inhibited from resetting for one full frame. The average number of frames for the search phase is, therefore

$$\alpha_1 = (\alpha_0 - \tfrac{1}{2})[1 + \beta F_n(\epsilon_1)] \tag{51}$$

where

$$F_n(\epsilon_1) << 1$$

$$H_\delta(\epsilon_1) << H_\beta(\epsilon_1)$$

If $H_\delta(\epsilon_1)$ is not neglected, an additional $(\alpha_0 - \frac{1}{2})H_\delta(\epsilon_1)$ frames will be gated out and the average frames required for the search phase will be

$$\alpha_1' = (\alpha_0 - \tfrac{1}{2})[1 + \beta F_n(\epsilon_1) + H_\delta(\epsilon_1)]$$

Average Number of Frames for Verification Phase, α_2

The verification phase begins after recognition of a frame sync pattern; for this reason, α_0 full frames must be scanned in order to examine α_0 sync patterns. At the beginning of verification, Gate 1 is closed by flipflop 2 (as shown in Figure 15) thus preventing reset of the bits-per-frame counter for one full frame. Therefore, the average number of frames during which a false-sync pulse can reset the bits-per-frame counter is $(\alpha_0 - 1)$. When $H_\delta(\epsilon_1)$ is neglected, the expected number of false-sync pulses that will occur during the verification phase is $(\alpha_0 - 1)\beta F_n(\epsilon_1)$. For each false-sync pulse that occurs, one frame is gated out, as explained previously. If it is assumed that the false-sync pulses occur, on the average in the middle of the frame, the average number of frames to reacquire sync is $(\alpha_1 + 1)$. Therefore, the average number of additional frames required because of false-sync pulses is $(\alpha_0 - 1)(\alpha_1 + 1)\beta F_n(\epsilon_1)$. The average number of frames required for the verification phase is then

$$\alpha_2 = \alpha_0 + (\alpha_0 - 1)(\alpha_1 + 1)\beta F_n(\epsilon_1) \qquad (52)$$

where

$$F_n(\epsilon_1) << 1$$

$$H_\delta(\epsilon_1) << H_\beta(\epsilon_1)$$

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NOMENCLATURE

A_b	Autocorrelation function. The number of bits in agreement minus the number of bits in disagreement with the recognizer in the overlap region for a displacement of b bits.
b	Number of bits displaced from true sync position.
C	Electrical capacitance.
C_r^n	Binomial coefficients of the number of combinations of n distinct things taken r at a time.
d_1	Width of actual sampling aperture.
d_2	One-half the period of one cycle of a continuous wave.
E_b	Bits in disagreement with the recognizer in the overlap region for a displacement of b bits.
E_p	Peak amplitude of non-return-to-zero (NRZ) signal.
$e_i(t)$	Input signal as a function of time.
erf x	Error function of x.
e(t)	Time function of input signal to integrating bit detector.
$F_n(\epsilon)$	Probability of false generation of an n-bit sync pattern with ϵ errors or less from a random bit stream.
$F_n(\epsilon)'$	Probability that the output of a linear matched filter (LMF) will exceed a threshold corresponding to ϵ allowed errors from a random bit stream.
$F_n(\epsilon)N$	Probability of falsely generating a sequence of n bits from a random bit stream that satisfies the preselected threshold conditions on both the positive and negative correlation peaks.
f_b	Bit frequency.
f_f	Frame frequency.
f_1'	Average transition frequency in a non-return-to-zero (NRZ) signal.
$G(\omega)$	Noise power spectral density at input to integrating bit detector.

$H_b(\epsilon)$	Probability of false recognition when the recognizer is displaced by b bits from the true sync position and with ϵ or fewer errors allowed by the recognizer.
H_β	Probability of false generation of an n-bit sync pattern one or more times in β successive random bits with the recognizer set to allow ϵ or fewer errors.
H_γ	Probability of one or more false-sync indications per frame from an n-bit recognizer set to allow ϵ or fewer errors.
H_δ	Probability of one or more false-sync indications during the overlap region of each sync pattern with ϵ or fewer errors allowed by the recognizer.
$H(j\omega)$	Transfer function.
i, j, k	Summation indexes.
K	Gain constant.
K	Probability that the retention phase will be acquired falsely.
k	Number of bits agreeing with the linear matched filter (LMF), also the number assigned to the corresponding LMF output level.
L_β	Probability of loss of frame sync in any one frame for the single-mode system where H_δ is neglected.
L_γ	Probability of loss of frame sync in any one frame for the single-mode system where H_δ is considered.
M	Probability that the dual-mode system will remain out of sync for α frames before switching back to acquisition when the recognizer is examining all random bits.
N	Probability that the dual-mode system will remain out of sync for α frames before switching back to acquisition when the recognizer is in an overlap position.
N_d	Number of bits in disagreement.
N_i	Instantaneous amplitude of noise at input.
N_o	Instantaneous amplitude of noise at output.
n	Number of bits in the frame sync pattern.
n_a	Number of bits in agreement.
$P(N_o > E_p)$	Probability that recognition will not occur in linear matched filter (LMF) when the threshold is set midway between the maximum and next-to-maximum levels.

$P(N_o < E_p)$ Probability that recognition will occur in a linear matched filter (LMF) when the threshold level is set midway between the maximum and next-to-maximum levels.

$P(N_o > S_o)$ Probability of an error in detection of a bit in an integrating bit detector.

$P(N_o > |2n - 1 - 2K - 2\epsilon| F_p)$ Probability of a false-sync indication occurring in a linear matched filter (LMF).

$P_n(\epsilon)$ Probability that an n-bit sync pattern will contain ϵ or fewer errors for a bit error probability of p.

$P_n(\epsilon)'$ Probability that a threshold corresponding to ϵ or fewer allowed errors will be exceeded at the output of the linear matched filter (LMF).

$P_n(\epsilon)N$ Probability that preselected threshold levels will be exceeded for both the positive and negative correlation peaks.

$P_n(k)$ Probability that the kth level will exist at the output of the linear matched filter (LMF) for any group of random bits.

$P_n^{\epsilon}(k)$ Probability of the simultaneous occurrence of the kth level in the output of the linear matched filter (LMF) and of instantaneous noise amplitude exceeding that kth level.

$P_n(r)$ Probability that an event will occur exactly r times in n independent trials when the probability that the event will occur in a single trial is p.

p Probability of error in a single bit.

q Probability of correct detection of a single bit.

R Electrical resistance.

S_i RMS signal at input to the integrating bit detector.

S_o Signal amplitude at the output of the integrating detector at end of the integration period.

S/N RMS signal to RMS noise ratio.

T Interval of time equal to 10 times the interval between assured bit transitions.

X The probability that α successive frame sync patterns will be examined without a recognition.

x Used in error function.

α Number of successive frames.

α_1 Average number of frames for search phase.

α_2	Average number of frames for verification.
α_3	Average number of frames to reacquire retention phase after a false alarm.
α_4	Average number of frames out of sync each time sync is lost because of a false alarm.
α_5	Average number of frames between false alarms for single-mode system where α consecutive frames are required to elapse without a recognition before the system returns to the acquisition or verification phase.
α_0	Average number of sync patterns examined per recognition.
α_{01}	Average number of frames to reacquire sync when lost (single mode).
β	Number of bit positions per frame in which the recognizer is examining all random bits.
γ	Total number of bits per frame.
ϵ	Maximum number of errors allowed by the recognizer. In general, it refers to the positive correlation peak.
ϵ_1	Maximum number of errors allowed by the recognizer in search and verification phases.
ϵ_2	Maximum number of errors allowed by the recognizer in retention mode.
ϵ_3	Minimum number of disagreements allowed by the recognizer in the search and verification phases when detecting the negative correlation peak.
ζ	Damping ratio.
λ_D	Fraction of frames out of sync in dual-mode system.
λ_s	Fraction of frames out of sync in single-mode system.
λ_{sc}	Fraction of frames out of sync in single-mode system when α consecutive frames must elapse without a recognition before the system returns to acquisition.
π	Probability of loss of sync per frame in the dual-mode system where $H_\delta(\epsilon_1)$ is neglected.
π'	Probability of loss of sync per frame in the dual-mode system where $H_\delta(\epsilon_1)$ is included.
σ	RMS value of noise.

σ_i	RMS noise at input to linear matched filter (LMF).
σ_o	RMS noise at output of linear matched filter (LMF).
τ	Period of bit frequency.
τ_2	Major control network time constant of phase-lock loop.
τ_2'	Effective control network time constant of phase-lock loop.
ω_n	Undamped natural resonant frequency of phase-lock loop.
ω_n'	Effective natural resonant frequency of phase-lock loop.

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UNCLASSIFIED

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