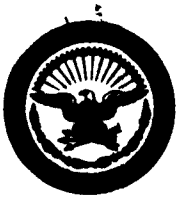

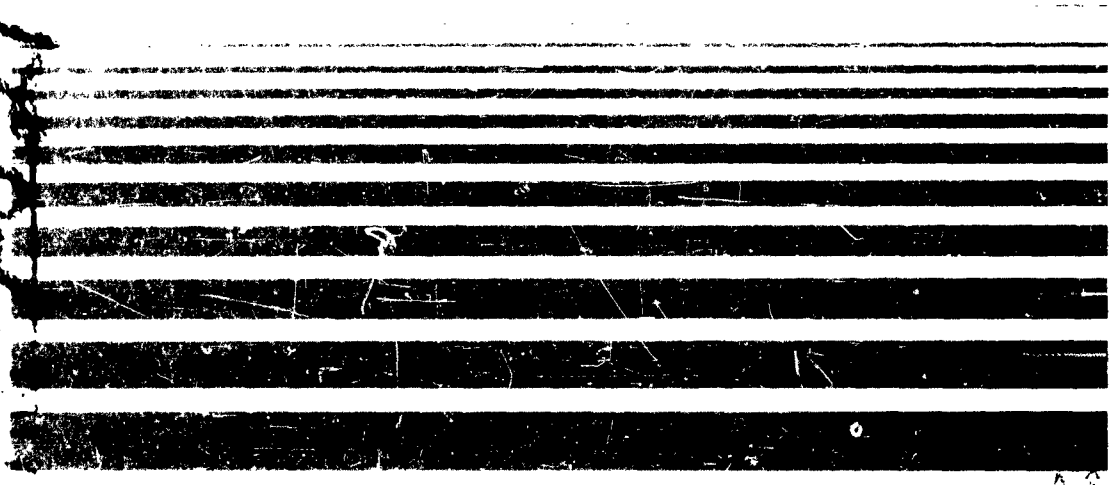

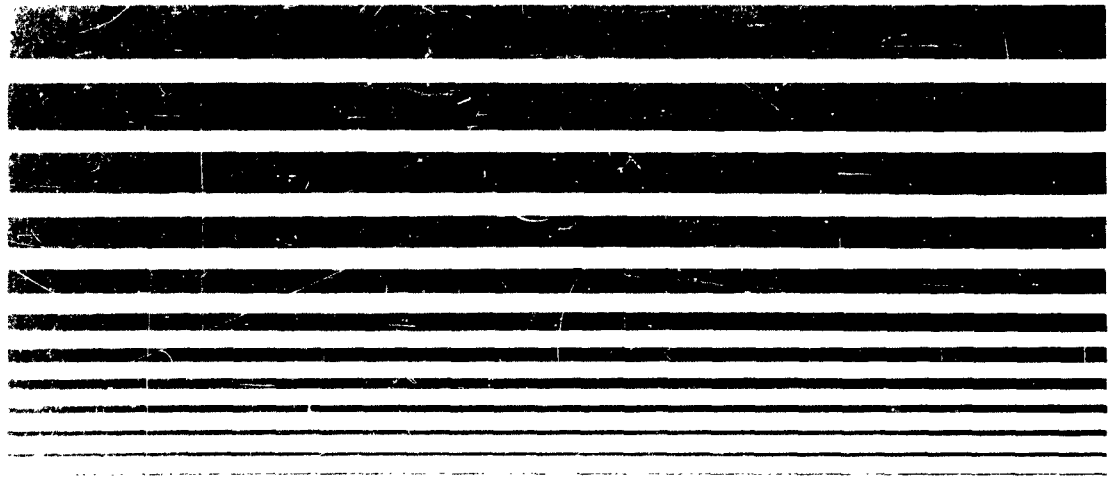

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Third Interim Development Report for Research and Development of Solid State Tunnel Devices and Arrays Capable of Operation at Microwatt Power Levels

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ABSTRACT

A material study on GaAs is performed in view of its possible use for the fabrication of microwatt tunnel diodes. A technology of actually fabricating these devices is described. The experimental diodes exhibit a peak current of < 10 μA at an optimum value for the peak current density of 10 A/cm^2, a peak-to-valley ratio of 6 to 10, and possess a theoretical switching time of about 0.1 μ sec at $\sim$ 0.5 pF junction capacitance.

A discussion of the properties of the experimental microwatt tunnel diodes in the frame work of the current theories on electron tunneling through a narrow p-n junction barrier is made. In some aspects agreement with theory is close, in others, it is poor.

SECTION I

I.1 Purpose

The purpose of the present contract is to conduct a research program in the field of solid state tunnel devices capable of non-linear and active operation at low power levels. In particular, studies are to be made of small area backward and tunnel diodes which are fabricated on semiconductor substrates and are capable of operating in the microampere range.

The most promising device will be developed further and tested with the view towards possible use in high speed microwatt logic circuits. In addition, attempts will be made at the fabrication of arrays of the device. If necessary, electron beam technology will be employed in the device fabrication in order to provide for more rigid control of the extremely small dimensions associated with such devices. In this regard, a simple feasibility model of a programmed deflection system for the electron beam will be developed. Such a system could then be used in conjunction with a process for automatically producing arrays of devices.

I.2 General Factual Data

1. Chief Investigator -- Dr. R. Engelmann
2. Fabrication and Measurement Apparatus:

Resistivity Measurements:

Baird Associates' Four-Point Probe

Alloying:

Tantalum Strip Heater, forming gas atmosphere

Penetration of Alloying:

Microscope interference measurement of 2° angle lapped and stained surface under glass plate in sodium light

DC Characteristic Measurements:

Type 575 Tektronix Curve Tracer

Capacitance Measurements:

Model 74C Boonton Capacitance Bridge

Voltage and Current Measurements:

a. Model 241 Keithley Voltage Supply

b. Model 415 Keithley Microammeter

c. Model 610-R Keithley Electrometer

Wafer Dicing:

Kulicke & Soffa Manual Wafer Scriber

I.3 Detailed Factual Data

1. Material Properties of GaAs

GaAs is available in single and poly-crystals. Because the material is still relatively expensive, it was decided to use the less expensive poly-crystalline material for the preliminary investigations in order to select a narrow resistivity range suitable for the fabrication of microwatt tunnel diodes.

GaAs crystals (single or poly) are grown by different methods: The floating zone process (zone refining) is carried out in a horizontal boat; the Bridgman type of procedure is made in a sealed crucible; in a third method the crystal is pulled vertically from the melt (Czochralski process). For the first two types a relatively large surface of the melt is in contact with the boat or crucible which gives rise to a certain amount of contamination in the produced crystals. This contact is maintained also during solidification and may introduce imperfections by micro-strains. In the Czochralski process the contact area is reduced by a large fraction and completely avoided for the crystallized portion. Pulled crystals, therefore, are marked by highest crystal perfection and purity.

The carrier concentration is determined by Hall measurements. For degenerate semiconductors the following relationship holds:[1,2]

$$n = \frac{1}{qR} \tag{1}$$

where R = Hall constant, q = electron charge = 1.6×10^{-19} coulombs and n = carrier density. From measurements of the resistivity ρ the carrier mobility μ can be calculated: One has

$$\rho = \frac{1}{qn\mu} \tag{2}$$

yielding with (1):

$$\mu = \frac{R}{\rho}$$

(Note: For degenerate semiconductors, Hall mobility and conductivity mobility are equal[1,2]).

Resistivity measurements on polycrystalline material are not uniquely determined because of potential barriers between crystallites[3] and, therefore, can only be considered as a guidance.

The carrier density in GaAs, as determined from Eq. (1), is not a unique function of the resistivity, as in the case of high quality silicon,[4] presumably because of large differences in the degree of crystal perfection and purity for GaAs. For GaAs, the spread in carrier mobility of the same carrier density is larger than a factor of 2, especially pronounced in p type material. It is therefore not possible to determine carrier densities from resistivity values as it is usually done in the case of silicon. Carrier densities for GaAs can only be determined by Hall measurements.

The polycrystalline GaAs material used in our studies so far was Zn doped (p type) and was supplied by Diotron, Inc., Philadelphia, Pennsylvania and by Merck & Company, Inc., Rahway, New Jersey. The material properties are shown in Table 1.

Diotron labeled only the approximate resistivity of its material and did not determine carrier densities. We intend to perform Hall measurements for this material in our laboratory as soon as suitable equipment is available.

Merck stated the carrier densities and, in case of Item 5, also resistivity (and hence mobility), which was actually determined on single crystals fabricated by the same process. Resistivity for Merck's Items 2 through 4 was measured in our laboratory by the four-point probe method by probing several times and taking the smallest values found.

2. Technology for Forming Tunnel Junctions

The technology for forming the small tunnel junction areas needed in order to reduce the peak tunnel current to the microampere range, was in principle the same as had proved suitable for fabricating microwatt backward

TABLE 1. Properties of Investigated GaAs

Supplier	Item	$\rho/10^{-3}\Omega$cm	$p/10^{19}$ cm^{-3}	μ/cm^2 V^{-1} sec^{-1}	Fabrication Process
Diotron	I	3 - 4	not det.	---	boat grown
" "	II	7 - 10	" "	---	" "
Merck	2	~25	0.60	~42	" "
" "	3	~15	0.84	~50	" "
" "	4	~12	1.2	~43	" "
" "	5	3.5	2.9	61	pulled

ρ = Resistivity

p = Hole density

u = Hole mobility

diodes (tunnel rectifiers) on silicon, which was described in the Second Interim Report: pieces of ultra-high pure Sn, a n type dope for GaAs, were alloyed to p type GaAs dice on a tantalum strip heater in forming gas atmosphere. After the alloying step, the junction area was reduced by a special etching procedure to the desired value.

2.a Preparation for alloying. GaAs was prepared for alloying as follows: 15 mil thick wafers, which had been sliced from the rod by the supplier exhibiting a dull mat surface, were cut into 60 x 60 mil^2 dice by scribing and breaking. A mechanical treatment of the surface such as any lapping or polishing did not prove necessary. Each die was treated simply by etching the surface in a mixture of 1 part concentrated HF, 3 parts concentrated HNO_3 and 4 parts H_2O (HF-HNO_3-etch) for 3 to 10 minutes[5]. This gave the die a fairly uniform, shiny bright surface. The etch rate established in our laboratory for the HF-HNO_3-etch is 0.5 mil/min. After the above polishing etch another etch in a mixture of 10 parts 5% NaOH and 3 parts 30% H_2O_2 (NaOH-H_2O_2 etch) proved favorable[6]. This etch solution is highly selective revealing clearly the grain boundaries in the polycrystalline die. Some crystallite surfaces appear dull, some bright after this etch which was carried out usually for 2 to 4 min. It is interesting to note that a surface that appeared dull on one side of the die appeared bright on the other side, as it was noticed for some cases. These different etch properties of two opposite sides of the same crystal plane is caused by the compound nature of the semiconductor and has been studied in detail for the (111) plane[5]. The etch rate of the NaOH-H_2O_2-etch has not been established because it depends on the orientation of the crystal plane. It is faster for a surface that appears dull after the etch than for one that appears bright.

Small pieces of tin were cut from a 40 mil diameter high purity tin wire and etched in HCL. Residues of HCL on the tin piece proved to be an excellent flux for the alloying process: if the tin pieces were rinsed in deionized H_2O before alloying, they assumed the shape of a total sphere after melting on the GaAs surface giving rise to only little and uncontrollable wetting of GaAs. However, if the tin pieces were taken from the HCL without further cleaning, they assumed a shape of a half sphere after melting on the GaAs surface wetting the whole area of GaAs underneath the half sphere. In the further progress of the study tiny tin disks of uniform size, 10 mil in diameter and 2 mil thick, were used (supplier: Alpha Metals, Inc., Jersey City).

The disks were placed on filter paper and shortly covered with another filter paper that was soaked in HCL. Then they were cautiously picked up with tweezers and placed on the prepared surface of the GaAs die for alloying.

2.b Alloying. A tantalum strip heater was used for alloying. The dimensions of the tantalum strip were 4.5 cm long, 1.5 cm wide and 4 mil thick. After placing the GaAs die on the center of the strip, and the tin dots on the die, the alloying chamber was purged for several minutes with a fast flow of forming gas which was then reduced to about 700 cm^3/min during the alloying cycle. Thereafter, the gas flow was increased again for cooling-off the sample. Alloying was carried out by raising the strip current slowly until the tin dots started to melt at 35 A (5 to 10 sec. raising time). Then the strip current was raised quickly to a maximum value which ranged from 50 to 80 A (1 to 2 sec. raising time). The maximum heater current was maintained for a certain period (0 to 30 sec) and thereafter switched off.

2.c Properties of formed tunnel junctions. It was found that the surface preparation of GaAs and the tin dots, as well as the temperature cycle of the alloy step have a profound influence on the dc characteristics of the formed tunnel junctions. Some junctions had to be etched in HCL (or $HF-HNO_3$) for a short time before evaluation, in order to remove some shunt channel on the surface. In particular, the following observations were made:

1. Using no HCl flux for the tin dots resulted in a rather large spread of the peak current density for the same GaAs material and at the same temperature cycle (junction areas were measured by microscopic means), e.g. for a 7 - 10 x $10^{-3}\Omega$cm GaAs from Diotron, peak current densities from 6 to 20 A/cm^2 were measured for junctions formed on the same GaAs die (bright surface, no $NaOH-H_2O_2$-etch) with a short, low maximum temperature cycle (maximum heater current 50 A maintained for less than 1 second). Peak-to-valley ratio was about 10 for the higher current-density units and 4 to 5 for the lower ones.

2. With HCl flux applied to the tin dots, peak current densities were fairly uniform for the same temperature cycle, somewhat higher on a bright GaAs surface compared to a dull one (after etch in $NaOH-H_2O_2$); e.g. peak current density for diodes on 7 - 10 x $10^{-3}\Omega$ cm GaAs from Diotron was about 10 A/cm^2 for a dull surface and 15 A/cm^2 for a bright one with a short, low maximum temperature alloying cycle. Peak-to-valley ratio was 5 to 7 (Fig. 1).

3. Increasing the duration at maximum heater current and/or increasing the maximum heater current resulted in lower current-density junctions with lower peak-to-valley ratios when HCl flux was used. The same happened for multiple alloying. In case of the 7 - 10 x $10^{-3}\Omega$ cm GaAs from Diotron, a reduction in peak current density to 1/10 of the original value was found (Fig.2). Simultaneously, the peak and valley point voltages shifted to lower values (compare Figs. 1 and 2, the peak current voltage decreases from about 150 mV to about 80 mV). The decrease in the peak-to-valley ratio is mainly caused by a pronounced increase of the excess current at the original valley point voltage of about 0.5 V, which may even create a secondary tunnel peak (hump excess current) near this voltage (see Fig. 2c). The GaAs surface usually stained to a dark blue color with these longer and higher temperature cycles.

4. Very rapid temperature cycling sometimes resulted in lower peak-to-valley ratios when HCl flux was used; e.g. peak-to-valley ratio measured with 7 - 10 x $10^{-3}\Omega$ cm GaAs from Diotron, at a temperature cycle with 60 A maximum heater current held for $<$ 1 sec, was 2 to 4 at ca. 10 A/cm^2 peak current density. It is assumed that in this case the higher valley current is caused by an imperfect GaAs regrowth yielding some kind of shorting between tin and the original p type surface.

5. Differences in the heat transfer between heater strip and sample sometimes may cause a certain deviation from the general trend outlined above. (Note that the tantalum surface oxidizes during use.) Automatic control of the alloying cycle and a tighter alloying chamber should eliminate observed deviations to a large extent.

2.d <u>Influence of the GaAs material properties on the tunnel junction characteristics.</u> The results for the tunnel characteristics obtained from diodes made with a short alloying cycle on the (polycrystalline) GaAs from Merck is shown in Figs. 3 and 4. Tunnel junctions on the boat-grown material, (Items 2 through 4) exhibit very high excess currents giving rise to a pronounced secondary tunnel peak at the same voltage, 0.45 V, as it was discovered with multiple alloying on 7 - 10 x $10^{-3}\Omega$ cm GaAs from Diotron (Fig. 2c). This secondary tunnel peak is caused by tunneling from or to narrow bands within the band gap (see First Interim Report) which are introduced by a high density of impurities and/or dislocations that have deep lying interband levels. For the pulled materials (Item 5 from Merck), however, no indication of a second tunnel peak could be detected with a quick alloying cycle (Fig. 3c and 4). The valley-point voltage is in the same order as found for short

alloying cycles on the Diotron material, i.e. between 0.4 and 0.6 volts. We conclude, therefore, that the boat-grown material from Merck contains a high density of imperfections that cause deep lying energy levels.

The peak current density for GaAs with 6×10^{18} cm^{-3} hole density (Item 2 from Merck) is < 0.04 A/cm^2 (no indication of a direct tunnel peak is seen in Fig. 3a), for GaAs with 1.2×10^{19} cm^{-3} hole density (Item 4 from Merck) about 0.2 A/cm^2 and increases for GaAs with 2.9×10^{19} cm^{-3} (Item 5 from Merck) to 3.2 A/cm^2. The peak-to-valley ratio in the last case is 2 to 4. It is interesting to note that Item 5 from Merck is designated with the same resistivity as Item II from Diotron, namely $3.5 \times 10^{-3}\Omega$ cm (see Table 1). The peak current density found at short alloying cycles with Item II from Diotron, however, is higher by a factor of nearly 100, ranging from 250 to 310 A/cm^2 at a peak to valley ratio usually between 10 and 20 (Fig. 5a: The peak-point voltage is shifted to higher value because of the influence of the series resistance R_s)[9]. The Diotron GaAs, therefore, should have a much lower hole mobility and hence higher hole density which we want to verify by Hall measurements in our laboratory, as already mentioned.

2.e Reduction of Junction Area by Etching. The reduction of the junction area after alloying involves two steps:

1. The tin dot size is reduced by etching in hot HCL to a diameter of about 2 mil which needs etching times in the order of 5 to 10 minutes. In this etch, GaAs is only barely attacked. Only a small decrease in junction current was revealed for very shallow regrowth in case of rapid alloying cycles indicating a slight etch of GaAs (e.g. reduction of peak current after 15 minute etch in HCL: 30% for dull GaAs surface and 10% for bright surface). The reduction of the tin dot size during etching was observed under a microscope and the sample removed from the etch when the desired dot size was reached. In most cases the reduction speed was not uniform. For reducing several tin dots on the same GaAs die to about equal size, masking of those dots that have already reached their desired size with black wax would be necessary.

2. After the HCL etch, the GaAs die is placed in a $NaOH\text{-}H_2O_2$-etch (composition as given in Section 2.a). In this etch Sn is not dissolved and acts as a mask. After the bare regrowth area is etched off (which takes about 1/2 to 2 minutes depending on the regrowth depth) the junction area is further

reduced by under-cutting the tin dot. An etch rate (horizontal) for the reduction of junction area was established by measuring the reduction of the tunnel peak current and assuming a circular junction area, calculated from the known peak current density that was considered to be uniform. It was fairly constant for all junctions investigated with various peak-current densities and different sizes when using a freshly mixed etch; its value, expressed in the decrease of junction diameter, is 8 - 10 μ/min. The etch rate was reduced to 1/2 of this value by diluting the etch with 5 parts of deionized H_2O. The etch rate decreased with the aging of the etch, 4 μ/min. being the smallest value measured after several hours from the time of mixing. No measurable difference, however, was found for a bright or dull GaAs surface, despite the fact that the vertical etch rate for the dull surface is much faster.

By this technique junction areas as low as 5×10^{-7} cm^2 can be achieved (diameter = 8 μ). Contact to these diodes was made by a pressure probe attached to a micro-manipulator. In some cases the tin dot broke off because of too high pressure, but without destroying the tunnel junction itself. Using a flat probe, contact to the tiny mesa still could be made and no alteration of the dc characteristic was found. In order to prevent the detachment of the tin dot some diodes were covered with black wax from which only the top portion of the tin dot emerged for contact purpose. The presence of the black wax did not introduce any deterioration for the dc characteristic at room temperature. It is hoped that instead of black wax some kind of epoxy can be used to give good mechanical strength to the extremely small diodes for higher temperatures as well.

2.f Selection of GaAs material suitable for the fabrication of microwatt tunnel diodes. Tunnel diodes for switching application dissipating only about 1 μW supply power must have peak currents of less than 10 μA. With junction areas in the order of 5×10^{-7} cm^2 which can be achieved by the above described etching technique a peak current density of about 10 A/cm^2 is necessary. To use a smaller current density is not advisable because it would unnecessarily reduce the switching speed of the device (see Section 3.a.2).

With the Merck GaAs with hole density 2.9×10^{19} cm^{-3}, a peak-current density of only 3 A/cm^2 and peak-to-valley ratios of < 5 were obtained with a fast alloying cycle. About 10 A/cm^2 peak-current density was obtained, however, for the $7 - 10 \times 10^{-3}$ Ω cm GaAs from Diotron at a peak-to-valley ratio of 5 to 7 using a fast alloying cycle (Fig. 1). (Note: It must be concluded

that the hole density is $>3 \times 10^{19}$ cm^{-3} in this material.) But 10 A/cm^2 peak-current density could also be achieved by performing a relatively long alloying cycle with the 3 - 4 x $10^{-3}\Omega$ cm GaAs from Diotron for which the peak current density obtained with a fast alloying cycle was 250-310 A/cm^2 (Fig. 5). The peak-to-valley ratio did not decrease essentially in this case and was measured to about 10. Long alloying cycles on relatively high doped GaAs, therefore, appears to be the best approach for the fabrication of microwatt tunnel diodes. A detailed study of the dc characteristics of microwatt tunnel diodes exhibiting about 10 A/cm^2 peak current, as was achieved by the two different procedures described above, was performed and will be discussed in the next section.

3. Electrical Characteristics of Microwatt Tunnel Diodes

3.a Experimental results. So far only dc measurements on the microwatt tunnel diodes at room temperature have been performed.

3.a.1 Current voltage characteristics

Figs. 6 through 9 show examples for the dc current voltage characteristic of four different diodes. Numbers 1-13 (Figs. 6 and 7) are made on 7 - 10 x $10^{-3}\Omega$ cm, numbers 1b-b (Figs. 8 and 9) on 3 - 4 x $10^{-3}\Omega$ cm GaAs from Diotron, with short and long alloying cycles respectively. For every characteristic a load line using the tunnel diode as a bi-stable switch is drawn, where the low-voltage stable point (a) was set at 80% peak current and the high-voltage stable point (b) at 20% of the peak current above the valley current. The power dissipation P is indicated for each operating point, as is the value of the load resistor R_L and the supply voltage E_B for every particular load line. A close comparison of the two different types of characteristics as obtained by the short (die #1-13, Curve 1) and long alloying cycle (die #1b-b, Curve 2) is made in Fig. 10, where the peak current is normalized to 10 μA (the shapes of the characteristics within each group are essentially identical if normalized). The shift of the peak and valley points to lower voltages for Curve 2 introduces only a slight decrease in the negative resistance value R, but an essential decrease of the load resistor R_L, the supply voltage E_B and the power dissipation P at the operating points.

Important quantities of the current-voltage characteristic are listed in Table 2 for 5 microwatt tunnel diodes.

TABLE 2. Current-Voltage Characteristic

Diode	$I_p/\mu A$	V_p/V	$R_T/k\Omega$ Calc.	$R_T/k\Omega$ Meas. dc	$R_T/k\Omega$ Meas. Bridge	$(\xi_c+\xi_v)/V$	$I_v/\mu A$	$V_v/\mu A$	$\frac{I_p}{I_v}$	$\lvert R\rvert /k\Omega$	V_f/V
1-13a	19.5	0.17	3.9	3.7	3.0	0.51	2.6	0.60	7.5	9.0	0.88
1-13e	7.6	0.16	9.4	8.3	---	0.48	1.1	0.58	6.9	26	0.86
1b-bb	2.65	0.065	11	10	9.0	0.19	0.255	0.325	10.4	56	0.70
1b-bc	14.5	0.065	2.0	1.9	1.85	0.19	0.14	0.31	10.4	9.8	0.70
1b-bd	3.3	0.06	8.1	---	---	0.18	0.30	0.32	11	---	---

I_p = peak current

V_p = peak-point voltage

R_T = differential resistance of current-voltage characteristic at zero point as calculated, and measured from the dc current-voltage characteristic and from admittance measurements with a transformer bridge.

ξ_c, ξ_v = penetration of the Fermi level into the conduction band and valence band respectively.

I_v = valley current

V_v = valley-point voltage

R = negative resistance of tunnel diode

V_f = forward voltage, when dc characteristic reaches I_p a second time.

3.a.2 Junction capacitance

Fig. 11 shows the junction capacitance vs. voltage for a diode from each group. The qualitative shape of the characteristics is typical for each group. As the junction area is nearly the same for both diodes, the curves may be considered as normalized to the junction area. Both curves have in common a sharp increase of junction capacitance at low voltages, which is theoretically not understood.

Capacitance measurements were made with a transformer bridge (Boonton 74C) in the direct method eliminating any stray capacitance to ground.[7] The ac voltage of the bridge signal was about 10 mV at 100 kc frequency. The part of the stray capacitance between leads and probes that could not be shielded was balanced out by the bridge before pressure contact to the tin dot was made. The capacitance measuring circuit is seen in Fig. 12. The loop 1-3-2 provides the dc voltage supply, as well as voltage and current measurements for the terminals 1 and 2 of the tunnel diode, with a load resistor $R_L < |R|$ to ensure stability also in the negative resistance region. The ground at point 3 eliminates any influence of the loop 1-3-2 on the direct measurement of ac admittance between points 1 and 2. The 0.1 μF capacitors shield the dc voltage supply from the bridge, but practically can be considered as a short circuit for the bridge signal.

Table 3 lists different quantities of 5 microwatt tunnel diodes that are related to the capacitance measurements. The switching time for the tunnel diode used as a bi-stable switch is calculated from the following approximate formula[8] valid with negligible series inductance $\omega L_s/|R| \ll 1$ (because of the large values of $|R|$ this condition can easily be fulfilled for microwatt tunnel diodes):

$$T_s = \frac{C_j}{I_p} \frac{V_f - V_p}{1 - I_v/I_p} \qquad (3)$$

using for the junction capacitance C_j the valley-point capacitance C_v. The main factor influencing T_s is the capacitance-to-peak-current ratio C_v/I_p, which should be as low as possible. Therefore, the highest peak-current density I_p that is still suitable for fabricating microwatt tunnel diodes has to be selected as already stated. This optimum value is $I_p = 10$ A/cm^2 yielding theoretical switching times in the order of 0.1 μ sec. The capacitance per unit area (at valley voltage) in this case is about 1 μF/cm^2. This is the

TABLE 3. Capacitance and Switching Time

Diode	C_v/pF	V_v/V	$\frac{C_v}{I_p}$ / pF/mA	T_s/μsec	J_p/A cm^2	$A_j/10^{-6}$cm^2	$\frac{C_v}{A_j}$ /μF cm^{-2}	$W_1/\text{Å}V^{-\frac{1}{2}}$	V_D/V
1-13a	2.1	0.60	108	0.08	8.8	2.2	1.0	150	1.03
1-13e	1.1	0.58	145	0.12	(~9)	(~0.9)	(~1.2)	130	0.93
1b-bb	0.16	0.325	60	0.04	12	0.22	0.7	130	0.85
1b-bc	2.7	0.31	186	0.12	7	2.0	1.3	90	0.91
1b-bd	0.46	0.32	139	0.10	(~10)	(~0.3)	(~1.5)	--	--

C_v = junction capacitance at valley point

V_v = valley-point voltage

I_p = peak current

T_s = switching time (theoretical)

J_p = peak-current density

A_j = junction area

W_1 = width constant

V_D = diffusion voltage

same value as measured for the microwatt tunnel rectifiers (backward diodes) on silicon (see Second Interim Report).

3.b Theoretical interpretation. The terminology used in the following theoretical analysis was also used in the theoretical part of the First Interim Report to which the reader is referred.

An analysis of the two different shapes of the dc current-voltage characteristic as obtained by the short and long alloying cycle for our microwatt tunnel diodes is made in Fig. 13. Both characteristics, normalized to the same peak current, are drawn in a semilogarithmic scale. Because of the nearly equal peak-current density for both units, the normalization can also be considered as made to the same junction area.

3.b.1 Band-to-band tunnel peak

To explain the shift of the current peak to lower voltage for Curve 2 we use the theoretical analysis of the overlap-integral (Esaki-integral) D(V) made by Winstel.[9] One finds for the peak-point voltage (at temperatures $T > 300^{\circ}K$ in case of GaAs):

$$V_p = \frac{\xi_c + \xi_v}{3} \tag{4}$$

ξ_c and ξ_v are the penetrations of the Fermi level into the conduction and valence band respectively. For $q\xi_c \gg kT$ one has:

$$\xi_c = \frac{1}{2q}\left(\frac{3}{8\pi}\right)^{2/3} \frac{h^2}{m_c} n^{2/3} = 3.7 \times 10^{-15} \left(\frac{m_o}{m_c}\right) n^{2/3} \text{ V cm}^2 \tag{5}$$

where h is Planck's constant; an analogous expression holds for ξ_v. The sum of the Fermi penetrations calculated from (4) is about 0.5 V for Curve 1 and 0.2 V for Curve 2 of Fig. 13 (Table 3). Inspecting Eq. (5), this means either lower carrier concentrations or higher density-of-state masses for the long alloying cycle. The first possibility can be explained by impurity diffusion during the long heating period, introducing a rather low effective doping for tunneling. The second one, however, seems to be rather unlikely.

A theoretical relationship exists for the differential resistance at the zero point of the current-voltage characteristic R_T and the peak point coordinates.[9] Neglecting any series resistance R_s to the tunnel junction,

i.e. $R_s \ll R_T$ (certainly fulfilled for microwatt tunnel diodes) one has:

$$R_T = \frac{9}{4} \frac{I_p}{V_p} \tag{6}$$

Calculated R_T values agree well with those measured from the dc characteristic and also with those obtained from admittance measurements using a transformer bridge (Table 2).

3.b.2 Excess current

For each curve the increasing exponential excess current at voltages $> V_v$ is extrapolated to smaller voltages and subtracted from the measured curve. This yields a decreasing exponential excess current branch[9] (termed "valley excess current" by Meyerhofer, et al.)[10] which proceeds smoothly into the band-to-band tunnel peak at lower voltages. We describe, therefore, according to Winstel[9] the dc characteristic around the valley point by the sum of a rising and falling excess current branch:

$$I_{ex} = B_\sigma \exp(\sigma V) + B'_\sigma \exp(-\sigma' V) \tag{7}$$

The parameters of this relationship fitting Curves 1 and 2 of Fig. 13 are given in Table 4. From the theoretical model for the rising exponential excess current follows (First Interim Report, Eq. (9)):

$$\sigma = \alpha' W_1 (m^*)^{\frac{1}{2}} \tag{8}$$

With

$$W_1 = \left(\frac{2\mathcal{E}}{q} \frac{1}{n^*}\right)^{\frac{1}{2}} \tag{9}$$

we get[9]:

$$\sigma = 3.0 \times 10^{10} \left(\frac{m^*}{m_o} \frac{\varkappa}{n^*}\right)^{\frac{1}{2}} V^{-1} cm^{-3/2} \tag{10}$$

($\varkappa$ = dielectric constant = 11.1 for GaAs.)

From Eq. (6) and (7), the reduced carrier density n* and the width constant W_1 was calculated (Table 4) assuming the same reduced effective mass as it is given for the band-to-band tunneling $m^* = 0.066\ m_o$ (which, however, is only justified because no better value is known). The found n* values seem to be low in view of the results obtained with Merck GaAs, Item 5, having

TABLE 4. Parameters of Excess Current

Diode	B_σ / I_p	σ / V^{-1}	$B_{\sigma'} / I_p$	σ' / V^{-1}	$n^* / 10^{19}$ cm^{-3} (from σ)	$W_1 / \mathring{A}\ V^{-\frac{1}{2}}$ (from n^*)
1-13e	8.7×10^{-5}	10.8	1.8	5.2	0.56	150
1b-bb	7.0×10^{-3}	7.1	9.0	18.6	1.3	98

a hole density of 2.9×10^{19} cm^{-3} and yielding a peak current density of only 3.2 A/cm^2 in a short alloying cycle. But the calculated width constants W_1 compare favorably with the values found from capacitance measurements (discussed in section 3.b.4) which are given in Table 3. This situation could be explained by assuming a relatively low electron concentration in the n regrowth (doping levels for tin in GaAs are not known) leading to $n \ll p$ and therefore $n^* \approx n$ (Note: n type GaAs gets degenerate already at $n = 3.8 \times 10^{17}$ cm^{-3}, p type GaAs, however only at $p = 1.2 \times 10^{19}$). With this interpretation the tin doping level is higher for long alloying cycles. A discrepancy arises if one compares the above results with those obtained from the analysis of the band-to-band tunnel peak, where it was found that the longer alloying cycle produces lower carrier densities near the junction: Calculating the Fermi penetration ξ_c with the assumption $n \approx n^*$ from Eq. (5) one obtains 0.17 V for Curve 1 and 0.28 V for Curve 2 of Fig. 13. In the latter case the value is even higher than the sum $(\xi_c + \xi_v)$ as obtained from V_p. This can be explained only by the fact that for the long alloying cycle the impurity diffusion proceeds so far that the step junction approximation underlying all tunnel junction calculations is not valid anymore. For the first case, however, ξ_v can be calculated from Eq. (4) yielding $\xi_v = 0.31$ V. Using the equation for ξ_v that is the analogue to Eq. (5) one obtains a hole concentration of $p = 4.6 \times 10^{20}$ cm^{-3} justifying the assumption $p \gg n$ (on the other hand this p value seems to be unrealistically high).

In another theoretical relationship between the excess current and the band-to-band tunnel peak good agreement is obtained. One finds for the peak current density[9] (at temperatures $T > 300^\circ$K for GaAs):

$$J_p = \frac{B}{kT} \left(\frac{\xi_c + \xi_v}{3} \right)^3 P_p \qquad (11)$$

where B is a constant and the tunnel probability P_p is:

$$P_p = \exp \left[-\alpha (m^*)^{\frac{1}{2}} W_1 E_G \left(1 - \frac{\xi_c + \xi_v - V_p}{2 E_G} \right) \right] \qquad (12)$$

(Note: In the First Interim Report $(\xi_c + \xi_v - V_p)/(2E_G)$ was neglected compared to 1 yielding a voltage-independent P).

Winstel[9] finds $\alpha = \frac{1}{2} \alpha'$ or with Eq. (8):

$$\frac{\sigma}{2} = \alpha (m^*)^{\frac{1}{2}} W_1 \tag{13}$$

Using in addition Eq. (4) one eventually arrives at:

$$J_p = \frac{B}{kT} \; V_p^3 \exp \left[- \frac{\sigma}{2} (E_G - V_p) \right] \tag{14}$$

Assuming a band gap in degenerate GaAs of $E_G = 1.29$ V which is about 6% lower than for intrinsic material, as was found by Winstel[9] for Si and Ge, one gets for the two curves of Fig. 13:

Curve 1: $J_p = \frac{B}{kT} \times 9 \times 10^{-6}$

Curve 2: $J_p = \frac{B}{kT} \times 3.5 \times 10^{-6}$

or, in other words, the same order of magnitude for the peak current density for the two cases, as was actually measured.

The constant B_σ of Eq. (7) is given by[9]:

$$B_\sigma = A' D' \exp (-\sigma V_D) \tag{15}$$

with the diffusion voltage V_D being:

$$V_D = E_G + \xi_c + \xi_v = E_G + 3V_p \tag{16}$$

For the two cases of Fig. 13, we obtain for the ratio of the density factors D' which is directly related to the ratio of the interband-level densities because of the almost equal peak current density:

$$\frac{D_1'}{D_2'} \; \frac{I_{p2}}{I_{p1}} = \frac{B_{\sigma 1}}{B_{\sigma 2}} \exp \left[3 (\sigma_1 V_{p1} - \sigma_2 V_{p2}) + E_G (\sigma_1 - \sigma_2) \right] \approx 70$$

This means that the interband level density is higher for Curve 1 ($7 - 10 \times 10^{-3}$ Ωcm GaAs and short alloy cycle) despite the smaller values of the rising excess current branch.

Interesting is an indication of a hump above the rising exponential excess current branch of Curve 2 ($3 - 4 \times 10^{-3}$ Ω cm GaAs, long alloying cycle) with maximum near 0.55 V. A similar hump, sometimes more pronounced appearing

as a second current peak, was also found for the lower resistivity GaAs from Diotron (7 - 10 x $10^{-3}\,\Omega$ cm) with the maximum near 0.45 V, when alloying was carried out for a longer period, as already pointed out (Fig. 2). This hump, which is caused by an impurity or defect level banding near the band gap center is therefore a common result of long alloying. A hump structure introduced by Sn alloying was also reported by Hamaker and Quinn[11] who, however, found two secondary tunnel peaks, the second one lying near 0.3 V.

For the falling branch of the excess current (valley excess current) the σ' value is much higher for Curve 2 of Fig. 13. As well as the low V_p value this again points towards a lower carrier density, for the long alloying cycle, with only a narrow banding of impurity levels near the band edges and, therefore, a rapid decrease in tunnel current with voltage.

3.b.3 Thermal Diffusion Current

From extrapolating the rising exponential excess current branch to higher voltages for Curve 1 of Fig. 13 the magnitude of the thermal diffusion current was obtained at 1 V forward bias:

$$J_{th}(1\ V) = 1.7\ J_p = 15\ A/cm^2$$

Theoretically, for the thermal diffusion current across a degenerate p-n junction the following expression is derived[9]:

$$J_{th} = B_{th}\left[\frac{m_c}{m_o}\exp\left(-q\,\frac{E_G+\zeta_v}{kT}\right) + \frac{m_v}{m_o}\exp\left(-q\,\frac{E_G+\zeta_c}{kT}\right)\right]\exp\frac{qV}{kT} \qquad (17)$$

with

$$B_{th} = 4\eta\, q m_o (kT)^2/h^2 = 1.08 \times 10^7\ (T/300^\circ K)^2\ A/cm^{-2} \qquad (18)$$

For GaAs $m_c \approx 0.1\ m_v$. If we assume $\zeta_c < \zeta_v$ the electron contribution to the thermal current is smaller than the hole contribution by a factor of < 0.1 and may, therefore, be neglected. The above assumption is supported by the evaluation of the excess-current parameter σ, where it was found $\zeta_c = 0.17$ V and $\zeta_v = 0.31$ V for Curve 1 of Fig. 13. Calculating then $(E_G + \zeta_c)$ from Eq. (17) with the thermal-current value found for 1 V at room temperature we get:

$$E_G + \zeta_c = 1.34\ V$$

or with

$$\zeta_c = 0.17 \text{ V}$$

$$E_G = 1.17 \text{ V} .$$

This E_G value is about 15% lower than measured for intrinsic GaAs ($E_G = 1.38$ V) which is twice as large a decrease in the band gap as reported by Winstel[9] for Si and Ge.

A similar evaluation cannot be performed for Curve 2 of Fig. 13, because the characteristic was not measured into the thermal region. This is so because we found out that the valley current had increased after applying higher forward voltages to the diode. This degradation is a well known effect for GaAs tunnel diodes and described by Pikor, et al.[12] and by Hickey[13].

3.b.4 Junction capacitance

The strange sharp increase of the junction capacitance at low voltages (Fig. 11) cannot be explained. Above about 0.4 V, however, the capacitance voltage characteristics assume a "normal" behavior, i.e., a relationship approximately $C^{\frac{1}{2}} \sim V$. From this portion of the characteristics the diffusion voltage V_D and width constant W_1 were determined (Fig. 14 and Table 3). The width constants agree fairly well with those obtained from the σ parameter of the excess current (Table 4), but the V_D values appear rather low when compared to the theoretical expected values according to Eq. (16). An explanation of this situation is possible: The rather steep but finite carrier gradients at the depletion layer boundaries suggest a lower diffusion voltage for the junction capacitance than the total diffusion voltage given by (16). Only assuming infinite carrier gradients (abrupt approximation) the total diffusion voltage builds up across the boundaries of the depletion layer.

The main difference between the two curves of Fig. 11 is the sharper decrease of the junction capacitance for decreasing voltages < 0.4 V before the steep rise near 0.1 V in case of Curve 2, not found in Curve 1. This sharper decrease was found even more pronounced with other diodes of the same group. This behavior indicates again deviation from the step junction behavior caused by impurity diffusion during the long alloying cycle.

I.4 Conclusions

Using the same technology that proved suitable for the fabrication of microwatt tunnel rectifiers (backward diodes) on Si (i.e. a combination of large area alloying and etching), it was possible to build microwatt tunnel diodes on GaAs. The peak current is typically < 10 μA, the peak-to-valley ratio 6 to 10, and the theoretical switching time 0.1 μsec at a junction capacitance of ~ 0.5 pF.

From a detailed study of material and technology an optimum peak current density of about 10 A/cm^2 was selected for the microwatt tunnel diodes. This current density can be achieved either by alloying Sn to a relatively high-resistivity Zn-doped GaAs in a short temperature cycle or by alloying Sn to low-resistivity Zn-doped GaAs in a long temperature cycle. The latter process yields lower peak and valley-point voltages (thereby decreasing the power dissipation) and, in addition, higher peak-to-valley ratios. An optimum Zn doping level has not been established yet.

Dimension control for the junction area by the employed etching technique is very satisfying down to junction diameters of < 10 μ. (Note: A similar close dimension control should be possible also for the fabrication of silicon microwatt tunnel rectifiers by establishing an appropriate etch rate. Some difficulties may arise in this case because of the non-uniformity of current density found for some of the Si junctions.)

The experimental results were interpreted in terms of current theories of tunneling through pn junction barriers. Agreement with the theory is close in some cases, but not throughout. Larger deviations from the simple step junction assumptions underlying all theoretical approaches may account for the found discrepancies.

SECTION II

II.1 Program for Next Interval

The GaAs microwatt tunnel diode will be developed further and tested with view towards possible use in high speed logic circuits.

This will involve the establishment of an optimum Zn doping level in GaAs for forming Sn alloyed junctions with 10 A/cm^2 peak current density by using an appropriate temperature cycle. Also switching speed will be measured on the actual device and the problem of encapsulation will be considered.

Fabrication of microwatt tunnel diodes in an array of about 6 units on an individual die will be tried.

II.2 Project Performance and Schedule

See the following page.

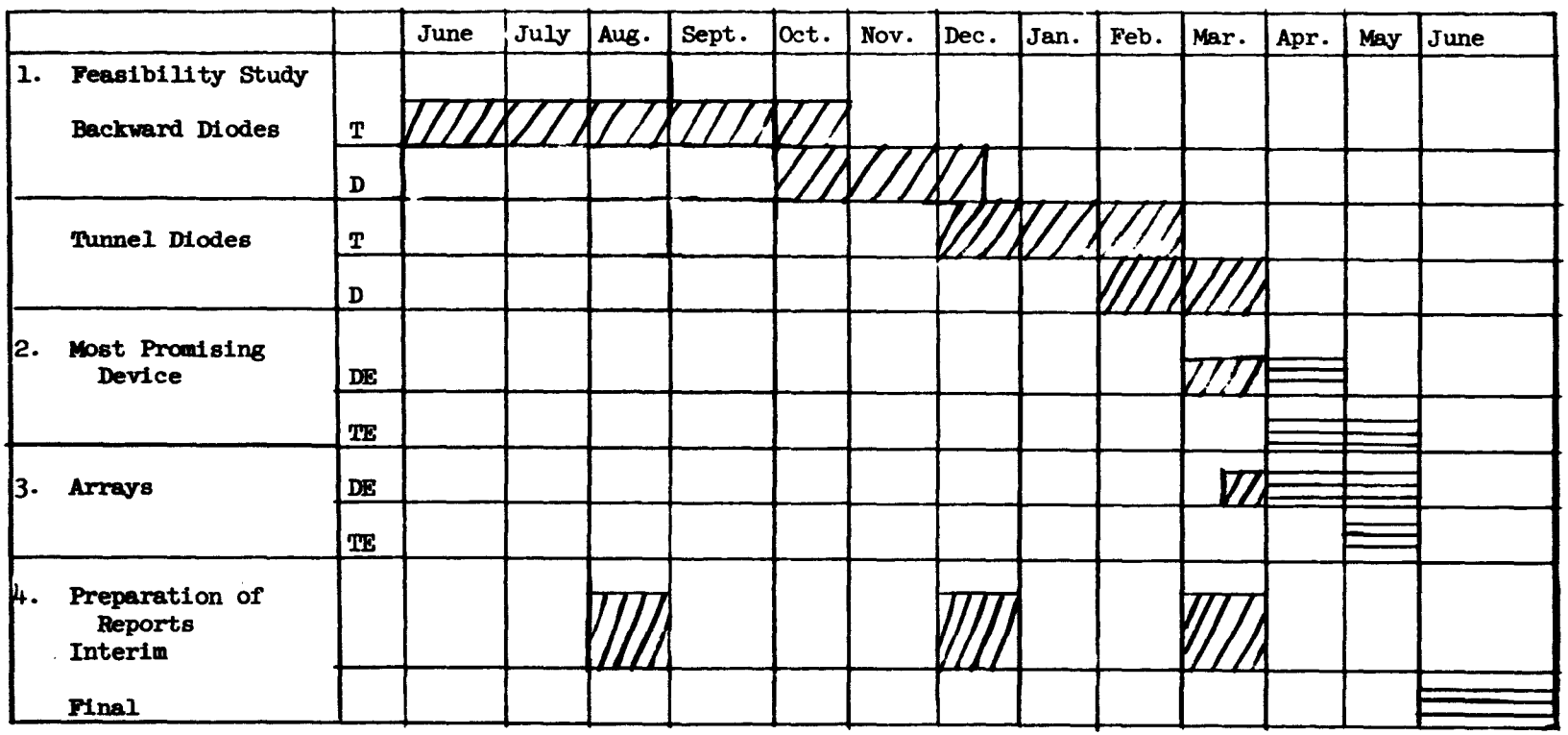
CBS LABORATORIES

Project Performance and Schedule

Contract No. NObsr-87512

March 30, 1963

Period Covered: 12/1/62 to 2/28/63



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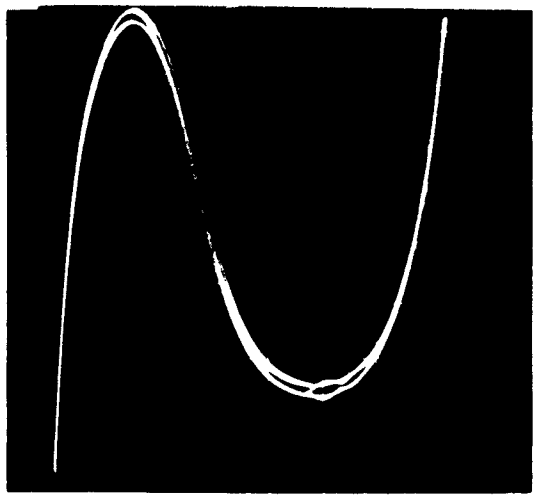
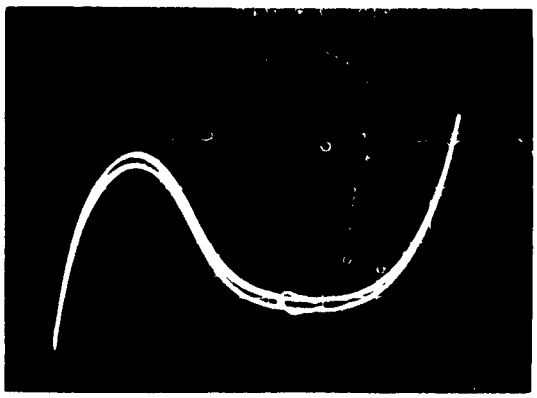
Fund and Fiscal Status Report

Contract Price	$45,847.00
Less Profit	2,986.00
Contract Cost	$42,861.00
Expenditures to 30 March 1963	$38,689.01
Open Commitments with G&A to 30 March 1963	187.62
Total Expenditures and Open Commitments to 30 March 1963	$38,876.63
Approximate Uncommitted Balance as of the End of Current Reporting Period	$ 3,984.37

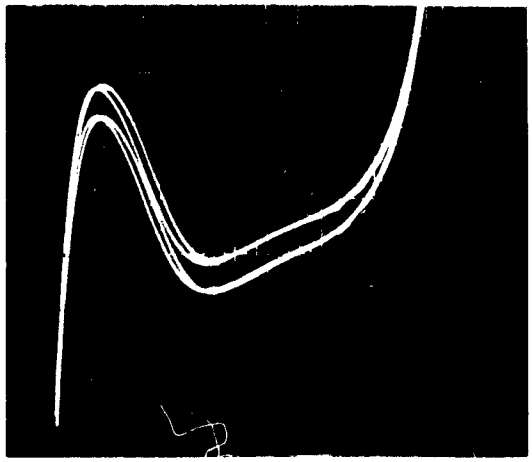


a) Quick alloying to 70 A heater current.
Vertical: 5 μA/div
Horizontal: 0.1 V/div
Peak current density
J_p = 10 A/cm^2



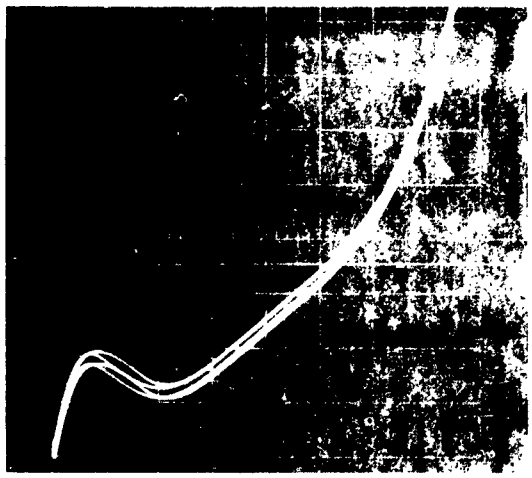
b) Quick alloying to 60 A heater current.
Vertical: 5 μA/div
Horizontal: 0.1 V/div
Peak current density
J_p = 8.8 A/cm^2

Fig. 1 Polycrystalline GaAs from Diotron. ρ = 7-10 x 10^{-3} Ω cm.
Quick alloying cycles.



a) Alloying for 20 sec. at 70 A heater current.
Vertical: 2 μA/div
Horizontal: 0.1 V/div

Peak current density
J_p = 2.6 A/cm^2



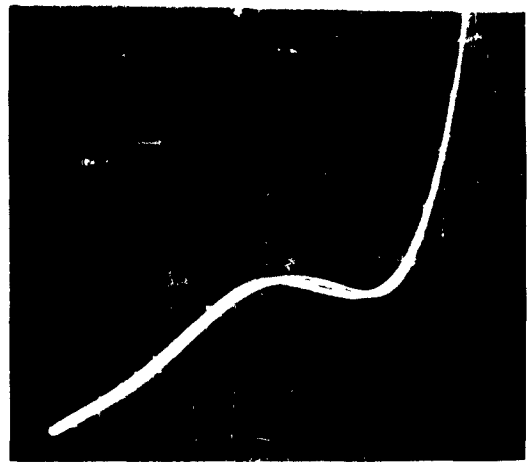
b) 2 alloying cycles: for 3 sec. at 70 A and for 10 sec. at 70 A heater current.
Vertical 5 μA/div
Horizontal: 0.1 V/div

Peak current density
J_p = 1.0 A/cm^2

c) 3 alloying cycles: for 10 sec. at 70 A, for 10 sec. at 70 A, and for 3 sec. at 70 A heater current.
Vertical: 20 μA/div
Horizontal: 0.1 V/div

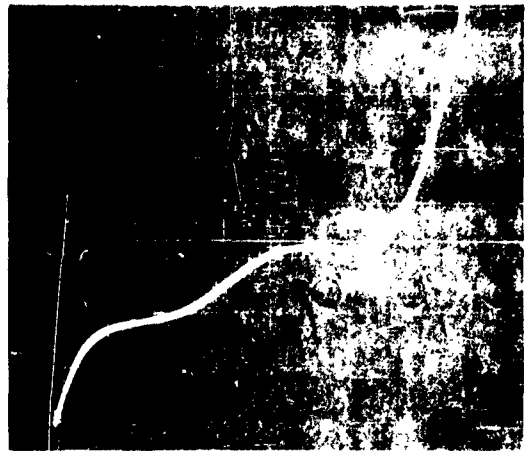
Peak current density (direct tunnel peak): $J_p \approx 0.9$ A/cm^2

Fig. [illegible] Polycrystalline [illegible] Diotron. ρ = 7 - 10 x 10$^{-3}\Omega$ cm.
[illegible]



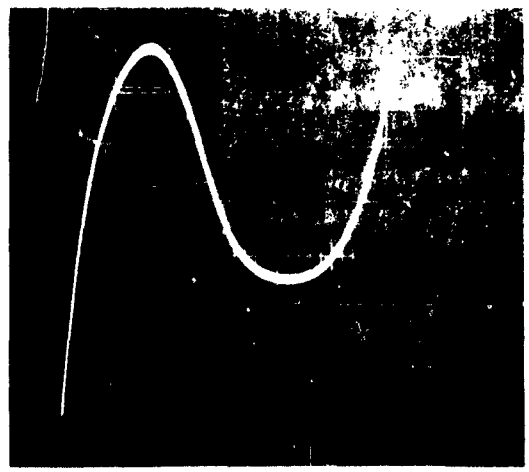
a) Boat grown, $p = 6 \times 10^{18} cm^{-3}$
Vertical: 10 μA/div
Horizontal: 0.1 V/div

No direct tunnel peak. Indirect tunnel peak: current density $J_p' \approx 0.2$ A/cm^2



b) Boat grown, $p = 1.2 \times 10^{19} cm^{-3}$
Vertical: 20 μA/div
Horizontal: 0.1 V/div

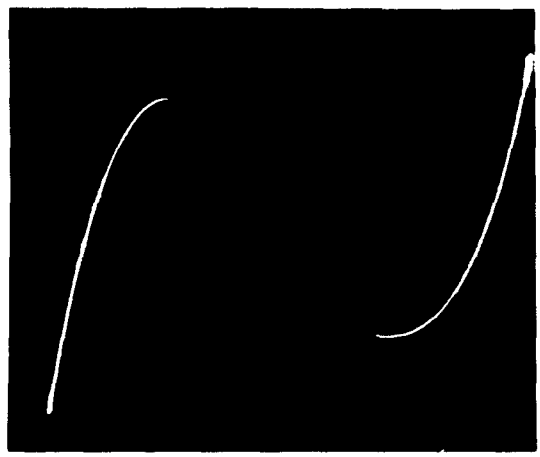
Direct tunnel peak: current density $J_p \approx 0.2$ A/cm^2.
Indirect tunnel peak: current density $J_p' \approx 0.5$ A/cm^2



c) Pulled, $p = 2.9 \times 10^{19} cm^{-3}$
Vertical: 5 μA/div
Horizontal: 0.1 V/div

Peak current density: $J_p = 3.2$ A/cm^2
(No indirect tunnel peak)

Fig. [illegible]. Quick alloying cycles to < 60 A [illegible] ion)



Vertical: 0.1 mA/div

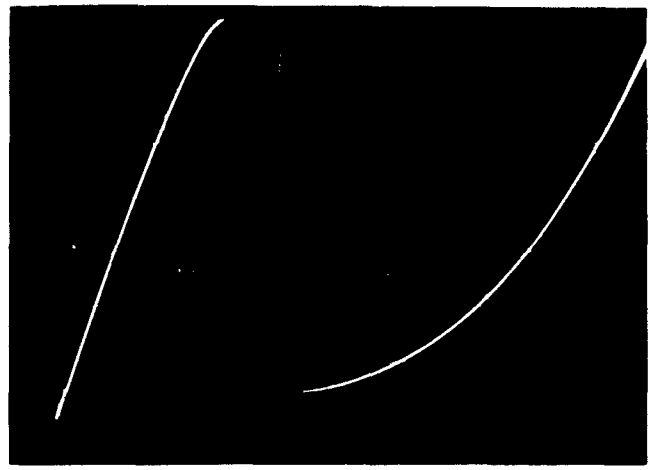
Horizontal: 0.1 V/div

Peak current density

$J_p = 3.2\ A/cm^2$

(Diode on same die as diode of Fig. 1c)

Fig. 4 Polycrystalline GaAs from Merck, pulled, $p = 2.9 \times 10^{19} cm^{-3}$. Quick alloying cycle to 60 A heater current.



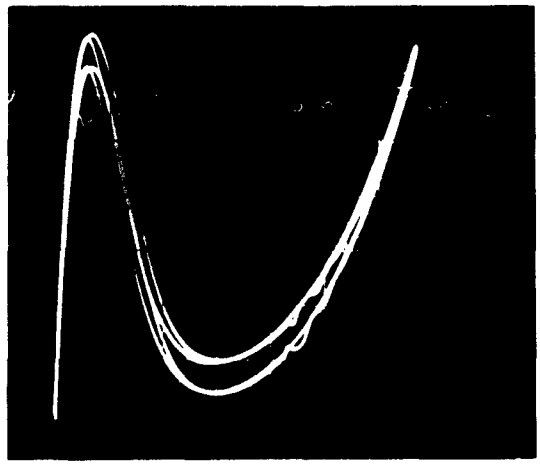
a) Quick alloying cycle

Vertical: 20 mA/div

Horizontal: 0.1 V/div

Peak current density
$J_p \approx 270$ A/cm^2

Series resistance
$R_s = 1.4\,\Omega$



b) 3 alloying cycles:

1. quick to $\sim$60 A heater current
2. 15 sec. at 65-70 A heater current
3. 30 sec. at 75 A heater current

Vertical: 2 μA/div

Horizontal: 0.1 V/div

Peak current density
$J_p = 7.0$ A/cm^2

Fig. 5 Polycrystalline GaAs from Diotron. $\rho = 3 - 4 \times 10^{-3}\,\Omega$ cm.

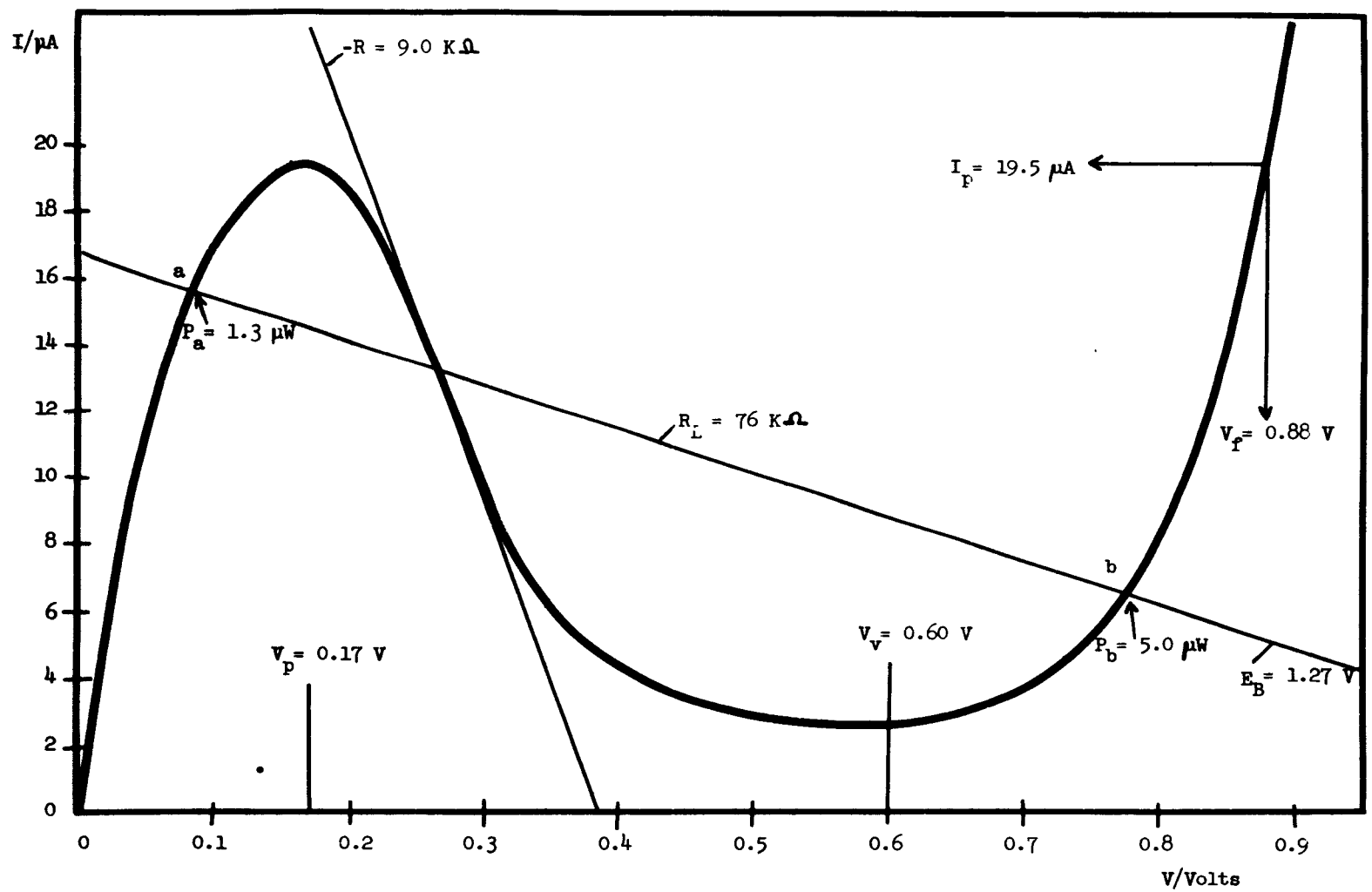


Fig. 6 Diode #1-13a

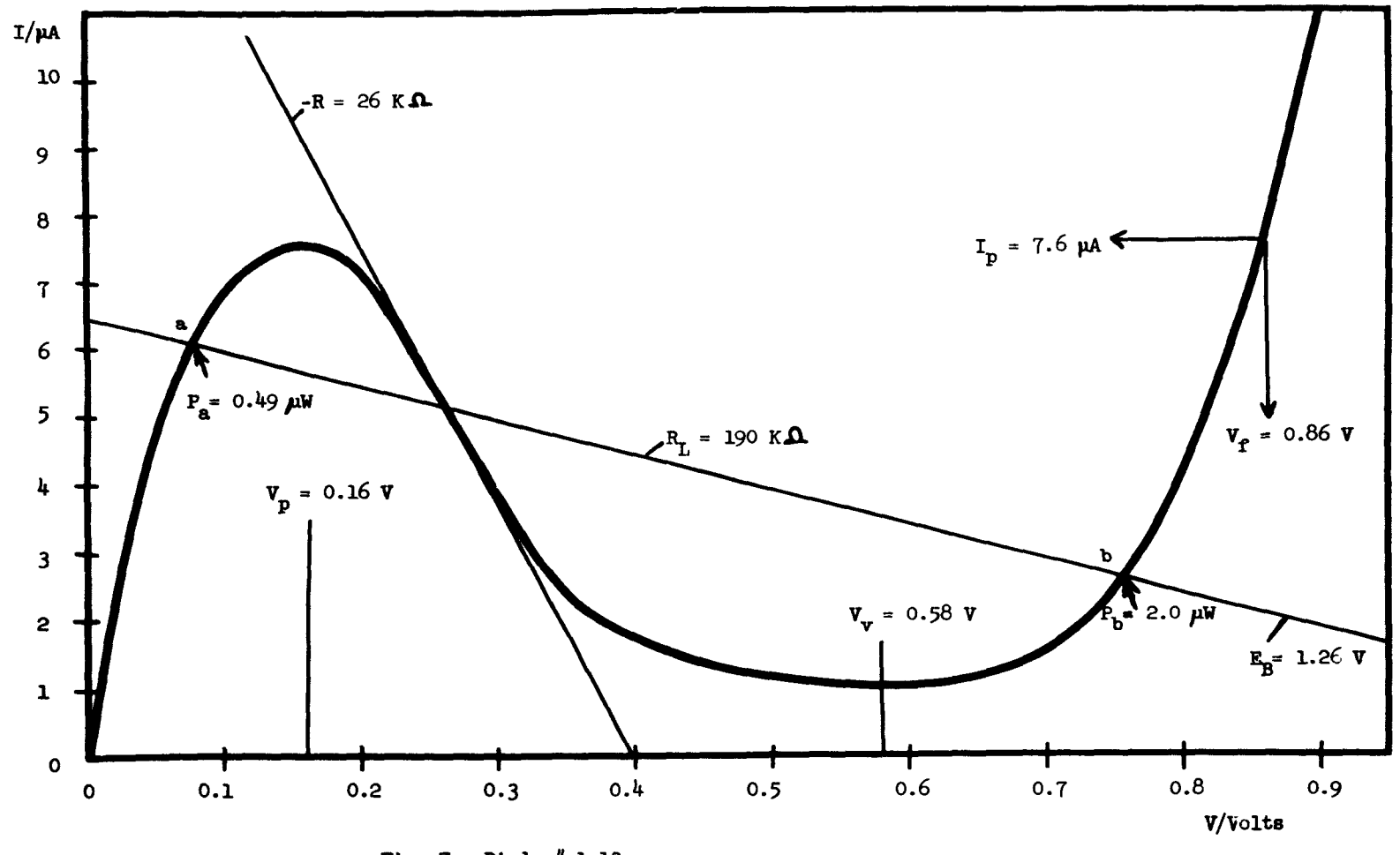


Fig. 7 Diode # 1-13e

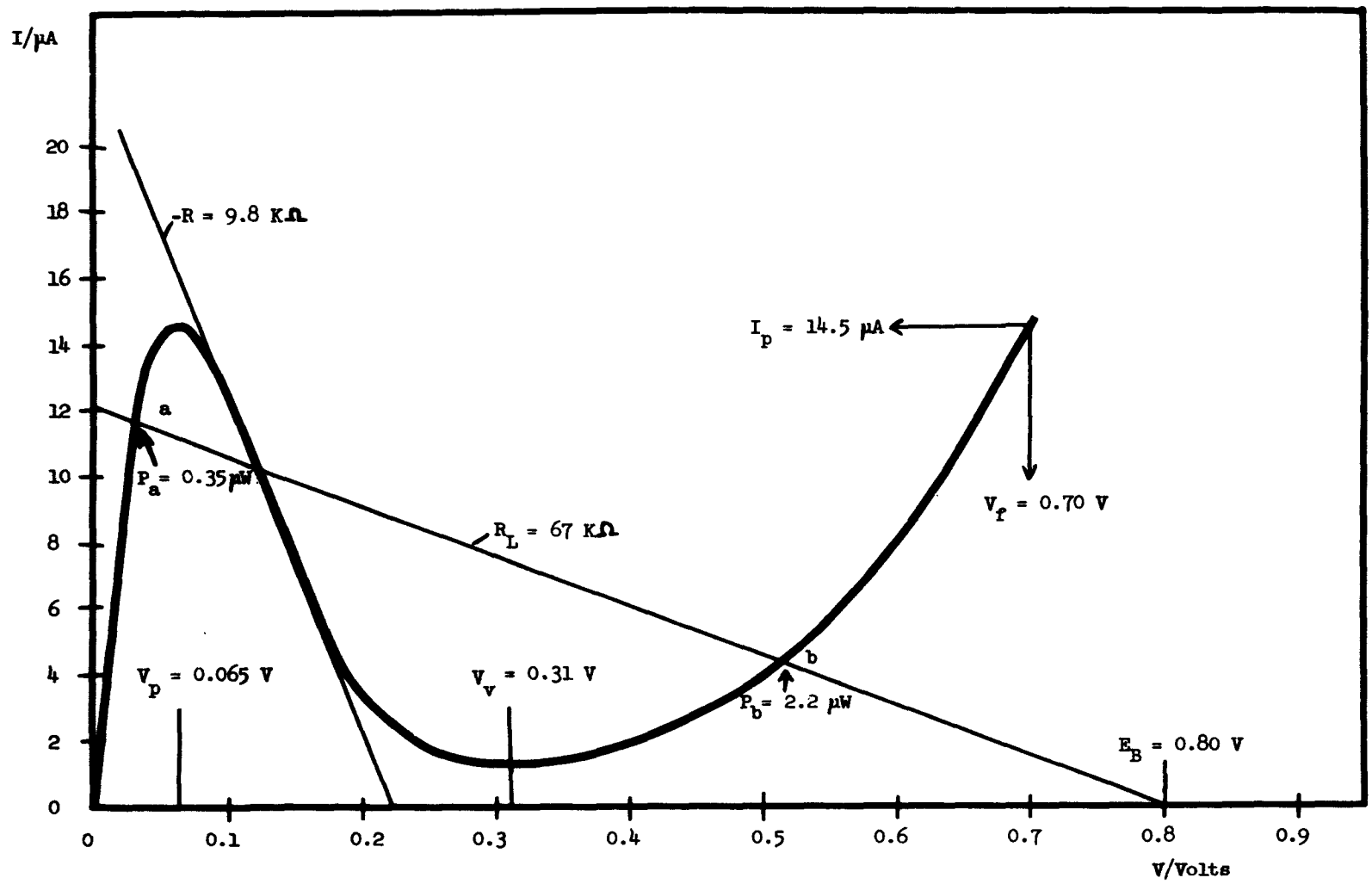


Fig. 8 Diode # 1b-bc

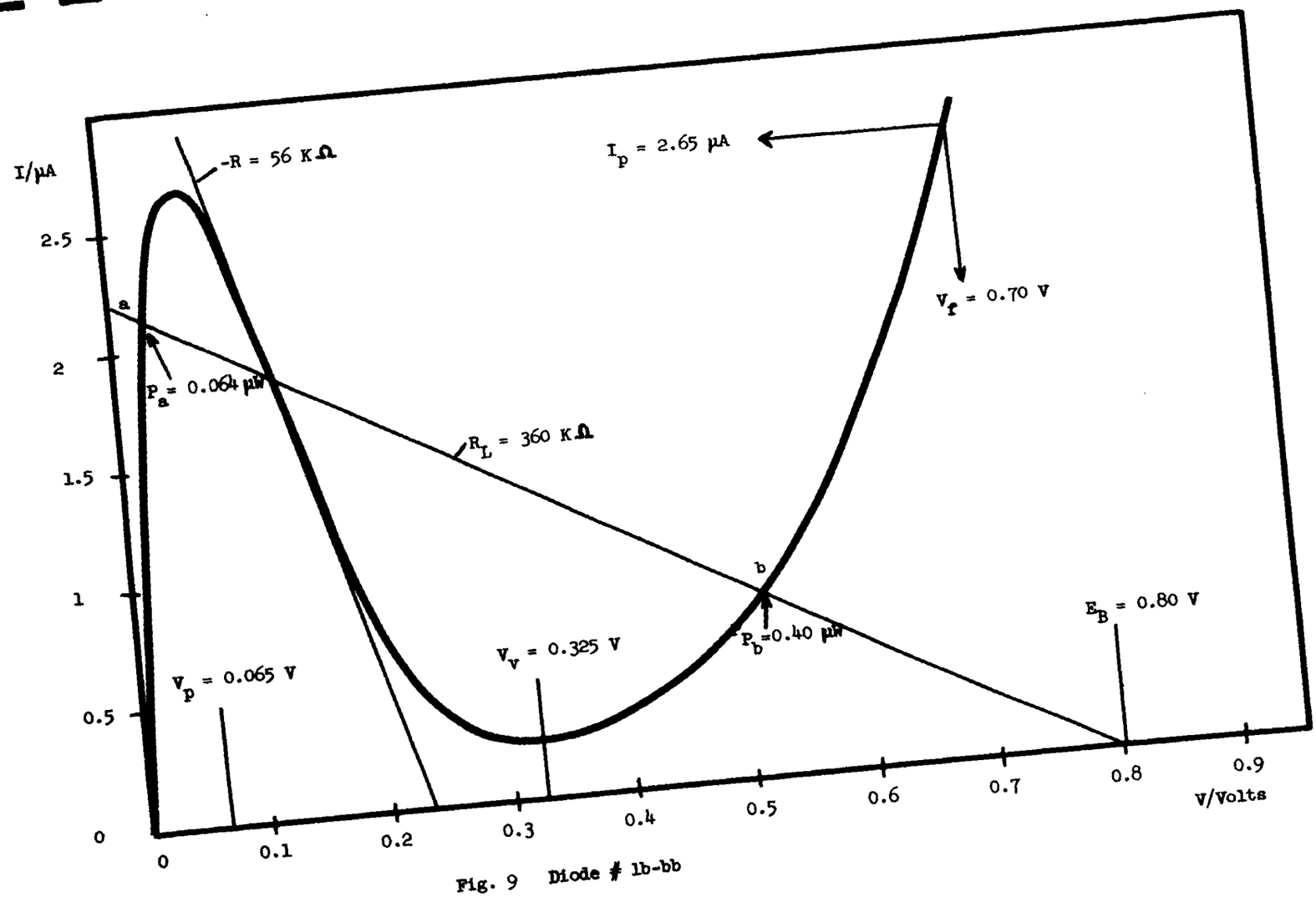


Fig. 9 Diode # 1b-bb

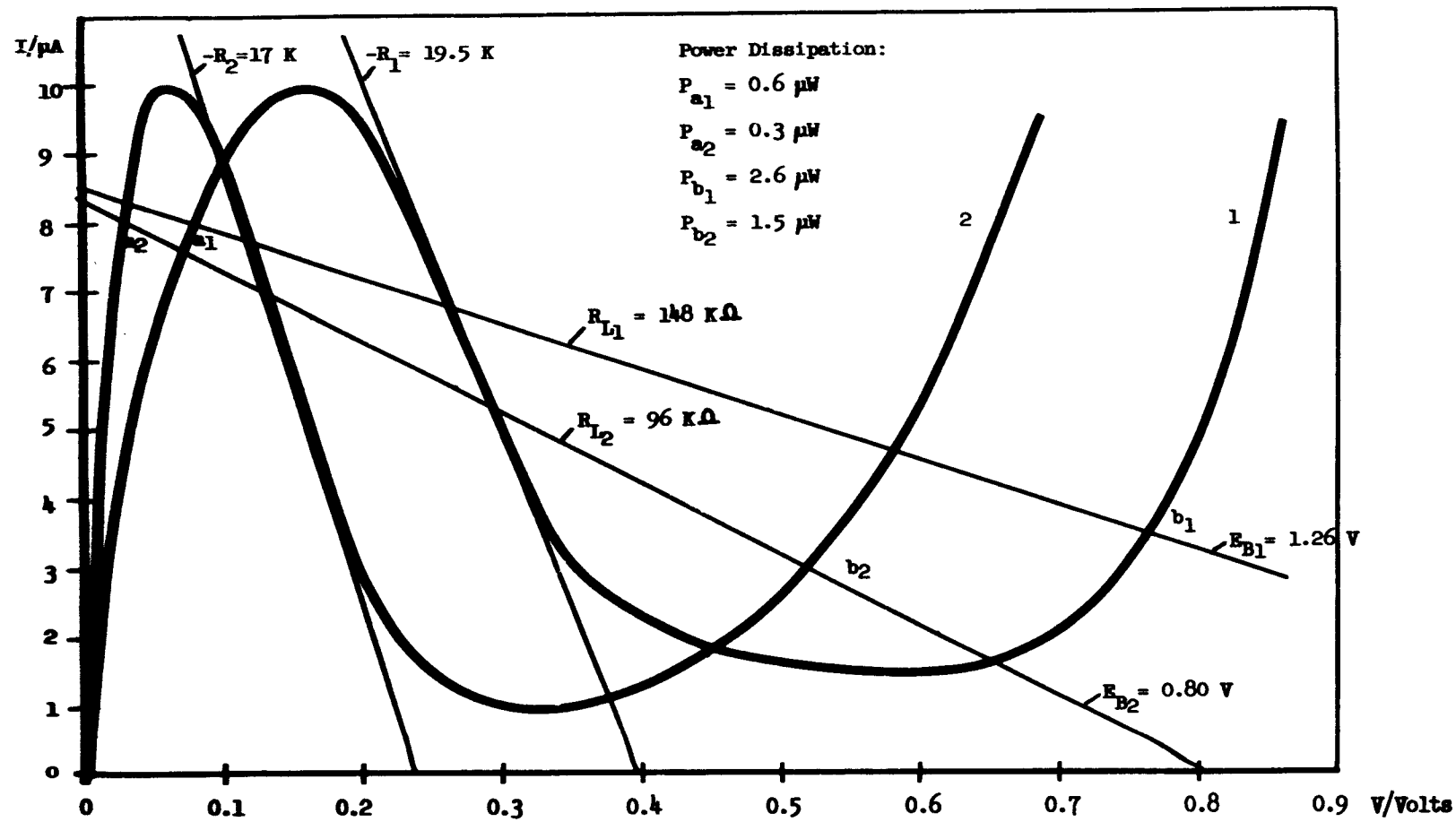


Fig. 10 Comparison of Diode # 1-13e (Curve 1) and #1b-bb (Curve 2) normalized to 10 μA peak current

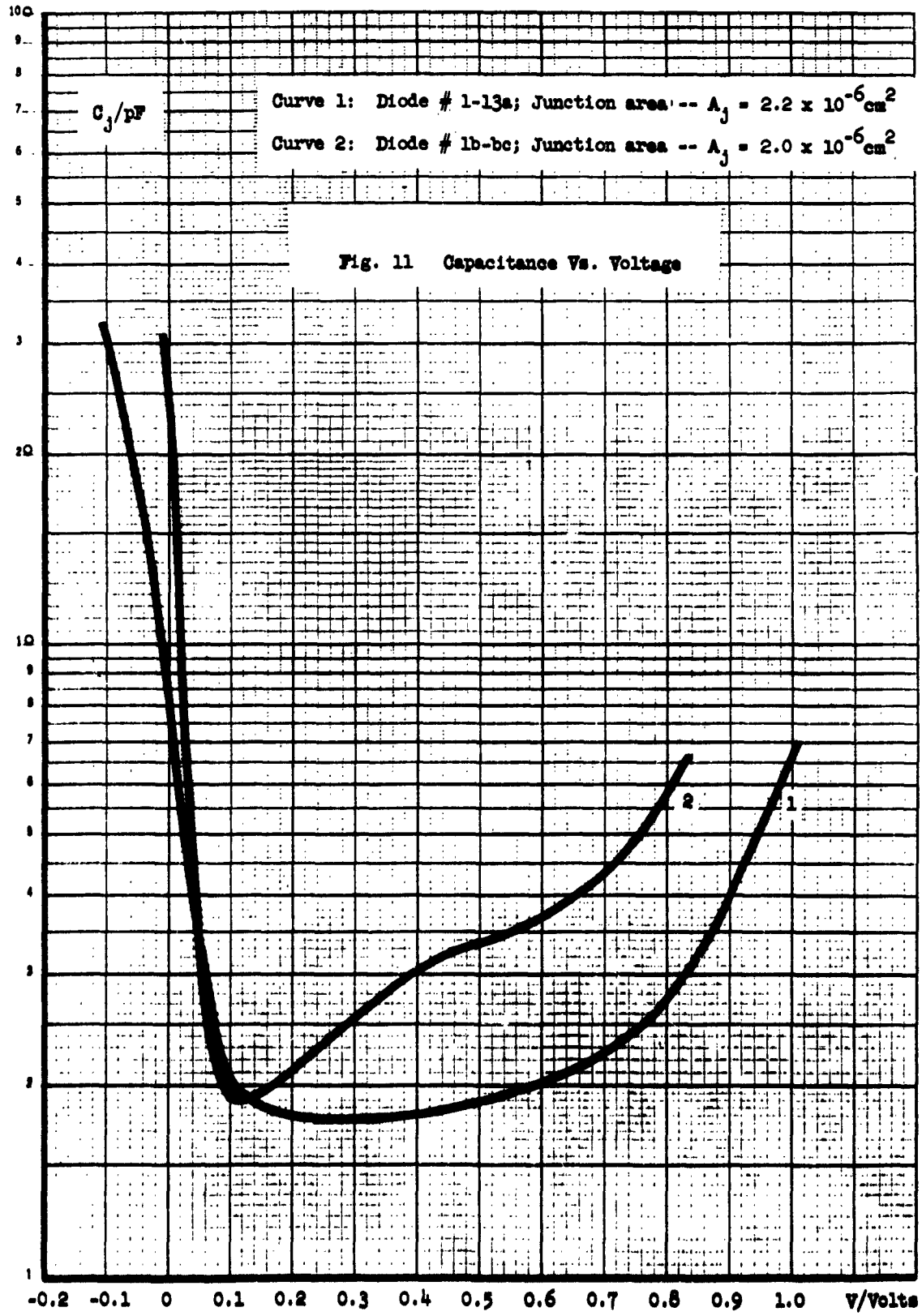


Fig. 11 Capacitance Vs. Voltage

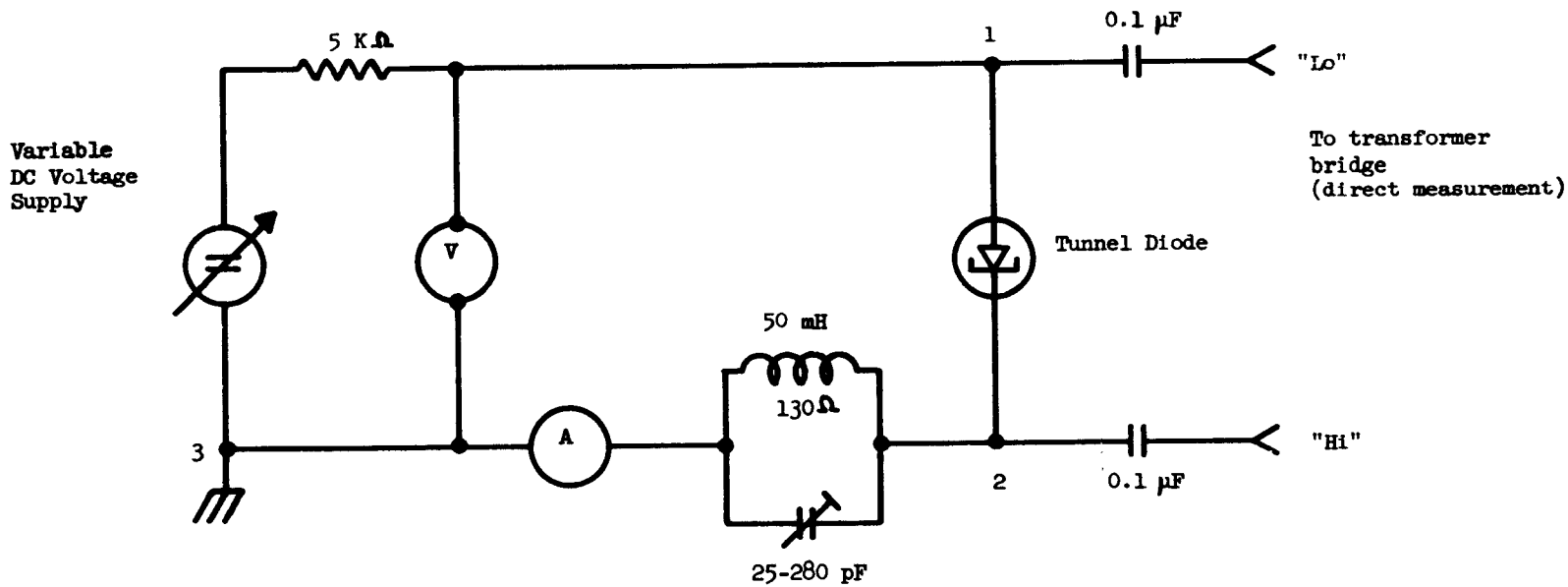
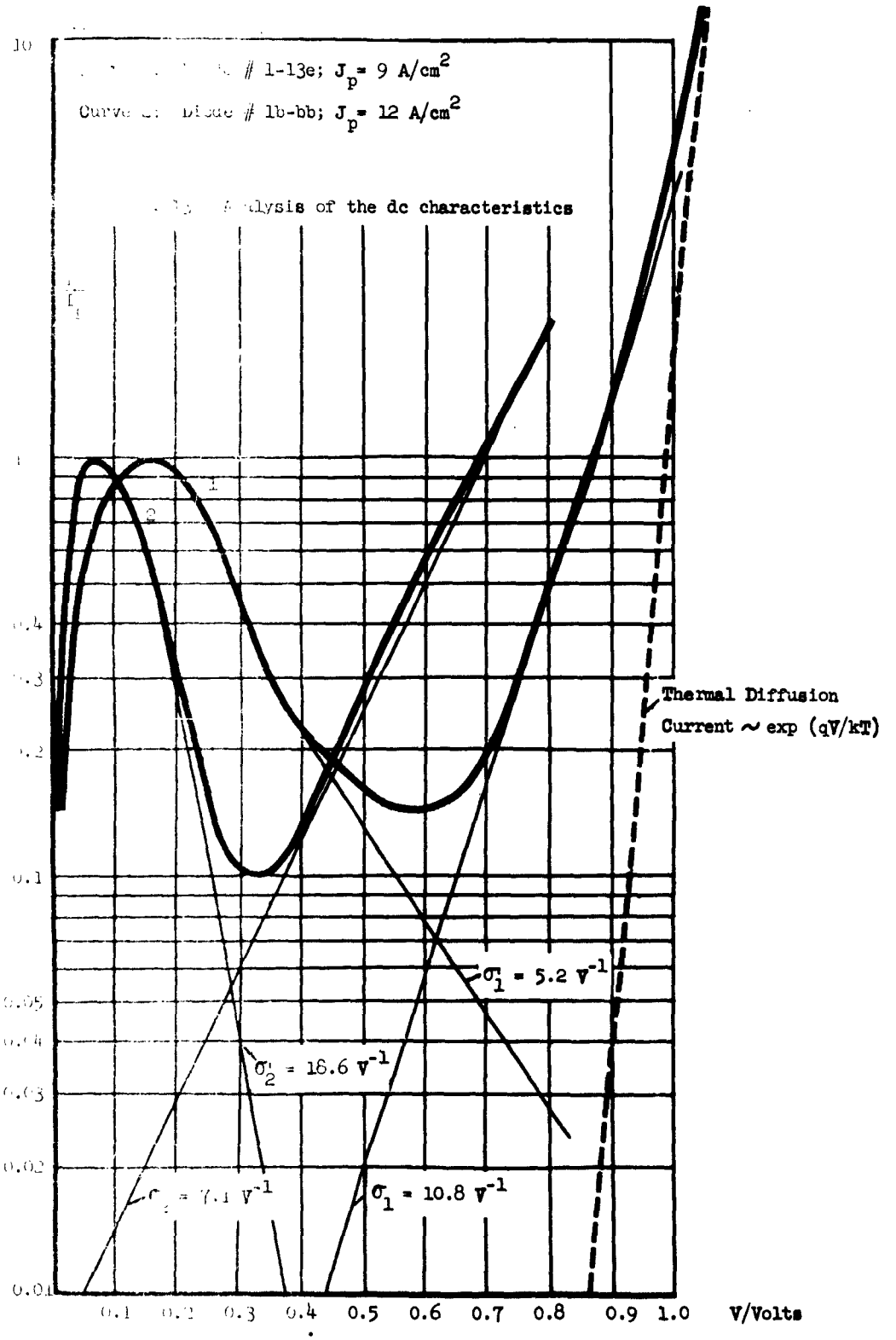


Fig. 12 Capacitance Measuring Circuit


Curve 1: Diode # 1-13e; J_p = 9 A/cm^2
Curve 2: Diode # 1b-bb; J_p = 12 A/cm^2
Analysis of the dc characteristics
10
1
0.4
0.3
0.2
0.1
0.05
0.04
0.03
0.02
0.01
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
V/Volts
σ_1 = 5.2 V^{-1}
σ_2 = 16.6 V^{-1}
σ_2 = 7.1 V^{-1}
σ_1 = 10.8 V^{-1}
Thermal Diffusion
Current ~ exp (qV/kT)

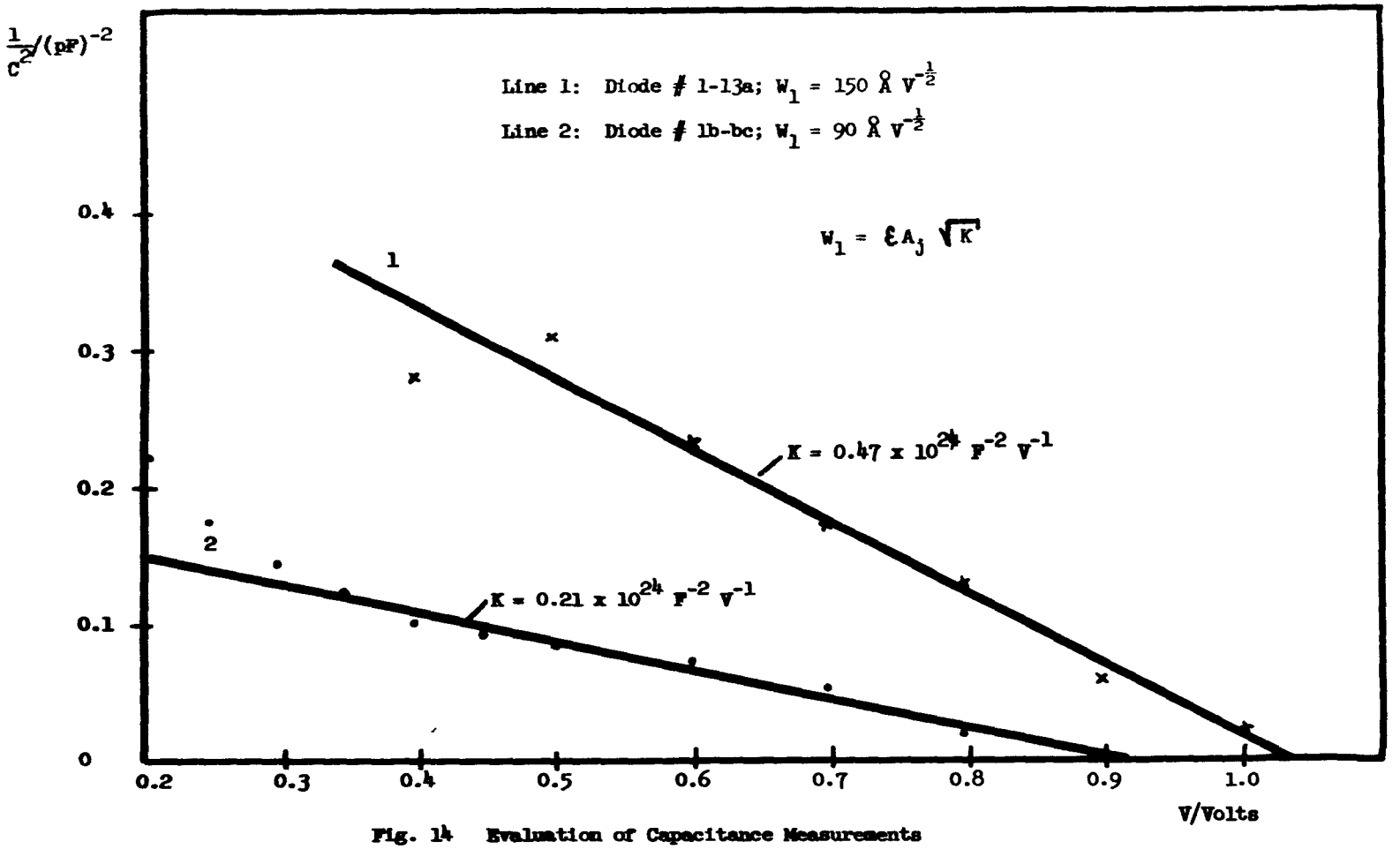


Fig. 14 Evaluation of Capacitance Measurements

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