20 kV, 2 cm^2, 4H-SIC GATE TURN-OFF THYRISTORS FOR ADVANCED PULSED POWER APPLICATIONS *

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Abstract

The need for high voltage solid-state power electronic devices for advanced power distribution and energy conversion has grown rapidly in recent years, especially for pulsed power applications that require high turn-on di/dt. However, current power converters built with silicon (Si) switches are quite bulky and inefficient, making their utilization difficult in practical energy conversion and power distribution systems. The development of high-voltage power devices based on wide bandgap semiconductor such as silicon carbide (SiC) has attracted great attention due to its superior material properties over silicon. Among the high-voltage SiC power devices, SiC gate turn-off thyristor (GTO) offers excellent current handling, very high voltage blocking, and fast turn-off capabilities. SiC GTO also exhibits lower forward voltage drop than the IGBT-based switch at high injection-level currents, resulting in lower power losses during normal operation. In this paper, we report our recently developed 2 cm^2, 20 kV SiC p-type gate turn-off GTO thyristor with very low differential on-resistance for advanced pulsed power applications.

I. INTRODUCTION

The need for renewable energy conversion and power grid technologies has grown rapidly in recent years for various high-power system applications, which require cost-effective converters with higher efficiency, higher power ratings, especially for advanced compact pulsed power applications. Over the last fifty years, silicon power devices have achieved great improvement in speed, voltage and current rating. The silicon thyristors used in current pulsed power systems are by far the most powerful solid-state power switches ever developed, and a single device can block voltage up to 8 kV and handle current up to 3000A [1]. GTOs made in Si have also been developed due to the advantages over thyristors in the higher switching speed and the ability to turn off the current without reversal of the anode to cathode voltage. In parallel to the Si thyristor and GTO, the Si IGBT is another main component for power electronics since the IGBT can be switched faster than other devices such as IGCTs and GTOs in Si. In addition, IGBT being a voltage controlled device enables smaller and more efficient gate drive systems as well as smaller passive elements. However, the use of current Si IGBT modules with a 3.5 kV rating (6.5 kV Silicon IGBTs are too slow) requires too many modules in series and/or in multi-level topologies, and a low switching frequency of 1-2 kHz, making the passive components very big and bulky. When IGBTs are connected in series, a problem arises in achieving stable and dynamic voltage balance among the devices. RC snubbers, gate timing adjustment, and pole clamps are used for dynamic balance while resistors are used for static balance. Using 6.5 kV Si Thyristors / GTOs with <1 kHz switching frequency, makes the overall system quite bulky with number of large snubbers and gate drives. In contrast, GTOs made in SiC that is capable of blocking voltage up to 20 kV or greater can greatly reduce the number of connected devices in series, resulting in a simpler gate circuitry, smaller volume, and hence cheaper system.

4H-SiC is a wide bandgap semiconductor that offers a factor of 10x higher breakdown electrical field and 3x higher thermal conductivity compared to silicon [2-3]. The intrinsic carrier concentration of SiC (3.4×10^{-8} cm^{-3}) is significantly lower than that of Si (1.5×10^{10} cm^{-3}), which makes the reverse leakage current of the SiC power devices extremely low even at elevated temperatures. This means that SiC power devices may be used for much higher frequency applications than what are possible with Si devices. For example, compared to converters based on Si GTO and Si diode, the SiC GTO and SiC PiN diode based converter can improve the efficiency by 1% at room-temperature and more than 6% at 200°C for an HVDC interface [4]. This is because of the much reduced power losses in the SiC than in the Si devices.

Among the high-voltage SiC power devices, the 4H-SiC gate turn-off thyristor (GTO) offers excellent current handling, very high voltage blocking, high turn-on di/dt, and fast turn-off capabilities. The 4H-SiC GTO also

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14. ABSTRACT
The need for high voltage solid-state power electronic devices for advanced power distribution and energy conversion has grown rapidly in recent years, especially for pulsed power applications that require high turn-on di/dt. However, current power converters built with silicon (Si) switches are quite bulky and inefficient, making their utilization difficult in practical energy conversion and power distribution systems. The development of high-voltage power devices based on wide bandgap semiconductor such as silicon carbide (SiC) has attracted great attention due to its superior material properties over silicon. Among the high-voltage SiC power devices, SiC gate turn-off thyristor (GTO) offers excellent current handling, very high voltage blocking, and fast turn-off capabilities. SiC GTO also exhibits lower forward voltage drop than the IGBT-based switch at high injection-level currents, resulting in lower power losses during normal operation. In this paper, we report our recently developed 2 cm2, 20 kV SiC p-type gate turnoff GTO thyristor with very low differential on-resistance for advanced pulsed power applications.

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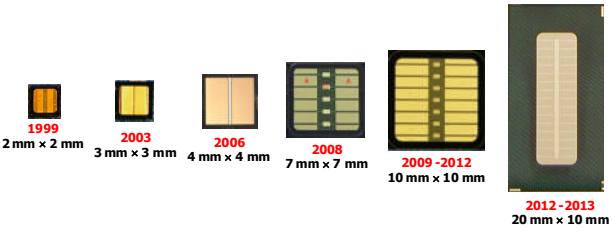
exhibits lower forward voltage drop than the IGBT-based switches, resulting in lower power losses during normal operation. Especially, it is an ideal switch for today's advance pulsed power applications that require high turn-on di/dt. While the high-voltage SiC IGBTs are making rapid strides [5], SiC IGBTs will be limited to 200°C junction temperatures, due to limitations of gate oxide reliability, which may be improved with more scientific studies and understanding of the SiC MOS material properties in future. Therefore, SiC GTOs can be operated with forced air cooling resulting in a much smaller system whereas SiC IGBTs may require active liquid cooling due to a possible thermal runaway at a high turn-on di/dt required for today's advanced pulsed power applications. Hence, the development of the high voltage (15-20 kV or higher) SiC GTOs will be crucial in building advanced pulsed-power energy conversion and power grid systems.

Over the past 14 years, SiC technology has made tremendous progresses in reducing the defect density (zero micropipe density) and growing large diameter wafers (4" commercially available, 6" demonstrated in 2010), which have enabled SiC GTOs made in larger sizes with higher blocking voltages and very low differential on-resistance [6-7]. In this work, for the first time to our knowledge, we've demonstrated 2 cm^2, 20 kV SiC p-GTO with very low differential on-resistance of 11 $m\Omega \cdot cm^2$ at high injection-level current, which represents the largest size and highest blocking voltage power switch made in SiC up-to-date.



Year	2006	2008	2009 - 10	2011	2012	2013
Chip Size (cm x cm)	0.4 x 0.4	0.7 x 0.7	1 x 1	1 x 1	1 x 1	2 x 1
BV (kV)	5	6	7 - 9	10 - 12	15 +	17 - 20
t_{drift} (µm)	60	75	75 - 90	90	120 - 160	160
Wafer ϕ (mm)	76	76	100	100	100	100 / 150
V_F degradation	Yes	Yes	No	No	No	No

Figure 1. Progresses made in SiC ultra-low defect density material growth and high-voltage SiC GTO development in the past 14 years at Cree Inc.

II. FABRICATION

A typical device cross-section of a 20 kV SiC p-type GTO is shown in Figure 2. A 2.5 µm thick p-type buffer layer was grown on an n^+ SiC substrate to achieve an asymmetrical structure. A 160 µm, $2x10^{14}/cm^3$ lightly doped, p-type layer was then grown, followed by a growth of a 2.5 µm n-type base layer. The heavily doped, p-type anode layer of 2 ~ 3 µm thickness was grown as the final top layer. To fabricate the SiC GTOs, the anode layer was first etched down to the base region. The gate layer was then etched through the base layer with a negative bevel profile around the device periphery so that the electric field crowding at edges of the device can be reduced. A lifetime enhancement process was then implemented [8-9]. The gate contact region was implanted by nitrogen, followed by a surface passivation using 4 µm PECVD oxide. The metal contacts to the anode and gate areas as well as backside cathode were then formed by rapid thermal anneal processes. The over-layer metal (Ti/Ni/Au) was deposited on both front and back sides to form the external electrical connections.

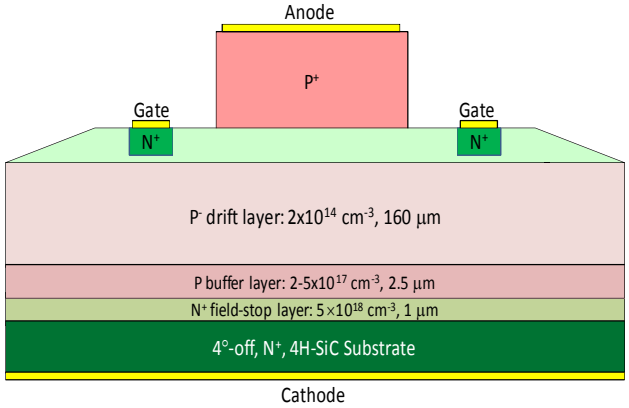


Figure 2. Simplified cross-section of a unit cell of the 20kV 4H-SiC p-GTO.

III. EXPERIMENT AND RESULTS

Due to the very high-voltage ratings (> 10 kV) for the 4H-SiC GTOs, they must be constructed using highly resistive and thick drift regions. In order to obtain a sufficiently large ambipolar diffusion length of the carriers in thick p-type epi-layer, the carrier lifetime must be made as long as possible.

A significant improvement of carrier lifetime for n-type SiC epi-layers has been achieved [8]. It has proven difficult to increase the carrier lifetime in p-type SiC epi-layers. In this work, prior to the metal contact processes, we measured carrier lifetime of the SiC p-GTO before and after the lifetime improvement process (oxidation at 1300°C for 5 hours). A method of microwave photo-conductivity decay (MW-PCD) was used to extract the carrier lifetime by illuminating the SiC GTO chip with a UV laser to create electron-hole pairs. The electrons and holes excited in this process increase the conductivity of the SiC GTO thick epi-layer. When the laser is turned off, the conductivity decays back to its original value as the electrons and holes recombine or are captured by defects in the material. Resolution of the lifetime

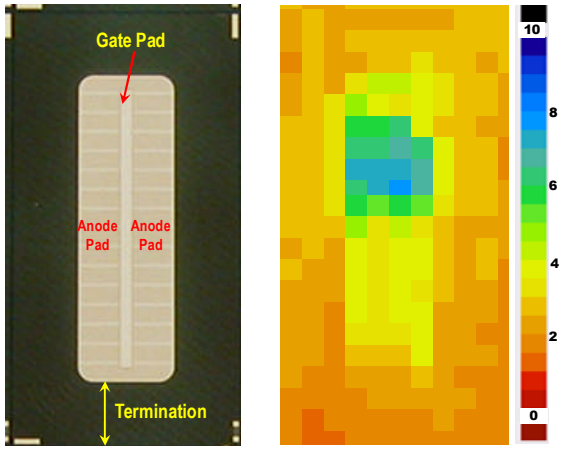


Figure 3. Top-view photograph of a 2 x 1 cm^2, 20 kV, SiC GTO chip (a) and its corresponding carrier lifetime measurement of a 20 kV, SiC GTO after the lifetime enhancement process.

measurement was set to 1 x 1 mm^2. As shown in Figure 3, for the first time to our knowledge on minority carrier lifetime improvement in the 160 µm thick p-type SiC epi-layer, we observed that the average carrier lifetime of a 2 x 1 cm^2, 20 kV, SiC GTO chip was improved from ~ 1 µs of the as-grown epi-layer to > 4 µs after the lifetime improvement process. This significant improvement on carrier lifetime in the thick p-type SiC epi-layers enables an enhanced conductivity modulation hence lower differential on-resistance at high injection-level current. However, as also seen in Figure 3 (b), the carrier lifetime was not uniform across the 2 x 1 cm^2, SiC p-GTO chip area. One potential way to control the lifetime uniformity is to control the concentration of point-defects in SiC by a low-energy electron irradiation [10].

Due to the limitations of the high-voltage test set-up, the 4H-SiC p-GTO showed an on-wafer gate-to-anode blocking voltage of ~ 20 kV at a leakage current of 1 µA (Figure 4), which corresponds to a one-dimensional (1D) maximum electrical field of ~ 1.5 MV/cm at room-temperature. To measure this large area, 4H-SiC, p-GTO at high current levels (≥ 100 A/cm^2), the forward characteristics of the device were evaluated using a Tektronix 371 curve tracer in pulse mode. As shown in Figure 5, due to the significant improvement of the carrier lifetime in this work, a very low differential on-resistance of 11 mΩ·cm^2 was obtained with respect to an active conducting area of 0.53 cm^2 at a gate current of 0.35 A and a high injection-level current of 150 A ~ 200 A. These results indicate that the SiC GTOs can be easily and safely paralleled to achieve much greater current handling capability with a gate-to-cathode blocking capability of 20 kV or higher.

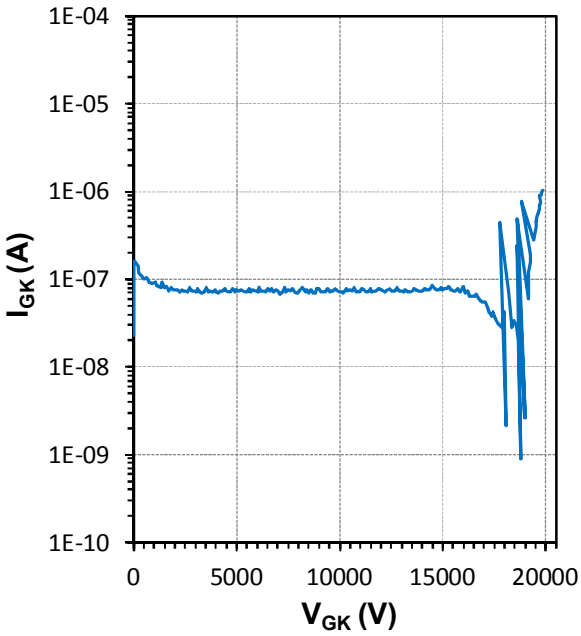


Figure 4. Gate-to-Cathode blocking (V_{GK}) capability of a 2 cm^2, 20 kV 4H-SiC GTO at room temperature.

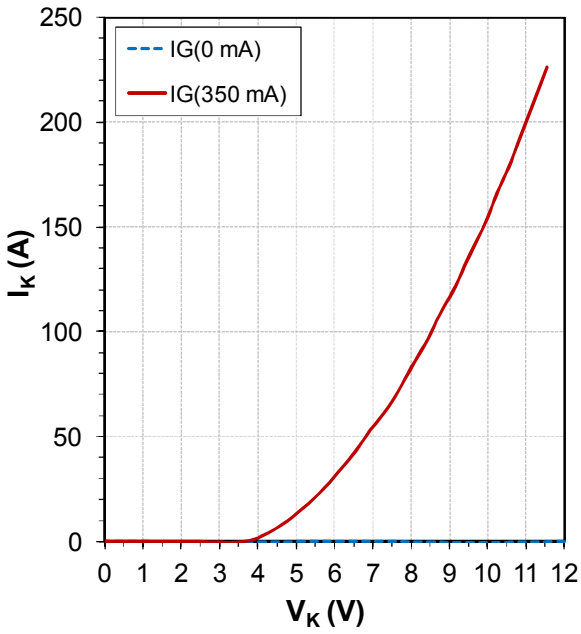


Figure 5. Forward conduction characteristics of a 2 cm^2, 20 kV 4H-SiC GTO at room temperature.

IV. SUMMARY

In this work, we have demonstrated a large area of 2 x 1 cm^2, 20 kV, 4H-SiC GTO with a very low differential on-resistance of 11 mΩ·cm^2. This significant reduction in the

on-resistance was attributed to an improvement of carrier lifetime in the 160 μm thick, $2x10^{14}/cm^3$ doped SiC p-type epi-layer. A gate-to-cathode blocking leakage current of ~ 1 μA was measured at a blocking voltage of 20 kV at room temperature. All these results indicate that the SiC GTOs can be easily and safely paralleled to achieve much greater current handling capability. Based on the results of this work, ultra-high voltage SiC GTO technology is paving the way for highly efficient pulsed power conversion and power grid applications.

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