SpaceWire Satellite Usage

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Abstract: *SpaceWire represents the most recent interface standard insertion in spacecraft computing interfaces since the widespread spacecraft adoption of CompactPCI in command and data handling systems. This paper reviews how SpaceWire's fabric based topologies are applied as a telemetry and control interface in spacecraft with discussions of hardware implementations, performance and power. SpaceWire usage in various standards including the upcoming Next Generation Space Interface Standard (NGSIS) is discussed.*

Keywords: SpaceWire; fabric topologies, telemetry and control, bandwidth, network standards, LVDS, test and debug, MIL-STD-1553B.

Introduction

SpaceWire, a medium speed interface initially standardized in the mid 2000 decade [1], continues to see increasing widespread usage among spacecraft. Early SpaceWire missions include the Lunar Reconnaissance Orbiter (LRO) and Lunar Crater Observation and Sensing Satellite (LCROSS) [2]. SpaceWire is being implemented on an international scale since its implementation is straightforward and does not require any specialized hardware beyond a space based FPGA or ASIC [3]. This widespread usage is applied across many types of satellites.

SpaceWire Component Types and Topologies

SpaceWire networks are fabrics of point to point connections. A typical SpaceWire entity contains an endpoint, a router or a combination of the two (a bridge contains a four port router and an endpoint. With these elements, one may create many topologies from simple point to point links to rings, meshes, trees and switches. See Figure 1. Each topology is often optimal for routers of a given size in number of nodes [4].

Medium Data Interface

Since SpaceWire links may provide up to 400 Mbaud of transmission bandwidth realizing up to 320 Mbps of data depending on packet lengths and traffic density, a major use of SpaceWire in some spacecraft is for passing data between spacecraft functions where the bandwidth provided is sufficient. This was true in the LRO spacecraft as a whole as well as in the Mini-RF payload [5]. When SpaceWire is used for heavy data distribution, most network connections are point to point or point to star as long as the star has sufficient bandwidth to handle the data.

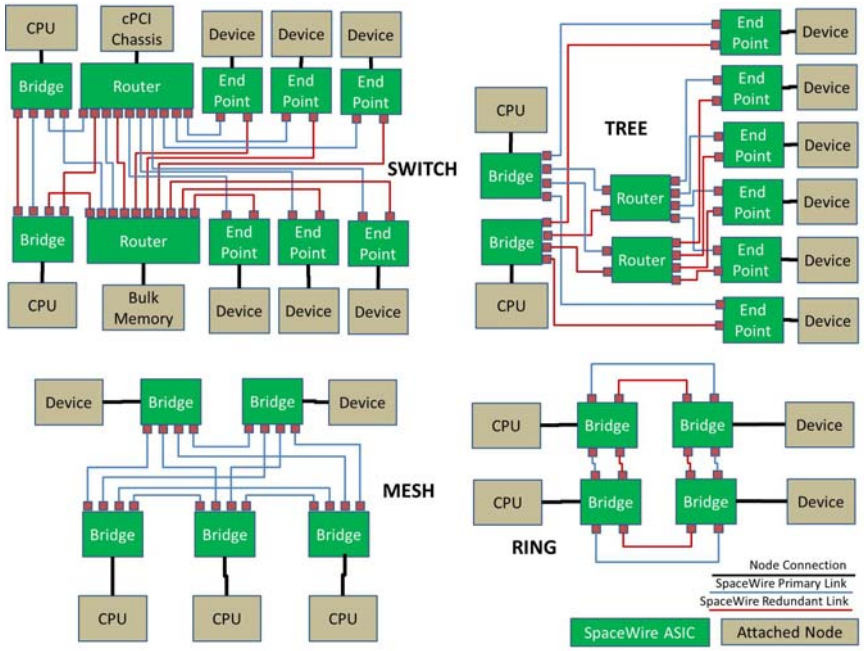

Figure 1. SpaceWire Topologies

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14. ABSTRACT
SpaceWire represents the most recent interface standard insertion in spacecraft computing interfaces since the widespread spacecraft adoption of CompactPCI in command and data handling systems. This paper reviews how SpaceWires fabric based topologies are applied as a telemetry and control interface in spacecraft with discussions of hardware implementations, performance and power. SpaceWire usage in various standards including the upcoming Next Generation Space Interface Standard (NGSIS) is discussed.

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If the data bandwidth is lower per endpoint and there is enough capacity to accommodate data, then a ring or tree may be used to cost effectively capture the data. Switches or other concentrated routers are not needed as the data may be communicated between nodes without using up all of the ring or tree's bandwidth. Often telemetry and control may be integrated onto the fabric as well, if sufficient bandwidth is available to guarantee commands may be handled in a timely manner. New real time and guaranteed delivery extensions to SpaceWire standards currently in development may make this easier in the near future.

Telemetry and Control

With the advent of SERDES links and components targeted for spacecraft data handling due to more data needing to be moved between components, SpaceWire will begin to be edged out for main data handling. A single SERDES link will provide 10x the data bandwidth of a SpaceWire link. Thus as data processing, handling and storage increase, SpaceWire may end up as an alternate network in charge of the commands and data handling. This is being pushed from the bottom by the need to replace the 500Kbps MIL-STD-1553B which is being overwhelmed more often as advanced processing is implemented.

A MIL-STD-1553B network was one or more busses connecting elements throughout the spacecraft. Each link could only provide 500 Kbps which is very limiting. Most spacecraft are not created anew but instead rely on reuse. Thus a spacecraft which begins to replace the 1553 will likely not jump entirely to SpaceWire. Instead some nodes will be changed over and some will remain. This requires a bridge from 1553 to SpaceWire so the controller may administer command and data handling efforts across all interfaces. See Figure 2.

MIL-STD-1553B busses were connected in only one direction and did not require loops. This was especially important in large spacecraft to minimize cable lengths. For this reason, either star or tree or non-connected rings are more likely used with SpaceWire than fully connected rings. The 10 meter limit on a SpaceWire link comes into play on larger more distributed spacecraft. These may require one or more routers to act as repeaters to reach the farthest nodes of the spacecraft.

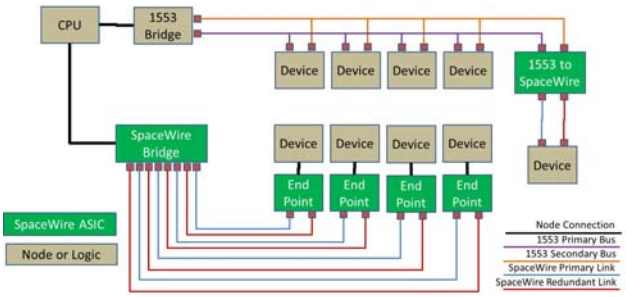

Figure 2. Telemetry and Command Network with 1553 and SpaceWire

Current Standards and Common Applications

There is several spacecraft standardization or commonality efforts that have included SpaceWire. These are shown in Table 1 [6]. Note SpaceWire is second to a SERDES level interface in three of these.

NGSIS Control Plane

NGSIS standards are currently in development and thus subject to change. A study group has been formed under VITA Standards Organization (VITA 78) and will result in a SpaceVPX standard derived from OpenVPX [7]. A typical NGSIS system as currently envisioned will require a control plane separate from the data plane.

Table 1. Spacecraft Commonality Efforts using SpaceWire

Effort	Sponsor	SpaceWire Usage;	Other Interfaces	Purpose	Comments
SpaceWire Standard	ESA	data interface; cables; backplane future	none	standard medium speed low complexity interface	
SpaceFibre Standard	ESA	sub-interface; cables	SpaceFibre	Higher speed data interface	tries to keep SpaceWire structure
Space Plug and Play	AFRL	data interface; cables	USB, I2C, Fiber	encapsulate function at each node hiding complexity	SPA-S demonstrated
Common Instrument Interconnect	NASA	data interface; cables	RS422	Hosted Payload data interface	
Joint Architeccture Standards	Sandia, LANL	control interface; backplane	sRIO, PCIe	Common standards for joint development projects	
Next Generation Space Interconnect Standard (NGSIS)	AFRL, JPL, AIAA, VITA, sRIO	control interface; backplane	sRIO, I2C	define interoperable interfaces cards and backplanes	SpaceVPX being defined under VITA78 for backplane and slots

Planes are defined based on OpenVPX heritage as examples of the network connections. A controller is expected to be required somewhere in the SpaceVPX backplane that will provide control information from the system monarch or controller to all active slots in the system. The controller will send configuration commands to each slot, gather telemetry from each slot and manage the onboard setup and testing. The controller will also manage any dynamic reconfiguration of the control or data plane networks.

A connection diagram of an NGSIS backplane showing data and control plane connections is shown in Figure 3. Note that unlike OpenVPX, a NGSIS system may be fully single point fault tolerant with M of N fault tolerance on the payload slots. Thus there will be two box controllers using SpaceWire present in a given system. The redundancy control of the controller and other basic box capabilities will be managed using the management plane over utility plane signals.

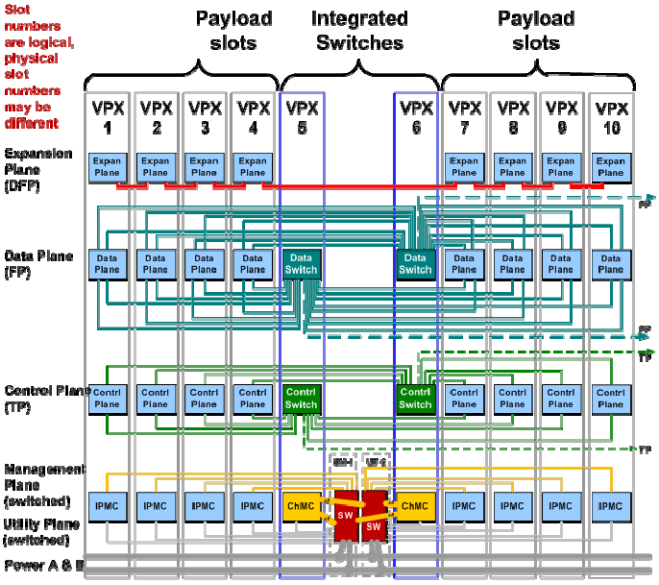

Figure 3. NGSIS Standard Backplane with control plane switch and two data plane connections per payload

As NGSIS is standardized in 2013, BAE Systems expects to begin seeing compliant systems fielded in 2014 and 2015. SpaceWire will play a key role in these systems.

Hosted Payload and Plug and Play Interfaces

Table 1 does also show applications where SpaceWire retains its data plane purpose. In many of these cases just like the telemetry and command applications, SpaceWire is connected by cables and many of the interfaces are remote from the command and data handling processor controlling the interface. Endpoints may be quite isolated and require a single SpaceWire interface. These interfaces will also have some form of smarts to manage the interface and hide the complexity of what is connected to that interface. For instance, in the plug and play standards effort, this is called an Applique Sensor Interface Module (ASIM) [8]. Often these SpaceWire endpoints do not require a router; only a redundant PHY.

BAE Systems Hardware Implementations

BAE Systems in conjunction with NASA Goddard Space Flight System designed one of the first SpaceWire ASICs in 2004 [9]. This ASIC has flown on LRO and other spacecraft. This single chip solution has both four SpaceWire ports and 2 endpoints in a single ASIC. This first generation part can be applied across all the applications mentioned above to provide SpaceWire interfaces, though only to 264 Mbaud per link due to its 250 nm CMOS technology base.

BAE Systems has improved on the first design and demonstrated higher performance and more fault tolerance as well as high numbers of router ports [4]. These demonstrations provided the base for five new ASICs in various stages of development, each that contain SpaceWire links. Combined, these new ASICs show BAE Systems' commitment to utilizing SpaceWire throughout spacecraft electronics.

With power dissipation between 0.1 and 1.5W depending on frequency and interface usage, the SpaceWire Endpoint ASIC provides single SpaceWire port with redundant PHYs. A small embedded microcontroller (EMC) runs independently wherever needed and is perfect for remote endpoint applications of SpaceWire for both medium data and command and telemetry functions. At 80 MHz maximum frequency, the SpaceWire Endpoint supports up to a 320 Mbaud SpaceWire link and 16 Dhrystone MIPS of EMC processing throughput. Several backend interfaces are provided including memory, a general purpose FIFO, SPI, I2C, JTAG, UART, SELECTMap and programmable discretes for connecting SpaceWire to existing or new spacecraft electronics. [10]

The Golden Gate Bridge ASIC [10] is a system on a chip. housing the same EMC as the SpaceWire Endpoint ASIC, has four SpaceWire ports and four internal endpoint interfaces along with two PCI busses, a MIL-STD-1553 interface, an optional 60x interface to a RAD750®, a generic FIFO and a high speed SDRAM / SRAM interface. Golden Gate provides a high performance update to the SpaceWire ASIC and may be used as a 1553 to SpaceWire bridge in upgrading legacy systems to SpaceWire.

The RAD5510™, RAD5545™ and RA***DSP***EED®-HB (Host Bridge) are three new system on a chip ASICs being developed in 45 nm SOI technology. Each features one or four RAD5500™ cores which is a radiation hardened version of Freescale Technologies e5500 core in state of the art QorIQ™ Power Architecture™ [11].

The RAD5510 has a single RAD5500 core and utilizes SpaceWire as its key data interface. A large internal router connects sixteen external SpaceWire links with eight

internal endpoint interfaces providing the large router elements described in the topologies above and previously demonstrated in BAE Systems space laboratory. Several memory interfaces are provided on the RAD5510 including a configurable DDR2/DDR3 interface, an SRAM/ROM interface, and multiple types of flash memory interfaces. The RAD5510 is targeted to be used in systems with medium data transport needs that utilize SpaceWire and its Gigabit Ethernet ports as the main data transport between multiple sources. The RAD5510 may also be used to provide the control plane switch for SpaceVPX slots. This single core processor plus the EMC provides up to 700 MIPS and 466 MFLOPS where medium processing capability and low power are required.

The RAD5545 and RA***DSP***EED-HB each have four RAD5500 processor cores. The RA***DSP***EED-HB provides this significant host processing as data managing support for its direct connection to one to four RA***DSP***EED® DSPs, each capable of 70 GFLOPS of signal processing [12]. The RAD5545 replaces the connections to the RA***DSP***EED DSP with a second DDR2/DDR3 memory interface that is shared across the four processor cores. Both of these high performance devices provide up to 5200 MIPS and over 3700 MFLOPS of processing. This higher processing capability requires the use of SERDES ports for external data movement. Each device contains four 20 Gbaud sRIO ports to move data into and out of the processor and/or to pass on to the RA***DSP***EED DSP. These devices use SpaceWire mainly as the control plane bus though it could also be used to attach to lower speed data sources and sinks not requiring the performance (and power) of the SERDES links. Thus, like the bridge ASICs before them, each of these CPUs have four SpaceWire external ports connected to four internal endpoint ports and an EMC. The target speed for these ports will be up to 400 Mbaud each.

Future of SpaceWire

SpaceWire is expected to see continued usage through spacecraft both as a data transport and as control plane. SpaceWire has a lower power per link than SERDES or optical devices, straightforward implementation, widespread application in standards efforts and yet still has orders of magnitude better performance than MIL-STD-1553, Just as MIL-STD-1553 has continued to be reused in spacecraft over multiple decades, SpaceWire should find continued usage over at least the next decade of spacecraft and likely beyond. BAE Systems, one of the first with a radiation hardened SpaceWire ASIC, continues to include SpaceWire in its space electronics building blocks, boards and systems greatly enabling the continued insertion and leverage of this interface in future space missions.

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