ARMY RESEARCH LABORATORY

0.15-µm Gallium Nitride (GaN) Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication

by John Penn

ARL-TN-0496 September 2012

Army Research Laboratory
Adelphi, MD 20783-1197

ARL-TN-0496 **September 2012**

0.15-µm Gallium Nitride (GaN) Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication

John Penn
Sensors and Electron Devices Directorate, ARL

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*
September 2012

2. REPORT TYPE
Final

3. DATES COVERED (From - To)

4. TITLE AND SUBTITLE
0.15-µm Gallium Nitride (GaN) Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
John Penn

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
ATTN: RDRL-SER-E
2800 Powder Mill Road
Adelphi, MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TN-0496

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
High-speed electronic circuits are needed for Army systems in communications, wireless sensors, imaging, and other systems. Gallium nitride (GaN) technology offers the highest power densities for radio frequency (RF) and wireless integrated circuits. Several GaN broadband high power efficient power amplifier designs for high frequency operation, such as satellite communications (SATCOM), were recently designed and submitted for fabrication using a proprietary 0.15-µm GaN process under development at TriQuint Semiconductor. These monolithic microwave integrated circuits (MMICs) are being fabricated by TriQuint as part of a recent cooperative research and development agreement (CRADA) with the U.S. Army Research Laboratory (ARL).

15. SUBJECT TERMS
MMIC, GaN

16. SECURITY CLASSIFICATION OF: a. REPORT	b. ABSTRACT	c. THIS PAGE	17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
Unclassified	Unclassified	Unclassified	UU	18	John Penn
					19b. TELEPHONE NUMBER (*Include area code*) (301) 394-0423

Contents

List of Figures

1. Introduction

Compact very efficient communication links are important to Army systems for communications, wireless sensors, and other electronic systems. Constantly improving power efficiencies, power densities, and higher bandwidths continue to push the state of the art in radio frequency (RF) electronics and devices. Recent advances in gallium nitride (GaN) technology have significantly increased power densities for monolithic microwave integrated circuits (MMICs) over previous technologies, such as gallium arsenide (GaAs) and other III/V devices. The U.S. Army Research Laboratory (ARL) is interested in custom design of circuits for state-of-the-art systems and also state-of-the-art commercially available parts. TriQuint Semiconductor is a provider of both foundry services for GaN custom MMICs as well as commercial MMICs. A previous technical report; *SATCOM and Ka-band Gallium Nitride (GaN) Power Amplifier Monolithic Microwave Integrated Circuit (MMIC)*, ARL-MR-0817[1]; described several custom GaN broadband power amplifiers at Ka-band, to demonstrate high efficiency, high-power power amplifiers (PAs) for microwave communications, applicable to satellite communications (SATCOM). Two of those Ka-band designs were submitted to TriQuint Semiconductor for fabrication under a recent cooperative research and development agreement (CRADA) between ARL and TQS, Inc. Additional circuits by the author, John Penn, and also by Caroline Waiyaiki of ARL, were submitted for fabrication and those designs will be documented in later reports.

2. Layout of GaN Die

Several PAs for Ka-band and higher frequency operation were designed using TriQuint's proprietary 0.15-µm GaN process. Early access to this unreleased fabrication process was obtained through the CRADA between ARL and TQS, Inc. TriQuint agreed to fabricate two 2.5 mm x 2 mm die, as these circuits are of mutual interest in obtaining high frequency, high performance PAs for SATCOM and other communications systems with military applications. Design was performed with computer-aided design (CAD) tools using models provided by TQS, and using a design kit containing passive components from TriQuint's lower frequency commercial 0.25-µm GaN process, which are compatible with the 0.15-µm GaN process. These circuits were then combined into two 2.5 mm x 2 mm die to comprise part of the tiling of TriQuint's next multi-project prototype 0.15-µm GaN wafer fabrication. Figure 1 shows the plot of the first die layout, which includes a broadband high third-order intercept low-noise amplifier

[1] Penn, J. *SATCOM and Ka-band Gallium Nitride (GaN) Power Amplifier Monolithic Microwave Integrated Circuit (MMIC)*; ARL-MR-0817; U.S. Army Research Laboratory: Adelphi, MD, April 2012.

(LNA), a 30-GHz one stage PA, two parallel combined 30-GHz PAs, and two versions of a 45-GHz single stage PA. Figure 2 shows Caroline Waiyaiki's harmonic power combiner of two parallel high electron mobility transistors (HEMTs) in a 30-GHz PA, test cells for the individual one-stage PAs, and the broadband LNA included on the previous die.

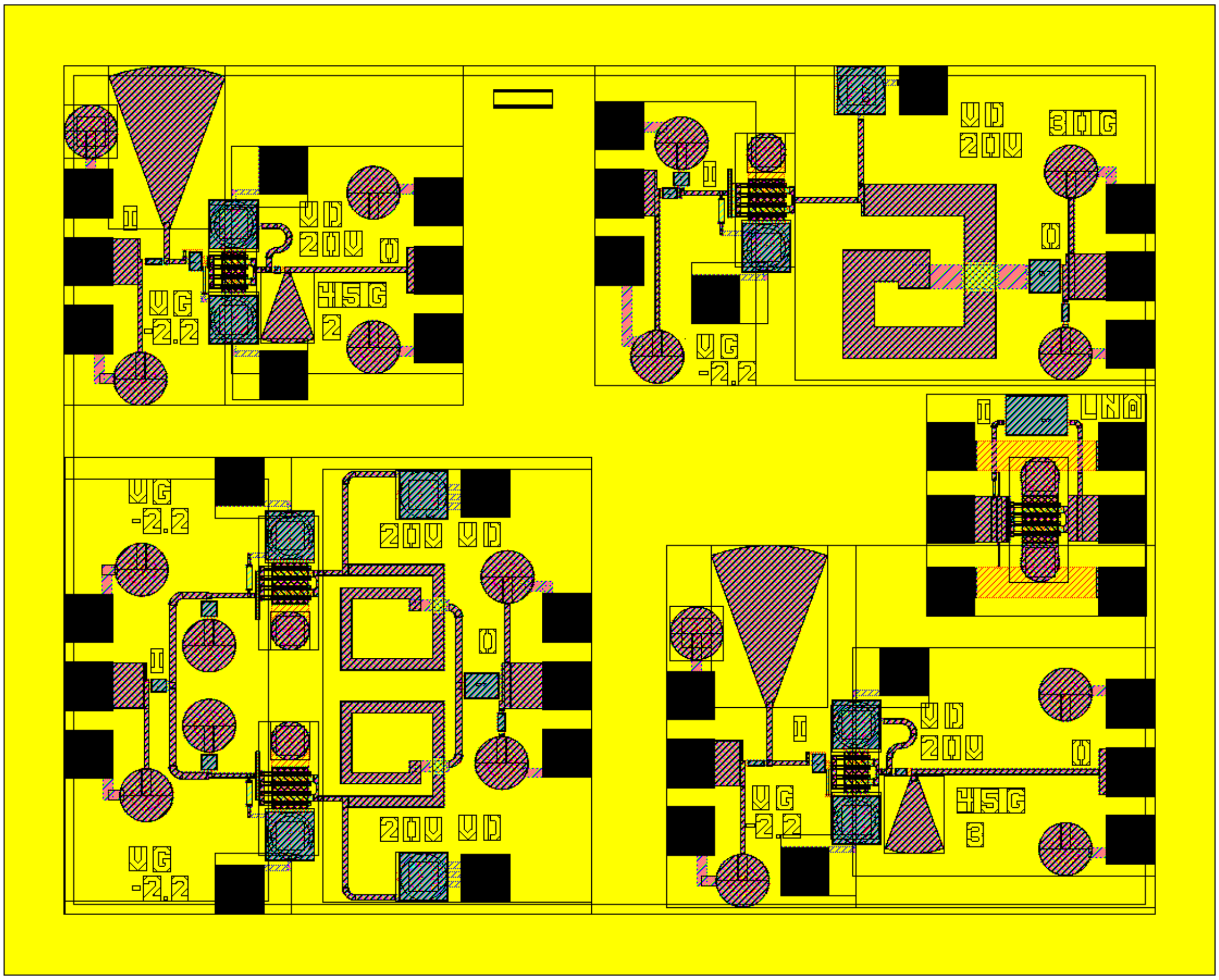

Figure 1. CKT1 30-/45-GHz PAs, plus a broadband LNA 2.5 mm x 2 mm.

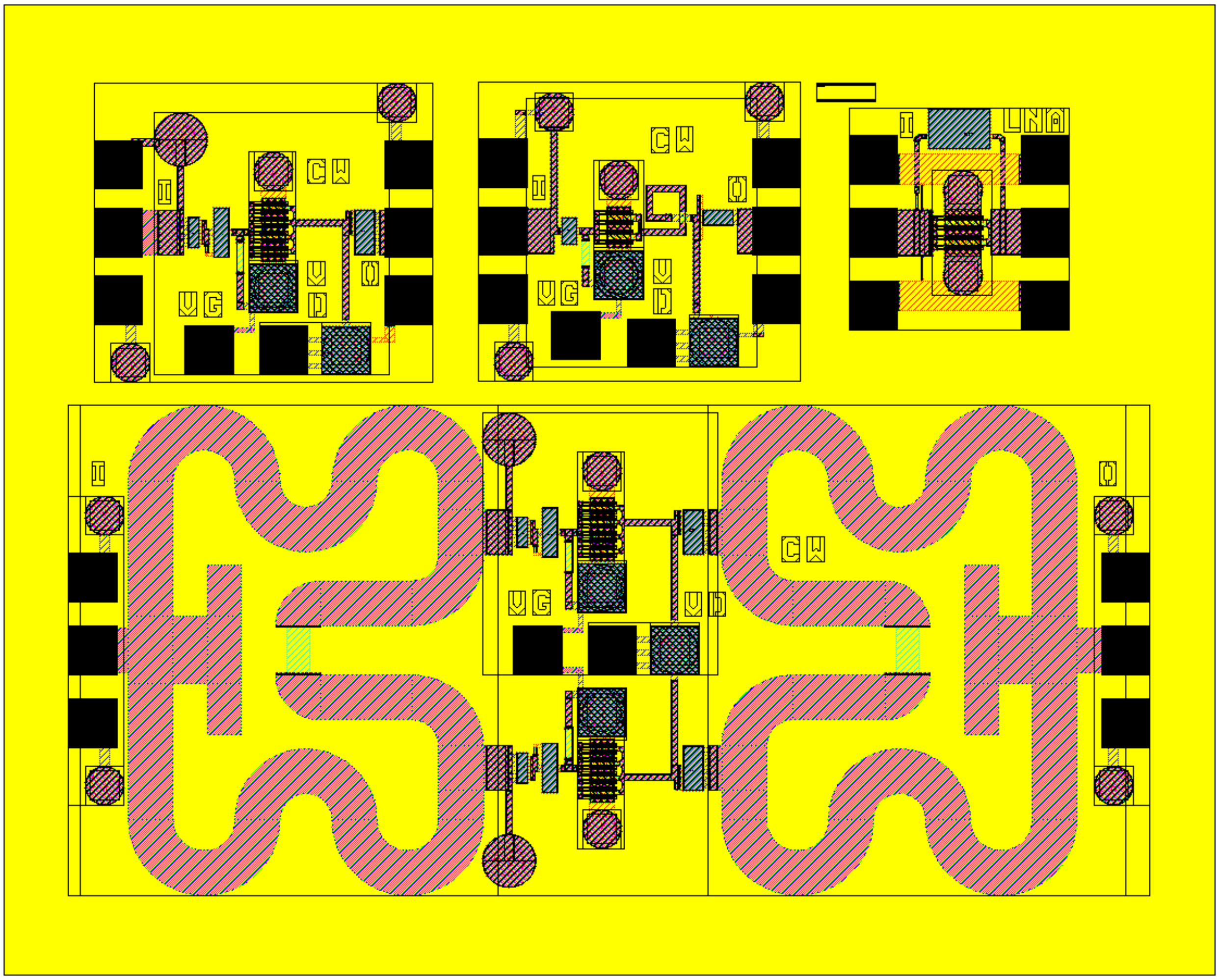

Figure 2. CKT2 30-GHz Harmonic two way combiner PA 2.5 mm x 2 mm.

3. Summary of Designs

Following is a list of the amplifier designs in each die layout:

- CKT1—0.3-mm, 30-GHz PA; 0.6-mm parallel combined 30-GHz PA; two versions of a 0.2-mm, 45-GHz PA; and a broadband high IP3 LNA. (2.5 mm x 2 mm die)
- CKT2—0.2-mm, 30-GHz PA; 0.4-mm, 30-GHz PA; 0.8-mm parallel combined 30-GHz PA; and a broadband high IP3 LNA. (2.5 mm x 2 mm die)

The first two 30-GHz PAs in CKT1 have been documented previously. Two different variations for a 45-GHz PA will be documented in another technical report, likewise, for the broadband high IP3 GaN LNA.

Caroline Waiyaiki has been designing high linearity, efficient, high frequency amplifiers using a harmonic termination power combiner passive circuit. The tradeoff is larger size in the combiner versus improved linearity due to reduced higher order harmonics. Her doctoral thesis is based on this harmonic power combiner circuit and those designs will be documented separately.

4. Design Rule Checking (DRC)

Design rule checking (DRC) verifies all the layout information to provide for manufacturability. Checks for correct line widths, spacing between polygons within the masks, and checks for appropriate combinations of layers, etc., to ensure a successful design are performed with the DRC software and design rules—both provided by TriQuint. Initially, the layouts were checked according to the process design rules supplied by TriQuint, but for their released 0.25-µm GaN process. TriQuint provided additional DRC for the research 0.15-µm GaN process. Discussions with a TriQuint layout engineer and modifications to the layout were performed to remove all design rule errors. There still is the possibility of an electrical error, even with a correct DRC check. No additional layout versus schematic checking was done for these designs, possibly that will be available in the future. This is the first ARL submission in this unreleased TriQuint 0.15 µm GaN process.

5. Design Data Sheet

TriQuint's customer design data sheet must be completed and submitted along with the standard GDSII layout file. The design checklist is completed to ensure that the tile design has passed DRC checks and ensure the avoidance of common pitfalls. Any fabrication options are designated such as 4-mil thinned wafers with substrate vias for this design. Lastly, plots of the die layouts are included. This should match what TriQuint receives when they import the GDSII file into their system.

6. Conclusion

ARL designed and submitted to fabrication several high efficiency, high power GaN Ka-band PAs for SATCOM applications and other communications systems of interest to the Army. TriQuint Semiconductor will fabricate these designs under the CRADA between ARL and TQS. Once the designs are returned, they will be tested and documented in future reports. These will be the first designs from ARL using early access to the high frequency 0.15-µm GaN research process from TriQuint. Earlier broadband GaN amplifiers using TriQuint's released 0.25-µm

GaN process are documented in ARL technical reports ARL-TR-5987[2], *Broadband, Efficient, Linear C-Band Power Amplifiers Designed in a 0.15 µm Gallium Nitride (GaN) Foundry Process from TriQuint Semiconductor*, April 2012. Testing of those devices is documented in a coming technical report. Additional reports on the design of the 45-GHz PAs and broadband LNA will be released. Likewise, Caroline Waiyaiki will document her thesis work on the harmonic power combiner circuit for improved linearity in PA design.

[2]Penn, J. *Broadband, Efficient, Linear C-Band Power Amplifiers Designed in a 0.15 µm Gallium Nitride (GaN) Foundry Process from TriQuint Semiconductor*; ARL-TR-5987; U.S. Army Research Laboratory: Adelphi, MD, April 2012.

INTENTIONALLY LEFT BLANK.

Appendix A. Checklist for 0.15 µm GaN Submission 7/20/2012

The following is the checklist for the 0.15-µm GaN submission, 7/20/2012.

Designer: Fill in all Yellow highlighted areas.

TQT Input Checklist for Foundry Custome **EG** **426**

Please initial each item.

X	Maximum current density not exceeded in actives or passives.
X	GDS file has all gates parallel to the x-direction.
X	All vias are 60 um
X	All vias are >= 145 um from the chip edge (layer 25)
X	Via-to-via, via-to-bondpad, and metal0 overlap of vias are correct.
X	All customer labeling is in nitride
X	Dielectric overlaps gate metal, resistors, and capacitor bottom plate.
X	Enclosed geometries of specified levels > 1% break periphery. > 5% is recommended.
X	All metal >= 125 um from the chip edge (layer 25)
X	Ohmic metal underneath all bond and RF probe pads.
X	Maximum die size and aspect ratio observed (in all directions).
X	Appropriate gate gph used for GaN
X	GPHs placed for required TriQuint Texas process structures and alignment markers.
X	On-chip ESD protection included as appropriate
X	Circuit naming convention has been followed.

USE TEST PLAN WORKBOOK TO DEFINE TESTS

Following checklist is for required items

NA	Schematics for all circuits with LVS option = Yes	
	___	Cap bottom plates are indicated.
	___	Number of vias equals number of grounds represented on schematic.
	___	Junctions, as opposed to crossovers, are clearly marked.
	___	FETs are labeled S,D,G.
	___	Resistors labeled with material type (TaN,Mesa).
	___	Capacitors are indicated for all cap tweakers.
	___	Resistors in series are shown individually (not grouped).
NA	DC probe of circuits, the following paperwork is completed:	
	___	DC Test Plan
	___	DC probe point diagram
	___	DC schematic showing DC probe points
		**This schematic does not have to be the same level of detail as LVS schematic.
		**This can be the same schematic as above - if probe points are called out.
	___	Test time is under 5 hours / maximum of 3 passes.
NA	RF probe of circuits, the following paperwork is completed:	
	___	RF Test Plan
	___	RF probe point diagram
	___	Initial Specification Limits provided.
	___	TQT RF Cal set selected on Data Sheet or GDS file of calibration structures supplied.
	___	Test time is under 5 hours / maximum of 3 passes.
NA	All Items completed for FTP Submittal	
	___	DC and/or RF Probe point diagrams
	___	GDS file of device section.

John E Penn	7/20/2012
Customer signature for completed checklist	Date
John E Penn	ARL
Customer name (printed)	Company

Appendix B. Customer Datasheet for 0.15 µm GaN Submission 7/20/2012

The following is the customer data sheet for the 0.15-µm GaN submission, 7/20/2012.

TriQuint Texas PCO Customer Data Sheet

Mask Number: EG______

TRIQUINT PCO CUSTOMER DATA SHEET

This Data Sheet, along with a clean design gdsii file (as determined by the on-line DRCs) and Foundry Customer Checklist comprise the complete PCO data packet. If LVS is required a clean schematic must also accompany this data packet. Mask plates will not be ordered without a fully completed data packet and purchase order. A copy of the most current Foundry Customer Checklist can be obtained through your Foundry Engineer or Program Manager.

Customer Information: Arl Date: 7/23/2012

Primary Technical Contact:	John Penn	Phone #	3013940423
		Alt. Phone #:	
		E-mail:	John.Penn4@Us.Army.Mil
Secondary Contact:	Romeo Delrosario	Phone #:	3013943562
		E-mail:	Romeo.Delrosario@Us.Army.Mil
PO number (if available)			

Indicate Clean Data File Deadline (as published on the web-site) that this file is intended for: 7/20/12

Die dimensions: (scribe street center to scribe street center). Select one:

[x-direction] X [y-direction] ☐ 4 mm X 4 mm ☐ 4 mm X 2 mm ☐ 2 mm X 4 mm ☐ 2 mm X 2 mm

GDS II Stream File name: Top Level Cell Name:

LVS (Layout vs Schematic): ☒ No ☐ Yes (you must supply schematics at or before time of submittal)

Process Requirements: (Click ONE box only)

PROCESS	
pHEMT	☐ 0.15µm pwr-pHEMT 3MI ☐ 0.25µm mmw-pHEMT 3MI ☐ 0.25µm XKu-pHEMT 3MI ☐ 0.35µm pwr-pHEMT 3MI
mHEMT	☐ 0.15µm LN-mHEMT 3MI
GaN	☐ 0.25µm GaN on SiC 3MI
other	☒ 0.15um GaN on SiC 3MI

Layout Requirements: (Click ALL that apply)

Does your layout contain:
- ☐ GaAs Resistors
- ☒ TaN Resistors
- ☒ TaN Resistors of width <12.5µm
- ☒ MIM Capacitor Type 7
- ☐ MIM Capacitor Type G
- ☒ Amp-style FETs
- ☐ Switch/Diode-style FETs

Thickness in mils: ☒ 4 (100 µm) ☐ 2 (50 µm) [2 mils is not available at this time]

Shipping Information: To protect intellectual property, PCOs are shipped wafflepacks. For exact wafflepack number, contact your TriQuint Foundry Program Manager.

Special instructions TRIQUINT PRIOR-APPROVAL REQUIRED:

The person who fills out this form must type their name on the signed line. This counts as an electronic signature. TriQuint Foundry Services will provide mask making service based on information from this datasheet.

Signed: John E Penn Date: 7/20/12

Page 1 of 1

This document is for informational purposes only and is not revision controlled

List of Symbols, Abbreviations, and Acronyms

ARL	U.S. Army Research Laboratory
CAD	computer-aided design
CRADA	cooperative research and development agreement
DRC	design rule checked
GaAs	gallium arsenide
GaN	gallium nitride
LNA	low-noise amplifier
MMIC	monolithic microwave integrated circuit
PA	power amplifier
HEMT	high electron mobility transistor
RF	radio frequency
SATCOM	satellite communications
TQS	TriQuint Semiconductor, Inc.

1 (PDF only) DEFENSE TECHNICAL
INFORMATION CTR
DTIC OCA
8725 JOHN J KINGMAN RD
STE 0944
FORT BELVOIR VA 22060-6218

1 DIRECTOR
US ARMY RESEARCH LAB
IMAL HRA
2800 POWDER MILL RD
ADELPHI MD 20783-1197

1 DIRECTOR
US ARMY RESEARCH LAB
RDRL CIO LL
2800 POWDER MILL RD
ADELPHI MD 20783-1197

1 DIRECTOR
US ARY RESEARCH LAB
RDRL CIO LT
2800 POWDER MILL RD
ADELPHI MD 20783-1197

12 DIRECTOR
US ARMY RESEARCH LAB
RDRL SER
PAUL AMIRTHARAJ
RDRL SER E
ROMEO DEL ROSARIO
BEN HUEBSCHMAN
JAMES WILSON
TONY IVANOV
JOHN PENN (3 HCS)
ROBERT PROIE
ROBERT REAMS
PANKAJ SHAH
ED VIVEIROS
2800 POWDER MILL RD
ADELPHI MD 20783-1197