Actuation and Response in Microsystems

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**Abstract**

THz and nm Transistors for 1-1000 GHz Electronics

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**Keywords**

- THz Transistors
- nm Transistors
- 1-1000 GHz Electronics

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**Number of Pages**

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THz and nm Transistors for 1-1000 GHz Electronics

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The End (of Moore's Law) is Near (?)

It's a great time to be working on electronics!

Things to work on:

* InP transistors: extend to 3-4 THz → GHz & low-THz ICs
* GaN HEMTs: powerful transmitters from 1-300 GHz
* Si MOSFETs: scale them past 16 nm
* III-V MOSFETs: help keep VLSI scaling (maybe)
* VLSI transistors: subvert Boltzmann → solve power crisis
* mm-wave VLSI: massively complex ICs to re-invent radio
Why THz Transistors?
Why Build THz Transistors?

- THz amplifiers \( \rightarrow \) THz radios
- Imaging, sensing, communications
- High-performance receivers
- Fiber optics
- 500 GHz digital logic

**Diagram:**
- Transistor Power Gain, dB
- Frequency, Hz

**Graph:**
- Precision analog design at microwave frequencies
- Higher-Resolution Microwave ADCs, DACs, DDSs

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How to Make THz Transistors
**Frequency Limits and Scaling Laws of (most) Electron Devices**

\[ \tau \propto \text{thickness} \]

\[ C \propto \text{area} / \text{thickness} \]

\[ R_{\text{top}} \propto \frac{\rho_{\text{contact}}}{\text{area}} \]

\[ R_{\text{bottom}} \propto \frac{\rho_{\text{contact}}}{\text{area}} + \frac{\rho_{\text{sheet}}}{4} \cdot \frac{\text{width}}{\text{length}} \]

\[ I_{\text{max, space-charge-limit}} \propto \frac{\text{area}}{(\text{thickness})^2} \]

\[ \Delta T \propto \frac{\text{power}}{\text{length}} \times \log \left( \frac{\text{length}}{\text{width}} \right) \]

**To double bandwidth,**

- reduce thicknesses 2:1
- improve contacts 4:1
- reduce width 4:1, keep constant length
- increase current density 4:1
Bipolar Transistor Scaling Laws

Changes required to double transistor bandwidth:

<table>
<thead>
<tr>
<th>parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>collector depletion layer thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.414:1</td>
</tr>
<tr>
<td>emitter junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>collector junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>emitter contact resistance</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>base contact resistivity</td>
<td>decrease 4:1</td>
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Linewidths scale as the inverse square of bandwidth because thermal constraints dominate.
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<table>
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<td>source &amp; drain contact resistance</td>
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</tr>
<tr>
<td>current density (mA/µm)</td>
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</table>

Linewidths scale as the inverse of bandwidth because fringing capacitance does not scale.
THz & nm Transistors: it’s all about the interfaces

Metal-semiconductor interfaces (Ohmic contacts):
very low resistivity

Dielectric-semiconductor interfaces (Gate dielectrics):
very high capacitance density

Transistor & IC thermal resistivity.
THz Bipolar Transistors
<table>
<thead>
<tr>
<th>Component</th>
<th>Industry</th>
<th>University 2007-9</th>
<th>University Appears Feasible</th>
<th>Maybe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitters</td>
<td>512</td>
<td>256</td>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Base</td>
<td>300</td>
<td>175</td>
<td>120</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>10</td>
<td>5</td>
<td>2.5</td>
</tr>
<tr>
<td>Collector</td>
<td>150</td>
<td>106</td>
<td>75</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>4.5</td>
<td>9</td>
<td>18</td>
<td>36</td>
</tr>
</tbody>
</table>

**Values:**
- 32 nm width
- 1 Ω·μm² access ρ
- 30 nm contact width,
- 1.25 Ω·μm² contact ρ
- 37.5 nm thick,
- 72 mA/μm² current density
- 2-2.5 V, breakdown

**Frequencies:**
- $f_t$: 370 → 1400 GHz
- $f_{max}$: 490 → 2800 GHz

**Applications:**
- Power Amplifiers: 245 → 1400 GHz
- Digital 2:1 Divider: 150 → 660 GHz

**Diagram:**
- $T_b$, $W_e$, $W_{bc}$, $T_c$
**InP DHBTs: September 2008**

![Graph showing f_max vs. f_t for various DHBT technologies.]

**Popular Metrics:**
- $f_t$ or $f_{max}$ alone
- $(f_t + f_{max}) / 2$
- $\sqrt{f_t f_{max}}$
- $(1/f_t + 1/f_{max})^{-1}$

**Much Better Metrics:**
- PAE, associated gain, mW/\mu m
- $F_{min}$, associated gain, digital
  - $f_{clock}$, hence
  - $(C_{cb} \Delta V / I_c)$,
  - $(R_{ex} I_c / \Delta V)$,
  - $(R_{bb} I_c / \Delta V)$,
  - $(\tau_b + \tau_c)$

*Updated Sept. 2008*
### Ohmic Contacts Good Enough for 3 THz Transistors

64 nm (2.0 THz) HBT needs $\sim 2 \ \Omega \cdot \mu m^2$ contact resistivities

32 nm (2.8 THz) HBT needs $\sim 1 \ \Omega \cdot \mu m^2$

| Contacts to N-InGaAs* | Mo | MBE in-situ | 0.3 (+/- 0.3) $\Omega \cdot \mu m^2$
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>TiW</td>
<td>ex-situ</td>
<td>~1 to 2 $\Omega \cdot \mu m^2$</td>
<td></td>
</tr>
</tbody>
</table>

| Contacts to P-InGaAs | Mo | MBE in-situ | below 2.5 $\Omega \cdot \mu m^2$
<table>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Pd/...</td>
<td>ex-situ</td>
<td>0.36 (+/- 0.3) $\Omega \cdot \mu m^2$</td>
<td></td>
</tr>
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*measured emitter resistance remains higher than that of contacts.*
THz HBTs: MOSFET-like Processes for 64, 32 nm Nodes

emitter | metal | planarize | etch | pattern

Planarization boundary

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nm MOSFETs
**FET Scaling Laws**

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What do we do if gate dielectric cannot be further scaled?
III-V MOSFETs for VLSI

What is it?
MOSFET with an InGaAs channel

Why do it?
low electron effective mass → higher electron velocity
more current, less charge at a given insulator thickness & gate length
very low access resistance

What are the problems?
low electron effective mass → constraints on scaling!
must grow high-K on InGaAs, must grow InGaAs on Si

Synopsis
III-V MOSFET might win... if Si gate dielectric cannot scale below 0.5 nm
THz Field-Effect Transistors (THz HEMTs)
### FET Scaling Laws

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*InGaAs HEMTs are best for mm-wave low-noise receivers... but there are difficulties in improving them further.*

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Why HEMTs are Hard to Improve

1\textsuperscript{st} challenge with HEMTs: reducing access resistance

low electron density under gate recess $\rightarrow$ limits current
gate barrier lies under S/D contacts $\rightarrow$ resistance

2\textsuperscript{nd} challenge with HEMTs: low gate barrier

high tunneling currents with thin barrier
high emission currents with high electron density

\textbf{III-V MOSFETs do not face these scaling challenges}
**InGaAs MOSFETs as THz Low-Noise Amplifiers**

### Why?

**Much lower access resistance in S/D regions**

**Higher gate barrier → higher feasible electron density in channel**

**Higher gate barrier → gate dielectric can be made thinner**

### Estimated Performance (?)

**2 THz cutoff frequencies at 32 nm gate length**
VSLI for mm-wave & sub-mm-wave systems
Billions of 700-GHz Transistors → Imaging & Arrays

65 nm CMOS: ~5 dB gain @ 200 GHz

22 nm will be much faster yet.

What can you do with a few billion 700-GHz transistors?

Build Transmitter / Receiver Arrays

100's or 1000's of transmitters or receivers
...on < 1 cm² IC area
...operating at 100-500 GHz.
Billions of 700-GHz Transistors → Imaging & Arrays

Arrays for point-point radio links:

\[ \text{bit rate} \cdot \text{distance}^2 \propto (\# \text{array elements})^2 \cdot \text{wavelength}^2 \]

Arrays for (sub)-mm-wave imaging:

\[ \# \text{resolvable pixels} = \# \text{array elements} \]

Arrays for Spatial-Division-Multiplexing Networks:

\[ \# \text{independent beams} = \# \text{array elements} \leq \frac{4 \cdot \text{array area}}{\text{wavelength}^2} \]
It's a great time to be working on electronics!

Device scaling (Moore's Law) is not yet over.

Challenges in scaling:
  contacts, dielectrics, heat

Multi-THz transistors:
  for systems at very high frequencies
  for better performance at moderate frequencies

Vast #s of THz transistors
  complex systems
  new applications.... imaging, radio, and more