A 45 PS TIME-INTERVAL COUNTER BOARD WITH A PCI INTERFACE

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Abstract

This paper describes the design and test results of a precise time-interval and frequency counter board with PCI interface. The counter utilizes two two-stage interpolators that provide 45 ps resolution (LSB) over the measurement range from 0 to 4400 s. The frequency is measured from 0.3 mHz to 3.5 GHz with the use of reciprocal method with two modes of operation. The counter board can also be used for estimation of frequency stability and frequency comparison of clock sources of the same nominal frequency. The main units of the counter are integrated in an FPGA device. The built-in digital clock manager units are used for frequency synthesis and for generation of the four-phase clock used in the first interpolation stage. The fast arithmetic carry chains are used as high-resolution tapped delay lines in the second interpolation stage. The internal FIFO memory allows one to decrease the dead time of the counter and achieve the maximum measurement rate of 5×10^6 measurements per second. The counter board is supported by the dedicated software, providing comprehensive control, diagnostics, and statistical data processing.

INTRODUCTION

Precise time-interval and frequency measurements are widely used in timekeeping and navigation systems, laser rangefinders, high energy physics, and test instrumentation. The desktop time and frequency counters are usually big and expensive, and have limited capability of processing and visualization of the measurement data. When used in an automatic measurement system, they have to be computer-controlled via wire or RF interface. But the precise counters made as computer boards offer advanced data processing, are lower in cost, and may be easily incorporated into any measurement system based on a typical computer. In this paper, we describe the design, test results, and specifications of a new time- interval and frequency counter board with 45 ps timing resolution. This design follows the former boards described earlier **[1-3]**. The main functional units of the counter are designed in the reprogrammable FPGA (*Field Programmable Gate Array*) device. The counter board is controlled by dedicated software operating in the Windows environment.

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14. ABSTRACT
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DESIGN

Figure 1 depicts the general architecture of the counter board. The main units of the counter for time-interval and frequency measurements, counter control, data collection, and frequency synthesis are integrated in the FPGA device from Spartan 3 family (*Xilinx*).

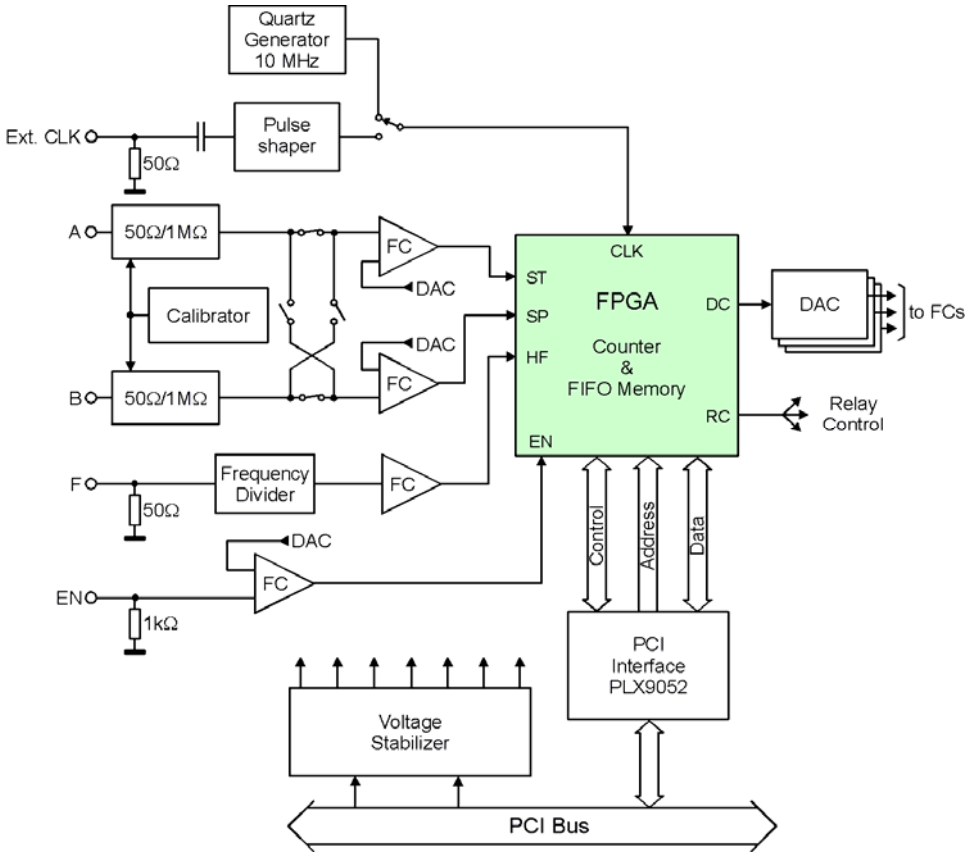

Fig. 1. Simplified block diagram of the counter board.

The counter board measures time intervals between the pulses START and STOP appearing consecutively at the inputs A (B) and B (A). The input threshold levels can be preset with the use of control software. Three Digital-to-Analog Converters (DAC) with internal data registers are utilized for this purpose. The input pulses are shaped by the fast comparators (FC) and fed to the inputs ST and SP.

The input channels A and B used for time-interval measurements are also used in the calibration procedure. The main goals of the procedure are identification of transfer characteristics of two two-stage interpolators integrated in FPGA and calculation of the input time offset between the channels A and B. For this purpose, the onboard calibrator generates pulses asynchronous with regard to the reference clock and the pulses are simultaneously applied to the A and B inputs via respective relays. The A and B inputs can also be used for direct frequency measurement up to 150 MHz. The fast frequency divider at the F input rises this limit up to 3.5 GHz.

The EN input allows for arming the input A or B. The enable signal can be generated either externally or internally after a delay preset on the virtual control panel. To enable the STOP pulse (at the B or A input), an internal programmable counter is utilized to set the required disabling time (after the START signal has been accepted) from 20 ns up to about 20 s.

The onboard 10 MHz quartz generator is the default clock reference. When using an external reference, the input signal is processed by the fast pulse shaper. The use of an external atomic clock may improve the accuracy of the counter, especially when measuring longer time intervals.

Figure 2 shows the external view of the counter board T2400. The FPGA device is located in the center and below is the PCI interface chip (PLX9052).

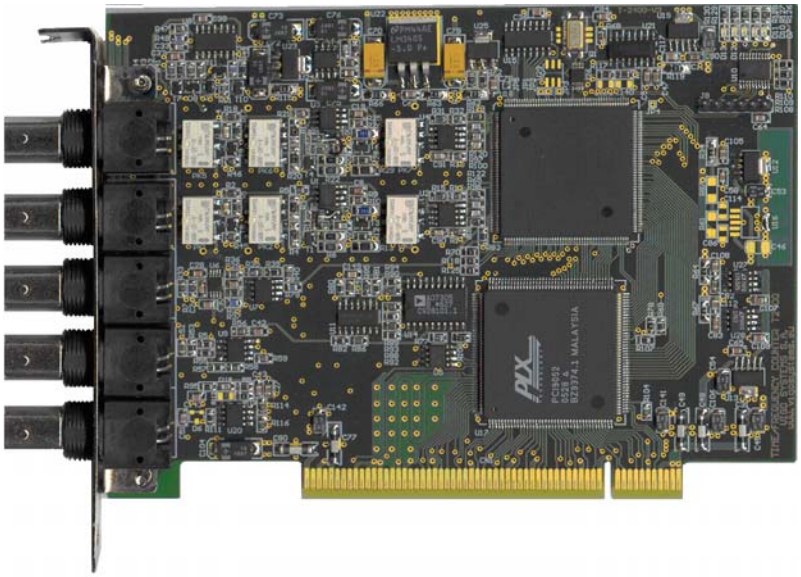

Fig. 2. External view of the counter board.

The FPGA device contains two two-stage interpolators, a frequency synthesizer, a four-phase clock generator, a binary counter with synchronizer, two Look-Up Tables (LUT), and a FIFO memory (Fig. 3).

Following the principle of the two-stage interpolation method **[3-5]**, the START interpolator measures the time interval between the START input pulse and the nearest active edge of the master clock in two steps. The first interpolation stage selects a single output of the four-phase clock. Then, in the second stage, a short time interval between the START pulse and the edge of the four-phase clock at the selected output is precisely coded with the aid of a tapped delay line formed by the fast arithmetic carry chain in FPGA device. A similar operation is performed in the STOP interpolator with reference to the STOP input pulse. The output data from both interpolators are encoded by the related look-up tables, where the nonlinearities of transfer characteristics are corrected on-the-fly. The content of the LUTs is stored during the calibration process.

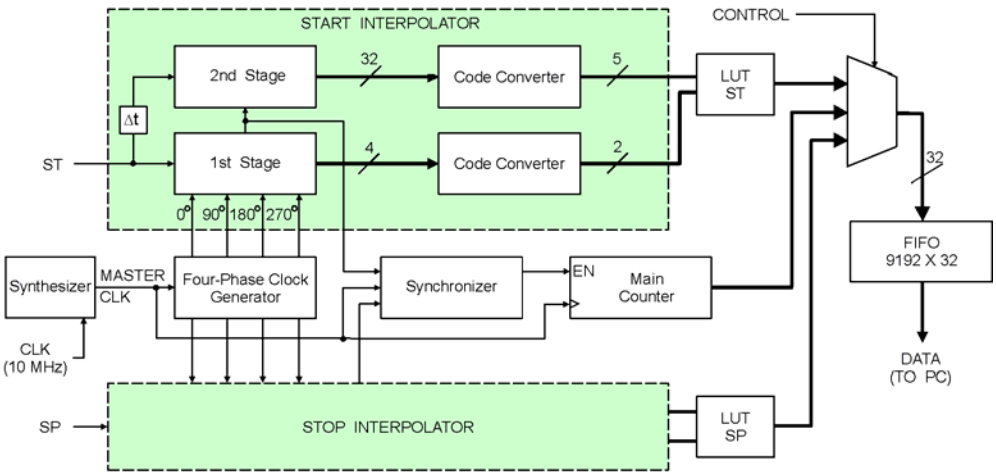

Fig. 3. Internal architecture of the integrated time-interval counter.

The 40-bit binary main counter is utilized for counting active edges of the master clock with a coarse resolution equal to a single clock period. The master clock is synthesized with the use of a Digital Clock Manager (DCM) unit integrated in the FPGA device. Two other DCMs are used to generate the four-phase clock used in the first stage of both interpolators.

To minimize the dead time between successive measurements, a FIFO memory module has been designed in the FPGA device. It allows increasing the maximum measurement rate up to 5 million measurements per second (when measuring the zero time interval).

Figure 4 shows a screen snapshot of the virtual front panel of the counter. The panel with all control tools and display was designed in software for the Windows environment.

The main objective of the virtual panel is the selection of measurement mode, setting its parameters and displaying the measurement results. The current state of the counter and the stage of measurement process can be easily identified on the screen. The measurement data can be saved in a text file and can be further processed to show, for example, a statistical histogram. The users who want to write their own applications for Windows operating system using C, C++, Delphi, or LabView may utilize the dedicated dynamic-link library (DLL) file.

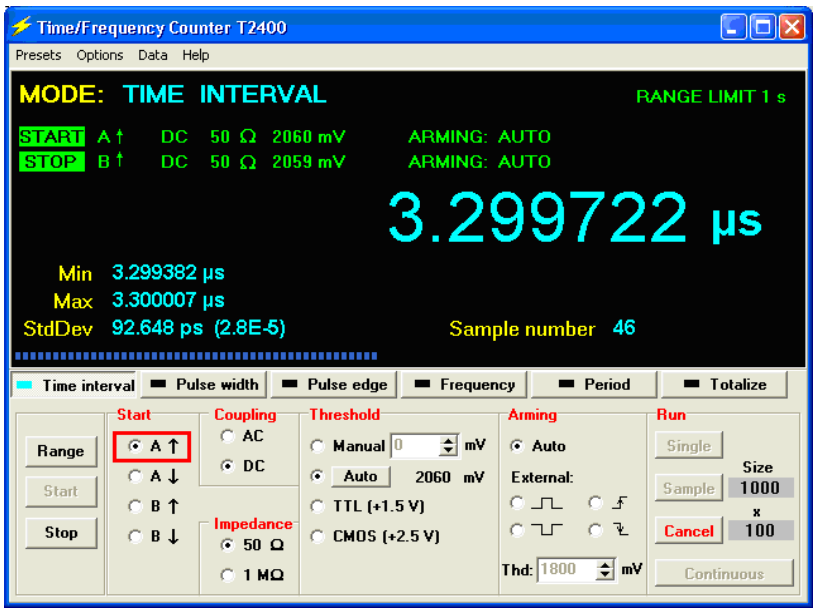

Fig. 4. An example of the virtual front panel of the counter board.

OPERATION MODES

The counter board can operate either in calibration mode or in one of two main measurement modes: time- interval or frequency measurement. The calibration is performed by two consecutive procedures. In the first one, the transfer characteristics of both integrated interpolators are identified. They are stored in two LUTs in the FPGA device and used for compensation of the interpolators' nonlinearity in measurement modes. The second calibration procedure calculates the time offset between the inputs A and B. Both calibration procedures are completed in about 6 s. Since the temperature of the FPGA counter may vary during a long measurement session, especially just after the cold start of the counter, the transfer characteristics of both interpolators may also vary. To keep the content of LUTs accurate, the calibration should be repeated periodically. A time interval between successive calibration procedures can be set manually by the user or can be determined automatically by the control software according to the drift of calibration data.

The signal frequency f_s is measured with the use of the reciprocal method by measuring the time interval T, consisting of a known integer number n of signal periods T_s ($T = nT_s$), calculating the duration of a single period ($T_s = T / n$), and calculating its reciprocal ($f_s = 1/T_s$) **[7]**. Two modes of the reciprocal method are employed or the number n of periods forming the measured time interval T can be selected in two ways. In the first (classical) mode, the gate time is selected to count n consecutive periods T_s of the tested signal. The number n is not preset and it has to be counted with the use of an additional counter. In the other mode, an exact number n of periods T_s can be selected, but the gate duration is then not preset.

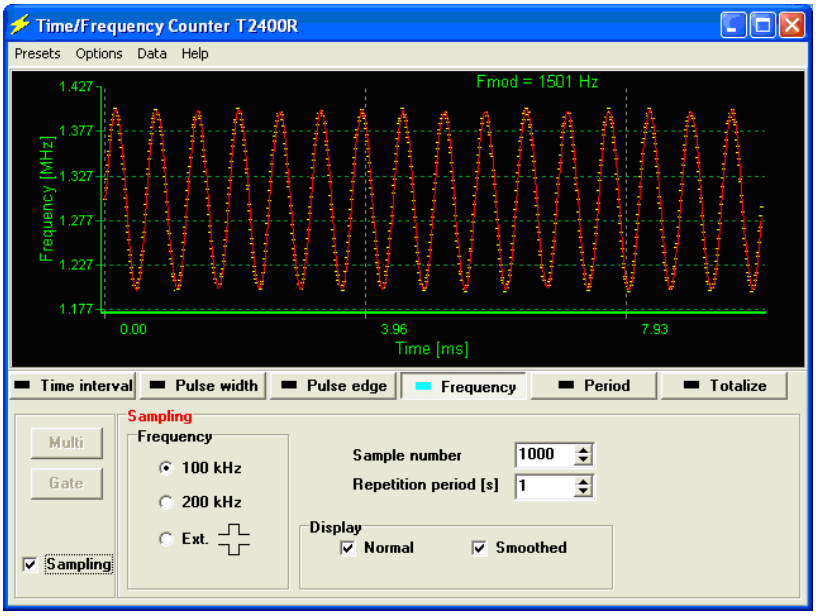

Fig. 5. Frequency measurements in the Sampling mode.

Thanks to the short dead time of the counter, the frequency measurements can be repeated at a high rate. It allows for observation of how the measured frequency varies in time. For example, it can be used for discovering a frequency modulation (needed or not) of the measured signal. The sampling can be performed with an internally generated frequency (100 kHz or 200 kHz) or using an external frequency source. The obtained values of sampled frequency are displayed on the screen (Fig. 5). To form a smoothed waveform, they can be approximated with the use of a three-point approximation. The number of samples and the repetition period are settable.

The counter allows also for the comparison of frequency of two signals having the same nominal frequency. The procedure consists of six measurement cycles separated by a user-selected time interval. In every cycle, the time lag T_i (i = 0..5) between two nearest slopes of the input signals is measured and the difference $T_i - T_{i-1}$ is calculated. For example, for the time stamps t_1 and t_2 and the corresponding time lags T_1 and T_2, the error is calculated as

$$\frac{\Delta f}{f} = \frac{T_2 - T_1}{t_2 - t_1}$$

Then the changes of this error in the following steps may be examined. The two tested signals should be attached to inputs A and B of the counter.

The frequency measurements can also be used for evaluation of the short-term stability of high-quality clock sources. The Allan variance can be calculated for the following time gates: 0.01 s, 0.1 s, 1 s, and 10 s. Since the designed counter has a dead time equal to 200 ns, the time distance between consecutive samples is relatively short and, for the most typical time gate τ = 1 s, the ratio (dead time)/τ is as low as 2×10^{-10}.

TEST RESULTS

The standard uncertainty (standard deviation) of time-interval measurement depends mainly on (1) the quantization step or resolution (LSB – Least Significant Bit), (2) the nonlinearity of two interpolators contained in the FPGA device on the board, and–of course–(3) on the jitter of the measured time interval. The quantization contribution is relatively small, because the time intervals measured by each embedded interpolator have a uniform probability distribution of the quantization error within the range (0, LSB), where LSB ≅ 45 ps. This is true when the input START and STOP pulses are asynchronous or are not statistically correlated in time with the reference clock of the counter board. Such a condition is usually met in typical applications. Then the quantization uncertainty caused by a single interpolator is expressed by the standard deviation of the related uniform distribution, or $s_{qs} = \text{LSB}/\sqrt{12} \cong 0.3$ LSB. When the measured intervals are not ideally constant, but are randomly distributed within LSB, the quantization uncertainty created by two interpolators contained in the counter can be roughly approximated **[4]** as $s_q = \sqrt{2}\, s_{qs} \cong 0.41$ LSB $\cong 18.5$ ps. When the intervals are constant, then the standard deviation can reach the maximum value $s_{q\,\max} = 0.5$ LSB = 22.5 ps and the *average* standard deviation is $s_{q\,\text{av}} = \pi$ LSB/8 ≅ 0.39 LSB ≅ 17.5 ps. As a general rule, we may accept the approximated formula $s_q \cong 0.4$ LSB and then $s_q \cong 18$ ps.

To determine the standard uncertainty of the counter board within a wide measurement range, we measured time intervals generated by the delay generator DG535 (*Stanford Research Systems*) driven by the external 10 MHz Rubidium Frequency Standard FS725 (SRS). The time intervals were measured by the counter board using either the onboard 10 MHz quartz generator or the external 10 MHz Standard FS725. The obtained standard uncertainties for both cases are shown in Fig. 6.

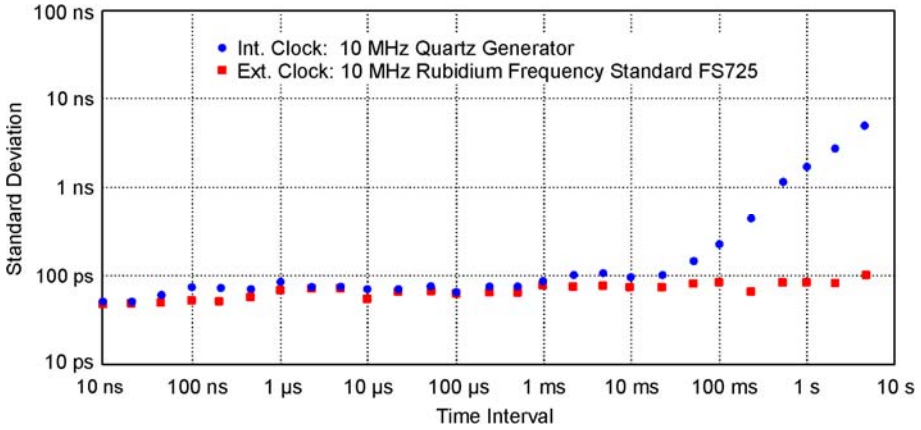

Fig. 6. Standard uncertainty of time intervals measured by the counter board using the onboard quartz generator or the external 10 MHz Standard FS725.

When the onboard clock source is used, the standard deviation does not exceed 90 ps RMS for time intervals up to 1 ms. For time intervals longer than about 10 ms, the measurement uncertainty of the counter becomes more influenced by the short-term instability of the reference clock. If an external highly stable clock source is used, the standard deviation is below 90 ps RMS for time intervals up to 2 s.

The jitter of time intervals produced by the DG535 was examined with the aid of two high-quality digital oscilloscopes having the jitter noise floor at about 1 ps. Then the jitter contributed by the DG535 has been subtracted (RMS) from the results displayed by the counter. The test results shown in Fig. 6 have been obtained after such a correction and provide reliable information about the counter accuracy.

The mode of comparison of frequency stability was tested with the use of two clock sources: the Rubidium Frequency Standard FS725 (*Stanford Research Systems*) and the temperature-stabilized quartz generator used in the counter SR620 (*Stanford Research Systems*). Both sources generate signals of nominal 10 MHz frequency. In the first test, we applied a highly stable signal from FS725 to both measurement inputs of the counter (A and B), and the same signal was also used as the external reference clock for the counter board. In this way, we estimated the ultimate noise floor of the counter board. The results of six tests made six times every 20 seconds are shown in Fig. 7 (left). The measurements were then repeated several times and the frequency difference did not exceed the level of 10^{-12}.

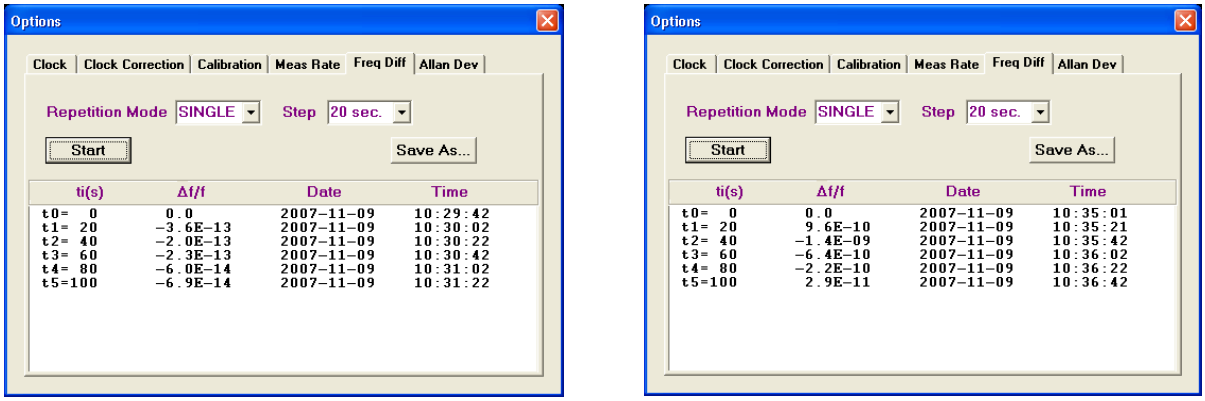

Fig. 7. Example of the frequency comparison test. Left: A = FS725, B = FS725; right: A = FS725, B = SR620.

In the second test, the internal quartz generator of the counter SR620 was compared with the FS725 clock used as a reference source. Since the quartz generator used in SR620 is characterized by moderate short-term frequency fluctuations, the compared frequencies differ much more than previously and reach -1.4 $\times 10^{-9}$ for measurement taken over 40 s. In general, results of such tests made with the use of a stable reference clock and an unknown source can be used for calibration of the latter.

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