FIELD PROGRAMMABLE GATE ARRAY CONTROL OF POWER SYSTEMS IN GRADUATE STUDENT LABORATORIES

by

Joseph E. O’Connor

March 2008

Thesis Advisor: Alexander Julian
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The Department of Electrical and Computer Engineering at the Naval Postgraduate School (NPS) continuously develops new design and education resources for students. One area of focus for students in the Power Electronics curriculum track is the development of a design center that explores Field Programmable Gate Array (FPGA) control of power electronics. Utilizing Mathworks® and XILINX® software to interface the FPGA with power converters, students gain experience with digital design, simulation, and hardware testing. This thesis focuses on the design, implementation and testing of a Student Design Center (SDC) employing an FPGA based digital controller. This thesis especially concentrates on the hardware interface between the FPGA and the power electronics and the development of laboratory procedures for students utilizing the design center.
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ABSTRACT

The Department of Electrical and Computer Engineering at the Naval Postgraduate School (NPS) continuously develops new design and education resources for students. One area of focus for students in the Power Electronics curriculum track is the development of a design center that explores Field Programmable Gate Array (FPGA) control of power electronics. Utilizing Mathworks® and XILINX® software to interface the FPGA with a voltage source converter (VSC), students gain experience with digital design, simulation, and hardware testing. This thesis focuses on the design, implementation and testing of a Student Design Center (SDC) employing an FPGA based digital controller. This thesis especially concentrates on the hardware interface between the FPGA and the power electronics and the development of laboratory procedures for students utilizing the design center.
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<tbody>
<tr>
<td>A</td>
<td>Amps</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>A/D</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>BNC</td>
<td>Bayonet Nut Connector</td>
</tr>
<tr>
<td>BOM</td>
<td>Bill of Materials</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial-Off-The-Shelf</td>
</tr>
<tr>
<td>dB</td>
<td>Decibel</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>FPD</td>
<td>Field Programmable Device</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>kHz</td>
<td>Kilohertz</td>
</tr>
<tr>
<td>LUT</td>
<td>Lookup Table</td>
</tr>
<tr>
<td>LPF</td>
<td>Lowpass Filter</td>
</tr>
<tr>
<td>NPS</td>
<td>Naval Postgraduate School</td>
</tr>
<tr>
<td>OPAMP</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>SDC</td>
<td>Student Design Center</td>
</tr>
<tr>
<td>SOP</td>
<td>Standard Operating Procedure</td>
</tr>
<tr>
<td>SVM</td>
<td>Space Vector Modulation</td>
</tr>
<tr>
<td>V</td>
<td>Volts</td>
</tr>
<tr>
<td>VHDL</td>
<td>Very-High-Speed-Integrated-Circuit Hardware</td>
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<td>VSC</td>
<td>Voltage Source Converter</td>
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EXECUTIVE SUMMARY

The Student Design Center (SDC) at the Naval Postgraduate School (NPS) Electrical Engineering Department (Solid State Microelectronics and Power Systems track) was created to expose students to the process of basic solid state power design and control, also known as "digital power". The SDC enables students to make accurate predictions of voltage source converter (VSC) behavior using software simulation; furthermore, the SDC allows students to test their simulations on the actual hardware to verify results.

The primary components of the SDC architecture are a Field Programmable Gate Array (FPGA), a VSC (augmented by other commercial, off-the-shelf components for various laboratories), a circuit board interface between the FPGA and the VSC, a circuit board interface between the FPGA and the power source, and a desktop computer. The design center is shown in Figure 1.
The SDC utilizes Mathworks' Simulink® software to generate hardware control simulations and run virtual experiments on VSCs and other power systems. XILINX® software produces Verilog Hardware Description Language (VHDL) code to interface the FPGA with hardware components; hence, basic knowledge of programming is required, but prior experience with VHDL coding is unnecessary.

The Semikron® VSC used in the SDC employs three parallel-connected half-bridges with an IGBT-diode brake for protection. Custom interface Printed Circuit Boards (PCBs) were designed, constructed, and tested to interface the FPGA with the VSC and the switching power source. The FPGA controls two analog-to-digital (A/D) converters for sampling VSC load currents and voltages. The FPGA was programmed with XILINX® software (embedded in the Simulink® model) and used to drive the VSC. The PCBs were thoroughly tested for compatibility and faults, and a digital low pass filter was designed and installed to reduce high frequency interference in the sampled signals. Four laboratory systems (buck converter, boost converter, H-bridge DC/AC converter and a diode-rectifier) were built to augment the VSC for various laboratories used in graduate power electronics courses.

The main thrust of this thesis was the exploration of the interface between the FPGA and the VSC and the actual construction and testing of the SDC. Emphasis was placed on the design, layout, and testing of each PCB as well as techniques used to minimize or eliminate adverse performance due to electromagnetic interference.
A secondary objective was to present the reader with a background and overview of the hardware and software used in the SDC including a brief description of current FPGA technology and its wide variety of applications in academic settings. A detailed derivation of Space Vector Modulation (SVM) was accomplished since it is the VSC control technique used in power electronics laboratories at NPS.

Finally, the last objective was to develop a Standard Operating Procedure (SOP) for laboratories conducted in the SDC in order to provide students with a better understanding of design flow prior to execution and to supplement laboratory assignments as a resource for frequently asked questions.
ACKNOWLEDGMENTS

I would like to express my sincere appreciation to the faculty and staff of the Naval Postgraduate School for their dedication to the ideals of higher education. You make it possible for professional military men and women to pursue their academic goals while supporting their family and this great country.

Thank you to Professor Julian for his genuine outlook on my educational experience and for his common-sense approach to life in general. Working side-by-side with him was an honor and privilege. I hope his attitude towards teaching and mentoring students is recognized by the department and used as a template for future hires.

Special thanks to the laboratory technicians James Calusdian, Jeff Knight, Warren Rogers, and Petty Officer McGill who were always ready and willing to help.

Thank you to my parents, Thomas and Kathleen O'Connor, for instilling a good work ethic and a passion for "figuring things out."

Finally, and most importantly, thank you to my wife, Kelly, and to my children. Without you I would not be the man and Marine I am today. You give my life meaning and purpose, and I hope I never let you down.
I. INTRODUCTION

A. BACKGROUND

The Student Design Center (SDC) for the Naval Postgraduate School Electrical Engineering Department (Solid State Microelectronics and Power Systems track) was created for the purpose of exposing students to the process of transforming performance requirements into basic design. The center exposes students to basic power electronics design, enables accurate behavior predictions using software simulation, and allows students to test their simulations on the actual hardware to verify results. Students enrolled in power electronics courses complete assigned laboratories and become thoroughly indoctrinated in the design simulation and testing process. Each laboratory strives to give students practical problems in a real-world environment while preparing them for future study in product design and control [1].

The primary components of the SDC architecture are a Field Programmable Gate Array (FPGA); a voltage source converter (augmented by other commercial, off-the-shelf equipment for various laboratories); a Printed Circuit Board (PCB) interface between the FPGA and the VSC; a PCB interface between the FPGA and the power source; and a desktop computer. Students use Mathworks' Simulink® software to generate hardware control simulations and run virtual experiments on VSCs and other power systems. XILINX® software produces Verilog Hardware Description Language (VHDL) code to interface the FPGA with hardware
components; hence, basic knowledge of programming is required, but prior experience with VHDL coding is unnecessary.

B. RESEARCH OBJECTIVES

The main thrust of this thesis is the exploration of the interface between the FPGA with the VSC, and the FPGA with the switching power source. Emphasis is placed on the design, layout, and testing of each interface PCB as well as techniques used to minimize or eliminate adverse performance due electromagnetic interference.

A secondary objective is to present the reader with a background and overview of the hardware and software used in the SDC, present a brief overview of current FPGA technology and its wide variety of applications in academic settings, and develop the voltage conversion technique used in Power Electronics laboratories.

Finally, a Standard Operating Procedure (SOP) is developed to provide graduate students with a better understanding of design flow prior to executing experiments. The SOP is intended to supplement laboratory assignments as a resource for frequently asked questions.

C. APPROACH

The equipment used to build the SDC included a Semikron® VSC employing three parallel-connected half-bridges with an Insulated Gate Bipolar Transistor (IGBT) diode brake for protection; a MEMEC™ Virtex-4™ Development Board containing a XILINX® FPGA; and a stand-alone personal computer workstation incorporating a Pentium® processor. Custom interface PCBs were designed, constructed, and
tested to interface the FPGA with the VSC, and the FPGA with the switching power source. The analog signal interface PCB included an output control for the VSC and two analog-to-digital (A/D) converters for detecting load currents and voltages. The FPGA was programmed with XILINX® software (imbedded in the Simulink® model) and used to drive the VSC. The PCB was thoroughly tested for compatibility and faults [2]. A digital low pass filter was designed to reduce high frequency interference from the converted signals. Four laboratory systems (buck converter, boost converter, H-bridge DC/AC converter and a diode-rectifier) were built to augment the VSC for various laboratories used in graduate power electronics courses. Finally, the SDC SOP was developed and implemented.

D. RELATED WORK

The subject of FPGA based learning in graduate laboratories has received considerable attention in literature. Iowa State University, the University of Vigo (Spain) and the University of Alabama, among others, have instituted laboratories or capstone design courses combining hardware and software tools to facilitate FPGA learning for students with a basic knowledge of digital electronics and VHDL [[1], [3], [4]]. FPGA based learning is not just limited to digital power applications, but may include control theory application and robotics as well. For example, the University of Alabama's capstone design course focuses on the design, implementation and testing of an FPGA-based robotic vehicle capable of performing a number of competition specific tasks [3]. Many universities
around the world are recognizing the value, both monetary and educational, of incorporating FPGA based learning in their academic institutions.

E. THESIS ORGANIZATION

- Chapter I introduces research goals and presents the organization of the thesis.
- Chapter II presents the SDC's hardware and software, gives background information on VSC control principles, and covers the computer aided design (CAD) layout of the SDC.
- Chapter III explores the design, construction, and testing of the analog signal interface PCB and power interface PCB.
- Chapter IV addresses conclusions and future research opportunities.
- Appendix A provides information on the XILINX® Virtex-4™ Development Board.
- Appendix B contains PCB schematics and the Virtex-4™ Development Board's bill of materials (BOM).
- Appendix C provides information on the SEMITEACH® VSC.

F. CHAPTER SUMMARY

This chapter gave a brief introduction of SDC objectives, research goals, and the approach taken to meet those goals. It concluded with the organization of this thesis. Chapter II introduces the reader to the hardware
and software used in the SDC, presents a background in FPGA technology, and discusses the voltage conversion technique used in Power Electronics laboratories.
II. STUDENT DESIGN CENTER OVERVIEW

A. FIELD PROGRAMMABLE GATE ARRAY

1. Overview

A Field Programmable Device (FPD) is a general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize different designs. Programming of such a device usually involves interfacing the device with specially designed programming software [5]. An FPGA is a semiconductor device containing programmable logic components and programmable interconnects. The programmable logic components can be programmed to duplicate the functionality of basic logic gates or more complex combination functions such as decoders and simple mathematical functions [6]. A major advantage of this technology is that FPGAs can execute codes in parallel whereas Digital Signal Processors (DSPs) execute codes in series. Hence, FPGA's do not have to "store" as much data as DSPs, and the need for large amounts of Random Access Memory (RAM) degrades significantly [7]. Another advantage of using FPGAs is their ability to work with whatever wordlength the programmer chooses. Whereas DSP processors must be selected to handle the longest wordlength that occurs in the code (thereby reducing efficiency when processing shorter wordlengths) FPGAs allow greater flexibility and efficiency by utilizing the smallest necessary wordlengths [8].
2. SDC FPGA

XILINX®, a leading manufacturer of FPGA's, primarily builds array-based circuits. These circuits incorporate chips comprised of two dimensional arrays of logic blocks that can be interconnected via horizontal and vertical routing channels [8]. An example of a generic, two-dimensional FPGA architecture is shown in Figure 2.

![FPGA Architecture](image)

Figure 2. FPGA Architecture [From [8]].

The key difference between an FPGA and a "gate array" is that the former can be reprogrammed in the "field" since the logic program is changeable. Furthermore, whereas early gate arrays were composed of NAND gates, FPGA's are a carefully balanced selection of multi-input logic, flipflops, multiplexors and memory [8]. A typical layout for an FPGA is shown in Figure 3.
For the XILINX® FPGA used in this thesis, each logic block references Look-Up Tables (LUTs), which are small, one-bit wide memory arrays. The LUT input is composed of address lines while the output is a one-bit output of the memory. A LUT with "K" inputs corresponds to a "2K x 1" bit memory and can realize any logic function of its "K" inputs by programming the logic function’s table directly into the memory [5]. FPGA's provide an excellent alternative for applications that require flexibility for various applications while avoiding the extra cost of multiple, hard-wired circuit boards. The SDC demands such flexibility since various design criteria are presented to students and the need to reprogram the board is essential.

For this thesis, a XILINX® Virtex-4™ Development Board incorporating a XC4VLX25-10SF363 FPGA was utilized and is shown in Figure 4.
The Virtex-4™ was designed as a user friendly platform for prototyping and verifying designs. This concept is a central requirement for the SDC. A high-level block diagram of the Virtex-4™ Development Board is shown in Figure 5. A complete description of each board subsection is provided in a condensed form of the Virtex-4™ user's guide found in Appendix B.
The Virtex-4™ Development Board provides 64MB of DDR SDRAM memory (32Mx16). The clock generation section of the board provides all necessary clocks for the I/O devices located on the board as well as the random access memory. An on-board 500MHz oscillator provides the system clock input to the XILINX® XC4VLX25-10SF363 FPGA; however, the SDC uses only a fraction of this clock speed. In addition to the clock input, a socket is provided on the board that can be used to provide a single-ended clock input to the FPGA via an 8- or 4-pin oscillator. The board provides a
10/100 Ethernet port for network connection and an 8-bit interface to a 2x16 LCD panel. The board also provides four user push button switches allowing an active low signal to be generated when a given switch is pressed. These switches can be remotely toggled using ChipScope™ Pro software (addressed later in this chapter). A JTAG connector is used as a port to load the software from a desktop computer, and the 5.0V connector pin is used to supply the main power to the card. The board has two interface connectors that provide easy access to the PCB interface [9]. An overview of the Virtex-4™ Development Board's layout is shown in Figure 6.

![Virtex-4™ Development Board Layout](image)

**Figure 6.** Virtex-4™ Development Board Layout [From [10]].

B. VOLTAGE SOURCE CONVERTER AND SPACE VECTOR MODULATION

The VSC used in the SDC is a three-phase, rectifier/converter specially equipped to allow students visualization of every part. The VSC is contained inside an external interface for safety and is produced by
Semikron® as an educational demonstrator. A photo of the converter is shown in Figure 7. The converter's data sheet is listed in Appendix C [11].

Figure 7. SEMITEACH® Voltage Source Converter [From [11]].

The basic schematic of the VSC is shown in Figure 8.

Figure 8. SEMITEACH® VSC Schematic [From [11]].

Controlled three phase (or single phase) output of the VSC can be obtained by a number of methods, but this thesis
adopted the Space Vector Modulation (SVM) model approach since it was utilized in existing laboratories [[12] and [13]]. SVM utilizes voltage commands assigned as "q" and "d" variables from the "qd" reference frame. The reference frame contained in the SVM hexagon is show in Figure 9.

![Space Vector Modulation Hexagon](image)

Figure 9. Space Vector Modulation Hexagon [From [12]].

The derivation and transformation below is an excerpt taken from [12] with variables adopted from the simple converter schematic shown in Figure 10.

![Simple Converter Schematic](image)

Figure 10. Simple Converter Schematic [From [12]].
The modulation indexes are described as $q$-axis and $d$-axis voltages in the stationary reference frame. The SVM hexagon maps the $qd$ voltages for each of the eight possible switching states (zero axis in the 3rd dimension mapped to the center of the hexagon). Transformation into the $qd0$ frame is defined by [12]:

$$
K_s = \frac{2}{3} \begin{bmatrix}
1 & -1 & -1 \\
\frac{2}{\sqrt{3}} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\
\frac{-1}{2} & \frac{-1}{2} & \frac{-1}{2}
\end{bmatrix}
$$

Equation 2.1

$$
\begin{bmatrix}
v_q \\
v_d \\
v_0
\end{bmatrix} = K_s \begin{bmatrix}
v_{an} \\
v_{bn} \\
v_{cn}
\end{bmatrix}
$$

Equation 2.2

where $V_{an}$, $V_{bn}$, and $V_{cn}$ are the line-to-neutral voltages for the three phase system shown in Figure 10. For the case where $Va$ is connected to the $p$ bus and $Vb$ and $Vc$ are connected to the $n$ bus ($p$, $n$, $n$), the $qd0$ voltages are [12]:

$$
\begin{bmatrix}
v_q \\
v_d \\
v_0
\end{bmatrix} = \frac{V_{dc}}{2} K_s \begin{bmatrix}
1 \\
-1 \\
1
\end{bmatrix} = \begin{bmatrix}
\frac{2V_{dc}}{3} \\
0 \\
-\frac{V_{dc}}{6}
\end{bmatrix}
$$

Equation 2.3

Equation 2.3 also defines the length of the radii forming the corners of the hexagon, $2/3$ $Vdc$. In the case
where Va and Vb are connected to the p bus and Vc is connected to the n bus \((p,p,n)\), the \(qd0\) voltages are [12]:

\[
\begin{bmatrix}
v_d \\
v_q \\
v_0
\end{bmatrix}
= \frac{v_{dc}}{2}
K_s
\begin{bmatrix}
1 \\
1 \\
-1
\end{bmatrix}
= \begin{bmatrix}
v_{dc} \\
\frac{3}{\sqrt{3}} \\
\frac{v_{dc}}{6}
\end{bmatrix}
\]

The two states defined by Equations 2.3 and 2.4 forms the sides of Sector I. When the reference voltage is in this sector, these two states and the zero states are used to produce an output voltage that, on average, equals the reference voltage.

Now let \(T_s\) be the total switching period, and let \(T_1\) and \(T_2\) represent the amount of time spent on states \((p, n, n)\) and \((p, p, n)\) respectively. The vectors \(V_1\) and \(V_2\) are proportional to the time spent on each state [12]:

\[
v_1 = \frac{T_s}{T_1} \frac{2v_{dc}}{3}
\]

\[
v_2 = \frac{T_s}{T_2} \frac{2v_{dc}}{3}
\]

The law-of-sines can be used to find the duty cycles for each state [12]:

\[
\frac{2v^*}{\sqrt{3}} = \frac{v_1}{\sin(60^\circ - \theta)} = \frac{v_2}{\sin(\theta)}
\]

Substituting Equations 2.5 and 2.6 into Equation 2.7 yields solutions for the time spent on each state [12]:

\[
T_1 = \frac{v^* \sqrt{3}}{v_{dc}} T_s \sin(60^\circ - \theta)
\]

\[
T_2 = \frac{v^* \sqrt{3}}{v_{dc}} T_s \sin(\theta)
\]

\[16\]
The time spent on each state cannot exceed the total switching period so the modulation index ($m_i$) is between zero and one [12]:

$$m_i = \frac{v^* \sqrt{3}}{v_{dc}}, \quad 0 < m_i < 1, \quad 0 < v^* < \frac{v_{dc}}{\sqrt{3}} \quad 2.10$$

Finally, the amount of time spent in the zero state is the time remaining in the period [12]:

$$T_0 = T_s - T_1 - T_2 \quad 2.11$$

When choosing a switching method for SVM, consideration should be given to minimizing switching events and minimizing distortion. Switching patterns for each sector are shown in Figure 11. Switching states are shown on the right, and time duration is on the left.

<table>
<thead>
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<th>Sector IV</th>
<th>Sector III</th>
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<td>2</td>
<td>npp</td>
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<td>2</td>
<td>npp</td>
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<td>nnn</td>
<td>2</td>
<td>nnn</td>
<td>2</td>
<td>nnn</td>
</tr>
</tbody>
</table>

Figure 11. Switching Pattern for Each Sector [From [12]].
C. HARDWARE AND SOFTWARE

The SDC utilizes Simulink® for modeling power electronics systems and for running simulations to test designs. Simulink® enables multi-domain simulation and model-based design for dynamic systems and provides an interactive graphical environment as well as a customizable set of block libraries. Most importantly, Simulink® enables model analysis and diagnostics tools to ensure model consistency and identify modeling errors prior to hardware setup and testing [14].

XILINX® software produces VHDL code from the Simulink® model in order to program the FPGA. VHDL is the most commonly used design-entry language for field-programmable gate arrays and learning the code is not a trivial task; however, XILINX® enables the student to compile VHDL code without becoming proficient in VHDL programming. The block diagram for loading VHDL from the computer to the FPGA is shown in Figure 12.

![Software Interface Block Diagram](From [9]).

Once the VHDL code is obtained, it is converted to a netlist and verified again using XILINX® Project Navigator.
Project Navigator allows the netlist to be compiled into a form that can be directly loaded into the FPGA. It also reports on the percentage of the FPGA usage. After verification, the netlist can be fitted to the FPGA by XILINX® Impact using a process called place-and-route. The graphical interface is very easy to use by right-clicking on the icon and selecting the appropriate file to load [9].

D. SDC COMPUTER AIDED DESIGN ARCHITECTURE

A block diagram of the SDC hardware configuration including Computer Aided Design (CAD) tools, including the Semikron® power module, passive components, and measuring instruments, are shown in Figure 13.

![Figure 13. SDC Hardware Configuration [From [15]].](image)

The design process is summarized as follows: A Simulink® is developed to simulate a power system. Elements of the model internal to the FPGA are designed using the System Generator library. The rest of the system is designed using Simulink® library blocks. Once the system is modeled, VHDL code is generated for the portion of the simulation controlled by the FPGA. After the VHDL is generated, the project is loaded into ISE Foundation
software and the design is synthesized. Then the program is uploaded into the FPGA through the JTAG cable, and ChipScope™ Pro is used to communicate with the target hardware. Finally, data is downloaded from the FPGA and imported into Matlab for measurement and plotting. The CAD architecture is shown in Figure 14.

![Diagram of CAD architecture](image)

**Figure 14.** Computer Aided Design Architecture [From [15]].

The XILINX® library blocks inside the Simulink® library browser behave like other library blocks during simulation. A screen snapshot of the Simulink® library browser with the XILINX® blocks highlighted is shown in Figure 15.
Figure 15. XILINX® Blocks for Simulink® Library Browser.

Every simulation that has System Generator library blocks inside must have the System Generator block at the top level. Note the System Generator block in the Buck-Converter Laboratory model shown in Figure 16.
After the VHDL code is compiled, ISE Foundation generates project files containing the VHDL code. Menu choices are shown in Figure 17.
1. **VHDL Synthesis Using ISE Foundation**

The design is synthesized using *ISE Foundation* software by opening the project file, generating the program file, and configuring the device in *Impact*. Once synthesized, the programming file is generated and the FPGA is programmed. The ISE Foundation window is shown in Figure 18.
2. Hardware Interface Using ChipScope™ Pro

The user can remotely control the converter through the computer using ChipScope™ Pro software. ChipScope™ Pro inserts a logic analyzer, bus analyzer, and virtual I/O low-profile software core directly into the design. This allows the user to view any internal signal or node, including embedded hard or soft processors. Signals are captured at or near operating system speed and the process is limited only by the speed of the A/D converter. The data is then viewed through the programming interface and analyzed with the ChipScope™ Pro Logic Analyzer [8].
ChipScope™ Pro is opened from the ISE Foundation window. The control screen is shown in Figure 19.

![ChipScope™ Pro Window](image)

**Figure 19.** ChipScope™ Pro Window.

In order to establish communication with the hardware the user must establish communication through the JTAG Chain with the FPGA and configure the device with a ChipScope™ program. The "configure" screenshot is shown in Figure 20.

![Configure Command](image)

**Figure 20.** The “Configure” Command under the “Device” Menu.
The VIO Console allows the user to control the hardware. For example, one bit can be toggled to turn the converter on and off. The VIO Console is shown in Figure 21.

![VIO Console in ChipScope™ Pro.](image)

Figure 21. VIO Console in ChipScope™ Pro.

Now the user can remotely control the FPGA, and thus the VSC digital control process, using ChipScope™ Pro; hence, detailed analysis of input and output signals can be accomplished digitally without instruments. The user can evaluate a signal bit-by-bit if necessary, and calibration of the sampled signal can be accomplished by simply adjusting gain blocks in the Simulink® model. For this power conversion laboratories, digital calibration is an essential feature given that laboratory instruments are often out of calibration. An example of digital calibration will be expounded on in the next chapter.

E. CHAPTER SUMMARY

An overview of the hardware and software utilized in the SDC was presented with a brief background of VSC digital control. A thorough development of the SDC's CAD
process was offered as well. The next chapter covers the design, construction, and testing of the analog signal interface PCB and the power source interface PCB.
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III. PRINTED CIRCUIT BOARD DESIGN AND TESTING

A. SCHEMATIC LAYOUT AND PCB DESIGN

The main objective of this phase was to interface with the Virtex-4™ Development Board and provide power to the boards while maintaining signal clarity in the sampled signals. PCB123 software was used to prepare the board schematics for manufacture. A primary objective for the design was the elimination of circuit interference, and a thorough implementation of noise reduction techniques was necessary to attain that objective. Signal decoupling, shielding of tracks and proper ground plane layout were critical to the success of the design. A summary of steps taken to attain these goals is outlined below:

- A common-mode choke was used on the ribbon cable connecting the analog and power PCBs.

- Snap grid and default track/pad sizes were chosen to minimize signal loss and properly space key components.

- Critical tracks were identified early so that traces would not be routed too close to the digital clock and other "noisy" components.

- All traces were kept as short as possible to minimize signal loss and coupling.

- Active components drawing significant switching current were “bypassed” using capacitors across power rails. Capacitors were placed as close to
the desired component as possible. 22uF and 0.1uF capacitors were used (depending on the voltage) throughout the PCBs.

- A design rule check on the completed PCBs ensured manufacturability, circuit connectivity, and electrical clearance.

The analog signal interface PCB is shown in Figure 22. The power source interface PCB is shown Figure 23. Each board's schematic is contained in Appendix A.

Figure 22. Analog Signal Interface PCB.
Individual components were manually placed on the board, and a system check revealed a manufacture defect (short) between the +/- 15V tracks and a missing track to the fourth sampling channel operational amplifier (OPAMP). The short and track were manually repaired. A follow-up test revealed electrical continuity and proper grounding throughout the circuits. The system was powered up and tested using the computer interface.
B. MAJOR COMPONENT PACKAGING

Student safety was the top priority during the component packaging phase. All equipment was physically insulated from students while still allowing a clear view of each component for visual inspection. The final component placement is shown in Figure 24. (Note that the clear-plastic shield is tilted up for the photograph.) The final layout for the SDC is shown in Figure 25. Grounding mats were installed to prevent electrostatic discharge to sensitive hardware, and students are required to use the grounding tether when inspecting components.

Figure 24. Student Design Center System Interface.
C. ANALOG-DIGITAL CONVERSION OF FEEDBACK SIGNALS

The analog signal interface PCB contains four channels to sample circuit voltages and four channels to sample circuit currents. An AD-7864 analog-to-digital (A/D) converter operating at a 500 kHz sampling rate was dedicated to each set of channels. Sample-and-hold for each channel was conducted in series for a total sampling rate of 133kHz for each channel. This sampling rate was more than sufficient to prevent aliasing when sampling low frequency measurements typical for power electronics laboratories. A diagram illustrating the conversion time for each channel and the overall timing sequence is shown in Figure 26.
The measurements taken by the AD-7864s are displayed in ChipScope™ Pro (or a standard oscilloscope) to enable the detailed analysis of the signals. Sampled signals can be calibrated precisely by adjusting the gain of the feedback signals in the Simulink® model, thus enabling accurate representation of physical samples. An example of gain adjustment in Simulink® to enable digital calibration is shown in Figure 27.
Figure 27. Simulink® Digital Calibration of Signals [After [16]].

1. Power Requirements

The Virtex-4™ board uses 1.2V, 2.5V, 3.3V and 5V power buses, but operates from a single 5V power supply and steps the voltage down internally. The analog signal interface PCB uses a 5V and +/- 15V bus. A compact, off-the-shelf AC/DC "switching" power source was chosen for the system so that a bulkier, linear DC power source would not be required in the SDC. It was also convenient to use a DC source that would fit inside the component box to maximize laboratory safety and usable space. The main shortcoming of the switching power supply was electromagnetic emission. A switching power supply for programmable circuits creates the potential for EMI and system re-boot. The high-frequency switching within an electronic power supply can also interfere with AD sampling and system clock operation. Switching power supplies generate more EMI because they
switch large currents at very high frequencies, anywhere from 50 KHz to 1 MHz. At these high frequencies, optimal power efficiencies and smaller components can be used in the construction of the system which is why they are much smaller than linear power sources. Because of its efficiency and size, a switching power supply was the first choice for the SDC [[18] and [19]].

To be certain that the power source did not interfere with the circuit, a test of each of the eight channels was conducted utilizing a linear power source (Tektronics PS280 DC power source) and a switching source to determine the difference in noise levels. An analysis of signal output showed no significant variation in signal noise due to the switching source.

2. Conditioning of Sampled Signals

Although careful consideration was given to implementing noise reduction techniques during PCB design and construction and extensive testing was done using both linear and switching power supplies, significant interference from high frequency noise was observed in ChipScope™ Pro during testing of the sampling channels. Since the switching power supply was ruled out as the primary source of noise in the preceding section, attention was focused on the signal-to-noise ratio of the AD-7864 converters. For a 12 bit converter, noise + distortion is in the range of 74dB, which is certainly enough to effect distortion in the channels [17]; hence, there was good reason to suspect that the AD converters were the source of the noise observed in ChipScope™ Pro. Regardless of the cause, a digital Low-Pass Filter (LPF) was utilized to
filter out the unwanted high-frequency interference. The addition of a digital LPF into the Simulink® model was easily achieved [20] and [21], and the SDC's software foundation prevented the addition of a hardware LPF into the design.

A cutoff frequency for the digital LPF was selected at 5kHz which was sufficient to pass all frequencies below 1kHz without significant attenuation. The 1kHz bandwidth was adequate for SDC laboratories since it satisfied frequency analysis requirement for all planned solid state laboratories. To minimize the filter order and reduce computational burden on the simulation software and the FPGA, a large transition band was used. A 5kHz band required only a 3rd order LPF for 20dB of attenuation in the stop band. The derivation of the difference equation coefficients for a symmetric Finite Impulse Response (FIR) Butterworth filter is shown below.

$$\begin{align*}
    F_s &= \frac{24 \text{ MHz}}{170} \quad F_c = 5 \text{ kHz} \\
    F_{\text{passband}} &= 5-10\text{kHz} \quad F_{\text{stopband}} = 10\text{kHz} \\
    \theta_1 &= \omega_1 T = 2\pi \left(F_c / F_s \right) \\
    \theta_2 &= \omega_2 T = 2\pi \left(F_{\text{stopband}} / F_s \right)
\end{align*}$$

(2.12)

The prewarped analog frequencies are:

$$\begin{align*}
    \omega'_1 &= \tan \frac{\theta_1}{2} \\
    \omega'_2 &= \tan \frac{\theta_2}{2}
\end{align*}$$

(2.13)

$$\begin{align*}
    \omega'_1 &= \tan \frac{\theta_1}{2} \\
    \omega'_2 &= \tan \frac{\theta_2}{2}
\end{align*}$$

(2.14)
Translating the prewarped analog frequencies into a normalized butterworth filter gives:

\[
\begin{align*}
\omega &= \omega_1 \quad \omega_a = \frac{\omega_2}{\omega_1}
\end{align*}
\]

(2.15)

Deriving the minimum butterworth filter order gives:

\[
N = \frac{[\log(10^{-\text{MdB}/10} - 1)]}{2 \log(\omega_a)} = 2.58 \approx 3
\]

(2.16)

Hence the transfer function for the normalized butterworth filter is:

\[
H_{LP}(s) = \left[ \frac{1}{s^2 + 2s^2 + s + 1} \right]_{s=\frac{\omega}{\omega_1}}
\]

(2.17)

Utilizing the bilinear transform \( s = \frac{z - 1}{z + 1} \), substituting into \( H_{LP}(s) \), and deriving the difference equation gives:

\[
\begin{align*}
H_{LP}(z) &= \left[ H_{LP}(s) \right]_{s=\frac{z-1}{z+1}} \\
0.2450e-6 \ x(n) + 0.7349e-6 \ x(n-1) \\
+0.7349e-6 \ x(n-2) + 0.2450y(n-3) - 2.9749y(n-2) \\
+2.9500y(n-1) = 0.9752y(n)
\end{align*}
\]

(2.18)

The coefficients were verified using the Matlab "maxflat" function, and the filter was integrated in the simulation AD converter subsystem. The magnitude response of the filter is shown in Figure 28. The filter subsystem is shown in Figure 29.
The results of the filter design were dramatic. A comparison of a sampled three input signals (shown in blue) at 1kHz, 5kHz and 10kHz and their filtered counterparts (shown in green) are shown in Figure 30.
Figure 30. Original and Filtered 1kHz Signal.

Figure 31. Original and Filtered 5kHz Signal.

Figure 32. Original and Filtered 10kHz Signal.
Excellent attenuation was shown as the frequency approached the stop band and virtually all high-frequency interference was blocked.

D. CHAPTER SUMMARY

This chapter covered the analog signal interface PCB and the power source interface PCB design, construction and testing. An overview of why a switching power source was used in the SDC and techniques used to troubleshoot and reduce system noise was presented. Finally, a digital LPF was developed and implemented to eliminate EMI. Chapter III summarizes this thesis and presents topics for future research.
IV. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY

This thesis began with an overview of the SDC objectives and descriptions of the hardware and software used therein. The purpose and function of each component was explained in order to develop a working knowledge of SDC capabilities. Standard operating procedures were developed to serve as a working document for future students conducting laboratories in the SDC and to provide them with a better understanding of design flow prior to execution. The thesis expounded on the design and testing of the interface PCBs and system performance testing was done to ensure EMI from the switching power supply did not inhibit signal sampling. Finally, a lowpass filter was designed and implemented to reduce the high frequency interference on the channel signals noted in ChipScope™ Pro during testing.

B. CONCLUSIONS

The SDC is an excellent resource for digital control of power electronics design. Students gain a fundamental understanding of the advantages of FPGA digital control of power systems and digital signal analysis using ChipScope™ Pro. The SDC enables students to make accurate predictions of component behavior using software simulation and testing to verify results. The SDC can be adapted as necessary to changing technology due to its flexible FPGA foundation. New programs and ideas can be implemented without changing hardware and increasing cost. Moreover, as noted in Chapter I, the SDC is not limited to power electronics design and
control. Since three systems are available, students in other curriculums can explore the potential of FPGA design and control of other electrical systems.

C. RECOMMENDATIONS FOR FURTHER RESEARCH

There are many opportunities for research in the area of FPGA digital control of power electronics. Below are three ideas to serve as platforms for further research:

- Development of FPGA laboratories for other electrical engineering curriculum tracks.
- Redundant FPGA control of power electronics in order to improve system reliability.
- Design and Implementation of FPGA "soft-radio" systems.

The reprogrammable nature of the FPGA hardware enables a large number of programs and systems to be explored without the burden of purchasing and installing new hardware; hence, electrical engineering design, especially at the graduate level, can benefit greatly from the use of FPGA technology.
APPENDIX A: PCB SCHEMATICS AND VIRTEX-4™ BOM
<table>
<thead>
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<th>كود</th>
<th>المكون</th>
<th>الوحدة</th>
<th>الكمية</th>
<th>السعر</th>
<th>التكلفة</th>
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<tr>
<td>إلهام</td>
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<td>المكعب</td>
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<td>5555.55</td>
</tr>
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<td>202</td>
<td>شاهر</td>
<td>المتر</td>
<td>234</td>
<td>67.8</td>
<td>15555.55</td>
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<td>303</td>
<td>جان</td>
<td>المليمتر</td>
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<td>89.0</td>
<td>23333.33</td>
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<td>404</td>
<td>علي</td>
<td>المليمتر</td>
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<td>12.3</td>
<td>5555.55</td>
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<td>505</td>
<td>محمد</td>
<td>المليمتر</td>
<td>567</td>
<td>34.5</td>
<td>12345.67</td>
</tr>
</tbody>
</table>

كلمة التكلفة هي تكلفة النقل إلى موقع العمل.
A. VIRTEX-4™ DEVELOPMENT BOARD COMPONENTS

All figures and information in this appendix were excerpted verbatim from the Virtex-4™ LC Development Board user's guide. Figure numbers were changed to correspond with this thesis.

1. DDR SDRAM

The Virtex-4™ LC Development Board provides 64MB of DDR SDRAM memory (32Mx16). A high-level block diagram of the DDR SDRAM interface is shown below.

![Figure 33. DDR SDRAM Interface.](image)

2. Clock Sources

The clock generation section of the Virtex-4™ LC Development Board provides all necessary clock for the I/O devices located on the board as well as the DDR SDRAM memory. An on-board 100MHz oscillator provides the system clock input to the FPGA. In addition to the above clock input, a socket is provided on the board that can be used...
to provide a single-ended LVTTTL clock input to the FPGA via an 8 or 4-pin oscillator. The following figure shows the clock.

![Clock Sources on the Virtex-4™ board.](image)

**Figure 34.** Clock Sources on the Virtex-4™ board.

### 3. 10/100 Ethernet PHY

The Virtex-4™ LC Development Board provides a 10/100 Ethernet port for network connection. A high-level block diagram of the 10/100 Ethernet interface is shown in the figure below.
4. LCD Panel

The Virtex-4™ LC Development Board provides an 8-bit interface to a 2x16 LCD panel (MYTECH MOC-16216B-B). The following table shows the LCD interface signals.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Virtex-4 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>LCD Data Bit 0</td>
<td>T2</td>
</tr>
<tr>
<td>D1</td>
<td>LCD Data Bit 1</td>
<td>T1</td>
</tr>
<tr>
<td>D2</td>
<td>LCD Data Bit 2</td>
<td>R2</td>
</tr>
<tr>
<td>D3</td>
<td>LCD Data Bit 4</td>
<td>T3</td>
</tr>
<tr>
<td>D4</td>
<td>LCD Data Bit 4</td>
<td>R4</td>
</tr>
<tr>
<td>D5</td>
<td>LCD Data Bit 5</td>
<td>R3</td>
</tr>
<tr>
<td>D6</td>
<td>LCD Data Bit 8</td>
<td>R1</td>
</tr>
<tr>
<td>D7</td>
<td>LCD Data Bit 7</td>
<td>R5</td>
</tr>
<tr>
<td>EN</td>
<td>LCD Enable Signal</td>
<td>R6</td>
</tr>
<tr>
<td>RW</td>
<td>LCD Write Signal (this signal is connected to logic &quot;0&quot; on the Virtex-4 LC board, enabling write only cycles)</td>
<td>NA</td>
</tr>
<tr>
<td>RS</td>
<td>LCD Register Select Signal</td>
<td>T8</td>
</tr>
</tbody>
</table>

Table 1. LCD Interface Signals.
5. RS232 Interface

The Virtex-4™ LC Development Board provides an RS232 interface with RX and TX signals and jumpers for connecting the RTS and CTS signals. The following figure shows the RS232 interface to the Virtex-4™ LX25 FPGA.

![RS232 Interface Diagram]

Figure 36. RS232 Interface.

6. User DIP and PB Switches

The Virtex-4™ LC Development Board provides four user push button switches as described in the following table. An active low signal is generated when a given switch is pressed.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Virtex-4 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUSH1</td>
<td>SW5</td>
<td>B4</td>
</tr>
<tr>
<td>PUSH2</td>
<td>SW6</td>
<td>C2</td>
</tr>
<tr>
<td>PUSH3</td>
<td>SW7</td>
<td>C1</td>
</tr>
<tr>
<td>PUSH4</td>
<td>SW8</td>
<td>F2</td>
</tr>
</tbody>
</table>

Table 2. Push Button Switch Pin Assignments.
The Virtex-4™ LC Development Board provides an 8-position DIP switch as described in the following table. An active low signal is generated when a given switch is ON.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Virtex-4 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP1</td>
<td>User Switch Input 1</td>
<td>T4</td>
</tr>
<tr>
<td>DIP2</td>
<td>User Switch Input 2</td>
<td>U3</td>
</tr>
<tr>
<td>DIP3</td>
<td>User Switch Input 3</td>
<td>U4</td>
</tr>
<tr>
<td>DIP4</td>
<td>User Switch Input 4</td>
<td>V4</td>
</tr>
<tr>
<td>DIP5</td>
<td>User Switch Input 5</td>
<td>W2</td>
</tr>
<tr>
<td>DIP6</td>
<td>User Switch Input 6</td>
<td>W3</td>
</tr>
<tr>
<td>DIP7</td>
<td>User Switch Input 7</td>
<td>W4</td>
</tr>
<tr>
<td>DIP8</td>
<td>User Switch Input 8</td>
<td>Y4</td>
</tr>
</tbody>
</table>

Table 3. DIP Switch Pin Assignments.

7. User LEDs

The Virtex-4™ LC Development Board provides four user LEDs that can be turned “ON” by driving the LEDx signal to a logic “0”. The following table shows the user LEDs and their associated FPGA pin assignments.

<table>
<thead>
<tr>
<th>LED Designation</th>
<th>LED #</th>
<th>Virtex-4 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS9</td>
<td>LED1</td>
<td>M5</td>
</tr>
<tr>
<td>DS10</td>
<td>LED2</td>
<td>M3</td>
</tr>
<tr>
<td>DS11</td>
<td>LED3</td>
<td>M8</td>
</tr>
<tr>
<td>DS12</td>
<td>LED4</td>
<td>N5</td>
</tr>
</tbody>
</table>

Table 4. LED Pin Assignments.

8. User GPIO

The Virtex-4™ LC Development Board provides a general-purpose GPIO header (JP26) that consists of 6 user signals, a 3.3V power pin and a ground pin. The following table shows the GPIO pin assignments.
9. Configuration and Debug Ports

Various methods of configuration and debug support are provided on the Virtex-4™ LC Development Board to assist designers during testing and debugging of their applications. The following sections provide brief descriptions of each of these interfaces.

a. JTAG Gain

The following figure shows the JTAG chain on the Virtex-4™ LC Development Board. The XC9536XV along with a serial data flash is used to configure the FPGA.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Connector Pin #</th>
<th>Virtex-4 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_0</td>
<td>2</td>
<td>V18</td>
</tr>
<tr>
<td>GPIO_1</td>
<td>3</td>
<td>V17</td>
</tr>
<tr>
<td>GPIO_2</td>
<td>4</td>
<td>W19</td>
</tr>
<tr>
<td>GPIO_3</td>
<td>5</td>
<td>W18</td>
</tr>
<tr>
<td>GPIO_4</td>
<td>6</td>
<td>W17</td>
</tr>
<tr>
<td>GPIO_5</td>
<td>7</td>
<td>Y17</td>
</tr>
<tr>
<td>3.3V</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>GND</td>
<td>8</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 5. GPIO Pin Assignments.
Figure 37. Vitex-4 LC Development Board JTAG Chain.

**b. System ACE Module Connector**

The Virtex-4™ Development Board provides the SAM 50-pin connector on the board for using the Memec System ACE Module (SAM). The SAM can be used to configure the FPGA or to provide bulk flash to a MicroBlaze processor implementation. The Virtex-4™ Development Board provides a System ACE interface that can be used to configure the Virtex-4 FPGA. The interface also gives software designers the ability to run realtime operating systems (RTOS) from removable CompactFlash cards. The Memec System ACE module (DS-KIT-SYSTEM ACE) can be used to perform both of these functions. The figure below shows the System ACE module connected to the header on the Virtex-4™.
Figure 38. System ACE module connecter.

c. System ACE Controller Signal Description

The following table shows the System ACE Module signal assignments to the FPGA I/O pins. It should be noted that on the V4LC development board the System ACE module and the P160 slot share a common bus structure. These two interfaces use a dedicated chip select for processor access while the other signals such as the address/data and control are shared.
Table 6.  GPIO Pin Assignments.

### d. Serial Flash

This section describes the procedure for programming the Atmel serial data flash on the Memec Virtex-4™ Development Board. This serial flash along with a CPLD is used to configure the Virtex-4™ FPGA located on the development board on power up. The following figure shows a high-level block diagram of the serial flash interface to the Virtex-4™ FPGA.
Figure 39. Virtex-4™ Configuration Interface.

An interface is provided between the FPGA and the CPLD to allow access to the serial flash after the FPGA has been configured. This interface uses FPGA I/O pins to interface to the serial flash via the SPI port. The Virtex-4™ FPGA uses 8Mb of the serial flash memory for configuration and this interface allows the other 8Mb to be used for general-purpose application after the FPGA has been configured. The following table shows the signals used to implement the interface between the FPGA and the CPLD after the FPGA has been configured.
Table 7. FPGA SPI Interface Pin Assignments.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Virtex-4 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA_SI</td>
<td>Serial Flash SPI port data input signal</td>
<td>P4</td>
</tr>
<tr>
<td>FPGA_SO</td>
<td>Serial Flash SPI port data output signal</td>
<td>P5</td>
</tr>
<tr>
<td>FPGA_SCK</td>
<td>Serial Flash SPI port clock input signal</td>
<td>P1</td>
</tr>
<tr>
<td>FPGA_CSn</td>
<td>Serial Flash SPI port chip select input signal</td>
<td>N2</td>
</tr>
<tr>
<td>FPGA_WPn</td>
<td>Serial Flash SPI port write protect input signal</td>
<td>N3</td>
</tr>
<tr>
<td>FPGA_RESETn</td>
<td>Serial Flash SPI port reset input signal</td>
<td>P2</td>
</tr>
<tr>
<td>FPGA_RDY/BUSYn</td>
<td>Serial Flash SPI port ready output signal</td>
<td>N4</td>
</tr>
</tbody>
</table>

The primary function of the CPLD is to translate the Master Serial interface to the SPI interface of the serial flash. The XC9536XV CPLD uses the FPGA CCLK clock along with the INITn and DONE signals to drive the SPI SI, SCK and CSn signals. The SO output of the serial flash is used by the CPLD to drive the DIN signal of the FPGA.

**e. JTAG Chain on the Virtex-4™ Development Board**

The following figure shows the JTAG chain on the Virtex-4™ Development Board. As mentioned, the CPLD is used for interfacing to the configuration flash and does not provide any user logic. Hence, this CPLD is programmed by Memec prior to shipping the board. The programming file for the CPLD is provided in case re-programming of the CPLD becomes necessary. The CPLD must be programmed prior to performing any operations on the serial flash such as erasing, programming, reading or verifying.
Figure 40. Virtex-4™ Development Board JTAG Chain.

The following table shows jumper settings for the JTAG chain on the Virtex-4™ Development Board.

<table>
<thead>
<tr>
<th>Devices in the JTAG Chain</th>
<th>JP14 Jumpers Installed</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPLD and FPGA</td>
<td>Pins 1-2, 3-4 and 5-6</td>
</tr>
<tr>
<td>CPLD</td>
<td>Pins 2-3 and 5-6</td>
</tr>
<tr>
<td>FPGA</td>
<td>Pins 1-2 and 4-5</td>
</tr>
</tbody>
</table>

Table 8. JTAG Chain Jumper Settings.

**f. Configuration Flash on the Virtex-4™ Development Board**

The following figure shows the detail of the interface between the FPGA and the serial flash. A PC4 cable is used to program the serial flash with the FPGA bitstream. Once the flash is programmed, on power-up, the
CPLD will read the data from the flash and configure the FPGA over the Master Serial interface.

Figure 41. Serial Flash Configuration Interface.

\textit{g. JTAG Port}

The Virtex-4\textsuperscript{TM} Development Board provides a JTAG port (PC4 type) connector for configuration of the FPGA. The following figure shows the pin assignments for the PC4 header on this development board.
h. Configuration Modes

The following table shows the Virtex-4™ Development Board configuration modes.

<table>
<thead>
<tr>
<th>Mode</th>
<th>PC Pull-up</th>
<th>1-2 (M2)</th>
<th>3-4 (M1)</th>
<th>5-6 (M0)</th>
<th>7-8 (HSWAP_EN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master Serial</td>
<td>Yes</td>
<td>Closed</td>
<td>Closed</td>
<td>Closed</td>
<td>Closed</td>
</tr>
<tr>
<td>Master Serial</td>
<td>No</td>
<td>Closed</td>
<td>Closed</td>
<td>Closed</td>
<td>Open</td>
</tr>
<tr>
<td>Slave Serial</td>
<td>Yes</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>Slave Serial</td>
<td>No</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>Master SelectMap</td>
<td>Yes</td>
<td>Closed</td>
<td>Open</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>Master SelectMap</td>
<td>No</td>
<td>Closed</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>Slave SelectMap</td>
<td>Yes</td>
<td>Open</td>
<td>Open</td>
<td>Closed</td>
<td>Closed</td>
</tr>
<tr>
<td>Slave SelectMap</td>
<td>No</td>
<td>Open</td>
<td>Open</td>
<td>Closed</td>
<td>Open</td>
</tr>
<tr>
<td>JTAG</td>
<td>Yes</td>
<td>Open</td>
<td>Closed</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>JTAG</td>
<td>No</td>
<td>Open</td>
<td>Closed</td>
<td>Open</td>
<td>Open</td>
</tr>
</tbody>
</table>

Table 9. FPGA Configuration Mode Jumper Settings.

10. Voltage Regulators

The following figure shows the voltage regulators that are used on Virtex-4™ Development Board to provide various on-board voltage sources. As shown in the following figure, a connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all onboard regulators to generate the 1.2V, 2.5V, and 3.3V voltages.
The following table shows the power provided on the development board for the on-board voltage sources. A 32.5W power adapter (5V @ 6.5A) is used to provide power to the on-board regulators. The following table shows typical power usage on the Virtex-4™ Development Board.

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current (A)</th>
<th>Power (W)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2V</td>
<td>1.5</td>
<td>1.8</td>
<td>FPGA Core voltage</td>
</tr>
<tr>
<td>2.5V</td>
<td>1.5</td>
<td>3.75</td>
<td>FPGA I/O voltage, P160 supply voltage</td>
</tr>
<tr>
<td>3.3V</td>
<td>3</td>
<td>9.9</td>
<td>FPGA I/O voltage, P160 supply voltage</td>
</tr>
<tr>
<td><strong>Total Power</strong></td>
<td><strong>15.45</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 10. FPGA Configuration Mode Jumper Settings.
If the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators.

11. Bank I/O Voltage

The following table shows the Virtex-4™ Development Board bank I/O voltages on the Virtex-4™ Development Board.

<table>
<thead>
<tr>
<th>Bank #</th>
<th>I/O Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.5V</td>
</tr>
<tr>
<td>1</td>
<td>3.3V</td>
</tr>
<tr>
<td>2</td>
<td>3.3V</td>
</tr>
<tr>
<td>3</td>
<td>2.5V</td>
</tr>
<tr>
<td>4</td>
<td>3.3V</td>
</tr>
<tr>
<td>5</td>
<td>3.3V</td>
</tr>
<tr>
<td>6</td>
<td>2.5V</td>
</tr>
<tr>
<td>7</td>
<td>3.3V</td>
</tr>
<tr>
<td>8</td>
<td>3.3V</td>
</tr>
</tbody>
</table>

Table 11. I/O Bank Voltages.

12. P160 Expansion Module Signal Assignments

The following tables show the Virtex-4™ pin assignments to the P160 Expansion Module connectors (JX1 & JX2) located on the Virtex-4™ Development Board.
<table>
<thead>
<tr>
<th>Virtex-4 FPGA Pin #</th>
<th>I/O Connector Signal Name</th>
<th>JX1 Pin #</th>
<th>I/O Connector Signal Name</th>
<th>Virtex-4 FPGA Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>TCK</td>
<td>A1 B1</td>
<td>FPGA BITSTREAM</td>
<td>NC</td>
</tr>
<tr>
<td>GND</td>
<td>A2 B2</td>
<td></td>
<td>SM DOUT/ BUSY</td>
<td>NC</td>
</tr>
<tr>
<td>NC</td>
<td>TMS</td>
<td>A3 B3</td>
<td>FPGA CCLK</td>
<td>NC</td>
</tr>
<tr>
<td>Vin</td>
<td>A4 B4</td>
<td></td>
<td>DONE</td>
<td>NC</td>
</tr>
<tr>
<td>NC</td>
<td>TDI</td>
<td>A5 B5</td>
<td>INITn</td>
<td>NC</td>
</tr>
<tr>
<td>GND</td>
<td>A6 B6</td>
<td></td>
<td>PROGRAMn</td>
<td>NC</td>
</tr>
<tr>
<td>NC</td>
<td>TDO</td>
<td>A7 B7</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>3.3V</td>
<td>A8 B8</td>
<td></td>
<td>LIOB8</td>
<td>D18</td>
</tr>
<tr>
<td>D17</td>
<td>LIOA9</td>
<td>A9 B9</td>
<td>LIOB9</td>
<td>C18</td>
</tr>
<tr>
<td>GND</td>
<td>A10 B10</td>
<td></td>
<td>LIOB10</td>
<td>G17</td>
</tr>
<tr>
<td>D18</td>
<td>LIOA11</td>
<td>A11 B11</td>
<td>LIOB11</td>
<td>C17</td>
</tr>
<tr>
<td>2.5V</td>
<td>A12 B12</td>
<td></td>
<td>LIOB12</td>
<td>F17</td>
</tr>
<tr>
<td>W9</td>
<td>LIOA13</td>
<td>A13 B13</td>
<td>LIOB13</td>
<td>C16</td>
</tr>
<tr>
<td>GND</td>
<td>A14 B14</td>
<td></td>
<td>LIOB14</td>
<td>F18</td>
</tr>
<tr>
<td>E18</td>
<td>LIOA15</td>
<td>A15 B15</td>
<td>LIOB15</td>
<td>D15</td>
</tr>
<tr>
<td>Vin</td>
<td>A16 B16</td>
<td></td>
<td>LIOB16</td>
<td>G19</td>
</tr>
<tr>
<td>G20</td>
<td>LIOA17</td>
<td>A17 B17</td>
<td>LIOB17</td>
<td>C15</td>
</tr>
<tr>
<td>GND</td>
<td>A18 B18</td>
<td></td>
<td>LIOB18</td>
<td>F19</td>
</tr>
<tr>
<td>F20</td>
<td>LIOA19</td>
<td>A19 B19</td>
<td>LIOB19</td>
<td>D13</td>
</tr>
<tr>
<td>3.3V</td>
<td>A20 B20</td>
<td></td>
<td>LIOB20</td>
<td>E20</td>
</tr>
<tr>
<td>E19</td>
<td>LIOA21</td>
<td>A21 B21</td>
<td>LIOB21</td>
<td>C13</td>
</tr>
<tr>
<td>GND</td>
<td>A22 B22</td>
<td></td>
<td>LIOB22</td>
<td>D19</td>
</tr>
<tr>
<td>C20</td>
<td>LIOA23</td>
<td>A23 B23</td>
<td>LIOB23</td>
<td>D12</td>
</tr>
<tr>
<td>2.6V</td>
<td>A24 B24</td>
<td></td>
<td>LIOB24</td>
<td>C19</td>
</tr>
<tr>
<td>GND</td>
<td>A26 B26</td>
<td></td>
<td>LIOB26</td>
<td>B18</td>
</tr>
<tr>
<td>A18</td>
<td>LIOA27</td>
<td>A27 B27</td>
<td>LIOB27</td>
<td>D9</td>
</tr>
<tr>
<td>Vin</td>
<td>A28 B28</td>
<td></td>
<td>LIOB28</td>
<td>B17</td>
</tr>
<tr>
<td>B16</td>
<td>LIOA29</td>
<td>A29 B29</td>
<td>LIOB29</td>
<td>C9</td>
</tr>
<tr>
<td>GND</td>
<td>A30 B30</td>
<td></td>
<td>LIOB30</td>
<td>A16</td>
</tr>
<tr>
<td>B15</td>
<td>LIOA31</td>
<td>A31 B31</td>
<td>LIOB31</td>
<td>D8</td>
</tr>
<tr>
<td>3.3V</td>
<td>A32 B32</td>
<td></td>
<td>LIOB32</td>
<td>A15</td>
</tr>
<tr>
<td>Y7</td>
<td>LIOA33</td>
<td>A33 B33</td>
<td>LIOB33</td>
<td>C8</td>
</tr>
<tr>
<td>GND</td>
<td>A34 B34</td>
<td></td>
<td>LIOB34</td>
<td>J16</td>
</tr>
<tr>
<td>Y6</td>
<td>LIOA35</td>
<td>A35 B35</td>
<td>LIOB35</td>
<td>H16</td>
</tr>
<tr>
<td>2.6V</td>
<td>A36 B36</td>
<td></td>
<td>LIOB36</td>
<td>G16</td>
</tr>
<tr>
<td>F16</td>
<td>LIOA37</td>
<td>A37 B37</td>
<td>LIOB37</td>
<td>E16</td>
</tr>
<tr>
<td>GND</td>
<td>A38 B38</td>
<td></td>
<td>LIOB38</td>
<td>E15</td>
</tr>
<tr>
<td>Y5</td>
<td>LIOA39</td>
<td>A39 B39</td>
<td>LIOB39</td>
<td>F15</td>
</tr>
<tr>
<td>Vin</td>
<td>A40 B40</td>
<td></td>
<td>LIOB40</td>
<td>E14</td>
</tr>
</tbody>
</table>

Table 12. P160 Connector Pin Assignments.
<table>
<thead>
<tr>
<th>Virtex-4 FPGA Pin #</th>
<th>I/O Connector Signal Name</th>
<th>JX2 Pin #</th>
<th>I/O Connector Signal Name</th>
<th>Virtex-4 FPGA Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>H18</td>
<td>RIOA1</td>
<td>A1</td>
<td>B1</td>
<td>GND</td>
</tr>
<tr>
<td>H17</td>
<td>RIOA2</td>
<td>A2</td>
<td>B2</td>
<td>RIOB2</td>
</tr>
<tr>
<td>J18</td>
<td>RIOA3</td>
<td>A3</td>
<td>B3</td>
<td>Vin</td>
</tr>
<tr>
<td>J17</td>
<td>RIOA4</td>
<td>A4</td>
<td>B4</td>
<td>RIOB4</td>
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<td>K18</td>
<td>RIOA5</td>
<td>A5</td>
<td>B5</td>
<td>GND</td>
</tr>
<tr>
<td>K17</td>
<td>RIOA6</td>
<td>A6</td>
<td>B6</td>
<td>RIOB6</td>
</tr>
<tr>
<td>L17</td>
<td>RIOA7</td>
<td>A7</td>
<td>B7</td>
<td>3.3V</td>
</tr>
<tr>
<td>M18</td>
<td>RIOA9</td>
<td>A3</td>
<td>B3</td>
<td>RIOB6</td>
</tr>
<tr>
<td>M17</td>
<td>RIOA9</td>
<td>A9</td>
<td>B9</td>
<td>GND</td>
</tr>
<tr>
<td>N18</td>
<td>RIOA10</td>
<td>A10</td>
<td>B10</td>
<td>RIOB10</td>
</tr>
<tr>
<td>P17</td>
<td>RIOA11</td>
<td>A11</td>
<td>B11</td>
<td>2.5V</td>
</tr>
<tr>
<td>T15</td>
<td>RIOA12</td>
<td>A12</td>
<td>B12</td>
<td>RIOB12</td>
</tr>
<tr>
<td>U15</td>
<td>RIOA13</td>
<td>A13</td>
<td>B13</td>
<td>GND</td>
</tr>
<tr>
<td>T18</td>
<td>RIOA14</td>
<td>A14</td>
<td>B14</td>
<td>RIOB14</td>
</tr>
<tr>
<td>U19</td>
<td>RIOA15</td>
<td>A15</td>
<td>B15</td>
<td>Vin</td>
</tr>
<tr>
<td>R17</td>
<td>RIOA16</td>
<td>A16</td>
<td>B16</td>
<td>RIOB16</td>
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<tr>
<td>R18</td>
<td>RIOA17</td>
<td>A17</td>
<td>B17</td>
<td>GND</td>
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<tr>
<td>H19</td>
<td>RIOA18</td>
<td>A18</td>
<td>B18</td>
<td>RIOB18</td>
</tr>
<tr>
<td>J19</td>
<td>RIOA19</td>
<td>A19</td>
<td>B19</td>
<td>3.3V</td>
</tr>
<tr>
<td>K20</td>
<td>RIOA20</td>
<td>A20</td>
<td>B20</td>
<td>RIOB20</td>
</tr>
<tr>
<td>K19</td>
<td>RIOA21</td>
<td>A21</td>
<td>B21</td>
<td>GND</td>
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<tr>
<td>L20</td>
<td>RIOA22</td>
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<td>L19</td>
<td>RIOA23</td>
<td>A23</td>
<td>B23</td>
<td>2.5V</td>
</tr>
<tr>
<td>M20</td>
<td>RIOA24</td>
<td>A24</td>
<td>B24</td>
<td>RIOB24</td>
</tr>
<tr>
<td>M19</td>
<td>RIOA25</td>
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<td>N19</td>
<td>RIOA26</td>
<td>A26</td>
<td>B26</td>
<td>RIOB26</td>
</tr>
<tr>
<td>P20</td>
<td>RIOA27</td>
<td>A27</td>
<td>B27</td>
<td>Vin</td>
</tr>
<tr>
<td>U12</td>
<td>RIOA28</td>
<td>A28</td>
<td>B28</td>
<td>RIOB28</td>
</tr>
<tr>
<td>P19</td>
<td>RIOA29</td>
<td>A29</td>
<td>B29</td>
<td>GND</td>
</tr>
<tr>
<td>V11</td>
<td>RIOA30</td>
<td>A30</td>
<td>B30</td>
<td>RIOB30</td>
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<tr>
<td>V10</td>
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<td>B31</td>
<td>3.3V</td>
</tr>
<tr>
<td>V9</td>
<td>RIOA32</td>
<td>A32</td>
<td>B32</td>
<td>RIOB32</td>
</tr>
<tr>
<td>U9</td>
<td>RIOA33</td>
<td>A33</td>
<td>B33</td>
<td>GND</td>
</tr>
<tr>
<td>R20</td>
<td>RIOA34</td>
<td>A34</td>
<td>B34</td>
<td>RIOB34</td>
</tr>
<tr>
<td>R19</td>
<td>RIOA35</td>
<td>A35</td>
<td>B35</td>
<td>2.5V</td>
</tr>
<tr>
<td>T20</td>
<td>RIOA36</td>
<td>A36</td>
<td>B36</td>
<td>RIOB36</td>
</tr>
<tr>
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</tbody>
</table>

Table 13. P160 Connector Pin Assignments.
APPENDIX C: SEMITEACH® POWER CONVERTER

Figure 44. SEMITEACH® Power Converter [From [11]].

When teaching and demonstrating the exciting world of power electronics, safety must be the main concern. Due to lack of experience, students should not be exposed immediately to live power. For a better understanding, it is valuable to actually see and electrically access the individual components of the system.

The new "Power Electronics Teaching System" from SEMIKRON achieves exactly this.

The "Power Electronics Teaching System" will meet various application requirements regarding converters up to 20 kVA: 3 or 1 phase motors, DC current motors, UPS, active filter... or the totally new application you just invented.

Power Design

The "Power Electronics Teaching System" was designed to provide a maximum of 30 A rms per phase.

Major components:

- 3 half-bridge module with IGBT and CAL-diode SKM 50GB123D
- 1 IGBT brake chopper SKM 50GL123D
- 3-phase diode rectifier SKO 51/14
- DC busbar capacitance of 1100 μF / 800 V
- 4 SKHI 22 drivers

Output power capability: up to 20 kVA (3 phases)

Switching frequency: up to 20 kHz

Max input AC voltage: 3x480 V - 400V with filter

Active Security

The driver SKHI 22 protects the IGBTs against:

- short-circuits (detection, switch off the IGBT, blocking of all further signals, error message)
- under-voltage of the power supply (blocking of all signals, error message), simultaneous command of both IGBTs in one phase-leg (through logic and dead-time).

Furthermore, a thermal protection prohibits destructive heatsink temperatures.

A sensor has been placed at the warmest point of the heatsink to measure the temperature and validate your calculations.

As an option, a complete EMC protection, defined in partnership with SCHAFFNER, can be delivered. This includes the filter against conducted perturbations, this protection allows the "Power Electronics Teaching System" to be CE marked.

Applications Manual/initial class assignments

With over 40 years of experience SEMIKRON has designed its "Power Electronics Teaching System" to expose students to realistic industrial applications design. The manual also gives an example for an initial educational demonstration. Students can compare the test results with the calculation method in the manual.

SEMIKRON Quality

As a leader in power IGBT power systems, SEMIKRON ensures the quality of your "Power Electronics Teaching System" by providing a final test certificate. Every IGBT of each power stack is tested in short-circuit, at maximum voltage, and the complete stack is tested under full load conditions (max. current, max. DC Voltage).
LIST OF REFERENCES


INITIAL DISTRIBUTION LIST

1. Defense Technical Information Center
   Ft. Belvoir, Virginia

2. Dudley Knox Library
   Naval Postgraduate School
   Monterey, California

3. Dr. Jeffrey Knorr
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