Advanced MRAM Concepts

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Abstract—Two important goals of Magnetoresistive Random Access Memory (MRAM) development are to improve MRAM manufacturability and to extend MRAM density to 100 nm dimensions. One potential barrier to MRAM manufacturability is associated with the method of write selection in which two orthogonal currents in coincidence must write data, whereas each of the orthogonal currents alone cannot disturb the data. This "2D" selection method places constraints on uniformity of MRAM memory cells. Using a transistor per cell for write select greatly improves operating margins and lowers write currents. Attaining reasonable memory densities for this scheme depends on limiting the required write current in order to minimize the area of the select transistor. A second goal is to extend MRAM density to 100 nm dimensions. Use of a vertical GMR multilayer ring structure, where the data is stored in circumferencially oriented magnetizations, can extend the density of MRAM [Zhu and Prinz, Paper GB-02, 1999 Intermag]. Stability is projected for cells with inside diameters of less than 50nm. A second approach is to use Joule heating, in combination with magnetic field from a current, to write by exceeding the Neel point of an antiferromagnetic pinning layer in a pseudo-spin valve cell. Feature sizes smaller than 100 nm are projected along with decreases in required switching currents.

TABLE OF CONTENTS

1. INTRODUCTION

Development of magnetoresistive random access memory (MRAM) is progressing toward products [1,2,3,4,5]. Two potential barriers to MRAM product success are yield of the magnetic cells and the scalability of MRAM to 100 nm dimensions. Section 2 describes a new MRAM memory cell and architecture which should circumvent cell yield problems associated with traditional 2D write select schemes, which require quite tight process tolerances. In this new scheme, a select transistor per memory cell is used for writing, and a much smaller current is used for reading than for writing. This should result in substantially wider process margins, but probably at the sacrifice of density due to the size of the required transistor in the cell. This "1D magnetic select" scheme is potentially ideal for small, high performance nonvolatile RAM.

Sections 3 and 4 describe two ideas for increasing the density of MRAM apace with the industry's decreasing lithographic limits. In Section 3 an MRAM cell is described which utilizes vertical giant magnetoresistance (GMR) rather than in-plane GMR. The cell is etched into ring shapes, with the magnetizations of the GMR multilayers lying circumferencially around the ring [10]. A word line is used to provide a half-select field, while current through the ring provides the other half-select field. The advantange of the cell is improved stability by avoiding magnetic "vortices" down to very small cell sizes - at least down to inner diameters of about 300 nm. Section 4 describes a technique to increase density of MRAM by heating an antiferromagnetic pinning layer above its ordering temperature (Neel temperature). This scheme effectively deepens the energy well depth of unselected cells, and potentially will permit higher storage densities at smaller current levels.

2. 1D MAGNETIC SELECTION

Magnetic memory cells, such as magnetic cores, have traditionally used selection schemes for reading and writing which don't require a transistor or diode in the memory cell, but which do place restrictions on uniformity and "disturb" sensitivity of the cell. Figure 1 is a diagram showing a typical 2D write selection scheme. Selected cells receive both Ix and Iy currents, and are switched into the desired memory states. The currents must be selected so that Iy or Ix separately do not disturb the memory state of stored data. Bits on the same x line or y line that are not

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Advanced MRAM Concepts

being written are subjected to "half-select" currents which tend to disturb the data. If very large currents are used to insure the writing of worst case cells, then the half-select currents are also large and tend to disturb the most disturb-sensitive cells. The half-selected memory states are also not nearly as stable as stored bits, and they provide the majority of projected cell failures in time [12]. In addition to half-select currents, these cells must withstand stray fields from neighboring cells and fields from leakage currents and stray environmental fields. Thus, the requirements for uniformity and design margins present challenges in manufacturing the 2D magnetic arrays.

Most magnetoresistive memory schemes also use a 2D selection scheme for reading data. The original MRAM [6] concept and the pseudo-spin valve (PSV) [7] concept both use magnetic 2D selection schemes for reading, which introduce further disturb conditions. Magnetic tunnel junction memories (MTJ) [1,2,8] use a diode or transistor to select a memory cell for reading, and thus do not have significant disturb conditions for reading, but they still have the constraints of 2D magnetic selection for writing.

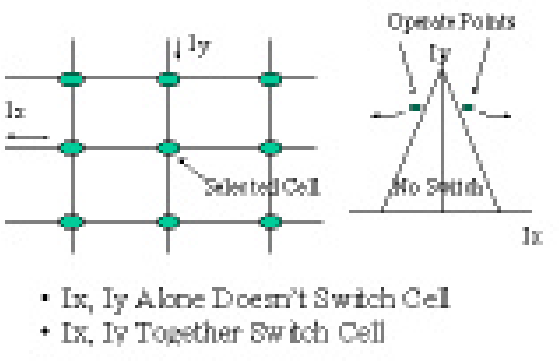

Figure 1. 2D Magnetic Selection Scheme

Figure 2 depicts a simple "1D selection" scheme for both reading and writing a magnetoresistive memory cell. A high current of either polarity (plus current for a "1" and negative current for a "0" is passed through a select transistor and through the memory cell to write. A lower current is used to generate a voltage across the cell which will be higher or lower depending on the data stored and the magnetoresistance of the cell. This voltage is then sensed and compared to a reference in order to determine the memory state.

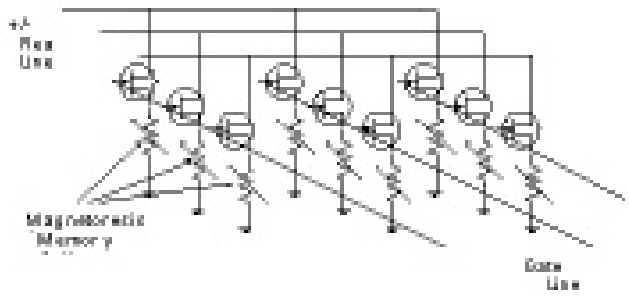

Figure 2. A 1D Magnetic Selection (Read and Write) Scheme For Magnetoresistive Cells.

Note that the transistor provides the selection of the memory cell, not the 2D magnetic switching properties of the cell. A very large current can be used to write and a small current can be used to read the cell, thus providing potentially very large margins. Of course it is important to use as small a current as will reliably write the cell so as to reduce the size of the transistor needed for selection. There are still 2D arrays of cells, but the transistors take up the burden of selection rather than placing severe constraints on the magnetic switching properties of the cell. This is why this is called a "1D magnetic selection". The scheme is quite similar to that used for DRAM where a transistor is used to write and detect charge on a capacitor.

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Advanced MRAM Concepts

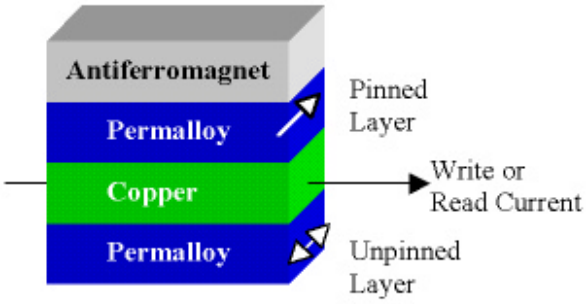

Figure 3. Cell Example For 1D Magnetic Selection.

Figure 3 shows an implementation of this concept in a cell using a "spin valve". Two magnetic films sandwich a conducting layer, and one of the two magnetic films is "pinned" with an antiferromagnet across a stripe etched from the materials. A magnetic field created by a current through the stripe can be used to magnetize the unpinned magnetic film in either of two directions, depending on the direction of the current. Then a smaller current through the stripe can be used to sense the value of resistance - higher if the films are oppositely magnetized and lower if they are magnetized in the same direction. A large current can be used for writing without disturbing other cells, and a much lower current can be used for sensing. This would suggest large margins. In practice, this cell would have difficulties with demagnetization
fields in cells with micron dimensions and smaller.

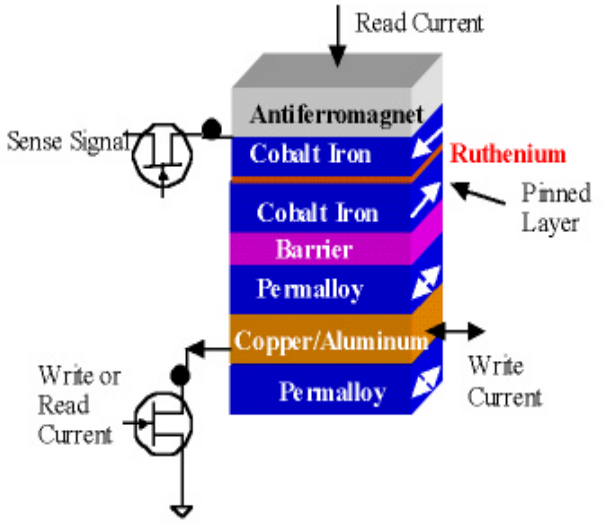

Figure 4. 1D Magnetic Write Selection Cell With Tunneling Readout.

Figure 4 shows a variation on the concept that uses spin dependent tunneling for a higher signal output and minimizing demagnetizing effects. A sandwich stripe with neither magnetic film "pinned" can be magnetized with a current through the sandwich into either of two magnetic states depending on the direction of current. With no magnetic field applied, the magnetizaions of the films are antiparallel and lie across the axis of the stripe. A tunnel barrier is deposited on top of the sandwich, and a pinned synthetic antiferromagnet is deposited on top of the barrier. The top layer of the synthetic antiferromagnet is pinned with an antiferromagnet. The synthetic antiferromagnet is comprised of two magnetic layers sandwiching a thin ruthenium layer, a structure which has very strong antiparallel coupling. The synthetic antiferromagnet thus produces very little stray magnetic field, and similarly, the unpinned sandwich also produces very little stray magnetic field. The spin tunneling current between the top layer of the sandwich and the pinned layer is then either higher or lower depending on the direction of magnetization of the top layer. Spin dependent tunneling has demonstrated about 40% magnetoresistance with 100 mV across the barrier, and thus a signal of approximately 40 mV could be observed. The barrier resistance is usually large enough to limit the read current to about 20 ?A, while the current needed to set the magnetization in the cell (write) should be about 2.5 mA for a cell on the order of a micron width. For those values, the disturb current would be about 1/100 of the write current.

	PSV	MTI	1D C4ell
Write Current	25 mA	25 mA	2.5 mA
Ease of Mfg.	Harder	Harder	Easier
Speed	Medium	High	High
Density	High	Medium	Lower

Table 1 gives a qualitative comparison of memory properties for spin dependent tunneling and pseudo-spin valve memory cells (based on limited published data) with the potential properties of memories based on this 1D cell. The major potential advantages for these memories are much lower write currents (power) and manufacturabililty. Memory performance should be as high as for MTJ memories, but because of the size requirement for the write transistor, densities will be lower, especially when compared with the pseudo-spin valve based memories. However, for many small, niche memories, the overhead

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space required for pads and peripheral electronics is much larger than the space required by the memory cells. In such applications the 1D selection scheme could be especially useful.

Table 1. Comparison of Potential Properties of 1D Cells with some projected properties of PSV and MTJ cells.

3. VERTICAL RING GMR CELLS

One of the problems encountered in high density MRAM cells has been magnetic anomalies or vortices [9]. These vortices cause inconsistant magnetic behavior, and may result in the inability to write or read a cell correctly. Magnetic simulations and measurements have confirmed this behavior. A structure which may circumvent this problem [10, 11] is shown in Figure 5. Magnetic films of a few nanometers thickness are separated by thin copper layers, and alternating magnetic layers are of two significantly different thicknesses. When a bit current is passed through the vertical stack, a circumferential magnetic field is created that can tend to magnetize these magnetic films, with the thinner magnetic layers switching at lower currents (fields) and the thicker layers switching at higher currents (fields). With the layers magnetized in one sense, the resistance of the stack is lower than when the layers are oppositely magnetized. The vertical GMR is in general larger than in-plane GMR, so that for a given current through the stack, the signal is quite usuable, even though the cell itself generally has relatively low resistance due to its shape.

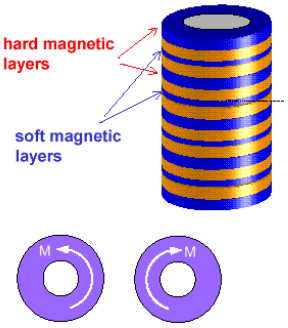

Figure 5. A Vertical GMR Cell and Circumferential Remnant Magnetizations.

In order to attain a 2D read/write select organization, a pair of parallel word lines lying on the outside edge of the cell carry currents in opposite directions, and an orthogonal pair of lines carrying similar currents is placed on the opposite side of the cell, as shown in Figure 6. With currents flowing through both pairs of word lines, a field configuration shown in Figure 7 is created. This field is a "tipping" field which lowers the bit current thresholds for switching. Thus, a 2D selection scheme is possible where the word currents by themselves or the bit currents by themselves cannot write the hard (thick) film layer, but the combination of the two currents can.

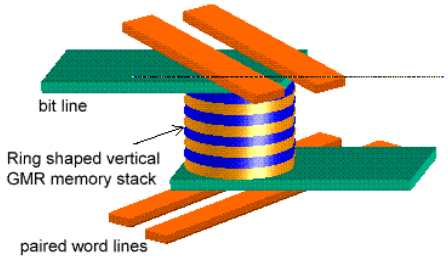

Figure 6. Vertical GMR Memory Cell Showing Bit Lines (Bit Current Direction Determining Data Written) and Word (Tipping Field) Lines.

One way read out data from such a cell is to switch the soft (thin) layer from one state to the other while observing the resistance. At some intermediate value of word current and sense current where the soft (thin) layer can be switched, but the hard (thick layer is not), the resistance of the sense line is observed as the sense current is reversed. In this way, the sense of the hard layer can be determined. In Figure 8, this would correspond to operating in the flat top region where the soft film is switched back and forth. The resistance of the cell is higher when the magnetization of the soft layer is antiparallel to the magnetization of the hard layer, and lower with a parallel orientation.

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Advanced MRAM Concepts

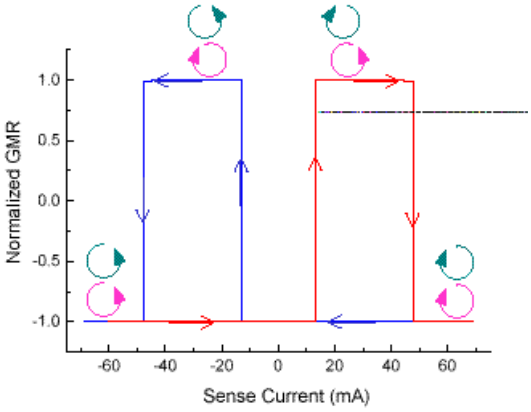

Figure 8. Magnetoresistance as a Function of Sense Current.

The primary advantage of this cell is the potential density which it can achieve. The storage mode, according to extensive numerical simulations, does not create vortices for cell sizes down to less than 100 nm diameter (approximately 30nm inside diameter), which is smaller than demonstrated PSV and MTJ cells. Data confirming this small achievable size for vertical GMR cells has not been published.

4. NEEL POINT WRITTEN CELLS

Another challenge for very high density MRAM is cell stability at nm dimensions. As the cell size shrinks and the volume, V, of magnetic materials gets smaller, thermal agitation can cause a cell to lose data. (This same problem gives rise to the so called " superparamagnetic limit" spoken of in recording technology". If Ht is the switching threshold of a half-selected cell and Ms is the magnetic moment, then the depth of the energy well associated with that switching threshold in the half-select state is proportional to Ms*Ht*V. For low error rates the ratio of this energy well depth to kT should be at least 55 [12]. Assuming a maximum operating temperature of 350 K and a cell size of 100nm X 100nm X 2 (nm), one finds that Ht must be about 166 Oe, and the threshold of a non-half-selected cell must be several times that. When enough current is applied to get this magnitude of field in a nm sized cell, thermal heating is a problem, and kT becomes even larger, and the higher densities are even harder to achieve.

An approach to improving the density of MRAM is to make use of heating effects in combination with magnetic fields from currents to switch cells which use antiferromagnetic pinning of a ferromagnetic layer. Figure 9 illustrates a thin ferromagnetic film which is deposited in contact with an antiferromagnet. After pinning, very large magnetic fields (several thousands of Oe) cannot permanently reverse the pinned direction if the temperature is significantly below the Neel (ordering) temperature of the antiferromagnet. This property could be used in many memory cells to obtain a deep energy well for stored data, and provided heat can be applied to the cell for writing, the writing currents may not have to be very large.

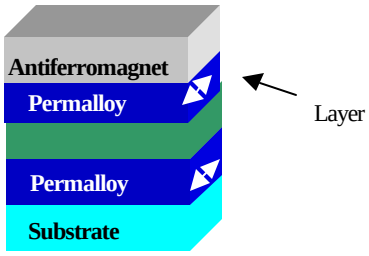

Figure 9. A Permalloy Layer Pinned With An Aniferromagnet. A second permalloy layer and a copper layer can be used to complete a PSV structure.

If the pinned layer in Figure 9 can be substituted for the storage layer in a PSV [7], and if the heating effects of the word and digit currents can heat the ferromagnet above the Neel temperature of the antiferromagnet, then the cell can be written in exactly the same way as a normal PSV, but the cell would have a decidedly higher stability.

In the PSV cell shown in Figure 10, current through the sense line acts as a tipping field and current in the word line in combination with that tipping field reverses the storage layer if the word current is large enough, but reverses only the soft layer at a smaller word current.

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Advanced MRAM Concepts

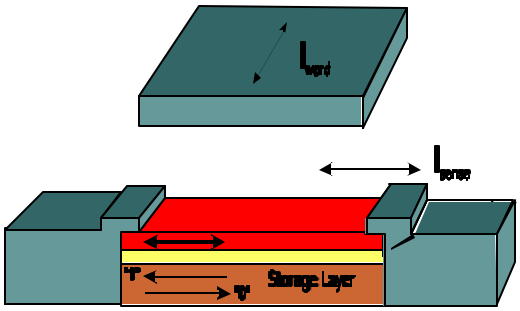

Figure 10. A Psuedo Spin Valve (PSV) Cell. Pinned ferromagnetic films were fabricated at NVE as storage layers in pseudo-spin valve cells in order to obtain experimental verification of switching using a combination of heating and magnetic field.. The pinned layer was cobalt-permalloy pinned with an iron manganese antiferromagnet, and the unpinned read layer was cobalt-permalloy. Repeatable switching was observed. A thermal time constant of about 3 ns was demonstrated for a silicon nitride dielectric thicknesses of 35 nm.

5. CONCLUSIONS

One approach to making a producible, high performance niche memory and two approaches for extending the density of MRAM to nm dimensions were described. It should be noted that these techniques could be used in combination. There are undoubtedly many more possibilities for improving MRAM density, performance, and producibility that will come to light in the next few years.

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