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The development of the processes necessary for fabrication of sub-100nm heteroepitaxial Si_xGe_{1-x} structures in Si (100) substrates is described. The structures are required to be planar, and definable by available patterning techniques (e.g., X-ray, *e*-beam, ion beam, or optical lithography). The report describes the investigation of two candidate patterning processes, enhanced ion beam etching, and standard *e*-beam lift off. The formation of the heteroepitaxial structures, in the form of nano-wires, is carried out using pulsed laser induced epitaxy, an ultra-rapid (<100ns) epitaxial growth technique driven by a pulsed excimer laser. Development of a novel, high yield cross sectioning process to examine the wire structures was also carried out during the course of this effort. This process used ion beam deposition of a platinum etch mask, followed by an enhanced, localized ion beam etch to define the wire specimen. Results from cross sectional transmission electron beam analysis indicate successful formation of the heteroepitaxial wires with no defects being observed.

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EXECUTIVE SUMMARY

Nanometer-scale devices have attracted great attention as the ultimate evolution of silicon integrated circuit technology. However, fabrication of nanometer-scale silicon based devices has met great difficulty because it places severe constraints on process technology. This is especially true for SiGe/Si heterostructures because they are particularly sensitive to strain relaxation and/or process induced defects. Recently developed Pulsed Laser Induced Epitaxy (PLIE) offers a promising approach for the fabrication of nanometer-scale SiGe/Si devices. It possesses the advantage of ultra-short time, low thermal budget and full compatibility with current silicon technology. The selective nature of the process allows epitaxial growth of high quality, localized SiGe layers in silicon. In this work, a process to fabricate SiGe nanowires in silicon using PLIE is described. In particular, Ge nanowires with a cross-section of ~ 6 x 60 nm^2 are first formed using a lift-off process on the silicon substrate with e-beam lithography, followed by a thin low-temperature oxide deposition. Defect-free SiGe nanowires with a cross-section of ~ 25 x 95 nm^2 are then produced by impinging the laser beam on the sample. We thus demonstrate PLIE is a suitable fabrication technique for SiGe/Si nanostructures. Fabrication of Ge nanowires is also studied using Focused Ion Beam (FIB) micromachining techniques. Based on the SiGe nanowire process, we propose two advanced device structures, a quantum wire MOSFET and a lateral SiGe Heterojunction Bipolar Transistor (HBT). MEDICI simulation of the lateral SiGe HBT demonstrates high performance of the device. In order to characterize the SiGe nanowires using cross-sectional transmission electron microscopy, an advanced versatile focused ion beam assisted sample preparation technique using a multi-layer stack scheme for localized surface structures is developed and described in this work.

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Chapter 1

INTRODUCTION

1.1 Motivation for Work

* *Scaling issues for ULSI*

Continued desire for increasing speed and packing densities of VLSI circuits has driven minimum dimensions of devices down to the half-micron scale and integration levels up to 33 million devices on a 100 mm^2 chip in manufacturing. The critical dimensions of devices are also predicted to decrease below 300 nm during the next five years, reaching 150 nm in late nineties.

However, further decrease in dimensions beyond 100 nm might prove to be problematic because of physical limitations [1.1], such as i) thermal and quantum perturbation; ii) statistical errors in threshold voltage due to small number of impurities in a unit volume; iii) electron tunneling through dielectric films below 4 nm in thickness and iv) built-in p-n junction depletion regions on the order of 20 nm.

* *Solution 1: Bandgap Engineering - Heterojunction Devices*

During the last two decades, heterojunction devices[2.2-2.4] have received considerable attention for achieving higher performance and/or obtaining novel optical and electrical properties beyond the capabilities of physical limitations imposed by homojunction devices. Heterojunctions supplement homojunctions by the use of multiple semiconductor materials within a single device. It is understood that in homojunctions, holes and electrons accumulate only in those regions defined by their parent donor and acceptor impurities. In the contrary, heterojunctions can be used to drive both carriers into the same volume, to separate carriers from the parent dopant atoms, or to form local accumulation and/or depletion regions, independent of doping.

The heterojunction offers a large array of device configurations when compare to

homojunctions and becomes the basis of the field of "bandgap engineering". The introduction of III-V heterostructures more than twenty years ago has resulted in the production of superior devices and found commercial applications in the high-end areas such as the millimeter-wave and optoelectronics industry. Nevertheless, it is estimated that heterojunction devices account for no more than a few percent of the current production of semiconductor devices. This result stems from the fact that the dominant semiconductor material, silicon, does not easily form heterostructures with other semiconductor materials.

* *Solution 2: Nanoscale Switching Devices Concept*

Quantum devices [1.5], including mesoscopic devices, represent another family of the most promising alternative devices to supersede silicon VLSI devices. Researchers have already observed interesting physical phenomena such as quantized conductance, wave-like behavior and enhanced luminescence. However, fabrication of such devices has been of great difficulty. Also in the last decade, most of the experimental research has been limited to III-V materials.

* *Si compatible heterojunction technology - Si-Ge*

Advances in the material growth technologies, specifically, in molecular beam epitaxy (MBE) and Ultra High Vacuum Chemical Vapor Deposition (UHV/CVD) have made possible the growth of psuodomophic epitaxial layers. Therefore, strained Ge_xSi_{1-x}/Si heterostructures have become a subject of active attention in the heterostructure family because of its compatibility with silicon [1.6]. Various devices [1.7-1.8], such as vertical Heterojunction Bipolar Transistors (HBTs) with cut-off frequency up to 113 GHz [1.9], infrared detectors, and high electron mobility transistor structures have been demonstrated.

* *Selective Epitaxy of Si-Ge*

The non-selective nature of most hetero-epitaxial growth techniques has proven to be an obstacle for exploitation of Ge_xSi_{1-x}/Si heterostructures for a large family of lateral

confinement devices such as lateral HBTs, quantum wires and dots. Several efforts [1.10-1.11] have been made with either little or no success or redesign of the device structures. To fabricate the above Ge_xSi_{1-x}/Si devices, a new materials growth technology is needed.

Recently developed Pulsed Laser Induced Epitaxy (PLIE) [1.12-1.13] offers a very promising alternative for fabrication of devices which require precise lateral confinement. The process works on a die-by-die basis and is fully compatible with current silicon lithography technology. It possesses an advantage of ultrashort process time scale (<1 μs) and the sample is exposed to elevated temperatures for short times (< 0.2 μs), resulting in a low thermal budget. The process has also demonstrated reliable process control [1.14]. Using this technique, excellent quality strained Ge_xSi_{1-x}/Si heterostructures have been demonstrated.

Fabrication of Ge_xSi_{1-x}/Si wells in a Si substrate using PLIE has also been reported [1.15]. In this experiment, defect-free SiGe wells of 3 and 6-μms in width were formed after PLIE using either standard oxide/Al masking or lift-off patterning techniques, respectively. The wells reported showed well defined, abrupt SiGe/Si interfaces and rounded corners for the structure.

In this work, we use the PLIE process to demonstrate fabrication of ultra-narrow SiGe wires in Si down to the 100-nm scale. We also discuss the possible applications of this result in lateral HBTs and quantum wires.

1.2 Organization

This report is divided into seven chapters, with each chapter covering a major topic. In Chapter 1 we discuss the motivation for the work and the organization of the report.

Chapter 2 discusses the fundamental concepts and physics of the PLIE process along with describing the experimental set-up and the corresponding characterization techniques.

Chapter 3 discusses possible applications for the SiGe wires. We also introduce the design of a novel lateral heterojunction bipolar transistor based on the successful fabrication of the wires using PLIE. We demonstrate the high performance behavior of this device using MEDICI, a 2-dimensional device simulator.

Chapter 4 describes a possible approach for fabricating the ultra-narrow Ge wires using focused ion beam micromachining.

Chapter 5 describes the fabrication process used for sub-100 nm Ge wires using electron beam lithography and lift-off techniques. In this Chapter, we also describe the techniques used to characterize the wires, including atomic force microscopy, scanning electron microscopy and cross-sectional transmission electron microscopy.

Chapter 6 describes the laser mixing process for the Ge wires and Si substrate, *i.e.* the epitaxial growth of the SiGe wires in the silicon substrate. We also discuss topology changes observed in the epitaxial process.

Chapter 7 discusses the contributions of this work, and suggestions for possible future work based on the results obtained to date.

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Chapter 2

PULSED LASER INDUSED EPITAXY SYSTEM SET-UP AND CHARACTERIZATION

2.1 Introduction

The PLIE system employed in this study was set-up at the Oregon Graduate Institute (OGI). The results described in Chapter 6 are mostly obtained using this system. A somewhat similar system exists at Lawrence Livermore National Laboratory (LLNL), and has also been used for some of the work discussed in Chapter 6. In this chapter, we describe only the system set-up at OGI. A rigorous description of the LLNL system can be found in references 2.1 and 2.2 for the interested reader.

2.2 Pulsed XeCl Excimer Laser System

The PLIE system is designed around a pulsed XeCl excimer laser. It is better known as a Gas Immersion Laser Doping (GILD) system [2.1-2.2]. The equipment required for the two processes are essentially the same. As shown in Fig. 2.1, the following three process modules are incorporated into the system.

i) Excimer laser, beam splitters, beam shaping optics, gas cell, and X-Y stages;

ii) *In situ* diagnosis and real time data acquisition apparatus;

iii) Homogenizing optics.

This laser-melting apparatus is designed to allow determination of all parameters required for characterization of the melt/diffusion/recrystallization process *in-situ* and in *real-time*. It utilizes a Questek 2860 excimer laser operating at the XeCl wavelength of 308 nm (3.9 eV photon energy) with a pulse duration full width half maximum (FWHM) of 27 nanoseconds. The excimer laser beam is directed through a set of reflective beam

splitters which allow coarse adjustment ($\Delta E \geq 5\%$) of the laser energy. Fine tuning of the laser energy is through the adjustment of the high voltage supplied to the discharge capacitors of the laser. After the beam splitters, the beam is directed into an optical integrator which is used to homogenize the input laser beam. The refined beam is focused to a final spot on the wafer whose size can be varied from 3x3 mm^2 to 1x1 cm^2. The wafer is contained in a portable vacuum cell filled with the dopant gas for *in-situ* doping or an inert gas for melt-recrystallization experiments. The cell is mounted on a set of x-y stages and the

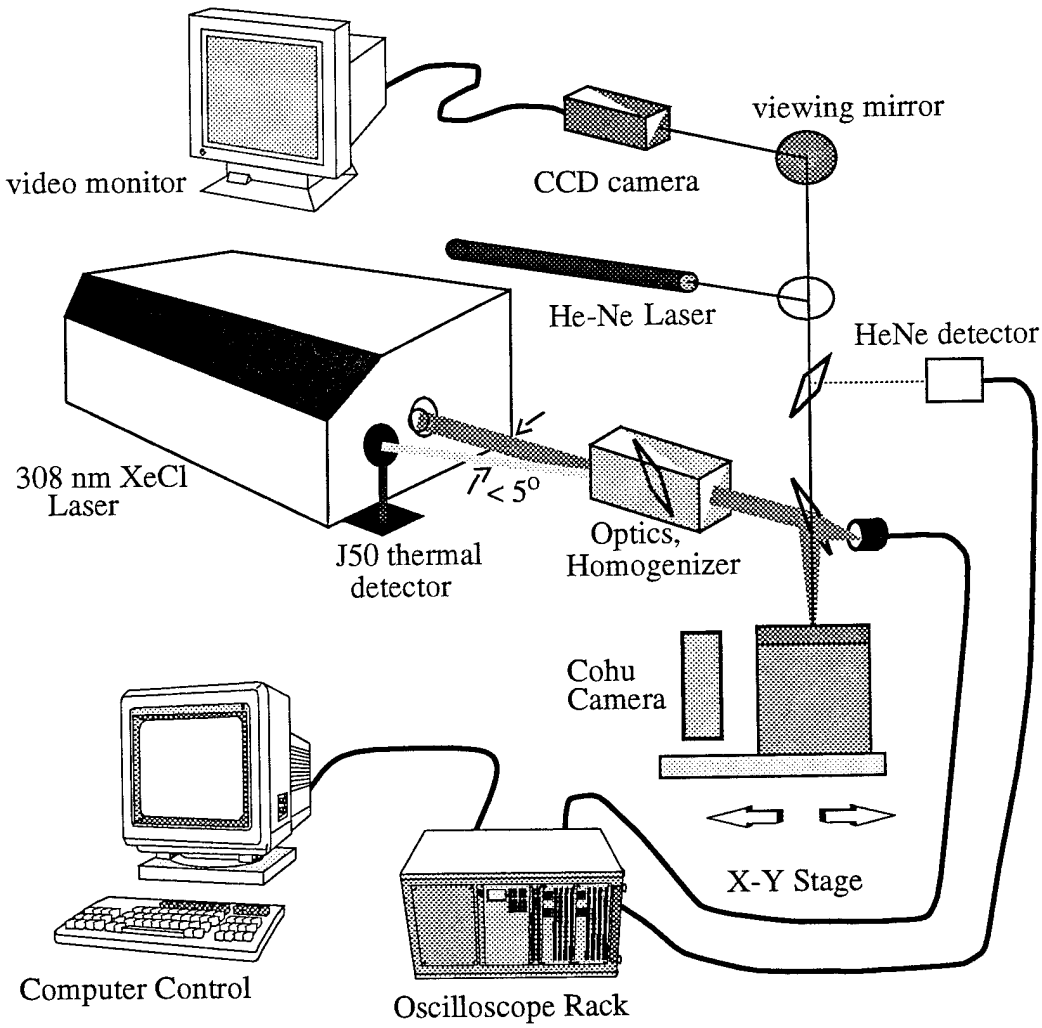


Figure 2.1 Schematic Illustration of the pulsed XeCl excimer laser processing system. This system is controlled by a computer and includes in-situ, digitized diagnostic capabilities for real-time process monitoring.

process is usually carried out on a step and repeat mode and die-by-die basis under computer control.

The real time process diagnostics consist of a HeNe laser reflectivity probe, Si PIN diode, Molectron J50 laser energy fluence probe, Coho high resolution CCD camera, high resolution video monitor, and a Tektronix 2410 2-channel digitizing oscilloscope. Together, this equipment is used to: 1) measure the duration for which the wafer surface remains molten, 2) monitor the temporal profile of the excimer laser beam, 3) measure the laser energy fluence, 4) visually inspect the processed areas, and 5) visually align the wafer for die-by-die processing. The surface melt duration is measured using the HeNe (λ=633 nm) laser focused on the silicon wafer and an avalanche photodiode (APD) to detect the reflected beam. This laser and the APD constitute a simple surface reflectivity probe. Since the HeNe is non-intrusive, the measurement can be made *in-situ*. The temporal intensity profile of the excimer laser beam is acquired using a Si pin photodetector placed behind one of the turning mirrors. The output of this detector and that of the APD are collected by the oscilloscope, which are in turn collected by the computer system controlling the X-Y stages and the laser.

The laser beam energy measurement is made by placing a beam splitter in the laser beam path following the other beam splitters at a small angle ($\leq 5^{o}$) relative to the incoming laser beam, as shown in Fig. 2.1. After passing through several beam splitters, the laser beam becomes partially polarized. The reflectivity of a beam splitter varies for different partially polarized light because of the difference between the reflectivity for the "S" and "P" components of the light. This setup minimizes the difference of the reflectivity of the "S" and "P" components of the laser beam. As shown in Fig. 2.2, the smaller the angle of the laser beam with respect to the beam splitter, the less difference between the reflectivity of the "S" and "P" components. The J50 thermal detector and JD-2000 Joul meter are used to integrate the total energy of the reflected beam and transfer the data to the computer. With the help of the beam profiling tools described below, the data can be easily

converted to the laser energy fluence put down on the sample by a constant attenuation factor depending on how much fraction of the beam energy is lost when the beam passes through the homogenizer and the turning mirrors. The thermal detector and the Joul meter constitute a laser energy probe, which can be used *in situ*, as are the HeNe reflectivity probe.

The final module incorporated into the laser system allows spatial beam profiling and precise laser energy fluence data conversion. The beam profiling system consists of a Cohu CID camera, a frame grabber and a PC interface card, an IBM PC, and analysis software obtained from Big Sky Corporation. The ability to profile the beam and insure its homogeneity is perhaps the most critical requirement for accurate characterization of the process. Without detailed knowledge of the spatial uniformity, size and energy of the beam described above, it is difficult to accurately determine the energy fluence. Further-

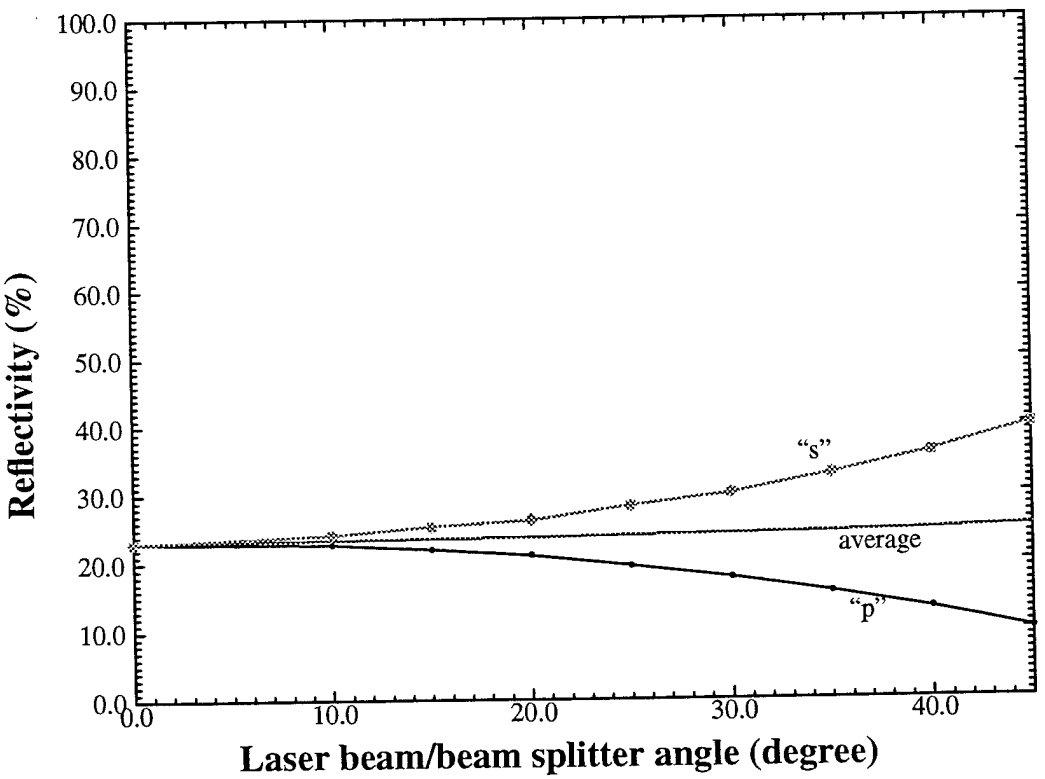


Fig. 2.2. Simulation results of the reflectivity of a beam splitter for a 308 nm laser beam with different polarization condition at different angles. The beam splitter has a nominal reflectivity of 23(±5)%. Courtesy of Acton Research Corporation, Acton, MA 01720.

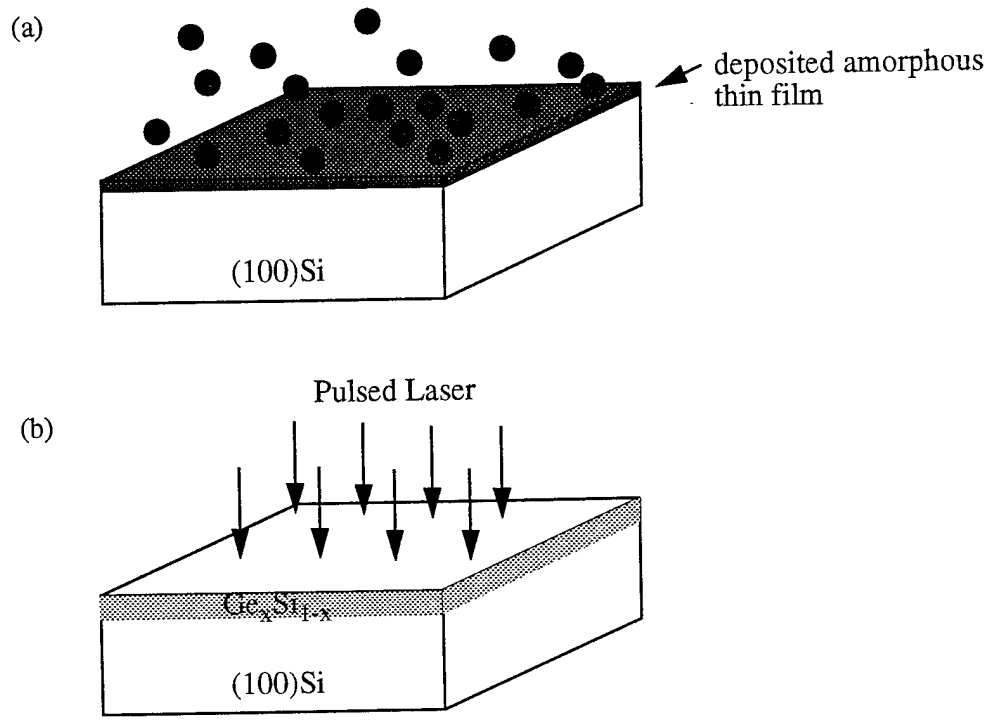


Fig. 2.3. Schematic process flow to illustrate the PLIE process using heteroepitaxial Ge_xSi_{1-x}/Si(100) formation as an example. (a) A thin layer of amorphous Ge film is deposited onto a Si(100) substrate by e-beam evaporation. (b) Pulsed XeCl excimer laser melts through the amorphous layer and part of the substrate to form an epitaxial layer of Ge_xSi_{1-x}.

more, nonuniformities of the beam intensity can cause erroneous results and create thermal gradients across the molten region which lead to breakup of the recrystallization front, resulting in the growth of highly defected layers. The typical homogenized beam has an intensity variation of ±3% across the central 3 mm of the spot. We have used both materials and electrical measurements, combined with modeling, to characterize the melt-doping process.

2.3 Fundamental Principles of the PLIE Process

PLIE is essentially a technique developed from the previously reported pulsed laser annealing and recrystallization process [2.3-2.5]. Initial studies indicated that by

using a Q-switched pulsed ruby or Nd-YAG laser to melt through a thin layer of deposited amorphous silicon, either doped or undoped, epitaxial layers structurally identical in quality to the under lying single crystal silicon substrate could be fabricated. In this work, the Q-switched ruby or Nd-YAG laser is replaced by an excimer laser operating at a wavelength of 308 nm.

Fig. 2.3 illustrates the fundamental principals of the PLIE process using heteroepitaxial Ge_xSi_{1-x}/Si(100) formation as an example [2.6]. First, an amorphous thin film is deposited onto a semiconductor substrate by, in this study, e-beam evaporation. If desired, dopant atoms can be incorporated in and/or onto the deposited film at the same time. PLIE is somewhat insensitive to interfacial contamination existing at the amorphous layer/substrate interface. Therefore, we believe the CVD techniques such as plasma enhanced CVD (PECVD) and low-pressure CVD (LPCVD), generally used in present day manufacturing lines can also be used for the deposition step.

Once the amorphous layer is deposited, the wafer is transferred to the laser system. It is mounted in a gas cell which can be purged and filled with either inert gases or a gaseous dopant species. Areas of the wafer are irradiated by the pulsed XeCl excimer laser. The laser energy is controlled such that the deposited thin film as well as part of the substrate is melted through. The melt depths and compositions of the melted layer are controlled by two independent adjustable laser parameters i.e. energy fluence or melt duration, and number of pulses.

Fig 2.4. illustrates the melting/re-solidification process for a Si(100) substrate following a single pulse laser irradiation at an energy fluence of 0.82 J/cm^2. The melting starts at the surface of the substrate and gradually reaches a maximum velocity. The re-solidification begins at the maximum melt depth and proceeds toward the surface as the latent heat is dissipated into the underlying cooler substrate.

For the case of a thin film Ge layer on a Si substrate, both the deposited Ge and any other deposited species will redistribute in the molten region. The distribution of each

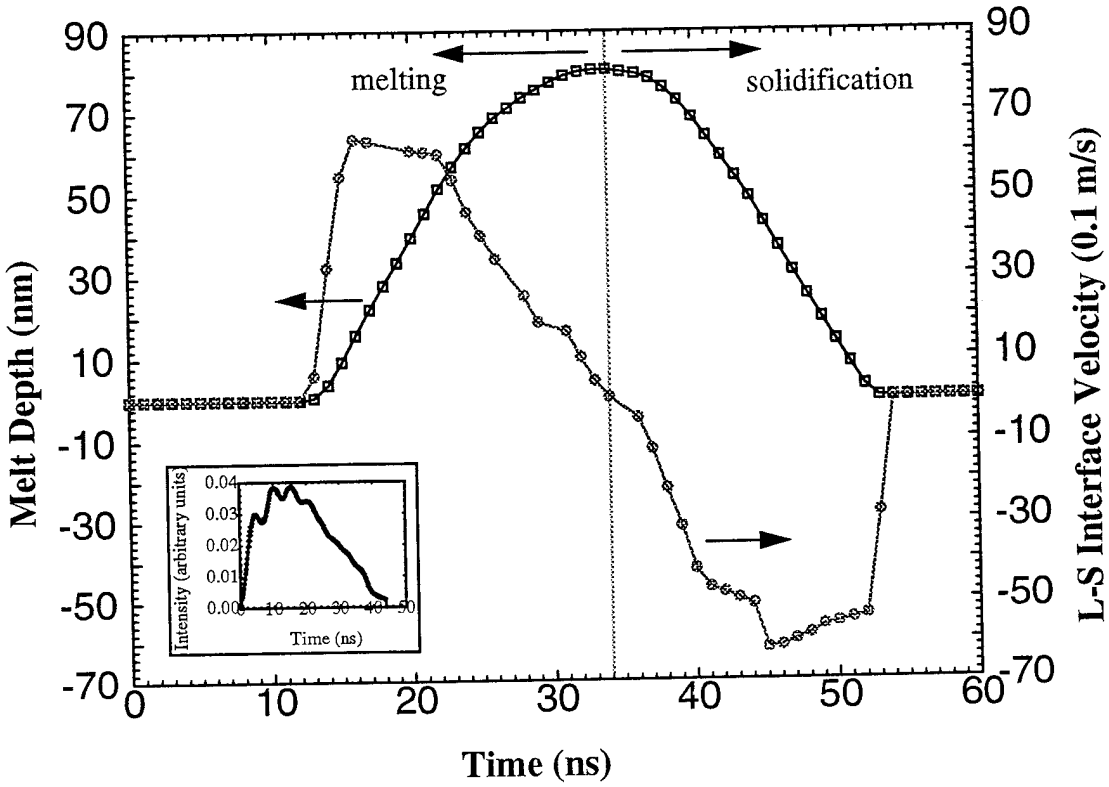


Fig. 2.4. Simulated melt/re-solidification process using the LASERMELT simulator for a Si(100) substrate during one laser irradiation pulse at an energy level of 0.82 J/cm^2. The inset shows the digitized laser pulse used for the time domain calculation.

atomic species in this molten layer is of concern since their redistribution behavior determines the final electrical properties of the layer, such as the bandgap and Fermi level. It has been reported by Gladush *et. al.* [2.7] that liquid-phase diffusion and convection may contribute to the redistribution of the atoms in such a molten layer. The strong convection currents, caused by lateral temperature gradient induced surface tension gradients, may produce more efficient mixing than is possible by liquid phase diffusion. In their work, the laser used was a scanned beam and created temperature gradients laterally to the beam axis as well as along the scan direction.

In our work, lateral temperature gradients are believed to be of minor importance because of the excellent laser beam uniformity achieved in our system. Hence, the dominant redistribution mechanism in the molten region in our process is liquid phase diffu-

sion. The diffusion coefficients for this process are typically on the order of 10^{-4} cm^2/sec for semiconductors [2.2]. The fast liquid phase diffusion i.e. mixing in our case results from several possible factors; such as vertical temperature gradients, thermal stress acting through the piezoelectric effects and photovoltaic effects [2.8]. These phenomena are observed for several material systems [2.9, 2.10]. In Fig. 2.5, we show a cross-sectional TEM image of Ge_xSi_{1-x}/Si grown by PLIE for a 50 ns surface melt duration. The distinctive contrast between the alloy region and the substrate suggests excellent composition uniformity in the once-molten layer, attributed to the fast liquid diffusion of Ge in the vertical direction in the Ge-Si material system and the use of only one laser pulse. This is one of the many factors which make PLIE a technique suitable for ultra-small dimension Ge_xSi_{1-x}/Si wire fabrication, particularly when using the lift-off technique where side diffusion is an issue, as we discuss later in Chapter 6.

The composition uniformity of the alloy region may be modified by using multiple irradiation pulses. Since each pulse results in a melt-solidification process, all species in the molten region have a chance to redistribute. Typically, the composition profile reaches

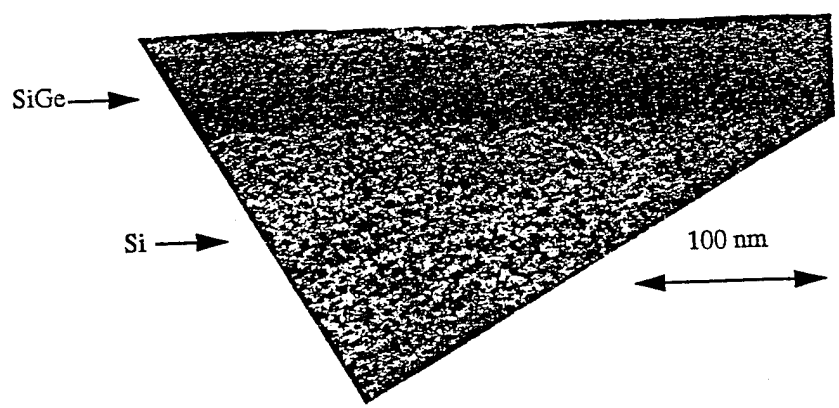


Fig. 2.5. TEM image of SiGe formed by 1 laser irradiation on a 7 nm Ge/Si substrate.

a quasi-equilibrium situation for the Ge-Si system after a few pulses [2.11]. Afterwards, segregation effects dominate the composition redistribution. A detailed review of this subject is presented in reference 2.2.

The PLIE process is essentially a very rapid liquid phase epitaxial process. The recrystallized crystal structure preserves the atomic arrangement of the substrate. In the case of heteroepitaxy, strained layers are formed, as observed in the Ge_xSi_{1-x}/Si system. In order to obtain high quality epitaxial layer, uniform epitaxial growth is essential. It has been previously reported that polycrystalline and cellular formation is resulted from the laser-induced recrystallization process [2.12]. However, the lasers used in that work, both continuous and pulsed types, are known to have significant spatially nonuniform beam intensities. These intensity variations create inhomogeneous melt front and result in random nucleation for the recrystallization process. This problem is resolved by using a uniform laser beam.

Although PLIE is a reliable fabrication technique, there exist several factors that are not fully understood, such as high temperature gradients, thermal stress and pressure exerted by the pulsed laser, as pointed out in reference 2.8. New phenomenon in the PLIE process are continually being discovered, such as surface evolution in the fabrication of ultra-small SiGe wires, which we discuss in Chapter 6. Future work is needed in order to establish a complete theoretical understanding of the mechanisms of the PLIE process.

2.4 System Characterization

In order to precisely control the PLIE process for fabrication of ultra-narrow SiGe wires, the system needs be well characterized. The critical parameter to be monitored in the PLIE process is the melt depth. It determines the epilayer thickness and in turn determines the concentration of the species in the epilayer. This parameter is directly related to the laser energy fluence and may be measured by monitoring the surface melt duration.

The GILD process is performed on well characterized Si substrates and together

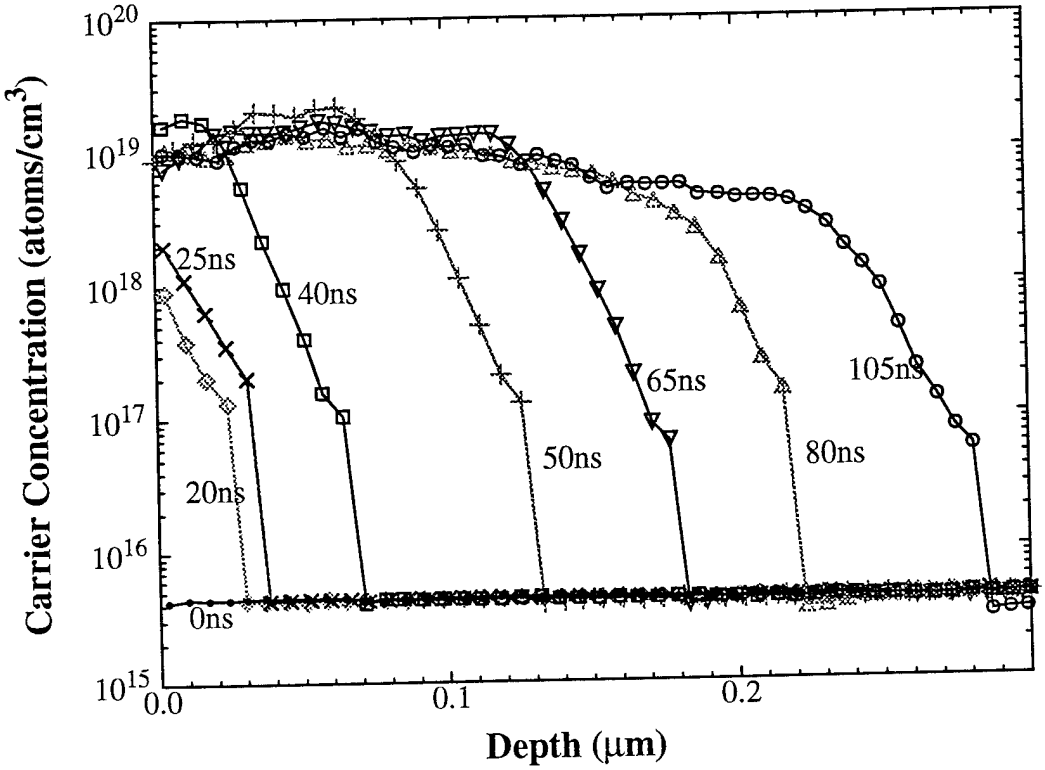
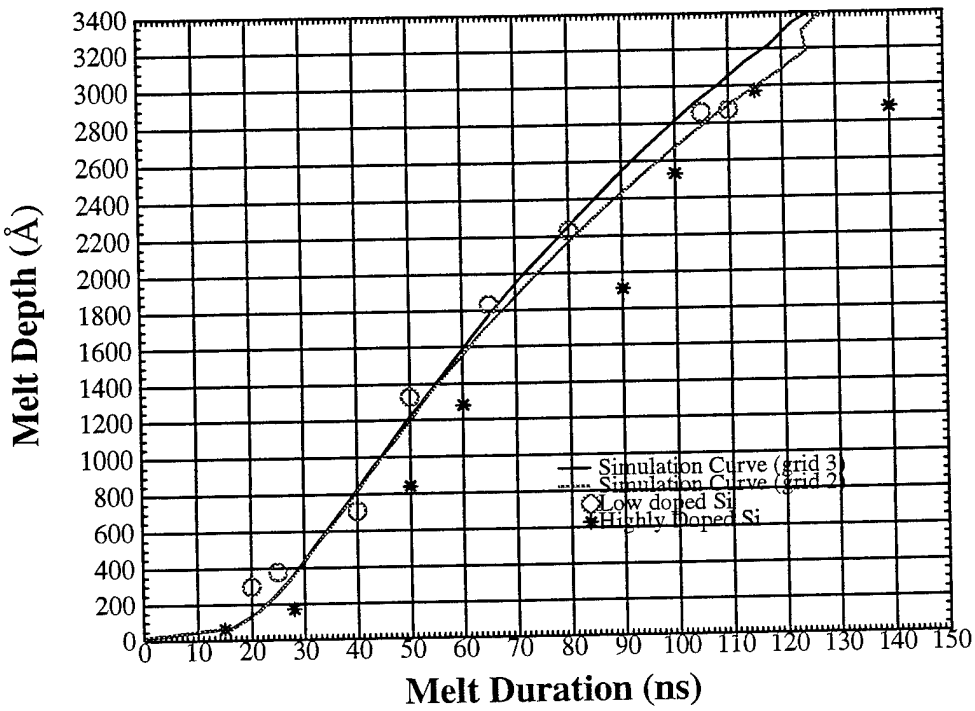


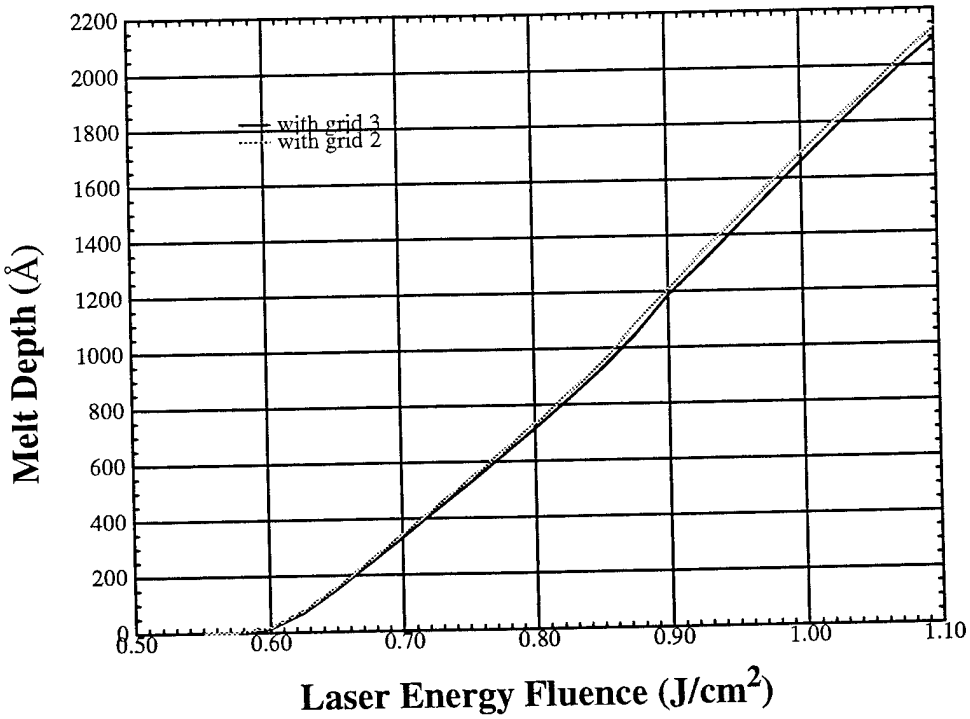
Fig. 2.6. Results of spreading resistance profilometry (SRP) conducted on p^+n junctions formed by gas immersion laser doping process. Ten laser pulses are used for each sample. The associated surface melt durations for each sample are indicated on the figure.

with the LASERMELT simulator to monitor the system. The GILD process is similar to the PLIE process, except for the fact that it basically is used to incorporate dopants in the surface layer through the gas phase rather than creating a change in the actual material through epilayer growth. Because of the nanosecond thermal cycles and the fast diffusion of dopants in the molten region, dopant atoms only diffuse up to the liquid/solid interface forming a box-like profile after multiple laser pulse irradiation; solid state diffusion during the ultra-fast heat cycle being negligible. The epitaxial regrowth occurring during the solidification process of the doped layer results in the impurities being incorporated onto substitutional lattice sites and these dopants are therefore electrically active.

Fig. 2.6 shows impurity profiles obtained using spreading resistance profilometry (SRP) on low-doped n(100) Si substrates processed by GILD in a BF_3 ambient. The BF_3



(a)



(b)

Fig. 2.7. (a) LASERMELT simulation results for experimental data. (b) LASERMELT simulation showing the relationship of melt depth and laser energy fluence.

gas pressure in the gas cell before laser irradiation is 50 torr. Each sample is irradiated with ten pulses at different energy fluence by the homogenized laser beam. The experimental results are fit with the LASERMELT simulator, and are shown in Fig. 2.7(a). In this figure, a finer grid is used for the simulation marked "grid 2". The abrupt change of the curve between 120 - 130 ns is caused by the grid setting used in the calculation. Note, that the experimental results for a highly doped n(111) substrate (dopant concentration = 1.5×10^{19} atoms/cm^3) are also shown. They do not fit the simulated results since the properties of the highly doped silicon substrates are changed by doping. Fig. 2.7(b) is the plot of simulated results showing the relationship of melt depth and laser energy fluence.

2.5 References

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Chapter 3

APPLICATIONS OF SIGE NANOWIRES

3.1 Introduction

Because of the complexity involved in the processing techniques, there are no demonstrations of the application of SiGe wire structures to date. Most research activities are focused on the fabrication techniques, rather than electrical properties, even though it is of great interest.

In this chapter, we will discuss two applications of SiGe wires. One is quantum wire based and which we will propose the fabrication of a novel device. The other is a lateral heterojunction bipolar transistor (HBT) whose performance is demonstrated on a two-dimensional device simulation tool - MEDICI.

3.2 SiGe Quantum Wires

One application of SiGe wires is two dimensionally confined quantum devices. Coherently strained Ge_xSi_{1-x} has a smaller bandgap than Si. The bandgap [3.1] can be approximated by the relationship

$$E_g(x, T) = E_0(T) - 0.96x - 0.43x^2 - 0.17x^3 \tag{3.1}$$

where T is the temperature, and $E_0(T)$ is the bandgap of Si. Most of the bandgap offset is located at the valence band edge. The offset at the valance band can be approximated [3.2] by

$$\Delta E_v = 0.74x \tag{3.2}$$

for strained $Ge_{1-x}Si_x/Si$. Therefore, holes will be driven into the alloy region. When a SiGe wire embedded in Si has a cross-section dimension smaller than the carrier deBrolie wavelength, the energy levels in the well are quantized, resulting in two-degreeless freedom of motion and forms the so-called "quantum wire".

As shown in Fig. 3.1, The density of states in such a 2-D confined quantum structure shows a significant discrete nature when compared to that of 1-D confined structure. Hence, tunneling behavior of the carriers, as seen in a resonant tunneling transistor, can be expected. In addition, an enhanced mobility along the quantum wire is possible [3.3], because of suppression of ionized-impurity scattering.

Fig. 3.2. shows a quantum wire MOSFET based on SiGe wires in Si. A thin undoped Si epi-layer is first grown on a p-type Si substrate followed by SiGe wire formation in the epi-layer. The electrical contacts can be formed on both ends of the wire utilizing the conventional metalizing technique. A gate structure (as an option) can be made over the wire with a thin deposited SiO_2 in between. This gate structure could be used to change the transport behavior of the carriers through the wire, thus providing a three terminal device.

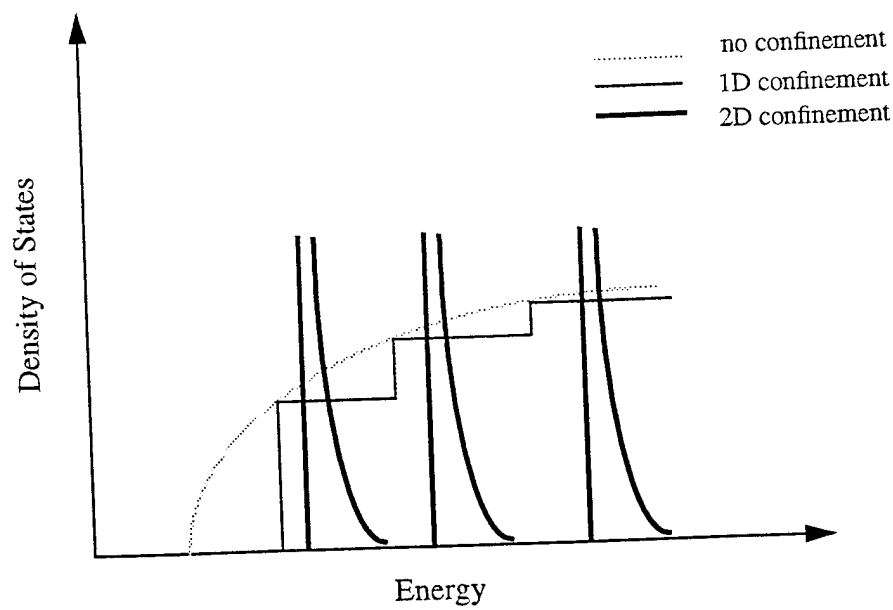

Fig. 3.1. Schematic of the density of states versus energy for the semiconductor with no confinement, 1D confinement, and 2D confinement.

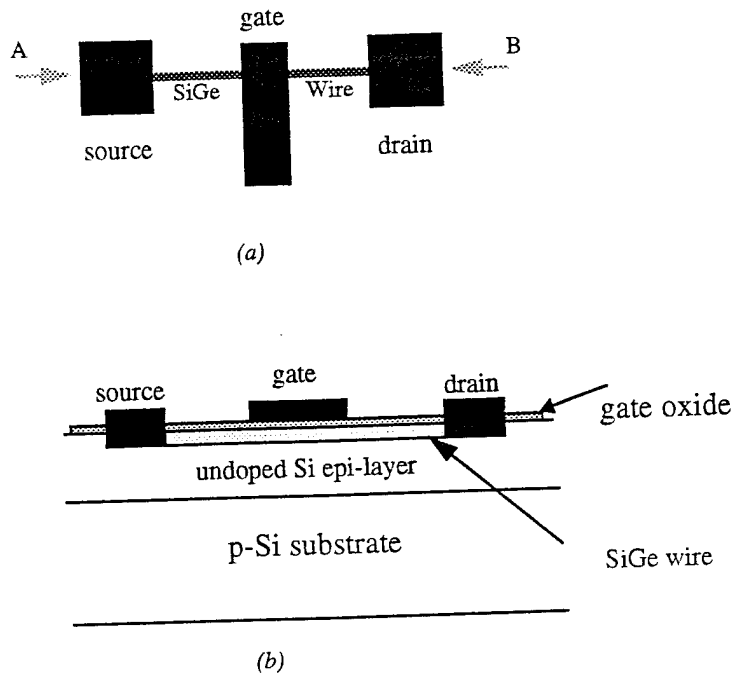

Fig. 3.2. Schematic of the quantum wire device (a) top view and (b) cross-section along A-B.

3.3 SiGe Lateral HBT

As discussed in 3.2, strained $Ge_{1-x}Si_x$ has a bandgap narrower than Si. A bandgap difference in the order of 200 mev (8kT) can be obtained when the Ge mole fraction is about 20%. In a bipolar transistor, the current gain [3.4], as limited by emitter injection efficiency, can be approximated by

$$h_{fe} = \frac{n_E}{p_B}\frac{v_e}{v_h}\frac{N_{CB}N_{VB}}{N_{CE}N_{VE}}\exp\left(\frac{\Delta E_g}{kT}\right) \tag{3.3}$$

where n_E is the emitter free electron concentration, p_B is the base free-hole concentration, N_{CB} and N_{CE} are the densities of states in the conduction band for the base and emitter, N_{VB} and N_{VE} are the densities of states in the valence band for the base and emitter, v_e and v_h are the effective velocities of electrons and holes, and ΔE_g is the bandgap difference between the emitter and base, i.e. $E_{gE} - E_{gB}$. Therefore, incorporation of Ge into the base of the transistor will dramatically enhance the emitter injection efficiency in a NPN

BJT. This allows obtaining an increased current-gain cut-off frequency f_t which, in general, reflects the speed performance of the transistor, and/or increased maximum frequency of oscillation f_{max} [3.4] which is approximated by

$$f_{max} = \left(\frac{f_t}{8\pi R_B C_{BC}}\right)^{1/2} \tag{3.4}$$

where R_B is the base resistance, C_{BC} is the base-collector capacitance.

Since their first demonstration in 1987 [3.5, 3.6], SiGe HBTs have attracted great attention. Commercial application of these devices are a reality. However, all of the work to date has concentrated on vertical structures rather than lateral, due to a lack in the selective epitaxial growth technology for SiGe.

In this section, we present a brief review of current lateral bipolar junction transistor (BJT) technology, We then propose a novel NPN SiGe lateral HBT and its processing procedures based on PLIE. Finally, we discuss the performance of this device and a conclusion is given.

3.3.1 A Review of Lateral Bipolar Transistors

Lateral bipolar structures are commonplace in silicon technologies, but not well developed for high speed, high frequency applications. Table 3.1 lists the performance of the state-of-the-art lateral BJTs fabricated using different technologies. The renewed interest in high performance lateral BJTs are driven by the prospect of incorporating BJT and CMOS on the same chip using a simplified, CMOS like, BiCMOS technology [3.7] to exploit the high speed of CMOS and high power of BJTs at the same time. One solution would be using the parasitic BJTs [3.8,3.9] which are inherently available in a CMOS process. One could make use of either the vertical BJT which has the substrate as its collector or the lateral BJT between the source and drain junctions of the MOSFETs [3.10,3.11]. However, the vertical BJT can only be used in a common collector configuration since the collector is always tied to the substrate potential. The parasitic lateral BJT has a low cur-

rent gain, low current driving capability, and large base transit time.

Recently, S. Verdonckt-Vandebroek et al [3.12] demonstrated a high gain lateral BJT formed by tieing together the gate and well of a MOSFET. Such transistors have lower f_t-I_c performance than conventional vertical BJTs and they are more like MOSFETs than BJTs, especially at high current. A. Tamba et al [3.13] demonstrated a lateral BJT using a modified MOS process. The cut-off frequency f_t reached 6.3 GHz and no buried layer is needed. In this device, the base resistance increases with decreasing base width and scaling of the device tends to be a problem. With the advent of SOI technology, several attempts [3.14-3.16] have been made to build lateral BJTs on the substrate. The highest f_t obtained using this technology is 20 GHz with a current gain of 20.

Table 3.1: State-of-art bipolar transistors

	High Performance Vertical BJT [3.17]	High Performance Lateral BJT [3.13]	Lateral BJT on SIMOX
Base width	1300 nm	~ 500 nm	~ 100 nm
β	72	20	10 ~ 30
f_t	25 GHz	6.3 GHz	20 GHz
R_b	306 Ω	450 Ω	
R_c	20 Ω	50 Ω	
R_e	10 Ω		8 Ω
C_{jc}	11 fF		21 fF
C_{jb}	10 fF		32 fF

There are few demonstrations of lateral HBTs. To date, using wet etching and regrowth techniques [3.18], lateral InP/InGaAsP HBTs with current gain of 6 and base width of 2 μm were demonstrated. Using impurity induced disordering [3.19], GaAs/GaAlAs lateral HBTs with a current gain up to 400 were also demonstrated. The latter approach is better suited to the fabrication of monolithic laser/bipolar circuits. Neither author discussed the high frequency performance of the device. In addition, both

approaches are based on III-V materials. However, these approaches demonstrate the possibility of fabricating laterally structured HBTs.

In the following, we propose a novel lateral HBT design based on SiGe/Si heterojunctions. Simulation using MEDICI shows f_t's could reach as high as 36 GHz with current gains of ~ 250 and a base width of 50 nm.

3.3.2 Design and Simulation

Fig. 3.3. (f) and (g) shows the cross-section and layout of the device. The emitter is surrounded by the $Si_{1-x}Ge_x$ base in order to make full use of the emitter area. Base contact is made through the buried layer which is partially overlapped by the SiGe base. A suggested process flow based on GILD and PLIE is shown in Fig. 3.3 (a)-(f). The GILD process is described in detail in ref. 3.20. Al/SiO_2 masks are used in the process for patterning and shielding the rest of the substrate from the laser beam. A boron-doped is first formed using the GILD technique in a selected area. Then a buried layer is formed in the p-well using ion implantation along appropriate channel direction followed by thermal annealing or using multiple laser irradiation [3.20, 3.21]. The edge area of the p-well is then further doped with boron for the base contact later on. The center area of the p-well is counter-doped with n-type donors to create an n-well in the p-well, as shown in Fig. 3.3(b). The SiGe base region is selected in the n-well and the SiGe alloy is formed using either lift-off techniques or regular lithography, followed by PLIE, as described in this report. If a lift-off technique is used, base dopant needs to be incorporated into Ge at the time Ge is deposited, or to be put down in a solid form together with the Ge. If regular lithography is used, the base dopant can be incorporated at the same time of PLIE using GILD. After stripping-off Al/SiO_2, if there is any, a thin SiO_2 layer is redeposited and openings are made for contacts. Emitter contact is made through n^+ poly-Si, preferably. Base-collector capacitance is controlled by the position of collector contact relative to the location of the base region, or a lightly-doped poly-Si collector. The effect from the parasitic vertical BJT

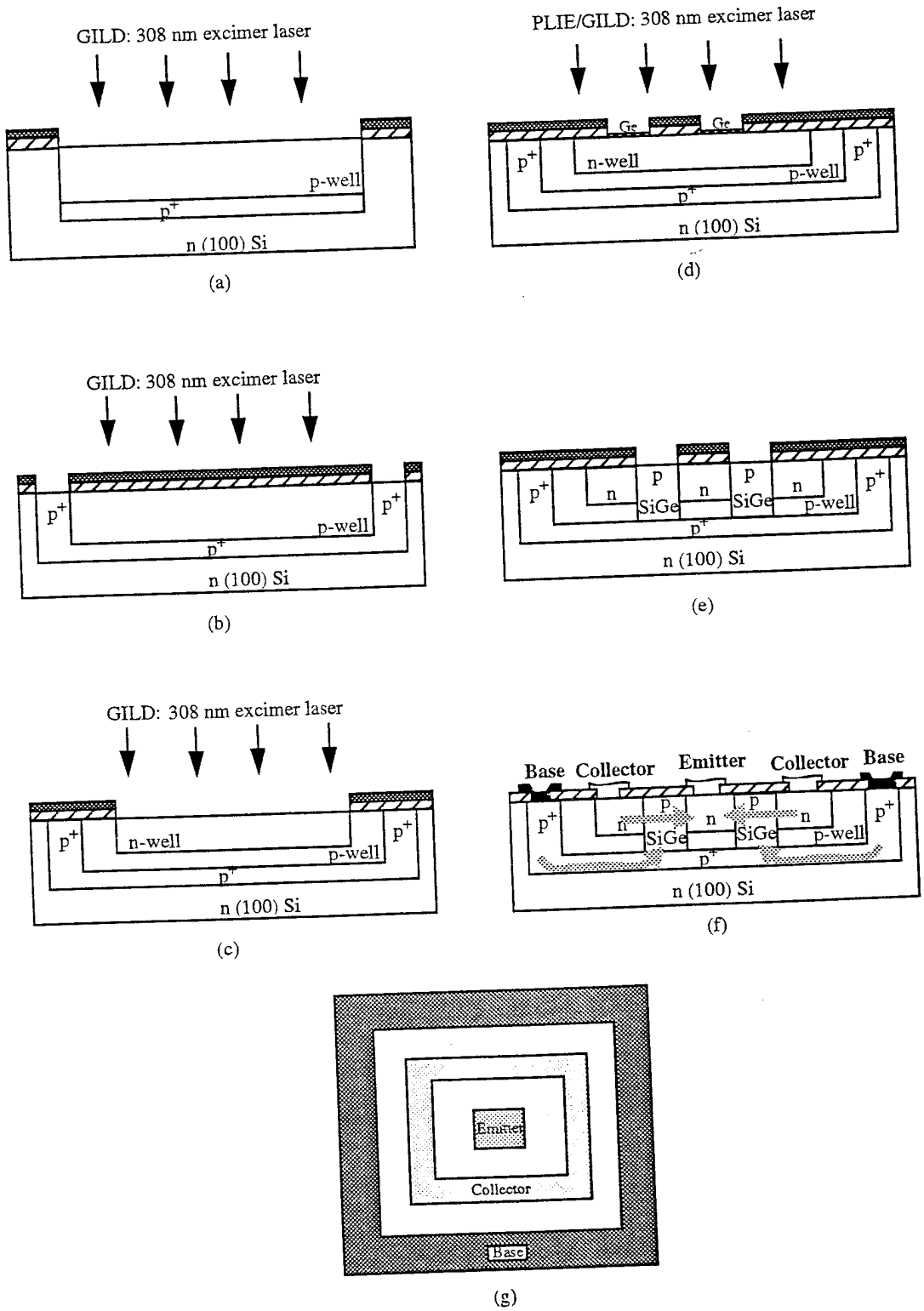

Fig. 3.3. Schematic illustration of the process flow (a)-(f), using Al/SiO_2-masking (Al, SiO_2) and the layout (g). Current flow direction is shown in the cross-section view of the final device (f).

between the emitter and the substrate is suppressed by the highly doped buried layer. Except for the Ge incorporation step, the process is fully compatible with an advanced CMOS process.

Simulation of the device was performed using the MEDICI device simulator. MEDICI is a simulation program that can be used to model the two-dimensional distributions of potential and carrier concentrations in a device such as MOSFET or BJT to predict its electrical characteristics for any bias condition. It solves Poisson's equation and both the electron and hole current continuity equations to analyze devices and effects in which the current flow involves both carriers. AC small signal analysis at a given frequency can also be performed to calculate frequency dependant capacitances, conductances, and admittances. For the strained SiGe/Si, a piecewise linear approximation to the lower curve of the strain split data shown in Fig. 2 of [3.22] is implemented for the energy band alignment. The actual bandgap value of the strained $Si_{1-x}Ge_x$ used in the MEDICI is converted from the data obtained in ref. [3.22], as shown below:

$$E_g(x) = E_g(90) - 4.0\,(E_g(90) - 0.950)\,x,\ x \leq 0.25 \tag{3.5}$$

Where Eg (90) is the bandgap value at a temperature of 90 K.

In the simulation, a cylindrical structure of the device is used instead of a square structure shown in Fig. 3.3(g). The right half of the cross-section of the cylindrical structure is shown in Fig. 3.4. The radius of the emitter region is chosen to be 0.1 micron. Box-like doping profiles were used for all the doped regions in the device. The depth of the emitter and collector was chosen to be 50 nm, which can be easily made using the GILD process [3.23]. The depth of the SiGe region was 100 nm [3.24] with constant concentration of Ge (20%) in the first half and linearly graded to zero in the second half. The doping profile along the surface of the device is shown in Fig. 3.5. Half of the emitter and collector region was used for contact, as shown by the dashed line in Fig. 3.4. Current flow also shown in Fig. 3.5 is concentrated in the first half of the base region and unlike MOSFETs, almost uniformly distributed in this region.

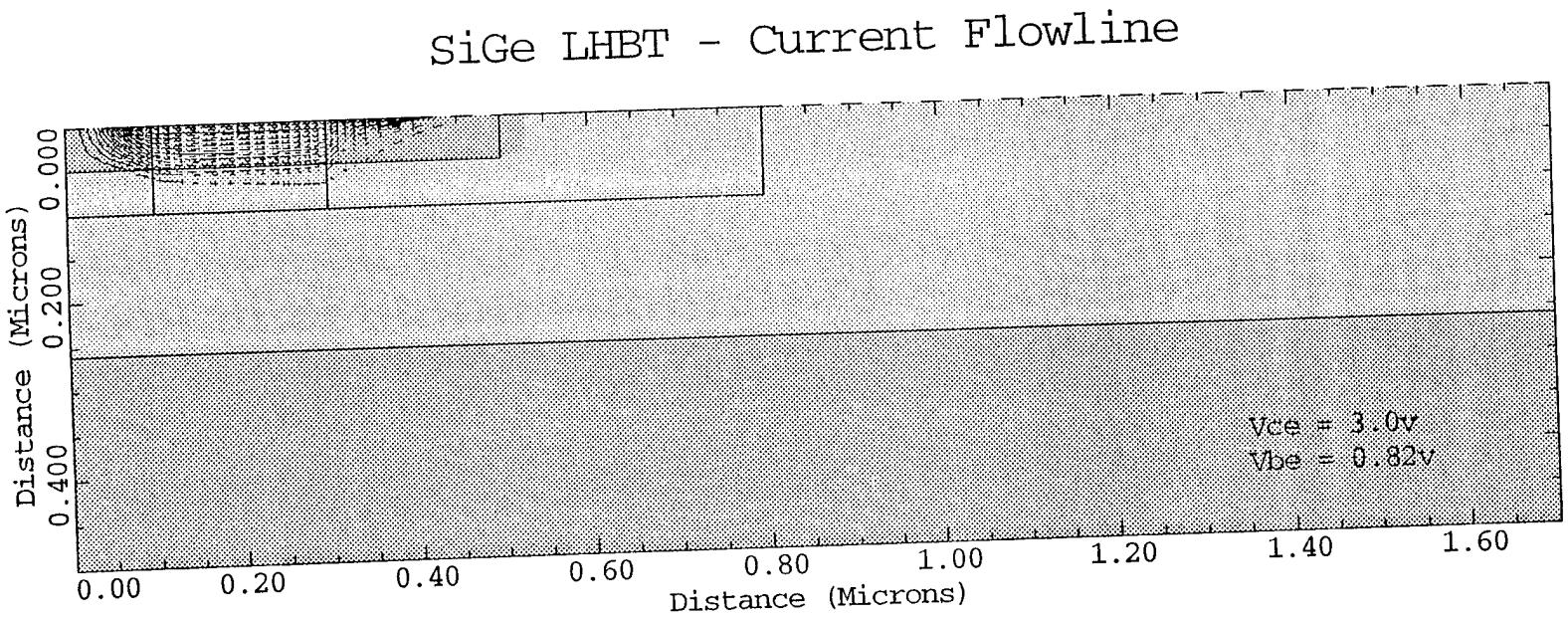

Fig. 3.4. Cross-sectional view of the SiGe lateral HBT (right half of the cylindrical structure). The dotted lines are current flow lines when Vce = 3.0 V and Vbe= 0.82 V. The dashed lines indicate the contact region.

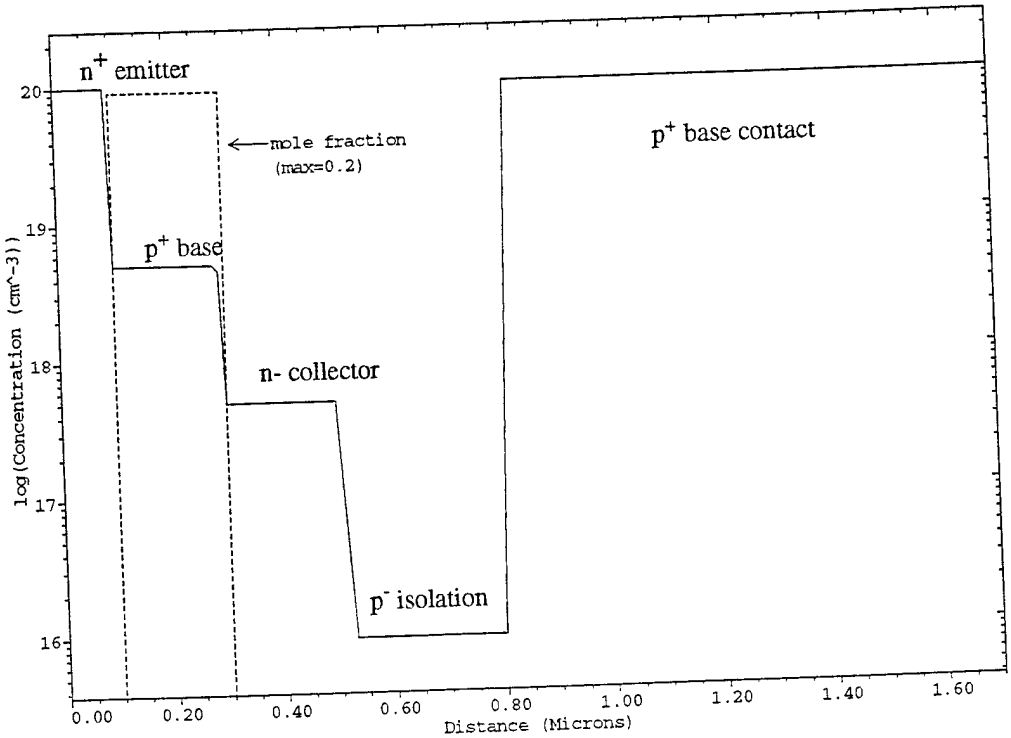

Fig. 3.5. Doping profile along the surface of the SiGe lateral HBT with a base width of 0.1 μm.

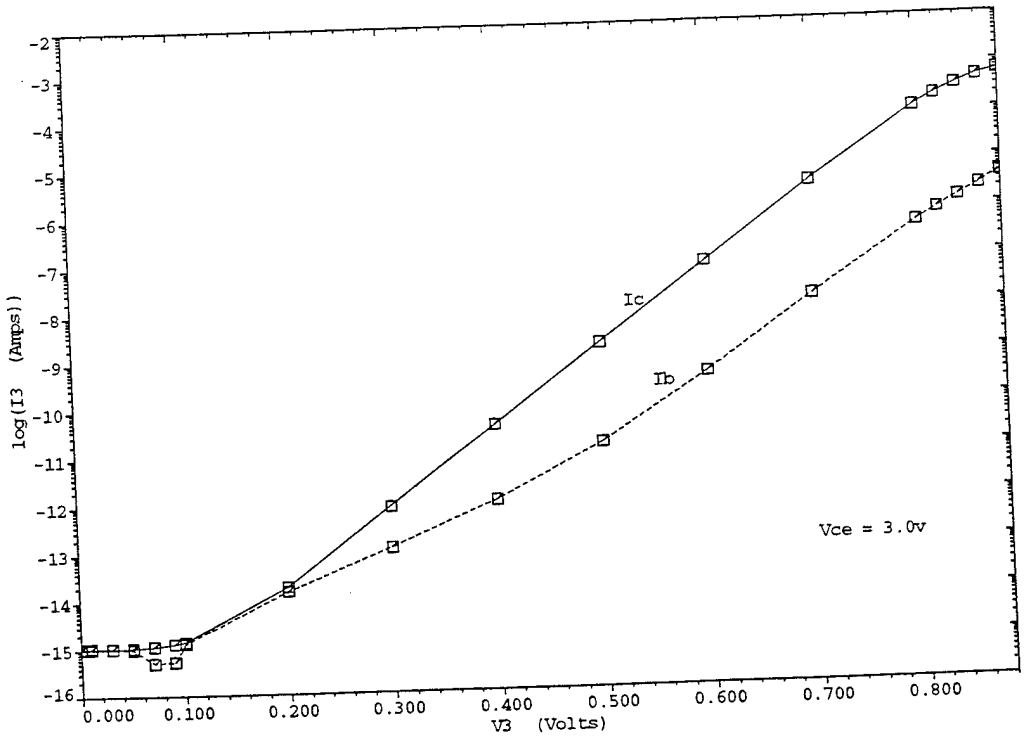

Fig. 3.6. Simulation results of the gummel plot for the SiGe lateral HBT with a base width of 0.05 μm.

Performance of the device is very similar to a vertical SiGe HBT. The Gummel plot [Fig. 3.6] of the device shows the typical characteristic of a BJT. The zero bias emitter junction capacitance is found to be 0.2 fF, while the collector junction capacitances are 0.42 fF, 0.56 fF and 0.84 fF corresponding to base width of 0.05 μm, 0.1 μm and 0.2 μm, respectively. Base width scaling significantly enhances the performance of the device. As shown in Fig. 3.7 and 3.8, a 200 nm wide base gives current gain of 10 and maximum f_t of 4.5 GHz. When the base width decreases to 50 nm, the maximum f_t reaches 36 GHz with a current gain of 260.

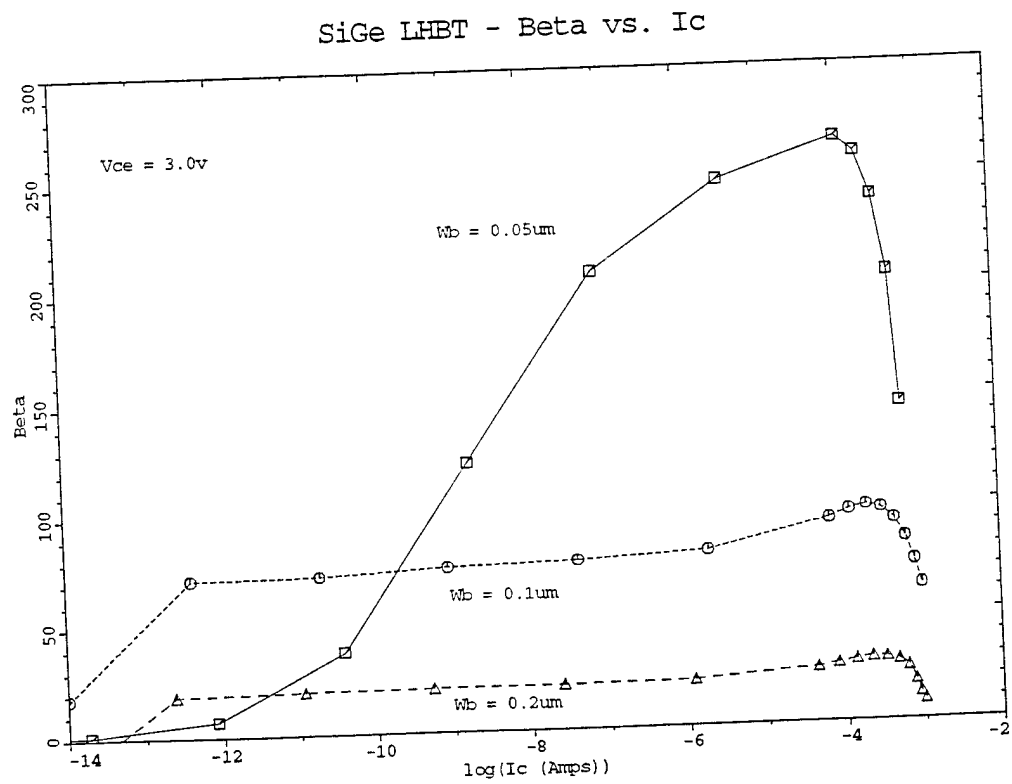

Fig. 3.7. Simulation results of Current gain v.s. collector current characteristics at three different base widths of the SiGe lateral HBT.

In summary, an advanced NPN lateral SiGe HBT is designed. Processing procedures fully compatible with advanced CMOS process with an additional mask for SiGe base formation is described for the device based on the GILD and PLIE fabrication technique. Simulation using a two-dimensional device simulator - MEDICI shows a maximum

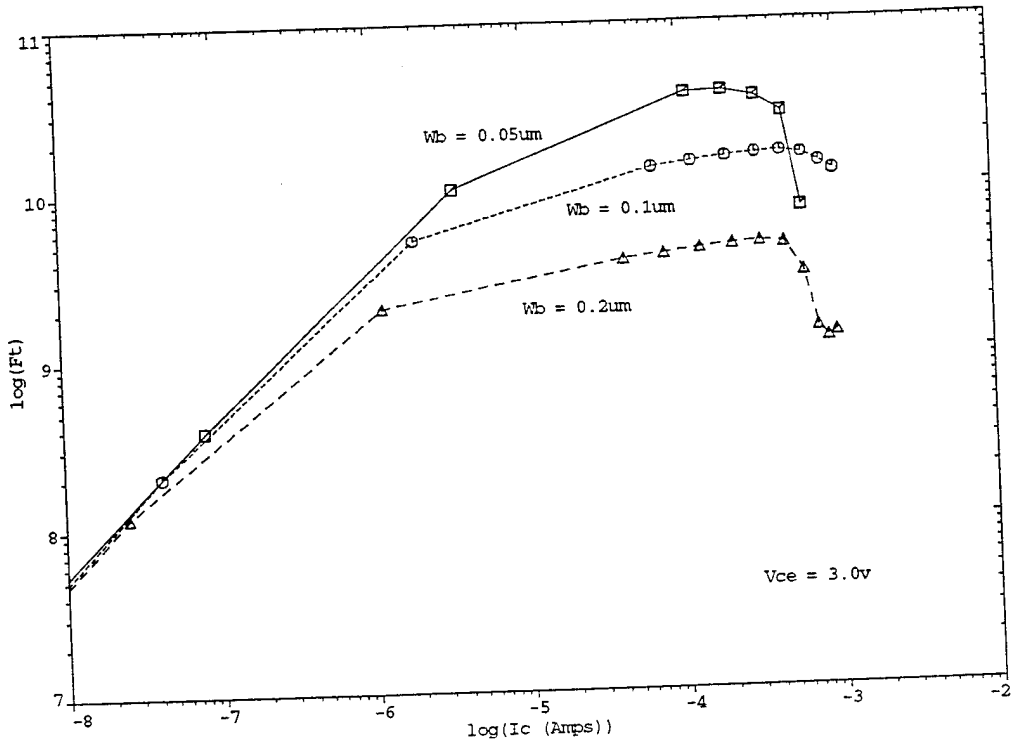

Fig. 3.8. Simulation results of cut-off frequency (Ft) and collector current (Ic) characteristics at three different base widths of the SiGe lateral HBT.

cut-off frequency of 36 GHz with a current gain of 260 can be obtained. Performance characteristics of the device is comparable to vertical HBT structures. Future work includes optimization and demonstration of the device using GILD and PLIE processing.

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Chapter 4

Ge Nanowire Fabrication Using Focused Ion Beam Micromachining

4.1 Introduction

In order to epitaxially grow SiGe nanowires, a technology to fabricate ultra narrow Ge wires on a Si substrate needs to be developed. There are a number of existing lithography technologies, such as e-beam lithography, which will be addressed in the next chapter. Focused ion beam (FIB) micromachining, however, seems to be a simple approach to form Ge nanowires directly by selectively removing a thin film Ge layer deposited on Si.

FIB technology [4.1-4.9] is made possible by the development of field emission liquid metal ion sources and their incorporation into electrostatic ion optical focusing columns. These quasi-point sources provide scanning focused ion beams with diameters less than 50 nm. Since the 1980's, FIB technology has been increasingly used for a variety of purposes such as implantation, milling, surface chemistry, lithography, microscopy, and materials analysis [4.10-16]. Focused ion beam micromachining offers a very flexible and localized method of etching materials without the need or use of a separate patterned mask. Material removal is carried out by both milling with the focused ion beam alone or by gas enhanced etching, where the surface being bombarded by the ions is also exposed to reactive gas molecules [4.17-4.19].

In this chapter, we describe our investigation into the FIB milling of amorphous Ge thin films on Si. Two processes with and without using an enhanced etch compound (Iodine) are compared. The final structures are evaluated by atomic force microscopy (AFM), scanning electron microscopy (SEM), and cross-sectional transmission electron microscopy (XTEM). Possible improvements of the processes for future work are dis-

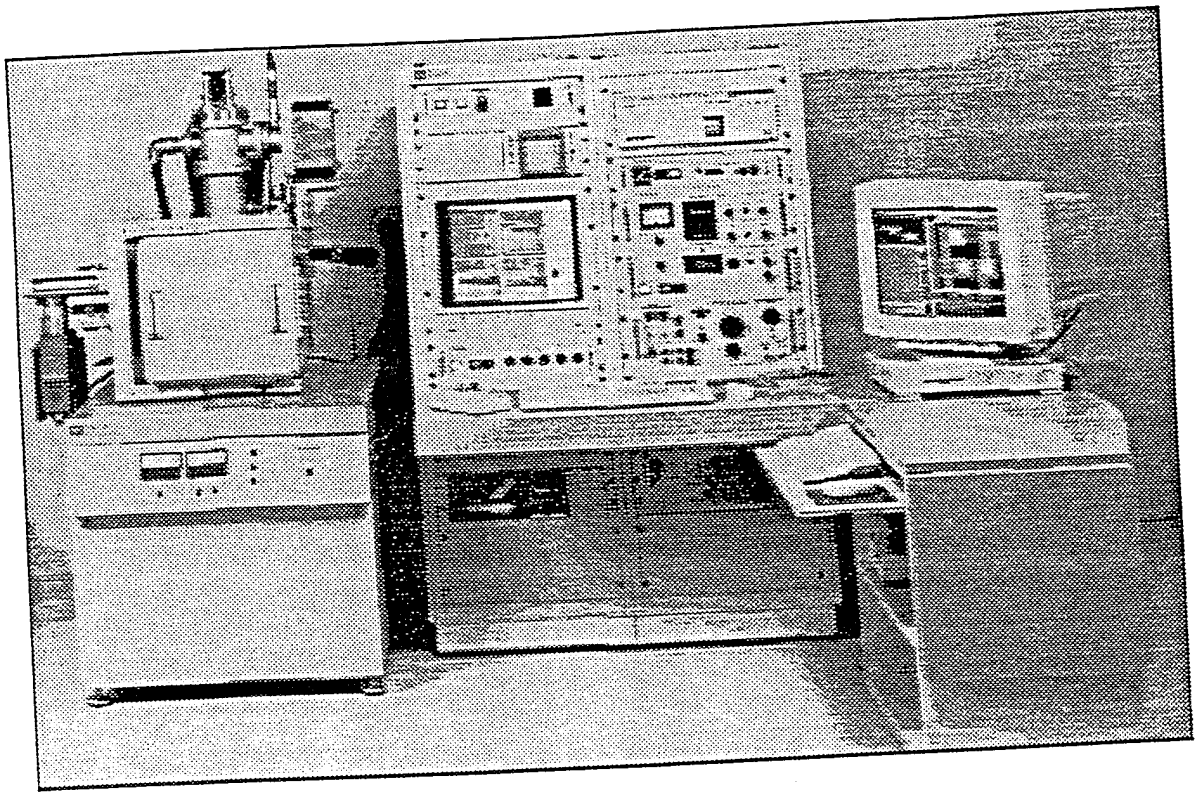


Fig. 4.1. FEI FIB 610 workstation

cussed.

4.2 Experimental Procedure

Our experiment employs an FEI FIB 610 workstation (Fig. 4.1). It has gas injection capabilities for iodine and a platinum compound. The configuration of the ion beam column and the sample stage in the vacuum chamber is shown in Fig. 4.2. For our milling experiments, the beam size of the gallium FIB is maintained around 280 Å, the beam current is kept at 6 pA with a beam energy of 25 keV. During milling, a dwell time of 1 μs of the ion beam for each pixel is used and the beam overlap between adjacent pixels is 50%. Fig. 4.3(a)-(b) illustrates the process flow for the experiment. The sample used for the experiment is a n-type Si(100) wafer. Before FIB milling, a thin film of amorphous germanium, typically 50 ~ 100 Å thick, is e-beam deposited at room temperature under a vac-

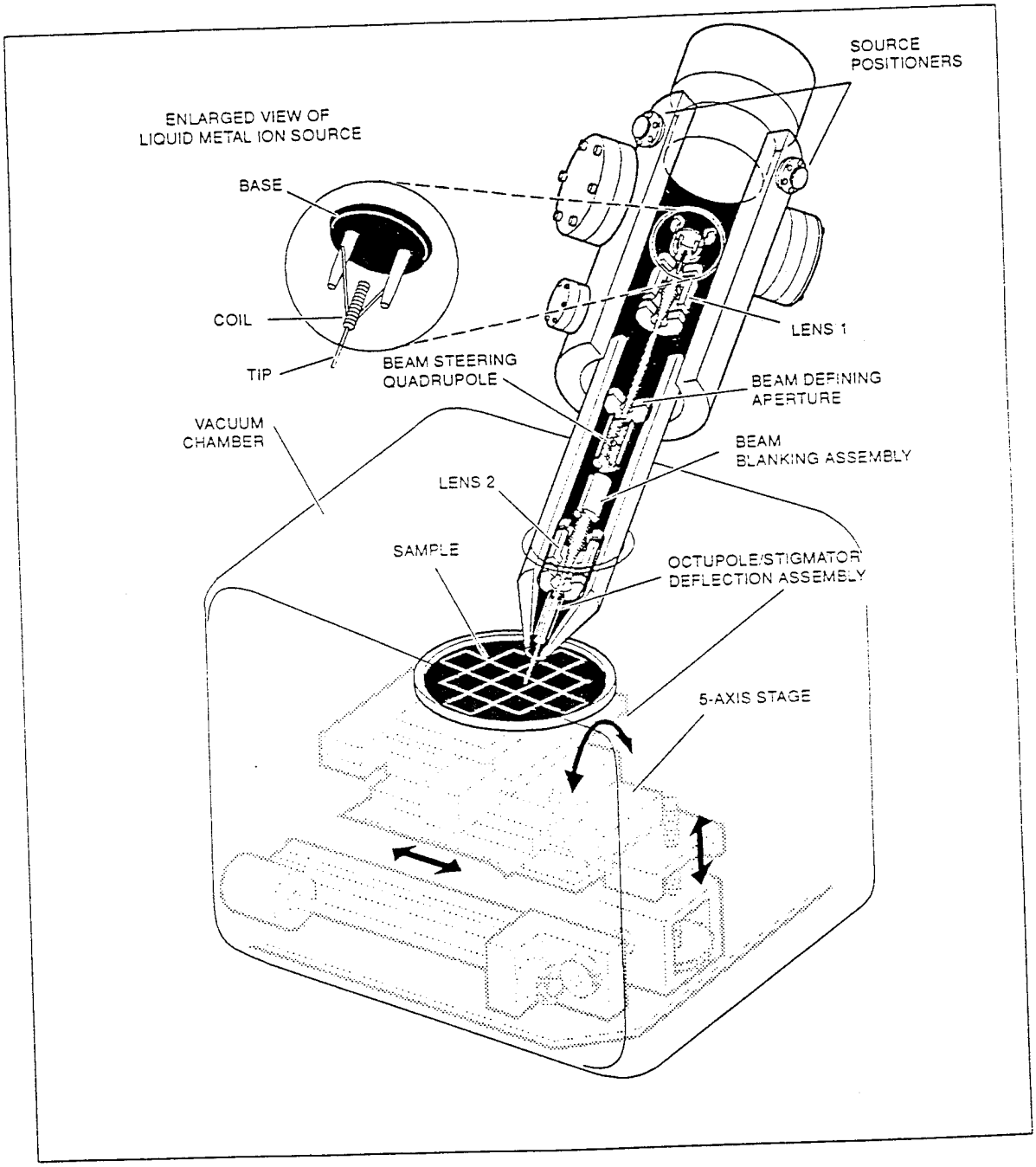


Fig. 4.2. Cross-section of the ion column and sample stage in the vacuum chamber

uum of < 10^{-7} torr. Milling patterns are created using start and end point files to ensure precise relative locations of the milled areas, as illustrated in Fig. 4.3(c). The distances between the milled strips are increased from 0.1 μm in steps of 0.1 μm from the left to right. The milled depth is controlled by the milling time. The milling starts from the left most strip, and proceeds one by one to the right. When the enhanced etch is used, iodine is

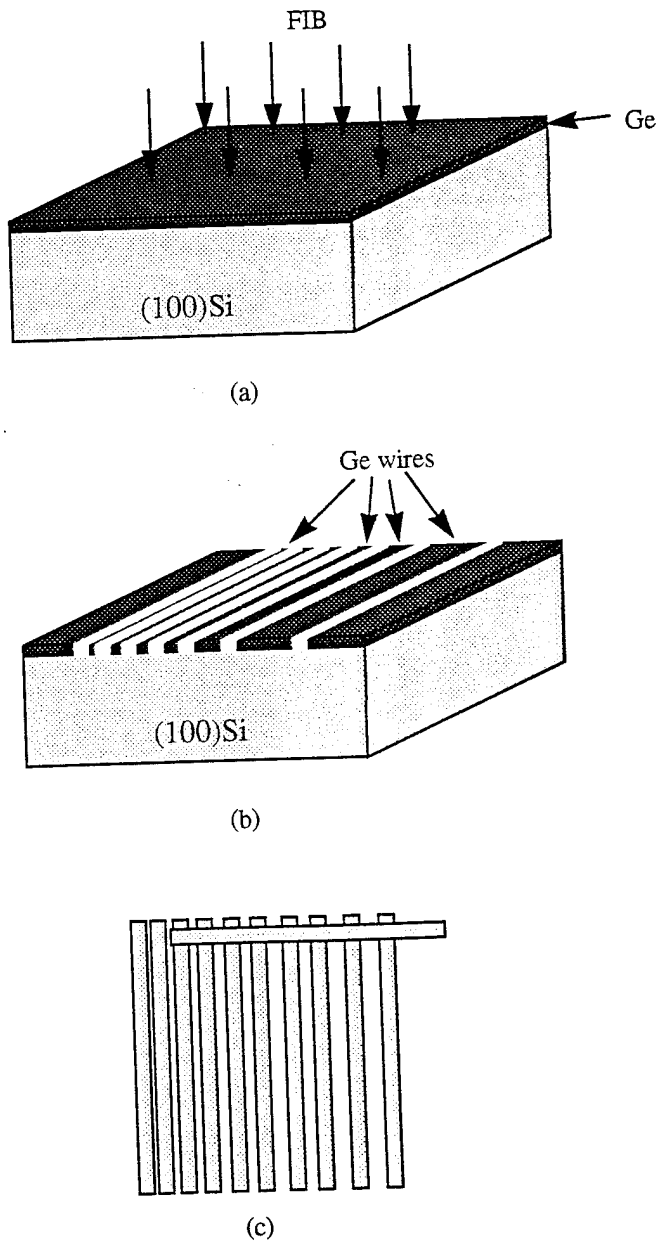


Fig. 4.3. Illustration of the FIB milling process (a-b) and milling pattern (c) created from a start and end point file. The shaded area are defined to be milled in (c).

introduced into the chamber through a small hollow needle after the iodine source is heated to 30°C. The introducing of iodine not only accelerates the milling rates, but also helps to remove the milled materials by forming volatile compounds that are pumped away by the vacuum system, preventing any material redeposition. In order to observe the significance of redeposition during FIB milling, the same pattern is also milled without introducing the enhanced etching agent. An additional strip is milled perpendicular to the standard pattern which overlaps the top part of the pattern for identification.

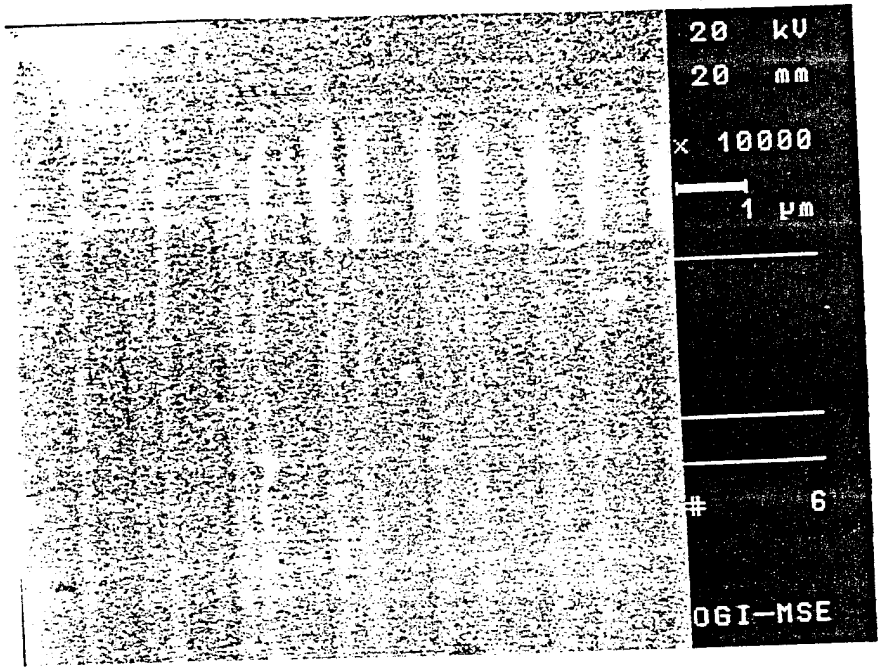
4.3 Results and Discussion

It is accepted that the materials milled from FIB micromachining would remain in the vicinity of where they are sputtered off rather than being swept away into the vacuum system. These redeposited materials are expected to adhere loosely and be mechanically unstable. However, to the author's knowledge, no research has been done to observe the significance of redeposition when only a small amount of material (such as the case in this study) is sputtered off from any type of milling target. The purpose of this experiment then was to see whether it is plausible to mill features using FIB without using an etch enhancing agent for reasons we shall discuss later in this section.

In fig. 4.4(a) we show the SEM image of the milled features without using enhanced etching. Redeposited materials are clearly seen to accumulate along the edges of the milled strips. These materials cannot be removed by additional milling without introducing modification to the substrate, even though the milling rate for the redeposited materials is expected to be significantly higher than that for the substrate. The top part of the SEM image in fig. 4.4(a) shows an area that received additional milling perpendicular to the strip pattern. It is seen that the surface is higher at the location where the materials are redeposited.

Fig. 4.4(b) shows the SEM image of the features milled using the enhanced etch process. Redeposition of materials is not observed. Instead, the substrate along the edge of

(a)



(b)

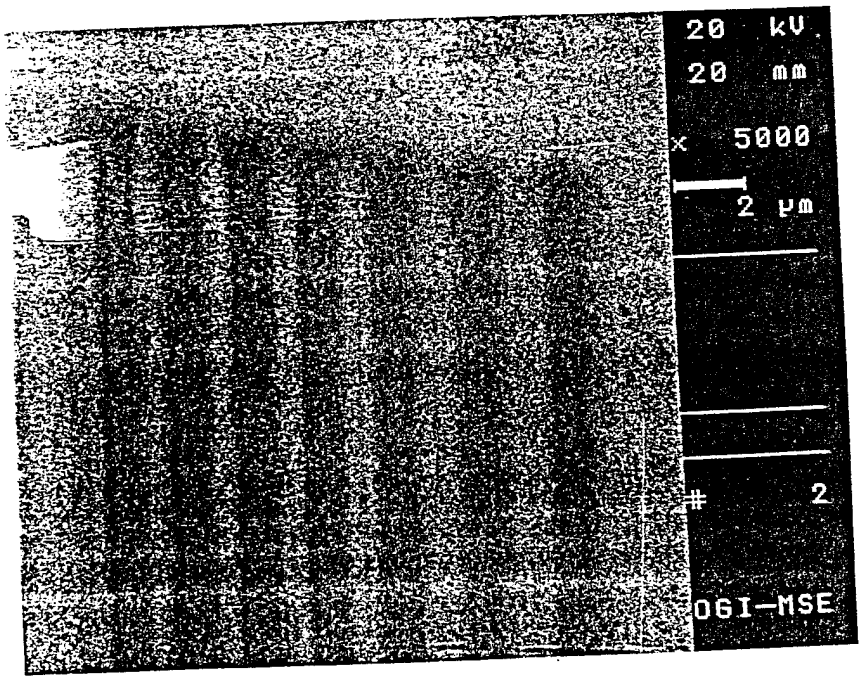


Fig. 4.4. SEM image of the features milled (a)without using enhanced etch and (b) using enhanced etch

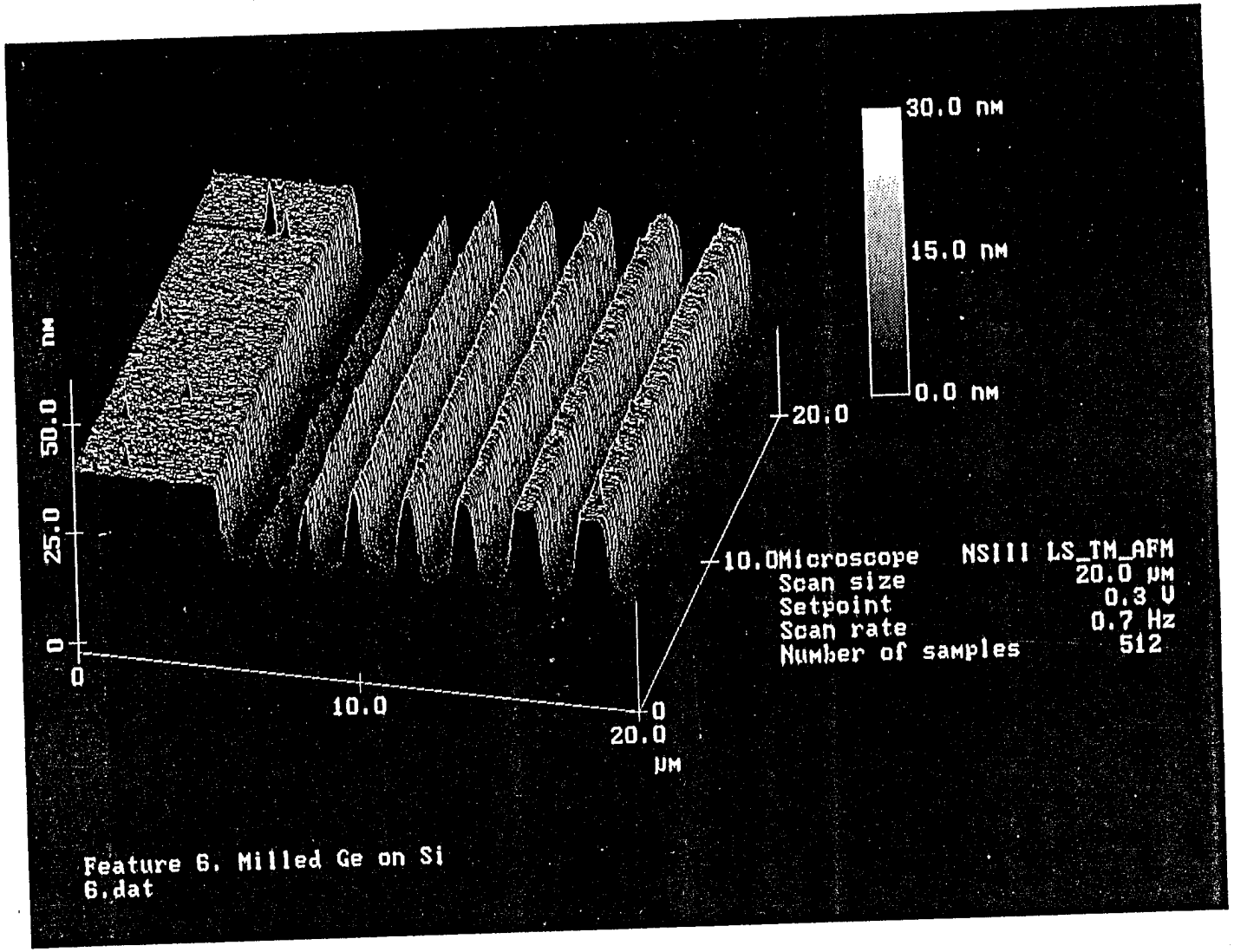


Fig. 4.5. 3-D AFM image of the feature milled using enhanced etch .

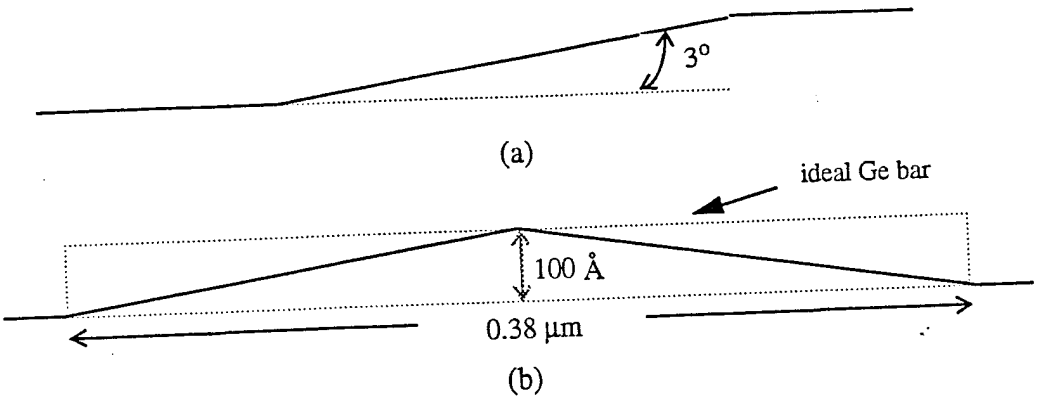


Fig. 4.6. (a) Schematics of the wedge shape. The slope of the wedge is about 3°. (b) The shape of the feature expected from FIB milling with the presence of iodine if a milling depth of 100 Å is required and the center of the feature is not milled. The dotted box shows the ideal Ge bar if no tail effect of the FIB is involved.

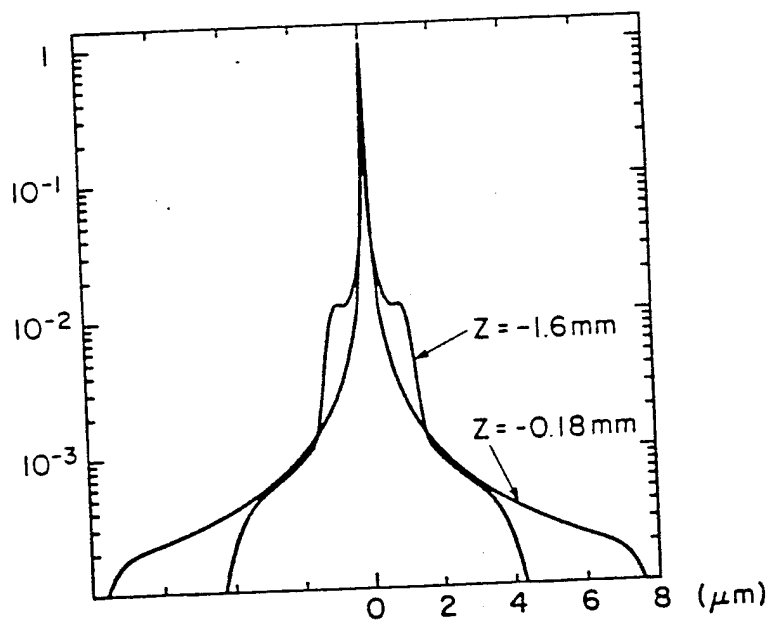


Fig. 4.7. The calculated current density distribution for a FIB system at two different states of focus, one minimizing the rise distance of the beam across a knife edge and one optimizing the spatial resolution [4.20-4.21].

the strip patterns is milled away, leaving wedges in the place. The shape of these wedges has been further studied using AFM. A 3-dimensional AFM image of the feature is shown in Fig. 4.5. The trenches in the image are strips of material removed by the FIB process. The slope of the edges of these trenches is measured to be ~ 3°, as shown in Fig. 4.6(a).

This results from the milling effect of the FIB tail. We show in Fig. 4.7 the calculation results of the current density of the FIB. The FIB tail is several orders of magnitude lower than that at the FWHM of the FIB [4.20-4.21]. Evidently, the milling efficiency of the FIB tail is enhanced more than that of the center of the beam with the presence of iodine. If a milling depth of 100 Å is required to remove a Ge thin film and a thickness of 100 Å is to be preserved at the center of the feature, FIB milling will only produce a pyramid of 100 Å high and 0.38 μm long at the bottom (Fig. 4.6(b)) instead of the rectangular bar (Ge wire) for the ideal case.

Contamination from the enhanced etch is observed as droplets randomly distributed in the milling area, indicated by the arrows in Fig. 4.8. Energy Dispersive X-ray (EDX) analysis shows a slight trace of iodine in the droplets. The droplets are not soluble in isopropyl alcohol.

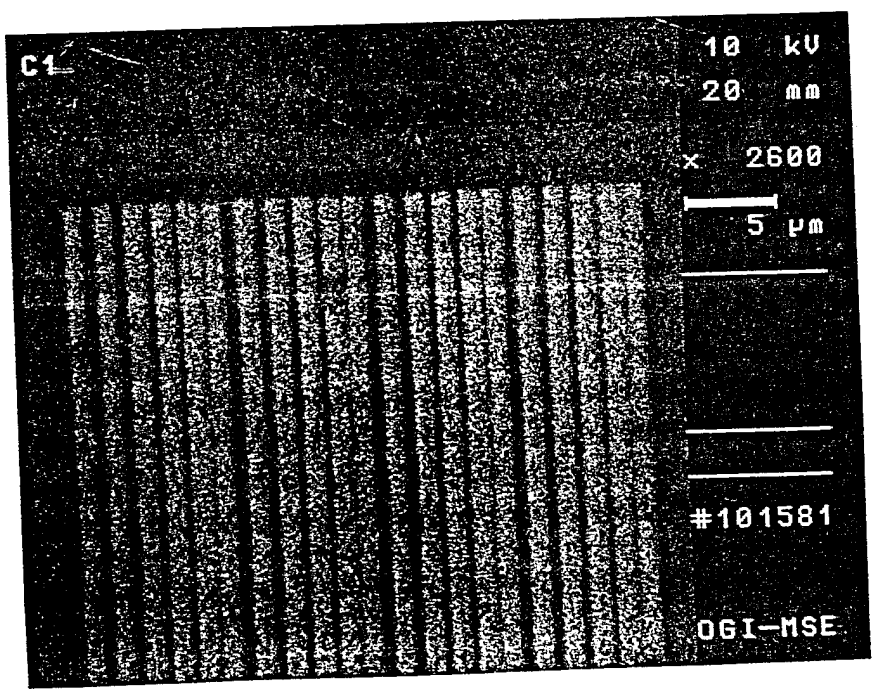
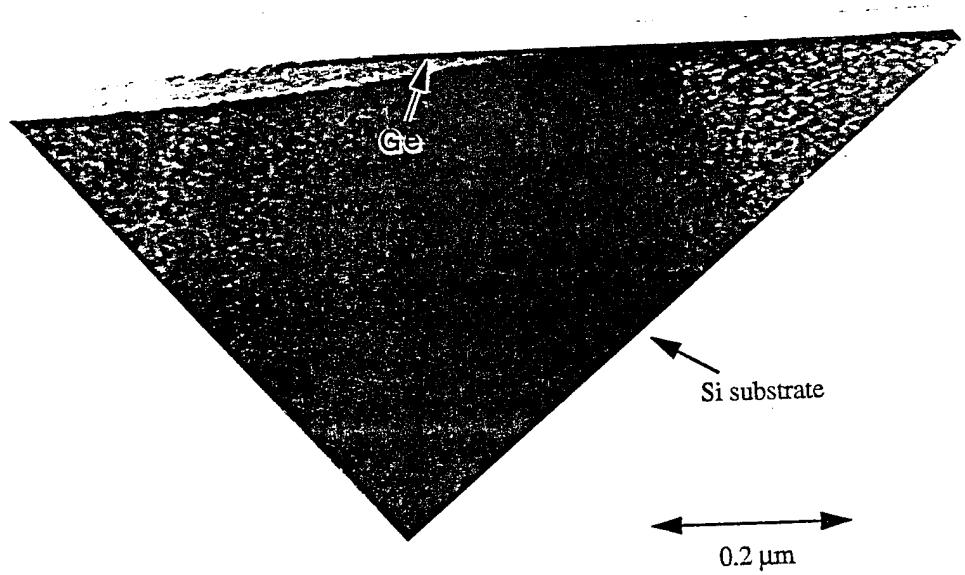


Fig. 4.8. SEM image of Ge wire array fabricated by FIB micromachining from a 50 Å Ge/Si sample using iodine as enhanced etch agent. The arrows point to the droplets randomly scattered over the milling area. EDX shows a slight amount of iodine in the droplet.

(a)



(b)

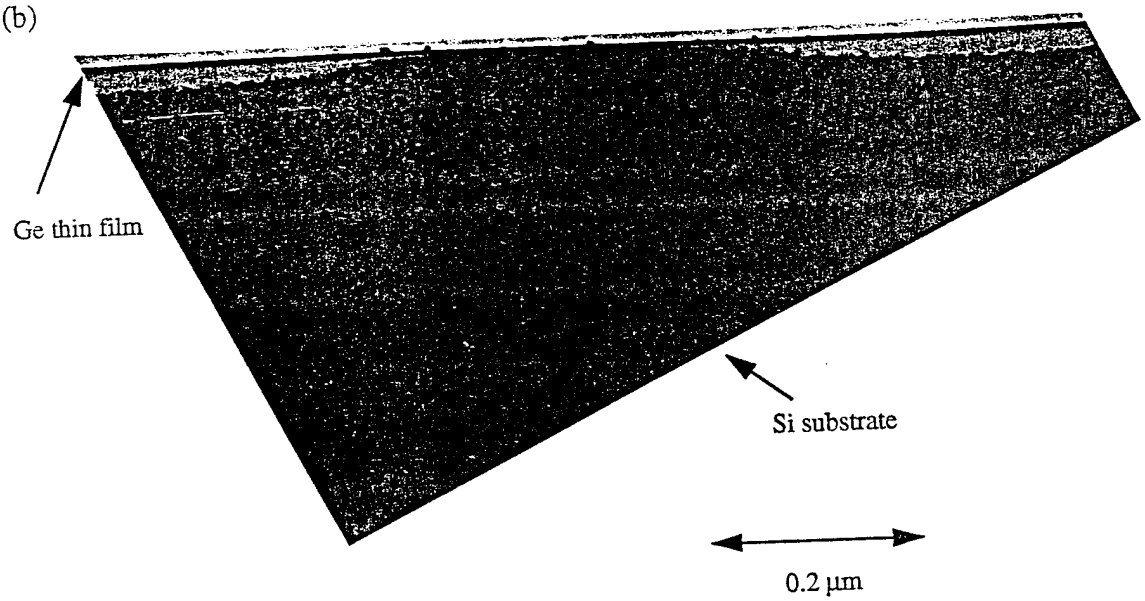


Fig. 4.9. XTEM image of (a) the wedge at one side of the Ge wire fabricated using a FIB dose of 1.8×10^{14} cm^{-2} and (b) a sample received a FIB dose of 1.12×10^{14} cm^{-2}. The Ge film thickness before FIB milling is 50 Å.

Cross-sectional transmission electron microscopy (XTEM) is used to help evaluate the quality of the Ge wires fabricated by FIB micromachining. The wedge shape of the edge of a Ge wire is shown in Fig. 4.9(a), from which we draw the following conclusions. Firstly, the image shows a ~ 300 Å thick Si layer beneath the Ge is amorphized in places where the Ge film is just completely removed. The height of the Ge layer above the amorphized Si is slightly higher than the Ge film which received no FIB milling. We believe this is a result of the effect of Ga ion implantation and resulting volume expansion occurred during Si amorphization. Secondly, the Ge film milled by the FIB is diffused, indicating the Ge atoms are "knock-on" displaced into the silicon substrate following collisions with the energetic Ga beam, even though some Ge atoms are removed by sputtering.

The threshold FIB dose for removal of 50 Å of Ge thin film is also investigated. In Fig. 4.9(a), the Ge film thickness is about 50 Å and the total FIB dose used is about 1.8×10^{14} cm^{-2}. The Ge film as well as a thin layer of Si is observed removed. Fig. 4.9(b) shows a sample for which a FIB dose of 1.12×10^{14} cm^{-2} is used. We see that the Ge film is not completely removed from the trench. Hence, the threshold dose for removal of 50 Å amorphous Ge lies between the two above mentioned values. Notice that in Fig. 4.9(b), significant amorphization of the Si substrate beneath the Ge film is induced before the Ge layer is completely removed.

4.4 Conclusions and Future Work

In conclusion, we have investigated the direct FIB micromachining technique to fabricate Ge nanowires. Without enhanced etch, significant redeposition of milled materials along the edge of the wires is observed even though the milling depth is extremely shallow (several hundred angstroms). Use of enhanced etch during the FIB milling avoids redeposition of the milled materials. However, several major problems still exist using enhanced etch FIB milling. First, milling effects resulting from the FIB tail produces

wedge shaped Ge wire edges, limiting the possible minimum width capability for the Ge wire. Secondly, introducing iodine for the enhanced etch process causes the formation of droplets of unknown composition randomly scattered over the milling area. Corrosion resulting from the remains of the iodine on the silicon substrate has been observed by other research groups [4.23]. Lastly, FIB milling modifies the composition of the target through intermixing effects resulting from the implantation of the Ga ions.

Future work should focus on resolving the above mentioned problems. As an example, a sacrificial layer (such as PMMA or SiO_2) with low FIB milling rates may be used on the Ge film to minimize the wedge effect. Chemical cleaning methods should be developed for removal of the contamination resulting from the enhanced etch agent.

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Chapter 5

GE NANOWIRE FABRICATION USING E-BEAM LITHOGRAPHY

5.1 Introduction

Electron beam (e-beam) lithography is the process of forming patterns by using a focused electron beam. Such beams can be readily scanned and accurately positioned on the substrate for exposing radiation-sensitive material (e-beam resist). Following early demonstrations of high-resolution patterning using focused electron beams [5.1-5.2], e-beam lithography has become a popular technique for delineating devices and structures on the scale of tens of nanometers [5.3-5.9].

E-beam lithography has several advantages over standard optical lithography. Firstly, it provides the ability to produce features without the use of a mask under direct control of a computer. Secondly, the equivalent wavelength of an electron beams is on the order of 0.2 to 0.5 Å. Therefore, diffraction effects, which limit resolution in optical lithography, are avoided. The resolution of e-beam lithography is limited by the so-called "proximity effect" which results when the electrons are forward scattered in the resist and back scattered from the substrate, resulting in exposure of the resist outside the desired areas. The proximity effect may be reduced by using thinner resists and higher energy electron beams to reduced forward scattering. However, the resist sensitivity drops as the primary beam energy increases. The contribution to the proximity effect from the back scattered electrons also increases with the atomic number of the substrate. As a result, the minimum line width obtainable on a Ge/Si substrate will be larger than that for a bare Si substrate for the same conditions.

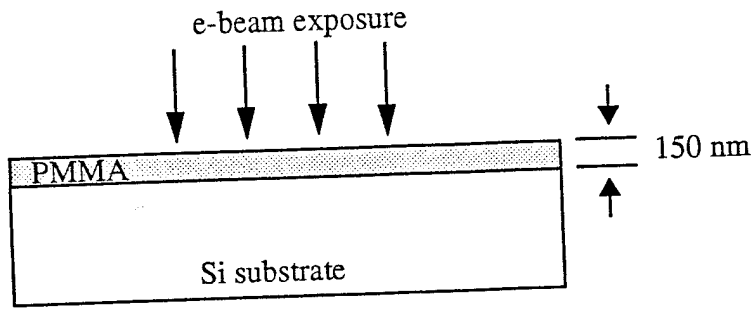
Critical to nanostructure patterning is the properties of the selected resist material

used for processing. Two types of electron resists are available: negative and positive electron resists. Negative electron resists have excellent sensitivity, but relatively low resolutions. This is due to exposed resist swelling during development for removal of unexposed resists. For this reason, positive electron resists are more frequently used for nanostructure patterning. Continuing efforts are underway in the research community to develop high sensitivity, high resolution electron resists with good adhesive and mechanical properties [5.10-5.12]. For our experiment, we select the most widely used positive e-beam resist: poly(methylmethacrylate), or PMMA in this work.

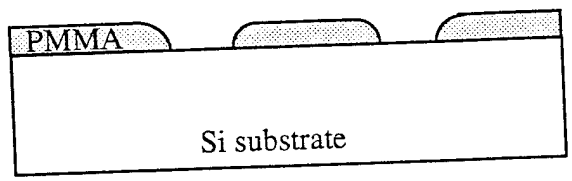
In this chapter, we describe the lift-off process used to fabricate Ge nanowires using e-beam lithography. Efforts to obtain the threshold e-beam dose for exposure of PMMA at a certain film thickness for nano-patterning are described. Field emission SEM, AFM, and cross-sectional TEM are used in the characterization of these nanowires. In order to prepare the TEM sample of the nanowires, an advanced technique using multiple protection layers and FIB marking and thinning is developed.

5.2 Experiment

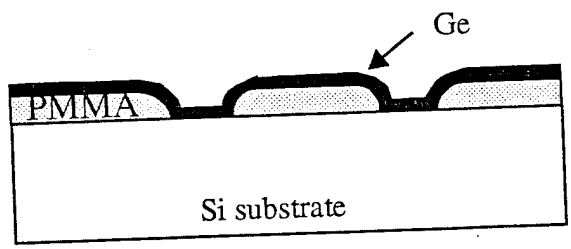
The process used in our experiment is illustrated in Fig. 5.1. Details of the experiment are as follows: first, an n-type (100) Si substrate is given a RCA clean followed by a 30 s 1:50 HF:H_2O dip. The sample is then spin coated with 1.5% PMMA dissolved in chlorobenzene. After being baked at 160°C for 8 hours, a thickness of about 150 nm of PMMA is obtained. The sample is then exposed in line patterns using a custom designed e-beam lithography system [5.13]. The scanned lines are located in an area of 47 x 80 μm^2. Various electron beam dosages, ranging from 0.9 to 1.4 nC/cm, are used for various sets of lines in the same pattern to determine beam dose effects on the quality of the Ge wires. The sets are separated by strip patterns for which the area scan is used. Next, the sample is developed for 80 s in a 1:3 MIBK:IPA solution at 25°C followed by a 15 s DI water rinse. Immediately prior to loading the sample into an electron beam evaporator, it



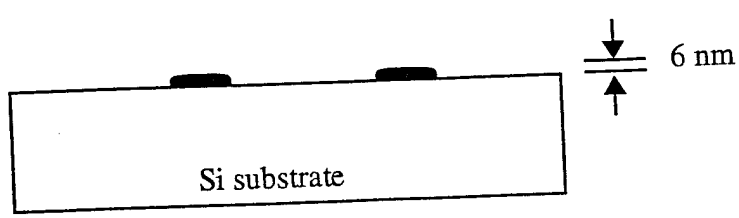
(a) A thin PMMA film is patterned by an electron beam.



(b) Exposed PMMA is developed in MIBK:IPA solution.



(c) A thin film of Ge is deposited using e-beam evaporation.



(d) Ge wires are formed after a lift-off process in acetone.

Fig. 5.1 Illustration of the lift-off process to fabricate Ge nanowires using e-beam lithography.

is exposed to HF vapor for 10 s to passivate the surface. A thin film of amorphous Ge, typically 50-100 Å, is then deposited at room temperature under a vacuum < 10^{-7} torr, similar to the process described in Chapter 4. The Ge wires are formed during the lift-off process in acetone.

5.3 Characterization and XTEM Sample Preparation

Since the Ge wires are extremely thin and narrow, field emission SEM is required in order to view the wires effectively. After examination using the field emission SEM and AFM, the sample is ready for cross-sectional TEM specimen preparation.

There are a number of methods for preparation of cross-sectional TEM specimens [5.14-5.16]. The conventional specimen preparation technique widely used consists of mechanical polishing, dimpling and ion milling. This method works very well with homogeneous, large samples. However, it is very difficult to apply to micron-scale structures. A common practice is the use of masks for selective ion beam milling. This method is cumbersome, and for micron-scale devices in a small area, does not ensure that the area of interest will be thinned to a uniform thickness for examination. In this work, the Ge wires are small and located in a specific area smaller than 100 μm on a side, It is physically very difficult to preselect this area in conventional specimen preparation techniques even using the above described masking technology. We therefore decided to use a FIB assisted milling technique for this process.

Cross-sectional TEM sample preparation using FIB assisted milling is a newly developed technology [5.17-5.26]. For purpose of convenience, different researchers use slightly different approaches. The general approach, shown in Fig. 5.2, is to cut the cross-section of the sample using a slow speed diamond saw as the first step, and make sure the area of interest is in this sample. Next the sample is mechanically polished to a thickness of up to 10 μm. The thinner the sample after polishing, the less time is required for FIB milling. However, a certain thickness is often required to ensure that the area of interest is

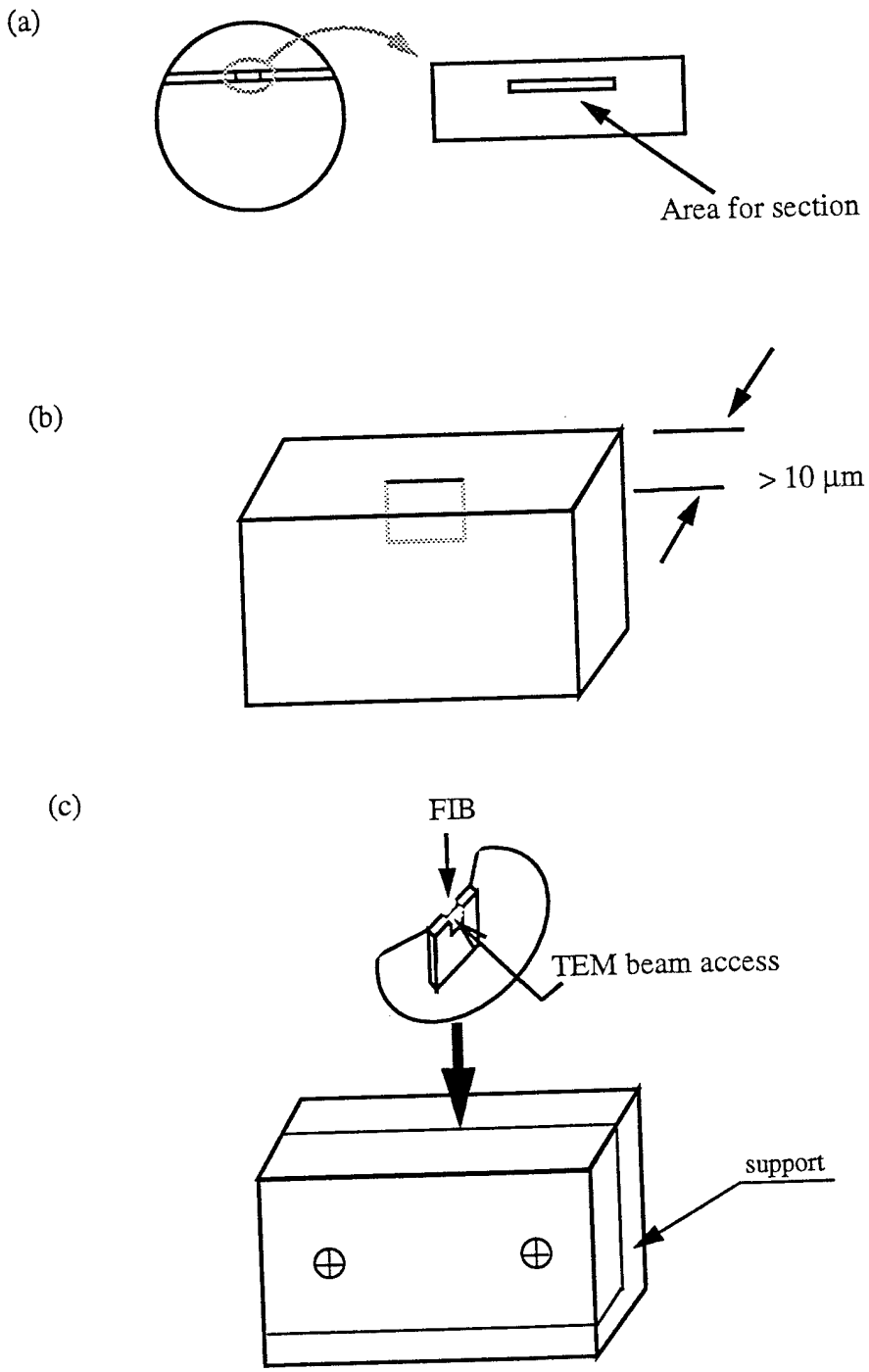
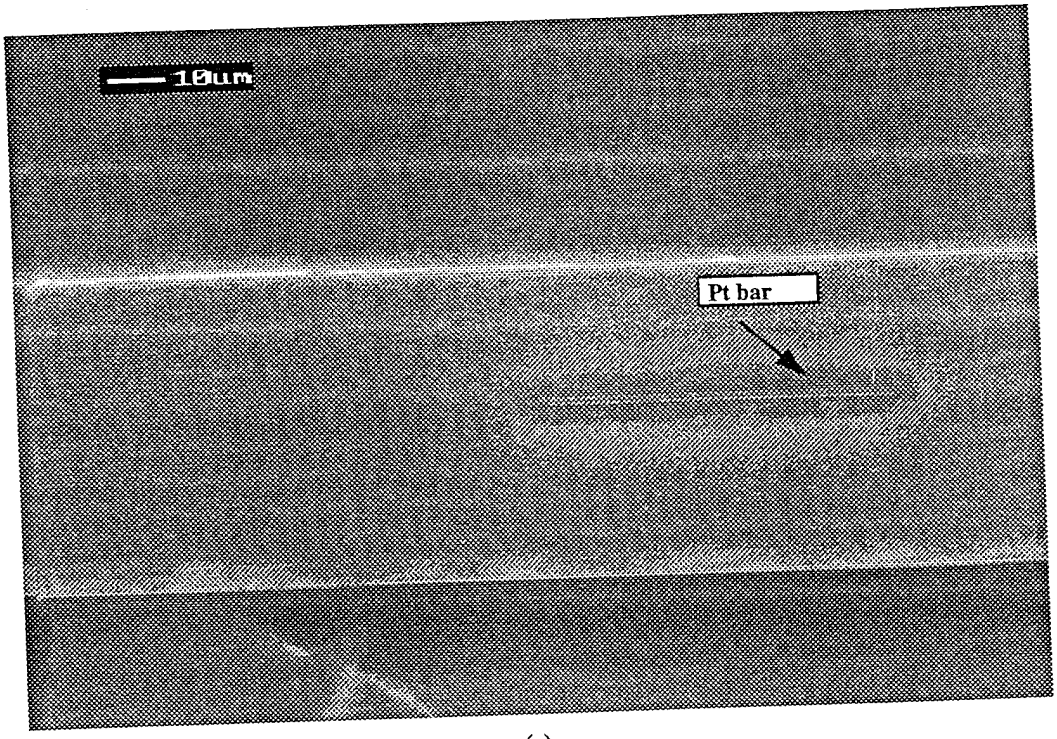


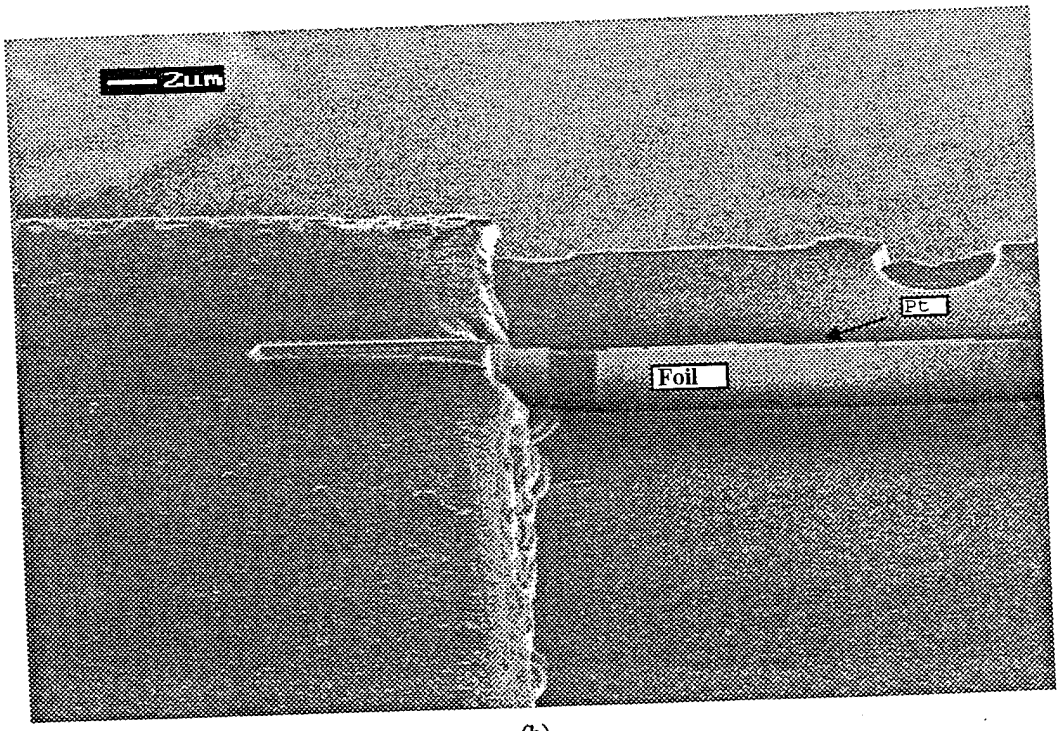
Fig. 5.2. Illustration of the cross-sectional TEM sample preparation process using FIB micromachining. (a) Mechanically saw a slice from the wafer containing the area of interest. (b) Mechanically polish this slice to > 10 mm. (c) Mount the slice on a modified TEM grid and mill two trenches, leaving a strip of materials which contains the feature of interest. The grid is then mounted to a support.

safe from damage. Once the desired thickness is reached, the sample is trimmed to a length that fits on the mount. Next, the sample is mounted to a modified grid which prevents the grid from blocking the ion beam during ion milling later in the process. If the sample is too long for the grid, the side(s) of the sample is trimmed away before mounting. The grid is then mounted on a support, which holds the sample straight. The support used in this work is a simple vise, as shown in Fig. 5.2(c). This vise can hold several samples at one time. After the sample is transported to the FIB station, two trenches are milled in it, leaving a narrow strip (or foil) of material surviving between them which forms the TEM section, within which the area of interest is contained. The milling is done with several different FIB currents, which gives different milling rates and beam sizes. To minimize the milling time, our milling starts at the largest available beam current, often as high as 13, 000 pA, depending on the condition of the ion source. The final milling is performed using a beam current of 16 pA, to obtain lattice resolution grade samples. Since the beam tail of the FIB may mill away features at the surface of the sample, FIB assisted *in situ* chemical vapor deposition (CVD) of a metal layer, such as the Pt shown in Fig. 5.3(a), is used in this work to serve as a protection layer. This is often performed on the area of interest before any milling [5.23]. Since a strong contrast exists between the Pt layer and the Si substrate for the focused ion microscopy image obtainable on the FIB machine, we use this layer of material as an indication wether the foil reaches the desired thickness. *In situ* observation, often in an area on the foil which does not contain the feature of interest, is performed from time to time using focused ion microscopy by tilting the sample in the FIB chamber when using the lowest beam current. A rule of thumb is that the foil is typically thin enough to obtain lattice imaging once the Pt is almost milled away at a beam current of 16 pA for a Pt layer thickness of 1 μm thickness when the milling was started. Fig. 5.3(b) shows a FIB made TEM sample with a small amount of remaining Pt on top of the foil between the two trenches.

Due to the small physical dimensions of the Ge wire array, a FIB marking tech-



(a)



(b)

Fig. 5.3. Scanning ion image of (a) the Pt bar deposited by FIB assisted CVD on the area of interest and (b) the foil made by milling two trenches and leaving a strip of materials in between. The Pt is visible in the image because of its distinguished contrast with the Si substrate. Traces of Pt on the top of the foil are used as an indication of the foil thickness in the milling process.

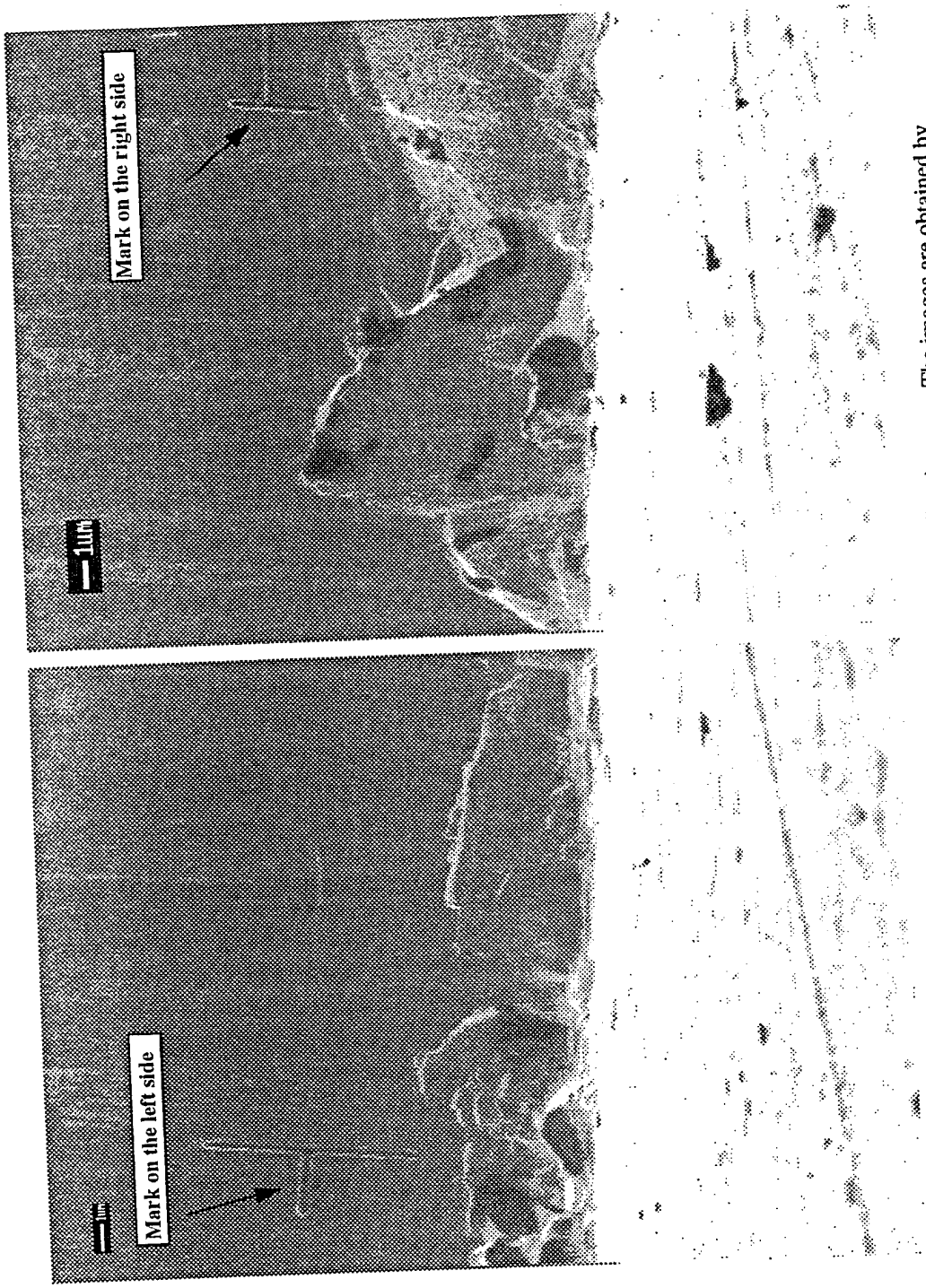


Fig. 5.4. Scanning ion image of the "T" marks made at the sides of Ge wire array. The images are obtained by scanning using FIB at the lowest current possible, e.g. 6 pA, to avoid modification of the sample surface.

nique [5.27-5.28] is used for location of the feature throughout the process. Immediately before the sample is subjected to XTEM sample preparation, it is transferred to the FIB workstation and two "T" shaped marks are made at the sides of the Ge wire array, as shown in Fig. 5.4. The lowest FIB current available, e.g. 6 pA, is used for locating the fea-

ture and care is used to avoid removing the Ge nanowires when using the FIB viewing scan.

The above process works well except that Ge or Si inter-diffuses into the Pt protection metal layer deposited by FIB assisted CVD. This problem becomes more serious due to localized heating from the ion beam when applied to an extremely thin foil of material(s). A diffusion barrier is needed in between the metal layer and the Ge/Si sample. Therefore, we developed a multilayer scheme to address this problem. As shown in Fig. 5.5, a thin carbon layer, about 100 Å thick, is thermally evaporated onto the sample, followed by a ~1200 Å layer of Au-Pd alloy, deposited using plasma sputtering. The final Pt

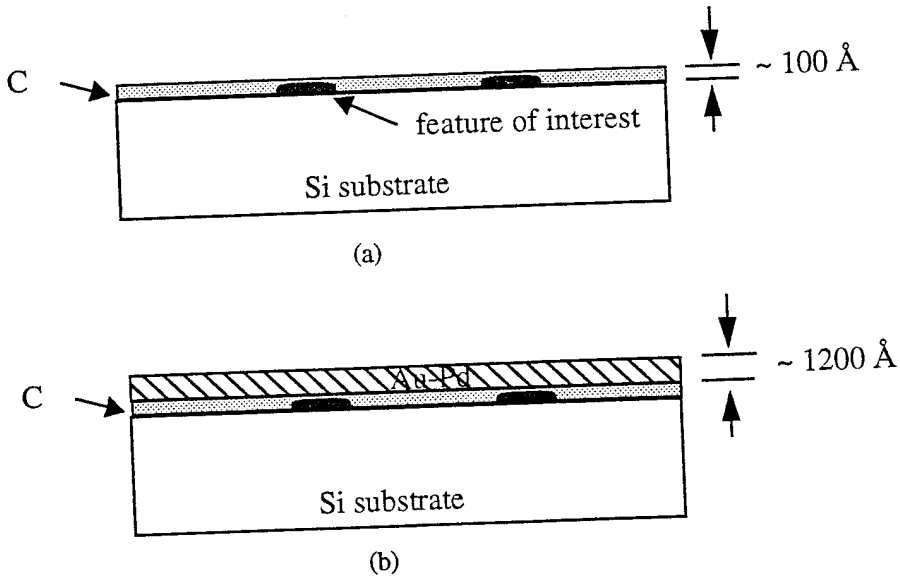
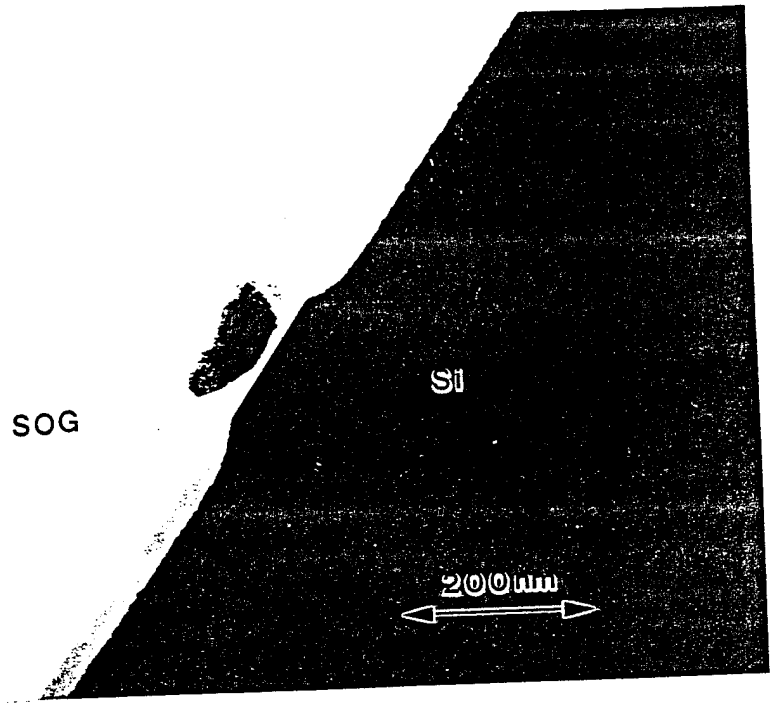


Fig. 5.5. Multilayer protection scheme to protect the surface of the substrate in the TEM, sample preparation process using FIB milling, particularly when the feature of interest is on the surface. (a) A thin layer of C(~ 100 Å thick) is thermally evaporated on the surface. (b) Au-Pd alloy (~ 1200 Å thick) is deposited using plasma sputtering.

layer is deposited on the top of this multilayer structure. The carbon layer serves as the diffusion barrier between the metal layer and the substrate. This layer cannot be replaced by SiO_2, which can be easily deposited by spin-on-glass. Fig. 5.6(a) shows a TEM sample prepared using spin-on-glass as the barrier layer. The surface of the Si substrate becomes amorphous in the foil, while the surface beneath a particle is protected and does not. We

(a)



(b)

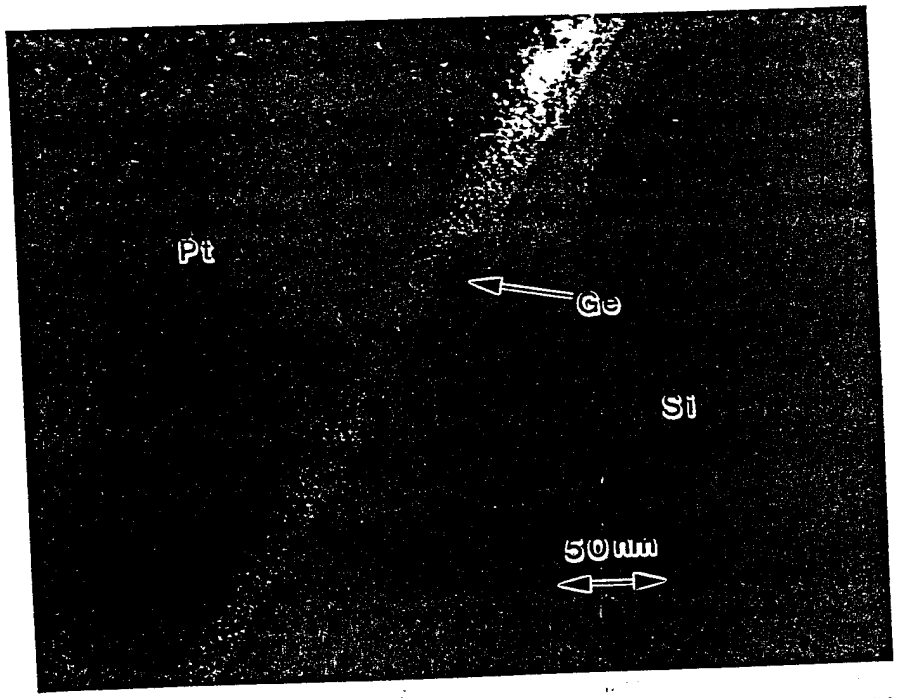


Fig. 5.6. Cross-sectional TEM image of a sample prepared using (a) spin-on-glass or (b)a thin film of carbon (~ 100 Å thick) as the diffusion barrier. The surface of the Si substrate of both samples becomes amorphous, indicating neither scheme is ideal to protect an area of interest at the surface. The surface of the Si substrate underneath a particle is protected in image (a).

believe this amorphous layer is formed by the inter-diffusion between SiO_2 and Si caused by localized heating from the ion beam because the SiO_2 has a low thermal conductivity.

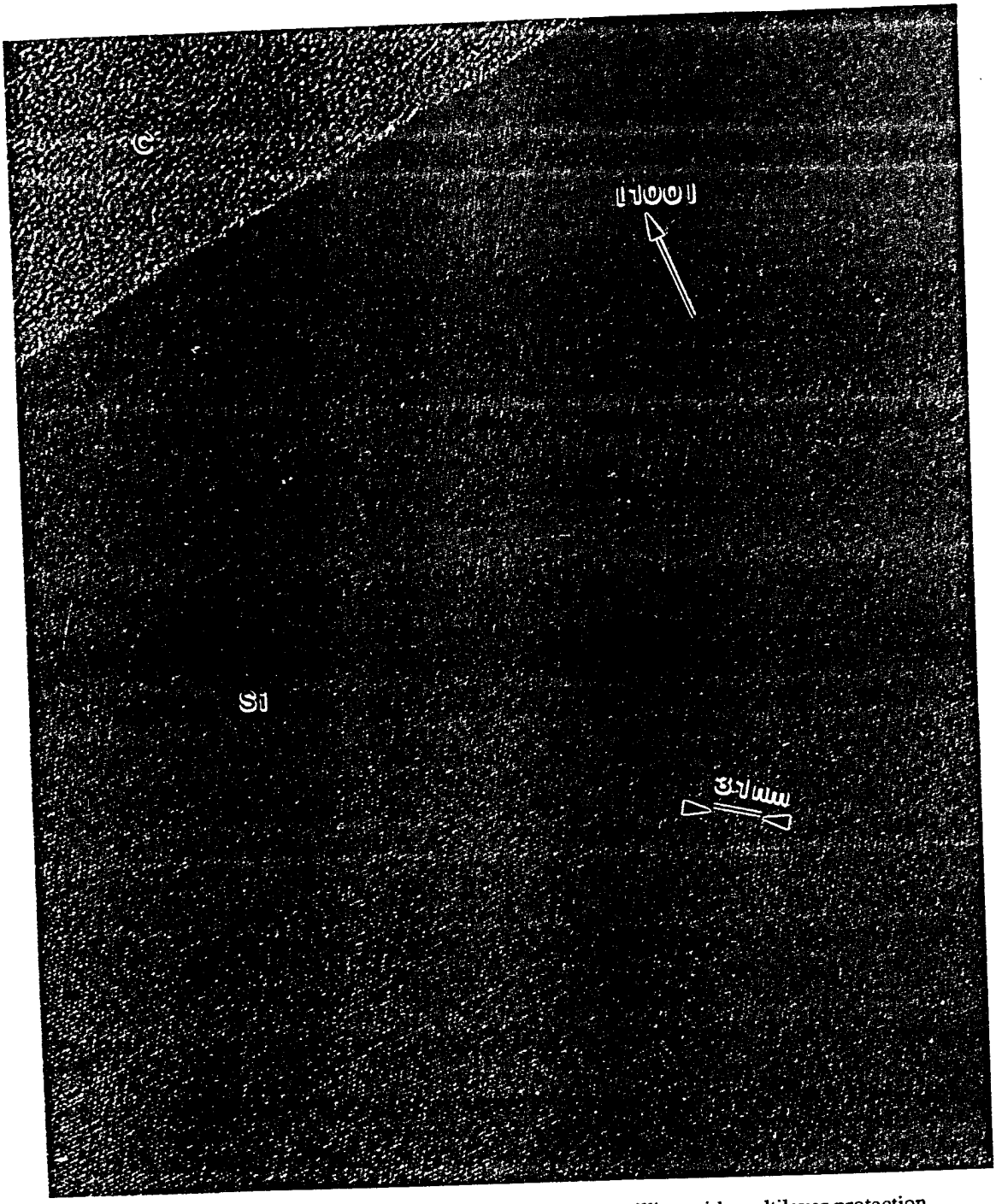


Fig. 5.7. Lattice image of a sample prepared using FIB milling with multilayer protection scheme. The foil made by this technique generally is believe to be wedge shaped, i.e. thinner at the top of the foil, thicker at the bottom. However, areas of lattice imaging quality in the foil can extend more than 1 μm from the top of the foil, as in the case for this sample. The image is taken along the [110] orientation.

The Au-Pd layer is necessary since the carbon layer is too thin to block the diffusion of Pt into the substrate, as shown in Fig. 5.6(b). The diffusion of Pt probably begins during its deposition by FIB assisted CVD since Pt atoms carry along the energy of the FIB. The thickness of the carbon layer is limited by the amount of carbon which can be thermally evaporated each run by our particular thermal evaporator. Note the FIB marks help to locate the area of interest after the Au-Pd deposition. A high quality XTEM sample is obtained in 5 to 6 hours using this multilayer scheme. Fig. 5.7. is a high resolution TEM image with lattice resolution obtained from a sample using the above process. It is believed that the foils made from FIB milling is wedge shaped, i.e. thinner at the top of the

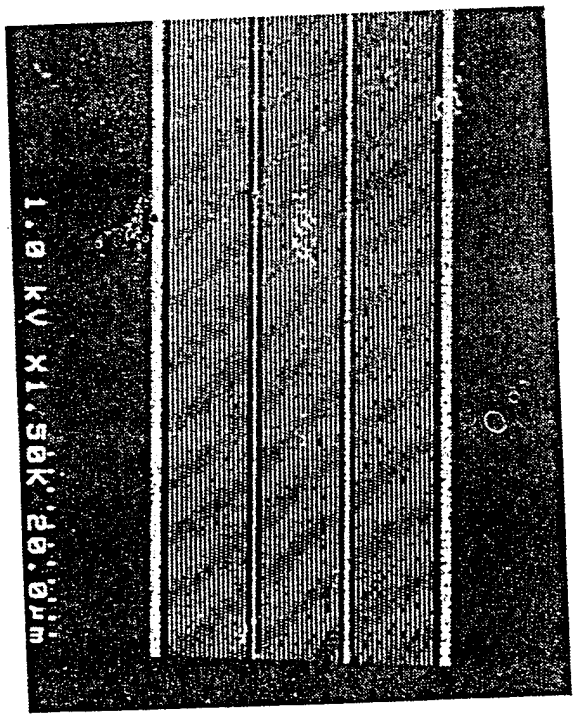


Fig. 5.8. Field Emission SEM image of three groups of Ge wires processed with e-beam dosages of 1.0, 0.95, 0.9 nC/cm from left to right respectively. The wires are not continuous when the e-beam dose used is blow 0.95 nC/cm.

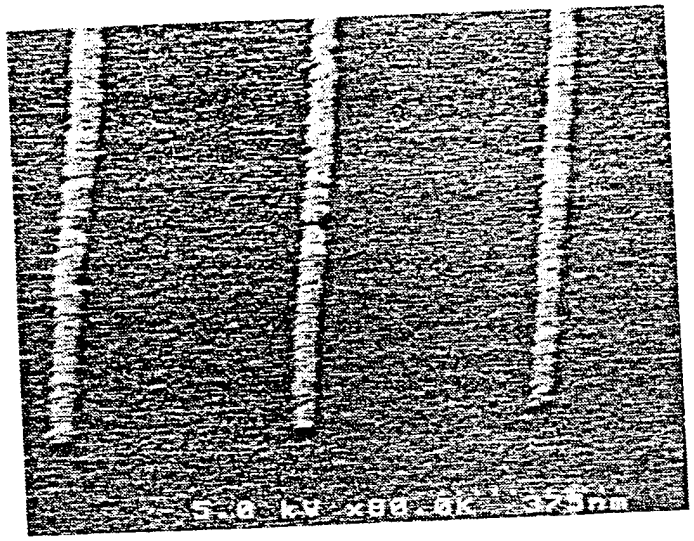


Fig. 5.9. High magnification field emission SEM image of Ge wires processed with e-beam dose of 1.0 nC/cm viewed at a tilt angle of 74°. The wires are seen to be fairly straight in the image.

foil and thicker at the bottom. However, with this particular sample, lattice resolution images are obtainable from the entire foil for more than 1 μm along its depth. In addition, all features of interest are preserved in the foil for observation. This process is universally applicable to any localized surface structures.

5.4 Results and Discussion

Figure 5.8 shows a field emission SEM image of three groups of fine Ge wire structures processed using e-beam doses of 1.0, 0.95, 0.9 nC/cm from left to right, respectively. The three groups of wires are separated by Ge wires with broad width. It is understandable that a low dose is preferred because the lower the dose, the less the beam broadening effect and therefore, the narrower the wires would be. However, as seen in the figure, for the lowest e-beam dose, the PMMA does not completely develop and the lift-

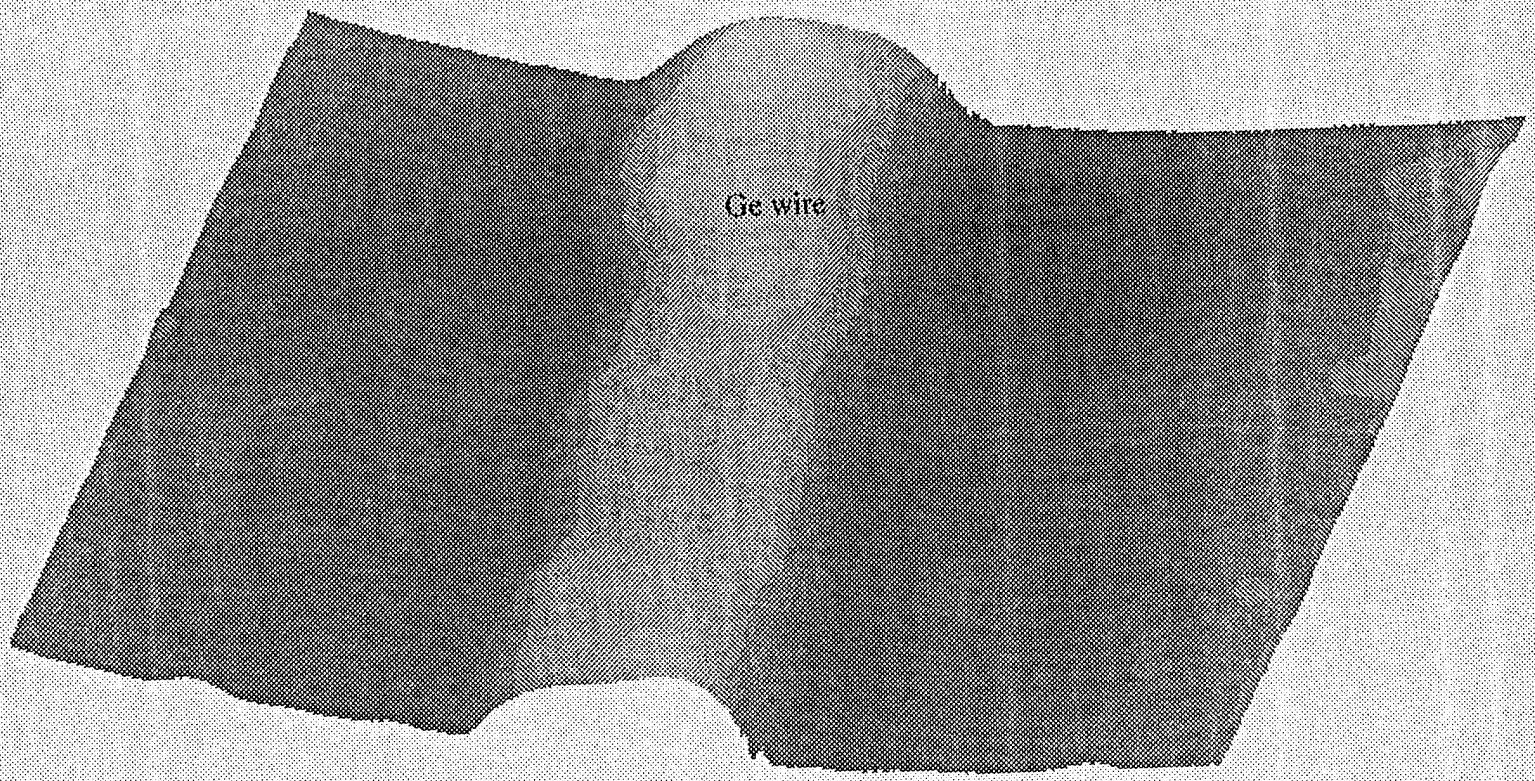


Fig. 5.10. Atomic force microscopy image of a Ge wire showing the topology of the Ge surface.

off process results in noncontinuous wires. The threshold dose required to maintain continuous wires is about 1.0 nC/cm. As shown in Fig. 5.9, the wires are seen to be fairly straight. The width of the fine wires in the most left group in Fig. 5.8 is measured to be 57 nm. These wires exhibit a certain degree of roughness which is typical in features defined by lift-off processes. The AFM image (Fig. 5.10) better depicts the topology of the wires.

The thickness of the wires is measured to be 6 nm from the cross-sectional TEM image (Fig. 5.11). The TEM image shows that the wire has knife edges. We believe this is formed by oxidation of both Ge and Si after the sample is exposed to the air. This is in agreement with the fact that the silicon surface beneath the Ge wire is slightly higher than the rest of the surface. The thin transparent layer (5 Å), believed to be oxide, is visible beneath the Ge wire in the image. There are several possible reasons for the formation of this layer: (i) the native oxide on the Si substrate is not completely removed before e-beam

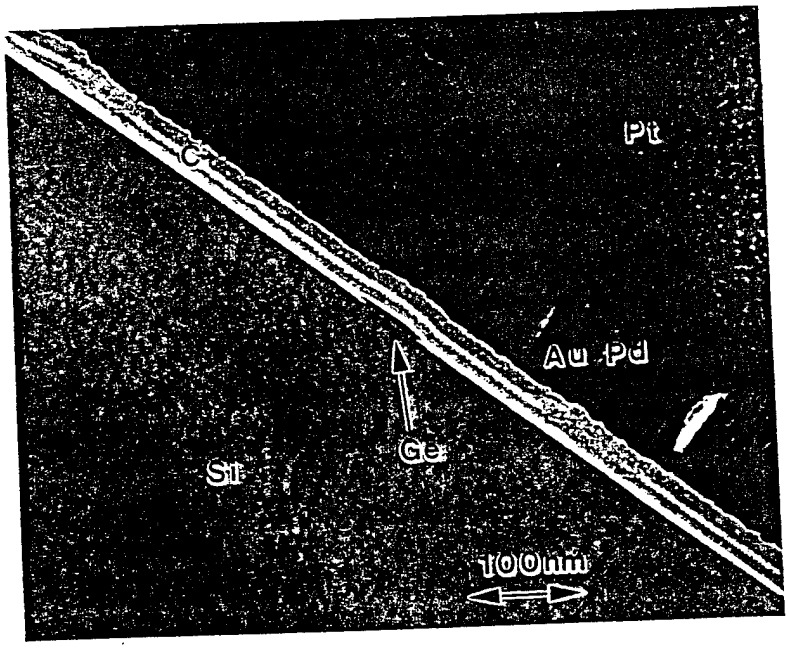


Fig. 5.11. Cross-sectional TEM image of a Ge wire on a Si substrate formed after a lift-off process using e-beam lithography.

evaporation or develops during the course of the e-beam evaporation; (ii) it is formed by oxidation during the FIB assisted specimen preparation. There is evidence showing the oxidation effect from the FIB milling. The 25 keV focused ions impinge on the side of the foil generating heat during the milling process. In some specimens prepared by FIB milling, the heating can produce an oxide layer of hundreds of nanometers in thickness on the surface of the Si. However, this oxide does not necessarily present a problem for the PLIE process because of its relative insensitivity to a very thin oxide layer [5.29], even if this thin layer is between the Ge wire and the Si substrate.

5.5 Conclusion

In conclusion, Ge wires with cross sections as small as 6 by 57 nm are fabricated on silicon substrates using a lift-off process combining e-beam lithography/evaporation. Line scanning is used for the e-beam exposure of the PMMA thin film. The e-beam dosage used for the line scans needs to be larger than 1.0 nC/cm for the formation of continuous wires. Lower e-beam dosage results in discontinuous wires. An advanced cross-sectional TEM specimen preparation procedure is developed to examine the wires. The procedure is applicable for any cross-sectional sample preparation using FIB micromachining for localized surface structures.

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Chapter 6

FABRICATION OF SiGe NANOWIRES USING PULSED LASER INDUCED EPITAXY

6.1 Introduction

In this chapter, we address the primary goal of this work to demonstrate direct formation of SiGe nanowires in Si using the pulsed laser induced epitaxy process. In the previous chapter, we described the successful development of a process to obtain Ge nanowires on a Si substrate and the corresponding characterization techniques. Specifically, Ge nanowires as narrow as 57 nm are demonstrated using a lift-off process with e-beam lithography. The thickness of Ge wires is readily controlled by e-beam evaporation, which has an accuracy of $\pm$ 5 Å [6.1]. This provides the ability for obtaining ultra-narrow SiGe wires by directly incorporating the Ge into the Si substrate with the PLIE process. Our advanced TEM specimen preparation procedure, described in Chapter 5, allows high resolution cross-sectional transmission electron microscopy analysis of the SiGe nanowires with a high sample preparation yield.

One concern we have neglected to date is the side diffusion effect occurring in the PLIE process as configured in our experiments. In the PLIE process, both Ge and the Si substrate are melted. The energetic laser pulse causes a rapid melt and regrowth process in the new surface region of the samples. The laser energy is absorbed very close to the surface as the absorption depth in Si for the 308 nm laser beam is about 7 nm and roughly 10 nm in Ge [6.2, 6.3]. Recrystallization occurs from the single-crystalline substrate. During the rapid melt process, the Si and Ge intermix to form localized alloy regions. When masks are used in the process, such as discussed in reference 6.1, where 3-μm wide, 200 nm deep SiGe wells are formed (Fig. 6.1), the Si substrate beneath the mask is not melted

limiting Ge diffusion to the un-masked area. In our work, areas other than those beneath the Ge nanowires described in the previous chapter are also subject to laser irradiation, and thus melt, as shown in Fig. 6.2, resulting in the possibility of side diffusion. This should not be significant, since the melt duration is on the order of tens of nanoseconds. However, the side diffusion may be enhanced by the fact that Ge is melted first since the melting starts from the surface of the sample and the Ge has a lower melting temperature than Si.

With this in mind, we pursue fabrication of the SiGe nanowires by two methods: In the first method we apply the laser beam directly onto the Ge nanowires/Si sample. This is a straight forward and simple process without additional steps. In the second method, we

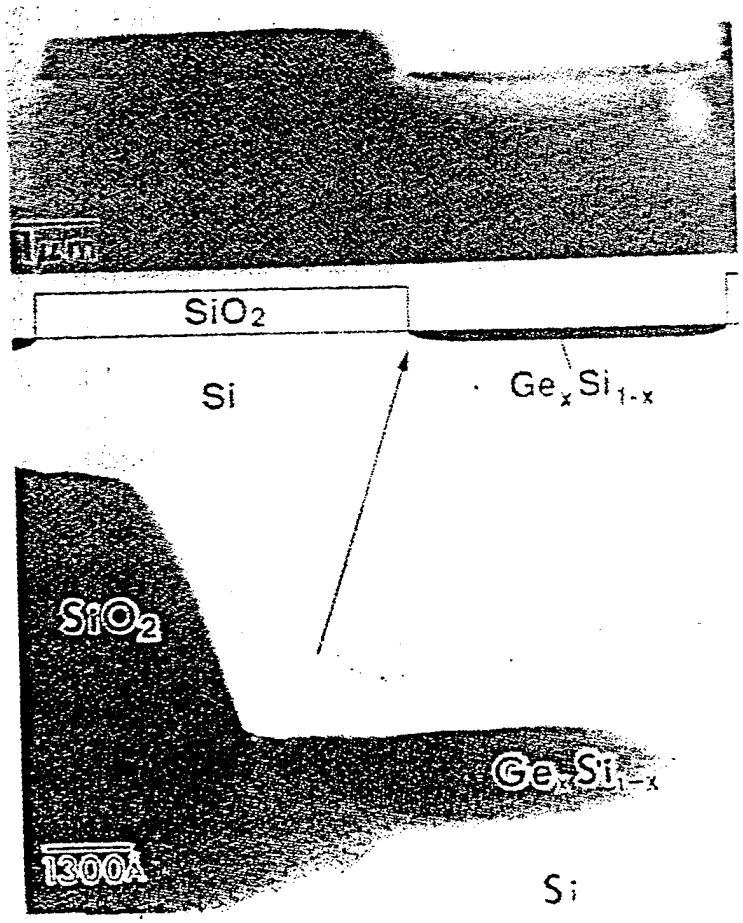


Fig. 6.1. Cross-sectional TEM image of SiGe wells formed in a PLIE process using an Al/SiO2 mask. No side diffusion is observed since the substrate area beneath the mask is not melted in the PLIE process. (Ref. 6.1)

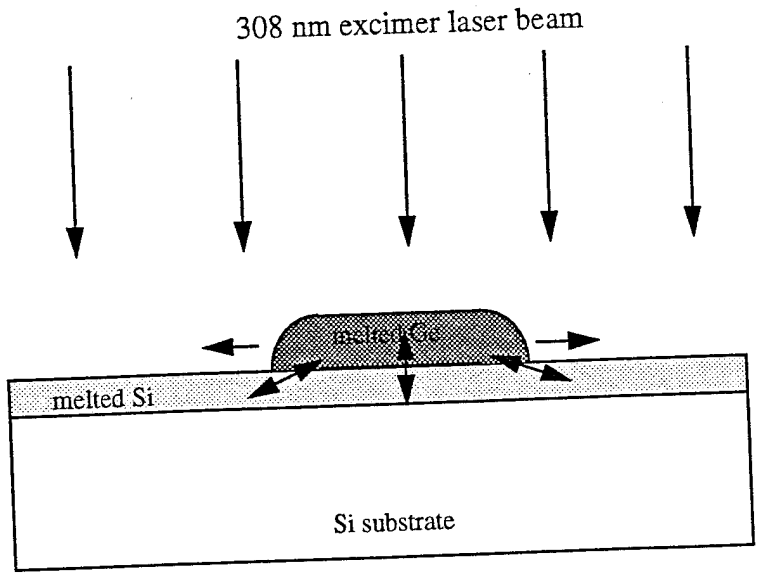


Fig. 6.2. Illustration of a possible melting and diffusion process in a PLIE process by directly applying the laser beam on the Ge nanowire on Si.

deposit a thin LTO capping layer on top of the Ge nanowires/Si sample. The thin LTO layer is essentially transparent to the 308 nm XeCl laser beam and does not hinder the melting process. However, the LTO layer is expected to prevent the Ge nanowires from ablation/evaporation when they are melted.

In the remainder of this chapter we present the details of our efforts to fabricate SiGe nanowires in Si. Section 5.2 describes the method without using the LTO capping layer. Interesting surface evolution observed after the PLIE process other than lateral diffusion is discussed based on the results obtained using SEM, Nomarski microscopy, cross-sectional TEM, atomic force microscopy, and Auger electron spectroscopy. Section 5.3 describes results obtained when using the LTO capping layer and are compared with those obtained from the first method. The final section summarizes our results.

6.2 Formation of SiGe Wires Without LTO Capping Layer

Details of this experiment are as follows: n-type (100) Si substrates are patterned

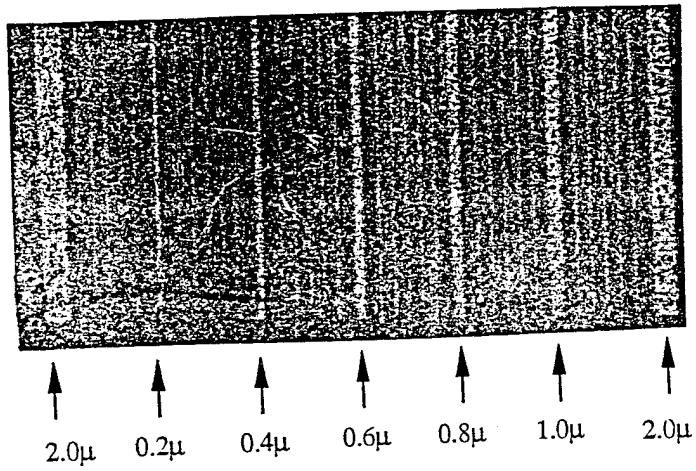


Fig. 6.3. Scanning electron micrograph of a Ge wire array on Si before laser irradiation.

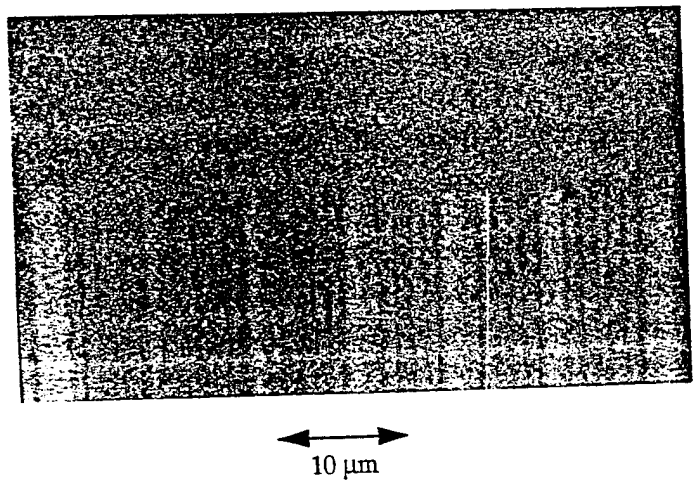


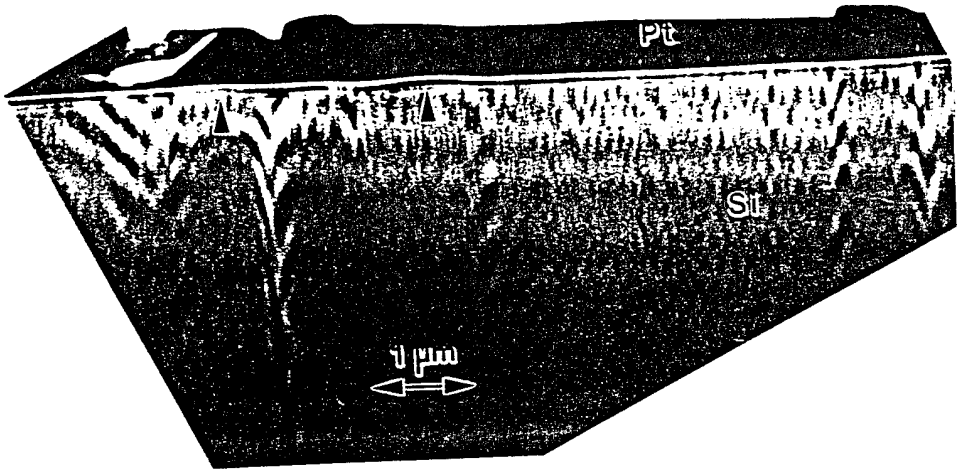
Fig. 6.4. Scanning electron micrograph of the Ge wire array shown in fig.6.3 after laser irradiation.

with Ge wire arrays using the lift-off process and e-beam lithography described in the previous chapter. The Ge wires are ~ 60 nm in width and ~ 6 nm in thickness with spacings of either 0.5 μm or 1 μm for different samples. As shown earlier in the SEM image (Fig. 1a), the six arrays of wires are divided by broader Ge wires of widths of 0.2 μm, 0.6 μm, 0.8 μm, 1 μm and 2 μm. Lower e-beam dosages are used for these broader lines resulting in a partial lift-off of Ge films in these wires, as seen in the image. The PLIE process is carried out in the gas cell through a quartz window. Immediately prior to placing the samples into the gas cell, the samples are rinsed in DI water for 20 s followed by 15 s HF vapor exposure to passivate the surface. The gas cell is pumped out to a pressure of less than 1×10^{-7} Torr and then backfilled with Ar gas to ~ 500 Torr. The samples are then irradiated through the quartz window using the spatially homogenized 308 nm XeCl excimer laser beam at an energy fluence of ~ 0.82 J/cm^2. The duration of the laser pulse is 27 ns. The homogenized beam is a square of 3 mm on a side. The applied laser beam covers the entire wire pattern as well as some of the surrounding area. The melting and resolidification process is monitored using a HeNe laser beam, which is used *in situ* to probe the sample surface exposed to the laser beam to record reflectance changes during the process. The surface melt duration at this energy fluence for the bare Si surface is found from the reflectance data to be ~ 40 ns.

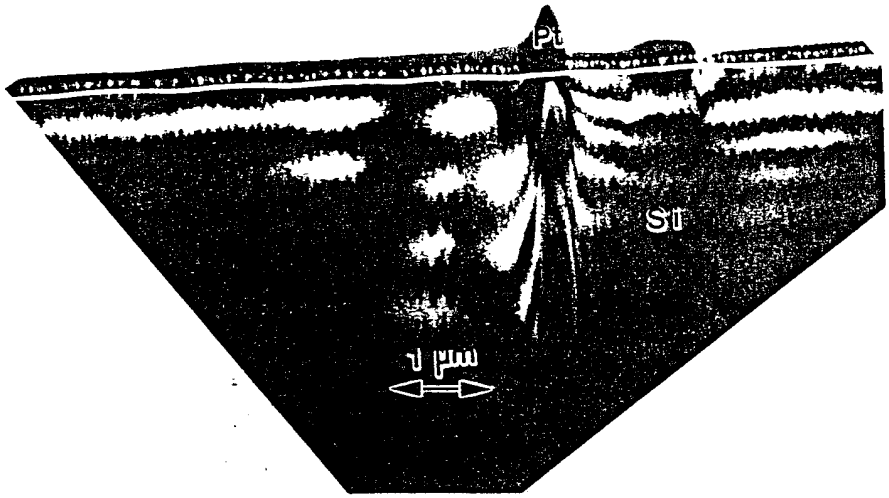
- **Characterization and Discussion**

Fig. 6.4 shows an SEM image of the same sample shown in Fig. 6.3 following application of a single laser pulse. Ripples are formed on the surface in regions where the Ge wire arrays are located. From this image, the original Ge wire locations are viewed as plateaus above the surface. This seems to conform with the fact that the original Ge wires are sitting on the surface of the substrate and their original shape is partially preserved after intermixing with the Si. However, cross-sectional TEM analysis reveals that this is *not* the case.

In fig. 6.5(a) we show a TEM micrograph which illustrates the topology of the sur-



(a)



(b)

Fig. 6.5. Cross-sectional TEM image following one laser irradiation of (a) Ge wires/Si with 0.5 μm spacing (b) Ge wires/Si with 1.0 μm spacing.

face of a sample with a spacing of 0.5 μm between the wires. The two large ripples seen in the image result from the original 1-μm wide Ge wire. To the left of these two large ripples can be seen several small ripples from the 60 nm wide Ge wire array. Apparently, the original Ge wire locations have become troughs rather than plateau after laser irradiation. The height of the ripples formed by the 60-nm wide Ge wires with 1 μm spacing (Fig. 6.5(b)), as measured from TEM, is about 22 nm, much higher than the original height (6 nm) of the Ge wires deposited on the Si surface. The topology of samples irradiated with different numbers of laser shots are also examined by AFM. As can be seen in Fig. 6.6, the ripple height decreases with increasing number of laser shots. Fig. 6.7 is a Nomarski inter-

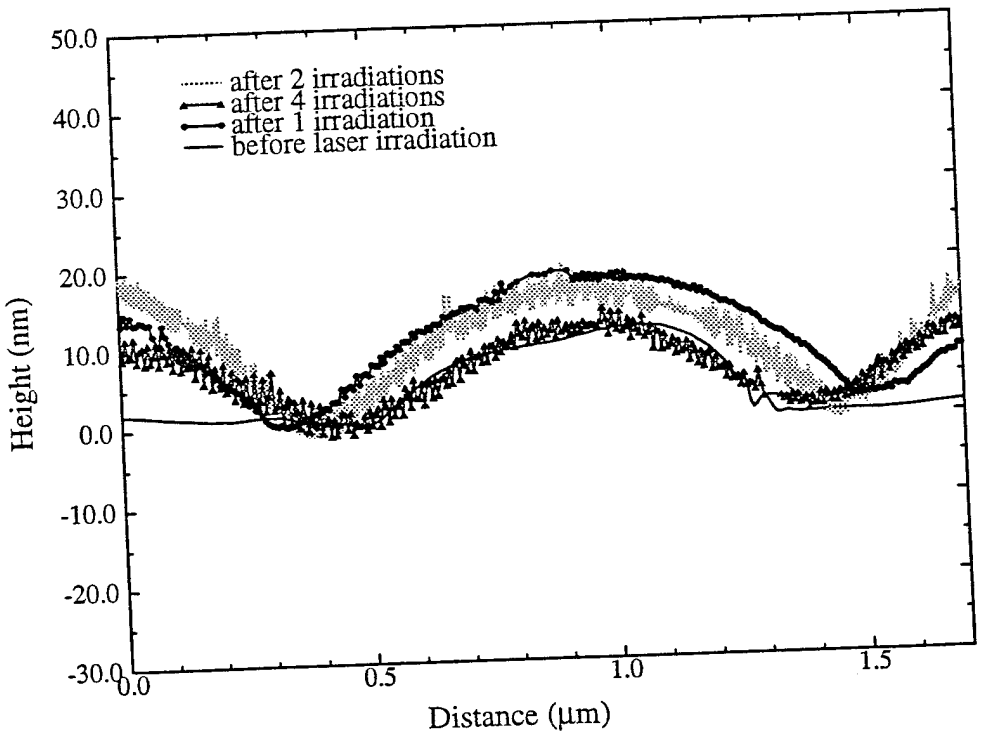
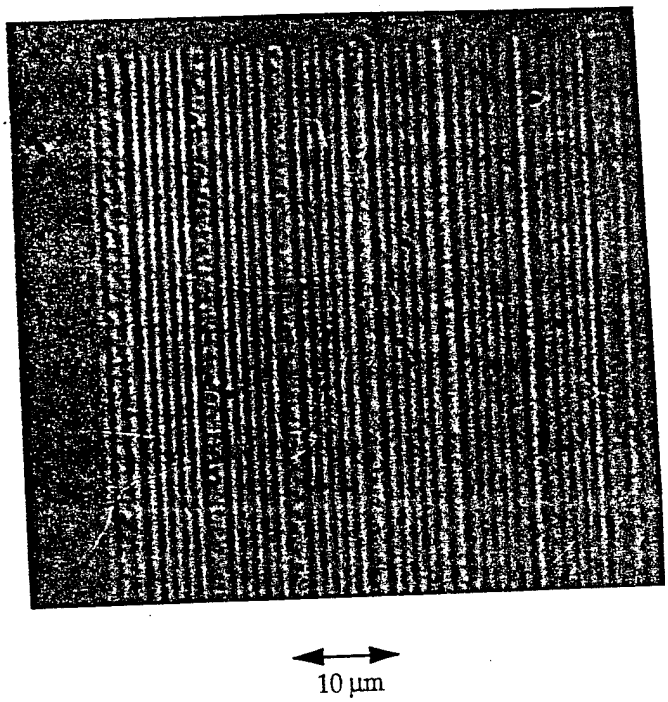


Fig. 6.6. Atomic force microscopy on a wire sample having 1-μm spacing showing decreasing ripple heights with increasing number of laser irradiation.



Fig, 6.7. Nomarski micrograph for a wire sample after laser irradiation. Trenches can be seen surrounded by ripples.

ference image which shows more detail of the ripple features formed on the surface. The troughs formed by the Ge wires surrounded by ripples are obvious. The roughness on the surface of the broader wires results from the partial absence of the Ge film. For the 60-nm wide Ge wire array, quasi-sinuous ripples are formed. However, for the broader Ge wires, the original Ge film height is still partially preserved. This can be seen in the surface topology formed by the 1-μm wide wire in Fig. 6.5(a). The SEM image in Fig. 6.3 has probably picked up more composition related contrast than topology contrast.

The reason for ripple formation is not fully understood at this time. One possible explanation follows. As illustrated in Fig. 6.8, during the 40 ns melt time of the PLIE process, Ge and Si inter-diffuse forming SiGe alloy. At the same time, particularly at the beginning of the melting process the Ge wires move downward because of mass and gravitational effects interacting with the Si surface resulting in the formation of the ripples

along the sides of the wires. This is similar to the case of ripple formation on a water surface when a drop of ink is put in. However, in the PLIE process, ripples are frozen in rather than disappearing as they are formed. the force of gravity, aided by the Brownian motion of the atoms, also aids the diffusion of Ge into the Si to form a compositionally uniform alloy of SiGe, as shown in Fig. 2.5. A factor which counteracts the ripple formation process is surface tension of the liquid Si. This results in the ripples formed from the 1-μm spacing 60-nm wide Ge wire array in Fig. 6.5(b) being larger than those formed in the 0.5-μm spacing 60-nm Ge wire array of Fig. 6.5(a). Similar surface evolution is observed for the PLIE process in fabricating SiGe nanowires when using a thin LTO capping layer on top of Ge wires/Si structures. We discuss this topic further in the next sec-

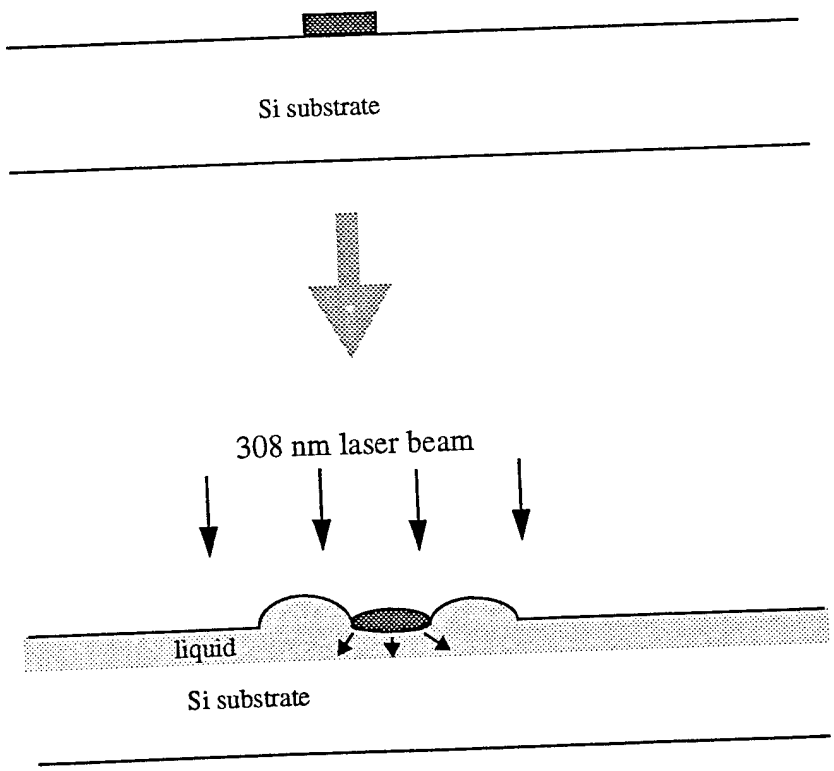


Fig. 6.8. Illustration of the ripple formation process

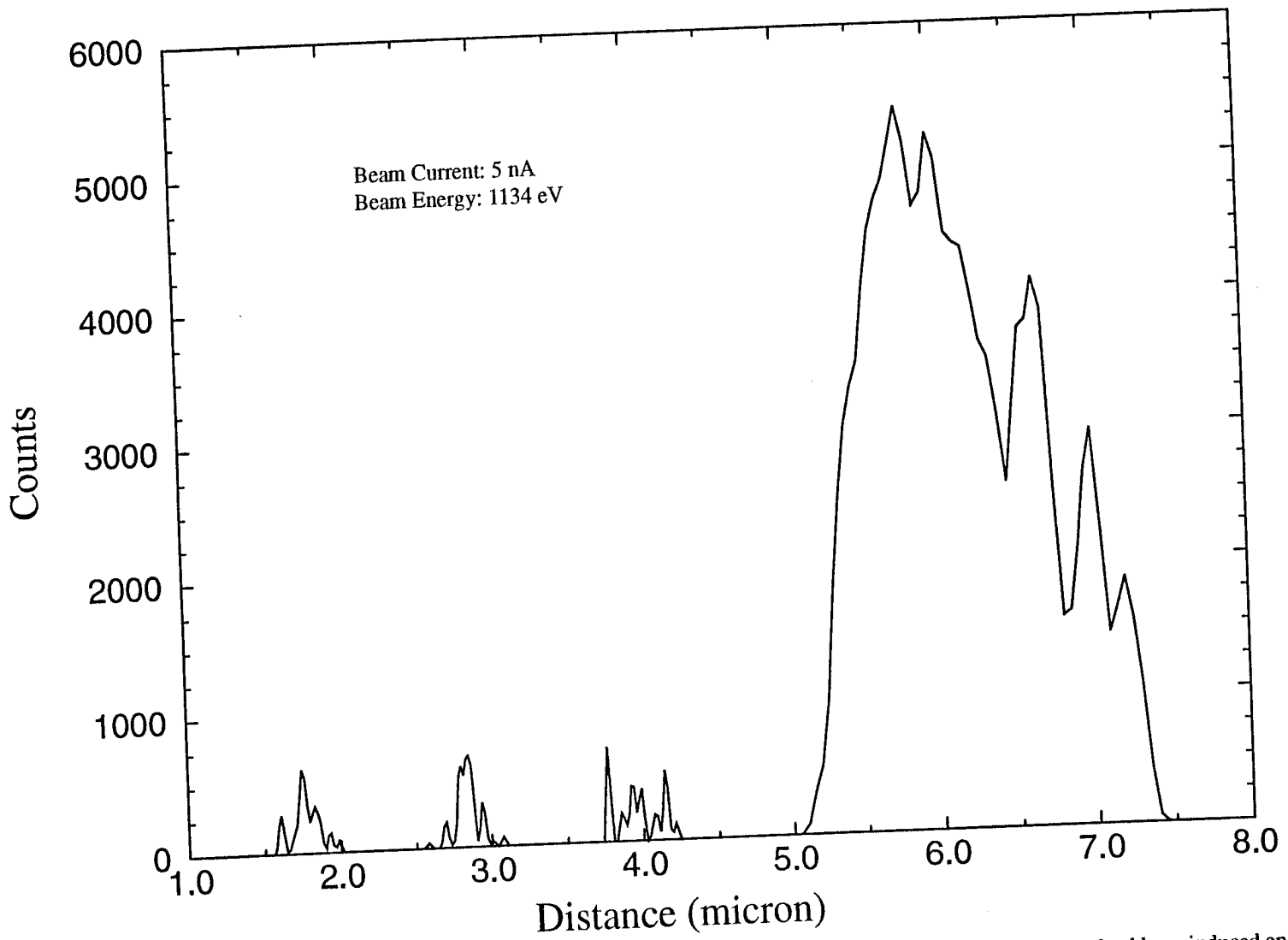


Fig. 6.9. Auger electron spectrum of SiGe wires formed by directly applying the laser beam on Ge nanowires/Si in a pulsed laser induced epitaxy.

tion.

Since the SiGe/Si mass contrast is not observed in the TEM image, we can not determine the boundary of the Ge diffusion. We use Auger Electron Spectroscopy (AES) to determine the lateral diffusion of the Ge. In order to retain reasonable resolution without losing intensity of Auger electrons, a beam current of 5 nA is used in the experiment. The beam energy used is chosen to be 1134 eV. Figure 6.9 shows Ge LMM Auger electron signals from three SiGe wires formed from 57-nm wide Ge wires and one formed from a 2-μm wide Ge wire. It is seen that all wires broaden in width. The intensity of the Auger signal is much lower for the three smaller wires than that for the 2-μm one, an indication of lower Ge concentration in the small wires. All three smaller SiGe wires consistently have a full width half maximum (FWHM) of about 300 nm. This indicates that significant lateral diffusion of Ge is induced in the 40-ns PLIE process. In the next section, we demonstrate how this lateral diffusion may be tremendously reduced simply by using a thin LTO capping layer on top of Ge nanowires/Si structure during the PLIE process.

6.3 Formation of SiGe Wires Using an LTO Capping Layer

In these experiments, experimental procedures similar to those described in section 6.2 are used with the exception of an additional LTO capping layer deposition step immediately before the PLIE process. A Ge nanowire samples is first degreased in hot TCE, acetone and methanol for 5 min each, followed by DI water rinse for 3 min. The sample is then dipped in a 2% HF:H_2O solution for 15 s. After the sample is rinsed in DI water and dried in nitrogen, it is loaded into an LPCVD furnace for LTO deposition. The LTO is deposited to a target thickness of ~ 12 nm at a sample temperature of ~ 300°C at a pressure of 225 torr. The sample is then transferred to the PLIE system. The PLIE process is carried out in air. The HeNe monitor laser beam is used in an area free of Ge wires for *in-situ* monitoring of the Si melt time. Figure 6.10 shows an example of the melt pulse and the laser pulse obtained for this experiment. The FWHM of the melt pulse is ~ 26 ns. This

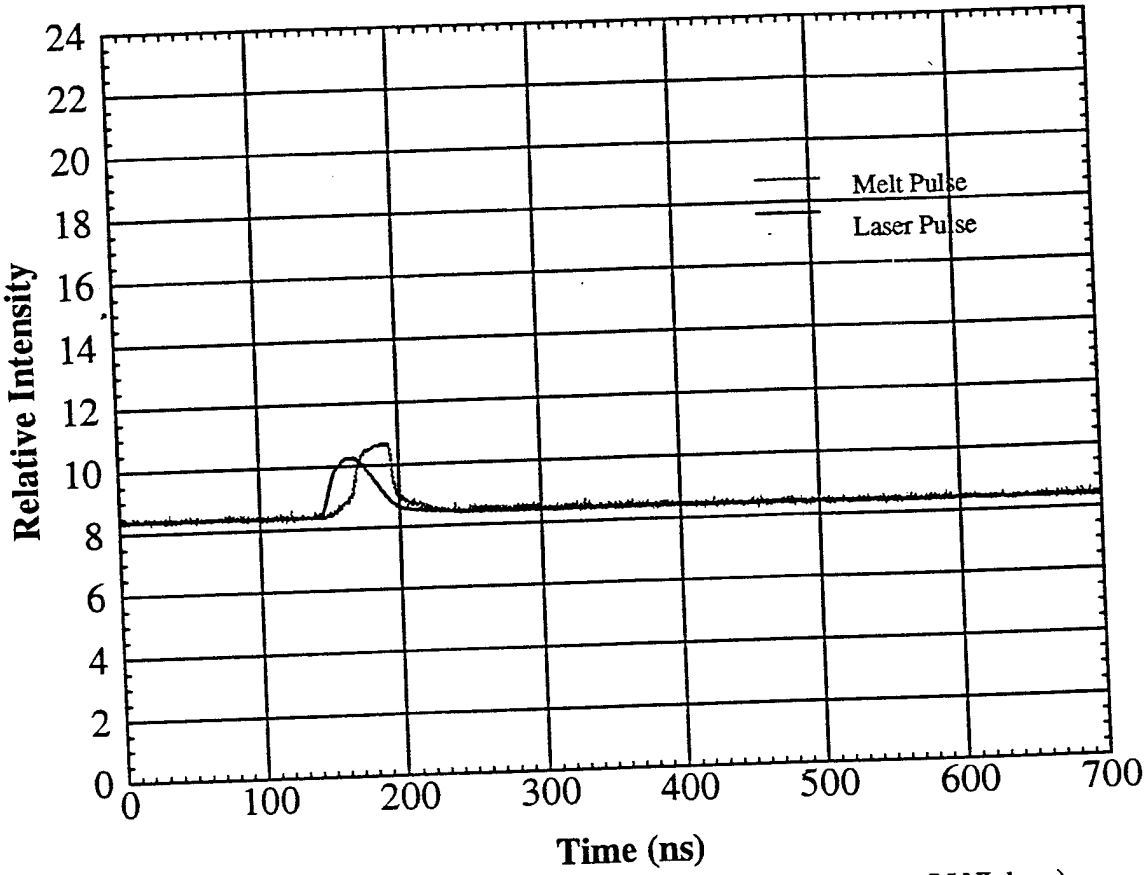


Fig. 6.10. The melt pulse from an LTO covered Si substrate when a laser pulse (LLNL laser) is applied. The LTO thickness is ~ 15 nm. The FWHM of the melt pulse is 26 ns.

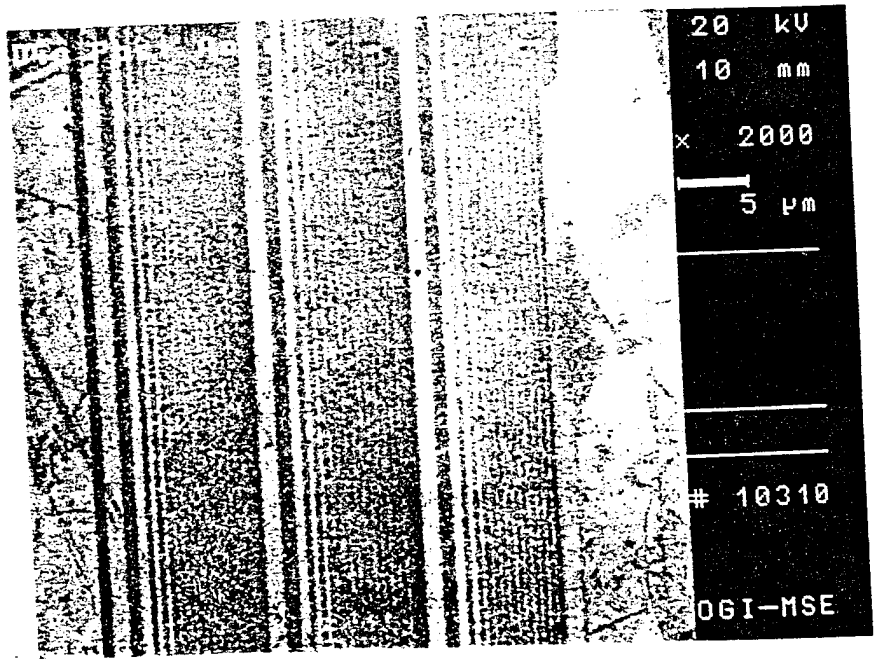
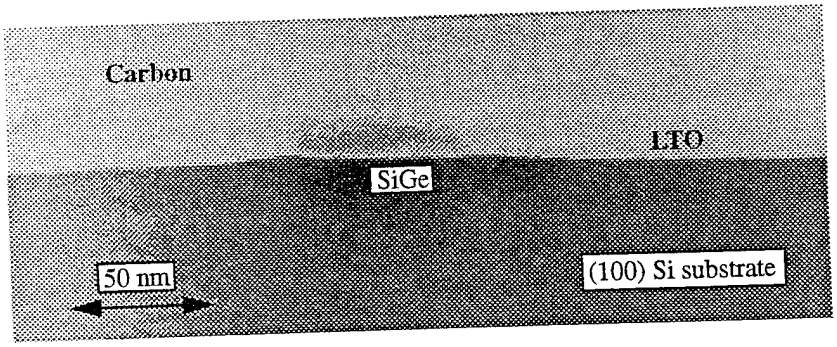


Fig. 6.11. SEM image of the SiGe wires with a thin LTO capping layer after laser irradiation.

implies an effective laser energy fluence of ~ 0.69 J/cm2 is used on the Si surface according to simulation results described in Chapter 2. Notice that the LTO layer reflects a small fraction of the laser beam [6.4].

Fig. 6.11 shows an SEM image of the Ge nanowire/Si sample after laser irradiation. The sample is still covered with the LTO capping layer as we shall see later in the TEM analysis. The 20 KeV electron beam in SEM Can easily penetrate this thin layer

(a)



(b)

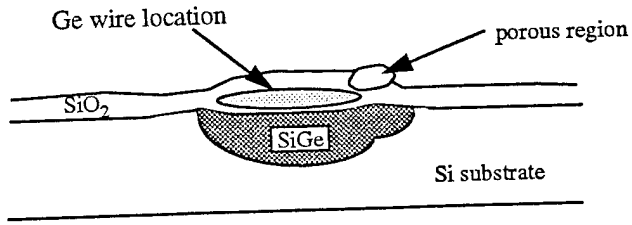


Fig. 6.12.(a) Cross-sectional TEM image of a SiGe wire formed by PLIE using LTO as a capping layer. (b) illustration of the SiGe wire interface and its relative location with respect to the original Ge wire.

with little effect on the SEM image. It can be seen that the wires retain their original continuous nature after laser irradiation. However, a slight contrast variation along the wires is observable. The black particles in the image are possibly dust or contamination from the LTO deposition.

Fig. 6.12(a) is a cross-sectional TEM image of a SiGe wire. A slight contrast is seen between the SiGe region and the rest of the substrate. The interface of the SiGe/Si is spherical, as illustrated in Fig. 6.12(b). The width and depth of the SiGe wire in the Si substrate are estimated to be about 95 nm and 25 nm respectively. Instead of inter-diffusion of the Si and Ge as expected, Ge diffuses through the thin native oxide layer between the Ge layer and the Si substrate, mixes with the Si substrate forming the SiGe alloy. The thin native oxide layer is retained after processing and is observable in the TEM image. The mechanism behind the phenomena is unclear at this time. Possible reasons are: (i) the molten Ge produced in the process carries the momentum from the high flux of photons of laser beam, and has a tendency to move towards the substrate; (ii) the rapid melting of the Ge and substrate produces an electric field [6.5], which pulls the Ge into the substrate and mixes with the Si. In addition, the native oxide layer beneath the Ge is thin and porous, allowing the Ge to diffuse through. The diffusion of materials through SiO_2 layers are also observed in the metal gate stack Al/SiO_2/Si system, where Si is observed to move through the SiO_2 layer segregating above Al after 12 hours annealing at 400°C [6.6].

High resolution TEM is performed on the samples. No defects are observed in the SiGe wire regions. The original Ge wire location is still seen in the image. Its slightly dark contrast when compared to the LTO is thought to be caused by Ge left behind in the LTO layer by incomplete diffusion. In some other locations, Ge is seen to have completely diffused into the substrate. Further experiments are needed to fully understand the cause of the incomplete diffusion. The Ge wire width is measured to be ~ 60 nm.

Comparing this process with the results obtained without using LTO capping layer, described in section 6.2, we see that the side diffusion of Ge is greatly reduced. However,

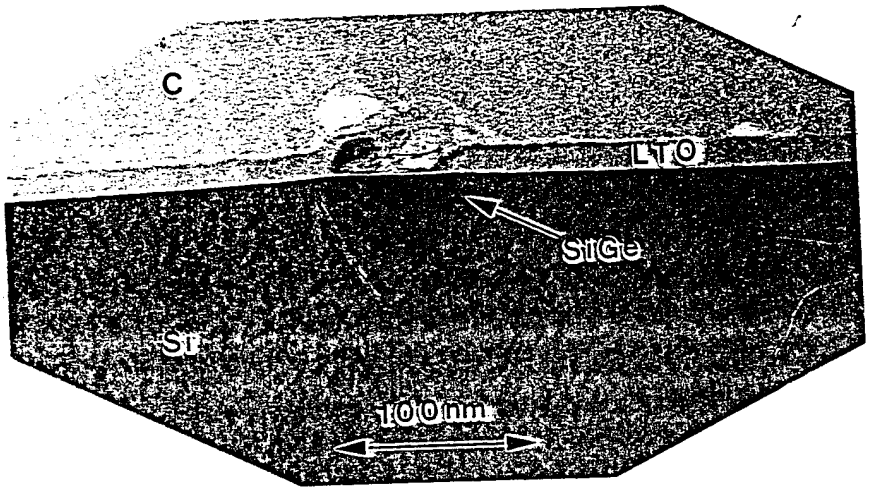
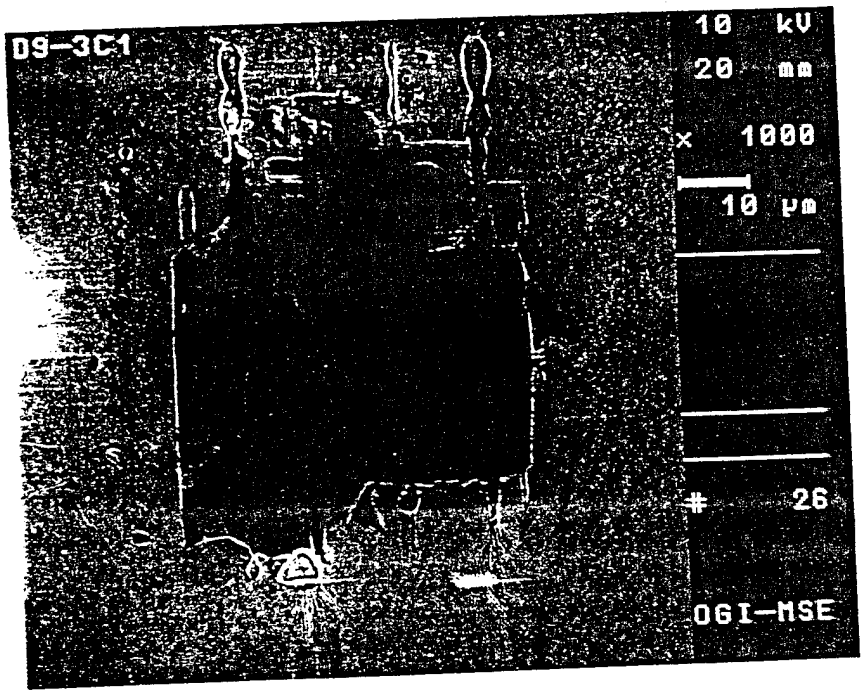


Fig.6.13. Cross-sectional TEM image of a SiGe wire showing the non-uniformity effect of the LTO layer on Ge wires.

the side diffusion appears to be asymmetrical. We believe this is the result of the non-uniformity, including thickness and density, of the LTO capping layer deposited on top of the Ge wire. The variation in thickness and density of the LTO layer produces a local variation in the transmission of the laser beam through the SiO_2 layer, which in turn produces a variation in the melt duration of the substrate. In figure 6.12, a porous region is seen in the image above the right portion of the SiGe wire. Fig. 6.13 is another cross-sectional TEM image which shows this non-uniformity effect. The LTO on the Ge wire is not uniform and is also thicker than the LTO deposited on the rest of the Si substrate. The maximum diffusion depth of the Ge into the substrate is smaller and the diffusion on the right side portion is more significant than on the left side. The Ge at the right side of the Ge wire completely diffuses into the Si substrate while some Ge remains on the left. Cleanliness of the Ge

(a)



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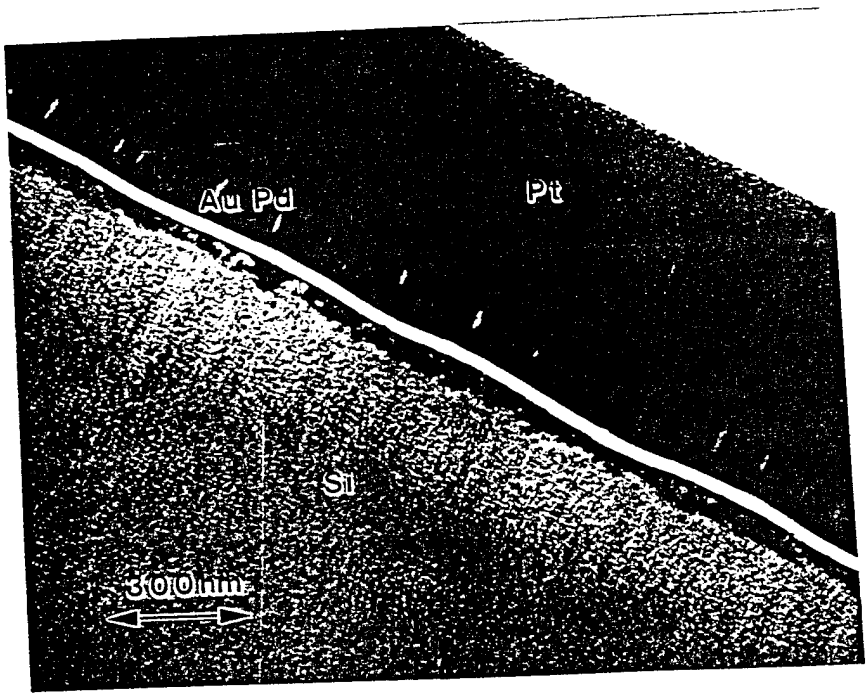

Fig. 6.14. (a) SEM and (b) XTEM image of a contaminated Ge nanowires/Si sample after laser irradiation. A highly defected layer is formed at the surface of the substrate.

wire/Si surface is believed to be important for high quality LTO deposition. Fig. 6.14 shows SEM and XTEM images of a contaminated Ge nanowires/Si sample after laser irradiation using the LTO capping layer. The contamination is believed to be hydrocarbon and other materials from SEM and FIB scanning. A highly defected layer is formed at the surface. Further experiments are needed to more fully understand and control the LTO deposition on the Ge nanowires/Si structures.

The surface of the substrate at the SiGe nanowire location in Fig. 6.12 is modified. Two shoulders are formed at the sides of the SiGe nanowire. This surface evolution is thought to be caused by the same reason as we discussed in section 6.2, in which case no LTO capping layer is used. However, the shape of the shoulder is less rounded and the size is much smaller. This indicates the LTO capping layer also effectively stabilizes the surface during the laser induced melting and resolidification process.

6.4 Conclusion

In conclusion, defect-free SiGe nanowires/Si with a cross-section of ~ 25 x 95 nm^2 are successfully fabricated using the pulsed laser induced epitaxy process using a thin LTO capping layer deposited on a Ge nanowires/Si sample. The SiGe nanowires formed in the 26 ns melting and recrystallization duration have spherical interfaces with the Si substrate. In the PLIE process, Ge diffuses into the Si substrate, mixes with the Si and forms the SiGe alloy. The quality of the LTO layer deposited on the Ge nanowires is believed to be important for the uniform diffusion of Ge into the substrate to obtain reproducible uniform SiGe nanowires. The LTO capping layer is also seen to prevent the excessive side diffusion of Ge into the Si substrate. It also stabilizes the molten surface of the substrate during the PLIE process for formation of the SiGe nanowires, resulting in less surface modification. The PLIE process for SiGe nanowires/Si samples fabricated without using the LTO capping layer results in excessive side diffusion of the Ge in the Si substrate, and is inappropriate for the fabrication of SiGe nanowires. Future work should

focus on obtaining high quality LTO depositions on Ge nanowires/Si structures and the mechanism of Ge diffusion in the PLIE process of LTO/SiGe nanowires/Si structures.

6.5 Reference

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Chapter 7

CONCLUSIONS AND FUTURE WORK

7.1 Summary and Conclusions

In the preceding chapters we demonstrated that pulsed *uv* laser induced epitaxy is a simple and effective process for fabrication of high quality SiGe nanowires on a silicon substrate. We discussed potential device applications of these SiGe nanowires. Two different approaches, i.e. focused ion beam micromachining and e-beam lithography, for obtaining patterned Ge nanowires are studied in this work. Based on the results described in the preceding chapters of this report we present the following conclusions:

1) An advanced process is developed for fabrication of SiGe nanowires using pulsed laser induced epitaxy using a XeCl excimer laser operating at a wavelength of 308 nm. In particular, Ge nanowires with a cross-section of ~ 6 x 60 nm^2 are formed in a lift-off process on the Si substrate using e-beam lithography, followed by a ~ 10 nm low-temperature oxide deposition. Defect-free SiGe nanowires with a cross-section of ~ 25 x 95 nm^2 are then produced by direct laser irradiation of the sample at an effective energy fluence of ~ 0.69 J/cm^2, which corresponds to a Si melt duration of 26 ns. The low temperature oxide is used as a capping layer to prevent side diffusion of the Ge in the Si substrate therefore keeping the width of the SiGe nanowire formed near to its patterned width. Excessive side diffusion of the Ge resulting in subsequent broadening of the SiGe wire width is observed when the low-temperature oxide capping layer is not used. Since the low-temperature oxide partially reflects the laser beam, its quality and uniformity are important for uniform Ge diffusion, and in turn, the uniformity of the SiGe nanowires.

2) In the above mentioned PLIE process for fabrication of the SiGe nanowires, Ge diffuses through the thin native oxide beneath the Ge wires forming the SiGe alloy in the Si substrate. No evidence of Si migration into the Ge wire location is observed. Interaction of the laser beam with the Ge nanowires/Si structure produces surface evolution in the PLIE process. This surface evolution is attenuated by the use of the LTO capping layer on the Ge nanowires.

3) Fabrication of SiGe nanowires in Si is made possible by the availability of technologies to initially fabricate Ge nanowires on the Si substrate. E-beam lithography proved to be an effective technique for fabrication of the Ge nanowires. Focused ion beam micromachining is also a promising technique to fabricate Ge nanowires. However, problems resulting from unexpected removal of materials by the FIB tail and contamination from the enhanced etching agent need to be addressed. As patterning technologies advance, we believe Ge nanowires with widths of < 10 nm will be available in the near future, resulting in the smaller dimension for the SiGe nanowires.

4) An advanced FIB assisted, cross-sectional TEM specimen preparation technique is developed for examination of the localized surface nano-structures. In particular, a multi-layer protection scheme i.e. Pt/Au-Pd/C/nano-structures/Si is developed with FIB assisted marking and *in situ* Pt deposition. This technique allows effective high resolution cross-sectional TEM characterization of SiGe nanowires with a high success rate.

5) Two advanced device structures, a quantum wire device and a lateral SiGe HBT based on SiGe nanowire technology are proposed. The lateral SiGe HBT is designed based on gas immersion laser doping, a technology similar to PLIE. The associated processing procedures used are compatible with current advanced CMOS processes. A MEDICI simulation of the lateral SiGe HBT shows a maximum cut-off frequency of 36 GHz

with a current gain of 260. Performance characteristics of the device are comparable to vertical SiGe HBT structures.

7.2. Suggestions for Future Work

In this work, we demonstrate the feasibility of using pulsed laser induced epitaxy to fabricate high quality SiGe nanowires. The effort has focused on the development of the processes for fabrication of the wires, not the mechanism understanding PLIE or applications and electrical characteristics of the SiGe nanowires. Both are beyond the scope of this work and represent individual research topics for future efforts. As a result of our efforts, the following topics are considered to be of great importance for continued development of PLIE technology for application in nano-fabrication.

1) *Improving the quality of SiGe nanowires fabricated using PLIE*

In this work, we observed that the quality of the low temperature oxide used for the capping layer on nanowires formed by the lift-off process is important in determination of the quality of the SiGe nanowires. The deposition process of this low-temperature oxide on the Ge nanowires/Si structures should be improved in order to obtain high quality, uniform thin film LTO on the nano-structures. Since the perfection and dimensions of the SiGe nanowires depend upon the quality and dimension of the Ge nanowires, further investigation into the fabrication of minimum dimension, high quality Ge nanowires is required to achieve the minimum dimension and highest quality for the SiGe nanowires. In addition, all work must performed in a clean room environment to avoid contamination seen in this effort.

2) *Further investigation of the mechanism of PLIE*

At the present time, the mechanisms behind the PLIE process is not fully understood. We discussed this briefly in Chapter 2. In Chapter 6, we described, for the first

time, the surface evolution and Ge diffusion behavior observed during the PLIE process, but have little knowledge about the physics behind the phenomena. Further investigation into the mechanisms understanding the PLIE process is a topic of interest for the future applications of this technique.

3) *Device demonstration and electrical characterization*

The primary undertaking of this effort was to show the feasibility of fabrication of SiGe nanowires using PLIE. We also proposed two novel device structures based on the SiGe nanowires in Chapter 3. Fabrication of these devices and their electrical characterization is necessary to prove that PLIE technology may be applied in nano-fabrication. In addition, SiGe quantum dot structures may be demonstrated using the PLIE technology as an understandable further demonstration of the capability of PLIE in this arena.