Final Technical Report

VLSI Reliability Research

8-6-92

Contract:
ONR N00014-85-0603

Principal Investigator: Chenming Hu
Department of Electrical Engineering
and Computer Sciences
University of California at Berkeley
Berkeley, CA 94720

This document has been approved for public release and sale; its distribution is unlimited.
Abstract

Aggressive scaling toward submicron VLSI technologies has greatly heightened the need for a better basic understanding of the reliability failure mechanisms and the need for better testing methods and technological solutions. This project researched these issues for the four leading failure modes of VLSI systems: oxide wearout, radiation effects, hot-electron-induced degradation, and interconnect and contact electromigration. We have developed quantitative physical (not simply empirical) models for the failure mechanisms, more accurate methods for testing, screening and reliability prediction, and explored promising new technologies for improved VLSI reliability. Many of the research results have already been accepted and used by the semiconductor industry.
Research in VLSI Reliability

I. Introduction

In order to increase the circuit density and speed of VLSI systems, microelectronic device geometry is shrinking from a few microns to submicron and beyond. This scaling has greatly heightened the need for a better understanding of the failure mechanisms affecting the long-term reliability of VLSI systems and for improved methods of designing and testing for reliability. In contrast to production technologies and circuit performances, whose failures to meet specifications will be either obvious or relatively easily discovered before the circuits are incorporated into complex systems or missions, reliability failures cannot be easily or completely eliminated. When they do occur, reliability failures can be costly in many ways. Yet, until recently, reliability issues have been given little systematic scientific research. They are relegated to empirical burn-in screening and costly design band-aids.

Analysis of field failures and laboratory test have identified three failure mechanisms as being the most important for VLSI systems. They are oxide wearout, hot-electron failures and contact and interconnect failures. We have investigated all these three failure mechanisms.

Due to aggressive scaling, the nature of reliability failures is undergoing a subtle change. Gross extrinsic defects used to be the main cause of, for example, oxide and contact failures. Now, the lifetime of a normally good oxide and contact becomes the issue. On the negative side, this has made reliability a more urgent issue, one that must be considered at the design stage. On the positive side, this has made some of the reliability failures more predictable and allowed reliability research to be performed on a larger group of samples. Interestingly, insights gained from studying these "predictable" failures will also help us to deal with the gross-defect failures, which remain important and significant.

The goal of this research was to perform basic scientific research into the mechanisms of the three leading hard failure modes: hot-electron-induced degradations, and contact and metal failures. Failure models have been developed and methods to improve reliability assurance through design, processing, and testing techniques have been invented and developed.

III. List of Publications


48. Book Chapter

IV. Ph.D. Students Graduated
Nine. Presently employed at MIT, University of Texas (Austin), Intel, TI, Motorola, Cypress Semiconductor, and Lawrence Berkeley Laboratory.

V. Best Paper Awards


VI. Keynote Address and Invited Papers


VII. Summary of Work Accomplished

The numbers in parentheses refer to the publications in Sec. III.

- Showed that hot-electron stress has no significant impact on oxide integrity, but hot hole injection significantly accelerates oxide wearout (7, 18). This additional "worst case" for MOSFET oxide reliability has attracted two followup studies by DEC and Hitachi, both published in 1990.
- An "effective thinning" model is proposed so that oxide reliability can be quantified from ramp breakdown data (8, 19, 32).
- The first oxide burn-in model was developed (27) and a comprehensive approach to oxide reliability prediction was introduced (43). The theoretical minimum oxide thickness for 20 year operation at 5.5 V was determined to be 80 Å.
- A method for making 230 Å oxide behave as a 60 Å tunneling oxide for EEPROM without the defect and reliability problem of the very thin oxide was proposed and demonstrated (9, 38).
- An AC electromigration model was developed (12, 26, 40) and the self-heating effect characterized (12, 33). Electromigration data at up to 20 MHz was collected (40) while previous studies never could exceed 0.5 MHz.
- World record of MOSFET speed (22 ps) was set and the reliability and performance constraints of highly scaled devices were determined (20, 21, 25).
- It was shown that no threshold (power supply) voltage exists for hot electron effects, contrary to previous optimistic suggestion (25, 44).
- A new total-overlap LDD structure was proposed (41).
- For the first time, an individual hot-electron-generated interface trap was observed and characterized. The technique was the random telegraphic noise (42).
- Preliminary reliability simulator development was carried out (34, 37, 39).

VIII. Interaction with Industry

The IC industry, in general, has considered our research highly relevant to the development of high density reliable IC's. Besides the awards and honors listed above, industry interest may be evidenced by the fact that supplementary funding for our reliability research has been provided by TI, GE, Rockwell International, Hughes, AMD, Signetics, and Sandia National Laboratory.

We were diligent in transferring knowledge generated by this research contract. Means for knowledge transfer included publication in journals and conferences, participation in industry workshops and standard committee (JDEC), career and summer student employment, visits and seminars at company sites, informal and organized visits by industry personnel to our laboratory, etc. Our new emphasis on reliability simulation, in our opinion, will be a major boost for knowledge transfer—it is considerably easier and more convenient for a large segment of IC engineers to use knowledge embedded in a turn-key software than to use the knowledge in a hundred journal articles. Developing improved device and process on the base of reliability physics knowledge is another form of knowledge transfer.