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OPERATION AND MAINTENANCE MANUAL,
ULTRASONIC FISH DETERRENT SYSTEM

by

James L. Pickens
Instrumentation Services Division

DEPARTMENT OF THE ARMY
Waterways Experiment Station, Corps of Engineers
3909 Halls Ferry Road, Vicksburg, Mississippi 39180-6199

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Final Report

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# Operation and Maintenance Manual, Ultrasonic Fish Deterrent System

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The Ultrasonic Fish Deterrent system, developed at Waterways Experiment Station, Vicksburg, Mississippi, consists of eight underwater transducers powered by eight 2 KVA switching amplifiers. The input signals to these amplifiers are controlled by a microprocessor and signal conditioner, also developed at WES. The timing durations and frequencies are variable, set by an external computer and can be changed to fit the parameters deemed optimum for the conditions found.

This report describes the various circuits, wiring diagrams, and function charts of the control chassis and microprocessor located in the console as well as instructions for changing the parameters with a computer.

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Preface

This report describes a fish deterrent system developed at the US Army Engineer Waterways Experiment Station (WES) by James L. Pickens, Instrumentation Services Division (ISD). Chief of ISD was George P. Bonner.

Commander and Director of WES was COL Larry B. Fulton, EN. Technical Director was Dr. Robert W. Whalin.
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OPERATION AND MAINTENANCE MANUAL,  
ULTRASONIC FISH DETERRENT SYSTEM

Introduction

The Ultrasonic Fish Deterrent (UFD) system, developed at Waterways Experiment Station, Vicksburg, Mississippi, consists of eight underwater transducers powered by eight 2 KVA switching amplifiers. The input signals to these amplifiers are controlled by a microprocessor and signal conditioner, also developed at WES. The timing durations and frequencies are variable, set by an external computer and can be changed to fit the parameters deemed optimum for the conditions found.

Since simultaneous transmissions result in field cancellation within the transmitted array, the transducers are sequentially triggered, producing a traveling acoustic field (Figure 1). Each transducer has its own impedance matching circuit, so that equal peak pulses will produce equal power out (Figure 2). It has been found during experimentation that frequent pulse signals are as effective as continuous sine waves. Therefore, the main power signals consist of bursts of high frequency energy lasting from 1-5 msec (0.001 sec to 0.005 sec) occurring at up to 20 pulses per second (Figure 3).

The system is designed so that operation can be totally automatic (with preselected pulse rates, frequencies, time intervals) or manually controlled with a computer at the location of the console (Figure 4). The UFD will ultimately be turned on and off by the main computer in the power plant control room, in the automatic mode.

The underwater transmitters are quartz crystal transducers, made by International Transducer Corp. of Santa Barbara, CA (Figure 5). The model No. ITC3003G is cut to resonate at between 112 KHz and 116KHz, although it will respond somewhat past these frequencies. It is driven by 1 KVA pulses from a 2 KVA power amplifier built by Instruments, Inc., of San Diego, CA. Eight of these amplifiers are sequentially enabled to drive eight separate transducers (Figure 6). These signals consist of approximately 118 KHz, 125 KHz, 132 KHz. The time each amplifier is on, and the frequency transmitted during this interval, are adjustable and are
controlled by a preset condition from the microprocessor. An external computer is used to change any of the preset conditions of operation.

A hydrophone (receiver transducer) is placed in the immediate vicinity of the underwater transmitter to monitor its signals (Figure 7). If a malfunction should occur, an alarm is activated at the console, and the red light corresponding to that channel is turned on, advising the operator as to which one is not functioning properly.

The following is a description of the various circuits, wiring diagrams, and function charts of the control chassis and microprocessor located in the console as well as instructions for changing the parameters with a computer.
Transmitter Section

The transmitter section of the system consists of the International Transducer Corporation (ITC) Model 3003G underwater transducer, driven by an Instruments, Inc., amplifier, Model SI1-16A, controlled by the WES logic control system.

The following is an explanation of the control system, including the main oscillator, sequence controller, gate control, and incremental gain control.

Oscillator Board 1 (Figure 8)

The main oscillator, Board 1 (Figure 8), consists of three separate oscillators adjustable for three separate frequencies (F1, F2, F3). These frequencies are selected by commands from the micro, energizing one of three relays on the oscillator card. F1 will be adjusted to some frequency around 118 KHz, F2 to about 124 KHz, and F3 to about 132 KHz. These frequencies can be monitored at test points on the front panel and on the printed circuit card.

Since the only way to change the amplitude of the power output signal is by changing the phase angle between the positive and negative inputs at the power amplifier, some modification of the oscillator signal is necessary. The method used to do this is readily seen in the RBRBLK2.DWG (Figure 9). By using three pairs of complimentary one-shot multivibrators on the RBRPHASE board (Figure 10) the separate oscillator signals are changed to narrow pulses, so the gain can be changed by varying the pulse width, while maintaining the frequency. The pulse width will be 1 usec, 2 usec, 3 usec for 15 sec each, respectively, for Gain 1, Gain 2, Gain 3. This will allow a "slow start" each time the system is activated, so no damage to the nearby fish will be done due to instantly being subjected to full power. The slow start will ensure the system operates at 10%, 25%, 66% of full power for 15 seconds each before full power is applied. The gain select commands originate in the microprocessor. The full power output level of the transmitter must be set at the power amplifier.
Phase Board (Board 2)

The phase board (Figure 10) changes the oscillator signal to narrow pulses for a step-up incremental gain sequence. The control to each pair of one-shots is supplied by a TTL pulse, activated by a gain select signal from the microprocessor. A Gain 1 select signal applies 5v to U2 and U3 (pin 5). The RC networks are set for 1 usec. The positive going edge of the oscillator will trigger U2, resulting in a 1 usec pulse at pin 4. The negative going edge of the oscillator signal will trigger U3, resulting in a 1 usec pulse at pin 2. These pulses are routed to the BNC output connectors, ultimately to the + and - inputs at the power amplifier. Each pair of one-shots are selected by Gain 1, 2, or 3 and result in 1, 2, or 3 usec pulses, resulting in 10%, 25%, 66% of full power out. Overall wiring diagram is found in Figure 22.

Logic Control Board (Board 3, Board 4, Figure 11)

The RBRLOGIC Board (Board 3, 4) (Figure 11) takes the oscillator signal, properly phased, and allows the signal to be sequentially applied to the power amplifier inputs. When the master timer signal from the microprocessor (T1 or T2) is on, the And gate U7A allows the phased oscillator signal to be applied simultaneously to And gates U3 and U4. The microprocessor supplies sequentially occurring gates to the And circuit so that the amplifiers work sequentially. Board 3 is for the positive amplifier inputs, Board 4 is for the negative amplifier inputs. All power amps are gated on simultaneously by T1 or T2 (see RBRBLK2.DWG) (Figure 9).

Amplifier Gate

The power amplifiers are enabled when a TTL level voltage is applied to the gate connector J-27 with T1 or T2 on.

Amplifier

Although the total amplifier is explained in the Operation and Maintenance manual, the following paragraph gives a simplified overall explanation of the Instruments, Inc. switching amplifier, Model S11-16A.
The amplifier system is actually eight separate amplifiers, each with a common maximum power output, adjusted by R12, the lower trimpot on the power control board (extreme right side of the upper bay). + 250 volts between TP2 on this card and chassis will produce a maximum output of 2.5 KW. This potentiometer should be adjusted to < 220 VDC max. at TP2 to keep from overranging the transducers. Final adjustment should be made to provide 0.5 vrms max at the front panel BNC (2 mv/v). With the proper matching transformer at the transducer, this should produce a power output of 1 KW RMS. Each amplifier channel is separate and can be operated singly by enabling only the one monitored at the front panel. The output adjustment must be made with the enable switch on and the load connected. The amplifier will not work unless the gate input to the amplifier is high (+5v TTL level).

Do not operate the amp very long with the air filters removed. This will result in overheating.

Matching Network

Each transducer cable is connected to a step-up transformer and choke coils. This will allow the amplifier to match the 50 ohm cable (RG-8 coax) with a lower voltage on the long cable. Since each channel has a high capacitive reactance due to the long cable (33 pf/ft) and a quartz transducer (4500 pf nom.), a 50 ohm transformer will allow matching, regardless of the cable length. Another transformer with a 50 ohm primary and 1:7.2 step-up ratio is placed in a box above the transducer (Figure 12). This allows full power to be restored at the top of each transducer with little loss due to cable capacitance. Together with choke coils equal to approximately 240 uH and parallel capacitors, the reactance of the transducer is virtually cancelled (Figure 13).

Each channel is individually tuned with the matching inductor and capitors in parallel with the transducers. The best compromise frequency, resulting in minimum reflected power, is 122 KHz. This setting allows the system to be operated at 119 KHz - 126 KHz with less than 10% power loss. With output transformers having selectable turns ratios, the individual channels could be tuned to reduce or eliminate reflected power altogether.
Transducer

The system uses the ITC 3003G underwater transducer, a quartz crystal, resonant at 112 KHz. These transducers are located 4 ft above each draft tube and 15 ft deep halfway between each tube (Figure 14). A total of eight transducers are installed to produce an acoustic field in front of the pump-back tubes. The lower transducers (Figure 15) are mounted at a +11 degrees angle to beam up along a 1:5 slope on the bottom of the tailrace (Figure 16). The complete description and specs are contained in the additional manufacturers manual.

Receiver

A hydrophone, ITC Model 1127, is mounted in the vicinity of each transmitter, picking up a portion of the transmitted signal (Figure 7). This signal is routed through the RBRAMP card (Figure 17) to the missing pulse detector (MPD) board. Each MPD has 4 channels and monitors the presence of a signal during the time T1 or T2 is active (Figure 18). Proper operation is indicated by a green light on the front panel. If a malfunction occurs, that particular green light will go off and its associated red light will come on. Each channel has its own MPD circuit and lights. The red light will remain on as long as that channel is not receiving a signal from that hydrophone during T1 or T2 time (Figure 19).
Microprocessor

The microprocessor requires +12 volts for operation and contains a converter for +/-12v, +5v operating voltage at approximately 150 ma. It provides internally pre-programmed, specifically timed signals for the various functions required. The schematic and timing chart (Figures 20 and 21) show how this is accomplished and the following is an explanation of its operation. A second micro is supplied as a spare.

Purpose

The purpose of this device is to provide TTL pulses to the UFD. The Rapid Fire Pulse Generator (RFPG) provides this function with 33 outputs and 2 inputs. The outputs consist of two timing signals T1 and T2, 8 signal enables, 8 amplifier enables, 3 oscillator select lines, 3 gain level lines, and 8 missing pulse detector lines. The two inputs consist of an automatic/manual select line and a computer start pulse line.

Setup

To configure the RFPG in the automatic mode or to operate it in the manual mode a terminal of some type is needed. In most cases an IBM compatible computer with a communications software package will be most convenient; however, any terminal will work.

To begin operation, connect the 36-Pin Centronics cable between the RFPG and the UFD. Next connect power via a Bendix connector to the RFPG. Common is on PIN A and +12 Volts in on PIN D. Next connect the communications cable (TC-4) between the RFPG and the terminal. An ONSET TC-4 cable must be used due to level shifting requirements. The modular end plugs into the RFPG and the DB-25 end connects to the terminal. Power up terminal or put computer in terminal mode. The RFPG communicates at 9600 baud, eight data bits, one stop bit, and no parity. Make sure CAPS LOCK is engaged. Place the power switch on the RFPG in the ON position. When the RFPG is powered up it checks to see whether it is in the manual or automatic mode. Therefore, to switch modes first power switch to OFF, change modes, and then power switch to ON.
Manual Mode Operation

In the manual mode, the user has the option to choose two functions. Selecting Function 1 places the RFPG in the T1 mode. First the user selects an oscillator and then starts and stops rapid fire by pressing S and Q respectively. Pressing X will take the user back to the manual mode menu. Selecting function 2 places the RFPG in a mode where all eight channels are continuously enabled. First the user selects an oscillator and then starts and stops continuous enable by pressing S and Q respectively. Pressing X will take the user back to the manual mode menu.

Automatic Mode Operation

In the automatic mode, the user enters predetermined values for:

T1
T2
TIME BETWEEN T1 and T2
TIME BETWEEN T2 AND NEXT T2
TIME ON FOR EACH OSCILLATOR

Oscillators select lines, one through three, will be fired sequentially and will be free running regardless of the state of T1 and T2. Once the values have been entered, the RFPG goes into a holding pattern where it waits for a computer start pulse or an S key from the terminal. Once the computer start pulse line goes high or the S key is pressed the RFPG follows through its timing sequence. The RFPG continues operation until the Q key is pressed or the computer start pulse line goes low depending on how the procedure was started. Upon completion, the RFPG displays the previous inputs and falls back into its holding pattern. To change the predetermined inputs, the user must power switch to OFF and then reapply power.
In the event of a power failure, the +12 volts to the micro is routed through a Time Delay Relay (TDR) to allow the computer time to boot up before power is applied to the microprocessor (approximately 1.5 minutes).

**Power**

The power required for the system is 240 volt, single phase at 30 A. A 5 KVA isolation 480 volt, transformer is used to step down the 480 volts available to 240 volts with a 110v outlet to supply AC for the electronics. The microprocessor power is supplied by a 12 volt battery, permanently connected to a battery charger through a TDR.
OVERHEAD VIEW OF SOUND SYSTEM RADIATION PATTERN

SOLID PATTERN IS -15 FT BETWEEN INTAKES
BROKEN PATTERN IS -45 FT DIRECTLY OVER INTAKES

80m

>100m

PUMP STORAGE BAYS

CONV TURBINE BAYS

FIG. 1
MATCHING COILS NEEDED FOR ITC TRANSDUCERS

\[ \text{O} = 3150 \text{ pF} \quad \triangle = 3450 \text{ pF} \quad \square = 4600 \text{ pF} \quad \times = 5000 \text{ pF} \]

FREQUENCY IN KILOHERTZ

FIG. 2
SEQUENTIAL FIRING__STATIONS 1-8
HI FREQ BURSTS @ 10% DUTY CYCLE
RICHARD B RUSSELL DAM
Typical Transmitter Station

8 2KW Switching Amps

Fig. 4
INSTRUMENTS INC.
S-16 POWER AMPLIFIER

FRONT

REAR

FIG. 6
10 sec TIMER1
off 5 sec TIMER2

TTL LEVEL PULSES 8 USEC SEL GAIN2 GAIN1

PHASE BOARD

ONE SHOT

GAIN 1
GAIN 2
GAIN 3

GATE 3

3 usec Pulse Produces 70% Full Power Out

ALL OSCILLATORS INDIVIDUALLY SELECTABLE FROM MICRO

118 KHz OSC.
F1 SEL

125 KHz OSC.
F2 SEL

132 KHz OSC.
F3 SEL

.005 sec SEQUENTIAL FIRING

Computer Start Pulse

Automatic Operation 10 sec on- 5 sec off

Computer stop pulse

| 20 ppm |

111 Pulse Widths And Gate Times
Controlled By The Microprocessor
Programmable With The Computer

Manual operation

FIG. 9
Signals from logic 80A are routed to + amp inputs
Signals from logic 80B are routed to - amp inputs
1 1/2 IN CONDUIT

1 1/2 IN CONDUIT

TERMINAL BLOCK

CAPACITORS

OUTPUT TRANSFORMER

MATCHING COILS

10 BY 10 BREAKOUT BOX LOCATED ON PARAPET WALL ABOVE EACH BAY
PERCENT OF POWER LOST DUE TO TRANSDUCER MISMATCH

FREQUENCY IN KILOHERTZ

FIG. 13
This board interfaces the MICROPROCESSOR board and the GAIN LEVEL board with the UFD to provide system I/O.
TI USER DEFINED TIME. LIMITS ARE FROM 10 MINUTES TO 60 MINUTES.

T2 USER DEFINED TIME. LIMITS ARE FROM 1 MINUTE TO 30 MINUTES.

TIME BETWEEN T1 AND T2 USER DEFINED TIME. LIMITS ARE FROM 10 MINUTES TO 60 MINUTES.

OSC. 1 - OSC. 4 USER DEFINED TIME. LIMITS ARE FROM 5 MINUTES TO 15 MINUTES.

AMP GATE 1 - AMP GATE 8 FIRING ORDER IS ALSO USER DEFINED: NOT NECESSARILY OSC 1, OSC 2, ...

AMP GATE 1 - AMP GATE 8 CONTINUOUSLY ENABLED WHENEVER T1 OR T2 IS HIGH.

AS & MPD 1 - AS & MPD 8 AS & MPD REFER TO AMP SIGNAL AND MISSING PULSE DETECTOR RESPECTIVE. PULSES ARE FIRED CONTINUOUSLY WHENEVER T1 OR T2 IS HIGH. PULSES ARE 200 MS APART: THAT IS, EACH CHANNEL PRODUCES 5 PULSES /

PULSE WIDTH PROGRESSES AS FOLLOWS: 7 MS FOR 15 SECONDS 10 MS FOR 15 SECONDS 15 MS FOR THE REMAINDER OF THE ACTIVE MODE (T1 OR T2).

FIG. 21
* NOTE. AFTER PREDETERMINED VALUES HAVE BEEN ENTERED IN THE AUTOMATIC MODE, THE RFPG WILL BEGIN EXECUTION AFTER THE COMPUTER START LINE GOES HIGH OR IF AN <S> KEY IS PRESSED.

THE RFPG WILL STOP EXECUTION AFTER THE COMPUTER START LINE GOES LOW OR IF A <Q> KEY IS PRESSED.

ES.

ES.

5. OSC 2, OSC 3, OSC 4.

RESPECTIVELY.

BLED.

5 PULSES / SECOND.

2).
### Table 1
RAPID FIRE PULSE GENERATOR (RFPG) SYSTEM INPUT/OUTPUT

<table>
<thead>
<tr>
<th>36-Pin Centronics Connector</th>
<th>40-Pin Interface Board Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>AMP. SIGNAL 8</td>
</tr>
<tr>
<td>19</td>
<td>2</td>
<td>AMP. SIGNAL 1</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>AMP. SIGNAL 7</td>
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<tr>
<td>20</td>
<td>4</td>
<td>AMP. SIGNAL 2</td>
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<tr>
<td>3</td>
<td>5</td>
<td>AMP. SIGNAL 6</td>
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<td>21</td>
<td>6</td>
<td>AMP. SIGNAL 3</td>
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<tr>
<td>4</td>
<td>7</td>
<td>AMP. SIGNAL 5</td>
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<tr>
<td>22</td>
<td>8</td>
<td>AMP. SIGNAL 4</td>
</tr>
<tr>
<td>5</td>
<td>9</td>
<td>MPD 1</td>
</tr>
<tr>
<td>23</td>
<td>10</td>
<td>MPD 8</td>
</tr>
<tr>
<td>6</td>
<td>11</td>
<td>MPD 2</td>
</tr>
<tr>
<td>24</td>
<td>12</td>
<td>MPD 7</td>
</tr>
<tr>
<td>7</td>
<td>13</td>
<td>MPD 3</td>
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<td>25</td>
<td>14</td>
<td>MPD 6</td>
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<tr>
<td>8</td>
<td>15</td>
<td>MPD 4</td>
</tr>
<tr>
<td>26</td>
<td>16</td>
<td>MPD 5</td>
</tr>
<tr>
<td>9</td>
<td>17</td>
<td>AMP. GATE 1</td>
</tr>
<tr>
<td>27</td>
<td>18</td>
<td>AMP. GATE 8</td>
</tr>
<tr>
<td>10</td>
<td>19</td>
<td>AMP. GATE 2</td>
</tr>
<tr>
<td>28</td>
<td>20</td>
<td>AMP. GATE 7</td>
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<tr>
<td>11</td>
<td>21</td>
<td>AMP. GATE 3</td>
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<tr>
<td>29</td>
<td>22</td>
<td>AMP. GATE 6</td>
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<tr>
<td>12</td>
<td>23</td>
<td>AMP. GATE 4</td>
</tr>
<tr>
<td>30</td>
<td>24</td>
<td>AMP. GATE 5</td>
</tr>
<tr>
<td>13</td>
<td>25</td>
<td>AUTO/MAN MODE (INPUT)</td>
</tr>
<tr>
<td>31</td>
<td>26</td>
<td>MICRO START/STOP (INPUT)</td>
</tr>
<tr>
<td>14</td>
<td>27</td>
<td>OSCILLATOR 3</td>
</tr>
<tr>
<td>32</td>
<td>28</td>
<td>OSCILLATOR 4 (Do not use)</td>
</tr>
<tr>
<td>15</td>
<td>29</td>
<td>T2</td>
</tr>
<tr>
<td>33</td>
<td>30</td>
<td>T1</td>
</tr>
<tr>
<td>16</td>
<td>31</td>
<td>OSCILLATOR 2</td>
</tr>
<tr>
<td>34</td>
<td>32</td>
<td>OSCILLATOR 1</td>
</tr>
<tr>
<td>17</td>
<td>33</td>
<td>GAIN LEVEL 3</td>
</tr>
<tr>
<td>35</td>
<td>34</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>35</td>
<td>GAIN LEVEL 2</td>
</tr>
<tr>
<td>36</td>
<td>36</td>
<td>GAIN LEVEL 1</td>
</tr>
</tbody>
</table>

* All signals are outputs unless stated otherwise in function description.
MICROPROCESSOR BOARD

This listing was compiled as an alternative to drawing a schematic of the specified board. This was done since the only components on the board are the two Tattle V's, three sips of pulldown resistors, and two UART connectors.

Corresponding sMARTWORK FILE for PRINTED CIRCUIT BOARD — TATSFIR

<table>
<thead>
<tr>
<th>ORIGIN</th>
<th>DESTINATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MICRO I Pin 14 -STBY</td>
<td>MICRO I Pin 15 REG 5V</td>
</tr>
<tr>
<td>MICRO I Pin 15 REG 5V</td>
<td>MICRO I Pin 14 -STBY</td>
</tr>
<tr>
<td>MICRO I Pin 16 I/O D16</td>
<td>MICRO II Pin 25 CLR AMP GATE &amp; MPD</td>
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<tr>
<td>MICRO I Pin 17 I/O D15</td>
<td>MICRO I Pin 26 I/O D9</td>
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<tr>
<td>MICRO I Pin 18 I/O D14</td>
<td>MICRO I Pin 23 GAIN LEVEL CLOCK</td>
</tr>
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<td>MICRO I Pin 19 I/O D13</td>
<td>MICRO I Pin 10 OSC. SEL 0</td>
</tr>
<tr>
<td>MICRO I Pin 20 DIG.GND</td>
<td>MICRO I Pin 53.55 Mother Board Gnd</td>
</tr>
<tr>
<td>MICRO I Pin 21 I/O D12</td>
<td>MICRO II Pin 22 I/O D11</td>
</tr>
<tr>
<td>MICRO I Pin 22 I/O D11</td>
<td>MICRO I Pin 12 OSC. SEL 3</td>
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<tr>
<td>MICRO I Pin 23 UDI</td>
<td>MICRO I Pin 2 I UART CON.</td>
</tr>
<tr>
<td>MICRO I Pin 24 I/O</td>
<td>MICRO I Pin 6 UDO</td>
</tr>
<tr>
<td>MICRO I Pin 25 I/O D10</td>
<td>MICRO I Pin 19 I/O D13</td>
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<tr>
<td>MICRO I Pin 26 I/O D9</td>
<td>MICRO I Pin 14 OSC. SEL 1</td>
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<td>MICRO I Pin 27 I/O D8</td>
<td>MICRO I Pin 13 OSC. SEL 2</td>
</tr>
<tr>
<td>MICRO I Pin 28 I/O D7</td>
<td>MICRO I Pin 36 ADDR (SEL A) AMP GATE</td>
</tr>
<tr>
<td>MICRO I Pin 29 I/O D6</td>
<td>MICRO I Pin 38 ADDR (SEL B) AMP GATE</td>
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<tr>
<td>MICRO I Pin 30 I/O D5</td>
<td>MICRO I Pin 18 T1</td>
</tr>
<tr>
<td>MICRO I Pin 31 I/O D4</td>
<td>MICRO I Pin 39 ADDR (SEL C) AMP GATE</td>
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<td>MICRO I Pin 32 I/O D3</td>
<td>MICRO I Pin 20 T2</td>
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<tr>
<td>MICRO I Pin 33 I/O D2</td>
<td>MICRO I Pin 19 Input Auto/Manual Select</td>
</tr>
<tr>
<td>MICRO I Pin 34 I/O D1</td>
<td>MICRO I Pin 22 Input Computer Start Level</td>
</tr>
<tr>
<td>MICRO I Pin 35 I/O D0</td>
<td>MICRO I Pin 20 Latch AMP GATE &amp; MPD</td>
</tr>
<tr>
<td>MICRO I Pin 37 BAT +</td>
<td>MICRO I Pin 41.43 Mother Board +12V</td>
</tr>
<tr>
<td>MICRO II Pin 14 -STBY</td>
<td>MICRO II Pin 15 REG 5V</td>
</tr>
<tr>
<td>MICRO II Pin 15 REG 5V</td>
<td>MICRO II Pin 14 -STBY</td>
</tr>
<tr>
<td>MICRO II Pin 17 I/O D19</td>
<td>MICRO II Pin 25 I/O D10</td>
</tr>
<tr>
<td>MICRO II Pin 20 DIG.GND</td>
<td>MICRO II Pin 53.55 Mother Board Gnd</td>
</tr>
<tr>
<td>MICRO II Pin 21 I/O D12</td>
<td>MICRO II Pin 9 Latch AMP SIGNAL</td>
</tr>
<tr>
<td>MICRO II Pin 22 I/O D11</td>
<td>MICRO II Pin 21 I/O D12</td>
</tr>
<tr>
<td>MICRO II Pin 23 UDI</td>
<td>MICRO II UART CON.</td>
</tr>
<tr>
<td>MICRO II Pin 24 UDO</td>
<td>MICRO II UART CON.</td>
</tr>
<tr>
<td>MICRO II Pin 25 I/O D10</td>
<td>MICRO II Pin 11 CLR AMP SIGNAL</td>
</tr>
<tr>
<td>MICRO II Pin 26 I/O D9</td>
<td>MICRO II Pin 17 I/O D15</td>
</tr>
<tr>
<td>MICRO II Pin 28 I/O D7</td>
<td>MICRO II Pin 16 ADDR (SEL A) AMP SIGNAL &amp; MPD</td>
</tr>
<tr>
<td>MICRO II Pin 29 I/O D6</td>
<td>MICRO II Pin 15 ADDR (SEL B) AMP SIGNAL &amp; MPD</td>
</tr>
<tr>
<td>MICRO II Pin 31 I/O D4</td>
<td>MICRO II Pin 17 ADDR (SEL C) AMP SIGNAL &amp; MPD</td>
</tr>
<tr>
<td>MICRO II Pin 37 BAT +</td>
<td>MICRO II Pin 41.43 Mother Board +12V</td>
</tr>
<tr>
<td>MICRO I UART Pin 1 GND</td>
<td>EDGE CON. Pin 53.55 Mother Board Gnd</td>
</tr>
<tr>
<td>MICRO I UART Pin 2 UDI</td>
<td>MICRO I Pin 23 UDI</td>
</tr>
<tr>
<td>MICRO I UART Pin 4 +5V</td>
<td>EDGE CON. Pin 46.48 Mother Board +5V</td>
</tr>
<tr>
<td>MICRO I UART Pin 6 UDO</td>
<td>MICRO I Pin 24 UDO</td>
</tr>
<tr>
<td>MICRO II UART Pin 1 GND</td>
<td>EDGE CON. Pin 53.55 Mother Board Gnd</td>
</tr>
<tr>
<td>MICRO II UART Pin 2 UDI</td>
<td>MICRO II Pin 23 UDI</td>
</tr>
<tr>
<td>MICRO II UART Pin 4 +5V</td>
<td>EDGE CON. Pin 46.48 Mother Board +5V</td>
</tr>
<tr>
<td>MICRO II UART Pin 6 UDO</td>
<td>MICRO II Pin 24 UDO</td>
</tr>
</tbody>
</table>

All Digital Output lines of each Micro are tied to a pulldown resistor with the exception of D4. D4, on both MICROs must stay pulled high as it is shipped from the factory.
Table 3
RAPID FIRE PULSE GENERATOR (RFPG)
MOTHER BOARD CONNECTOR PINOUT

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>DATA</th>
<th>PIN NO.</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>COMMON</td>
<td>2</td>
<td>COMMON</td>
</tr>
<tr>
<td>3</td>
<td>COMMON</td>
<td>4</td>
<td>COMMON</td>
</tr>
<tr>
<td>5</td>
<td>+5 VDC</td>
<td>6</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>7</td>
<td>+5 VDC</td>
<td>8</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>9</td>
<td>D12 MICRO II (LATCH AMP SIG &amp; MPD)</td>
<td>10</td>
<td>D13 MICRO I (OSC 0)</td>
</tr>
<tr>
<td>11</td>
<td>D10 MICRO II (CLEAR AMP SIG &amp; MPD)</td>
<td>12</td>
<td>D11 MICRO I (OSC 3)</td>
</tr>
<tr>
<td>13</td>
<td>D8 MICRO I (OSC 2)</td>
<td>14</td>
<td>D9 MICRO I (OSC 1)</td>
</tr>
<tr>
<td>15</td>
<td>D6 MICRO II (S1 ADDR SEL)</td>
<td>16</td>
<td>D7 MICRO II (S0 ADDR SEL)</td>
</tr>
<tr>
<td>17</td>
<td>D4 MICRO II (S2 ADDR SEL)</td>
<td>18</td>
<td>D5 MICRO I (T1)</td>
</tr>
<tr>
<td>19</td>
<td>D2 MICRO I (AUTO/MAN SEL)</td>
<td>20</td>
<td>D3 MICRO I (T2)</td>
</tr>
<tr>
<td>21</td>
<td>D0 MICRO I (LATCH AMP GATE)</td>
<td>22</td>
<td>D1 MICRO I (COMPUTER START/STOP)</td>
</tr>
<tr>
<td>23</td>
<td>D14 MICRO I (GAIN LEVEL CLK)</td>
<td>24</td>
<td>D15 MICRO I (HOUSEKEEPING)</td>
</tr>
<tr>
<td>25</td>
<td>D16 MICRO I (CLEAR AMP GATE)</td>
<td>26</td>
<td>GAIN LEVEL 1</td>
</tr>
<tr>
<td>27</td>
<td>NO CONNECTION</td>
<td>28</td>
<td>GAIN LEVEL 2</td>
</tr>
<tr>
<td>29</td>
<td>NO CONNECTION</td>
<td>30</td>
<td>NO CONNECTION</td>
</tr>
<tr>
<td>31</td>
<td>NO CONNECTION</td>
<td>32</td>
<td>GAIN LEVEL 3</td>
</tr>
<tr>
<td>33</td>
<td>NO CONNECTION</td>
<td>34</td>
<td>NO CONNECTION</td>
</tr>
<tr>
<td>35</td>
<td>NO CONNECTION</td>
<td>36</td>
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<td>37</td>
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<td>38</td>
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</tr>
<tr>
<td>39</td>
<td>NO CONNECTION</td>
<td>40</td>
<td>NO CONNECTION</td>
</tr>
<tr>
<td>41</td>
<td>+12 VDC UNREGULATED</td>
<td>42</td>
<td>+12 VDC UNREGULATED</td>
</tr>
<tr>
<td>43</td>
<td>+12 VDC UNREGULATED</td>
<td>44</td>
<td>+12 VDC UNREGULATED</td>
</tr>
<tr>
<td>45</td>
<td>+5 VDC</td>
<td>46</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>47</td>
<td>+5 VDC</td>
<td>48</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>49</td>
<td>-12 VDC</td>
<td>50</td>
<td>-12 VDC</td>
</tr>
<tr>
<td>51</td>
<td>-12 VDC</td>
<td>52</td>
<td>-12 VDC</td>
</tr>
<tr>
<td>53</td>
<td>COMMON</td>
<td>54</td>
<td>COMMON</td>
</tr>
<tr>
<td>55</td>
<td>COMMON</td>
<td>56</td>
<td>COMMON</td>
</tr>
<tr>
<td>57</td>
<td>+12 VDC</td>
<td>58</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>59</td>
<td>+12 VDC</td>
<td>60</td>
<td>+12 VDC</td>
</tr>
</tbody>
</table>
SSI Gates
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:
Y = A\* B

SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)

See page 86

01
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
Y = A\* B

SN5401/SN7401(J, N)
SN54H01/SN74H01(J, N)
SN54L01/SN74L01(J, N)
SN54L501/SN74L501(J, N, W)
SN54S01/SN74S01(J, N, W)

See page 88

02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
Y = A + B

SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54L502/SN74L502(J, N, W)
SN54S02/SN74S02(J, N, W)

See page 82
**54/74 Families of Compatible TTL Circuits**

### SSI Gates... Logic and Pin Assignments (Top Views)

#### 03

- **Quadruple 2-Input Positive-NAND Gates with Open-Collector Outputs**

  **Positive Logic:**
  
  \[ y = \overline{AB} \]

  See page 68

  - SN54LS03/SN74LS03 (J, N)
  - SN54L03/SN74L03 (J, N)
  - SN54LS03/SN74LS03 (J, N, W)
  - SN54LS03/SN74LS03 (J, N, W)

#### 04

- **Hex Inverters**

  **Positive Logic:**
  
  \[ y = \overline{A} \]

  See page 96

  - SN54D04/SN74D04 (J, N)
  - SN54L04/SN74L04 (J, N)
  - SN54LS04/SN74LS04 (J, N, W)
  - SN54LS04/SN74LS04 (J, N, W)

#### 05

- **Hex Inverters with Open-Collector Outputs**

  **Positive Logic:**
  
  \[ y = \overline{A} \]

  See page 88

  - SN54D05/SN74D05 (J, N)
  - SN54D05/SN74D05 (J, N)
  - SN54LS05/SN74LS05 (J, N, W)
  - SN54LS05/SN74LS05 (J, N, W)

#### 06

- **Hex Inverter Buffers/Drivers with Open-Collector High-Voltage Outputs**

  **Positive Logic:**
  
  \[ y = \overline{A} \]

  See page 108

  - SN5406/SN7406 (J, N, W)
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES... LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

07
HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
Y = A

See page 106

08
QUADRUPLE 2-INPUT
POSITIVE-AND GATES

positive logic:
Y = AB

See page 94

09
QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
Y = AB

See page 96

10
TRIPLE 3-INPUT
POSITIVE-NAND GATES

positive logic:
Y = ABC

See page 96
### 54/74 Families of Compatible TTL Circuits

#### SSI Gates... Logic and Pin Assignments (Top Views)

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Diagrams</th>
<th>Pin Assignments</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Triple 3-Input Positive-AND Gates</td>
<td><img src="image1.png" alt="Diagram" /></td>
<td>SN54H11/SN74H11(J, N) SN54LS11/SN74LS11(J, N, W) SN54S11/SN74S11(J, N, W)</td>
</tr>
<tr>
<td>12</td>
<td>Triple 3-Input Positive-NAND Gates with Open-Collector Outputs</td>
<td><img src="image2.png" alt="Diagram" /></td>
<td>SN54H12/SN74H12(J, N, W)</td>
</tr>
<tr>
<td>13</td>
<td>Dual 4-Input Positive-NAND Schmitt Triggers</td>
<td><img src="image3.png" alt="Diagram" /></td>
<td>SN5413/SN7413(J, N, W)</td>
</tr>
<tr>
<td>14</td>
<td>Hex Schmitt-Trigger Inverters</td>
<td><img src="image4.png" alt="Diagram" /></td>
<td>SN5414/SN7414(J, N, W)</td>
</tr>
</tbody>
</table>

*See page 94*

*See page 88*

*NC – No internal connection*
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

15
TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
\[ Y = ABC \]

See page 96

16
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
\[ Y = \overline{A} \]

See page 106

17
HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
\[ Y = A \]

See page 106

20
DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
\[ Y = ABCD \]

See page 86

NC – No internal connection
### 54/74 Families of Compatible TTL Circuits

#### SSI Gates... Logic and Pin Assignments (Top Views)

<table>
<thead>
<tr>
<th>Family</th>
<th>Description</th>
<th>Logic Equation</th>
<th>Part Numbers</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>Dual 4-Input Positive-And Gates</td>
<td>( Y = ABCD )</td>
<td>SN54H21/SN74H21 (J, N)</td>
<td>See page 94</td>
</tr>
<tr>
<td>22</td>
<td>Dual 4-Input Positive-NAND Gates with Open-Collector Outputs</td>
<td>( Y = ABCD )</td>
<td>SN54H22/SN74H22 (J, N)</td>
<td>See page 88</td>
</tr>
<tr>
<td>23</td>
<td>Expandable Dual 4-Input Positive-NOR Gates with Strobe</td>
<td>( Y = \overline{G(A+B+C+D)} \times X ) ( 2Y = \overline{G(2A+2B+2C+2D)} \times \overline{X} ) ( X ) = output of SN5460/SN7460</td>
<td>SN5423/SN7423 (J, N, W)</td>
<td>See page 113</td>
</tr>
<tr>
<td>25</td>
<td>Dual 4-Input Positive-NOR Gates with Strobe</td>
<td>( Y = \overline{G(A+B+C+D)} )</td>
<td>SN5425/SN7425 (J, N, W)</td>
<td>See page 82</td>
</tr>
</tbody>
</table>
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES ... LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

26
QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

positive logic:
\[ Y = A \overline{B} \]

See page 106

27
TRIPLE 3-INPUT
POSITIVE-NOR GATES

positive logic:
\[ Y = \overline{A} + \overline{B} + \overline{C} \]

See page 92

28
QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

positive logic:
\[ Y = A \overline{B} \]

See page 102

30
8-INPUT
POSITIVE-NAND GATES

positive logic:
\[ Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} \]

See page 96

NC = No internal connection
## 54/74 Families of Compatible TTL Circuits

### SSI Gates . . . Logic and Pin Assignments (Top Views)

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Logic Equation</th>
<th>Pin Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>32</strong></td>
<td>Quadruple 2 Input Positive OR Gates</td>
<td>( Y = A + B )</td>
<td>SN5432/SN7432(J, N, W) SN54LS32/SN74LS32(J, N, W)</td>
</tr>
<tr>
<td><strong>33</strong></td>
<td>Quadruple 2 Input Positive NOR Buffers with Open-Collector Outputs</td>
<td>( Y = \overline{A + B} )</td>
<td>SN5433/SN7433(J, N, W) SN54LS33/SN74LS33(J, N, W)</td>
</tr>
<tr>
<td><strong>37</strong></td>
<td>Quadruple 2 Input Positive NAND Buffers</td>
<td>( Y = \overline{A \cdot B} )</td>
<td>SN5437/SN7437(J, N, W) SN54LS37/SN74LS37(J, N, W)</td>
</tr>
<tr>
<td><strong>38</strong></td>
<td>Quadruple 2 Input Positive-NAND Buffers with Open-Collector Outputs</td>
<td>( Y = \overline{A \cdot B} )</td>
<td>SN5438/SN7438(J, N, W) SN54LS38/SN74LS38(J, N, W)</td>
</tr>
</tbody>
</table>

See page 108

---

### Positive Logic

\[ Y = A \cdot B \]

SN5432/SN7432(J, N, W) SN54LS32/SN74LS32(J, N, W)

---

### Positive-NAND Logic

\[ Y = \overline{A \cdot B} \]

SN5437/SN7437(J, N, W) SN54LS37/SN74LS37(J, N, W)

---

### Positive-NOR Logic

\[ Y = \overline{A + B} \]

SN5433/SN7433(J, N, W) SN54LS33/SN74LS33(J, N, W)

---

### Positive-NAND Buffers with Open-Collector Outputs

\[ Y = \overline{A \cdot B} \]

SN5438/SN7438(J, N, W) SN54LS38/SN74LS38(J, N, W)
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

AND GATED JK MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRESET CLEAR CLOCK</td>
<td>J</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

positive logic: J = J1 + J2 - J, K = K1 + K2 - K

See pages 120, 124, and 128

DUAL JK FLIP-FLOPS WITH CLEAR

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLEAR CLOCK</td>
<td>J</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

See pages 120, 124, 128, and 130

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRESET CLEAR CLOCK</td>
<td>D</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

See pages 120, 124, 128, 130, and 132

H = high level (steady state); L = low level (steady state); X = irrelevant

* = high level pulse; data inputs should be held constant while clock is high, data is transferred to output on the falling edge of the pulse

T = transition from low to high level; = transition from high to low level

Q0 = the level of Q before the indicated input conditions were established

Toggel: Each output changes to the complement of its previous level on each active transition (pulse) of the clock

This configuration is not stable; that is, it will not persist when preset and clear inputs return to their inactive high level.