VAXELN Experimentation:
Programming a Real-Time
Periodic Task Dispatcher Using
VAXELN Ada 1.1

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VAXELN Experimentation: Programming a Real-Time Periodic Task Dispatcher Using VAXELN Ada

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Review and Approval

This report has been reviewed and is approved for publication.

FOR THE COMMANDER

Karl Shingler
SEI Joint Program Office

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VAXELN Experimentation: Programming a Real-Time Periodic Task Dispatcher Using VAXELN Ada 1.1

Abstract. The purpose of this paper is to provide the reader with some technical information and observations, Ada source code, and measurement results based on experimentation with respect to developing a real-time periodic task dispatcher in Ada. The results presented here are specific to a \( \mu \)VAX-II/VAXELN 2.3 target system, the VAXELN 1.1 Ada compiler, and a KWV11-C programmable real-time clock. Specifically, these results provide answers to the question: How can one achieve the effect of scheduling a set of periodic Ada tasks when the runtime frequency of some of the individual tasks is less than the clock cycle frequency supported by an Ada runtime implementation?

Executive Summary

1. Background

The Ada Embedded Systems Testbed Project's investigative approach promotes three typical stages to developing real-time systems: benchmarking; experimentation and prototyping; and designing, coding, and testing an application. To study the performance characteristics of Ada cross-compilers, we are running several existing benchmark test suites to explore the time, space, and capacity constraints associated with individual Ada features. To minimize programming risks such as those inherent in developing low-level device interfaces, we are performing evaluation experiments (i.e., prototyping) to explore programming alternatives available to an application developer, implementation strategies employed by a compiler vendor, and real-time ramifications with respect to using Ada in these high risk areas. We are also designing and implementing an application that is characteristic of real-time embedded systems. This application system provides a context for using the experiment and benchmark results and will be the primary vehicle for investigating the portability of Ada code across several target processors.

The intent of this experimentation was to investigate various programming alternatives available to an application developer for writing a real-time periodic task dispatcher in Ada. The approach was to design and prototype alternative versions of a task dispatcher for the Inertial Navigation System (INS) [INS Specification 87, INSP TLDD 87] simulator being developed by the project to support a detailed schedulability analysis of the INS periodic task set.

\(^1\)In this context, a periodically scheduled task set implies that each task in the set is executed at its own fixed frequency. A periodic task dispatcher is a software component that schedules the individual tasks at their implied runtime frequency.
2. Scope

For this particular target configuration and cross-compiler (VAXELN 2.3/VAXELN Ada 1.1), a total of four different (prototype) periodic task dispatchers were developed. Two different periodic task dispatching approaches were used; for each of these, two different synchronization techniques were used, namely, the Ada rendezvous and the VAXELN semaphore. This paper first discusses the rationale for needing a real-time periodic task dispatcher and then presents the high-level design from which the prototypes were developed. Next, the task dispatcher prototypes are described in some detail, as is the experimentation approach used to test their feasibility. Finally, the empirical results are presented and analyzed, and relevant technical observations are provided.
1. Real-Time Periodic Task Dispatcher

The Ada tasking mechanism provides the real-time application programmer with a facility to do multi-tasking. The decision to use Ada multi-tasking depends mainly on the scheduling requirements of the application. Real-time applications can be classified into three categories by their inherent scheduling requirements [MacLaren 80]: (1) purely periodic scheduling with no aperiodic events, (2) primarily cyclic with some aperiodic events and possible variations in computing loads, and (3) event-driven (totally aperiodic) and no periodic scheduling. Common practice has been to employ a cyclic executive for all three levels, but it has been shown that the benefits of Ada multi-tasking (e.g., supports aperiodic events, monitors intertask dependencies, controls task interaction, and supports cyclic processing at arbitrary frequencies) can be realized with applications having scheduling requirements falling the latter two categories [MacLaren 80]. With Ada multi-tasking, the runtime is responsible for scheduling tasks, whereas with a cyclic executive the application programmer controls the scheduling.

The Inertial Navigation System simulator must not only schedule\textsuperscript{2} periodic tasks for execution, but also must handle the scheduling of aperiodic tasks\textsuperscript{3}. Its scheduling requirements therefore fall into the second category above. As such, we decided to use Ada tasking wherever possible to meet the application’s scheduling requirements. This chapter first motivates the need for a real-time periodic task dispatcher executing on top of the Ada runtime system. It then presents a high-level description of the design of the INS executive subsystem that supports the scheduling of the INS task set via the real-time task dispatcher.

1.1. Motivation and Rationale

One of the most important concerns for developing a real-time application is satisfying timing requirements. The INS simulator has certain real-time requirements that it must meet:

1. scheduling periodic tasks at frequencies of 400, 25, 16, and 1 Hz;
2. providing a task time-out service that must notify waiting tasks after expiry of 10.24 ms; and
3. supporting a time stamp mechanism at a granularity of 2.56 ms.

The \texttt{delay} statement in Ada was designed to aid in satisfying timing deadlines. However, validated Ada compilers to date have implemented the semantics of this statement by only ensuring that the task that executes it will be suspended from further execution for \textit{at least} the duration specified, rather than supporting a guaranteed upper bound on the duration of time a task’s execution will be suspended. To further aggravate this problem, the validated Ada compilers investigated to date have at best supported a 10 ms clock cycle (\texttt{SYSTEM.TICK}). These issues in combination with the INS simulator’s requirement for a fine-grained (2.56 ms) notion of time serve as the rationale for using a programmable real-time clock and a real-time task dispatcher on top of the Ada runtime system for supporting periodic task scheduling.

\textsuperscript{2}We use the term “schedule” loosely in this report to mean that an Ada task has been marked ready to be scheduled by the Ada runtime task scheduler.

\textsuperscript{3}For example, the INS communication subsystem irregularly requests time-outs through an aperiodic task.
1.2. Top-Level Design

This section provides an overview of the INS simulator’s executive subsystem design, which serves as a prototype of the INS simulator’s real-time task dispatcher. This subsystem consists of three major components, namely a Real-Time Clock Manager, an Activation Queue Manager, and a Task Manager, each of which is represented by one Ada package as shown in Figure 1-1.

![INS Executive Subsystem - Package Dependencies](image)

Figure 1-1: INS Executive Subsystem - Package Dependencies

The rounded, unshaded rectangles in the figure represent Ada package specifications, whereas the shaded one represents package bodies; the arrows indicate the dependency relationships (an arrow from A to B implies that A depends on B). The three packages at the bottom of the diagram are a subset of the packages that the executive imports from other INS subsystems to gain visibility of the periodic tasks that are part of the task set. The remaining packages constitute the executive subsystem whose responsibilities include scheduling the periodic task set and servicing time-out requests and cancellations. The following sections briefly describe each of these packages.

1.2.1. INS Data Types

The INS Data Types package (see Appendix A.e) of the INS executive subsystem provides the common data types used by the other packages. Specifically, it defines a data type for representing the executive’s notion of time (i.e., the number of ticks since program invocation).

1.2.2. Real-Time Clock Manager

The Real-Time Clock Manager component of the INS executive subsystem provides a set of Ada interfaces to a KWV1-C programmable real-time clock [LSI-11 User’s 86]. This component consists of one Ada package (see Appendix A.a — A.d) that provides the necessary data types, procedures, functions, and exceptions for interfacing to multiple KWV1-C real-time clocks via Ada application code [Clock TR 87]. These routines support all four modes of the clock’s operation (Single Interval Interrupt, Repeated Interval Interrupts, External Event Timing Zero Base, and External Event Timing Cumulative) in addition to its five different internal clock rates (1 MHz, 100
KHz, 10 KHz, 1 KHz, 100 Hz). In addition to providing a mechanism for establishing a link between clock interrupts and an Interrupt Service Routine (ISR), the Real-Time Clock Manager supports typical programmable clock operations such as setting the clock's operation mode (e.g., repeated interrupts), setting the clock frequency, enabling and disabling clock interrupts, and programming the clock interrupt period.

1.2.3. Activation Queue Manager

The Activation Queue Manager component of the INS executive subsystem implements a single time and priority ordered task activation queue. This component is represented in the design as one package named Activation_Queue_Manager. The package specification (see Appendix A.o, A.p) exports the necessary data types, procedures, and exceptions for accessing the elements of the time-priority ordered task activation queue. Specifically, the package specification defines a data type that represents a task activation record (AR) so that the users of this package can build such data objects. An AR contains the task's name, activation period, activation time, execution priority, and its activation mode (e.g., periodic, aperiodic). The Activation Queue Manager supports typical queue operations such as inserting, fetching, deleting, and re-inserting for activation records via the exported procedural interfaces.

The implementation details of the task activation queue are hidden in the package body. The prototyping described in Chapter 2 presents the details of two different implementations of the activation queue and its corresponding operations.

1.2.4. Task Manager

The Task Manager component of the INS executive subsystem provides a centralized task name service for the entire INS simulator program in addition to supporting the operations of enabling, disabling, and querying the schedulability status (e.g., enabled for activation) of periodic INS tasks. It is represented in the design as one package named Task_Manager (see Appendix A.q, A.r). The Task Manager also provides a mechanism for registering and canceling time-out requests from the communications subsystem. The package specification exports an enumeration type that contains an enumeration literal for each task in the INS task set. The package exports subprograms to support the aforementioned operations on any of these tasks. Furthermore, the package specification exports a procedure for initializing the INS task activation queue and one for initializing the real-time clock and activating the Dispatcher task. Initializing the activation queue involves inserting activation records for each of the pre-defined periodic tasks within the INS. The process of programming the real-time clock involves setting up the mode, rate, and Interrupt Service Routine. Finally, the Task Manager implements a real-time periodic task dispatcher on top of the task services provided by the Ada runtime using interrupts generated from a real-time programmable clock.

To implement this task dispatcher, specific knowledge of the mapping between the task ID enumeration literals and the actual Ada task names within the INS simulator program is located in the package body. The Dispatcher task is a high priority Ada task within the INS simulator program. Its body has a loop that attempts to dispatch a new task at every clock interrupt. Inside the loop it first waits for the signal from the clock ISR indicating that an interrupt just occurred. It then updates its notion of time, namely the current tick number, and then requests, from the Activation_Queue_Manager, an AR of a task that should be scheduled at the current time.
Finally, then, based on the activation mode of the task represented by the returned AR, it takes appropriate action.

1.2.5. Data and Control Flow
A brief description of the data and control flow of the INS executive subsystem follows. This discussion is relative to the data and control diagram appearing in Figure 1-2 and assumes a VAXELN target system.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Initialize the activation queue. Initializing the activation queue involves creating new activation records for each of the pre-defined periodic tasks within the INS and inserting those ARs into the activation queue. Depending on the activation queue management approach, either an index for the just-inserted AR is returned or the next tick number at which time a task needs to be scheduled is returned.</td>
</tr>
<tr>
<td>2</td>
<td>Program the real-time clock's settings. The process of programming the real-time clock involves setting up the mode, rate, and Interrupt Service Routine. The association between the hardware interrupt and the Ada ISR must be established through a VAXELN service (CREATE_DEVICE); this kernel routine returns a device object tag back to the caller; as can be seen in the data/control diagram, this information is passed back to the Activate Dispatcher subprogram.</td>
</tr>
<tr>
<td>3</td>
<td>Activate the task dispatcher and instruct the real-time clock to begin generating interrupts. Prior to starting the real-time clock, the Dispatcher task is activated via an Ada rendezvous from the Activate Dispatcher subprogram. The data passed to the Dispatcher is precisely the device object returned from the CREATE_DEVICE kernel service. The Dispatcher uses this data to properly synchronize with the clock interrupts. Upon activation of the Dispatcher, the real-time clock is started.</td>
</tr>
<tr>
<td>n</td>
<td>A real-time clock interrupt occurs. The VAXELN kernel transfers control to the ISR associated with the clock interrupt.</td>
</tr>
<tr>
<td>n+1</td>
<td>The ISR signals the Dispatcher using the VAXELN Signal/Wait mechanism.</td>
</tr>
<tr>
<td>n+2</td>
<td>The Dispatcher fetches the next AR from the activation queue.</td>
</tr>
<tr>
<td>n+3</td>
<td>The Dispatcher, if necessary, activates the appropriate task for execution.</td>
</tr>
</tbody>
</table>

In Figure 1-2, rounded rectangles represent packages, rectangles correspond to individual subprograms in the body of the Task Manager, and parallelograms are Ada tasks. Note: The Dispatcher task is in the body of the Task_Manager package.

A sample main program that initiates the executive subsystem is shown below.

```ada
with Task_Manager;

procedure INS is
begin
    Task_Manager.Initialize_Activation_Queue;
    Task_Manager.Activate_Dispatcher;

end INS;
```

After this initiation sequence, the Dispatcher runs autonomously, being driven by the real-time clock interrupts (step n) and continually performing steps n+1, n+2, and n+3.
Figure 1-2: INS Executive Subsystem - Data and Control Flow Diagram
2. Real-Time Task Dispatcher Prototyping

To lessen the risks of implementing the INS simulator using Ada tasks, alternative prototype versions of the real-time periodic task dispatcher were developed to assess the schedulability of the INS periodic task set based on estimates of task execution times. This chapter presents the results of this system modeling and analysis.

2.1. Schedulability Analysis

To assess the schedulability of the INS periodic task set, the following four-step approach was taken.

Step 1 - Make real-time measurements

Prior to embarking on the modeling of the INS simulator tasking structure, it was essential to understand the internal operation of the underlying VAXELN [VAXELN Release 86, VAXELN User's 85] runtime executive. Key real-time measurements shown in Table 2-1 were either empirically obtained or taken from the VAXELN performance documentation.

<table>
<thead>
<tr>
<th>Event</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt latency (VAXELN manual)</td>
<td>33 μsec</td>
</tr>
<tr>
<td>Context switch (VAXELN manual)</td>
<td>150 μsec</td>
</tr>
<tr>
<td>VAXELN signal/wait (empirical result, no process contention)</td>
<td>285 μsec</td>
</tr>
<tr>
<td>Ada rendezvous (empirical result)</td>
<td>1780 μsec</td>
</tr>
<tr>
<td>Attitude and Heading calculations (empirical result)</td>
<td>450 μsec</td>
</tr>
</tbody>
</table>

Table 2-1: VAXELN Real-Time Measurements

Step 2 - Estimate CPU utilization for task set

As a second step in the schedulability analysis, runtime estimates for each INS periodic task were made; execution time and CPU utilization estimates for the INS task set appear in Table 2-2. The execution time of the Attitude Updater was empirically measured to be 0.45 ms, whereas the runtime for the remaining periodic tasks was estimated. The overhead associated with each periodic task represents the context-switching time for entering and leaving the task (2 context switches = 0.30 ms); for the Attitude Updater the overhead represents the sum of interrupt latency and a context switch to the Dispatcher (0.03 + 0.15 = 0.18 ms). The synchronization times associated with each periodic task is 1.48 ms, which is the measured Ada rendezvous times less 0.30 ms for context switches; the 0.29 ms of synchronization time for the Attitude Updater corresponds to the VAXELN Signal/Wait time (see Table 2-1). If the analysis is correct, the implication is that only 15% of CPU time is available for the task dispatcher and background processing.
Step 3 - Build INS tasking model

The next step of the analysis was the development of a skeletal INS tasking model. The control logic of each periodic task was virtually the same: an autonomous loop containing first a synchronization point at the top followed by code to perform the task's computation. For the sake of modeling, the computational load of each periodic task was represented using a busy wait mechanism whose variability was between 5 and 10 percent. For instance, the Velocity Updater task was instrumented with a 4 ms busy wait (see Table 2-2). This busy wait was implemented using an external subprogram call, and its basic unit of time measure was 100 µs; the routine was independently tested to be accurate to within 10%. To achieve the effect of varying the percentage of free CPU time, the duration of all of these busy waits was scalable using a global load factor. For example, a global load factor of 0.75 is equivalent to the duration of each task's busy wait being 75% of its estimated value (0.75 * 4 ms = 3 ms for the Velocity Updater); a load factor of 1.25 increases the duration of the waits to 125% of their estimated values.

Step 4 - Monitor missed deadlines

The final step of the analysis was to vary the global load factor and monitor the model behavior with respect to missed deadlines. For each dispatching technique under investigation, the global load factor was continually increased by 0.05 (its fixed point delta) until a task deadline was missed. This critical load factor value, termed the schedulability threshold, was empirically determined for each dispatching alternative implemented. These periodic task dispatching prototypes are described in the next section.

2.2. Periodic Task Dispatching Alternatives

Given the high level design abstraction for the Activation Queue Manager, described in Section 1.2.3, two different queue management approaches were implemented, each associated with its own periodic task dispatcher. For each of these two different task dispatching prototypes, two different synchronization techniques were employed, namely the Ada rendezvous and the VAXELN semaphore. This section describes the two dispatching approaches, hereafter referred to as the general-purpose queue management (GPOM) and the static queue management (SOM) approaches.
2.2.1. General Purpose Queue Management

In the general-purpose queue management approach, the ordered activation queue is implemented as an array of indices into a table of existing activation records. Thus, the manipulation (e.g., insertion, deletion) of the ARs in the queue essentially involves the proper maintenance of these indices and the AR table entries. For instance, inserting a new AR into the queue involves creating a new entry in the AR table, locating the proper queue position of this new AR based on its activation time and priority, and finally inserting its AR table index at the proper queue position while at the same time relocating any other queue elements affected by the insertion. Deletion of a specific element is similar in logic to insertion; however, at present, no mechanism is in place for reclaiming space in the AR table when ARs are deleted. Fetching an AR, of course, removes the element from the head of the ordered queue.

In this implementation, the task Dispatcher calls the Activation Queue Manager (AQM) every clock tick (2.56 ms), passing it the current time (i.e., tick number). The AQM compares this time to the activation time of the AR at the head of the queue (in this implementation, the first array element); if the values are equal, then the first AR is returned; otherwise, a null AR is returned. When a non-null AR is returned (i.e., taken off the queue), its activation mode value is checked; if it represents a periodic task, a new activation time is computed, and the AR gets updated within the table and is re-inserted into the queue. It is possible that more than one AR meets the activation time criteria specified in the Get_Activation_Record call; in such cases the first AR is always returned since it is guaranteed to have the highest execution priority; the other qualifying ARs have their activation times incremented by 1 tick and are re-inserted into the queue; however, the original schedule for the delayed tasks is maintained.

2.2.2. Static Queue Management

In the static queue management approach, the activation queue is implemented as a statically sized array of activation records. The ARs are never moved from their initial position in the array, and one special array element is reserved for the AR of the Communications Controller task, which is called when a time-out has expired. In the purist sense, the data structure is not managed as an ordered queue, but rather as an array of elements, of which one is always marked as the next AR to be returned upon a fetch operation. In this scheme, the AQM maintains information regarding the next task to be scheduled and when to schedule it by performing a linear search of the array upon each insert and fetch operation. A benefit to this approach is that the need for special processing to resolve scheduling conflicts is obviated by the linear searching upon each fetch and insert operation, since the search implicitly resolves conflicts.

In this implementation, the task Dispatcher calls the Activation Queue Manager only at the times when tasks are scheduled to be activated. Upon each insert (e.g., time-out request) and fetch (e.g., get next AR) operation, the AQM returns the next activation time. When an AR is returned (i.e., taken off the queue) to the Dispatcher, its activation mode value is checked by the AQM; if it represents a periodic task, a new activation time is computed, and the AR gets re-inserted into the queue. To handle scheduling conflicts easily, the Dispatcher fetches ARs from the AQM when the current time is either equal to (no conflicts) or past (a conflict has occurred) that time specified by the AQM as the next time to schedule.
3. Results

Empirical results produced from the schedulability analysis are presented in this chapter from two different perspectives. First, a comparison of the two queue management approaches and their associated task dispatching prototypes is made by analyzing their effects on total CPU utilization when the synchronization mechanism is held fixed. Second, an analysis of the performance ramifications of the two synchronization techniques, namely the Ada rendezvous and the VAXELN semaphore, is done with respect to total CPU utilization. Finally, relevant technical observations are provided.

3.1. Dispatching Techniques

Tables 3-1 and 3-2 show that the calculations performed by the Attitude Updater require 18% CPU utilization and that the elapsed cycle time for the general-purpose queue management (GPQM) task dispatcher is 0.10 ms (0.32 - 0.22 = 0.10 ms) slower than the looping time of the static queue management (SOM) task dispatcher. These Dispatcher cycle times measure the elapsed time (from when the Dispatcher is signaled by the ISR) of resetting the clock's interrupt flag, updating the Dispatcher's notion of time, and fetching the next AR. However, this cycle-time measurement does not include the elapsed time for activating the next periodic task to be scheduled since this time has already been accounted for as the synchronization overhead associated with each periodic task. Note: These cycle times were empirically measured using a programmable real-time clock.

Given the minor difference (0.10 ms) between the GPQM and SOM elapsed dispatching loop times, it is not surprising to find that their effective CPU utilization percentages differ by only 4% (12.8 - 8.8 = 4.0 [Tables 3-1 and 3-2]) regardless of the synchronization mechanism employed to schedule the periodic tasks. By adding in the corresponding context switching overhead (6%), the total CPU utilization percentage for each dispatching technique can be obtained. Since only one context switch, namely the one necessary to switch from the Dispatcher to another process context, is recorded as dispatching overhead for either approach, the relative difference of their total CPU utilization remains 4%. For instance, the difference in total CPU utilization percentage between the GPQM and SOM techniques using VAXELN semaphores for synchronization is 4% (97 - 93 = 4% [Table 3-2]). Comparing the Dispatcher segments of the two columns labeled "Estimate (100%)" in either Figure 3-1 or Figure 3-2 illustrates this small difference in total CPU utilization percentages attributable to the change in dispatching methods.

The imputation of the synchronization and context switching overhead for the individual periodic tasks depends on the synchronization mechanism in use. In the case of Ada rendezvous, 1.78 ms (2 context switches + synchronization time = 2 * 0.15 + 1.48 = 1.78 ms) of total synchronization overhead is charged to each periodic task; for VAXELN semaphores, only the signaling time of 0.28 ms is associated with the individual tasks since a context switch out the dispatcher has already been counted.
It is clear from inspecting Figure 3-1 that the estimated CPU utilization associated with both the
GPOS and SOM dispatching techniques, when using the Ada rendezvous for task synchronization,
is equal to or exceeds 100%; obviously in these cases, the INS task set would not be
schedulable without incurring missed deadlines. Nevertheless, empirically it is important to deter-
mine the critical point at which the task set becomes schedulable for each different dispatching
approach. The schedulability threshold represents this critical scheduling point and by its very
nature is expressed in terms of a percentage of the sum of the periodic tasks’ estimated CPU
utilizations. For example, a schedulability threshold of 82% for the INS task set implies that the
tasks are schedulable (i.e., will not miss deadlines) for only up to, but not including, a periodic
task set CPU utilization level that is 82% of the original estimate (see Tables 3-1 and 3-2).

<table>
<thead>
<tr>
<th>Task ID</th>
<th>Frequency</th>
<th>Execution</th>
<th>Overhead</th>
<th>Synch. Utilization</th>
<th>Total Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Hz)</td>
<td>(ms)</td>
<td>(ms)</td>
<td>(%)</td>
<td>(%)</td>
</tr>
<tr>
<td>Attitude Updater</td>
<td>490</td>
<td>0.45</td>
<td>0.18</td>
<td>0.28</td>
<td>18.09</td>
</tr>
<tr>
<td>Velocity Updater</td>
<td>25</td>
<td>4</td>
<td>0.90</td>
<td>1.48</td>
<td>10.00</td>
</tr>
<tr>
<td>Attitude Sender</td>
<td>16</td>
<td>10</td>
<td>0.30</td>
<td>1.48</td>
<td>18.00</td>
</tr>
<tr>
<td>Notification Sender</td>
<td>1</td>
<td>20</td>
<td>0.90</td>
<td>1.48</td>
<td>2.00</td>
</tr>
<tr>
<td>Status Request</td>
<td>1</td>
<td>100</td>
<td>0.30</td>
<td>1.48</td>
<td>10.00</td>
</tr>
<tr>
<td>Position Update</td>
<td>0.8</td>
<td>25</td>
<td>0.30</td>
<td>1.48</td>
<td>0.50</td>
</tr>
</tbody>
</table>

**Table 3-1: General/Rendezvous and Static/Rendezvous Estimated CPU Utilization**

4Since tasks under VAXLEN Ada are implemented as separate processes, the process switching times in the table
 coincide with Ada task switches.
Since the amount of CPU utilization consumed by the periodic tasks varies directly with the value of the global load factor, the corresponding "Periodic Tasks" segments of the "Estimate" columns in Figures 3-1 and 3-2 must be adjusted so that the entire CPU utilization is below 100%, thus making the task set theoretically schedulable.
For example, the schedulability threshold for the GPQM Dispatcher using Ada rendezvous for task synchronization is 75%. One can observe from the first two columns of the bar chart in Figure 3-1 that the "Periodic Task" segment shrinks to 75% of its original size to reach a total CPU utilization level under 100%. The schedulability thresholds can be read from Figures 3-1 and 3-2 and are summarized in Table 3-3.

<table>
<thead>
<tr>
<th></th>
<th>Base Calculations</th>
<th>Switch</th>
<th>Sync</th>
<th>Dispatcher Execution</th>
<th>Periodic Tasks</th>
<th>Total Utilization</th>
<th>Schedulability</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPQM/R Estimate</td>
<td>10.00</td>
<td>14.66</td>
<td>18.03</td>
<td>12.60</td>
<td>40.50</td>
<td>104</td>
<td>75</td>
</tr>
<tr>
<td>GPQM/S Estimate</td>
<td>10.00</td>
<td>13.16</td>
<td>12.65</td>
<td>12.80</td>
<td>40.50</td>
<td>97</td>
<td>199</td>
</tr>
<tr>
<td>SOM/R Estimate</td>
<td>10.00</td>
<td>14.66</td>
<td>18.03</td>
<td>8.80</td>
<td>40.50</td>
<td>120</td>
<td>65</td>
</tr>
<tr>
<td>SOM/S Estimate</td>
<td>10.00</td>
<td>13.16</td>
<td>12.65</td>
<td>9.00</td>
<td>40.50</td>
<td>93</td>
<td>110</td>
</tr>
</tbody>
</table>

Table 3-3: Estimated CPU Utilizations and Schedulability Thresholds

Interpretation of the schedulability threshold data in Table 3-3 indicates that, assuming the same synchronization mechanism, changing from the GPQM Dispatcher to the SOM Dispatcher yields a 10% (85 - 75 = 110 - 100 = 10%) increase in the schedulability threshold.

3.2. Synchronization Mechanisms

The difference in total CPU utilization (computed from the data in Tables 3-1 and 3-2) when varying the synchronization mechanism used by the Dispatcher is 7%. Specifically, for the GPQM Dispatcher, a change in its synchronization mechanism from the Ada rendezvous to a VAXELN semaphore results in a 7% (104 - 97 = 7%) savings in CPU utilization; for the SOM Dispatcher, this savings is equal to 7% (100 - 93 = 7%). This implies that using VAXELN semaphores for task synchronization uses roughly 7% less CPU time than Ada rendezvous for this real-time periodic task dispatcher application.

Since the (estimated) execution times of both the INS simulator's base calculations and periodic
tasks are constant, Table 3-3 can be used to illustrate the implications of the synchronization mechanism employed for scheduling the periodic tasks on total CPU. The bar chart (generated from this data) in Figure 3-3 clearly illustrates the pervasive effect of the Ada rendezvous on the percent of context switch, synchronization, and dispatching CPU utilization.

Finally, interpretation of the schedulability threshold data in Table 3-3 indicates that, assuming the same dispatching approach is being used, a 25% increase in the schedulability threshold results if the synchronization mechanism is changed from the Ada rendezvous to a VAXELN semaphore. Furthermore, a 35% improvement in the schedulability threshold is obtained when changing from the GPQM Dispatcher and the Ada rendezvous for synchronization to the SQM and VAXELN semaphores.

3.3. Technical Observations

The total estimated CPU utilization for the Interrupt Service Routine and the periodic task, without including the empirical results for the Dispatcher's utilization, is quite high. In the case of using Ada rendezvous for synchronization, it is 85%, and similarly for VAXELN semaphores, it totals 78%. It is clear from the tables in Tables 3-1 and 3-2 that a savings of 11% CPU utilization would be gained if the synchronization between the ISR and the Dispatcher could be eliminated. Quite simply this could be done by moving Dispatcher responsibilities into the ISR. In practice, however, this was not possible since numerous VAXELN Ada ISR restrictions limited the number of Dispatcher implementation alternatives. These ISR restrictions disallow tasking operations, input/output operations, and accessing variables not in the immediate scope of the ISR, and strongly recommend against making subprogram calls external to the ISR.

The empirical results illustrate the pervasive effect of the Ada rendezvous on the schedulability of the INS task set. Using the Ada rendezvous for synchronizing between the Dispatcher and the periodic tasks rather than VAXELN semaphores, regardless of the dispatching technique employed, results in an increase in total CPU utilization of 7%. Furthermore, for both dispatching methods implemented, given the original execution time estimates for the INS periodic tasks, using the Ada rendezvous as the synchronization mechanism results in missed task deadlines. Only when these estimates are scaled by 75% and 85% for the GPQM and SQM dispatching approaches, respectively, does the task set become schedulable assuming Ada rendezvous for task synchronization.

Interpretation of the schedulability threshold data in Table 3-3 further demonstrates the impact of the Ada rendezvous on the task set schedulability. The empirical results show that, assuming the same dispatching approach is being used, a 25% increase in the schedulability threshold results if the synchronization mechanism is changed from the Ada rendezvous to a VAXELN semaphore; moreover, a 35% improvement in the schedulability threshold is obtained when changing from the GPQM Dispatcher and the Ada rendezvous for synchronization to the SQM and VAXELN semaphores.

Based on real-time scheduling theory, the optimal rate-monotonic scheduling algorithm [Lui 73] guarantees schedulability of the INS task set for a processor utilization below 70% since the individual periodic tasks priorities are assigned in direct proportion to their execution frequencies.
However, since the INS task set CPU utilization is greater than 70%, another schedulability test based on the rate-monotonic algorithm, namely task-lumping [Sha 87], was necessary to calculate the theoretically expected schedulability thresholds. The schedulability thresholds determined empirically were consistent with those computed theoretically. For example, given the original execution time estimates for the INS periodic tasks, the SQM dispatching approach using VAXELN semaphore for task synchronization yielded a total CPU utilization level of 93%. Furthermore, it was found empirically that the task set was schedulable until the original time estimates of the periodic tasks were scaled by 1.1 or until the total CPU utilization level reached 97% (ISR + Scaled Periodic Tasks + Dispatcher = 37 + 1.1 * 41 + 15 = 97.1%). Similarly, solving for the schedulability threshold using the task-lumping method results in an expected threshold value of 1.12.
References

[Clock TR 87] Borger, M.W.
**VAXELN Experimentation: Programming a Real-Time Clock and Interrupt Handling Using VAXELN Ada 1.1.**

[INS Specification 87] Landherr, S.F., and Klein, M.H.
**INS Behavioral Specification.**

[INS TLDD 87] Klein, M.H., Landherr, S.F.
**INS Simulator Program: Top-Level Design.**


[Lui 73] Liu, C.L., Layland, J.W.


[Sha 87] Sha, L., Lehoczky, J.P., and Rajkumar, R.
**A Schedulability Test for Rate-Monotonic Priority Assignment.**

[VAXELN Release 86]
**VAXELN Ada 1.1 Release Notes**

[VAXELN User's 85]
**VAXELN User's Guide.**
Appendix A: INS Executive: Ada Source Code for SQM/Rendezvous Dispatcher

A.a. KWV_Register_Definitions Package Specification

---

------------- SEI Ada Embedded Systems Project Prologue -------------
---
--- Unit name : KWV_Register_Definitions package specification
--- Experiment : RALI
--- Version : 1.0
--- Author : Mark W. Borger
---
--- Date created : 20 Feb 1987
--- Last update : 12 Mar 1987
---
--- Host Machine : VAX/VMS 4.5
--- Target Machine : VAXELN 2.3
---
---
---
--- Abstract : This package specification provides the necessary
data types to access the Control Status and Buffer
Registers of a KWV11-C real-time programmable clock.
---
---

-- Revision History -----------------------------------------------
---
--- Date Version Author Change
--- 12 Mar 87 1.0 Mark W. Borger Added prologue
---
---

-- End of Prologue ------------------------------------------------
---
---

with SYSTEM; use SYSTEM;
with VAXELN_SERVICES;

package KWV_Register_Definitions is

-------------
-- KWV11-C Control Status Register layout
-------------
type KWV_CSR_RECORD is record

  go : BOOLEAN;  -- start the counter
  mode : UNSIGNED_2;  -- mode of operation
  rate : UNSIGNED_3;  -- clock rate
  int_ovf : BOOLEAN;  -- interrupt on overflow
  ovf_flag : BOOLEAN;  -- counter overflow occurred
  main_st1 : BOOLEAN;  -- simulate firing of st1
  main_st2 : BOOLEAN;  -- simulate firing of st2
  main_oac : BOOLEAN;  -- simulate one cy. of oac
  dio : BOOLEAN;  -- disable internal oscillator
  flag_overrun : BOOLEAN;  -- true if ovf occurs with ovf_flag still set
  st2_go_enable : BOOLEAN;  -- assertion of st2_flag sets go bit
  st2_int_enable : BOOLEAN;  -- assertion of st2_flag causes an interrupt
  st2_flag : BOOLEAN;  -- start interrupt request for st2
end record;

for KWV_CSR_RECORD use record at mod 2;

  go at 0 range 0..0;
  mode at 0 range 1..2;
  rate at 0 range 3..5;
  int_ovf at 0 range 6..6;
  ovf_flag at 0 range 7..7;
  main_st1 at 0 range 8..8;
  main_st2 at 0 range 9..9;
  main_oac at 0 range 10..10;
  dio at 0 range 11..11;
  flag_overrun at 0 range 12..12;

CMU/SEI-87-TR-32
--- ENV1-C Buffer/Preset Register layout
---
subtype ENV_BPR_TYPE is VAXHS_SETTINGS.ENV_COUNTER_TYPE;

--- Record type containing the ENV1-C's CSR and Buffer/Preset Register
---
type ENV_REGISTERS is record
CSR : ENV_CSR_RECORD; -- control/status register
BPR : ENV_BPR_TYPE; -- buffer/preset register
end record;
pragma PACK(ENV_REGISTERS);

procedure Put_CSR (CSR : in ENV_CSR_Record;
Register_Address : in ADDRESS);

function Get_CSR (Register_Address : in ADDRESS) return ENV_CSR_Record;

end ENV_Register_Definitions;

A.b. KWV_Register_Definitions Package Body

---

package body ENV_Register_Definitions is

function Convert_it is new UNCHECKED_CONVERSION(ENV_CSR_Record, UNSIGNED_WORD);
function Convert_it is new UNCHECKED_CONVERSION(UNSIGNED_WORD, ENV_CSR_Record);

procedure Put_CSR (CSR : in ENV_CSR_Record;

with UNCHECKED_CONVERSION;

end ENV_Register_Definitions;
Register_Address : in ADDRESS) is

Current_CSR : UNIGNED WORD;
CSR_Unsigned : UNIGNED WORD;
for CSR_Unsigned use at Register_Address;

begin
Current_CSR := Convert_It(CSR);
WRITE_REGISTEX(Current_CSR, CSR_Unsigned);
end Put_CSR;

function Get_CSR (Register_Address : in ADDRESS)
return ENV_CSR_Record is

CSR : ENV_CSR_Record;
Current_CSR : UNIGNED WORD;
CSR_Unsigned : UNIGNED WORD;
for CSR_Unsigned use at Register_Address;

begin
Current_CSR := READ_REGISTER(CSR_Unsigned);
CSR := Convert_It(Current_CSR);
return CSR;
end Get_CSR;

and ENV_Register_Definitions:

A.c. Real-Time Clock Manager Package Specification

---------------------- Self Ada Embedded Systems Project Prologue ----------------------

---
-- Unit name : ENVU_Clock_Manager
-- Experiment #: PA01
-- Version : 1.0
-- Author : Mark W. Borger
--
-- Date created : 17 Mar 1987
-- Last update : 18 Mar 1987
--
-- Host Machine : VAX/VMS 4.5
-- Target Machine: VAXLM 2.3
--
---------------------- ---

---------------------- ---

-- Abstract : This package specification provides the necessary
-- data types, procedures, functions, and exceptions
-- for interfacing to multiple ENVU-C real-time clocks
-- (p-bus device) via Ada application code. All four modes
-- of the clock's operation are supported in addition to
-- its five different internal clock rates. To use these
-- routines one must first invoke the Initialize procedure
-- to create a clock device object and get a clock identifier.
-- This device object can be used by the application to wait
-- on a device signal from an Interrupt Service Routine; the
-- clock id is used as a key for the remainder of the package's
-- interface. The Initialization exception is raised if
-- the VAXLM kernel device object cannot be created for
-- whatever reason. The Clock_Not_Initialized exception is
-- if a specified clock id is invalid.
--
-- These routines only support counter overflow interrupts
-- and not Schmitt trigger interrupts. The counter routines
-- (Start_Counting, Read_Counter, Stop_Counting) should only
-- be used in modes Mode_Two or Mode_Three; when used in any
-- mode, the Invalid_Clock_Mode exception will be raised.

CMU/SEI-87-TR-32 23
with VAXSLM SERVICES;
with CONDITION_HANDLING;
with SYSTEM:

package ENVIL_Clock_Manager is

    --- Data types imported from SYSTEM package
    subtype ADDRESS is SYSTEM.ADDRESS;

    --- Data types imported from CONDITION_HANDLING package
    subtype COND_VALUE_TYPE is CONDITION_HANDLING.COND_VALUE_TYPE;

    --- Data types imported from VAXSLM SERVICES package
    subtype DEVICE_TYPE is VAXSLM_SERVICES.DEVICE_TYPE;
    subtype ENV_COUNTER_TYPE is VAXSLM_SERVICES.ENV_COUNTER_TYPE;
    subtype VECTOR_NUMBER_TYPE is VAXSLM_SERVICES.VECTOR_NUMBER_TYPE;

    --- Local Data types

    type Clock_ID is private;
    type Clock_Mode is (Mode_Zero, Mode_One, Mode_Two, Mode_Three);
    type Clock_Rate is (Stop, Rate_1KHZ, Rate_10KHZ, Rate_100KHZ, Rate_1000KHZ);

    procedure Initialize(Clock_Name in STRING;
        Clock_Identifier out Clock_ID;
        Mode in Clock_Mode;
        Rate in Clock_Rate;
        Vector_Number in VECTOR_NUMBER_TYPE;
        Service_Routine in ADDRESS;
        CSR_Address in ADDRESS;
        Device_Object in DEVICE_TYPE);

    procedure Re_Initialize(Clock_Identifier : in Clock_ID;
        Mode in Clock_Mode;
        Rate in Clock_Rate);

    procedure Display_CSR (Clock_Identifier : in Clock_ID);
    procedure Enable_Interrupts (Clock_Identifier : in Clock_ID);
    procedure Disable_Interrupts (Clock_Identifier : in Clock_ID);
    procedure Generate_Interrupts (Clock_Identifier : in Clock_ID);
    procedure Reset_Interrupt_Flag (Clock_Identifier : in Clock_ID);
    procedure Clear_Overrun_Flag (Clock_Identifier : in Clock_ID);
    procedure Set_Interrupt_Period (Clock_Identifier : in Clock_ID;
        Period in ENV_COUNTER_TYPE);

    procedure Start_Counting (Clock_Identifier : in Clock_ID);
    procedure Read_Counter (Clock_Identifier : in Clock_ID);

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A.d. Real-Time Clock Manager Package Body

-- --------------------------------------------------
-- SEI Ada Embedded Systems Project Prologue        --
-- --------------------------------------------------
--
-- Name     : ENV11_Clock_Manager package body
-- Report   : PAG1
-- Version  : 1.0
-- Author   : Mark W. Borger
-- Date     : 17 Mar 87
-- Last update
--
-- Host Machine : VAX/VMS 4.5
-- Target Machine: VAXELM 2.3
--
-- --------------------------------------------------
--
-- Abstract : This package body implements the subprograms of its
-- specification. It maintains a Clock ID array containing
-- the corresponding clock’s CSR address to allow for the
-- control of multiple clocks.
--
-- Revision History ------------------------------------------------
--
-- Date    Version Author   History
-- 22 Mar 87 1.0 Mark W. Borger Added data structure to contain
--                          Mode and Rate for each Clock_ID.
--
-- End of Prologue --------------------------------------------------
--
package body ENV11_Clock_Manager is

-- Local Data types

-- type Clock (Information_Record is record
-- Rate : ClockRate;
-- Mode : ClockMode;
-- end record;
-- type Clock_Info_Array_Type is array(Clock_ID) of Clock_Info_Record;
-- type Clock_Array_Type is array(Clock_ID) of ADDRESS;
--
-- Current_Clock_Number : Clock_ID := Clock_ID'FIRST;
Rate : in Clock_Rate;
Vector_Number : in VECTOR_NUMBER_TYPE;
Service_Routine : in ADDRESS;
CSR_Address : out ADDRESS;
Device_Object : out DEVICE_TYPE)

Return_Code : out CODE_VALUE_TYPE;
ENV1_CSR_Address : ADDRESS;
Current_CSR : ENV_CSR_Record;
Time_Device : DEVICETYPE(0..0) := (others => 0);

function Convert_It is new UNCHECKED_CONVERSION(Clock_Mode, UNSIGNED_2);
function Convert_It is new UNCHECKED_CONVERSION(Clock_Rate, UNSIGNED_3);

begin
----------
-- Create the ENV11-C device object and associate with its interrupts the
-- Interrupt Service Routine.
----------
Create_Device(Status => Return_Code,
Device_Name => Clock_Name,
Vector_Number => Vector_Number,
Service_Routine => Service_Routine,
Registers => ENV1_CSR_Address,
Device_Array => Timer_Device,
Device_Count => 3);

if CONDITION_HANDLING.Success(Return_Code) then
Device_Object := Timer_Device(0);
Clock.Identifier := Current.Clock_Number;
CSR_Address := ENV1_CSR_Address;
Clock_Info(Current.Clock_Number) := ENV1_CSR_Address;
Clock_Info(Current.Clock_Number) := Clock.Information.Record'(Rate, Mode);
Current.Clock_Number := Current.Clock_Number + Clock_ID(1);
----------
-- Initialise clock via CSR settings
----------
Current_CSR := ENV_CSR_Record'(Mode => Convert_It(Mode),
Rate => Convert_It(Rate),
others => FALSE);
Put_CSR(Current_CSR, ENV1_CSR_Address);
else
raise Initialization_Error;
end if;
end Initialize;
----------

Re_Initialize procedure
with UNCHECKED_CONVERSION;
with VAXLEN_SERVICES;
with ENV_Register_Definitions;

separate (ENV11_Clock_Manager)

procedure Re_Initialize (Clock.Identifier : in Clock_ID;
Mode : in Clock_Mode;
Rate : in Clock_Rate) is

Current_CSR := Get_CSR(Clock_Arrey(Clock.Identifier));

function Convert_It is new UNCHECKED_CONVERSION(Clock_Mode, UNSIGNED_2);
function Convert_It is new UNCHECKED_CONVERSION(Clock_Rate, UNSIGNED_3);

begin
----------
-- If specified clock's CSR address is non-zero (i.e., the clock exists
-- and has been initialized) then re-initialize it by clearing the CSR
-- settings; otherwise raise an exception since the specified clock has
not been initialized properly.

--------
if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
  Current_CSR := ENV_CSR_Record'(go => FALSE,
                              mode => Convert'It BaseActivity),
                              rate => Convert'It(Rate),
                              others => FALSE);
  Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
  Clock_Info(Clock_Identifier) := Clock_Information_Record'(Rate,Mode);
else
  raise Clock_Not_Initialized;
end if;
end Be_Initialize;

Display_CSR procedure

with TEXT_IO; use TEXT_IO;
with ENV_Register_Definitions; use ENV_Register_Definitions;
with UNCHECKED_CONVERSION;

separate (KMW12_Clock_Manager)

procedure Display_CSR (Clock_Identifier : in Clock_ID) is
  Current_CSR := ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));

  package Rate_IO is new ENUMERATION_IO(Clock_Rate);
  package Mode_IO is new ENUMERATION_IO(Clock_Mode);
  package BOOLEAN_IO is new ENUMERATION_IO(BOOLEAN);

  function Convert'It is new UNCHECKED_CONVERSION(DESIGNED_2, Clock_Mode);
  function Convert'It is new UNCHECKED_CONVERSION(DESIGNED_3, Clock_Rate);

  procedure Formattted_String.Put(Str : in STRING) is
  begin
    Put(Str);
    Set_Col(20);
    Put('" => ");
    end Formattted(String.Put):

begin
  --------------
  -- If specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then display contents of CSR;
  -- otherwise raise an exception since the specified clock has
  -- not been initialized properly.
  --------------
  if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
    Formattted_String.Put("CSR.go");
    BOOLEAN_IO.Put(Current_CSR.go) ; New_Line;
    Formattted_String.Put("CSR.mode");
    Mode(IO.Put(Convert'It(Current_CSR.mode)); New_Line;
    Formattted_String.Put("CSR.rate");
    Rate_IO.Put(Convert'It(Current_CSR.rate)); New_Line;
    Formattted_String.Put("CSR.int_cvf");
    BOOLEAN_IO.Put(Current_CSR.int_cvf) ; New_Line;
    Formattted_String.Put("CSR.ovf_flag");
    BOOLEAN_IO.Put(Current_CSR.ovf_flag) ; New_Line;
    Formattted_String.Put("CSR.maint_et1");
    BOOLEAN_IO.Put(Current_CSR.maint_et1) ; New_Line;
    Formattted_String.Put("CSR.maint_et2");
    BOOLEAN_IO.Put(Current_CSR.maint_et2) ; New_Line;
    Formattted_String.Put("CSR.maint nec");
  end if;
Enable_Interrupts procedure
with ENV_register_Definitions; use ENV_register_Definitions;
separate (ENV1_CLOCK_Manager)
procedure Enable_Interrupts (Clock_Identifier : in Clock_ID) is
  Current_CSR : ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));
begin
  ---------------
  -- If specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then enable interrupts on counter overflow;
  -- otherwise raise an exception since the specified clock has
  -- not been initialized properly.
  ---------------
  if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
    Current_CSR.int_ovf := TRUE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
    else
      raise Clock_Not_Initialized;
    end if;
end Enable_Interrupts;

Disable_Interrupts procedure
with ENV_register_Definitions; use ENV_register_Definitions;
separate (ENV1_CLOCK_Manager)
procedure Disable_Interrupts (Clock_Identifier : in Clock_ID) is
  Current_CSR : ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));
begin
  ---------------
  -- If specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then disable interrupts on counter overflow;
  -- otherwise raise an exception since the specified clock has
  -- not been initialized properly.
  ---------------
  if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
    Current_CSR.int_ovf := FALSE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
SetInterrupt_Period procedure

with UNCHECKED_CONVERSION;
with VAXLX.Services; use VAXLX.Services;
with ENV_Register_Definitions; use ENV_Register_Definitions;

separate (ENV11_Clock_Manager)

procedure Set Interrupt_Period (Clock_Identifier : in Clock_ID;
                                Period : in ENV_COUNTER_TYPE) is
  Device_Ticks : ENV_COUNTER_TYPE;
  for Device_Ticks use at (Clock_Array(Clock_Identifier) + 2);
begin
  ------------
  -- if specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then set the current value of the clock
  -- interrupt period using two's complement notation; otherwise raise
  -- an exception since the specified clock has not been initialized properly.
  ------------
  if Clock_Array(Clock_Identifier) /= ADDRESS.ZERO then
    Device_Ticks := ((65536 * Period) + 1), Device_Ticks;
    else
      raise Clock_Not_Initialized;
      end if;
end Set Interrupt_Period;

Generate Interrupts procedure

with ENV_Register_Definitions; use ENV_Register_Definitions;

separate (ENV11_Clock_Manager)

procedure Generate Interrupts (Clock_Identifier : in Clock_ID) is
  Current_CSR : ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));
begin
  ------------
  -- if specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then start internal counter that causes
  -- interrupts; otherwise raise an exception since the specified clock has
  -- not been initialized properly.
  ------------
  if Clock_Array(Clock_Identifier) /= ADDRESS.ZERO then
    Current_CSR.CC := TRUE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
    else
      raise Clock_Not_Initialized;
      end if;
end Generate Interrupts;

Reset Interrupt_Flag procedure

with ENV_Register_Definitions; use ENV_Register_Definitions;

separate (ENV11_Clock_Manager)
procedure Reset_Interrupt_Flag (Clock_Identifier : in Clock_ID) is
    Current_CSR : RW_CSR_RegRec := Get_CSR(Clock_Array(Clock_Identifier));
begin
    begin
        -- If specified clock's CSR address is non-zero (i.e., the clock exists
        -- and has been initialised) then clear counter overflow flag to allow
        -- another interrupt to be generated; otherwise raise an exception since
        -- the specified clock has not been initialised properly.
        if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
            Current_CSR.ovf_flag := FALSE;
            Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
            else
                raise Clock_Not_Initialized;
                end if;
        end Reset_Interrupt_Flag;
    end

Reset_Overrun_Flag procedure
    with RW_Register_Definitions; use RW_Register_Definitions;
    separate (K861_Clock_Manager)

procedure Reset_Overrun_Flag (Clock_Identifier : in Clock_ID) is
    Current_CSR : RW_CSR_RegRec := Get_CSR(Clock_Array(Clock_Identifier));
begin
    begin
        -- If specified clock's CSR address is non-zero (i.e., the clock exists
        -- and has been initialized) then clear interrupt overrun flag:
        -- otherwise raise an exception since the specified clock has
        -- not been initialized properly.
        if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
            Current_CSR.ovf_flag := FALSE;
            Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
            else
                raise Clock_Not_Initialized;
                end if;
        end Reset_Overrun_Flag;
    end

Start_Counting procedure
    with RW_Register_Definitions; use RW_Register_Definitions;
    separate (K861_Clock_Manager)

procedure Start_Counting (Clock_Identifier : in Clock_ID) is
    Current_CSR : RW_CSR_RegRec := Get_CSR(Clock_Array(Clock_Identifier));
begin
    begin
        -- If specified clock's CSR address is non-zero (i.e., the clock exists
        -- and has been initialized) then start the clock's internal counter:
        -- otherwise raise an exception since the specified clock has
        -- not been initialized properly.
        if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
            if (Clock_Info(Clock_Identifier).Mode = Mode_Two or else
                Clock_Info(Clock_Identifier).Mode = Mode_Three) then
                Current_CSR.go := TRUE;
                Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
                else
                    raise Invalid_Clock_Mode;
            end if;
        end if;
    end Start_Counting;
Read.Counter procedure

with ENV_Register_Definitions; use ENV_Register_Definitions;
separate (ENV1_Clock_Manager)

procedure Read.Counter (Clock_Identifier : in Clock_ID;
Number_of_Ticks : out ENV_COUNTER_TYPE) is

Current_CSR : ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));

Device_Ticks : ENV_COUNTER_TYPE;
for Device_Ticks use at (Clock_Array(Clock_Identifier) + 2);

begin
---------
-- If specified clock's CSR address is non-zero (i.e., the clock exists
-- and has been initialized) then simulate an external event to
-- get current value of the clock's internal counter written to the
-- BUFFER/RESET register and then read that value and return it while
-- the clock continues to run; otherwise raise an exception since the
-- specified clock has not been initialized properly.
---------
if Clock_Array(Clock_Identifier) /= ADDRESS ZERO then
  if (Clock_Info(Clock_Identifier).Mode = Mode_Two or else
      Clock_Info(Clock_Identifier).Mode = Mode_Three) then
    Current_CSR.t2_int_enable := FALSE;
    Current_CSR.maint_st2 := TRUE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
    loop
      Current_CSR := Get_CSR(Clock_Array(Clock_Identifier));
      exit when Current_CSR.t2_flag;
    end loop;
    Number_of_Ticks := READ REGISTER(Device_Ticks);
    Current_CSR.t2_flag := FALSE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
    else
      raise Invalid_Clock_Mode;
    end if;
  else
    raise Clock_Not_Initialized;
  end if;
end Read.Counter;

Stop.Counting procedure

with ENV_Register_Definitions; use ENV_Register_Definitions;
separate (ENV1_Clock_Manager)

procedure Stop.Counting (Clock_Identifier : in Clock_ID;
Number_of_Ticks : out ENV_COUNTER_TYPE) is

Current_CSR : ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));

Device_Ticks : ENV_COUNTER_TYPE;
for Device_Ticks use at (Clock_Array(Clock_Identifier) + 2);
begin
-----------------
-- If specified clock's CSR address is non-zero (i.e., the clock exists
-- and has been initialized) then simulate an external event to
-- get current value of the clock's internal counter written to the
-- BUFFER/PRESET register and then return that value;
-- otherwise raise an exception since the specified clock has
-- not been initialized properly.
-----------------
if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
  if (Clock_Info(Clock_Identifier).Mode = Mode_Two or else
      Clock_Info(Clock_Identifier).Mode = Mode_Three)
  then
    Current_CSR.st2_int_enable := FALSE;
    Current_CSR.st2_int := TRUE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
    loop
      Current_CSR := Get_CSR(Clock_Array(Clock_Identifier));
      exit when Current_CSR.st2_int;
    end loop;
    Number_Of_Ticks := READ_REGISTER(Device_Ticks);
    Current_CSR.go := FALSE;
    Current_CSR.st2_flag := FALSE;
    Put_CSR(Current_CSR, Clock_Array(Clock_Identifier));
  else
    raise Invalid_Clock_Mode;
  end if;
else
  raise Clock_Not_Initialized;
end if;
and Stop_Counting;

Interrupts_ENABLED function
with KMV_Register_Definitions; use KMV_Register_Definitions:
separate (EML11_Clock_Manager)

function Interrupts_ENABLED (Clock_Identifier : in Clock_ID) return BOOLEAN is
  Current_CSR : KMV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));
begin
-----------------
-- If specified clock's CSR address is non-zero (i.e., the clock exists
-- and has been initialized) then return a BOOLEAN value indicating
-- whether or not the clock will generate an interrupt when its internal
-- clock overflows; overflow flag: otherwise raise an exception since
-- the specified clock has not been initialized properly.
-----------------
if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
  return Current_CSR.int_ovf;
else
  raise Clock_Not_Initialized;
end if;
end Interrupts_ENABLED;

Current_Mode function
with UNCHECKED_CONVERSION;
with KMV_Register_Definitions; use KMV_Register_Definitions:
separate (EML11_Clock_Manager)

function Current_Mode (Clock_Identifier : in Clock_ID) return Clock_Mode is
  Current_CSR : KMV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));
function Convert_It is new UNCHECKED_CONVERSION(UNSIGNED_3, Clock_Mode);
begin
    -----------
    -- If specified clock's CSR address is non-zero (i.e., the clock exists
    -- and has been initialized) then return current clock mode;
    -- otherwise raise an exception since the specified clock has
    -- not been initialized properly.
    -----------
    if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
        return Convert_It(Current_CSR.mode);
    else
        raise Clock_Not_INITIALIZED;
    end if;
end Current_Mode;

Current_Rate function
with UNCHECKED_CONVERSION;
with ENV_Register_Definitions; use ENV_Register_Definitions;
separate (ENV11_Clock_Manager);
function Current_Rate (Clock_Identifier : in Clock_ID) return Clock_Rate is
    Current_CSR : ENV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));
function Convert_It is new UNCHECKED_CONVERSION(UNSIGNED_3, Clock_Rate);
begin
    -----------
    -- If specified clock's CSR address is non-zero (i.e., the clock exists
    -- and has been initialized) then return current clock rate;
    -- otherwise raise an exception since the specified clock has
    -- not been initialized properly.
    -----------
    if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
        return Convert_It(Current_CSR.rate);
    else
        raise Clock_Not_INITIALIZED;
    end if;
end Current_Rate;

Interrupt_Period function
with UNCHECKED_CONVERSION;
with VAXEMPL_SERVICE; use VAXEMPL_SERVICE;
with ENV_Register_Definitions; use ENV_Register_Definitions;
separate (ENV11_Clock_Manager);
function Interrupt_Period (Clock_Identifier : in Clock_ID) return ENV_COUNTER_TYPE is
    Device_Ticks : ENV_COUNTER_TYPE;
    for Device_Ticks use at (Clock_Array(Clock_Identifier) + 2);
begin
    -----------
    -- If specified clock's CSR address is non-zero (i.e., the clock exists
    -- and has been initialized) then return current value of the clock
    -- interrupt period; otherwise raise an exception since the specified
    -- clock has not been initialized properly.
    -----------
    if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
        return READ_REGISTER(Device_Ticks);
    else
        raise Clock_Not_INITIALIZED;
    end if;
end Interrupt_Period;
Interrupt_Flag_On function
with NV_Register_Definitions; use NV_Register_Definitions;

separate (NV11_Clock_Manager)

function Interrupt_Flag_On (Clock_Identifier : in Clock_ID) return BOOLEAN is
Current_CSR : NV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));

begin
"---------------
  -- If specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then return current BOOLEAN value of counter
  -- overflow flag; otherwise raise an exception since the specified clock
  -- has not been initialized properly.
  "---------------
if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
return Current_CSR.ovf_flag;
else
raise Clock_Not_Initialized;
end if;
end Interrupt_Flag_On;

Overrun_Flag_On function
with NV_Register_Definitions; use NV_Register_Definitions;

separate (NV11_Clock_Manager)

function Overrun_Flag_On (Clock_Identifier : in Clock_ID) return BOOLEAN is
Current_CSR : NV_CSR_Record := Get_CSR(Clock_Array(Clock_Identifier));

begin
"---------------
  -- If specified clock's CSR address is non-zero (i.e., the clock exists
  -- and has been initialized) then return current BOOLEAN value of overrun
  -- flag; otherwise raise an exception since the specified clock
  -- has not been initialized properly.
  "---------------
if Clock_Array(Clock_Identifier) /= ADDRESS_ZERO then
return Current_CSR.flag_overrun;
else
raise Clock_Not_Initialized;
end if;
end Overrun_Flag_On;

A.e. INS Data Types Package Specification

| MODULE NAME: INS_Data_Types |
| MODULE TYPE: Package Specification |
| PURPOSE:
  Export Executive global constants and types. |
| DESCRIPTION:
  This package defines the constants and global data types
  used throughout the executive subsystem. |
package IN5_Data_Types is
  Maximum_Priority : constant NATURAL := 15;
  Maximum_Tick_Value : constant NATURAL := 34_560_000;
  Maximum_Period_Value : constant NATURAL := 313;
  Microseconds_Per_Tick : constant NATURAL := 2_560;
  subtype Tick_Range is NATURAL range 0..Maximum_Tick_Value;
  subtype Period_Range is NATURAL range 0..Maximum_Period_Value;
  subtype Priority_Range is NATURAL range 0..Maximum_Priority;
end IN5_Data_Types;

A.f. Clock Interrupt Service Routine

with VAXLS thirdVICES;
with CONDITION_HANDLING;
with IN5_Data_Types;

with SYSTEM: use SYSTEM;

procedure Timer_Interrupt_Routine
  (Device_Register : in ADDRESS;
   Comm_Region : in out IN5_Data_Types.Executive_Communication_Region;
   ISR_Context : in VAXLS_SERVICES.ISR_CONTEXT_TYPE ) is
  Return_Code : CONDITION_HANDLING.COMD_VALUE_TYPE;
  Temp_Int : INTEGER := 0;

begin
  for Index2 in 1..110 loop
    Temp_Int := Temp_Int + Index2;
  end loop:

  Comm_Region.Current_Tick_Number := Comm_Region.Current_Tick_Number + 1;

  if Comm_Region.Current_Tick_Number >= Comm_Region.Next_Schedule_Time then
    VAXLS_SERVICES.SIGNAL_DEVICE(Status => Return_Code,
                                Device_Number => 0,
                                ISR_Context => ISR_Context);
  end if;

end Timer_Interrupt_Routine;

pragma SUPPRESS_ALL;
pragma EXPORT_PROCEDURE(Timer_Interrupt_Routine);

A.g. Runtime BIT Package Specification

---
--- | MODULE NAME:       Runtime_BIT
--- | -- | MODULE TYPE:     Package Specification
--- | -- | MODULE PURPOSE:
--- | -- | This package implements the Runtime Built-In Tests
--- | -- | for the AIXTS simulator program.
--- |
A.h. Runtime BIT Package Body

package body Runtime_BIT is

  task body Runtime_BIT_Processor is
  begin
    loop
      accept Activate; -- called every 1000 msec by the dispatcher
      pragma PRIORITY(2);
      end Runtime_BIT_Processor;
      procedure Runtime_Tests; -- implements the tests
    end Runtime_BIT;

end Runtime_BIT;

-----------------------------------------------------------------------

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A.i. Motion Simulator Package Specification

---
<table>
<thead>
<tr>
<th>MODULE NAME:</th>
<th>Motion_Simulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE TYPE:</td>
<td>Package Specification</td>
</tr>
</tbody>
</table>

---
| MODULE PURPOSE:  
| This package implements the various motion simulation calculations that are the core of the AEST INS simulator program. |

---
| MODULE DESCRIPTION:  
| This package implements the various motion simulation calculations that are the core of the AEST INS simulator program. |

---
| REVISION HISTORY:  
| -- see end of listing |

---

package Motion_Simulator is

procedure Update_Attitude_and_Heading; -- called by the clock ISR every 2.56 ms

task Ship_Velocity_Updater is
  entry Activate; -- called by the dispatcher every 40.96 msec
  pragma PRIORITY(9);
end Ship_Velocity_Updater;

task Ship_Position_Updater is
  entry Activate; -- called by the dispatcher every 1300.0 msec
  pragma PRIORITY(1);
end Ship_Position_Updater;

and Motion_Simulator:

---

A.j. Motion Simulator Package Body

---
<table>
<thead>
<tr>
<th>MODULE NAME:</th>
<th>Motion_Simulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE TYPE:</td>
<td>Package Body</td>
</tr>
</tbody>
</table>

---
| MODULE PURPOSE:  
| This package implements the various motion simulation calculations that are the core of the AEST INS simulator program. |

---
| MODULE DESCRIPTION:  
| This package implements the various motion simulation calculations that are the core of the AEST INS simulator program. |

---
| REVISION HISTORY:  
| -- see end of listing |

---

pragma PAGE:
package body Motion_Simulator is

   procedure Update_Attitude_and_Heading is
      begin
         null;
      end Update_Attitude_and_Heading;

   task body Ship_Velocity_Updater is
      begin
         loop
            accept Activate;
            Load_Control.Busy_Wait(40); -- 4 milliseconds
         end loop;
      end Ship_Velocity_Updater;

   task body Ship_Position_Updater is
      begin
         loop
            accept Activate;
            Load_Control.Busy_Wait(250); -- 25 milliseconds
         end loop;
      end Ship_Position_Updater;

end Motion_Simulator;

--|---

A.k. Comms Handler Package Specification

package Comms_Handler is

   procedure Time_Out;

   task Attitude_Periodic_Message_Sender is
      entry Activate;
      pragma PRIORITY(7);
   end Attitude_Periodic_Message_Sender;

   task Navigation_Periodic_Message_Sender is
      entry Activate;
      pragma PRIORITY(5);
   end Navigation_Periodic_Message_Sender;

end Comms_Handler;

A.l. Comms Handler Package Body

with Load_Control;
with Task_Manager;
package body Comms_Handler is

   procedure Time_Out is
      begin
         null;
      end Time_Out;

   task body Attitude_Periodic_Message_Sender is
      begin
         loop
            accept Activate;
            Load_Control.Busy_Wait(100); -- 10 milliseconds
         end loop;
      end Attitude_Periodic_Message_Sender;

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A.m. Screen Area Handler Package Specification

package Screen_Area_Handler is

  task body Navigation_Periodic_Message_Sender is
  begin
    loop
      accept Activate;
      Navigation_Periodic_Message_Sender:
    end loop;
  end Navigation_Periodic_Message_Sender;

end Screen_Area_Handler;

A.n. Screen Area Handler Package Specification

with Load_Control;
package body Screen_Area_Handler is

  task body Periodic_Status_Display_Processor is
  begin
    loop
      accept Activate;
      Periodic_Status_Display_Processor:
    end loop;
  end Periodic_Status_Display_Processor;

end Screen_Area_Handler;

A.o. Activation Queue Manager Package Specification

-- | MODULE NAME: Activation_Queue_Manager (AGM)
-- | MODULE TYPE: Package Specification
-- | MODULE PURPOSE:
-- | Implement task activation queue manager.
-- | MODULE DESCRIPTION:
-- | This package provides the necessary data types, procedures, and exceptions for implementing a time-ordered activation queue. The package only supports one such queue whose implementation details are hidden within the package body.
-- | REVISION HISTORY: -- see end of listing

package Activation_Queue_Manager is

pragmas PAGE;

with Task_Manager;
with INS_Data_Types;

package Activation_Queue_Manager is
subtype Priority_Range  is IES_Data_Types.Priority_Range;
subtype Activation_Time_Range is IES_Data_Types.Time_Range;
subtype Activation_Period_Range is IES_Data_Types.Period_Range;

subtype Task_ID_Type is Task_Manager.Task_ID_Type;
type Activation_Mode_Type is (Single_Shot, Periodic, Time_Out, No.Op);

type Task_Activation_Record is record
  Task_ID : Task_ID_Type;
  Activation_Period : Activation_Period_Range;
  Activation_Time : Activation_Time_Range;
  Activation_Priority  : Priority_Range;
  Execution_Priority : Priority_Range;
  Activation_Mode : Activation_Mode_Type;
end record;

procedure Insert_Activation_Record (Record_ID : in Task_Activation_Record);
  Next_Schedule_Time : out Activation_Time_Range);

procedure Get_Activation_Record (Record_ID : out Task_Activation_Record;
  Next_Schedule_Time : out Activation_Time_Range);

procedure Delete_Activation_Record (Record_ID : Task_ID);

end Activation_Queue_Manager;

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-----------------------------------------------------------------------
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-- A.p. Activation Queue Manager Package Body

-- MODULE NAME: Activation_Queue_Manager
-- MODULE TYPE: Package Body
-- MODULE PURPOSE:
-- Implement task activation queue manager.
--
-- MODULE DESCRIPTION:
-- This package supports the implementation of a time
-- ordered task activation queue and its associated
-- interfaced exported in the package specification.
-- The activation queue is maintained as a static array of
-- activation records (ARs) as defined in the package specification.
-- The ARs are never moved from their initial position in the array and
-- one special array element is reserved for the AR of the
-- Communications Controller task, which is called when a time-out has
-- expired. The AQM maintains information regarding the next task to be
-- scheduled and when to schedule it by performing a linear search of
-- the array upon each event and fetch operation. When an AR is
-- returned (i.e., taken off the queue) to the Dispatcher, its activation
-- mode value is checked by the AQM; if it represents a periodic task, a
-- new activation time is computed, and the AR gets re-inserted into the
-- queue.
--
-- REVISION HISTORY: -- end of listing
-----------------------------------------------------------------------

pragma PAGE;

with Task_Manager; use Task_Manager;

package body Activation_Queue_Manager is

Last_Activation_Time : Activation_Time_Range := Activation_Time_Range'LAST;
Last_Task_to_Schedule : Task_ID_Type;
Activation_Records : array(Task_ID_Type) of Task_Activation_Record;

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-- Insert the specified AR information into the AR Table

procedure Insert_Activation_Record (Record_ID : in Task_Activation_Record;
    Next_Schedule_Time : out Activation_Time_Range) is
begin
    Activation_Records (Record_ID, Task_ID) := Record_ID;
    if Record_ID, Activation_Time < Next_Activation_Time and then
        Record_ID, Activation_Mode /= No_OP then
        Next_Activation_Time := Record_ID, Activation_Time;
        Next_Task_To_Schedule := Record_ID, Task_ID;
    and if;
    Next_Schedule_Time := Next_Activation_Time;
    end if;
end Insert_Activation_Record;

procedure Get_Activation_Record (Record_ID : out Task_Activation_Record;
    Next_Schedule_Time : out Activation_Time_Range) is
begin
    Record_ID := Activation_Records (Next_Task_To_Schedule);

    if Activation_Records (Next_Task_To_Schedule), Activation_Mode = Periodic then
        if Activation_Records (Next_Task_To_Schedule), Activation_Time +
                Activation_Time_Range (Activation_Records (Next_Task_To_Schedule), Activation_Period);
        and if;
        Next_Activation_Time := Activation_Records (Next_Task_To_Schedule), Activation_Time;
        Next_Task_To_Schedule := Next_Task_To_Schedule;
        Next_Schedule_Time := Next_Activation_Time;
    end if;
end Get_Activation_Record;

procedure Delete_Activation_Record (Tank_ID : in Tank_ID_Type) is
begin
    Activation_Records (Tank_ID, Task_ID) := No_OP;
end Delete_Activation_Record;

end Activation_Queue_Manager;

-- Mark AR associated with Tank_ID as not available for scheduling.
-- Its slot will most likely be used at a later date (e.g., timeouts).

-- Get next AR from the Activation Queue. Re-schedule any tasks with
-- same activation time as the one taken off the queue.

procedure Get_Next_Activation_Record (Record_ID : out Task_Activation_Record;
    Next_Schedule_Time : out Activation_Time_Range) is
begin
    Record_ID := Activation_Records (Next_Task_To_Schedule);

    if Activation_Records (Next_Task_To_Schedule), Activation_Mode = Periodic then
        if Activation_Records (Next_Task_To_Schedule), Activation_Time +
                Activation_Time_Range (Activation_Records (Next_Task_To_Schedule), Activation_Period);
        and if;
        Next_Activation_Time := Activation_Records (Next_Task_To_Schedule), Activation_Time;
        Next_Task_To_Schedule := Next_Task_To_Schedule;
        Next_Schedule_Time := Next_Activation_Time;
    end if;
end Get_Next_Activation_Record;

for Index in Tank_ID_Type'First..Tank_ID_Type'Last loop
    if Activation_Records (Index), Activation_Time < Next_Activation_Time and then
        Activation_Records (Index), Activation_Mode /= No_OP then
        Next_Activation_Time := Activation_Records (Index), Activation_Time;
        Next_Task_To_Schedule := Index;
    end if;
end loop;

Next_Schedule_Time := Next_Activation_Time;
end Get_Next_Activation_Record;

end Activation_Queue_Manager;

-- MARK HISTORY

---------------
A.4. Task Manager Package Specification

-- | MODULE NAME: Task_Manager
-- | MODULE TYPE: Package Specification
-- | MODULE PURPOSE:
-- | This package provides an interface to initialize the task activation
-- | queue and start the dispatcher of the AEM IMS simulator program.
-- | MODULE DESCRIPTION:
-- | This package provides the necessary procedures
-- | to initialize the task activation queue, start the task dispatcher,
-- | enable/disable periodic tasks, and support time-outs for base
-- | level tasks.
-- |
-- | REVISION HISTORY: -- see end of listing
-- |
pragma PAGE:

with IMS_Data_Types;

package Task_Manager is
    -- Imported data types

    subtype Activation_Time_Range is IMS_Data_Types.Tick_Range;
    subtype Activation_Period_Range is IMS_Data_Types.Period_Range;

type Task_ID_Type is
    (Ship_Velocity_Updater,
     Attitude_Periodic_Message_Sender,
     Navigation_Periodic_Message_Sender,
     Periodic_Status_Display_Processor,
     Runtime_Sky_Processor,
     Ship_Position_Updater,
     Comma_Controller)

subtype Periodic_Task_ID_Type is Task_ID_Type range
    Ship_Velocity_Updater..Ship_Position_Updater;

subtype Timeout_Task_ID_Type is Task_ID_Type range
    Comma_Controller..Comma_Controller;

procedure Initialise_Activation_Queue;
procedure Activate_Dispatcher;
function Task_Is_Enabled (Task_ID : in Periodic_Task_ID_Type) return BOOLEAN;
procedure Enable_Task (Task_ID : in Periodic_Task_ID_Type);
procedure Disable_Task (Task_ID : in Periodic_Task_ID_Type);
procedure Request_Time_Out (Task_ID : in Timeout_Task_ID_Type;
    Time_Period : in Activation_Period_Range);
procedure Cancel_Time_Out (Task_ID : Timeout_Task_ID_Type);Dispatcher_Activation_Error : EXCEPTION;
end Task_Manager;

-- | REVISION HISTORY

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A.r. Task Manager Package Body

-- Module Name: Task_Manager
-- Module Type: Package Body
-- Module Purpose: Implement a periodic task dispatcher.
-- Module Description:
| This package body implements a task dispatcher that gets and re-inserts task activation records from and onto the activation queue. The dispatcher waits for signals from a real-time clock that is generating interrupts every 2.56 milliseconds.
-- Revision History: -- see end of listing

pragma PAGE:

with Runtime_BIT;
with Comm_Handler;
with Motion_Simulator;
with RNIVL_Clock_Manager;
with Screen_Area_Handler;
with Activation_Queue_Manager;

with SYSTEM; use SYSTEM;

package body Task_Manager is

package RNIVL renames Runtime_BIT;
package COM renames Comm_Handler;
package MOS renames Motion_Simulator;
package RNIVL_Clock renames Screen_Area_Handler;
package RNIVL_Clock_Manager renames Activation_Queue_Manager;

-- Imported Data Types

type Task_Stats is (Disabled, Enabled);

subtype Clock_ID is RNIVL_Clock_Manager.Clock_ID;
subtype Device_ID is RNIVL_Clock_Manager.DEVICE_ID;
subtype RNIVL_COUNTER_TYPE is RNIVL_Clock_Manager.RNIVL_COUNTER_TYPE;

Periodic_Task_Type is (Enabled, Enabled);

type Periodic_Task is array (Periodic_Task_ID_Type) of Task_Stats :=
( Ship_Velocity_Update, => Enabled,
  Attitude_Periodic_Message_Sender => Disabled,
  Navigation_Periodic_Message_Sender => Enabled,
  Navigation_Periodic_Message_Sender => Enabled,
  Periodic_Status_Display_Processor => Enabled,
  Runtime_BIT_Processor => Enabled,
  Ship_Position_Update => Enabled );

Clock_ID isUnsigned_LONGWORD;
Comm_Area_Address isADDRESS;
Schedule_At_Tick_Number is Activation_Time_Range :=
Activation_Time_Range/LAST;

-- Local Subprograms and tasks

procedure Update_Ship_Schedule_Tick is separate;

function Current_Tick_Number return Activation_Time_Range is separate;
procedure Activate_Task (Task_ID : in Task_ID_Type;
    Missed_Deadline : out BOOLEAN);

procedure Time_Out_Task (Task_ID : in Timeout_Task_ID_Type);

task Dispatcher is
    entry Activate (Clock-Identifier : in Clock_ID;
        Clock_Device_ID : in DEVICETypeID);
        pragma PRIORITY(9);
    end Dispatcher;

    task body Dispatcher is separate:

-----------------
-- Exported Subprograms
-----------------
    procedure Initialize_ActivationQueue is separate;
    procedure Activate_Dispatcher is separate;

-----------------
-- Is the specified task enabled?
-----------------
    function Task_Is_Enabled (Task_ID : in Periodic_Task_ID_Type) return BOOLEAN is
        begin
            return Periodic_Task_State(Task_ID) = Enabled;
        end Task_Is_Enabled;

-----------------
-- Enable the specified task.
-----------------
    procedure Enable_Task (Task_ID : in Periodic_Task_ID_Type) is
        begin
            Periodic_Task_State(Task_ID) := Enabled;
            end Enable_Task;

-----------------
-- Disable the specified task.
-----------------
    procedure Disable_Task (Task_ID : in Periodic_Task_ID_Type) is
        begin
            Periodic_Task_State(Task_ID) := Disabled;
            end Disable_Task;

-----------------
-- Activate the specified task.
-----------------
    procedure Activate_Task (Task_ID : in Task_ID_Type;
        Missed_Deadline : out BOOLEAN) is
        begin
            Missed_Deadline := FALSE;
            if Task_Is_Enabled(Task_ID) then
                case Task_ID is
                    when Ship_Velocity_Update =>
                        select
                            MOD.Ship_Velocity_Update.Activate;
                        else
                            Missed_Deadline := TRUE;
                            end select;
                when Attitude_Periodic_Message_Sender =>
                    select
                        COM.Attitude_Periodic_Message_Sender.Activate;
                    else
                        Missed_Deadline := TRUE;
                        end select;
                when Navigation_Periodic_Message_Sender =>
                    select
                        end Task_ID is
                    when Ship_Velocity_Update =>
                        select
                            MOD.Ship_Velocity_Update.Activate;
                        else
                            Missed_Deadline := TRUE;
                            end select;
                when Attitude_Periodic_Message_Sender =>
                    select
                        COM.Attitude_Periodic_Message_Sender.Activate;
                    else
                        Missed_Deadline := TRUE;
                        end select;
            when Navigation_Periodic_Message_Sender =>
                        select

PROCEDURE Time_Out_Task (Task_ID : in Timeout_Task_ID_Type) is
begin
  COM.Time_Out;
end Time_Out_Task;

PROCEDURE Request_Time_Out (Task_ID : in Timeout_Task_ID_Type;
  Time_Period : in Activation_Period_Type) is
begin
  AQM.Insert_Activation_Record(
    Task_ID, Activation_Time_Range(Time_Period),
    Activation_Time_Range(Time_Period) + Current_Tick_Number,
    10, 10, AQM.Time_Out, Schedule_At_Tick_Number);
end Request_Time_Out;

PROCEDURE Cancel_Time_Out (Task_ID : Timeout_Task_ID_Type) is
begin
  AQM.Delete_Activation_Record(Task_ID);
end Cancel_Time_Out;
end Task_Manager;

--------------------------------- REVISION HISTORY ---------------------------------
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Load Control Package Specification
with ENV1.Clock_Manager;

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package Load_Control is

subtype Clock_ID is HW11_Clock_Manager.Clock_ID;

procedure Initialise (Clock_Identifier : in Clock_ID);

procedure Read_Load_Factor;

procedure Busy_Wait (Time_Period : in POSITIVE);

end Load_Control;

Load Control Package Body
with Text_IO;

package body Load_Control is

type Load_Factor_Percentage is delta 0.05 range 0.0..10.0;

My_Clock_ID : Clock_ID;
Load_Factor : Load_Factor_Percentage := 1.0;
Calibration : constant Load_Factor_Percentage := 0.75;
Factor : Load_Factor_Percentage;
Temp : BOOLEAN;

package Load_Factor_IO is new Text_IO.Fixed_IO(Load_Factor_Percentage);

procedure Initialise (Clock_Identifier : in Clock_ID) is
begin
My_Clock_ID := Clock_Identifier;
end Initialise;

---
-- Open external Factor file on host; read current value; close file
---

procedure Read_Load_Factor is
Factor_File_Name : constant STRING := "25::ps:[burger]load_factor.inp";
Factor_Files : Text_IO.FILE_TYPE;

use Text_IO;
begi
Open(Factor_Files, In_File, Factor_File_Name);
Load_Factor_IO.Get(Factor_Files, Load_Factor);
Factor := Load_Factor_Percentage(Calibration * Load_Factor);
Close(Factor_Files);
end Read_Load_Factor;

procedure Busy_Wait (Time_Period : in POSITIVE) is
begin
for Index in 1..INTEGER(Time_Period * Factor) loop
Temp := HW11_Clock_Manager.Interrupt_Flag_On(My_Clock_ID);
end loop;
end Busy_Wait;

end Load_Control;

Activate Dispatcher procedure
with Text_IO;
with Load_Control;
with Timer_Interrupt_Routine;

separate(Task_Manager)

procedure Activate_Dispatcher is
My_Clock_Name : constant STRING := "HW11";
My_Clock_ID : Clock_ID;
My_Clock_Device : DEVICE_TYPE;
CSR_Address : ADDRESS;
Period : HW_COUNTER_TYPE := HW_COUNTER_TYPE(2_560);
use TEXT_IO, IMS_Data_Types, ENV1_Clock_Manager;
begin

--- Initialise the clock to operate in mode one at a LMS rate.
--- The Interrupt Service Routine is "Timer_Interrupt_Routine".

Initialise(Clock_Name  \rightarrow My_Clock_Name,
Clock_Identifier \rightarrow My_Clock_ID,
Mode \rightarrow Mode_One,
Rate \rightarrow Rate_LMS,
Vector_Number \rightarrow 1,
Service_Routine \rightarrow Timer_Interrupt_Routine'ADDRESS,
CSR_Address \rightarrow CSR_Address,
Clock_Priority \rightarrow Clock_IFL,
Communication_Region_Size \rightarrow Executive_Communication_Region'SIZE,
Communication_Region_Address \rightarrow Comm_Region_Address,
Device_Object \rightarrow My_Clock_Device);

--- Update next schedule time in communication region.
--- Start current tick number at 0 in communication region.

declare
Comm_Region : IMS_Data_Types.Executive_Communication_Region;
for Comm_Region use at Comm_Region_Address;
begin
Comm_Region.Current_Tick_Number := 0;
Comm_Region.Next_Schedule_Time := Schedule_At_Tick_Number;
end;

--- Properly initialise load control
--- Enable clock overflow signals (interrupts)
--- Set interrupt time period to be 2560 ticks (2.56 milliseconds)
--- Start Dispatcher task
--- Start generating periodic interrupts

exception
when Initialisation_Error =>
  Put_Line("Error during clock initialisation.");
  raise Dispatcher_Activation_Error;
when Clock_Not_Initialized =>
  Put_Line("Invalid clock identifier.");
  raise Dispatcher_Activation_Error;
when others =>
  Put_Line("Unexpected exception raised back to Dispatcher_Activate.Dispatcher.");
  raise Dispatcher_Activation_Error;
end Activate_Dispatcher;

Initialize Activation Queue procedure
Dispatch task

with K911_Clock_Manager: use K911_Clock_Manager;
with VAXELA SERVICES;
with Task_ID;

separate (Task_Manager)

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"Missed deadline."

Task_IO.Put_Line("Tick #: " & INTEGER'IMAGE(Tick_Number));
end if;

when Time_Out =>
  Time_Out_Task(Current_AB.Task_ID);
when others =>
  null;
end case;
end loop;

-- Stop clock operation
--
  Re_Initiate(My_Clock_ID, Mode_zero, Stop);
end Dispatcher;

A.s. Main Program

with Task_Manager;

procedure INS is
begin
  Task_Manager.Initiate_Activation_Queue;
  Task_Manager.Activate_Dispatcher;
  and INS;

Abstract. The purpose of this paper is to provide the reader with some technical information and observations, Ada source code, and measurement results based on experimentation with respect to developing a real-time periodic task dispatcher in Ada. The results presented here are specific to a µVAX-II/VAXELN 2.3 target system, the VAXELN 1.1 Ada compiler, and a KWV11-C programmable real-time clock. Specifically, these results provide answers to the question: How can one achieve the effect of scheduling a set of periodic Ada tasks when the runtime frequency of some of the individual tasks is less than the clock cycle frequency supported by an Ada runtime implementation?