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5/1/81 - 4/30/82

MICROWAVE SEMICONDUCTOR RESEARCH -
MATERIALS, DEVICES, CIRCUITS

Contract # -
F49620-81-C-0082
This program covers the growth and assessment of Gallium Arsenide, and related compounds and alloys, for use in microwave, millimeter, and optical devices. It also covers the processing of the material into devices, and the testing of the devices. Both molecular beam epitaxy (MBE) and organo-metallic vapor phase epitaxy (OMVPE) are used for growth. Modulation doped heterostructures and very short gate field effect transistors are two areas covered. The following is a list of tasks pursued.
Task 1  Growth and characterization of GaAs for high performance microwave devices

Task 2  Investigation of microwave field-effect transistor performance limits set by layer composition and contact geometry

Task 3  Use of MBE tailored profiles for GaAs power FET's for improved performance

Task 4  MBE multiple GaAs-Al$_x$Ga$_{1-x}$As heterojunctions for confinement of electrons for improved FET performance

Task 5  High speed receivers for optical communications

Task 6  Dynamic and spectral characteristics of semiconductor laser materials and structures

Task 7  Carrier dynamics in compound semiconductors studied with picosecond optical excitation

Task 8  Advanced design techniques for microwave GaAs FET amplifiers

Task 9  Wide band circuits and systems

Ballistic Task - Gallium arsenide ballistic electron transistors.
WORK STATEMENT

TASK 1 Grow and characterize GaAs for high performance microwave devices.

TASK 2 Determine the effect of design and processing on GaAs power FET performance limitations.

TASK 3 Use MBE tailored profiles for improved GaAs power FET performance.

TASK 4 Investigate MBE multiple GaAs Al_xGa_{1-x}As heterojunctions for confinement of electrons.

TASK 5 Develop high speed receivers for optical communication using optical field effect transistors and large area epitaxial photoconductive detectors.

TASK 6 Model and construct components and subsystems which can be useful as transmitters in optical communication systems.

TASK 7 Develop advanced design techniques for microwave GaAs FET amplifiers.

TASK 8 Improve direct method of broad band circuit design.

TASK 9 Use optical excitation to study carrier dynamics in compound semiconductors.

TASK 10 Study ballistic electron effects in transistors for high frequency operation.
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Task 1 GROWTH AND CHARACTERIZATION OF GaAs FOR HIGH PERFORMANCE MICROWAVE DEVICES

L. F. Eastman and D. W. Woodard

Objective

Overall objectives are improved GaAs epitaxial materials for microwave devices and further understanding of substrate properties and their relation to interface and layer properties. The approach taken has been to employ deep level transient current spectroscopy ("current DLTS") to study the presence of traps in FET devices made with various implanted or epitaxial starting materials.

Progress

The technique of conductance DLTS was automated and made more sensitive. Sophisticated analysis routines (modified Boxcar, Fast Fourier Transform and Method of Moments), were developed and applied to the DLTS data in order to identify deep levels in GaAs MESFETs. Many levels found have never been reported. Conductance DLTS theory was developed to enable the calculation of trap densities thus obtaining trap density profiles in the active region of the FETs. The conductance DLTS experiment was also extended to temperatures as low as 150K to observe traps with smaller activation energies than previously possible. Electron traps and hole traps with energies less than 50 meV were observed for the first time in GaAs. Some of these levels can possibly be identified by comparison of the DLTS and photoluminescence data.

MESFETs fabricated from ion-implanted, MBE, VPE and LPE material were analyzed by obtaining trap profiles to enable determination of
the effects of deep levels present on the device's performance. Looping, dc drift and light sensitivity of the I-V characteristics were correlated with large densities of deep levels located at the surface and at the active region - buffer layer (or substrate) interface. Trap populations were shown to be deleterious to power applications of the devices by causing premature breakdown through impact ionization processes. It was seen that buffer layers, while decreasing the density of traps coming from the substrate, were not sufficiently opaque to eliminate them. By knowing the locations and energies of the traps in the channel, the contribution of specific deep levels to microwave performance has been calculated. Traps with energies between .07 and .2 eV contribute to the minimum excess noise figure between 1 and 80 GHz. Deeper traps, depending on their emission rates, can affect the performance of the devices down to the dc characteristics.

Electron and hole traps introduced as a result of Si$_3$N$_4$ surface passivation have been identified and profiled. Nitride capping and annealing of ion implanted material was found to introduce various low energy surface traps. The effects of these traps on microwave performance were calculated.

Degrees

G. N. Maracas, Ph.D., Jan. 1982
Publications


Objective
The objectives of this task have been to investigate experimentally and analytically the performance limits of GaAs microwave power FET devices. The approach taken has been to explore structural and materials related determinants of the breakdown voltage and output conductance.

Progress
In previous reports, FET structures having 2 micron gates and drain-source breakdown voltages of 85 volts at pinch-off were described. During the current period, the breakdown voltage of optimally designed structures was studied as a function of gate length down to 0.8 microns.

The breakdown voltage of a MESFET may be calculated by considering the operation of the device under pinched-off condition. Under these conditions a simplified electrostatic model can be used. Such a model would numerically evaluate the ionization integral over an approximate field distribution. Ladbrooke\(^{(1)}\) has performed such computer calculations which take into account the effect of gate length on breakdown voltage. These calculations predict that the gate-to-drain breakdown voltage of the MESFET will decrease with decreasing gate length. Optimum breakdown voltages observed during the course of this work for short gate lengths (0.8-1.0 microns)
indicate that this is indeed the case. Figure 1 is a plot of breakdown voltage at pinch-off as a function of gate length. The plot illustrates the calculations by Ladbrooke\(^1\) as well as the results of this work. Also indicated is the result of Tiwari\(^2\), at Cornell, who achieved 85 volts breakdown at pinch-off for a 2 micron gate. The results of this work, as well as the results of Tiwari, are for undoped LPE GaAs buffer layers 2.5 micron thick. As was previously discussed, this is at the optimum undoped buffer layer thickness necessary for high breakdown voltage and low leakage current. All of the data indicated is for a doping of \(8 \times 10^{16} \text{cm}^{-3}\), where the breakdown voltages for power FET structures used in this work have been shown to have a maximum.\(^2\) Thus, this figure is based on an optimum power structure and doping. It, therefore, indicates the best possible breakdown voltages that can be achieved given the present state-of-the-art.

Both the experimental results of this work and the theoretical results of Ladbrooke show a strong linear dependence of breakdown voltage on gate length. This result is very important for high power and high frequency MESFET design since higher frequency devices must have shorter gate lengths in order to operate at these higher frequencies, but the corresponding reduction in breakdown voltage capability with decreasing gate length limits the maximum output power of the device. There is, therefore, a trade-off between high frequency and high power performance that must be considered when designing a device for high frequency power amplification. Figure 1 can be used as a design guide to predict the breakdown voltage of a device for a given gate length.
Also studied during the present period was the microwave performance of power FET structures with 175 micron maximum finger width per cell, and airbridged source interconnects employed to combine cells up to 1100 micron total periphery. Figures 2-6 summarize the results output power versus gate periphery and gain versus frequency for device fabricated under the present program. Also included for comparison are measurements made on devices obtained from Narda Microwave Corp. and Fujitsu Laboratories.

References

1. P. Ladbrooke, to be published.
3. JSEP 5 Year Technical Report, Cornell University, Contract F49620-80-C0069.

Degrees

J.G. Tenedorio, Ph.D., May 1982
Figure 1 Plot of Breakdown Voltage (at pinchoff) as a function of gate length \(N_d = 8 \times 10^{16}/\text{cm}^3\).

- △ Ladbrooke (calculated) Ref. 1
- □ Tiwari Ref. 2
- ● This work

Figure 2 Output power at unity gain plotted against total gate width, for both 4 GHz and 6 GHz.

- ○△ This work
- ○ NARDA devices
Figure 3 Maximum available gain plotted as a function of frequency for $V_{ds} = 3 \text{ V}, 6 \text{ V}, 8 \text{ V}$, and $12 \text{ V}$.

Figure 4 Maximum available gain plotted as a function of frequency for a power structure device. ($Z = 4 \times 175 \mu\text{m} = 700 \mu\text{m}$) for $V_{ds} = 3 \text{ V}, 6 \text{ V}$, and $8 \text{ V}$. 
Figure 5  Maximum available gain plotted against log frequency for devices of Figure 4.8 at $V_{ds} = 0$ volts. (Note 6 dB/oct drop).

Figure 6  Power gain plotted against log frequency for $P_{IN} = 10$ dBm, 12 dBm, and 14 dBm at $V_{ds} = 0$ V. (Note slope is 4 to 5 dB/oct).
Task 3 USE OF MBE TAILORED PROFILES FOR GaAs POWER FET's FOR IMPROVED PERFORMANCE

L.F. Eastman, C.E.C. Wood and G. Wicks

Summary of Accomplishments

Following the success in our laboratory by Stall et al. of achieving extremely low contact resistances to GaAs \( (\rho_c < 10^{-7} \, \Omega \cdot \text{cm}^2) \), an MBE grown Ge layer, a similar approach for contacts to AlGaAs was investigated. The abrupt Ge-AlGaAs heterojunction was found to have a high specific interface resistance.

For AlAs mole fractions between 14% and 37% interface resistances were between 0.08 and 8 \( \Omega \cdot \text{cm}^2 \). These results indicate that the abrupt Ge-AlGaAs interface is not a low resistance ohmic contact to AlGaAs. However, by grading the AlGaAs to GaAs then depositing Ge, contact resistances to AlGaAs on the order of those to GaAs may be achieved.

GaAs layers, grown by MBE on superlattice buffer layers have been characterized by photoluminescence (PL) and found to be superior to those grown on AlGaAs or GaAs buffers. The superlattice buffer simultaneously alleviates the major problem of the GaAs buffer: the outdiffusion of impurities from the substrate, and that of AlGaAs buffers: structural problems which propagate into the subsequently grown GaAs.

Degrees
D. DeSimone, Ph.D., January 1982.
Publications

2. "Magnesium and Calcium Doping from Dissociative Captive Sources or 'Now You See It, Now Your Don't'", C.E.C. Wood, D. DeSimone and K. Singer, Third Workshop on MBE, Santa Barbara, CA.
Task 4  MBE MULTIPLE GaAs-Al$_x$Ga$_{1-x}$As HETEROJUNCTIONS FOR
CONFINEMENT OF ELECTRONS FOR IMPROVED FET PERFORMANCE

L.F. Eastman, C.E.C. Wood and G. Wicks

$\mu_{77}$ figures for modulation doped structures are routinely in excess of 100,000 cm$^2$/v-sec.

Annealing of modulation doped structures, necessary to achieve ion implanted self aligned FET's, was investigated. It was found that the electric field which is built into the structure causes the silicon donors in the AlGaAs to drift toward the GaAs-AlGaAs junction. When the donors reach the GaAs, the junction interdiffuses which drastically reduces the mobility of the structure. A heavily doped p-type layer added to the top of the structure inhibits the movement of the silicon donors by reversing the field in the AlGaAs layer. This allows the structures to retain their high mobility after anneals of 800°C for 10 minutes or longer.

Problems in the reproducability of the barrier heights of planar doped barriers (PDB's) were traced to impurity outdiffusion from substrates. Substrate pre-baking at $T > 700^\circ$C in $H_2$ was found to solve the problems allowing the growth of PDB layers with high yield (~ 90%) and good reproducability.

Degrees
W.I. Wang, Ph.D., January 1982
G.W. Wicks, Ph.D., August 1981
Publications


Task 5  HIGH SPEED RECEIVERS FOR OPTICAL COMMUNICATIONS

J. Ballantyne and D. K. Wagner

High Speed Detector and Amplifier for Optical Communications

A GaAs MESFET amplifier has been integrated with four different types of fast photoconductive detectors of the OPFET geometry. Fabrication processes are described which yield successful integration of the different photodetectors with the GaAs MESFET amplifiers.

The four different photoconductive detectors integrated are all of the OPFET geometry. They include small OPFETs with and without notches, and interdigitated OPFETs with and without notches. The real response of the interdigitated detectors taken with a scanning laser microscope is relatively uniform, showing they behave as expected and are suitable for receiving light from optical fibers. (See Appendix 1). Gain for the interdigitated OPFET detectors was measured at about 14 (low frequency). High-speed testing of the discrete detectors was temporarily delayed due to lack of a satisfactory low capacitance carrier. However, suitable modification of existing commercial SMA end launches proved successful. Recent results show the slower detectors without notches have response speeds on the order of 200 ps. Measurements are in progress on the much faster notched detectors, which are expected to have response times of less than 100 ps.

Standard MESFET's have been successfully integrated and quite reliably fabricated with 1 micron length gates, gate widths of 50-250 microns, and transconductances of 80-90 ms/mm. The processing sequence for the monolithic circuit consists of four steps.
First, moats are etched around transistor and detector areas using a 3:1:1 methanol :H₂O₂:H₃PO₄ etch for electrical isolation. A more conventional mesa etch was not used due to technical problems in fabricating larger clear areas in masks by e-beam lithography. The moat etch is highly successful in isolating the components, however. Ohmic contacts consisting of layers of about 500 Å of AuGeNi, 500 Å Ag, 1500 Å Au are then thermally evaporated onto the substrate and annealed at 600°C for 90 s. This second step, which in addition to the normal optical photolithography also includes a liftoff of excess metallization in acetone, provides ohmic contacts and virtually all of the required metallization. The third step consists of defining uniform 1 micron gates using a projection mask aligner, etching self-aligned notches in the transistors to lower quiescent currents, evaporating about 1000 Å of Au for the Schottky barrier gates, and performing a liftoff of the excess gate metallization. The last step is a notch etch (if desired) performed on the photoconductive detectors.

At the present time a ceramic carrier has been made incorporating 50 ohmic microstrip transmission lines. The GaAs wafers have been both successfully cleaved or alternatively sawed up (with a higher yield) to obtain individual circuits. Methods of applying DC bias to the chip so that the leads are suitably bypassed at the 5-10 GHz range is a problem which is being studied at present.

In the near future the chips will be tested electrically by injecting electrical pulses and when the biasing problems have been worked out, with optical picosecond pulses. Future work will also include noise measurements and evaluation of the system.
MOCVD Growth of GaAs and AlGaAs

In work joint with Professors Eastman and Tang, the MOCVD system for the growth of uniform and large-area thin layers of III-V compounds was completed to the first phase. The system has been used to grow state-of-the-art layers of GaAs and AlGaAs. (See Appendix 2). Mobilities exceeding 90,000 cm²/V sec at 770K are measured in layers of GaAs grown on the system, with total impurity levels well below 10¹⁵ cm⁻³ reproducibly achieved. High quality layers of AlGaAs are also grown on this system by the incorporation of a unique Ga/Sn/Al bubbler to remove unwanted O₂ from the source gas flows.

The system is being used to grow layers for high speed transistors and opto-electronic devices. Work is in progress to install In and P sources for growing optoelectronic materials in the GaInAlAsP alloy system.

Personnel


Publications and Talks


Boston, MA, June 8-10, 1981.


Optical Information Processing for Aerospace Applications

SUMMARY

We discuss considerations relevant to the monolithic integration of optical detectors, lasers, and modulators with high-speed amplifiers. Some design considerations for representative subsystems in the GaAs-AlGaAs and GaInAs-InP materials systems are described. Results of a detailed numerical design of an electro-optical birefringent filter for monolithic integration with a laser diode is described, and early experimental results on monolithic integration of broadband MESFET amplifiers with photoconductive detectors are reported.

INTRODUCTION

A number of workers have been involved in the monolithic integration of detectors and lasers with amplifiers for applications in optical communication. The work reported here is specifically aimed at circuits and subsystems suitable for use in very-high data rate applications. The OFET class of photoconductive detectors in III-V compounds shows picosecond response time coupled with internal gain and low noise. In order to realize the potential of these detectors in a practical system, monolithic integration with high-speed, low-noise preamplifiers is probably a necessity. In addition, there is a need for integration of laser diodes with high-speed amplifiers in order that complete opto-electronic systems can be constructed.

Frequency tunable lasers are useful for radio communication, for frequency multiplexed systems, and offer outstanding potential for very-high data rate transmission. These may be constructed by suitable combinations of gain, birefringent and electro-optical components in the laser cavity.

Two materials systems seem especially attractive for monolithic integration of opto-electronic subsystems. They are the GaAs-AlGaAs and GaInAs-InP heterostructure systems. The first system is useful because well-characterized opto-electronic components and amplifiers have been constructed in this system, and much is known about the materials problems which must be overcome to construct successful subsystems. The GaInAs-InP heterostructure system, lattice-matched to InP substrates, is interesting because of its potential application for longer wavelength communications, where optical fibers show minimum dispersion. A further reason for interest in this system is the very high electron saturation

*Portions of this work were supported by NASA Langley Research Center, The National Science Foundation, and the Joint Services Electronics Program at Cornell University. Facilities of the National Research and Resource Facility for Submicron Structures and the Materials Science Center at Cornell University were employed in this work.
velocity, which was shown to be the greatest for any of the GaInAsP quaternaries grown lattice-matched to InP. In previous work we showed that the electron saturation velocity in GaInAs is nearly double that of GaAs for comparable carrier densities at room temperature. This enables one to construct photoconductive detectors with higher internal gain, and transistors with higher G, and speed in the GaAs system than in the conventional InP system. A drawback to the GaAs-InP system is that unsoled material problems must be overcome to construct successful monolithic opto-electronic circuits, and the individual devices are much less developed in this materials system, particularly the transistor technology.

SOME DESIGN CONSIDERATIONS FOR MONOLITHIC OPTO-ELECTRONIC SUBSYSTEMS

Monolithic integration of optical and amplifying devices requires semi-insulating substrates if the well-developed M-device technology is to be utilized for amplifiers. Such substrates are readily available in both GaAs and InP; however, problems immediately arise for MESFET type transistors on InP substrates. From initial considerations, it might seem that a simple GaInAs-InP heterostructure interface would be useless for both optical and electrical confinement, and would be suitable for construction of M-structures. One of the problems with such interfaces grown by MBE is shown in Fig. 1, where it is seen that in an abrupt GaInAs-InP interface substantial leakage currents can flow which prevent construction of good transistors. In these MBS grown layers the interfacial current was linked with the growth process for the interface, which may result in an INAP interfacial layer with poor electrical characteristics. These problems were initially solved by incorporating Al into the system to provide an AlGaAs interfacial layer between the GaInAs active region and the InP substrate.

While this approach solved problems with leakage current in transistors, it raises further problems for laser diodes. A schematic diagram of a proposed heterostructure system for monolithically integrated opto-electronic circuits on indium phosphide substrates is shown in Fig. 2. The structure indicated schematically has the potential for producing good transistors for amplifiers, good optical properties. The second layer is similar to those of the MESFETs, which are that one can be able to construct low leakage Schottky barrier gates on active layers which are thin enough to be pinched off at a reasonable voltage, and that the structure show no excessive leakage currents through interfaces. The structure shown in Fig. 2 meets these requirements. The AlGaAs layer under the gate serves to make a good Schottky barrier as was previously demonstrated. Fig. 2 is schematic in the sense that details of the above structures and Schottky barriers are not shown. Under the contacts, the undoped upper layers must either be removed, doped, or consumed in the contact allowing processes. There are various approaches for doing these steps, the details of which are not discussed here. The requirement for pinching of the active layer at a reasonable gate voltage means that the thickness of the layer must be 0.2 microns or below for a doping of 10^7 cm^-3, or that the doping must be reduced for thicker active layers.

The AlGaAs layer between the substrate and active layer serves to reduce the leakage currents in the transistor to reasonable values. It also serves to provide excellent carrier and optical mode confinement for the laser structure. One advantage of this material system for the InGaAsP laser structure shown is that the cladding layers can be easily made semi-insulating, providing excellent current confinement in the TJS laser diode. Another advantage of the structure shown for the TJS laser is that it incorporates two-dimensional index guiding, which should give extremely good mode confinement. The parallel metal stripes on the surface serve as a slot waveguide to confine the laser mode in the direction parallel to the surface. We have done extensive calculations, and modeling on various geometries of these slot waveguides, some of the results of which are included in the following section.

The problem with the AlGaAs interlayer is that in cases studied to date, it reduces the quality (in terms of luminescence linewidth and efficiency) of the GaAs active layer. However other workers have shown that this is not a fatal limitation. Substantial material work remains to be done to solve this problem.

SLOT WAVEGUIDES FOR MONOLITHIC INTEGRATION

The slot waveguide configuration shown schematically in Fig. 2 appears to be extremely promising for monolithic integration in InGaAsP compounds. The reasons for this are the experimental demonstration of stable guiding with very low threshold injection lasers at the AlGaAs heterostructure system, the compatibility with TJS lasers as shown in Fig. 2, and the obvious compatibility with electro-optic devices employing planar surface electrodes.

We have done extensive numerical calculations on the properties of slot waveguides in various geometries, and confirm that excellent low-loss waveguides can be made in various InGaAsP compound heterostructure systems. These waveguides contain an inherent component, the electro-optic effects necessary for inducing electro-optic effects, for enticing InGaAsP. We have also investigated the geometry that is compatible with optical pumping, which is convenient for fundamental investigations. The basic geometry of the slot waveguide system we analyzed is shown in Fig. 3. The long direction of the slot is oriented along a <110> direction so that electric fields applied by the electrodes are along the <110> directions as required for usable electro-optic devices. The various guide geometries we analyzed are shown in Fig. 4. These waveguides are not only useful to provide a passive guide for a laser structure, but are also suitable for combining an electro-optically active device within a laser cavity, such as a Q-switch or a tunable birefringent filter (which will provide a frequency tunable diode laser).

We previously demonstrated the feasibility for rapid electro-optic frequency tuning of diode laser by edge pinning, and are now constructing integrated electro-optic systems of this system. While the simple slot waveguide geometry shown as Type I can provide good guiding and low enough loss for a laser cavity, additional considerations arise when the system is the simple structure. We have previously demonstrated the feasibility for rapid electro-optic frequency tuning of diode laser by edge pinning, and are now constructing integrated electro-optic systems of this system. We have previously demonstrated the feasibility for rapid 2D electro-optic frequency tuning of diode laser by edge pinning, and are now constructing integrated electro-optic systems of this system. We have previously demonstrated the feasibility for rapid 2D electro-optic frequency tuning of diode laser by edge pinning, and are now constructing integrated electro-optic systems of this system.
guide appears to have released fabrication tolerances as compared to Type I. The fabrication tolerances are very sensitive functions of the Aluminum content in the cladding layers. Decreasing Al content relaxes these tolerances. The mode confinement for a representative Type VI guide is shown in Fig. 8 and the electro-optic coupling efficiency for TE to TM modes is shown in Fig. 9. As shown in Fig. 5, the smaller waveguide types I-IV show a great difference between loss for TE and TM modes. Such a structure would be particularly useful for Q-switching a diode laser in a monolithically integrated configuration.

INTEGRATED SUBSYSTEMS

In Figs. 10 and 11 we show the circuit diagram and photograph of a finished circuit of a monolithically integrated OPFET detector and three stage wide bandwidth amplifier. This system has been designed to give a voltage gain of 7, a power gain of 250 (over 23 dB), and a frequency response exceeding 5 GHz. One unique feature of this chip is the inclusion of a new type of interdigitated OPFET detector shown in Fig. 12. The aerial response of this detector is shown in Fig. 13 which is the photocurrent due to a HeNe laser spot, raster scanned over the detector. The low frequency gain measured in this experiment was 14, which is most likely a factor of 2 larger than would be measured at high speeds. Such high speed measurements are now in progress. In Figs. 14 and 15 we show the circuit diagram and layout for an integrated laser/driver-transistor circuit being fabricated in the materials structure shown in Fig. 2. The two small FETs connected in series on the gate of the driver transistor provide a convenient, area-and-power-efficient method for setting the bias level on the laser diode.

CONCLUSIONS

In this paper we have identified what we consider to be viable approaches for the monolithic integration of detectors, lasers, amplifiers, and electro-optic components in two material systems which operate in quite different wavelength regions. For the first time, we have carried out extensive numerical calculations on slot waveguide structures in III-V compounds, and have computed parameters which are useful for the design of guides for electro-optic components in the system. The results of these computations give information on the confinement of various geometry guides, the attenuation and the electro-optic coupling parameters of these guides. Finally, we have fabricated the most complex monolithic integrated opto-electronic circuits so far reported in III-V compounds, and have verified their performance at low frequency. We expect these circuits to give good operation at gigahertz speeds.

REFERENCES


Fig. 5. Results for modes in Type I waveguide.

a) Attenuation vs. clad thickness for several electrode spacings.

b) Mode confinement.

c) Guide Thickness (mm)
d) Clad Thickness (mm)

Note: Slab-waveguide geometries for which analysis was carried out, along with basic models used for two classes of guides.
Fig. 6 Phase difference, \( \Delta \phi \), between TE and TM modes in Type V waveguide. 
\( \Delta \phi \) is zero for a 2.5 \( \mu \)m wide guide and an oxide clad of 0.04 \( \mu \)m. 
Note sensitivity to fabrication tolerances.

Fig. 7 Phase difference, \( \Delta \phi \), between TE and TM modes in Type VI waveguide: 
Oxide and AlGa. As thickness are \( d \) and \( b \) respectively. Case illustrated is for \( x = 0.05 \). Note large tolerances in \( d, b \), and width to allow \( \Delta \phi \) to be nearly zero.

Fig. 8 Mode confinement for a representative Type VI waveguide. Amplitudes are normalized.

Fig. 9 Efficiency for coupling TE to TM modes in Type VI guides via the electro-optic effect.
Fig. 10. Circuit diagram of a semiconductively integrated receiver combining an OPEF with a 5-stage amplifier.

Fig. 11. Photograph of receiver of Fig. 10. Gates are missing in this photograph.
Fig. 13  Spatial response of detector in Fig. 12. Increasing response is downward. Response in lower left is an artifact due to light reflecting from bonding wire.

Fig. 14  Circuit diagram for an integrated laser-driver circuit being constructed in materials systems of Fig. 2.

Fig. 15  Layout of circuit of Fig. 14.
Characterization of High-Purity GaAs Grown by Low-Pressure OMPE


Abstract: High-purity epitaxial films of GaAs have been grown by OMPE under a reduced hydrogen pressure. These films exhibit fine exciton structure in low-temperature photoluminescence (PL) spectra and high electron mobilities (\(90,000\) cm\(^2\)/Vs) at 77K. The dominant residual impurities in undoped films have been determined by PL and far-infrared photo-luminescence spectroscopy for the acceptors and donors, respectively. The effects of the growth temperature, As\(_2\):Ga mole ratio, arsenic prepyrolysis, and in-situ etching have been investigated. Carbon-free films have been obtained with the starting sources trimethylgallium and arsenic under suitable growth conditions. Finally, results on the interface abruptness of selenium-doped films grown at low pressure with high gas velocities are discussed.

1. Introduction

Organometallic vapor-phase epitaxy (OMPE) has received an increasing amount of attention as a source for epitaxial layers of III-V compound semiconductors since its introduction by Manasevit in 1965 [1]. A variety of device structures obtained by OMPE spanning both microwave and optical applications has been realized by workers on III-V compound semiconductor IC systems such as GaAs/AlGaAs [2] and InP/GaAs or GaInAsP [3].

Recently, the OMPE process has been successfully used for the epilaxial growth of the active materials under reduced hydrogen pressure [4,5]. The use of reduced pressure in OMPE has the potential advantages of better uniformity in thickness and doping, reduced transients when changing aperture levels and alloy compositions, and the reduction of parasitic reactions encountered in premixing reactants prior to their reaching the deposition zone [4]. Devices utilizing interfaces of a few nanometers, such as quantum well lasers and modulation-doped FET's, have recently been realized using OMPE [7,8,9]. In addition, OMPE has potential for the growth of epitaxial layers with sufficient uniformity for optical and microwave integrated circuits.

In this paper, we report the optimization of the growth of high-purity GaAs at a reduced hydrogen pressure. The conclusions resulting from this investigation are applicable to multilayer device structures incorporating GaAs and other III-V compounds. For example, we have determined that by using in-situ etching and a high As\(_2\):Ga mole ratio, the optical quality of epitaxial GaAs at a given growth temperature can be improved substantially.

2. Experimental

The epitaxial growth apparatus is similar in design to low-pressure reactors used by Duchemin et. al. for GaAs and InP growth with the following exceptions:

(i) During operation at low pressure, no flow restrictions are present between the sources and the reactor cell. A hydrogen manifold and all gas sources (i.e. AsH\(_3\) and dopants) are maintained at 4 psig. The gas expands as it is pumped and is dropped across the mass flow controllers (MFC) to the growth pressure (760 Torr for all experiments except in-situ etching). The trimethylgallium (TMG) bubbler is downstream from its MFC which results in a reduced pressure (~760 Torr) over the liquid in the bubbler. This increases the TMG transport in the hydrogen carrier gas by approximately one order of magnitude compared to the same mass flow at atmospheric pressure.

(ii) Between growth experiments provision has been made to bake the reactor cell with a furnace to a temperature of 900°C at atmospheric pressure for cleaning. Any poly GaAs material left after baking is removed by introducing a small amount of HCl (~10%vol.) into the hot cell and is condensed on a water-cooled baffle near the exhaust. This procedure avoids the problems of disassembling the reactor cell for cleaning.

The substrates used in all experiments were (100) Cr-doped. In addition, undoped LEC semi-insulating substrates were used in in-situ etching experiments. The wafers were prepared by: degreasing in organic solvents, chemically etching in 5:1:1 (H\(_3\)PO\(_4\)/H\(_2\)SO\(_4\)/H\(_2\)O) for 15 minutes, treating in warm DI H\(_2\)O for 30 min for a native oxide growth, and sumermering in 3:1 (HCl:H\(_2\)O) for 5 min to remove the native oxide. Loading was accomplished in a dry N\(_2\) ambient. Experiments were carried out consisting of a preanneal in arsine, followed by etching in HCl and arsine (when etching was used), then GaAs epitaxial growth. The hydrogen carrier flow throughout each of this sequence was maintained at 7 slm. During the preanneal a flow of approximately 6 sec of arsenic was used to prevent any surface decomposition of the GaAs substrate. The 15 min preanneals were done at atmospheric pressure at a substrate temperature of 650°C for layers grown without the in-situ etch and 900°C for layers grown with an In-situ etch. When used, the In-situ etching followed the preanneal at 900°C and was carried out at atmospheric pressure. The etch was done by adding 2 sec of HCl gas into the reactor chamber and resulted in an etch rate of 2000 Å/min. Typically 2 μm of surface was removed prior to the growth. Following the preanneal and the etching step, the reactor pressure was decreased to 760 Torr, the substrate temperature and asine flow were adjusted and stabilized, and the TMG was introduced into the reactor to initiate the GaAs growth. The TMG temperature was maintained at ~140°C and the hydrogen flow through the bubbler was 1.5 sec for all experiments. These conditions produced a growth rate of approximately 1000 Å/min with a uniformity across a 2" wafer of ~3%.

Experiments were done to determine the effect on film properties of in-situ etching, arsenic cracking, substrate temperature during growth, and V:III ratio. The arsenic cracking was done in a hot-wall silica tube heated to a temperature of 750°C. The substrate temperature range investigated was from 500 to 700°C. The V/III ratio was varied from 5:1 to 100:1 by changing the arsenic flow. Changes in these growth parameters had little effect on the growth rate. The epitaxial film thicknesses were typically around 10 μm for all the characterization studies.
The carrier concentrations were evaluated by capacitance-voltage and Hall measurements. Hall mobility data were taken on undoped films at 300 and 77K in a magnetic field of 24G. The optical quality of the GaAs epilayer was assessed by high-resolution (2AX) low-temperature (1K) photoluminescence measurements. Photoluminescence measurements at 1K were performed to determine the dominant residual donor and acceptor impurities. Far-infrared photo-ionization data were taken on an undoped film grown under optimum conditions in order to determine the dominant residual donor and acceptor impurities. The deep levels in the epilayer and their concentrations were evaluated by DLTS experiments. Finally, the interface abruptness between doped regions was evaluated from C-V data at room temperature and compared to the expected Debye tails calculated for the doping levels obtained.

3. Results and Discussion

In order to reduce the contamination from the GaAs substrate surface from chemical cleaning and impurity redistribution effects, HCl in situ etching was used prior to epilayer growth. Without in situ etching, substantial concentrations of Fe, Mg, Gz, and Mn have been observed at the interfaces of epilayer grown by OMVPE on semi-insulating substrates.[10] With etching, the build up of carbon at the growth interface has been reduced to non-detectable limits, as observed by an SIMS analysis.[11] Figure 1 illustrates the effects of a preanneal and in situ etching on GaAs semi-insulating substrates used in this study. The temperature of 300°C was chosen for each to ensure a mass-transport-limited process which has previously been shown to eliminate surface faceting due to a kinetically-controlled reaction.[12]

Near the surface, and the PL intensity is 20 times that of the undoped GaAs substrate. The manganese concentration in the Bridge pattern material was not sufficient to thermally convert the surface. Carbon is also present in the Hall and etching step after the annealing and etching but its PL signature relative to the bound exciton peaks is reduced after the etching step. This result is useful in interpreting the origin of carbon observed in the PL of the epilayer to be discussed later.

As reported by Dogrus et al.,[13] a much higher arsenic mole fraction is required in the growth ambient for reduced-pressure growth than is normally required at atmospheric pressure. Because high V:III ratios make inefficient use of the AsH3 source, we have investigated in detail the effects of V:III ratio on electrical and optical properties of undoped films at relatively low ratios for which it is practical to operate the reactor. Also we have determined that the V:III ratio can be reduced substantially when the AsH3 is prepyrolyzed.

Hall data were taken on films grown at 650°C under various V:III ratios, and film thicknesses. The results are shown in Table I. The best films were obtained for V:III ratios near 70 and have 77K mobilities of 93,000 cm²/Vs. Little dependence on the film thickness is observed as demonstrated by the two films grown with V:III = 72. However, the thinner film (4.1μm) did not conduct at room temperature. As indicated by Table I, as the V:III ratio decreases, the total number of shallow impurities (N₂H₄) increases faster than the net (N₂H₄), meaning the concentration of shallow acceptors increases with decreasing V:III ratio.

Table I. Hall data on undoped GaAs films grown at 650°C

<table>
<thead>
<tr>
<th>V:III Conductivity Thickness (μm)</th>
<th>C-V Mobility (cm²/Vs)</th>
<th>Carrier Concentration (cm⁻³)</th>
<th>Net</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>72 n</td>
<td>11.5 8000 93,000</td>
<td>2(10⁺⁴) 7(10⁺⁴)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>72 n</td>
<td>-4.1 88,000</td>
<td>2(10⁺⁴) 7(10⁺⁴)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55 n</td>
<td>7.8 7300 61,000</td>
<td>2(10⁺⁴) 2(10⁺⁴)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>36 n</td>
<td>12.0 6500 37,000</td>
<td>5(10⁺⁴) 4(10⁺⁴)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24 p</td>
<td>6.5 340 3.200</td>
<td>1(10⁺⁴)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 p</td>
<td>21.0 300 3.170</td>
<td>7(10⁺⁴)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Data did not conduct at 300K.

These results have been identified by PL as carbon and zinc. Their relative concentrations are strongly dependent on the V:III ratio as indicated by Figs. 2a and 2b. This behavior is expected since at higher V:III ratio, i.e. arsenic-rich conditions, the incorporation of carbon on an arsenic site is less likely, due to the higher arrival rate of arsenic at the growth interface. Similarly, the incorporation of zinc on a gallium site is favorable under arsenic-rich conditions. However, from the Hall data it was determined that the total acceptors, carbon and zinc, decrease with higher V:III ratios indicating that carbon is the dominant acceptor species grown under lower V:III ratios and that its concentration decreases with increasing V:III ratio. As a result, by using sufficiently high V:III ratios we have obtained carbon-free films for the first time with the starting sources TMC and Arsenic. These photoluminescence spectra for these films are shown in Fig. 2b for a V:III ratio of 120 and in-situ spectra. The PL spectra have been observed in films grown under similar conditions with triethylgallium (TEG) and Arsenic (14).
As shown in Fig. 3b, at low V:III ratios where the carbon concentrations are the largest, the exciton-bound-to-carbon acceptor transition dominates the PL spectrum. At the other extrema at high V:III ratios, where little or no carbon is detectable by PL, the exciton-bound-to-donor transitions dominate the PL spectrum. Other transitions observed in the spectrum agree labeled in a similar fashion as was done by Bhat et al., in earlier work [14].

Fig. 3(a) Free exciton PL efficiency vs V:III ratio of undoped GaAs films. Excitation wavelength was 6421Å and illumination intensity was 25 mW/cm². (b) PL data on undoped films at 3K. (Without in-situ etching.)
The residual donors were identified on an undoped film grown with a V:III ratio of 72 and a growth temperature of 650°C by far-infrared donor spectroscopy [15]. The results are shown in Fig. 4. The spectrum is dominated by the "Xy" center which has been observed in all OMPE GAAs. Silicon donors are also present in undoped layers as shown. Attempts to identify the "Xy" center using transmission electron microscopy [16] suggest that it may be due to the presence of Ga donors. However, no Ga acceptors or silicon acceptors have been observed in the PL spectrum. The silicon acceptors may be masked by the presence of larger quantities of In, but with Ge, which occupies both Ga and As sites, it appears that the acceptor should be detectable with PL at relatively large concentrations of the donor species are present. Some question as to the exact species responsible for the Xy center and its origin still remains. Also indicated by the figure, common impurities in OMPE GAAs such as Pb, Sn and S are undetectable in these films.

The characterization of the GAs films for interface abruptness and deep level contents were accomplished on films doped with Se using hydrogen selenide as a source. Several films were prepared at different V:III mole ratios with an intentional doping level of 5(10^16) cm^-3 for the DLTS experiments. Using optical stimulation, no hole traps were detectable by DLTS experiments. The sensitivity of the DLTS measurement was 5(10^12) cm^-3 for trap concentrations. With electrical stimulation, the presence of "EL2" was detected in epitaxial layers grown on semi-insulating or n-type substrates. As observed previously[17], the concentration of EL2 increases with the V:III mole ratio. For example, our films grown at 650°C with V:III mole ratios of 24, 35 and 72 have an estimated concentration of approximately 5(10^14), 2.1(10^15), and 4(10^15) cm^-3 respectively. These EL2 concentrations are comparable to the state of the art achieved by OMPE at atmospheric pressure[17]. The EL2 concentration appears to be more sensitive to the growth substrate temperature than the V:III mole ratio. For example, increasing the substrate temperature from 600 to 700°C at a V:III mole ratio of 55, the concentration of EL2 increases almost one order of magnitude.

A primary consideration for the use of low-pressure in OMPE is the interface abruptness which can be achieved by variations in different doping levels. Figures 5a and 5b illustrate the interface abruptness obtained for layers grown without stopping the growth as measured by C-V measurements at 300K. In Fig. 5a, the measured Debye tail at the n-n' interface corresponds closely to the calculated value of 500Å, suggesting that the interface region is less than 100Å. In Fig. 5b, a C-V profile of a repetitive structure consisting of 500Å of alternating doped and undoped regions is shown.

4. Conclusions

The growth of OMPE by OMPE at reduced pressure has been optimized for the best structural and electrical properties. Fine structure obtained at low-temperature PL is obtained on samples grown over the entire range of substrate temperatures and V:III mole ratios at reduced pressure. Best mobilities and lowest background carrier concentrations were obtained on films grown at 650°C with a V:III mole ratio of 72. Deep level concentrations in these films are below 10^14 cm^-3 when the substrate temperature is less than 650°C. Arsenic cracking at 750°C reduces by as much as 35% the amount of arsenic required for optimum film quality. Finally, in-situ etching using HCl has significantly reduced the carbon content in the films and improved PL efficiency. Using in-situ etching, carbon free layers are reproducibly obtained with the starting sources both Se and arsenic.

Acknowledgments

Support for the work was provided by the Joint Services under Contract F49620-81-C-0082 and support for one of the authors (JRS) was provided by DSOE General Electric Co., Syracuse, NY.

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Cryst. Growth 55 10

Symp. GaAs and Related Comp. Japan 101.

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Growth 55 164
Summary of Accomplishments

I. The ultimate speeds of semiconductor electronic and optic devices depend upon the relaxation time of hot electrons in the conduction band and the transit time of ballistic electrons over submicron distances in semiconductors. These are in the sub-picosecond ($10^{-13}$ to $10^{-12}$ sec) range. Thus, to determine these time constants, a time resolution less than 0.1 psec ($10^{-13}$ sec) is required in the measurements. In a related project sponsored mainly by the National Science Foundation, we have recently developed a technique (1-4) that allows one to measure certain optical processes in liquids and solids down to 60 femtoseconds ($6x10^{-14}$ sec), which is more than an order of magnitude faster than any optical phenomena previously measured. Work is under way to extend such experiments to semiconductor electronic and optic devices. This work is carried out partly under the auspices of the JSEP program.

II. Luminescence decay and injected carrier lifetime in the high injection region of AlGaAs laser diodes have been measured (5). Using an optical gating technique, decays in the high injection region of laser diodes following current pulse excitation were measured with a 100 ps time resolution. The observed luminescence decay is shown to be strongly affected by the gain in the active region. It is also shown that both monomolecular and bimolecular carrier recombination must be considered. A model has been developed
that takes these effects into account and is shown to accurately
describe the steady-state and decay spontaneous emission intensities
from laser diodes. A procedure is outlined for determining the
necessary device and material parameters for interpreting laser diode
characteristics.

III. In a related project, a nondestructive optical technique
that is accurate and direct for measuring the diffusion profiles of
photo-generated electrons and holes in semiconductors has been
developed. The time evolution of the diffusion profile of electrons
and holes in GaAs has been measured for the first time with a time
resolution of 0.5 nsec. The results are being prepared for
publication. Combination of this type of measurements with the
optical-gating technique described above (II) will allow one to study
the relaxation of hot electrons in semiconductors and thus help to
determine the ultimate speeds of response of semiconductor devices.

IV. Coherent optical interference effects in external-cavity
semiconductor lasers have been observed and interpreted. A
broadening of the apparent linewidth of semiconductor laser modes with
external optical feedback is observed. This is shown to be due to
the coherent nature of the feedback and multiple reflections in the
external cavity. A theory for the steady-state behavior of the
external-cavity semiconductor laser taking into account such coherent
optical effects is developed. The inclusion of these effects is also
important in the interpretation of the threshold data of such lasers.

V. Pulses on the order of 6-8 psec are obtained in an actively
mode-locked external-cavity antireflection (AR) coated semiconductor
laser. We also report the mode-locking of a ring-cavity
References


3. "Observation of light induced refractive index change in molecular liquids by femtosecond interferometry", C.L. Tang and J-M. Halbout, invited talk, XIIth International Conference on Quantum Electronics, Munich, Germany (June, 1982).


Task 7  CARRIER DYNAMICS IN COMPOUND SEMICONDUCTORS STUDIED WITH PICOSECOND OPTICAL EXCITATION

G. J. Wolga

This reporting period was the first year in which we had JSEP support. The primary objectives for the period were to set up laboratory facilities for generating tunable, picosecond optical pulses in the red - near infrared spectral region corresponding to the bandgaps of common compound semiconductor materials, to set up diagnostic facilities for measuring the special pulse duration and characterizing the shape of the pulse, and to commence setting up the first experiments. A synchronously mode locked, tunable dye laser pumped by a mode locked Krypton ion laser was purchased. After some delay in receiving the laser system, we were limited in operating it until several months had passed because of inadequate electrical service in the laboratory. Subsequently, this problem was eliminated and the laser has been operating very satisfactorily. As delivered and installed, the dye laser was producing 1-1.5 picosecond pulses at an 82 MHz pulse repetition rate in the 7000 Å region. We have obtained continuous tunability over a 900 Å range with a single dye. An additional limitation during the first year was that essentially the entire budget was allocated to procurement of the laser system and thus no graduate students were supported. Two students did associate themselves with the project and are now receiving support from JSEP funds.

To measure the dye laser pulse duration we designed an optical Michelson interferometer with calibrated variable spacing in one arm.
This apparatus permits us to measure optical pulse duration by observing the autocorrelation between an optical pulse and a time delayed optical pulse obtained from it. We have designed the interferometer with both a sinusoidal time delay (using an audio speaker cone to provide the motion) of variable amplitude for rough measurements and tuning up of the laser, and with calibrated linear time delay (using a dc servo motor driving a precision translation stage) for precise measurements. The interferometer functions properly and has been incorporated as a permanent part of the laser apparatus.

Experimental studies are planned in two areas. The first involves the use of photoexcited fast photoconductors coupled by strip lines as pulsed current generators and as sampling gates to study charge carrier relaxation in compound semiconductors. The basic structure involves a strip line deposited on a semiconductor film with a ground plane beneath. Gaps in the strip line form fast photoconductors when radiation damaged. The photoconductors are illuminated with pico second pulses generating electron-hole pairs causing conduction across the gaps. By delaying the optical excitation of one gap with respect to the other, the delayed gap acts as a sampling gate permitting autocorrelation of the current pulse to be accomplished. The detected autocorrelation pulse shape and width is a function of pulse propagation on the strip line and can be analyzed to characterize the material properties of the strip line. As described above, fast photoconductors illuminated with pico second optical pulses form the building blocks (pulse generators and sampling gate) for pico second electronic systems. We plan to extend
these techniques to the study of new materials, more complex circuits, and to the development of a measurement system for the characterization of ultrahigh speed electronic devices.

To date our progress in this area includes the development of suitable fabrication techniques for microstrip transmission lines with micron size gaps. The substrate preparation is done with a two step lithography-lift off process. High quality 11 micron wide transmission lines with 3 micron gaps have been fabricated and mounted in a versatile substrate fixture. The optical components required to focus one or more beams with variable time delay in at least one beam path have been assembled. The present configuration is suitable for device measurement via autocorrelation techniques. The adjustable path length can be adjusted with 1 micron precision. A semiinsulating InP substrate with 11 micron wide microstrip and a 3 micron gap has been tested. InP was chosen because it was believed to have very fast electron relaxation without additional processing. The response of the gap to a 3 psec, 1 n joule pulse has been directly measured with a 24 psec resolution sampling oscilloscope. We observed a scope limited (< 50 psec) rise time and a much longer exponential decay. The decay indicated that our fixture requires some improvement and we are redesigning it. A two gap transmission line structure is currently under investigation with the goal of initiating autocorrelation studies.

The second area of work involves picosecond optical excitation of compound semiconductor materials across the bandgap and observation of luminescent decay. We are setting up a low temperature optical device to hold the sample with both direct
observation of the luminescence and the capability for autocorrelation measurements. Initial experiments will include discrimination of the hot electron tail in photoluminescence, and observation of bandedge shifts under high power excitation. We are also planning a study of variation in luminescence as the optical excitation promotes electrons below and above the upper valley in Gats.
Task 8  ADVANCED DESIGN TECHNIQUES FOR MICROWAVE GaAs FET AMPLIFIERS

W. H. Ku

Objectives

The primary objectives of this research program are to develop advanced and integrated analytical and computer-aided design (CAD) techniques for the synthesis and design of microwave GaAs MESFET amplifiers leading to monolithic microwave integrated circuits (MMICs). A secondary objective of this research program is to fabricate GaAs MESFETs and circuits in microstrip and monolithic realizations using both low-noise and high-power submicron gate-length MESFETs to verify the integrated design approach developed in the main portion of this JSEP program.

Progress (or Results)

Significant progress was made during the year in both theoretical and experimental work on the sub-half-micron single-gate and dual-gate GaAs MESFETs and amplifiers. Using optical lithography, sub-half-micron GaAs MESFETs have been successfully designed and fabricated. 0.2 micron length mushroom gate GaAs MESFETs are fabricated using a new single-level photolithographic techniques. Measured gate resistance from this test device was 6.1 Ω/mm gate width which is the lowest value ever reported for gates of equal length. Using this technique, GaAs single-gate and dual-gate MESFETs with 0.3 microns long mushroom gates have been fabricated. At 18 GHz, maximum available gain of 9.5 dB in the single-gate FET and maximum stable gain of 19.5 dB in the dual-gate FET have been measured.
In the areas of GaAs MESFET amplifier design, we have completed the development of large-signal broadband amplifier design techniques resulting in the successful fabrication of two medium-power ultrawideband amplifiers in microstrip. These amplifiers cover 2-8 GHz and 2-10 GHz frequency bands and the experimental results verify the computer-aided design techniques involving broadband large-signal characterizations of the FETs. During this reporting period we have initiated the design of MMIC broadband amplifiers using the APPLICON in the Submicron Facility at Cornell. The submicron gate-length FETs will be fabricated using the optical lithography techniques.

Based on the sub-half-micron GaAs MESFETs developed at Cornell University, we have also developed new design techniques for the design of direct-coupled feedback amplifiers and distributed amplifiers. New computer-aided synthesis and design programs are being developed which will incorporate both lumped and distributed circuit elements and nonlinear models of the active devices. Specific applications for these new programs include the design of mixers and monolithic power amplifiers.

Publications


Task 9  WIDE BAND CIRCUITS AND SYSTEMS

H. J. Carlin

General

The research under this task has been primarily concerned with two basic applications of circuit techniques. The first concerns the fundamental limitations on broad band equalizers plus the use of computer aided design (CAD) techniques to obtain optimum equalizers within these constraints. Particularly emphasized are the implementation of the general methods for the design of microwave FET amplifiers.

The second topic is concerned with a new approach to dispersion analysis in wide band dielectric waveguide (e.g., graded index dielectric guide) using distributed parameter circuit modeling.

Wideband Equalization (H.J. Carlin and B.S. Yarman)

As a consequence of the Ph.D. research of Siddik Yarman under this contract we have obtained a new and general analytic gain-bandwidth theory for the double matching problem. This concerns the case where a complex source feeds a complex load and is basic for the design of interstage equalizers in broadband amplifiers. We have implemented certain aspects of the double matching problem into a "Real Frequency" CAD procedure which avoids many of the difficulties inherent in the implementation of the analytic theory.

In connection with this research a basic paper has been accepted for publication by the CAS Trans of IEEE entitled "The Double Matching Problem: Analytic and Real Frequency Solutions". We believe this paper represents a breakthrough in that a simple and complete
theory of the difficult wideband double matching problem has been delineated. Furthermore our Real Frequency procedure of single matching has been extended to the double matching problem resulting in a viable CAD method for obtaining practical interstage equalizer designs.

A version of this CAD method applied to multistage microwave FET amplifiers was presented at the May 1982, IEEE MTT Symposium in Dallas. Finally an IEEE MTT Trans paper entitled "A Simplified Real Frequency Technique Applied to Broadband Multistage Microwave Amplifiers" by B. S. Yarman and H. J. Carlin has been accepted for publication.


A new and simple network approach for computing the dispersion characteristics of multi-step and continuous graded index dielectric slab waveguide has been studied. The analysis is performed from an electromagnetic wave and circuit theoretic point of view. Thus, compared to a ray optic approach, a somewhat different perspective as to the physical mechanisms underlying the phenomenon of improved dispersion characteristics are obtained. The transverse geometry of the slab is modeled using a cascade transmission line circuit, each line having a characteristic impedance which is frequency dependent. Circuit analysis of this cascade directly yields the eigenvalue equation of transverse resonance analysis. The transmission line system in fact emulates the performance of the actual graded index structure by exhibiting a terminal plane on one side of which the lines propagate and beyond which they are cut off. The location of
this plane depends on the spatial distribution of dielectric constants, the free space wave number, and the mode in question. Indeed, in this model it is the existence of this transverse cutoff which gives the graded index slab its desirable dispersive properties. The relatively poor dispersion characteristics of the uniform dielectric slab can be attributed to the abrupt step discontinuity at the air/core interface. In the graded index case, an evanescent section of lines existing between the propagating lines and air provide shielding which in effect prevents the propagating section of lines from "seeing" the abrupt dielectric discontinuity at the air/dielectric interface. The propagating portion of the line system on the other hand functions like an impedance matching transformer. The exact electromagnetic field solution for the graded index slab with dielectric permittivity varying as $1-x^2$ is given by confluent hypergeometric functions. Computational difficulties arise for such functions in a frequency range of interest (specifically, a normalized frequency of $K_0d = \omega \sqrt{\mu_0\varepsilon_0}d = 100$ which corresponds to an operating wavelength of approximately 1000 nm for a typical guidewidth of $d = 15 \mu$). The transmission line circuit model that we are investigating yields an excellent approximation to the exact structure for only a 10-line cascade. The table below compares the deviation from asymptotic group delay $\tau_g (= dB/dKo)$ with $Ko = 20$, and $\frac{\varepsilon}{\varepsilon_0} = 2.45$. At this frequency the exact solution is "well behaved" numerically and a comparison is readily made for the first five TE symmetric modes as below (in nanoseconds/meter)
At a typical operating frequency of \( K_0 = 100 \) (normalized) the deviation from asymptotic group delay for the first five TE symmetric modes via a 10-line model are (in nanoseconds per meter)

<table>
<thead>
<tr>
<th>Mode</th>
<th>( t_g - \sqrt{\varepsilon_m/\varepsilon_0} )</th>
<th>( t_g - \sqrt{\varepsilon_m/\varepsilon_0} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.129 x 10^{-3}</td>
<td>1.676 x 10^{-3}</td>
</tr>
<tr>
<td>2</td>
<td>34.37 x 10^{-3}</td>
<td>34.83 x 10^{-3}</td>
</tr>
<tr>
<td>3</td>
<td>125.9 x 10^{-3}</td>
<td>127.2 x 10^{-3}</td>
</tr>
<tr>
<td>4</td>
<td>277.3 x 10^{-3}</td>
<td>278.5 x 10^{-3}</td>
</tr>
<tr>
<td>5</td>
<td>499.7 x 10^{-3}</td>
<td>501.0 x 10^{-3}</td>
</tr>
</tbody>
</table>

The intrinsically simple form of the cascade allows easy computation of the group delay at any frequency possibly on a computing machine as simple as a hand calculator, but the true beauty of the technique is that arbitrary grading profiles should be readily analyzable even in instances where an exact solution of the differential equation is impossible and numerical solutions of such equations difficult at best.
Transfer of Information

1. In December 1981 our gain bandwidth technique was used by R.C.A. Government Systems Division in the design of broadband microwave antenna equalizers.


Technical Publications


3. B.S. Yarman and H.J. Carlin, "A simplified real frequency technique applied to broadband multistage microwave amplifiers", to be published IEEE Trans. MTT.

Degrees


Task 10  **GALLIUM ARSENIDE BALLISTIC ELECTRON TRANSISTORS**

L.F. Eastman, D.W. Woodard, C.E.C. Wood and G. Wicks

**Progress**

A multilayer heterojunction photo-transistor (HPT) structure has been grown by molecular beam epitaxy (MBE) with a double base structure. The first base region close to the $Al_xGa_{1-x}As$ emitter layer is $Al_yGa_{1-y}As$ with $y < x$. ($x = 30\%$, $Y = 12\%$), Be doped $p = 10^{17} \text{ cm}^{-3}$. The second base region 1000 Å thick is GaAs Be doped $10^{19} \text{ cm}^{-3}$. The aluminum mole fraction ratio is graded between the emitter and $Al_yGa_{1-y}As$ base region. The interface between the two base regions is abrupt. With this double base region configuration, the heterojunction transistor has exhibited a typical dc current gain $\beta$ of 175. Moreover $\beta = 1$ for a current density as low as $10^{-3} \text{ A cm}^2$ due to a lower recombination current in wide gap depletion region. Very small area transistors have been fabricated with an interdigitated structure. Emitter base junction area is $6 \times 30 \, \mu\text{m}^2$ and base collector area, is $30 \times 40 \, \mu\text{m}^2$. The capacitance measured at 1 MHz for these devices are a $C_{EB}^{(OV)} = 0.5 \, \text{pF}$ and $C_{BC}^{(OV)} = 1.6 \, \text{pF}$ (including the pads).

The transition frequency of the device has been inferred from $S$ parameter measurements $f_T = 7$ is close to 8 Hz. $I_C = 5 \, \text{mA}$ and $V_{CE} = 8 \, \text{V}$.

The response speed of the phototransistor has been tested by a synchronously pumped dye laser. The pulse width is 3 ps with a wavelength of 720 nm.

As compared to previous work, the response time is very short, $\tau$
= 250 ps for a load resistance $R_L$ of 1 $\Omega$. The dc current gain is 15 and optical current gain is evaluated to 10^{-12}. The dependence of the response time on bias conditions shown that the response time, in this optimum configuration, is given by $\tau = \beta \tau_{ec}$, where $\tau_{ec}$ is the total emitter to collector transit time.

Work was done with graduate student Susan Palmateer on the growth of planar doped barriers in GaAs and the effects of impurity out diffusion from substrates on the diode characteristics. PDB's were grown by MBE and processed for characterization as ballistic electron launchers, however this work remains incomplete.

Work was also done on a new type of rectifying heterojunction structure in the AlGaAs-GaAs system. The structure is a triangular barrier n-n heterojunction exhibiting unipolar transport which has applications in barrier transistors, ballistic electron launchers, and possibly tunnel diodes.

Diode structures have been fabricated by MBE. Diodes have been processed and characterized by DC I-V measurements. Rectification has been observed at room temperature for a number of AlGaAs composition.

A computer model based on thermionic emission has been developed which provides rough agreement with experimental data.

Attempts to realize vertical microwave transistors in GaAs with various sizes have been made by MIT-Lincoln Labs., Westinghouse and Cornell. For mm-wave performance sub-micron technologies have been primarily directed towards gate length control.

A novel vertical electron transistor (VET) which combines for the first time both lateral and vertical submicron dimensions was
done (figures 1 and 2). Its major advantages are:

i. The submicron drain to source contact spacing allows for the first time to study the impact of near-ballistic electron transport on transistor performance.

ii. The technology is amenable to the incorporation of hot electron launchers via MBE or MOCVD.

iii. The unique technological approach allows the fabrication of different channel slopes to optimize the intrinsic device configuration for mm-wave applications.

iv. The use of thick Schottky gate metallization minimizes gate resistance.

First devices were fabricated by MBE with 0.5 micron active layers of two doping levels sandwiched between $n^+$ contact layers. Patterning of the submicron channel configuration was done by optical lithography and a combination of dry and wet etching. Rectangular and trapezoidal channel cross-sections were realized. (See figures 1(a) and 2(a)). The Schottky gate was angle-evaporated onto the channel side walls.

The device characteristics are summarized below (also see figures 1(b) and 2(b)).

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Figure 1</th>
<th>Figure 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active layer doping</td>
<td>$7 \times 10^{15}$ cm$^{-3}$</td>
<td>$5 \times 10^{16}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Gate periphery</td>
<td>640 microns</td>
<td>640 microns</td>
</tr>
<tr>
<td>Source drain spacing</td>
<td>0.5 microns</td>
<td>0.5 microns</td>
</tr>
<tr>
<td>Gate length</td>
<td>0.15 microns</td>
<td>0.15 microns</td>
</tr>
<tr>
<td>$g_m$</td>
<td>47 mS/mm</td>
<td>81 mS/mm</td>
</tr>
<tr>
<td>Gate-drain breakdown</td>
<td>$\sim 10$ V</td>
<td>$\sim 10$ V</td>
</tr>
<tr>
<td>Active input cap. at 1 MHZ</td>
<td>$\leq 0.33$ pF</td>
<td></td>
</tr>
</tbody>
</table>
(a) gate offset +0.5V
channel doping:
\[ N = 5 \times 10^{16} \text{ cm}^{-3} \]

(b) gate offset +0.5V
channel doping:
\[ N = 7 \times 10^{15} \text{ cm}^{-3} \]

Back contact is the drain
Fingers form the source
Recessed metallization is the gate contact
The measurements on $5 \times 10^{16}$ cm$^3$ devices conservatively predict an $f_T$ of 24 GHz. In the $7 \times 10^{15}$ cm$^3$ devices, electron average velocity appears to be around $3 \times 10^7$ cm/s based on current flow considerations. Subtracting parasitic elements leads an estimated intrinsic $f_T$ of around 50 GHz. Further device analysis and microwave measurements are currently being undertaken.

Work was aimed at developing planar ion-implanted self-aligned submicron GaAs MESFETs. Our initial fabrication process development for these devices at Hughes was done. Sputtering of TiW with good adhesion to GaAs and plasma etch, using a metal etch mask, with good control of etch rate and undercut in a CF$_4$-O$_2$ plasma was done. Successful ion implantation and capped annealing of these structures was demonstrated with both SiO$_2$ and Si$_3$N$_4$ encapsulants. Diodes fabricated by this process had slightly better electrical characteristics than those originally reported by Yokoyama et al. at Fujitsu. Processing of some wafers for ring oscillator measurements were done at Hughes. When completed, these wafers had propagation delays as low as 25 ps at 300$^0$K, the fastest all-GaAs digital circuits to date. These results were reported at the 1982 Device Research Conference, and have been submitted for publication in Electron Device Letters.

At Cornell work focussed on capless annealing, alternative refractory gate metalizations, and submicron gate structures, all aimed at using this self-aligned gate process to achieve ultrashort electrical gate lengths with enhanced electron velocity.

Capless annealing studies were undertaken in several different areas. C-V profiling was used to evaluate relative activation
efficiencies for implanted Si$^+$ ions into GaAs under different capless anneal schedules (temperature/time), so that a suitable annealing schedule could be chosen. Studies were done of annealed TiW diodes on MBE GaAs, with encouraging results. The stability of GaAs/TiW and GaAs/Ti/Mo interfaces under capless annealing conditions was evaluated by RBS and by electrical measurements. Capless annealing of various modulation-doped structures were also done in order to evaluate their suitability for post-implant annealing.

Plasma etching and RIE of TiW under an aluminum etch mask was performed, using the etching systems at Cornell and was found to be feasible to begin device fabrication.

The first working ion-implanted SAGFET devices made at Cornell were processed during April 1982. These were entirely fabricated by E-beam lithography, using ion-implanted active layers and sputtered TiW done at Hughes. These represent the first such devices done by E-beam lithography, and the first to employ arsenic-overpressure capless annealing. In addition to process test patterns (for measurement of gate resistance, $n^+$ sheet resistance, device isolation, etc.), these wafers included an array of 8 test FETs with various gate lengths. The two wafers processed had electrical gate lengths (the spacing between implanted $n^+$ regions) ranging between 0.5 and 1.4 microns. Transconductances of 80-100 ms/mm were observed, but the devices also had an undesirably high output conductance, and exhibited a marked decrease in threshold voltage with decreasing gate length. DC measurements seemed to offer some possible preliminary evidence of enhanced electron velocity in the 0.5 micron FETs.
Related Work

The planar doped barrier transistor was proposed as a new device structure in which to study electron motion in the realm of "near ballistic" transport.

Conclusion of study of manganese in GaAs experimentally and theoretically - Mn was originally chosen as a p-type dopant to be used in the PDB structures as an alternative to Be which is highly toxic. Mn for a number of reasons (i.e., diffusion, surface segregation and electrically inactive \(T < 300^\circ\text{K}\)) is not a suitable dopant for the growth of PDB structures.

Growth of PDB diode structures on 360 MBE system - Si used as n-type dopant, Be p-type dopant. Due to variation of fluxes across a wafer there were large variations in doping uniformity and layer thickness which resulted in a variation of \(\Phi_{BO}\) across a 1" wafer of 50%. Symmetric around 0.5 eV-1.0 eV PDBD's were grown and analyzed.

Growth of PDBD's initiated on new Generation II MBE system - Continuous azimuthal rotation necessary for precise control of doping and thickness uniformity across a 2" GaAs wafer. Initially there was no reproducibility of designed barrier heights which was found to be substrate related. SIMS showed that the Be \((p^+)\) plane in layers grown on Si-doped (around \(4 \times 10^{18} \text{cm}^{-3}\)) Bridgeman GaAs substrates diffused around 200 Å not observed in layers grown on Sn-doped, Cr-doped or undoped substrates. This is attributed to defect enhanced diffusion. Reproducibility of \(\Phi_{BO}\) in layers grown on Sn-doped (around \(4 \times 10^{17} \text{cm}^{-3}\)) Bridgeman GaAs substrates was found to be growth parameter dependent. Fast growth rate (1.6 micron/hr compared to 0.95 micron/hr) and high substrate temperature (around 640°C)
resulted in the most reproducibility. High $T_s$ volatile unintentional impurities desorb from growth surface. Fast growth rate in the growth surface outruns substrate-epilayer interface effects and related fields which can effect impurity incorporation in the intrinsic regions. Precise control and excellent uniformity on designed barrier heights was achieved by heat-treatment of semi-insulating substrates (and removal of converted surface) (Cr-doped and undoped) prior to MBE growth. A Be cell transient was identified. The Be flux is a factor of 2.5 x higher for 10 second-1 minute shutter times as compared to infinite shutter times. The transient is reproducible from run to run.

Design, processing, measurements, and analysis of GaAs planar-doped barrier ballistic electron transistors - The epi-layer for the first successful prototype of the planar-doped barrier (PDB) transistor was grown in a Varian 360 MBE machine by Dr. Roger Malik at the U.S. Army ERADCOM in Ft. Monmouth, NJ in mid-May, 1981. The intended emitter barrier height was 0.25 V, the intended collector barrier height was 0.2 V, and the $V$ base width was 1000 $\AA$. The wafer was delivered to Cornell where it was processed and measured by graduate student Mark Hollis. The transistor, which is a vertical current flow device, uses two mesa etches followed either by deposition of an insulator ($Al_2O_3$) or by a proton bombardment step to achieve contact pad isolation. The prototype transistor exhibited no power gain at room temperature, but at $77^0K$ it displayed a maximum DC power gain of 2.5 dB and a maximum common-base current gain $\alpha$ of 0.15.

In an effort to improve on this performance, six more transistor
layers were grown at ERADCOM and processed at Cornell between July 1981 and October 1981. Measurements after processing revealed that both the emitter and the collector barriers in all six layers were effectively nonexistent (i.e., shorted out). In October 1981, work was begun at Cornell by graduate student Susan Palmateer, senior research associate Colin Wood and Mark Hollis to solve the apparent MBE materials growth problems responsible for the barrier height reduction. In December, a new Varian Generation II MBE machine was put into operation at Cornell. From January to April a large number of PDB calibration diode layers were grown on this machine. Using a procedure developed by Mark Hollis, the resulting I-V characteristics of these diodes were fitted to a thermionic emission model in order to determine the effective barrier heights and leverage ratios of the diodes. The barrier heights of these diodes were observed to vary randomly by as much as a factor of 2 or 3. In April 1982 this nonreproducibility problem was shown to be related to the outdiffusion of impurities and/or deep levels from the substrate during growth. The problem was solved by baking the wafers at 750°C for 24 hours and polishing off a few microns of material before MBE growth.

The thermionic I-V model has also been instrumental in explaining the disappointing performance of the prototype PDB transistor. The real emitter barrier height has been ascertained to be 0.46 V which is well above the intervalley scattering threshold of 0.34eV, and the base doping was actually found to be roughly $10^{18}$cm$^{-3}$ which is a factor of 2 or 3 higher than desired. These facts combined to yield the poor $\alpha$ observed in the device.
All of the early planar-doped barrier problems had now been solved, and renewed PDB transistor work was begun at Cornell in late April 1982.

Degrees
R. Malik, Ph.D., August 1981
M. Hollis, M.S., May 1981

Publications


