THE DEVELOPMENT OF REFRACTORY METALLIZATION FOR HIGH-SPEED VLSI CIRCUITS
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The Development of Refractory Metallization for High-Speed VLSI Circuits

by

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ABSTRACT

The use of refractory materials (metals, silicides and composites) in VLSI circuits is reviewed. Material consideration, including deposition techniques, film structure, electrical and mechanical properties, are covered. Gate structures implemented with a variety of refractory materials are described. Semiconductor device processes incorporating these materials—plasma etching, ion implantation, oxidation—are discussed from the perspective of VLSI compatibility. Characteristics of MOS devices and circuits using refractory technology are reviewed.
I. INTRODUCTION

Refractory metals and metal silicides have been recently under active development for use as gate and interconnection materials in very-large-scale-integrated (VLSI) circuits. The main advantage of these refractory materials over conventional doped polycrystalline silicon (poly-Si) is their high conductivity. Since it has become apparent that the scaling down of semiconductor devices may not lead to overall higher performance unless low resistance gates and interconnects are implemented, refractory materials are becoming an indispensable part of any VLSI process.

To quantitatively describe the relationship between signal propagation delay and line resistance, an open-end, unloaded transmission line model was used for 1000 μm-long lines of Mo, MoSi$_2$ and poly-Si. The sheet resistance assumed were 0.2, 2 and 20 Ω/□ square, respectively. The thicknesses of the oxide layer underneath the signal line were 250 and 5000Å representing typical active and field areas, respectively. Also, the fringing field effect due to narrow line width has not been included. The results of the simulation are shown in Fig. 1. The delay time, with a metal line over 250 and 5000Å oxide is only 20 and 300 ps respectively (A and C). The silicide and the poly-Si lines, on the other hand, can delay the signal for 150 ps and 1.2 ns respectively when running over field oxide regions (B and D). It is worth noting that the present simulation probably represents the best case in signal response because both loading of the line and fringing field effects degrade the response time. Hence, replacement of poly-Si with refractory metals or metal silicides can alleviate this problem in very high speed and high density microcircuits.

In this paper the development of refractory materials for VLSI circuits is reviewed. The following aspects are covered: thin film structural and electrical properties, processing technology (patterning, oxidation, ion implantation and contacts), gate
structures (metal, silicide, composite), device and circuit characteristics.

(Figure 1)
II. MATERIALS PROPERTIES

In this section, thin film material properties of refractory metals and metal silicides are discussed.

In Table 1, the elements which form refractory metal silicides are shown.

(Table 1)

In particular, the deposition, structure, composition and resistivity of Mo, W, MoSi₂, NbSi₂, WSi₂, TaSi₂, TiSi₂ and related composites are reviewed.

A. Deposition

Chemical vapor deposition (CVD), sputtering and electron-beam evaporation are the main methods used for thin film deposition.

For refractory metals, the use of CVD usually requires the reduction of the related halide compound. In the case of Mo deposition, MoF₆[1] and MoCl₅[2] are employed, while for W deposition WF₆[3] and WC₁₅[4] are used. The fluoride process requires more control as HF is released during hydrogen reduction and can etch the underlying thin gate oxide. Sputtering and e-beam deposition are mostly physical processes and do not depend on the specifics of the reaction process as CVD does. However, other problems arise, such as incorporation of sputtering gas atoms or radiation damage [5].

Deposition of metal silicide films has to take into account additional considerations, such as stoichiometry. DC magnetron sputtering and evaporation are the methods most frequently used [6;7,8]. Co-deposition methods [9, 10] are the most attractive because of flexibility in the silicon/metal ratio obtained. CVD has not been employed in the deposition of silicides because of undesirable formation of intermediate silicide phases [11].

B. Structure and Composition

The structure of the refractory metals studied (Mo and W) is body-centered cubic. The thin films exhibit columnar grains and are strongly oriented on oxidized silicon substrates [12].
Secondary-ion mass spectrometry (SIMS) reveals that carbon is a major contaminant in Mo films.

The structure of most refractory metal silicides is either hexagonal or tetragonal. Molybdenum disilicide exhibits both phases. It is hexagonal for temperatures below 800°C and changes to tetragonal above that point [13].

In Fig. 2, the x-ray diffraction pattern of a 3000 Å-thick molybdenum silicide (Si/Mo-2.2) film is shown. The film was deposited by cosputtering from the elemental targets and then annealed at 1000°C for 1 hr. The spectrum indicates that the only silicide phase present is tetragonal MoSi₂.

(Figure 2)

Tungsten disilicide is normally tetragonal. The hexagonal phase is less stable than its MoSi₂ counterpart and has been observed only recently [14,62, 63]. NbSi₂ and TaSi₂ thin films show only the hexagonal structure [15,16]. TiSi₂ is the only silicide to show the orthorhombic phase in thin film form [17]. Since the desired composition (of the disilicide) is the most silicon-rich phase, a silicon/metal ratio greater than two is employed to prevent the formation of intermediate phases [18,22]. Major contaminants detected in sputtered silicide films are carbon and argon [15,19].

C. Resistivity
In bulk form, the resistivity of most refractory metals falls between 5 to 10μΩ-cm and for most refractory silicides the range is 20 to 50μΩ-cm [20].

In thin film forms, the resistivity reported [21] for Mo is 8μΩ-cm for e-beam evaporation, 14μΩ-cm for RF-sputtering and 10.5μΩ-cm for DC-magnetron sputtering. In the case of W, the resistivity values reported [21] for each deposition technique are 13, 34 and 21μΩ-cm, respectively. CVD deposition results in the lowest reported resistivity for both Mo(6.5μΩ-cm) [1] and W(55μ-cm) [4], approaching bulk values.

The thin film resistivity of the sili-
cides is highly dependent on deposition technique. For example, MoSi$_2$ films prepared by e-beam co-evaporation [9], RF sputtering [7], DC sputtering [6,19] and cosputtering [22] showed a resistivity of 45, 60, 120 and 100$\mu$Ω·cm, respectively.

In Fig. 3, the sheet resistivity of two cosputtered molybdenum silicide films (Si/Mo=2 and 2.3) are shown as a function of isochronal annealing temperature.

(Figure 3)

For comparison, the MoSi$_2$ bulk resistivity is 22$\mu$Ω·cm [20]. The thin film resistivity of WSi$_2$, NbSi$_2$ and TaSi$_2$ closely parallel the case of MoSi$_2$. TiSi$_2$ shows substantially lower resistivity for all deposition techniques, with the lowest value of 21$\mu$Ω·cm (vs. 17$\mu$Ω·cm bulk value) reported for e-beam evaporation [23].
III. GATE STRUCTURES

The implementation of novel materials into a gate structure suitable for VLSI requires, in addition to low resistance, a high melting point. However, there are substantial differences on the other gate structure requirements between refractory metals, metal silicides and various composites.

In Fig. 4, four different refractory gate structures involving the metals and/or metal silicides are illustrated.

(Figure 4)

A. Refractory Metals
Refractory metals, such as Mo and W, have a resistivity of 5-10 $\mu\Omega$-cm, which is at least two orders of magnitude lower than that of polysilicon. However, they have poor resistance to oxidation and to chemicals used in semiconductor processing. In addition, some refractory metals (such as Mo and W) exhibit columnar grains [12,21] are, thus, prone to mobile ion contamination. Therefore, one of the key requirements for the use of the refractory metal gate approach is proper gate passivation. This has been accomplished using doped glass (PSG) [24,25], self-grown silicide [26,27] and silicon nitride/oxide [28] and molybdenum nitride [29]. Doped phosphosilicate glass containing 2% or more phosphorus has been found to be an effective gettering agent for the mobile ions [25]. The self-grown silicide and deposited Mo-nitride passivation techniques are discussed in the section on composite structures. The silicon nitride passivation has also been successfully used [28] with the additional advantage of deposition in an oxygen-free ambient. This prevents possible oxidation of the gate metal during passivation.

B. Refractory Metal Silicides
Refractory metal silicides generally have resistivities of 50-100 $\mu\Omega$-cm, which places them in between those of the refractory metals and of doped polysilicon. However, like poly-si, the silicides have a high resistance to chemical attacks and can grow a
high-quality and self-limiting oxide. The oxidation process of the silicide film produces silicon dioxide and can partially (or totally) consume the film resulting in a higher sheet resistance and can lead to lower gate reliability [9,30].

\(\text{MgSi}_2\) gate structures have been shown to be overall compatible with \(\text{SiO}_2\) and \(\text{Si}_3\text{N}_4\) gate dielectrics [6,7]. Other silicide gate structures incorporated in MOS devices include \(\text{NbSi}_2\) [15] and \(\text{WSi}_2\) [31].

C. Composite Materials
A variety of composite gate materials, involving refractory metals and silicides, have been investigated with the goal of enhancing the overall characteristics of the MOS structure.

i. Silicidation Approach.
One disadvantage of the refractory metal gate is its poor oxidation resistance. Since the metal oxides are volatile at high temperatures, surface passivation techniques (as described in Section III.A) usually involve deposited dielectrics. An alternative is the process of silicidation [26,27] in which molybdenum is reacted with \(\text{SiH}_4\) to form a surface layer of molybdenum silicide. The \(\text{Mo/MoSi}_2\) composite (so-called "heart-of-moly") has the advantage of good oxidation properties, which the metal itself lacks.

The sheet resistance of the composite structure as a function of reaction time is shown for two \(\text{SiH}_4\) flow rates in Fig. 5. As can be seen, the higher flow rate results in a faster conversion of the Mo into \(\text{MoSi}_2\) and thereby a higher sheet resistance. This structural modification can be clearly seen from the corresponding x-ray data (Fig. 6) taken on samples A and B.

(Figure 5)

(Figure 6)

ii. Metal Nitride Approach.
Other disadvantages of the refractory metal gate are mobile ion contamination and ion channeling due to its columnar grain structure. By fabricating a com-
posite gate material which combines the metal (Mo) with one of its nitrides (Mo$_2$N), an effective ion barrier is introduced [29]. Since the nitride is metallic in character it does not lower the gate conductivity greatly.

iii. Polycide Approach.
One disadvantage of the silicide gate approach is the consumption of the layer during oxidation. To prevent this problem, a polysilicon pad can be placed between the gate dielectric and the silicide layer [8,9]. This polycide approach has been shown to effectively preserve the low silicide gate resistivity while maintaining the high reliability of silicon-gate technology. The polycide approach has been realized in structures using WSi$_2$ [8,9,32], MoSi$_2$ [33,34], TaSi$_2$ [30,35,36], TiSi$_2$ [23,30,37].

Various techniques have been employed to realize such a polycide structure. These include: a. deposition and doping of the poly-Si pad followed by deposition (or co-deposition) of the silicide [8,9,23,30,34]; b. deposition and doping of the poly-Si pad followed by deposition of the metal and by sintering [40,42]. Because of the lower conductivity of the poly-Si pad, the resistivity of the polycide structure is controlled by the silicide. In the case of the WSi$_2$/n+ poly-Si gate, a sheet resistance of 1.2Ω/μm was reported [9] for a combined structure consisting of 2500Å of WSi$_2$ on 3000Å of doped poly-Si. For TiSi$_2$ and TaSi$_2$ (2700Å) cosputtered on poly-Si, sheet resistances of 1 and 2Ω/μm were obtained [30]. Threshold voltage and gate breakdown voltage distribution for polycide-gate devices have been shown [8,9] to be equivalent to those with silicon-gate.

D. Edge-Defined Structures
To fabricate sub-micron gate structures without elaborate lithographic systems, edge-defined technique have been employed with silicon-gate technology [38]. The edge-defined approach usually involves the following steps: (a) definition of a vertical edge; (b) conformable deposition of either a gate material (direct technique) or a
material to be used as a transfer mask (indirect technique); (c) anisotropic etching of the conformable film, resulting in a residue along the initial edge; (d) selective removal of the initial step material, leaving only the residue; and (e) transferral of the pattern with an underlying gate material layer (indirect technique only). The direct edge-defined process sequence is shown schematically in Fig. 7.

(Figure 7)

Even though the edge-defined techniques are basically not oriented toward high-density circuits, they offer the ability to fabricate and study the sub-micron device components of VLSI. The direct edge-defined technique has been applied to MoSi$_2$-gate MOS structures [39]. Al steps, defined by CCl$_4$ plasma etching, were used in conjunction with MoSi$_2$ films etched in NF$_3$ plasmas to achieve controllable line widths as small as 0.1μm.

SEM micrographs of an edge-defined structure is shown in Fig. 8.

(Figure 8)
IV. PROCESSING TECHNOLOGY

To incorporate refractory materials into the integrated circuit fabrica-
tion, the development of specific pro-
cesses is required. These include etching for pattern definition, oxy-
dation, the effect of ion implantation, and contact formation. In this section, the work covering processing technology with refractory materials is discussed.

A. Patterning
Pattern definition is an important step in the circuit fabrication sequence. Conventional wet chemical etching tech-
iques which usually results in iso-
tropic edge profiles are not adequate for high resolution VLSI structures. Various dry etching methods, such as planar plasma etching and reactive ion etching, have been widely investigated. Whereas dry etching of silicon has been extensively studied [43], relatively little work has been reported for refractory metals and metal sili-
cides. Most of the work on these materials is confined to fluoro carbons, such as CF$_4$/O$_2$ [21,44,45,46], and to a lesser degree, NF$_3$ [47,48], SF$_6$ [49], and CCl$_4$/O$_2$ [37,50].

In the case of silicide etching in CF$_4$/O$_2$ plasma, the basic mechanism presumed [44] to involve the reaction of the silicide with fluorine radicals resulting in the metal hexa-fluoride and SiF$_4$. For a CF$_4$/4% O$_2$ mixture in a barrel reactor MoSi$_2$ etch rate of 920Å/min was measured at an RF power of 100W and 0.3 torr [44]. Under similar conditions, an etch rate selectivity of ~18 for MoSi$_2$ over SiO$_2$ and of ~3 for poly-Si over MoSi$_2$ were reported [44]. An etch rate of 820Å/min was obtained for NbSi$_2$ [15]. For WSi$_2$ in CF$_4$/O$_2$ mixtures, an etch rate ratio of 1.2-0.9 for WSi$_2$/poly-Si has also been measured for O$_2$ percentage up to 10% [45]. In NF$_3$ plasmas, the Mo and MoSi$_2$ etch rates have been found to be generally higher than those in CF$_4$/O$_2$ plasmas. Fig. 9 shows the etch rate in NF$_3$ plasma as a function of reactor pressure at 1A of RF current.

(Figure 9)
At a pressure of 0.2 torr in a planar reactor, an etch rate of 1800 and 7850 Å/min has been reported [47] for Mo and MoSi₂, respectively. Diluting NF₃ with inert gases, such as argon and helium, resulted in significant decrease in etch rate [48]. The etch selectivity of MoSi₂ over SiO₂, Mo over SiO₂ and MoSi₂ over poly-Si were 4-8, 1.5-4 and 2.5-4, respectively [48]. The capability of the plasma etching process is demonstrated in the fabrication of 1μm MoSi₂ lines, as shown in the SEM micrograph of Fig. 10.

(Figure 10)

Plasma etching of MoSi₂ in a barrel reactor with CF₄/O₂ mixtures has resulted in an isotropic edge profile. On the other hand, a fairly anisotropic profile (vertical-to-lateral etch ratio of ~3) was measured in planar plasma etching with NF₃ [48]. The edge profiles of the WSi₂/n+poly-Si structure have been investigated in CF₄/O₂ mixtures in a planar reactor [45] as well as in a flexible diode reactor [46].

B. Oxidation

The growth of a high-quality oxide layer is an attractive aspect of the silicide-gate technology. The oxidation kinetics of several of the silicides have been studied in oxygen and steam ambients for silicide on oxide or silicon substrates. In the case of MoSi₂ thin films on SiO₂/Si, oxidation in dry oxygen leads to the formation of SiO₂ and intermediate silicides (Mo₅Si₃, Mo₃Si) [51,52]. The value of the activation energy for the linear and parabolic rate constants have been shown to be 44 and 37 Kcal/mole, respectively. Similar oxidation characteristics have been found for WSi₂ films sputtered from alloy targets, resulting in W₅Si₃ and SiO₂ [53]. Oxidation of coevaporated WSi₂ films, results in free tungsten in coexistence with WSi₂, but no intermediate silicide phases [54]. The difference in structure upon oxidation may be attributed to the level of impurities (cf. carbon) present in the deposited films [55].

Oxidation studies on other silicides, such as TaSi₂ [56-58] and TiSi₂ [59,60] have also been done. These silicides
have different oxidation characteristics. For TaSi$_2$, in dry oxygen or steam, silicon dioxide was found on surface. However, for TaSi$_2$ on poly-Si in oxygen, only a very thin (~70Å) layer of SiO$_2$ (but no metal oxide) and no further oxidation were observed. On the other hand, TaSi$_4$ can be readily oxidized in steam, resulting in a surface layer of mixed Ta-Si oxide with SiO$_2$ underneath. The activation energy for parabolic rate constant in steam has been determined to be 32 Kcal/mole [56]. In the absence of an underlying silicon layer, steam oxidation leads to formation of mixed oxide at low temperatures (<1000°C) but only SiO$_2$ at high temperatures [58]. A mixed Ti-Si oxide with underlying SiO$_2$ has also been found in steam oxidation of TiSi$_2$ on single crystalline or poly-Si [59,60]. Similar values of activation energy have been deduced.

C. Ion Implantation
Since the gate metal is often used as ion implantation mask during the source/drain doping, the effect of implantation of various Group III and V ions on silicide thin films needs to be investigated. The case of phosphorus implantation into MoSi$_2$ thin films has been recently studied [19]. Structurally, implantation increases the hexagonal to tetragonal MoSi$_2$ transition temperature. Also, possible presence of MoP was detected at high dosages. Significant redistribution of phosphorus after annealing was also observed, similar to the WSi$_2$ case [32] but the level of contaminants (Ar,C) remained essentially the same. Isothermal and isochronal annealing have indicated a minimum temperature of 950°C and a maximum dose of 2x10$^{16}$/cm$^2$ may be used without significantly increasing the sheet resistance of these silicide films.

D. Ion-Beam-Induced Contacts
Since the thermal formation of metal-to-silicon ohmic contacts for many of these refractory materials are not optimal [13], interface mixing for contact formation has been studied for various refractory metal/Si structures by implantation with different types of ions. Inert gases [61] and Group III or V elements [62-64] have been
explored. When Group III or V ions are used, silicide formation and contact doping can be combined in one step. In the case of Mo/Si, implantation of phosphorus or arsenic leads to the formation of hexagonal MoSi$_2$ [62-64] which is transformed to the tetragonal phase after annealing at temperatures higher than 800°C. Also, traces of MoP were found at high dosage of phosphorous [64]. Smooth surface morphology and low contact resistance are some of the attractive features of these ion-beam-induced contacts. Recently, an application of this technique has been reported in the fabrication of an Mo-gate, 4K static RAM circuit [65].
V. DEVICES AND CIRCUIT CHARACTERISTICS

The incorporation of refractory materials in state-of-art integrated circuits requires the study of the related MOS structures and device and circuit components. In this section, we first discuss the characteristics of MOS capacitors and discrete FET's. The performance potential of refractory materials in VLSI circuits is then presented in the results from typical test vehicles. Finally, VLSI circuits implemented with this technology are reviewed and their performance described.

A. MOS Structures
To successfully utilize these refractory metals and metal silicides in circuits, various MOS device parameters need to be determined and carefully controlled. The work functions of these materials, MOS threshold voltage and its stability, gate breakdown voltage distribution as well as device and circuit parameters are among them. Capacitance-voltage measurements on MOS capacitors have been used to determine the work functions of these refractory materials. Whereas the metal work functions have been well known and also been determined with other techniques [66], the silicide work functions have only been obtained from MOS structures recently [6,15,67, 68].

For example, the flatband voltages versus oxide thickness for NbSi₂ p- and n-MOS structures, as shown in Fig. 11, correspond to work function values of 4.35 and 4.53 eV, respectively.

(Figure 11)

Generally, values ranging between 3.67 and 4.25 eV have been reported for TiSi₂ and TaSi₂ and between 4.35-4.8 eV for NbSi₂, WSi₂, and MoSi₂, while values between 4.02-4.63 eV for all the metals considered here. Hence, the metal and metal silicide work functions are nearly the same. Comparing these with the value (4.2 eV) for n+ poly-Si, the disilicides of niobium, tungsten and molybdenum have higher values.
Unlike doped poly-Si, these metals or metal silicides do not have a phosphorus gettering cycle in their process. Consequently, threshold voltage stability may not be realized due to contaminants within the metal or metal silicides. Phosphorus has been put into MoSi$_2$ films [69,70] to ensure threshold stability. Furthermore, surface state densities comparable to that of poly-Si have been shown for Mo-, MoSi$_2$- and WSi$_2$-gate devices [21,6,31], as well as for many polycide-gate devices [9,35,37].

B. Test Devices and Circuits
Several short channel refractory-gate MOSFET's have been reported [7,8,9,21,28,35,37]. For refractory metals, Mo-gate devices have been scaled down to <2μm [21,28]. Also, size effects, similar to those observed for silicon-gate devices, have also been measured in silicide- or polycide-gate MOSFET's using MoSi$_2$, WSi$_2$, and TiSi$_2$ [7,33,71,35,28].

An example of a short-channel, MoSi$_2$-gate MOSFET, with dimensions of 1.7x1.7μm$^2$, is shown in Fig. 12.

(Figure 12)

Generally, significant decreases in threshold voltage were found for FET's with channel lengths less than 3μm.

Threshold voltages as a function of channel length for MoSi$_2$-gate MOSFET's are shown in Fig. 13.

(Figure 13)

Field-effect electron mobilities approaching the silicon-gate counterparts (600V/cm-s) have also been reported [71,9,35,28]. Finally, N-channel, depletion-mode devices using WSi$_2$-gates have also fabricated [72].

A number of refractory-gate test vehicles used to study the circuit performance have been reported. These include NMOS, CMOS/SOS and CMOS ring oscillators, and an 8K ROM [73,33,34,6]. An NMOS silicide-gate, 2-μm, 25-stage ring oscillator exhibited a minimum delay of 1ns [73] while a MoSi$_2$/n+ poly-Si gate, 4μm CMOS/SOS ring oscillator
had a delay of 0.6 ns [33]. A micro-
photograph of a test chip implemented
with 3μm CMOS technology and polycide
(MoSi2/n+ poly Si) and MoSi2 gates is
shown in Fig. 14.

(Figure 14)

A 39-stage ring oscillator and a 1100-
transistor block of pattern generator
contained on the test chip showed simi-
lar delay of 1.2ns/stage.

Switching delays and power-delay
products for ring oscillators implemen-
ted with both gate technologies are
shown as a function of power supply
voltage in Fig. 15. The delay per
stage as a function of power consumed
is shown in Fig. 16. It is interesting
to compare the performance of this cir-
cuit with the state of the technology
[81] in 1982 as shown in Fig. 17.

(Figure 15)
(Figure 16)
(Figure 17)

C. VLSI Circuits
Recently, refractory gate technology,
particularly molybdenum, has matured
to the extent that VLSI circuits have
been fabricated. Among the refractory
metal gate RAM circuits reported to
date include: 64K and 256K Mo-poly-Si
gate dynamic RAM's [74,75,76] as well
as 2 4K Mo-gate static RAM with novel
buried contact techniques [77,65].

Also, two polycide-gate memory circuits,
a 1 m, 2K WSi2/n+ poly-gate dynamic RAM
[32,78] and a 64K dynamic RAM [36] using
TaSi/n+ poly-Si, have been presented.

Furthermore, a 32-bit VLSI processor
containing 450K transistors using poly-
Si gates but two upper levels of tung-
sten interconnects [79,80] have also
been announced.

In the dynamic RAM's fabricated with Mo-
Poly technology, molybdenum is used for
the word line and gate electrodes for
MOSFET's in memory cells and aluminum
for the bit line and the column select
line. Poly-Si is only used for gate
electrodes for MOSFET's in peripheral
circuits and storage capacitor elec-
trodes. Since both the word line and
the bit line use metals, the propaga-
tion delay within the memory array is
small. The 64K chip has a
die size of 3mm x 3mm and memory cell size of 8μm x 8μm. An access time of 95ns has been achieved. Scaling up the complexity to 256K increases the die size to 5.8 x 5.9 mm but the memory cell size (8μm x 8.6μm) and access time (100 ns) remains essentially the same. Novel buried contact schemes tried in the 4K Mo-gate RAM's are: incorporation of phosphorus during molybdenum film evaporation and its subsequent diffusion into the silicon substrate [77], and ion-beam-induced contact formation with arsenic [65] prior to Mo deposition. Small memory cells (21 μm x 34 μm) and fast access time (18ns) are the main attractive features of these RAM's.

For the polycide-gate RAM's, in the case of WSi₂/n+poly-Si, a memory cell size of 34 μm² with 1 micron minimum feature size has been described [32, 78]. An almost order-of-magnitude improvement in wordline risetime has been achieved with the use of the polycide as the word-line material instead of poly-Si [32].
VI. SUMMARY AND CONCLUSION

Refractory metals and related compounds have been known for some time to be compatible with MOS IC processing. Until recently, the lower sheet resistance achieved with refractory metals was outweighed by the increased process complexities and difficulties. The present drive towards one micron resolution for VLSI has resulted in renewed interests in this technology. Considerable activities have been undertaken in the understanding and development of the science and technology of refractory gate materials for VLSI. While those activities continue at present, the technology has been developed to the point where most VLSI memory and logic circuits contain refractory materials as a critical component. In this paper, we have reviewed the development of refractory gate metallization for VLSI circuits in all of its aspects: thin film material properties, gate structures, processing technology and device and circuit characteristics.

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<td>Schematic cross-sections of various refractory gate structures (a) Mo gate, (b) MoSi₂ gate, (c) MoSi₂/poly-Si (polycide) gate, and (d) MoSi₂/Mo (&quot;Heart-of-Moly&quot;) gate.</td>
<td>7</td>
</tr>
<tr>
<td>Fig. 5</td>
<td>Sheet resistance of silicidized Mo films as a function of reaction time for times up to 2 min.</td>
<td>8</td>
</tr>
<tr>
<td>Fig. 6</td>
<td>Comparison of major X-ray diffraction peaks of Mo films which were silicidized at 800°C for 60 sec. at a 10% SiH₄ flow rate of (a) 48 and (b) 144 cm³/min.</td>
<td>8</td>
</tr>
<tr>
<td>Fig. 7</td>
<td>Schematic process procedure of direct edge-defined patterning technique.</td>
<td>10</td>
</tr>
<tr>
<td>Fig. 8</td>
<td>SEM micrograph of hyperfine structure. (a) Cross section of MoSi₂ line, (b) Bird's view of MoSi₂ line.</td>
<td>10</td>
</tr>
<tr>
<td>Fig. 9</td>
<td>Etch rates of Mo, MoSi₂, doped poly-Si and SiO₂ are shown as a function of reactor pressure at 1A in 100% NF₃.</td>
<td>11</td>
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</tbody>
</table>
Fig. 10  SEM cross-sectional view of a-1μm MoSi$_2$ line which was etched in 100% NF$_3$ at 1A and 100mTorr. The-1μm-thick positive photoresist that was used as mask has not yet been removed. The 3000Å-thick silicide film was deposited on oxidized silicon substrate.

Fig. 11  Flatband voltage as a function of oxide thickness for n- and p-channel NbSi$_2$-gate MOS capacitors.

Fig. 12  SEM microphotograph of a MoSi$_2$-gate MOSFET with-2μm channel length and width. Tilt angle is 50°.

Fig. 13  Threshold voltage of silicide-gate MOSFET's as a function of channel length.

Fig. 14  Microphotograph of test chip implemented with 3μm CMOS technology and polycide (MoSi$_2$/n+ polySi) and MoSi$_2$ gates.

Fig. 15  Switching delay and power-delay product as a function of power supply voltage for both silicide- and polycide-gate ring oscillators.

Fig. 16  Power-delay product curves for both MoSi$_2$- and MoSi$_2$/n+ poly-Si-gate ring oscillators.

Fig. 17  Power-delay products for state-of-art integrated circuits.
Table I: Elements which form refractory metal silicides.

<table>
<thead>
<tr>
<th></th>
<th>Ti</th>
<th>V</th>
<th>Cr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zr</td>
<td></td>
<td>Nb</td>
<td>Mo</td>
</tr>
<tr>
<td>Hf</td>
<td></td>
<td>Ta</td>
<td>W</td>
</tr>
</tbody>
</table>
FRINGING FIELD EFFECT NOT INCLUDED

\[ L = 1000 \mu \]

<table>
<thead>
<tr>
<th></th>
<th>Material</th>
<th>( R_S )</th>
<th>( X_OX )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Mo</td>
<td>0.2 ( \Omega )/( \square )</td>
<td>5 K( \AA )</td>
</tr>
<tr>
<td>B</td>
<td>MoSi(_2)</td>
<td>2 ( \Omega )/( \square )</td>
<td>5 K( \AA )</td>
</tr>
<tr>
<td>C</td>
<td>Mo</td>
<td>0.2 ( \Omega )/( \square )</td>
<td>250 ( \AA )</td>
</tr>
<tr>
<td>D</td>
<td>Si</td>
<td>20 ( \Omega )/( \square )</td>
<td>5 K( \AA )</td>
</tr>
<tr>
<td>E</td>
<td>MoSi(_2)</td>
<td>2 ( \Omega )/( \square )</td>
<td>250 ( \AA )</td>
</tr>
</tbody>
</table>
Si/Mo
\[
\begin{array}{c|c}
2 & 2.3 \\
\end{array}
\]

\[\circ \quad \bullet \quad 30 \text{ min} \]
\[\triangle \quad \Delta \quad 1 \text{ Hr} \]
\[\triangledown \quad \nabla \quad 2 \text{ Hrs} \]

ARGON ANNEAL

Sheet Resistivity (\(\mu\Omega \cdot \text{cm}\)) vs. Temperature (\(^\circ\text{C}\))
1.6 \times 10\% \text{SiH}_4 \times 47.8 \text{ cc/min} \quad \text{MAIN H}_2 \times 30\text{ cc/min} \\
143.5 \text{ cc/min} \quad \text{FLOW} \quad \text{FLOW} \quad \text{FLOW} \quad \text{FLOW} \\

\text{TEMPERATURE 800°C} \\
\text{INITIAL Mo FILM THICKNESS 2800 Å} \\

\begin{figure}
\centering
\begin{tikzpicture}
\begin{axis}[
    xlabel={\text{TIME (SEC)}},
    ylabel={\text{$R_s$ (Ω/□)}},
    xmin=0, xmax=120,
    ymin=0, ymax=1.6,
    xtick={0,20,40,60,80,100,120},
    ytick={0,0.2,0.4,0.6,0.8,1.0,1.2,1.4,1.6},
    legend pos=north west,
]
\addplot coordinates {
(0,0.2) (20,0.4) (40,0.6) (60,0.8) (80,1.0) (100,1.2) (120,1.6)
};
\addlegendentry{SAMPLE A}

\addplot coordinates {
(0,0.5) (20,0.7) (40,0.9) (60,1.1) (80,1.3) (100,1.5) (120,1.7)
};
\addlegendentry{SAMPLE B}
\end{axis}
\end{tikzpicture}
\end{figure}
SAMPLE A
LOW SiH₄ FLOW

SAMPLE B
HIGH SiH₄ FLOW

X-RAY RELATIVE INTENSITY
(arb. units)

Mo
(110) (111)

h-MoSi₂
(101) (112)
0.1 Micrometer Lines Fabricated by Edge-Defined Lithography
Fig. 9

GAS - 100% NF₃
CURRENT - 1A

ETCH RATE (Å/min)

Poly-Si
MoSi₂
SiO₂

PRESSURE (mTorr)

80 100 150 200 250

10² 10³ 10⁴ 10⁵
NbSi$_2$-GATE MOS CAPACITORS

- N-TYPE SUBSTRATE
- P-TYPE SUBSTRATE

FLATBAND VOLTAGE (VOLTS)

OXIDE THICKNESS (Å)
MoSi$_2$-GATE MOSFET'S

$V_{DS} = 2\,\text{V}$  \hspace{1cm}  $W = 9.3\,\mu\text{m}$

$V_{SS} = 2\,\text{V}$

- $1\,\text{V}$
- $0\,\text{V}$

Threshold Voltage, $V_T$ (V)

Channel Length, $L$ ($\mu$m)
Fig. 16

![Graph showing delay vs. power for different MOS transistors.](image-url)