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Technical Reliability Studies

EOS/ESD TECHNOLOGY
ABSTRACTS
Summer 1982

Prepared by:
William K. Denson
John P. Farrell

IIT Research Institute
Under Contract to:
Rome Air Development Center
Griffiss AFB, NY 13441

Ordering No. TRS-3A

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   Electrical Overstress, Test Techniques
   Semiconductor Failure Phenomena, Failure Analysis

20. **ABSTRACT (Continue on reverse side if necessary and identify by block number)**
    The EOS/ESD Technology Abstracts is a bibliography of approximately 400 papers, reports and articles related to the subject of electrical overstress/electrostatic discharge. The intent of this bibliography is to make more accessible the present information on the subject of EOS/ESD, such as design, failure analysis, protective measures and techniques, and training programs. The cut-off date for inclusion of material was March, 1982. The 400 abstracts represent a 50% increase in content over TRS-3.
The purpose of this bibliography is to make more accessible present information on Electrical Overstress and Electrostatic Discharge. Duplication of previous studies can be avoided by the increased information retrieval capability provided by this bibliography. This bibliography contains approximately 400 abstracts of papers and articles, representing 50% more than contained in its predecessor, TRS-3. March, 1982, was the cut-off date for inclusion of material.
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INTRODUCTION AND USER'S GUIDE

The EOS/ESD Technology Abstracts references literature pertinent to Electrical Overstress and Electrostatic Discharge damage or degradation of electronic devices. Aspects found herein encompass design, failure analysis, protective measures and techniques, and training programs. References are selected for citation from the Reliability Analysis Center document files. The portion presented here dates from acquisitions made during 1969 to May 1982. Documents are selected on the basis of informational currency and usefulness as well as availability to the engineering community.

ARRANGEMENTS

This publication is arranged in eight sections: alphabetical list of terms (subjects), (subject) index, author index, corporate index, keywords in title index, bibliographic citations, source index, technology abstracts, and standards. The five digit number associated with each document is the RAC document number and is used in this publication for cross-referencing purposes.

The alphabetical list of terms is a list of terms without citations and serves as a look-up table for the "index" which it precedes. The terms are arranged alphabetically to permit easy scanning for selecting similar terms. Scanning of this list can have the following useful benefits: (1) the researcher can develop a search strategy by serendipitous association and (2) the likelihood of overlooking a highly relevant citation is minimized.

The index is the alphabetical list of terms of Section 1 with citations. The citations include the document number and the title of the documents. Including the title is a convenience which provides a possibility for selecting the most appropriate citation and eliminating those not applicable without the necessity of looking up more information elsewhere.

The author index is an alphabetical list of all authors cited whether principal or secondary.

The corporate index is an alphabetical list of all corporations, companies, institutions and government agencies with whom the authors were affiliated at the time the papers were prepared. Citations in the index include document number and title.

The keyword in title index is an alphabetical list of selected keywords in the title of the documents. Citations include document number and title. This index can be used to locate documents for which the keyword is a principal topic.

The bibliographic citations list is a compilation of all the citations of documents given in this publication. The citations are given in decreasing order by document number.
The SOURCE INDEX is an alphabetical list of the sources where the documents may be obtained.

The TECHNOLOGY ABSTRACTS provide complete coverage of the citations. Abstracts are in ascending numeric order.

The STANDARDS provide a list of government and industry standards.

IMPLEMENTATION

These indexes were composed and printed out on RADC's Honeywell 6180 computer using the General Comprehensive Operating Systems (GCOS). Programs for data input and the output reports were developed by RAC software engineers. The final manuscript was printed on an Anderson-Jacobson (Model AJ832) terminal.

SEARCH EXAMPLE

The following example illustrates the use of Section 1 and 2:

Suppose we are interested in studying the input protection on CMOS devices. The possible terms for finding applicable citations, we decide, would be "CMOS," "Input" and "Protection." Scanning Section I for these terms, we find by serendipitous association the following terms listed:

- CMOS B Series Versus A Series Input Protection
- CMOS Devices
- CMOS Protection Levels
- Input Protection
- Protection Networks
- Protection Techniques

When the terms are looked up in the index (Section 2), the following sixteen citations are accepted for study:

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HOW TO OBTAIN DOCUMENTS IN THIS BIBLIOGRAPHY

Each reference listed herein contains complete bibliographic information including the personal and corporate author with location. Where the document is available from one of the government document distribution centers, see information shown below. Other documents can be obtained from the original source (i.e., author, journal, society, etc.). Documents other than those published by RAC cannot be obtained from RAC.
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(703)321-8888

or if you are a government contractor, contact:

Defense Technical Information Center (DTIC)
Cameron Station
Alexandria, Virginia 22314
(202)694-7633
SECTION 1

ALPHABETICAL LISTING OF INDEX TERMS
ALPHABETICAL LISTING OF INDEX TERMS

ACCELERATED STRESS TESTING
ALI LIMITING GRIDS
ALI-LIMITED ENHANCED-JET
AL-SI02-SI CAPACITORS
ANNEXING
ANTISTATIC AGENTS
ANTISTATIC AGENTS, LUBRICANT AND BEARING DAMAGE
ANTISTATIC CONTAINERS
ANTISTATIC EQUIPMENT
ANTISTATIC FOOTWEAR
ANTISTATIC GARMENTS
ANTISTATIC LAMINATION (KGS 3600)
ANTISTATIC MATERIALS
ANTISTATIC MICROFOAM
ANTISTATIC NYLON (KGS 2400)
ARC GAPS
ARC POTENTIALS
ATOMICIZER
AUTOMATIC MACHINES
AVAILANCHE INJECTION
BAGS
BIMOS
BIPOLAR IC
BIPOLAR MICROCIRCUITS
BIPOLAR SEMICONDUCTORS
BIPOLAR TRANSISTORS
CABLE TRANSIENTS
CAPACITOR DAMAGE
CARBON BLOCK
CARPETING, STATIC GENERATOR
CASE HISTORIES
CHARGING MECHANISMS
CLEAN ROOMS
CLEANING SOLVENTS
CLOUD PHYSICS THEORY
CMOS 1K RAM (6518)
CMOS AND GATE (40018)
CMOS B SERIES VERSUS A SERIES INPUT PROTECTION
CMOS DESIGN PRECAUTIONS
CMOS DEVICES
CMOS FLIP-FLOP (4013A)
CMOS (4011A)
CMOS NAND GATE (4011A)
CMOS NOR GATE (40111)
CMOS NOR GATE (4001)
CMOS NOR GATE (4002)
CMOS NOR GATE (TP4000)
CMOS OPERATION
CMOS PROTECTION LEVELS
CMOS RELIABILITY
CMOS SHIFT REGISTER (4015A)
CMOS SHIFT REGISTER (4021A/B)
COMPUTER ANLYSIS
COMPUTER DATA LINES
COMPUTER FACILITIES
COMPUTER SIMULATION
COMPUTER SYSTEMS
CONDUCTILE
CONDUCTIVE ADHESIVE
CONDUCTIVE CARBON BLACKS
CONDUCTIVE COATINGS
CONDUCTIVE CONTAINERS
CONDUCTIVE CUSHIONS
CONDUCTIVE FILAMENTS
CONDUCTIVE FLOORS
CONDUCTIVE MATERIALS
CONDUCTIVE ORGANIC SURFACE COATINGS
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CONDUCTIVITY
CONTAINER MARKING
CROW/BARS
CRYOCENIC COOLANTS, STATIC GENERATOR
ALPHABETICAL LISTING OF INDEX TERMS

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DATA COMPARISON
DC MODULE DEVELOPMENT
DESIGN CONCEPTS
DESIGN INDUCED MECHANISMS
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DEVICE DEGRADATION
DEVICE GEOMETRY
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DIELECTRIC BREAKDOWN
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DIODE, PIN
DIODE, SCHOTTKY BARRIER
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ELECTRIC DISCHARGE TUNNING
ELECTRIC SHOCK ELIMINATION
ELECTRICAL NOISE
ELECTRICALLY CONDUCTIVE PAINT
ELECTROMAGNETIC EFFECTS
ELECTRO-EXPLOSIVE DEVICE HAZARDS FROM ESD
ELECTRO-EXPLOSIVE DEVICE PROTECTION AGAINST ESD
ELECTRO-HEATNO-MIGRATION
ELECTROSTATIC ANALYZERS
ELECTRO-TERMAL MODEL
EMI SUSCEPTIBILITY
EMI SYSTEM COMPATIBILITY
EMI TESTING
EMI/RFI SHIELDING
EMP DAMAGE
EMP DATA BASE
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EMP HARDENING
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EMP THEORETICAL MODELING
EMP TO ESD CONVERSION
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PULSE POWER TESTING OF MICROCIRCUITS.

Failure analysis of microcircuits subjected to high current transient pulses shows the principal cause of failure to be junction shorting. Thin film resistors are especially susceptible. Current and thermal profile analyses do predict the required energy to cause burnout. Metallization burnout is a function of current density for 200 msec pulses but depends more on the thickness of the SiO\textsubscript{2} passivation at longer pulse widths.

04834

ELECTRICAL OVERSTRESS FAILURES IN SILICON DEVICES.

Experimental evidence is used to substantiate a proposed mechanism of overstress failures. The mechanism is considered to be a migration of liquid along a line determined by crystal and electric fields. Graphs are shown showing the relationship between voltage and electrode spacing. Oxidation temperature is identified as a factor that affects sensitivity, higher temperature oxidation providing devices with higher resistance to surface zaps.

10000

Domingos, H. (Clarkson College of Technology, Potsdam, NY).
ELECTRO-THERMAL OVERSTRESS FAILURE IN MICROELECTRONICS.

Failure of microelectronic circuits caused by electrical overstress has been investigated theoretically and experimentally. Computer calculations on heat flow in silicon structures have pointed out the necessity of using temperature-dependent thermal constants for silicon. The effect of surface layers and power distribution on the peak temperature in silicon devices under transient conditions has been investigated.

Integrated circuits representing several fabrication technologies from several different manufacturers were pulsed to failure over pulse lengths from 100 nanoseconds to 10 milliseconds. The threshold power per unit area to produce permanent damage was found to vary by a factor of 20 among the parts tested. Peak temperatures to initiate current constriction were estimated to be 1000-1200°C.

MOS/LSI CIRCUIT DESIGN: DESIGNING-IN RELIABILITY.
IEEE - 10th Reliability Physics Symposium, 1972, pp. 36-41.

The solution to the need for extensive burn-in and temperature cycling calls for the circuit designer to "design in" product reliability. By "designing-in reliability" is meant establishing reliability by design and fabrication with appropriate experimental monitoring. This is not a novel concept by any means but all too often it is forgotten when the topic of reliability is discussed. The application of this concept in MOS circuit design requires an understanding of the tools available to the designer and their relative importance and how they affect the MOS circuit design.

Ebel, G.H., and H.A. Engelke (Singer-Kearfott Division, Wayne, NJ).
FAILURE ANALYSIS OF OXIDE DEFECTS.

There have been many good papers presented on various failure analysis techniques for studying oxide defects. This paper will review some of these and will describe, in detail, the application of nematic liquid crystals to the problem of locating the failure sites in oxides.

ELECTROSTATIC GATE PROTECTION USING AN ARC GAP DEVICE.

An ideal MOS protection device should respond to very fast and very slow rise time pulses and be able to short the input to ground before damage to the gate can occur. In general, all failures occur where the gate oxide overlaps the source or drain. The field plate protective diode by itself affords no protection to fast rise time pulses because of its connection in parallel with the input gate.

An arc gap is formed by locating the bonding pad 2.0 mils from a ground metallization ring encircling the chip. The ambient package atmosphere will support a low impedance gaseous discharge from pad to ground.
10792

Kennan, W.F., and D.M. Smith (Texas Instruments Inc., Dallas, TX).

PULSE POWER STUDIES OF HARDENED MICROcircuits

The effects of large amplitude transient pulses on radiation tolerant integrated circuits was investigated. Two distinct burnout mechanisms were discovered to exist, diode failure and resistor burnout. Both mechanisms were investigated independently by test structures to measure the influence of processing variations on the failure levels.

10839

Viele, A.A. (IBM, Manassas, VA).

A FAILURE ANALYSIS TECHNIQUE FOR LOCATING THE FAIL SITE IN MOSFET (LSI) LOGIC CHIPS WITH SPUTTERED SILICON DIOXIDE PASSIVATION.


Failure analysis of MOSFET chips with sputtered SiO₂ passivation must be preceded by the removal of the passivation layer to allow probe contact. The electrical integrity of the chip must be maintained to locate the fail site by signal tracing. Mechanical removal of the SiO₂ passivation has a greater success. The chip is removed from the C-DIP by melting the eutectic or by polishing away the backside ceramic. Chips are removed from ceramic controlled-collapse connection (C-4) packages by etching the solder pads in a 5:1 solution of acetic acid/hydrogen peroxide, then rinsed in DI water, or as recommended mechanically by cutting the C4 pads on all sides of the chip. Parallel polishing in a syntron vibromat using a slurry of aluminum oxide powder (.05 micron) and DI water down to the aluminum surface removes the SiO₂. Even polishing can be facilitated by coating areas of excess polishing with fingernail polish. Electrical analysis isolates the failed circuits and signal analysis characterizes the failure mechanism. Physical analysis confirms the damage location.

10841


TECHNIQUES IN FAILURE ANALYSIS OF MOS DEVICES

Failure analysis of gate oxides of MOSFET devices is discussed using a copper decoration and plating technique. Static discharge failures can be readily identified while subtle gate failure (submicron) from leakage and stress testing shorts require copper decoration to identify the physical appearance of the defect site. Solutions of NH₄F (40%, 4 parts) HF (48%, 1 part) and glycerine (2 parts) are used to remove glass passivation layers; also HNO₃ (70%, 1 part) HF (48%, 5 parts) and glycerine (10 parts). Lands are opened using capacitive discharge. Aluminum is etched away using a standard H₃PO₄ - HNO₃ - CH₃COOH-H₂O solution. Poly-silicon gates are removed using an etch of 20 parts HNO₃ and 1 part HF. A displacement solution of 2% CuSO₄ and 28% HF with a high intensity lamp locates conductive paths through the gate oxide and where gate silicon is exposed. Regions of defects are analyzed using SEM analysis. To avoid etching any oxide a standard electroplating solution of...
CuSO₄ and H₂SO₄ can be used. Pinholes in oxides, surface pits in gate region, Al₂O₃ formation in gates, single mounds and raised plateaus on oxide surface can be detected.

Jones, W.K. (Charles Stark Draper Laboratory, Cambridge, MA).
PLASMA ETCHING AS APPLIED TO FAILURE ANALYSIS.
IEEE - 12th Reliability Physics Symposium, 1974, pp. 43-47.

Failure analysis is discussed using a carbon tetraflouride plasma etch. The CF₄ is excited to plasma by RF energy in a vacuum of .7 torr. Helium is used to control the reaction as it is viewed through a sapphire viewer under a stereomicroscope at 150x magnification. Prior to complete removal the subpassivation aluminum has a green yellow tint, while bonding pad metallization is metallic in appearance. Backgrinding and polishing with final plasma etch will reveal the underside of metallization.

Examples given of the use of optically controlled plasma etching are: (1) removal of passivation for SEM analysis; (2) backlapping of bipolar devices; (3) thin-section for TEM analysis of nichrome fuses.

A MODEL FOR THE FAILURE OF BIPOLAR SILICON INTEGRATED CIRCUITS SUBJECTED TO ELECTROSTATIC DISCHARGE.

A mathematical model to predict ESD voltage thresholds is presented. Device failure occurs as a result of emitter-base junction degradation caused by electrical overstress. The degradation is manifested as a lowered breakdown voltage or higher reverse leakage current. The charges may come from a human body or the device itself. The resulting current of discharge is an exponentially decaying pulse. The failure is deemed to have occurred when the local power density causes the temperature to melt the semiconductor. The threshold level is a function of the current path cross section area, not of the junction area. The total power dissipated is the expression P=Vₐ+RₐΔV (Vₐ = junction drop and Rₐ = junction resistance). The current path is from the edge of the emitter to the base contact. Its area is emitter length times base junction depth. The power density vs pulse length is plotted to show good correlation with the Wunsch-Bell plot.

Freeman, E.R., and J.R. Beall (Martin Marietta Corp., Denver, CO).
CONTROL OF ELECTROSTATIC DISCHARGE DAMAGE TO SEMICONDUCTORS.

A study was done on the failures of three devices. The first, a 2N3970 N-channel FET, suffered a degraded reverse breakdown when subjected to ESD pulses of 6000v. The second, a 2600 internally compensated amplifier, suffered a shorted MOS compensation capacitor when subjected to ESD pulses. The third example, a 54L04 hex inverter low power TTL circuit, experienced phase-splitter transistor failure mode subjected to ESD pulses of 2500 to 3000v. Facilities were examined and verified the presence of electro-static charges in excess of the levels necessary to produce failures in the laboratory.

Himmel, R.P. (Hughes Aircraft, Culver City, CA).
THE EFFECT OF STATIC ELECTRICITY ON THICK FILM RESISTORS.
Insulation/Circuits, September 1972, pp. 41-44.

The effects of static electricity in the manufacturing process, packaging and use of thick film resistors is analyzed. Thick film resistors' sensitivities are related to resistivity which in turn is directly related to the materials used in manufacture. Isolated metal particles take part in the conduction process through the breakdown of dielectrics between particles. The clean room conditions of manufacturing often result in high static charge levels. Elimination of these charges may be facilitated by special precautions. The use of protective packaging materials is encouraged.

RELIABILITY EVALUATION OF C/MOS TECHNOLOGY IN COMPLEX INTEGRATED CIRCUITS.

The objective of this study was to investigate reliability of small and medium scale CMOS integrated circuits. Four manufacturers' type 4011A Quad 2-input NAND gates and three manufacturers' type 4015A dual four stage static shift registers were chosen as test vehicles. Only Manufacturer A's product was intended for MIL-M-38510 end use.

Results of pulsed power burnout testing of the Fairchild 9046 quad dual-input NAND gate and the Amelco 6041 three input NAND gate showed the circuits to be vulnerable to junction burnout for pulses of less than 100V and pulse widths on the order of 100 nsec. Calculations based on Wunsch-Bell junction burnout theory showed good agreement with experimental results. Sample calculations are given.


The dielectric breakdown of SiO₂ is studied using a thin metallization. The dielectric breakdown results in removal of metallization in the area of breakdown. Positive plate voltages resulted in anisotropic removal of metallization regardless of silicon dopant. Negative plate voltages result in irregular metallization removal. With positive field plate potentials and p-type substrate the anisotropic breakdown regions were square with smooth edges. The anisotropy is explained by hot electron conduction in the presence of a large radial electric field. Slow-high field instability also resulted in aSi-SiO₂ structural breakdown enhanced at lowered temperatures. A steady state current was observed and attributed to the tunneling of electrons in the presence of field plate voltages well below the point of instability. The instability results when the production and trapping of holes dominates over recombination caused by electron tunneling from the silicon substrate into the conduction band of the oxide.


This paper shows how CMOS integrated circuits can be protected against electrical transients originating from nuclear explosions, static discharge, etc. First, the causes of transient failures are determined and then analyzed. Next, a wide range of protection devices are designed and evaluated. Finally, complete transient hardened logic gates are fabricated and tested to prove the feasibility of EMP hardened CMOS circuits.


The control and elimination of static discharge in the work area is discussed. The human body is represented in a capacitive discharge model. The degradation to a 2N4118A varies according to the resistance in series with the human discharge. A transient voltage detection system is used to monitor ESD. The peak voltages generated by operators occurred when an operator lifts her feet or increases the static charge by gliding in a roller chair. Conductive shoes on a conductive floor can limit static voltages to as low as 50 volts. Increased relative humidity above 45% can also reduce static levels. Spray cleaning increases the electrostatic potential. Wrist straps are shown to be impractical. Conductive floor, chair and shoes all help to reduce static voltages as do conductive packaging, table tops and grounded soldering tips.


The electromagnetic vulnerability data needed to determine the effects of high power microwave signals on solid state components involves testing 2N5179 and 2N918 transistors using 240mhz RF single pulse signals. Physical analysis of the 2N5179 revealed emitter base shorting.

Theoretical predictions of circuit failure in an Electromagnetic Pulse (EMP) environment require a knowledge of failure levels for each component of the circuit due to surge voltages or currents. For most circuits, the semiconductor devices are the weakest elements with respect to such failure. This paper presents the results of an extensive experimental program to determine pulse power failure levels of semiconductor junctions. Approximately 80 different types of silicon diodes and transistors were studied with variations in junction areas for 10⁻⁴ to 10⁻¹ cm² and with widely varying function geometries. Power levels of up to two kilowatts, with time durations of 0.1 to 20 microseconds, were applied to semiconductor junctions in both forward and reverse polarity modes. A semi-empirical formula, based on experimental data and on a simple thermal failure model is given. From the formula one can make order-of-magnitude estimates of the failure level as a function of pulse length for many silicon diodes or transistors whose junction area is known.


The results of a new study into the high voltage sensitivity of this "new" generation of resistor materials is reported here. In this study, thick-film resistive pastes from five manufacturers were printed, fired, and tested for sensitivity to electrostatic discharge. The results of the tests indicate significant change from the materials previously tested, with an order of magnitude reduction in resistor sensitivity in many cases.


Packaging and handling precautionary measures that should be with ESD devices from Receiving to Shipping are described. Anti-static equipment needed at the work station is also identified. Advantages and disadvantages of different materials and equipment are discussed as well as the results of an evaluation on ionizing air blowers.

Trigonis, A.C. (Jet Propulsion Laboratory, Pasadena, CA). ELECTROSTATIC DISCHARGE IN MICROCIRCUITS DETECTION AND PROTECTION TECHNIQUES.
the thickness of the oxide film between the resistor and silicon substrate (0.5-1.5 micrometer). The FV depends on the resistor geometry, substrate material, and post fabrication annealing of the resistors. The most commonly used resistor geometry is adequate for use on ICs. The most dramatic change in FV obtained in the study was for resistors formed on glass substrates. The FV was reduced by almost a factor of 2 for 0.1 microsecond pulses over that of resistors on Si substrates.

Post fabrication annealing resulted in marked increases in FV for each material for the 0.1 microsecond pulses but had diminishing effects for 1.0 and 10 microseconds. Annealing for times greater than 60 minutes or temperatures greater than 470°C did not result in important further increases.

12666

Mykkanen, C.F. (Honeywell).
ESD (ELECTROSTATIC DISCHARGE) CONTROL UPDATE NO. 1.

This component comment addresses ESD protective work surfaces and floor surfaces. The advantages and disadvantages of pink poly and melamine work surfaces are discussed. Test results of charge dissipation is given on the two work surfaces. Various types of floor surfaces are described along with an assortment of floor polishers and cleaners.

12686

Walker, R.C., and H.C. Rickers (IIT Research Institute).
SEMICONDUCTOR ELECTROSTATIC DISCHARGE DAMAGE PROTECTION.

ESD is generated upon the contact of two dissimilar materials. Contact then separation results in the retention of charges. The magnitude of the charges generated depends on the ranking of materials in the triboelectric series and the intimacy and duration of contact. Fast, repetitive contact increases charge accumulation. Electronic semiconductor devices are particularly susceptible to ESD because of the catastrophic damage which results upon contact. Metal gate MOS devices are unusually susceptible. As a result of this susceptibility input protection circuitry has been devised and is successful at low limits of ESD. Failure analysis should be used whenever ESD damage is suspected. Failure duplication caused by ESD overstress can be used to confirm ESD damage.

Precautionary measures to prevent ESD damage include the identification of electrostatic sources using a noncontacting electrostatic voltmeter, humidity control, ionized air and protective clothing can all be used to eliminate the source of ESD.

12728

HYBRID PROTECTIVE DEVICE FOR MOS-LSI CHIPS.

Several structures that can be used to protect MOS-LSI chips against electrostatic discharges (ESD) are examined experimentally to determine some of the possible specification tradeoffs that result in improved overall performance. It is shown that by using structures able to withstand larger energy discharges at the expense of their voltage-clamping characteristics, higher overvoltages can be handled. Additional protection is possible by incorporating a spark-gap device on the chip-carrying module. Conditions under which this hybrid combination is effective are examined.

13210

Li, S.P., E.T. Bates, and J. Maserjian (Jet Propulsion Laboratory, Pasadena, CA).
TIME-DEPENDENT MOS BREAKDOWN.

A general model for time-dependent breakdown in metal-oxide-silicon (MOS) structures is developed and related to experimental measurements on samples deliberately contaminated with Na. A statistical method is used for measuring the breakdown probability as a function of log time and applied field. It is shown that three time regions of breakdown can be explained respectively in terms of silicon surface defects, ion emission from the metal interface, and lateral ion diffusion at the silicon interface.

13265

Jowett, C.E.
STATIC ELECTRIFICATION HAZARDS IN MICRO-ELECTRONICS PRODUCTION.

Three criteria exist for the existence of an electrostatic hazard: (1) charging of material or nearby structures; (2) slow, small leakage of such charge; (3) ignition, explosion, or damage by ensuing sparks of material. Relative humidity and ionization of
the local atmosphere decrease the relaxation time for stored charge. Warning devices include goldleaf electroscopes, neon lamps, electro-static voltmeters, electrometers and field mills. The magnitude and polarity of the charge acquired by a powder or its container may depend on: (1) the moisture content of the atmosphere and the powder; (2) the particle size distribution; (3) the velocity with which the powder moves or impinges on surfaces; (4) the state of surfaces on which the particles impinge. Ignition of combustible gases requires a minimum spark energy and voltage.

13309

RELIABILITY CONSIDERATIONS FOR COS/MOS DEVICES.

CMOS low-power digital logic finds many applications because of its high volume manufacturing and inherent reliability. All CMOS devices are susceptible to ESD. About 50% of devices fail as a result of ESD damage, overstress or application problems. An input protection network has been devised to protect gate oxides against ESD up to 1000v. Zener diodes at the output pins can clamp the voltage to safe levels. Latchup can occur when operating above maximum ratings. Bias life tests are used to accelerate chip related mechanisms sensitive to time, temperature and voltage. Leakage mechanisms respond to bias life test. Operating life tests are switching in nature and relate to the quality of the chip process. Real time controls are accelerated tests designed by reliability and application engineers working cooperatively. CMOS devices of lower junction temperatures will provide lower failures than TTL. To detect ESD a curve tracer check is made in the area isolated by electrical test. Overstress failure is internally seen as a burned or open metallization path. Gate oxide shorts are the most common failures modes for MOS devices. They may occur in weak spots anywhere, though in a perfect MOS transistor they would occur at the four corners of the gate area. Moving ionic charges under the gate area can reduce or increase threshold voltages of ESD. Bias applied to the gate metal can cause shorts from source to drain by ionic redistribution. HTRB tests can be used to check for contamination.

13310

CMOS RELIABILITY.

This report, which presents new data on the reliability of CMOS integrated circuits, is divided into four major sections. The first section is a review of background information on MOS integrated circuit reliability, the second section presents new experimental results of comprehensive studies of the reliability of RCA CMOS (or COS/MOS) integrated circuitry, the third section is a discussion of application considerations and outlines RCA electrical specifications for COS/MOS integrated circuits, and the fourth section is a review of the effects of some of the trends occurring in the CMOS industry. Some generalizations and conclusions concerning CMOS reliability are included in the fourth section.

13319

Anon. (NASA, Langley Research Center, Hampton, VA).
ELECTROSTATIC-DISCHARGE DAMAGE TO SEMICONDUCTORS.

Electrostatic discharge damage is responsible for a large number of failures in semiconductor devices. The devices examined, a J-FET, an internally-compensated op-amp and a TTL hex inverter, exhibited degradation in reverse breakdown voltage. The op-amp experienced latch-up at 80% of supply voltage. A hybrid circuit in the TTL hex inverter failed to respond to a digital command. All facilities where failures were being experienced had ESD levels in excess of those needed to produce failures. Semiconductors can be tested for ESD using a 150-200pf capacitor and 1.5k to 2k ohm resistor model. ESD can be controlled by eliminating generators and relieving charges.

13387

Van Lint, V.A.J. (Mission Research Corp., La Jolla, CA).
MECHANISMS OF SEMICONDUCTOR JUNCTION BURNOUT.

Mechanisms of semiconductor junction burnout are reviewed with particular emphasis on parameters controlling variation in energy to achieve second breakdown and device damage. Stabilizing effects promoting uniform current distribution and destabilizing effects promoting filamentary currents are identified. Those destabilizing factors involving thermal changes lead to thermal-mode second breakdown. They include resistivity peak and reverse saturation current. A nonthermal destabilizing effect at high injection conditions leads to current-mode second breakdown. The
13672
Dunn, R., and H.Y. Ho (Xerox, El Segundo, CA).
INPUT PROTECTION NETWORKS ON MOS DEVICES.
Rept. No. CTFT-77-6511, Components and
Packaging Tech. A2-29/Ext. 1730-3303, December

The ESD failure levels for MOS devices of
various manufacturers are discussed. A
failure incidence of 1% on the factory floor
occurs with MOS devices having an input
protection capability of 500-800v. MOS
devices with protection of 1000-2000v had no
failures. With multiple sources, vendors of
devices with 1000-2000v are preferred. Humans
are the primary source of ESD. Partially
degraded networks will often continue to
deteriorate and become hard failures. Overall
test procedures verify the worst stress mode
of charge, isolate particularly susceptible
inputs and extend data base to several date
codes and package types.

13717
Pancholy, R.K. (Rockwell International,
Anaheim, CA).
GATE PROTECTION FOR CMOS/SOS.
IEEE - 15th Reliability Physics Symposium,
Catalogue No. 77CH1195-7PHY, April 1977, pp.
132-137.

Pulse-power burn-out test results on SOS
resistors, high voltage diodes, and thermally
grown gate oxides are described. For SOS
diffused resistors, the failure power per unit
area ranged from 4 x 10^6 to 3.7 x 10^6
watts/cm^2 for pulse widths of 100 nanoseconds
to 10 microseconds. The failure mechanism is
heat-induced resistivity variation resulting
in formation of low resistivity hot spots or
filaments. High voltage diode and resistor
combinations extended the failure voltages to
325 volts for 100 nanoseconds pulses.

13718
Minear, R.L., and G.A. Dodson (Bell Telephone
Laboratories, Reading, PA).
EFFECTS OF ELECTROSTATIC DISCHARGE ON LINEAR
BIPOLAR INTEGRATED CIRCUITS.
IEEE - 15th Reliability Physics Symposium,
Catalogue No. 77CH1195-7PHY, 1977, pp. 138-
143.

Electrostatic Discharge (ESD) can easily
damage bipolar integrated circuits. "Second
breakdown" of npn transistor emitter-base
junctions is a common failure mode. No
external emitter connection is needed for this
to occur. ESD current paths, physics of ESD
failure, and design concepts for improved ESD
resistance are discussed.
Hickernell, F.S. (Motorola, Scottsdale, AZ).
DC VOLTAGE EFFECTS ON SAW DEVICE INTERDIGITAL
ELECTRONICS.
IEEE - 15th Reliability Physics Symposium,
Catalogue No. 77CH1195-7PHY, 1977, pp. 144-
148.

The transducer electrodes of high
frequency surface acoustic wave (SAW) devices
can be damaged by dc voltage transients as low
as 150 volts. Controlled dc pulsed voltage
levels applied to SAW device aluminum
interdigital electrodes on piezoelectric
quartz and lithium niobate have served to
define arc discharge and surface fracture
conditions affecting device performance. It
is recommended that high frequency SAW devices
be handled as voltage sensitive parts.

Gallace, L.J., and H.L. Pujol (RCA/Solid State
Division, Somerville, NJ).
THE EVALUATION OF CMOS STATIC-CHARGE
PROTECTION NETWORKS AND FAILURE MECHANISMS
ASSOCIATED WITH OVERSTRESS CONDITIONS AS
RELATED TO DEVICE LIFE.
IEEE - 15th Reliability Physics Symposium,

All CMOS devices, which are composed of
complementary insulated gate field effect
transistors, IGFET's, are susceptible to damage
by the discharge of electrostatic energy
between any two pins. The gate oxide
breakdown voltage of a CMOS device is
typically 80v. Series resistors and zener
diodes can clamp voltages to safe levels. Gate-oxide shorts are the most common failure
mode for MOS devices. Theoretical rupture
points would be located at any one or more of
the four corners of the gate area. In
practice, voltages may puncture a weak spot
elsewhere. A circuit capacitance of 100
picofarads and series resistance of 560 ohms
is used in equivalency to the human body
discharge circuit. Life test showed that
leakage level associated with the input
protection diodes can degrade with operating
life especially those prestressed to low level
simulated ESD.

Anon. (NASA, Lyndon B. Johnson Space Center,
Houston, TX).
SAFE HANDLING PRACTICES FOR ELECTROSTATIC
SENSITIVE DEVICES.
MSC-16642, Fall 1977, 19 pp.

The primary consideration for all
electrostatic precautions is that they must be
continuous. Static sensitive devices shall be
identified with tags and/or labels. Personnel
must follow static precautions at a static
free work station including grounding of all
equipment and using uninsulated metal hand
tools. Plain plastic trays shall not be used
for unprotected devices. Shunting clips shall
not be removed until the item is in a wired
circuit or receptacle. Notes on design
drawings will include static warnings. DC
voltages will be applied before signal
voltages when testing MOS and CMOS devices.
Antistatic polyethylene shall have its
properties protected from degradation by
immersion in water.

Antinone, R.J. (BDM Corp., Albuquerque, NM).
SPECIFICATIONS FOR MICROCIRCUIT ELECTRICAL
OVERSTRESS TOLERANCE, VOL I.
Rept. No. RADC-TR-78-28, Contract No. F30602-
76-C-0308, March 1978, 139 pp.

During a literature search and survey,
two types of transients were identified as
being important in microcircuit applications. These are electrostatic discharge transients
resulting from handling and system transients
generated within a system or within the
environment in which it operates. It was
found that the static discharge transient
could be simulated by a decaying exponential
pulse with a short circuit time constant of
150 nanoseconds, delivered through a source
impedance of 1500 ohms. Provisions were made
for varying the peak amplitude of the pulse,
but a charging voltage of 1000 volts was found
to provide the best screening.

Further, it was found that the system
transients could be simulated by a decaying
exponential pulse with a short circuit time
constant of 10 microseconds, delivered from a
100 ohm source impedance. Provision was made
for varying peak voltage. Different
technologies require different charging
levels, but a level of 50 volts was found to
separate microcircuit types into sensitive and
non-sensitive categories.

A pulser having the capability of
delivering either the static discharge or
system transient simulation pulse was
fabricated. This pulser was used in subsequent
procedure evaluation and sample qualification
tests.

Singletary, J.B., H.O. Collier, and J.A. Myers
(BDM Inc., Albuquerque, NM).
SEMICONDUCTOR VULNERABILITY VOL. II.

This report presents, for a selected
group of semiconductor devices, pulsed power
burnout data sufficient to establish failure threshold curves. The failure curves were obtained from the experimental failure data using previously developed device failure models. This work is an extension and experimental corroboration of estimated pulse power failure levels obtained from two simple failure models which make use of device handbook parameters.

13986


This report provides an electromagnetic pulse vulnerability listing for a number of selected semiconductor diodes and transistors. The power required to cause failure was determined based on models verified experimentally. For diodes it was found experimentally that the PM junction is more vulnerable in the reverse polarity mode. For transistors testing showed the base emitter junction, in general, to be most vulnerable.

14026


This report presents the results of a program to expand and interpret the data base for EMP susceptibility of semiconductor components. The primary objective was expansion of the data base. Secondary purpose was to gain improved understanding of failure modes. Failure testing was performed on over 60 integrated circuit and 83 discrete circuit types. Specific tasks addressed were (1) IC failure modes, (2) components, (3) bulk resistance in discretes.

14075


Arc gaps have been used on MOS chips in conjunction with resistor, capacitor, and diode networks to provide protection against potentially damaging fast rise-time, high voltage pulses. Such pulses can occur due to equipment transients or electrostatic discharges during handling. There is little information in the literature on the operation of aluminum planar arc gap structures fabricated under standard MOS design and processing rules. A two-phase study was conducted to investigate in greater detail the use of such arc gap structures. The first phase had two objectives. The first was to identify improved arc gap structures with low ignition voltages and fast turn-on times. The second objective was to gain a better overall understanding of arc gap operation. The second phase of the study consisted of taking the glassivated arc gap structure identified as optimal in the first phase and incorporating it on a CMOS LSI logic test chip. The objective was to reduce the chip's susceptibility to damage by fast rise-time, high-voltage pulses.

14077


Static protective packaging materials must prevent damage to static-sensitive components from triboelectrically generated charges and also electrostatically shield them from the effects of charged objects. Protection of static-sensitive components from the two types of static charges by using protective bags, tote boxes and dip tubes is discussed.

14082


Major advances in processing are already resulting in very-large-scale MOS integrated circuits with increased packing density, higher operating speed, and lower operating power. However, the finer lines and thinner oxide layers of these new superchips will aggravate a problem that has plagued MOS manufacturers and users since the emergence of these devices: device failure from electrostatic damage. Fortunately, effective methods and materials for handling and packaging static-sensitive devices have been developed. For MOS devices (whether individual parts or mounted on printed-circuit boards), transpor-
cation in bags, tote boxes, or storage tubes made of special metallized film laminates or carbon-loaded plastics serving as static-protective materials is required. The use of older, military-specified materials has resulted in device damage and failure.


An investigation into the protection various aluminaized packaging materials provide microelectronic devices in radar RF environments was conducted. It was determined that packaging shielding materials could protect microelectronic devices in RF environments. The packaging materials used in the investigation are described along with their ability to protect devices from various RF sources.

Ignaczak, L.R. (Lewis Research Center, Cleveland, OH).

A self contained spark-gap arc generator has been developed to simulate the electrical noise from the discharge of a static charge. The arc potentials are variable from 3 to 15kv with the energy per arc .01 to .25 joules or greater. Application has been found in testing spacecraft components. Spacecraft operating in synchronous altitudes have been surface charged to 11000 volts.

Brown, W.D. (Sandia Laboratories, Albuquerque, NM).
SEMICONDUCTOR DEVICE DEGRADATION BY HIGH AMPLITUDE CURRENT PULSES. IEEE - Trans. on Nuclear Science, Vol. NS-19, No. 6, December 1972, pp. 68-75.

If the short duration, high amplitude current pulses produced by gamma radiation in a nuclear environment flow through semiconductor devices permanent damage may result in the form of a low impedance shunt across the device junction. The current required to initiate damage in the forward direction is 5 to 15 times that necessary to initiate damage in the reverse direction. The emitter base junction is most vulnerable.

The area used to calculate power density is the active emitter's sidewall area. Only a fraction of the sidewall area is involved for deep junctions. The emitter periphery plays a most important role in determining the threshold level of a device. Deeper emitter diffusions produce more tolerant devices.

Porter, D.C. (Boeing Co., Seattle, WA) and M. Bahan (U.S. Army Missile Research and Development Command, Huntsville, AL).

A plastic encapsulated 40 pin, 630 gate LSI PMOS circuit on a 30,000 square mil chip was introduced into commercial service in 1974. By 1977, 3.7 x 10^9 unit hours had been accumulated and a failure rate of 0.042%/1000 hours was demonstrated. Failure analysis was performed on 150 devices removed during the maintenance cycle with date codes spanning two years. One third were good units. Of the remaining, 55% were devices which had never worked properly and were sent to the field because they were not tested properly. Detailed autopsy efforts were completed on 70 units and no failures traceable to the packaging technique were encountered.

Frankel, H.C. (U.S. Army Electronics Research and Development Command, Fort Monmouth, NJ).

This report describes a Hybrid Microcircuit and Assembly Team (HMDTA) investigation to develop the relative vulnerability of various thick film materials to degradation by ESD. Test specimens of alumina substrates with 31 resistors mounted were subjected to Corona, Tesla, and Polyurethane sheet tests. Measurements were made to determine the relative influence of device factors to vulnerability. Factors considered were materials, geometry, and location on substrate. Material effects were compared for observable differences to determine the most susceptible configurations.
In the course of investigations over the past two years, the electromagnetic engineering department of Bell-Northern Research has reached a much better understanding of the static discharge process and how it affects equipment.

The Bell Northern research investigation explored the radiation aspect of the phenomenon in greater detail.

The electrostatic spark jumps right at the heart of the equipment and so is a sharp spike. The current and radiated field it creates, though extremely brief, can produce significant effects. They depend on the rate of change of voltage, not on the voltage directly.

Measurement probes had to be specially made to pick up the transient currents and radiated fields. As discharge current in a cabinet travels along its conducting frame it radiates energy. Other items such as cables add their own pattern. Both the electrical and magnetic components of these patterns were measured.

Radiation patterns can be contained using transient suppressing devices, shelf and rack grounding, and damage can be prevented by keeping sensitive circuit tracks away from structural or circuit members likely to carry large discharge currents.


The following are some of the stresses that will cause integrated circuit failures: radiation (alpha, beta, gamma), static electricity, vibration, power line transients, excessive hot or cold, temperature cycling, and moisture. Special conditions apply to each mode; an example is vibration. Bonding wires resonate at 30 to 50 KHz. The presence of such frequencies may cause this failure.


Generation of static electricity by movement of low conductivity fluids relative to each other causes the accumulation of hazardous electrical charges. This report discusses the origin and nature of electrostatic phenomena, gives methods for calculating their magnitude in practical engineering units and describes techniques for controlling and minimizing static electricity in process operations. Values for the dielectric constants, specific conductivities, and minimum ignition energies of various materials are presented.


For static protection techniques to be effective they must be applied at all times and places where electrostatic damage might occur. Simple demonstrations help to bring personnel to see the realities of static. Tape unrolled over an ash tray will pick up ashes, indicating a surface charge of 4000 volts. A neon bulb in a plastic bag will glow after being rubbed with a sweater (Anderson Effect). The point should be made that nonconductors generate charges, conductors pick them up and deliver.


Observed effects of ESD on JFETs included changes in the reverse breakdown voltages. The capacitance value of the discharge model influenced the voltage required to degrade the transistor. Repeated discharge pulses at voltages below the degradation level did not significantly degrade the device. Half of the JFETs showed a decrease in breakdown voltage with no significant change in the transconductance or pinch-off voltage.

Human operator-generated voltages were also measured. Peak generated voltages were observed at points where the feet of the subject partly or totally lost contact with ground plane. Conductive floors and spraying with low resistivity solvents helped to reduce environmental static.

The results of tests outlined herein will provide valuable information that will enable valid electrostatic sensitivity tests for explosives and also aid in explaining the variation of human skin resistance with applied voltage and in determining the depth at which the charge having most effect resides. The results will also enable the analysis of possible bodily dangers involved in discharges of this nature and give considerable insight into the RF response of the human body.


The occurrence of accidents involving electroexplosive devices (EED) has renewed interest in the static electric charge that can be accumulated and transferred by personnel. This monograph develops an electrical model to use in rough checks of EED sensitivity to personnel-borne charges: a series circuit of 500 pf capacitance and 5000 ohms resistance that can be charged to potentials up to 20 KV. It is shown that very sensitive EED's can be fired with charges developed by personnel and it stresses caution with respect to so-called insensitive types which may be susceptible in the pin-to-case mode. The study indicates that the hazard may be greater than anticipated and it is recommended that these limited studies be supplemented with additional investigations to furnish a firmer quantitative basis for action.


In almost every case of electrostatic discharge damage encountered in the electronic industry, the source of the static is everyday plastic, including synthetic textiles, which are, after all, spun plastics. CMOS devices, precision resistors and countless similarly static-sensitive components are destroyed or damaged daily by this simple but misunderstood phenomenon. Even when static is recognized as the principal cause of damage, most companies fail to envision the simplicity of proper protection. They often waste money on expensive "overkill" techniques, or ignore the problem as being too expensive to correct.
MOS input protection techniques are increasing diode size, using diodes of both polarities, adding series resistors and utilizing a distributed network effect.

Design precautions dictate avoiding crossunders beneath strips connected to external pins. Oxide thicknesses and the distances between contact edges and junctions should be carefully controlled. Transistors can be better protected by increasing the emitter perimeter adjacent to the base contact. Likewise "phantom emitters" incorporated by a second emitter diffusion shorted to the base contact add additional extrinsic base resistance ballast.

To avoid latchup in CMOS circuits, limit input current to 10 mA. For particularly sensitive CMOS devices, outputs should be isolated from cable lines via resistors and by clamping each line to VDD or VSS via high speed switching diodes.

In general all inputs and outside terminations must be protected via some circuit or device. All ESD sensitive items must be labeled as such and handled appropriately.

STC has initiated a wafer level oxide test that must be performed before the unit is packaged. Intel has found that testing of MOS devices with overvoltage proved more effective in eliminating potential failures than normal 125°C 168 hours burn-in. This was true, as explained, because the dominant failure mode on MOS was and still may be poor oxides. Anti-Static Air Cap designed to cushion as well as give anti-static protection to electronic components and materials has been introduced by Sealed Air Corporation. 3M has introduced a three layer film consisting of a conductive metallic outer layer, a middle layer of polyester film and a final inner layer of heat-sealable polyethylene film.

The primary consideration for all electrostatic (static) precautions is that they must be continuous. Just as a precision clean part must have a maintain cleanliness requirement for all operations, a static sensitive item must have a 'maintain static free' requirement from the original component manufacturer through final production assembly.

In the vicinity of unprotected static sensitive devices avoid activities which tend to be friction producing, such as putting on or taking off smocks, wiping feet, rubbing hands, etc. Develop the habit of first touching the grounded bench top before handling static sensitive items. All equipment used at a static free work station shall be grounded, such as soldering irons and tips, lead forming tool, test fixtures and lights.

Huntsman, J.R., and D.M. Yenni (3M, St Paul, MN).

COPIING WITH STATIC ELECTRICITY-PART VII
A NEW TECHNOLOGY IN TRANSPARENT STATIC PROTECTIVE BAGS.

Because of the intrinsic deficiency in antistatic polyethylene, Static Control Systems of 3M Company has developed a new packaging material to provide transparency and the shielding effectiveness more like that of a metallic conductor. It is unique in having very low surface resistivity (less than or equal to 10^4 ohm/sqcm) but very high volume resistivity (greater than or equal to 10^15 ohm-cm). It is a multilaminate sheet of three electrically distinct layers.

The humidity-independent conductive outer layer has a metallic coating providing a faraday cage-like protective shielding. The center layer is polyester, which provides good mechanical strength and puncture resistance. The inner layer consists of antistatic polyethylene which is heat sealable.

An ESD pulse in an antistatic polyethylene bag lasts 60-70 milliseconds and has a peak of 3000 volts. The pulse in a static shielding bag lasts just several microseconds with a peak of 75 volts.
Even with protection, problems can arise with MOS circuits. Soldering with an unisolated iron, wearing silk smocks and leaving pins unterminated increase the probability of discharge damage.

A noncatastrophic failure mode occurs when input pins are left open. For example control inputs such as recirculate for a shift register, that are left open may cause a device to be in the wrong operating mode if sufficient charge is accumulated to reach the input switching threshold voltage. The device would not necessarily be damaged but would appear to malfunction.


The radioactive static eliminator is a self powered ionizer of air molecules. The development of 3M brand radiating microspheres presents a convenient method of safely containing the isotopes. The microsphere is a ceramic bead in which the isotope can be absorbed, then permanently sealed. The size of these beads is very small, 20-80 microns in diameter.

The use of a radioactive neutralizer for a particular application depends on a number of considerations. Cost considerations are in favor of tinsel and wire brushes if a reduction of 3000 to 10000 volts is required. If a reduction of static charge from 5000 to 500 volts is required, then a radioactive system is a must.

Erickson, D. ANTISTATIC EQUIPMENT AND TECHNIQUES. Electronic Packaging and Production, February 1979, pp. 74-96.

Static electricity, also referred to as ESD (electrostatic discharge), has its real danger arise from the illusive "docility" of its nature. Static problems are unusual in that it is often more difficult to identify the problem than to solve it. One of the best instruments for identifying the nature of ESD damage is the SEM (scanning electron microscope).

Planning for minimizing static charges involves taking a look at all poor conductors that move. In practice there are often too many nonconductive materials involved directly or indirectly to ban all. Antistatic soldering/desoldering equipment and device carriers are available from a number of manufacturers. Conductive bags are often used for packaging protection. For the occasional requirement of antistatic coating, liquid immersion or sprays can be a practical answer. Conductive trays, containers and tote boxes help make static protection continuous. Complete static work stations are available also. Static clothing including smocks of various fiber construction and tools designed to reduce static damage are being offered in various styles. Portable work stations grounding kits complete the "arsenal".


There is no way to totally eliminate static sensitivity; but, following common-sense antistatic procedures do a lot to protect your circuits, increase yields, improve MTBFs and lower costs. First, test all components and devices for static sensitivity. If vendors perform satisfactory testing and certification, only spot-checking is necessary. Second, specify static-shielding packaging on all static-sensitive devices coming from outside sources. Third, counsel assembly/manufacturing personnel regarding types of devices that will require special static protection. Fourth, give anti-static measures publicity; keep reminding everyone you know that static is a problem and encourage protective measures. The solution is largely one of attitudes and work habits.


While some skepticism existed one or two years ago as to whether static charge is responsible for high failure rates, it is now an accepted fact that some MOS devices can be destroyed by less than 100v of static charge.

You can ground conductive materials but you can not ground nonconductive materials. As a result anything less than a complete safeguard system is only partial protection. Clothing is not the only nonconductive material that is brought into the work station area. Items such as plain plastic tote boxes, plastic work-order sleeves or covers, candy wrappers, etc., all have the capability of blowing or degrading static sensitive electronic devices.
Schreier, L.A. (Hughes Aircraft Company, Culver City, CA).

**ELECTROSTATIC DAMAGE SUSCEPTIBILITY OF SEMICONDUCTOR DEVICES.**

Devices were chosen for ESD degradation threshold testing on the basis of high failure rates in manufacturing environments. Critical electrical parameters were measured before and after each simulated ESD. A change of more than 10 percent of the specification was considered a failure.

In addition, devices were pulsed at 75 percent of the ESD degradation threshold and then subjected to burn-in. In most cases, the critical parameter change was dramatic. Device sensitivity ranged from 100V for MOSFET to above 3KV for JFET.

The data gathered on burn-in of devices suggests that there is no long term first-order degradation mechanism if ESD levels are kept below the ESD degradation threshold.

14980

Mendelsohn, A.

**TRANSIENT SUPPRESSORS.**

A transient is a brief voltage pulse or surge of current that can wreck havoc in milliseconds. It may cause slow degradation, erratic operation or catastrophic failure in semiconductors, insulation dielectrics and switch and relay contacts.

Combining or "staging" of protective devices can provide overall protection unattainable with one device alone.

Silicon avalanche diode suppressors can be effective alternatives to bulky selenium stacks used to protect SCR's triacs and diodes in solid state power control technology. Exhibiting extremely fast turn-on times these devices are available in a dozen voltage breakdown ratings between 500 and 1600 volts.

Tin, zinc, or bismuth oxide voltage dependent resistors (VDRs), often referred to as MOVs (metal oxide varistors), offer a cost effective means of dealing with high, medium, and low level transients. MOVs change resistance nonlinearly in response to applied voltage. A gradual deterioration in characteristics occurs each time a MOV conducts.

Prior to making an ultimate judgment on any given type of suppressor, a final analysis must take into account all parameters and the end product protection level desired.

14981

Williams, J.H. (General Dynamics, Pomona, CA).

**COPING WITH STATIC ELECTRICITY - PART VIII ELECTROSTATIC DAMAGE TO SEMICONDUCTOR DEVICES: CAUSES AND CURES.**

All components are static sensitive to some degree. The smaller the part, the less power it can dissipate and the more likely it is to be damaged by an electrostatic discharge.

Even now industry cannot agree on the most effective method to provide adequate protection. It frequently resorts to an expensive "overkill" practice or takes no action at all because it feels that the precautions are too expensive.

Industry experience with solid state devices has revealed numerous cases of actual or potential damage from static discharges. One of the more dramatic incidents occurred in 1964 when a polyethylene drape used as a dust cover for a Thor Delta third stage solid propelled rocket created an estimated 28000 volts as it unrolled and accidently ignited the rocket by inducing a charge on its igniter squib.

14982

Anon.

**COPING WITH STATIC ELECTRICITY - PART IX METAL FILM RESISTORS CAN BE ZAPPED BY STATIC ELECTRICITY.**

Some evaluation engineers are not aware that precision metal film resistors are subject to damage by static electricity, and they are shocked to discover the problem.

The zapping problem occurs during sampling where some resistors are pulled out of the lot for testing. The technician walks across the room, building up a static charge on his body. Upon touching the resistor, he zaps it and it is no longer a precision film resistor with a stability of .1%. Instead, it is now a film resistor with a .2-1% tolerance.

14983


**COPING WITH STATIC ELECTRICITY - PART X.**

Most MOS devices contain zener diode protection to ground or substrate. Zener diodes can bleed off excess static voltages, but there is normally no protection on output pins.
To say that some ICs are not susceptible to static discharge is unrealistic, for there is a potential that can damage any chip. The characteristic of a static charge to spread itself thin (cover all conducting surfaces) makes it a problem. The solution then is to establish a chip or board ground and ground yourself to it before work starts.

Some of the body characteristics that influence voltage levels are the dielectric constants of the clothing worn and the skin moisture level of the body.

14984

Shelton, S. (Simco Company, Lansdale, PA).
COPING WITH STATIC ELECTRICITY, PART XI WHY USE ANTISTATIC GARMENTS?

Antistatic garments generally are somewhat conductive in nature and are normally worn over street clothing. In effect, they provide a type of "screen" to aid in reducing strong static fields which could induce damaging static charges on nearby electronic devices. The antistatic garment should cover all static generating clothing where possible and should at some point make contact with the person's body to provide a resistive path to ground.

A strong static field may be associated with charged clothing and radiates from it. This strong static field can induce an opposite charge on an isolated object within the field without any point or direct contact with the person's charged clothing. As long as this person remains in proximity to the object it will remain charged.

The individual being of different potential than the component causes a static discharge which may either degrade or destroy the sensitive device.

14985

Johnson, W.D. (Hughes Aircraft Company, Los Angeles, CA).
COPING WITH STATIC ELECTRICITY - PART XII STATIC AWARENESS TRAINING FOR FACTORY PERSONNEL.

Product reliability and production costs are directly affected by static electricity. Static controls will improve product reliability and reduce production rework or scrap. "Static Safe" ESD protection must be maintained at all times. Personnel must maintain all static free requirements for sensitive devices from the original source of manufacture through all assembly operations to point of use.

All work stations must be essentially equipped with an anti-static conductive work surface, conductive wrist band and operator ground straps, "static safe" approved label, caution signs, caution labels, static free shop carriers and approved soldering irons. Conducting materials, handling containers and packaging supplies are also necessary.

14986

Klein W.G. (United Technical Products, Westwood, MA).
STATIC ELECTRICITY: PROBLEMS AND SOLUTIONS IN COMPUTER FACILITIES.
8 pp.

Although static problems are well-recognized, their causes are not widely understood. Floor coverings (particularly carpeting) and the relative humidity are known generally to play important roles.

The matter of degree of homogeneity of conductivity is very important as most practical permanent antistatic systems involve a two-phase approach in which a small amount of discrete conductive material is added to a textile system which is otherwise nonconductive. An example of this is the introduction of conductive filaments at a predetermined spacing throughout a carpet. It has been found experimentally that conductive elements with a resistivity on the order of 108 ohms/cm constitute good electrostatic conductors.

One frequently hears requirements for floor coverings having static property less than 1KV or even .5KV. It is the opinion of the author that, in the absence of a specified shoe, no floor covering material can under dry conditions permanently assure performance below the 2KV level.

14987

BASIC ELECTRICAL CONSIDERATIONS IN THE DESIGN OF A STATIC-SAFE WORK ENVIRONMENT.

Static damage of components is fast becoming one of the most significant problems plaguing the electronics industry. Technological advances in IC manufacture such as ion implantation, ion beam milling and electron beam direct current lithography all make possible devices with higher circuit densities, higher unit performance and quite often higher static susceptibility.

Fortunately, the problems associated with static charges in the electronics environment can be controlled. To accomplish this, programs must be instigated throughout the manufacturing cycle to increase static
awareness in all personnel who handle static sensitive devices. Once educated, personnel must be provided with the proper equipment to implement these techniques of static control. At the work bench this includes conductive table mats, conductive wrist straps, conductive floor mats and ionized air.

The purpose of this paper is to discuss the basic electrical requirements of the conductive components of this system in relation to the individual function each provides.

Sinclair, R.E. (Lockheed Aircraft, Sunnyvale, CA).

SEMICONDUCTOR CIRCUIT FAILURE AND PROTECTION IMPLEMENTATION SCHEMES.


The transient pulse failure mechanism in semiconductor devices and thermal models for heat generation and transfer within the device are described. From these, formulas and criteria are developed to enable calculation of the critical energy for permanent damage. This is the applied pulse energy necessary for device failure. From these results, device protection criteria are developed. Protection resistor values can be calculated which permit protection of devices for specified critical energies and applied energy levels.

Keller, J.K. (Lehigh University).

PROTECTION OF MOS INTEGRATED CIRCUITS FROM ELECTROSTATIC DISCHARGE.

Presented to the Graduate Committee of Lehigh University, 1976, 50 pp.

One of the primary purposes of this paper is to present a realistic model of the human body for static electric protection purposes. It is extremely important that the model be highly correlated to actual human characteristics. It is generally agreed that the best model for the human body is that of a charged capacitor, a series resistor and a relay type switch. Human body capacitance can be related to the subject’s height and other physical parameters such as shoe thickness and area. Likewise human body resistance varies for different conditions (humidity, skin conditions, etc). Extensive study indicates that the human body “switch” bounces several times before making final contact. In simulated testing a high voltage relay was discovered to closely resemble the human discharge.

Protective input resistors, when fabricated from non-diffused material so that no parasitic diode results, are of little value. To be effective they must be combined with a device that will prevent the gate voltages from reaching destructive levels. Fabrication of input protection diodes must be such that the reverse breakdown voltage of the diode is less than that of the gate oxide. Thick oxide, punch through, gated punch through and field plate diodes are all designed to do this. Spark gaps are also useful precautionary devices although certain precautions with nonconducting encapsulants must be taken.

The most versatile and effective network is a gated punch through device in combination with a spark gap which may extend the protective limit to five kilovolts.

Singletary, J.B., and J.A. Hasdal (BDM, Albuquerque, NM).

METHODS, DEVICES, AND CIRCUITS FOR THE EMP HARDENING OF ARMY ELECTRONICS.


Electric and magnetic pulse fields generated by nuclear weapon detonations can temporarily or permanently disable military electronic equipment. Communications/electronic systems are particularly vulnerable where the pulse energy may be coupled into antennas and cables and thereby affect highly sensitive circuitry.

In the higher range of voltage applications for protective devices the use of spark gaps immediately comes to mind. Extensive conducted indicate that when response occurs on a test pulse rise the response is linear. At longer pulse duration when applied voltages still exceed d.c. sparkover voltages, longer response occurs. The minimum response time for a gap may be interpreted as the sum of the times required for formulation of avalanche discharge. As a protective device a spark gap is obviously better as its response time is decreased.

Opposed series diode protection indicates this configuration is restricted in its range of passed frequencies and are susceptible themselves to EMP damage. Opposed parallel diodes offer slightly better frequency response for those applications where low voltage operation is possible. Opposed parallel diode stacks offer higher voltage protection but frequency response is lowered and response time increased.

Various diode configurations indicate usefulness in the voltage range below 90 volts, the lower limit of spark gap protection.

Supplementary analysis relates the spark gap parameter impulse ratio as defined as the ratio of surge peak voltage to static breakdown voltage. Widely observed facts indicate that higher impulse ratios produce faster response times. Analysis of the kanal.
The transfer characteristics of BIMOS MOSFET's throughout the nanoampere to milliampere range are presented, and their use in current mirrors, amplifiers, oscillators, and timing circuits is discussed. Linear operation in the subthreshold region is shown to provide extended performance in micropower integrated circuits, with transconductance levels similar to those of bipolar devices. Advances in MOSFET pair-matching are analyzed; commercial capabilities are described; and the combination of submicroampere input-bias levels with protected-gate devices is shown to be practical at elevated temperatures.

The RF vulnerability of integrated circuits was investigated. Both interference and failure testing were performed to define the relationships between RF vulnerability and (1) fabrication technology (CMOS vs. bipolar), (2) circuit function (NAND, NOR, etc.), and (3) manufacturer. Wide variations in interference and failure power levels were found both within a device type (e.g., 5474) and between manufacturers. These variations can produce differences between one device and another by as much as 20dB for the same application. As yet, electrical screens have not been useful in predicting the vulnerability levels. It was also found that interface testing did not predict the failure power level of a device.

Based on the ICs used in the tests, CMOS devices are not susceptible to interference as bipolar (either linear or digital). But little difference exists between bipolar and CMOS for RF failure susceptibility. Bipolar linear devices appear to be the most susceptible types of devices to interference although some digital bipolar devices may approach these levels.

The electrical indication of interference or failure was also found to vary widely. This fact makes the diagnosis of system failures and their causes even more difficult.


The primary consideration for all electrostatic precautions is that they must be continuously performed. In the vicinity of unprotected static sensitive devices avoid activities which tend to be friction producing. Before performing any work operate ionized air blowers for two or three minutes until there is no residual charge at the work area as measured by a static meter.

The antistatic precautions taken to protect individual static sensitive devices shall also be taken as applicable to protect assemblies.

Dielectric strength or insulation resistance tests are not recommended for equipment containing static sensitive devices. All unused inputs of MOS and CMOS devices must be connected to either device supply or ground. DC voltages shall always be applied before signal voltages and signal voltages shall always be removed before DC voltages.

Facilities shall include static free work stations, including metal frame work benches and conductive surfaces. Velostat (conductive black polyolefin) is electrically conductive. Carbon particles impregnated in the poly provide volume conductivity. Sloughed particles of carbon from this material preclude its use in most precision clean operations.

All CMOS devices are susceptible to damage by the discharge of electrostatic energy between any two pins. Their extremely high input impedance lends itself readily to the buildup of electrostatic charges. Basic protection of these devices starts with personnel and materials all at the same or ground potential. Precautionary handling is extremely important. For example: in the sequence in which bonds are made, the Vpp (device supply) connection should always be made before the Vgg (ground) bond. Automatic handling equipment should include the use of ionized air blowers in addition to good grounding. PC boards incorporating ICs should have shorting bars installed prior to assembly.


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The electrical indication of interference or failure was also found to vary widely. This fact makes the diagnosis of system failures and their causes even more difficult.
Care must be taken in the use of input resistors as they may reduce speed because of the added RC delay. Operation above maximum ratings can force CMOS devices into a PNPN(SOR) latch-up mechanism. "Latchup" is considered to be the creation of a low resistance path between the power supply and ground on a circuit during an electrical pulse. For latchup to occur combined beta gain is greater than 1, all junctions are forward biased, and the bias supply must supply current above holding.

Recent experience with hybrid assemblies has included ESD problems in numerous part types including bipolar devices, thin film substrates, ECL and CMOS devices. The base-emitter junction was degraded to a low resistance short and the reverse I-V curve was shifted several tenths of a volt due to the effect of ESD on several Westinghouse bipolar op-amp chips for hybrid usage. Typical damage could be induced by standing up from a lab stool and touching the package lid. Beta degradation may also occur because of ESD.

The physical mechanism of damage is aluminum transport that may thermally crack the silox overcoat in severe cases. The shorts can occur between metallization crossovers in multiple layer metallizations. A quasi-square anomaly often is detected by SEM after static discharge. This square pattern was observed in simulated ESD testing. ESD failures were observed to cause several tenths of a volt shift in the emitter outputs of ECL devices. Damaged oxide over the E-B junction could be seen near one end of each emitter contact area. Multiple damage to ECL from ESD resulted in several cases of shorts between Vcc and ECL outputs, also in leaky reverse base-emitter junctions.

The cholesteric liquid crystal method was used to detect the exact short site caused by ESD in several CMOS devices. Subsequent testing under various loads found CMOS devices least susceptible with nothing attached to any nodes rather than having one or more nodes grounded.

Component evaluation and manufacturing engineering groups have been involved in some experiments to determine the magnitude of the static problems with semiconductors in Tek Manufacturing. Several electronic devices were subjected to typical production handling, then tested. Out of 50 MOS devices tested, five had parameters degraded and five more were catastrophic failures. Techniques to minimize handling and the use of conductive containers such as Velostat can reduce losses in manufacturing. Multimeters and other testing devices must also be used with care on MOS IC's.

Olin, R.P. (Control Data Corp.). 
"CONDUCTILE" STATIC CONDUCTIVE VINYL FLOORING. 

The "conductile" test sample submitted by Vinyl Plastic Inc. (VPI), Sheboygan, Wisconsin passed the current CDC requirement for maximum generation of static electricity in a computer room environment.

The test conducted by Control Data Corp. measured the voltages generated when a tester generated standard voltages by shuffling his feet on a test carpet using neolite soles. No measured voltage was generated when a test sample tile was cemented to a metal 2'x2' floor with conductive cement.

Johnson, W.D., and R.R. Weekley (Hughes Aircraft Company, Los Angeles, CA).
MELAMINE LAMINATE AND RCAS-1200 WORK SURFACE MATERIALS, EVALUATION STUDY. 

An evaluation was conducted on two work surface materials to determine if they are acceptable as static safe.

The test results indicate that melamine laminate is an acceptable "static safe" work surface. The antistatic properties of melamine laminate are unaffected by exposure to low relative humidity and to various cleaning agents.

The antistatic properties of RCAS-1200 "pink poly" are not degraded by low humidity but are seriously degraded by all cleaning agents except antistatic fabric softeners such as "Downy".

Warsher, A. (Charles Stark Draper Laboratory, Cambridge, MA).
USE OF MELAMINE WORK SURFACES FOR ESD POTENTIAL BLEED-OFF. 

Paper-base melamine sheets can be used for work surface tops under certain
conditions. The conditions are as follows: the top surface of the melamine be abraded away before applying a spring loaded contact for electrical ground, the ambient relative humidity be above 30% if the work surface will be relied upon for electrical discharge, the earth return circuit not be through an additional current limiting resistor, and other ESD measures be continued such as the use of operator wrist straps.

Metal bench tops using a 250,000 ohm resistor to ground are still the preferred method for ESD protection of work stations.

15001

Madzy, T.M. (IBM Corp, Endicott, NY).
FET CIRCUIT DESTRUCTION CAUSED BY ELECTROSTATIC DISCHARGE.

MOSFETs are particularly susceptible to ESD damage because of the low destructive breakdown voltages of their oxides.

In IC FET packages the PD is normally another FET with its gate and source connected to the substrate and is in effect a voltage limiting diode with the result that ESD potentials are developed directly across its gate oxide. The I-V curve of the device can depend on whether or not a potential exists at the ground pin of the module.

The destruction of the gate oxide is due to joule heat and arc action when the potential across the device is 5-10 MV/cm. ESD pulses less than 12ns in width require large magnitudes to cause destruction. Pulses of greater than 130ns width require magnitudes of 44v.

The lowest ESD susceptibility level occurs when the substrate is connected to an electrostatic source through some very low impedance return and a charged human makes contact with one module pin.

15002

ELECTROSTATIC DISCHARGE DAMAGE PREVENTION.

Sanders Associates, Inc. have established Corporate Standard SA-STD-228 for Electrostatic Discharge Damage Prevention. Corporate Standard 228 includes provisions for distribution of ESD sensitive device listngs, purchase specification preparation, engineering drawing and parts list callouts, assembly markings and maintenance manual cautionary notes.

Employee training and basic awareness requirements are specified and the use of protective antistatic devices is required.

15003

Koenigsberg, H.M. (Hughes Aircraft Company, Los Angeles, CA).
ANTI-STATIC PROTECTION FOR THE PCB YELLOW ROOM AREA.

The most practical method of minimizing or eliminating the effects of static electricity is by ionization using the high voltage discharge of alternating current. The contamination problem in the yellow room of PCB manufacturing is aggravated by the use of processing materials, paper articles and work in progress. Laminar flow hoods can effectively eliminate 2-3kv charges at 3y' distance within 5 seconds. Several sequential processing steps must be carried on and several different materials utilized before the net effect on product yield can be determined.

15005

Gardner, P.R. (TRW, Redondo Beach, CA).
HARDNESS ASSURANCE LATCHUP SCREEN PROCEDURE.

There are two types of radiation induced latchups, a hard latchup and an incipient latchup. A hard latchup is a sustained functional failure. Incipient latchup is not sustained but lasts longer than can be explained by normal circuit times constants.

The source used to promulgate radiation induced latchup will be a flash X-ray machine or a Linac. A dry run radiation exposure and a pass status to verify dosimetry will be performed.

Oscilloscopes or pre-set comparators will monitor outputs to verify device parameters.

The method to analyze four layer integrated circuit latchup is valid for bipolar junction-isolated and dielectrically isolated integrated circuits.

The latchup or PNPN sustaining mechanism in a bipolar integrated circuit occurs in four-layer bistable structures. One operating state is characterized by high impedance, low current while the second state is characterized by low impedance and high current.

The existence of a PNPN structure within an integrated circuit does not imply that it is a sustainable latchup path even if the parameters for bistable action are present. For a latchup to be sustained, a bias of positive polarity from anode to cathode must be present; in addition, the current must not be limited below holding. For example, if an intermediate function is reverse-biased latchup is not possible.
INSTRUCTIONS FOR INSTALLATION AND MAINTENANCE OF CONDUCTILE.

Static conductive vinyl flooring must be installed on smooth, dry, clean, subfloors. New concrete must be properly cured preferably by covering it with polyethylene film. Under ideal conditions a drying time of at least eight weeks is required.

Conductive flooring will not be guaranteed if the rate of moisture emission from subfloor exceeds three pounds per 1000 sq ft per 24 hours. Conductile may be installed on radiant heated floors provided the surface temperature does not exceed 90°F.

Installation of conductile directly over wood strip or plank subfloors is not recommended.

TRW Systems Group has incorporated handling and protection fabrication/inspection process procedures for static sensitive electronic parts and assemblies. Procedures specified involved the material receiving area, receiving inspection and control, testing, and storage. Special procedures for X-ray analysis, power aging and radiation screening areas also are written. Component tinning, production line assembly areas, bonding, conformal coating and general area control are also covered.
Surveys showed industry was facing potential ESD damage to components and had serious problems throughout the manufacturing assembly and shipping activities.

Semiconductors, chips and other component parts are generally sensitive until fabricated or installed in assembly. To eliminate this possibility, the receiving inspection of electronic items should be moved to a controlled area and "good practice" suitable for handling static sensitive classes of parts should be initiated. The above findings showed a general lack of understanding of field force protection and the basic electrical phenomena involved.

PULSE POWER FAILURE MODES IN SEMICONDUCTORS.

It was observed that a common mode associated with permanent damage effects in reverse-biased junctions is the phenomenon known as "second breakdown." Both energy and current modes were observed.

The occurrence of thermal second breakdown which is energy-dependent was found to represent the point of incipient permanent damage at submicrosecond pulse conditions. In contrast the energy required for current mode second breakdown has not in itself been observed to represent incipient junction damage. Thermal second breakdown physically is a local thermal runaway effect at the junction induced by severe current concentration. Current mode second breakdown has not been fully understood or observed. It is initiated by relatively high material current densities under the emitter during collector to base junction reverse pulsing resulting in a forward bias on a portion of the emitter.

Comparison of the mathematical model with experimental data indicates that if the volume of the thermal second breakdown current constriction site across the junction and the critical initiation temperature are known then the model can be used to determine the pulsed power susceptibility of any general P-N junction. On a practical basis it is relatively easy to assign specific values to the initiation temperature and to empirically determine the typical current constriction site volumes.

Lee, J. (Raytheon, Portsmouth, RI).
93L415 BOARD FAILURES.
The failure mechanism causing the input leakages of the 93L415 to increase was due to electrical overloading of the input protection diode caused by static discharge. The devices that failed were six 93L415s in ceramic packages. All six units exhibited at least one input pin which exceeded the high input current parameter specified at 40ua at $V_{IN} = 4.5v$ and $V_{CC} = 5.25v$.

15017

Patterson, J. (Teledyne Microelectronics, Manager Failure Analysis Laboratory), A TEST METHOD TO DETECT ELECTROSTATIC DAMAGE IN THICK FILM RESISTORS.

The test method described herein allows the examinations of high voltage characteristics of thick film resistors and reveals the voltages to which they have previously exposed. The model that best fits recorded data to explain why thick film resistors decrease in value when subjected to ESD is thin oxides surrounding resistive particles in thick film ink. During exposure to high electric fields these oxides break down permanently and provide additional conduction paths within resistors.

15018

Anon. (U.S. Navy, Naval Sea Systems Command), MILITARY SPECIFICATIONS, STANDARDS AND CONTRACT CLAUSES SPECIFYING CONTROLS FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGE.


15019


This work was authorized under MERDC, Ft. Belvoir, contract No. DAAK02-70-C-0464 funded by the Defense Nuclear Agency. The effort included the design, construction and checkout of a fast, high voltage pulser with a component test effort. This latter work is emphasized in this report; the operator's manual covers the details of the pulser.

15020

Hart, A.R. (U.S. Navy, Naval Electronics Laboratory Center, Electron Material Sciences Division, San Diego, CA), RF FAILURE PREDICTION FOR MOS 4001 AND 4011 INTEGRATED CIRCUITS.

This report defines the effects of a single, high-power, 5 microsecond, 3 GHz RF pulse injected into the output of two types of MOS devices: 4001 (NOR Gate) and 4011 (NAND Gate). This report presents a possible theory which explains the 12d8 difference in power level for RF failure of the devices tested and compares the effects of different manufacturers' chip layout designs on the RF susceptibility of these devices. A DC model was developed and applied to the RF problem and found to fit very well to the experimental data. The DC model predicted the RF susceptibility hierarchy for several manufacturers and helped to define potential ways of reducing the RF susceptibility of these types of MOS devices. This report also points out how some EMP radiation hardness protection circuits may actually increase the RF susceptibility of similar types of devices.

15022

Huntsman, J.R., and D.M. Yenni (3M Company, St. Paul, MN), DON'T ZAP IT - BAG IT.

Advances in IC technology are increasing circuit densities and thus accentuating static damage susceptibility. Protective devices are not always a guarantee of protection. Insulators have a very large surface resistivity and therefore do not dissipate static electricity. Organic additives can increase their conductivity on their surfaces. Antistatic bags do not effectively protect their contents from external electric fields. Charges may accumulate, forming a significant voltage gradient from top to bottom. 3M Company has developed an effective field shielding antistatic bag consisting of an outer metallic coating, a center polyester film, and an inner antistatic polyethylene. The ESD pulse in this shielding bag lasts only several microseconds with a peak of 75v.

Antistatic film surface resistivity tests show that it falls into the range of an insulator. Velostat is 100 million times more conductive than anti-static films. A test was run at 35% RH. A subject with static charge of 1000v touched a grounding strap of velostat conductive plastic. The voltage dropped to 0 volts instantaneously. The decay time was less than 1/10 second regardless of humidity or electrode. Age affects the anti-static qualities of certain anti-static films.

Electric ionizing air blowers induce low but significant voltages in ungrounded objects brought near it; nuclear powered blowers do not.


The hazard of ESD is an existing problem which is becoming more severe with the advancement of technology. Government and Navy personnel lack knowledge on the hazard of ESD. This lack of knowledge is resulting in unnecessary repair costs, excessive equipment downtime and reduced mission effectiveness in that electrical/electronic devices and equipment which incorporate them are being damaged throughout the equipment life-cycle during processing, assembly, inspection, packaging, shipping, storage, testing and maintenance.

An awareness program on ESD along with the implementation of an effective ESD control program can minimize the ESD hazard.


A retrospective search/survey was performed to determine precautions necessary in handling MOS or CMOS devices in automatic test and insertion equipment. The problem is that large amounts of static voltages on portions of machine handling equipment. The static charge build-up is approximately 10,000 volts depending on humidity levels.


An electrostatic discharge (ESD) study was performed in order to provide the R&D engineer with data necessary to properly protect sensitive components from ESD damage and the production and service engineers with information necessary to determine appropriate antistatic production assembly and repair techniques.

The study consisted of an ESD susceptibility comparison on CMOS devices from various vendors. A latent failure life test was also performed.

A test station was assembled capable of delivering a repeatable discharge to the D.U.T. and a standard test method was developed for determining ESD sensitivities for this study.


It is very apparent that the overall failure rate caused by static discharge can be reduced dramatically for both CMOS and low-power Schottky by careful handling. Opto-isolaters can benefit from delicate handling. The failure rate for CMOS was cut 88% and 76% for low-power Schottky by the application of the recommended handling procedures.


This study was initiated to determine what parts used by Sperry Univac Defense Systems Division are potentially sensitive to electrostatic discharge. Device structural features influence ESD susceptibility. Components very sensitive to ESD damage (Cat. I) include MOS with no input protection circuitry, dielectrically isolated semiconductors with internal capacitor contacts connected to external pins and microcircuits utilizing N+ guard ring construction (with metallization crossing over the guard ring). Category II devices include MOS with input protection, dielectrically isolated and fine metal bipolar, low power Schottky and Schottky TTL, high speed ECL.
high input impedance linear (greater than or equal to 10 ohms) junction FET's, small signal transistors with \( f_T \) greater than 500 MHz, and all devices that use metallization paths over active areas and ladder networks.

EMPRESS is a facility of the U.S. Navy to test ship behavior in a simulated EMP environment. This brochure presents what EMPRESS is, why it is needed, and how it is used.


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15050


Experiments on CD4021A CMOS eight-stage shift registers were conducted to investigate the susceptibility of the device to electrostatic discharge (ESD), to investigate the possibility of latent functional failures of a device degraded by ESD, and to isolate the cause and location of failures during assembly. Experiments were also conducted on two buffered CMOS devices, 4021B and CD4081B, and two additional unbuffered ones, CD4011A and DC4013A, to compare the ability of two types to withstand ESD. After the CD4021A devices were subjected to ESD by using a human-body-equivalent circuit model, each one was given an operating life test at 150°C for 308 h (equivalent to 2000 years of operation at room temperature). None of them failed to (logically) function after the life test. The low-bias terminal, VSS, and an output terminal were found to be the most susceptible to ESD pulses causing failures. All of the assembly failures in a recent production run were reproduced by subjecting devices to ESD pulses on the VSS terminal. By using the same ESD circuit on both the "A" and "B" devices, it was found that gate oxide ruptures occurred at considerably lower voltages in the unbuffered devices.

15056


The EIA has criticized the Government's effort to institute more rigid safeguards for the control of electrostatic discharge. Industry officials assert that only one half to three quarters of the users' industry has taken adequate steps to combat the problem. The Navy is seeking to develop a standard which would mandate compliance before companies using ESD sensitive devices would be approved for government contracts. The EIA cites cost factors and an "overkill" mentality as causing unreasonably high cost impact.
GaAs FET failures are obviously catastrophic events. Long-term events such as changes in Schottky gate characteristics and intermetallic reactions can eventually cause loss of gate control. Specifically an explanation and solution to the potential reliability problem of electrostatic discharge-created changes in Schottky gate reverse leakage currents.

The changes vary in degree from just discernable creation of a resistive reverse current to catastrophic eruption of gate metal, GaAs channel and source contact metal.


The purpose of this article is to provide an awareness of (1) common sources of static, (2) detrimental effects, and (3) available controls for protection from the damaging effects of electrostatic discharge (ESD). Particularly susceptible to damage from ESD are metal oxide semiconductors, discrete bipolar transistors and diodes. Damage does not always result in sudden failure but may produce degradation, often apparent as reduced reverse voltage breakdown.

McAteer, O.J. SHOCKING BLOW TO MILITARY ELECTRONICS. Military Electronics/Countermeasures, June 1979, pp. 59-63.

ESD has been recognized in recent years as a major source of electronic device failures. The problem becomes even more acute for military applications where reliability is a critical parameter and semiconductor part counts are high. Subtleties in physical analysis make recognition of ESD failures difficult. More thorough analysis such as chemically etching the SiO2 passivation layer and site isolation using special heat sensing cholesteric crystals are used. Capacitive coupling and loading between nodes is another subtlety making ESD failure analysis even more difficult.
Data on lightning incidence is examined to determine the number of lightning strikes to be expected over a period of time by climatological areas. The physical parameters of lightning are discussed, with the main emphasis on the direct effects of flashes to grounds. Intra-cloud discharges and static and electromagnetic fields generated by lightning are also described.


A new electrostatic discharge failure mode was discovered which affects MOS LSI components in hermetic packages with nonconductive lids. Failure can be induced by spraying package lids with canned coolant. It is shown that charge from the freeze spray causes breakdown in the air-gap between the die surface and the lid. As a result, localized surface charging and field inversion occurs in the array, which produces leakage currents and circuit failure. The failure mode can be characterized by its recovery with either a strong UV exposure to the die surface or a DI water rinse.


A nondestructive technique to identify localized defects in the gate dielectric of MOS devices has been developed. The technique is based upon electron beam induced conductivity modulation which gives rise to a relatively large increase in gate current under an applied bias when the beam scans a localized defect area. Measurements on devices with low gate breakdown voltage have been made and correlated with regions where subsequent catastrophic gate breakdown occurred. A circuit description and physical model of the technique is presented.

Tasca, D.M. (Boeing Aerospace Company, Seattle, WA). PULSE POWER DAMAGE CHARACTERISTICS OF ELECTRICAL RESISTORS.

This report defines the EMP induced damage characteristics of a variety of electrical resistor types. The experiments evaluate the change in device resistance. Of the five resistor classes tested, wire wound resistors were most resistant followed by carbon composition, carbon film, metal film and metal oxide, respectively.


Methods for handling and testing MOS semiconductor IC's used in the prevention of overstressing by ESD were investigated and developed. Testing was performed in six areas of static discharge damage: DC testing, process evaluation test circuits, DC testing of MOS LSI devices, functional testing of MOS devices, switching time testing of MOS devices and fault testing of MOS devices. The Fairchild 5000 C with low frequency generation was capable of only limited testing of the MOS LSI devices.


This manual provides HP Data Systems Division with a single document covering many of the considerations associated with developing, testing (including a test for ESD susceptibility) and specifying the environmental capabilities of Data Systems Products.


The substitution of a conductive plastic for the normal dielectric plastic was considered the most satisfactory retrofit to provide human electrostatic discharge protection for electroexplosive devices (EEDs) employing plastic initiator plugs. Conductive gaskets may also be satisfactorily used for protection in those cases where the length of the EED can be increased.
Voltage transients are one of the three general types of power line disturbances. The use of uninterruptable power supply can take care of voltage transients, but this is too expensive a solution if transients are the only problem of immediate concern. This report defines and describes voltage transients and identifies their sources. The probability of occurrence is discussed. The key characteristics desired for the suppressors were determined to be energy handling ability and response time.


This article describes a new generation of electrostatic instruments designed for use in establishing and monitoring Environmental Static Control (ESC) programs. An overview as to the range of selection and application of types of instruments available for material selection, component classification, survey, monitoring and analysis is provided.


Glaze resistors of the PdO-Ag formulation have established their worth in numerous applications for several years. Their primary advantages of allowing fast, economic production with reliable results are well-known in the industry. In most cases, it is required that the resistors be given a final adjustment to achieve the proper value for the intended application.

A method for adjusting the value of PdO glaze resistors by proper application of a high electric field is described. Material response and reliability after trimming are described. A model concerning the removal of silver from the PdO lattice is also discussed.

A unique and little-understood characteristic of thick-film resistors is their sensitivity to high voltage, a phenomenon both useful (as in the case of resistance adjustment) and undesirable (as in the case of static electricity). In a recently concluded experiment the high voltage sensitivity of the latest generation of thick-film resistors was studied. The conclusions included: (1) most of the newer materials exhibit a sensitivity to high voltage; (2) high voltage sensitivity is more pronounced in high resistivity materials that typically reduce in resistivity upon exposure to high-voltage pulses; and (3) some of the newer materials exhibit a significant shift in their temperature coefficients of resistance (TCR) during pulse adjustment.

15143


This article points out the need for a standardized approach to combating ESD-related failures. It discusses why ESD has been ignored in the past, what new product areas should be developed, and how standardization can eliminate ESD-caused failures.

15188


This volume of the detailed summary presents the data and rationale supporting the conclusions reached with respect to shielding elements. This summary includes areas such as the specification selection in terms of quality assurance programs and procedures, the assignment of levels of shielding effectiveness to the various elements, the most significant conclusions reached and recommendations to be made, and a complete reference bibliography.

15188-01


DETAILED SUMMARY - EMP SPECIFICATION DEVELOPMENT VOL. III - MIX OF SPECIFICATIONS.
Clark, O.M., and J.J. Pizzicarelli (General Semiconductor Industries, Inc., Tempe, AZ).

**EFFECT OF LEAD WIRE LENGTHS ON PROTECTOR CLAMPING VOLTAGES.**

Under high current pulse conditions, excessive lead lengths on suppressor components can be responsible for destruction of the protected circuit. This is caused by voltage build-up across the small but finite amount of inductance in the interconnecting leads of the protector. Some suppressor devices have been tested and observed to have more than twice the specified clamping voltage which was subsequently shown to be caused by inductive effects. Problems and corrective measures are illustrated and discussed in this paper.

**FORUM: PROTECTING ICS FROM ELECTROSTATIC DISCHARGE.**

In an attempt to determine the extent of the ESD problem as it relates to ICs and to uncover ways of handling the problem, Electronic Products Magazine brought together a group of industry experts to present their views. The experts included manufacturers and user of ICs along with members of the static protection industry. They discussed problems caused by ESD and ways to prevent ESD.

**DEVELOPMENT OF HIGH-LEVEL ELECTRICAL STRESS FAILURE THRESHOLD & PREDICTION MODEL FOR SMALL-SCALE JUNCTION INTEGRATED CIRCUITS.**

This report summarizes the experimental and theoretical work performed in order to develop engineering-type prediction techniques to predict both surge impedances and failure levels of small-scale junction integrated circuits when exposed to EMP-type environments.

**FORUM: PACKAGING HIGH-VOLTAGE ELECTRONICS.**

The packaging of high-voltage systems can be both critical and complex. This is because the number of variables having an effect on high-voltage performance is high and many variables are interrelated, the types of voltage failures with these variables are interrelated, the types of many variables are interrelated. Voltage failure conditions are frequently transient in ways which prevent accurate knowledge of the actual voltage stress conditions for which electronic packaging is required. This article will first present the major fundamentals which must be considered in the packaging of high-voltage electronic systems, and this will be followed by discussion of the critical factors in the design of high-voltage electronic packages and in the all-important application of high-voltage materials.

**PERFORMANCE OF CONDUCTIVE CARBON BLACKS IN A TYPICAL PLASTICS SYSTEM.**
Carbon black, used primarily as a reinforcing filler in rubber, exhibits properties of electrical conductivity and physical form which render it the preferred filler for imparting conductivity to normally insulative elastomeric and thermoplastic polymers. The properties of carbon black, important in imparting conductivity to polymer systems, are discussed. The effects of three different carbon black types at varying concentrations on the electrical, physical, and rheological properties of poly(ethylene vinyl acetate) (EVA) in both thermoplastic and thermoset form are also illustrated. Reference is also made to the phenomenon of significant resistivity variations with increasing temperature of carbon black-loaded plastics systems.

Friedlander, G.D.
ELECTRICITY IN HOSPITALS: ELIMINATION OF LETHAL HAZARDS.

The problems of macroshock and microshock in hospitals have received considerable coverage recently in the press, in symposia sponsored by professional societies, and in technical publications. The general subject falls within a sensitive and controversial area in which proposals for upgrading the safety of medical-electrical equipments are being studied and/or implemented.

COPING WITH STATIC ELECTRICITY - PART XXII, HIGHLIGHTS FROM EOS/ESD SYMPOSIUM PAPERS.

Many people believe that one topical antistat is as good as another. That belief is absolutely false. Using a good topical antistat solution not only controls electrostatic damage during printed circuit board (PCB) processing but actually improves solderability, reducing solder defects by over 80%. This paper discusses the author's experiments and results using antistat during PCB processing.

REDUCING SOLDER DEFECTS USING TOPICAL ANTISTATS.
Circuits Manufacturing, Vol. 21, No. 4, April 1981.

Many people believe that one topical antistat is as good as another. That belief is absolutely false. Using a good topical antistat solution not only controls electrostatic damage during printed circuit board (PCB) processing but actually improves solderability, reducing solder defects by over 80%. This paper discusses the author's experiments and results using antistat during PCB processing.
Metal migration induced by electric field and temperature gradients has been studied in aluminum-silicon and gold-silicon interdigitized test structures. At current densities of $2 \times 10^6$ A/cm$^2$ and temperature gradients of 75 °C/cm, migration occurred across the Si-SiO$_2$ interface. Calculated diffusion profiles show that below 350°C, mass transport is more rapid with aluminum. At temperatures between 350°C and 550°C, metal migration is more rapid with gold metallization. Metal migration was shown to be a multistaged process without the existence of a unique activation energy.

DeForest, S.E. (University of California, Inst. for Pure and Applied Physical Science, La Jolla, CA).

SPECIFICATION OF GEOSYNCHRONOUS PLASMA ENVIRONMENT.

Data for UCSD plasma instruments on the ATS 5 & 6 satellites has been studied to specify the geosynchronous plasma environment as it affects electrostatic charging of spacecraft. The emphasis of the initial study has been primarily to service the needs of the design engineer, while simultaneously establishing the context in which a more general model could be developed. The report includes an environmental specification plus a review of geosynchronous plasma and wave phenomena.

Morel, P.R., F.A. Hanser, and B. Sellers (Panametrics, Inc., Waltham, MA).

DESIGN OF INSTRUMENTATION SUITABLE FOR THE INVESTIGATION OF CHARGE BUILDUP PHENOMENA AT SYNCHRONOUS ORBIT.

A satellite-borne Rapid Scan Particle Spectrometer (RSPS) has been designed to measure the charge buildup phenomena at synchronous orbit. Simultaneous measurements along two orthogonal axes are made. Each axis incorporates 4 electrostatic analyzers (ESA) and 2 solid state spectrometers (SSS). Four ESAs (low energy p, low energy e; high energy p, high energy e) and two SSSs (proton, electron) with four and five energy bins, respectively, in each analyzer provide a logical compromise of energy resolution and high time resolution. The low energy ESAs cover the energy range 0.05 to 1.7 keV; the high energy ESAs cover the 1.7 to 60 keV...
range. The electron SSSs cover the 30 to 1000 keV range and the proton SSSs cover the 70 to 7000 keV range. A complete energy spectrum is generated every 1 second. The digital data output consists of a 9 bit mantissa and a 3 bit exponent, allowing accumulation of greater than 1.3 x 10^5 counts. A command control allows the ESA or SSS sweep rate to be decreased, or fixed, enhancing the time resolution of portions of the spectrum. A digital count ratemeter with 250 usec integration time is included. A multiplexer controlled by ground command selects the ratemeter input from one of the 8 ESAs or 8 SSSs. Very high time resolution data can be generated by this circuit. Two instruments have been fabricated, tested and calibrated. The first of these was launched into near-synchronous orbit on board the SCATHA satellite on 30 January 1979.

15562
CHEMICAL PHYSICS OF ELECTROCHEMICAL MECHANISMS IN NONMETALLIC SPACECRAFT MATERIALS.

The interactions of spacecraft and space systems with the changing solar illumination and charged-particle environments in the vacuum of space result in the occurrence of a number of electrostatic and electromagnetic phenomena. These phenomena, commonly referred to collectively as spacecraft charging effects, can produce undesirable and sometimes serious problems with the performance and operation of military, commercial and NASA spacecraft.

15569
MICROWAVE INTERFERENCE EFFECTS IN INTEGRATED CIRCUITS.
IEEE - 17th Electromagnetic Compatibility Symposium, Session 4A18, October 7-9, 1975, 6 pp.

The susceptibility of components to conducted EM energy is required to determine the severity of potential problems in specific cases and to establish the degree of protection required to ensure proper system operation. Representative circuit types are studied to determine underlying physical mechanisms from which models can be derived to extend the results across entire device families.

15576
ATOMIZER WITH INDUCTIVE ELECTRODE.

This is an invention in the field of pneumatic devices for producing electrically charged particles in a gas medium. It can be used for the settling of sprayed substances on various surfaces; for example, in the aerosol disinfection method and in neutralizing electrostatic charges.

15581
PULSE POWER RESPONSE AND DAMAGE CHARACTERISTICS OF CAPACITORS.

This project summarizes the experimental and theoretical work performed to define EMP pulse response and damage characteristics of a variety of capacitor types. 2079 capacitor units were experimentally evaluated. Of these, 1201 were of the electrostatic type and 878 were of the electrolytic type.

15583
Aleksandrov, V.G., B.I. Bazanov, and A.V. Mayorov (U.S. Army Foreign Science and Technology Center).
INDIVIDUAL PROTECTION AGAINST MICROWAVE RADIATION AND STATIC ELECTRICITY.

This report deals with microwave radiation and static electricity protective gear, the various types of gear available, and what working conditions would warrant the wearing of protective garb.

15584
Naplava, A. (Research Institute for Processing and Applications of Plastics, Nitra).
INTRODUCTION TO THE ANTISTATICS OF PLASTICS.

This article contains a brief outline of the principles of the formation of an electrostatic charge and the method for its elimination. The practical application of the
method is shown specifically as it relates to plastics. Basic methods for elimination of an electrostatic charge are described together with a detailed analysis of antistatic finishing of plastics with emphasis on thermoplastics. Various types of antistatics are characterized with a view to their applications.

15585

Solomon, P.M., and J.M. Aitken (IBM, Thomas J. Watson Research Center, Yorktown Heights, NY). CURRENT AND C-V INSTABILITIES IN SiO\(_2\) AT HIGH
FIELDS.

Results have been obtained concerning the interrelation of current and C-V instabilities in MOS capacitors subjected to negative gate high field pulsing. Rising current transients and negative C-V shifts both show the formation of positive charge in the oxide. However, this charge appears to be situated close to the electrodes rather than in the bulk of the oxide and the temperature dependence of the rate of charge accumulation near the electrodes is different for the aluminum and silicon electrodes.

15662

Jordan, A.S., J.C. Irvin, and W.D. Schlosser (Bell Laboratories, Murray Hill, NJ). A LARGE-SCALE RELIABILITY STUDY OF BURNOUT
FAILURE IN GaAs POWER FETS.

Burnout can be the dominant failure mode in GaAs power FETs. Since this is a process without electrical precursors, special experimental and statistical treatment appropriate to censored data has to be employed. The resulting failure distribution is lognormal and depending on the operating conditions a maximum failure rate between 400 and 4500 FITs is projected.

15672

Hart, A., T. Teng, and A. McKenna (Hewlett Packard Co., Corvalis, OR). RELIABILITY INFLUENCES FROM ELECTRICAL OVERSTRESS ON LSI DEVICES.

Reliability prediction of MOS LSI devices by testing at elevated temperature can be influenced by electrostatic discharge and electrical overstress conditions during the test period. MOS devices that used junction diodes in the input protection structure were found to be more susceptible to failure from electrostatic discharge in 1250°C ambient temperature than at 250°C. Failure analysis and modeling indicate that this effect is more severe for MOS LSI devices than for bipolar devices due to the doping levels used in the MOS technology. These effects will impact accelerated life testing, simulation testing of electronic systems to be operated at elevated temperatures and failure analysis techniques performed at elevated temperatures.

15726

Wunsch, D.C. (BDM Corp., Albuquerque, NM). THE APPLICATION OF ELECTRICAL OVERSTRESS MODELS TO GATE PROTECTIVE NETWORKS.

The study of electrical overstress failure in bipolar semiconductor devices from transients induced from nuclear electromagnetic pulses resulted in understanding of failure mechanisms, models to predict failure levels, test techniques, and guidance for hardiness assurance and reliability of gate input protective networks. The applicability of failure mechanisms and models for components of gate input protective networks such as resistors, diodes, and interconnect metallization stripes is shown.

15732

Calvin, H., H. Hyatt, H. Mellberg, and D. Pellinen (Experimental Physics Corp., Hayward, CA). MEASUREMENT OF FAST TRANSIENTS AND APPLICATION TO HUMAN ESD.
Voltage and current diagnostics have been developed with nanosecond response for measuring electrostatic discharges of humans. Calibration techniques and waveform corrections for actual electrostatic discharges from a number of people will be and are compared with equivalent circuit models.


MOS and linear devices need protection from electrostatic discharge. Bipolar devices (including TTL logic and discrete transistors) require protection, too. Yet the same potential for degradation and failure exists. This article presents descriptions of how integrated circuits and discrete components can be damaged by electrostatic discharge.


Preliminary tests indicated that the electrostatic properties of materials are highly dependent on environmental conditions and on the particular type of apparatus used for testing. An attempt was therefore made to develop an apparatus and test method which would provide reliable measurements.


It is the purpose of this paper to illustrate that for some time a design constraint namely EOS/ESD susceptibility has been overlooked in the design of electronic equipment and must now be recognized and instituted as a design criteria to avoid costly redesign and retrofit programs. Not taking EOS/ESD susceptibility into account will result in program cost overruns from production waste, equipment delivery delays, and spares usage.


Present state of the art MOS devices with 1000Å thick gate oxides have breakdown voltages in the 60-80 volts range. Due to higher fields in the oxide at the bottom of the V-groove, VMOS devices with the same oxide thickness have lower breakdown voltages (25-30 volts). A VMOS protection device with higher protection capability than conventional MOS protection devices has been designed and tested. It consists of a poly resistor connected to a npn diode, followed by an implanted n+ diffusion which acts as a distributed RC network attenuating the input voltage spikes. The final section consists of a planar NMOS transistor connected between the n+ diffusion and the VMOS gate. Tests show that this type of protection device is superior to conventional protection devices.


A technical literature survey is presented of theoretical and experimental work on static protection in the electronics industry. These results are compiled and discussed with respect to the usefulness of alternative passive static protection systems. A survey of end-users of passive static protection systems has been conducted, and these practical results are compared with the published literature data. The advantages and disadvantages of alternative systems' approaches are summarized.


This paper attempts to quantify and provide models for the electrostatic charge levels generated and the residual charges.
remaining in high humidity conditions. The results of a controlled experiment with sufficient replications to assure statistical significance will be presented.

15771

Bossard, P.R., R.G. Chemelli, and B.A. Unger (Bell Laboratories, Murray Hill, NJ).

ESD DAMAGE FROM TRIBOELECTRICALLY CHARGED IC PINS.


Integrated circuit failures can be caused by discharging a device through a low-impedance path. Discharge pulses with average power densities of approximately $10^5 \text{W/cm}^2$ occur with subnanosecond time constants. These pulses contain sufficient power to damage or melt silicon IC components. A simple equivalent circuit that describes the discharge pulse agrees with experimentally observed results.

15772


ELECTROSTATIC DISCHARGE (ESD) MONITOR DESIGN.


This paper is based on work performed during interference analysis for computer systems. Emphasis is on the designing of a high-efficiency, economically feasible ESD monitor which detects external ESD events of a given magnitude on designated positions of a system. Design characteristics, test results and possible ways for improvement are also discussed.

15773


TRANSIENT PROTECTION WITH ZnO VARISTORS: TECHNICAL CONSIDERATIONS.


ZnO varistors are novel ceramic devices used for the protection of electronic circuits against transient overvoltages. A technical description of the operation of this device is given including conduction mechanisms, response time and energy handling capability. Its applicability to a wide variety of transient phenomena is discussed.

15774

Hopkins, D.C. (General Electric Co., Syracuse, NY).

PROTECTIVE LEVEL COMPARISONS FOR VOLTAGE TRANSIENT SUPPRESSORS (120V, AC TYPE).


This report compares test results of voltage suppression capability for a selected number of suppressors. The following test conditions were used for testing: (1) .5 us rise time to rest, followed by a 100 kHz ring with a 40% reduction in each successive peak; (2) .5 us - 100 kHz ring wave applied to an L filter (200 uH inductor and a .25 uF shunt capacitor); (3) a 2500 volt peak surge having 2 us maximum rise time to crest and a 10 us minimum decay time to half crest; and (4) the 2 us x 10 u wave of condition (3) applied to the L filter of condition (2). Results from tests using these waveforms were also correlated with the cost of the devices.

15775

Bazarian, A. (General Instrument Corp., Chicago, IL).

GAS TUBE SURGE ARRESTERS FOR CONTROL OF TRANSIENT VOLTAGES.


This article summarizes briefly the state-of-the-art of gas discharge surge arrestors including a description of Uni-Imp devices, miniature CommGaps and the recent development of carbon block replacement arrestors for the telecommunications industry. Applicability to power line surges and signal line transients will be discussed. Characteristics of various types of devices with respect to electrical and environmental parameters will be presented.

15776


IDENTIFICATION OF LATENT ESD FAILURES.


At the present time there is much interest in the subject of latent ESD failures. A latent ESD failure is defined as a time-dependent failure that occurs under use conditions because of earlier exposure to electrostatic discharge that did not result in
an immediately detectable out-of-spec condition. There is considerable disagreement among ESD specialists as to whether or not latent failures of this type are a reality. The purpose of this paper is to present the results of accelerated life tests conducted on Trident program parts of several semiconductor technologies after both single and multiple ESD exposures.

15777


A model was developed for simulation of charged-personnel ESD (Electro-static Discharge) damage to selected solid-state devices. ESD damage levels are presented, and recommendations for handling static-sensitive devices are given.

15778


A sample of 10,000 bipolar silicon transistors had been tested to provide information on the functional form and parameter values for failure threshold distributions arising from exposure to electrical overstress pulses. The sample was chosen to permit evaluation of the effects of topological and diffusion profile variations on the failure threshold. Testing results are summarized in terms of parameter values for mathematically defined distributions which fit the data within a 5% level of significance.

15779


JFET preamplifiers, used in electric microphones, can be damaged by ESD from human bodies. Unprotected microphones were subjected to ESD simulation tests, and damaged units were analyzed to determine the discharge path and failure mechanism. Thermal vaporization of the contact finger metallization was revealed as the failure mode.

15780


Protection of MOS integrated circuits from electrostatic discharge (ESD) is a necessity. To allow selection of the most efficient on-chip protection network, an experimental test method was developed. This paper briefly describes various networks and their evaluation using this technique. From the data gathered, a new design was proposed and tested. Guidelines for chip layout and resultant voltage levels of ESD protection are presented, especially as related to this design.

15781


This paper discusses the design aspects of protection networks for SOS circuits. Topics such as critical parameters, design constraints, desirable features, and design perspectives are covered. An example is presented to illustrate some of the compromises required.

15782


Process and design layout variations can drastically change the ESD protection capability of proven input protection structures on LSI devices. Resistor-Diode type structures are investigated for lot-to-lot and wafer-to-wafer variations and their effects on ESD failure voltage. Failure modes and mechanisms are described. Data from ESD tests on devices using corrective redesign approaches allowing for these effects will be shown.
Design criteria are demonstrated by which certain undesirable structural and doping configurations can be avoided in bipolar device designs, based on the physics of hot spot and melt channel formation. The roles of avalanche breakdown, ratios of certain structural dimensions, and other factors are explored. The Wunsch model is extended to a distributed source model.


Experiments were performed on thin film (0.4 um) silicon-on-sapphire (SOS) diodes (p+n+n°) to determine the effect of junction diffusion spikes (5 um length) and doping level (1015 to 1017 atoms/cm°) on current configurations and second breakdown susceptibility for pulses 10us in duration. Voltage, current and energy thresholds were obtained. The results provide perspective on some types of "maverick" devices, on second breakdown testing methodology, and on device design for reducing second breakdown susceptibility.


Electrical overstress on semiconductor devices is often oscillating (e.g., lightning and EMP), but theoretical considerations of such pulses have been severely limited. An electrothermal model computer program has now been applied to study high-current forward conduction in silicon diodes and reverse-bias switching transients, which result in avalanche breakdown.

An overview of existing methodologies utilized by TRW Systems Group for the statistical assessment of electronic equipment is presented. Analysis guidelines for the evaluation of both direct-drive and buried circuit potential vulnerabilities are considered. The treatment includes a discussion of damped sine frequency spectrum versus calculated transient threats, system probability of survival, modeling and computerized analysis.


A thermal model to bound the burnout phenomenon associated with electrical overstress in solar cells is presented. Analyses suggest that for a typical cell undergoing an overstress of duration between 100ms and 1000ms, failure will result from melting of metallization at the input point.


Electronic devices and equipment may be subjected to electrical transients caused by several stimuli including lightning, nuclear electromagnetic pulse (NEMP), electromagnetic interference (EMI), and handling-related electrostatic discharge. The characteristics and severity of the resulting electrical transients vary considerably depending on the specific source. This paper describes the various sources of electrical overstress and the unique problems they create relative to analysis, simulation and protection design.


Various design trends in aerospace vehicle electrical/electronic equipment have resulted in a heightened concern about system hardness to the EM transients produced by lightning. The Society of Automotive Engineers (SAE) Committee AE-4L (lightning) to improve the ability to define and obtain equipment hardened against the lightning-induced transients is preparing definitions for test waveforms, test techniques, and hardness categories. This paper provides a status report of this effort.


An energy source being investigated by the United States Department of Energy (DOE) is photovoltaic generation of electricity from sunlight. Most of such arrays use large areas of solar cells which face the sun. Since silicon solar cells are relatively expensive, photovoltaic concentrator systems are being developed, where the sunlight is optically focused on the cells. These solar cells will be located in populous areas with high incident sunlight. Many of the locations have a high incidence of thunderstorms as well. This paper presents the theory by which lightning-induced electromagnetic pulses (EMP) can cause failure in a photovoltaic system.


Transformers powering communications equipment can be damaged by energy surges on either power of communications lines. Providing a relatively low impedance fault-current path through the transformer and reducing the containment of discharge energy will minimize physical damage. This paper describes the measures and data taken to accomplish this goal in the design of a small, wall-mounted transformer intended for use on the premises of telephone company subscribers.

A large number of microcircuits fabricated with modern technologies have been tested to determine typical electrical overstress tolerance. Qualification procedures have been recommended for electrostatic discharge and system transient generated overstress. Test results, including statistical distribution information, will be presented along with a discussion of testing problems, maverick devices, and testing-induced reliability reduction.

15796

Halperin, S.A. (Analytical Chemical Laboratories, Elk Grove Village, IL).

FACILITY EVALUATION: ISOLATING ENVIRONMENTAL ESD PROBLEMS.


The flow of ESDS components for primary manufacture through assembly and end use of operational equipment consists of several static loss areas. Investigation reveals that each facility in the production chain shares similar static problems. A basic technique of identifying these repetitious loss areas, applying effective long-term problem solutions, and maintaining facility control can eliminate the bulk of those ESD losses attributable to environmental problems. This presentation summarizes the efforts of many corporate engineers, manufacturers, and independent consultants to identify and isolate various operational ESD problems, and introduces the Facility Evaluation guideline.

15797

Domingos, H. (Clarkson College of Technology, Dept. of Electrical and Computer Engineering, Potsdam, NY).

BASIC CONSIDERATIONS IN ELECTRO-THERMAL OVERSTRESS IN ELECTRONIC COMPONENTS.


When an electronic device fails due to excessive power dissipation, several factors must be considered in an analysis of the failure: 1) the amount and spatial distribution of the power; 2) the thermal properties of the materials; and 3) the critical temperature which causes failure. This paper summarizes the important aspects and gives general guidelines which should be considered in the design and application of various components.

15798


STATIC CONTROL SYSTEMS.


This paper discusses recent innovative technological advances which have made possible static controlling systems which operate at high rates of ion generation without the production of ozone or EMI and modern microprocessor technology which has made possible extremely accurate and sensitive static monitoring and measurement instruments.

15799

Sohl, J.E. (Honeywell, Inc., St. Petersburg, FL).

AN EVALUATION OF WRIST STRAP PARAMETERS.


A comprehensive investigation was undertaken to evaluate the human engineering of wrist straps; several alarming results were found. Two points of view are taken: first was the effect of the wrist strap on the operator (operator acceptance); second was the effect of the operator on the wrist strap (durability and reliability). Two sample wrist straps from every major supplier representing the majority of designs presently on the market were included in the study.

15816

Bernett, M.K., and H. Ravner (U.S. Navy, Naval Research Laboratory, Washington, DC).

ALTERNATE ANTISTATIC MATERIALS FOR INSTRUMENT BEARING PACKAGING.

Presented at Communication Control Meeting; also in ASLE Transactions. This document shall not be released to Foreign Governments without approval of the Strategic Systems Project Office or the Ballistic Missile Office.

Antistatic materials in current use as instrument bearing packaging consist of nylon or polyethylene films containing small amounts of surface-seeking antistatic agents. Previous NRL work showed that, on contact, such agents contaminated the bearing metal surface and/or the bearing lubricant. To lessen or eliminate these problems, an investigation was carried out on 1) alternate antistatic agents applied to the polymer films as internal additives or topical coatings, and 2) alternative film materials. Effects of exposure to these alternates on pure lubricants, lubricated bearing steel surfaces, and clean steel surfaces were examined. The results provided valuable information on possibly deleterious transfer of the antistatic agent or other constituents to any contacting surface material.
Bernett, M.K., and H. Ravner (U.S. Navy, Naval Research Laboratory, Washington, DC).

**ANTISTATIC AGENTS, LUBRICANTS, AND PRECISION BEARINGS.**


Currently used antistatic agents incorporated into polyethylene or nylon films have shown adverse effects on contact with precision miniature bearings and their lubricants. Concern for improvement prompted a search for alternate materials, with the problem being addressed by investigating chemically characterized antistatic agents incorporated in the polymer films. Antistatic agents applied topically to the polymer film, and alternative films. Effects of exposure of these alternative materials to pure lubricants, lubricated bearing steel surfaces, and clean steel surfaces were studied. The results suggest possibly deleterious transfer of the antistatic agents to any contacting surface and are discussed in terms of alteration of lubricant properties, lubricant displacement, and surface wettability.

Woods, W.R. (Jet Propulsion Laboratory, Pasadena, CA).

**TEST REPORT ON NEW EQUIPMENT AND TECHNIQUES FOR CONTROLLING/MINIMIZING ELECTROSTATIC CHARGE BUILDUP.**


Some equipment was recently evaluated at JPL that is designed to provide a flood of positive and negative ions in approximately equal quantities into a room typically, but not necessarily, incorporating laminar air flow. In the order of something less than one minute, this is intended to effectively drain any electrostatic charge from almost anything that might inadvertently have been charged up by rubbing, separation, air flow or other phenomena. The equipment consists of plus and minus high voltage power supplies connected to high voltage insulated wires that have been penetrated at regular intervals with sharp needle-like emitters, somewhat similar to phonograph needles. The sharp needles at high potential emit large quantities of ions of both polarities which, when swept throughout the room by air flow and prior to combining and neutralizing each other, allow discharging of objects that the ionized air comes into contact with.

Cable configurations, needle spacing, voltages, and other parameters were varied in the tests to determine which were effective and which of the arrangements gave the best results. One configuration was markedly superior to all others evaluated and did produce a very beneficial effect. Within the bounds of the one-week time period available for the testing, the conclusion was reached that the equipment could be of significant benefit to many JPL facilities involved with electrostatic-sensitive electronic hardware. With a typical room installation requiring very little installing cost and the equipment priced in the several hundreds to very few thousands of dollars bracket, it would appear to be extremely cost-effective as well as providing a significant additional safeguard for our flight and other sensitive electronic hardware that is vulnerable to ESD damage.

Unger, B.A. (Bell Laboratories, Murray Hill, NJ).

**ELECTROSTATIC DISCHARGE FAILURES OF SEMICONDUCTOR DEVICES.**

19th Annual Reliability Physics Proceeding, April 7-9, 1981, Catalogue No. 81CH1619-6, pp. 193-199.

Electrostatic discharge (ESD) is a significant cause of device failures at all stages of device and equipment production, assembly, test, installation and field use. Even though device designs include protection circuitry, it is relatively easy to generate static potentials during handling and shipping that exceed the limits of the protection networks. Damage from electrostatic discharge can cause either complete device failure by parametric shifts, or device weakness by locally heating, melting, or otherwise damaging oxides, junctions or device components.


**PROCEDURE FOR TESTING ELECTROSTATIC DISCHARGE SUSCEPTIBILITY OF MOS DEVICES.**

19th Annual Reliability Physics Proceeding, Catalogue No. 81CH1619-6, April 7-9, 1981, pp. 200-203.

This paper delineates a method for determining the susceptibility levels of packaged devices to electrostatic discharge potential. This paper presents examples of protection network configurations, along with failure threshold levels, and the damage mechanisms.


**A NEW TECHNIQUE FOR INPUT PROTECTION TESTING.**

19th Annual Reliability Physics Proceeding, Catalogue No. 81CH1619-6, April 7-9, 1981, pp. 212-217.
Input protection circuits are evaluated in a typical manner by resistively discharging a capacitor into the tested device with some of its pins grounded. These techniques usually result in junction damage in or near the input protection circuit rather than in gate oxide ruptures as is seen in most electrostatic damage field failures. A new testing technique has been developed to eliminate this inconsistency.

Dechiaro, L.F. (Bell Laboratories, Allentown, PA).
ELECTRO-THERMOMIGRATION IN NMOS LSI DEVICES.

Electro-thermomigration of aluminum metallization through contact windows into the substrate accounts for many of the burn-in failures for certain NMOS LSI devices. The developmental history of this failure mode was studied by an analysis of the failed devices and by controlled electrostatic discharge stressing.

Stevens, N.J., F.D. Berkopec, and J.V. Staskus (Lewis Research Center, Cleveland, OH).
TESTING OF TYPICAL SPACECRAFT MATERIALS IN A SIMULATED SUBSTORM ENVIRONMENT.

A series of survey tests have been conducted in the Lewis Research Center substorm simulation facility. The test specimens were spacecraft paints, silvered Teflon, thermal blankets and solar array segments. The samples, ranging in size from 300 to 1000 cm$^2$, were exposed to monoenergetic electron energies from 2 to 20 keV at a current density of 1mA/cm$^2$. The samples generally behaved as capacitors with strong voltage gradients at their edges. The charging characteristics of the silvered Teflon, Kapton, and solar cell covers were controlled by the secondary emission characteristics. Insulators that did not discharge were the spacecraft paints and the quartz fiber cloth thermal blanket sample. All over samples did experience discharges when the surface voltage reached -8 to -16kV. The discharges were photographed. The breakdown voltage for each sample was determined, and the average energy lost in the discharge was computed.

Purvis, C.K., N.J. Stevens, and J.C. Ogley (Lewis Research Center, Cleveland, OH).
CHARGING CHARACTERISTICS OF MATERIALS COMPARISON OF EXPERIMENTAL RESULTS WITH SIMPLE ANALYTICAL MODELS.

An understanding of the behavior of materials, of dielectrics in particular, under charged particle bombardment is essential to the prediction and prevention of the adverse effects of spacecraft charging. This paper presents an effort to obtain such an understanding through a combined analytical and experimental approach. A one-dimensional model for charging of samples in the Lewis Research Center test facility is used in conjunction with experimental data taken in this facility to develop "material charging characteristics" for silvered Teflon. These characteristics are then used in a one-dimensional model for charging in space to examine expected response. Relative charging rates as well as relative charging levels for silvered Teflon and metal are discussed.

Lehn, W.L. (U.S. Air Force Materials Laboratory, Wright-Patterson AFB, OH).
CONDUCTIVE SPACECRAFT MATERIALS DEVELOPMENT PROGRAM.

The control of absolute and differential charging of spacecraft cannot be effected without the development of new and improved or modified materials or techniques that will provide electrical continuity over the surface of the spacecraft. The materials' photoemission, secondary emission, thermo-optical, physical, and electrical properties in the space vacuum environment both in the presence and absence of electrical stress and ultra-violet, electron, and particulate radiation are important to the achievement of charge control. The materials must be stable or have predictable response to exposure to the space environment for long periods of time. The materials of interest include conductive polymers, paints, transparent films and coatings as well as fabric coating interweaves. The program initiated by the Air Force Materials Laboratory (AFML) and related efforts to develop these new and modified materials will be discussed in this article.
This report presents an overview of the design, development, fabrication, and testing of transparent conductive coatings and conductive lattices deposited or formed on high resistivity spacecraft dielectric materials to obtain control of static charge buildup on spacecraft external surfaces. It discussed fabrication techniques for the deposition of indium/tin oxide coatings and copper grid networks on Kapton and FEP Teflon films and special frit coatings for OSR and solar cell cover glasses. The techniques include sputtering, photolithography, and mechanical processes. This report also describes a facility designed and built to simulate the electron plasma at geosynchronous altitudes along with test procedures. The results of material characterizations as well as electron irradiation aging effects in this facility for spacecraft polymers treated to control static charge are presented. The data presents results for electron beam energies up to 30 kV and electron current densities of 30 nA/cm². Parameters measured include secondary emission, surface leakage, and through the sample currents as a function of primary beam energy and voltage.

Belanger, V.J., and A.E. Eagles (General Electric Company, Space Division, Valley Forge, PA).

SECONDARY EMISSION CONDUCTIVITY OF HIGH PURITY SILICA FABRIC.


High purity silica fabrics have been proposed for use as a material to control the effects of electrostatic charging of satellites at synchronous altitudes. These materials have exhibited very quiet behavior when placed in simulated charging environments as opposed to other dielectrics used for passive thermal control of which exhibit varying degrees of electrical arcing. Secondary emission conductivity is proposed as a mechanism for this superior behavior. Design of experiments to measure the phenomena and data taken in GE research facilities on silica fabrics are discussed as they relate to electrostatic discharge (ESD) control on geosynchronous orbit spacecraft. Studies include the effect of varying electric fields impressed across the material under test.
A series of laboratory measurements have been performed to explore the effects of various external parameters on the conductivity properties of several typical and potential spacecraft insulating materials in a simulated space environment. The materials tested included Kapton, Teflon, quartz, and polyvinylidene fluoride. The parameters varied in these tests included sample thickness, temperature, applied voltage, illumination intensity and wavelength, and electron beam energy and current density. Tests were performed both with conventional optically transparent gold-front-surface electrodes and with the front surfaces of the test samples exposed directly to an electron beam. All tests were conducted in a vacuum chamber at a pressure of approximately 10^-6 torr. This paper summarizes some of the more interesting general properties of the materials tested.


A technique for determining the conductance per unit area of thermal control coatings for "electrostatically clean" spacecraft is described. In order to simulate orbital conditions more closely, current density - voltage (J - V) curves are obtained by a contactless method in which the paint on an aluminum substrate is the anode of a vacuum diode configuration with a tungsten filament cathode. Conductances greater than 10^-9 A/V cm^2 have been observed on black paints containing carbon and in white and green paints filled with zinc oxide which has been fired in order to induce defect conductivity. Because of surface effects and the non-homogeneous nature of paints, large discrepancies are found between measurements taken using the contactless method and measurements employing metallic contacts, particularly at low current densities. Therefore, measurements with metallic contacts are considered to be of questionable value in deciding the suitability of coatings for electrostatic charge control.


System Generated Electromagnetic Pulse (SGEMP) and Dispersed Electromagnetic Pulse (DEMP) are nuclear-generated spacecraft environments. Electrostatic Discharge (ESD) is a natural spacecraft environment resulting from differential charging in magnetic substorms. All three phenomena, though differing in origin, result in the same problem to the spacecraft: Electromagnetic Interference (EMI). A common design approach utilizing a spacecraft structural Faraday Cage is presented which helps solve the EMI problem. Other system design techniques are also discussed which minimize the magnitude of these environments through control of materials and electrical grounding configuration.


This paper discusses the relative importance of visual microscopic data as it pertains to recognizing the characteristic traits of semiconductor failures. This visual data can be a tremendous aid to the analyst in identifying the cause of semiconductor failure due to external influence. Residual damage observed on a microcircuit surface is often the result of temperature excursions localized at the chip surface. Temperature excursions that occur with certain types of damage to microcircuits are discussed in terms of voltage, current and time and are thereby related to the nature of the external abuse.

Also presented are case histories which describe the usefulness of these characteristic traits when applied during system failure analysis.


This article presents explanations by which spacecraft can get charged up by space
plasma, how this charge can cause malfunctions or failures, and ways this charge buildup can be controlled. It also presents a summary of the information obtained by the Scatha (spacecraft charging at high altitudes) satellite, flight P78-2.

15993

Beall, J.R. (Martin Marietta Corp., Denver, CO).
EBIC GENERATION, IMAGING AND TYPICAL APPLICATIONS.

Electron Beam Induced Current (EBIC) is a practical technique for locating and imaging subsurface defects in semiconductors. It is also practical to perform physical measurements using EBIC. The generation processes of EBIC in semiconductors and the techniques for measurement and imaging are described. Although the generation processes and imaging techniques are relatively straightforward, detailed interpretation of EBIC data requires a familiarity with semiconductor construction and layout. Examples demonstrating typical EBIC applications are described.

15994

McAteer, O.J. (Westinghouse, Baltimore, MD).
A CLUE FROM COLUMBO.
Quality, December 1980, pp. 54-55.

This article shows that there is more to failure analysis than sophisticated lab techniques. It compares electronic failures to a murder mystery where the failed part is regarded as the analog of the murder victim.

15995

DeForest, S.E., and E.C. Whipple (University of California, La Jolla, CA).
SPECIFICATION OF THE NATURAL PLASMA ENVIRONMENT AT GEOSYNCHRONOUS ORBIT.

The use of UCSD plasma instruments on board the ATS spacecraft could be used to specify an environmental mode which would be of use to the Air Force in developing design specifications for spacecraft to prevent faulty operation due to environmentally induced electrostatic charging.

15998

SPACECRAFT CHARGING.

If a spacecraft is exposed to a steady stream of current density, the charge of which is deposited on the surface of a cylindrical, conducting spacecraft, internal electromagnetic fields are generated. If the internal fields are of sufficient strength, undesirable electronic noise or damage may result. This thesis presents three approaches for calculating the induced E-field: separation of variables, variational calculus, and the use of Green's functions.

15999

SATellite SPACECRAFT CHARGING CONTROL MATERIALS.

The feasibility of conductive adhesive techniques for the electrical interconnection of ITO-coated second surface mirrors has been studied. The good electrostatic performance and the durability of components combining ITO-coated aluminized Kapton and aluminum straps by means of silver loaded silicone have been confirmed by a prequalification program.

The charge dissipation mechanisms for silica fabrics in a geosynchronous magnetic substorm environment have been studied by means of various sample configurations that have been tested under electron beam. Some recommendations have been given for a better use of silica fabrics as thermal control coatings in space.

16014

Kinzig, B.J., and H. Ravner (U.S. Navy, Naval Research Laboratory, Washington, DC).
PROBLEMS ENCOUNTERED WITH ANTISTATIC PACKAGING.

Packaging of miniature aerospace components in antistatic polyethylene or nylon is generally considered an attractive route to eliminate major problems in their handling and storage. Although most electronic components appear compatible with antistatic packaging materials, lubricated parts, such as precision ball bearings, can apparently be adversely affected. Surfaces exposed to lubricants, for example, may become nonwetted or the lubricant may become grease-like after relatively short exposure to antistatic containers. That such packaging adversely affects lubricated parts suggests potential problems involving unwanted surface-active effects for nonlubricated parts as well.
Our recent studies indicate that the surfactant material incorporated into the packaging film may be responsible for the adverse effects observed.

16015

UNDERSTANDING AND CONTROLLING ELECTROSTATIC DISCHARGE.

This component comment addresses the areas of comprehensive cost-effective methodologies for the control of electrostatic potentials. This component comment is organized as follows: Testing/Results, major concerns of Design (Reliability, Quality, Production services, and Procurement), Control Methods, and Conclusions. Voltage sensitivity ranges were Category I, 0-170v; Category II, 171-2000v; Category III, 2001 to 15000v; Category IV, 15001 and above.

16022

Dabkowski, J. (IIT Research Institute, Chicago, IL).
INVESTIGATE FEASIBILITY OF ELECTROMAGNETIC PULSE TESTING FOR RELIABILITY SCREENING OF SEMICONDUCTOR DEVICES.

Tests presently used for the screening of microelectronics are generally patterned after MIL-STD-883. In addition to the accepted screening tests, it has become apparent that an additional test procedure is necessary for some technologies. MIL-M-38510 incorporates a test requirement to qualify ESD protective circuitry on the CMOS chip.

EMP tests are primarily oriented towards establishing damage thresholds and failure criteria for semiconductors exposed to an electromagnetic pulse.

Due to thermal breakdown failure effects a commonality between accepted reliability screening tests and EMP tests can be shown to exist.

16055

Danley, L.W. (General Semiconductor Industries, Inc., Tempe, AZ).
PARAMETER TRADE-OFFS IN HIGH-VOLTAGE HIGH-SPEED SWITCHING POWER TRANSISTORS.

A continuing problem confronting the power supply designer is the selection of the "ideal" power transistor, one that provides not only high speed and high voltage but also good second breakdown capability, all within a single part. Current device technology, however, imposes interactive restraints upon these parameters, forcing compromises that are less than the designer's ideal component.

This paper presents an examination of these interactive factors in terms that are both familiar and meaningful to the power supply designer, providing a practical and useful baseline for the knowledgeable specification of state-of-the-art devices.

16067

COS/MOS ELECTROSTATIC-DISCHARGE PROTECTION NETWORKS.

RCA's two families of CMOS devices, the standard A series (3 to 15 volts) and the high voltage B series (3 to 20 volts), are equipped with networks to protect the gate oxide of the devices against damage resulting from discharge of electrostatic energy between any two pins. Figures show the various protection networks incorporated in all COS/MOS products.

16068

Albing, B. (Hickok Electrical Instrument Company, Cleveland, Oh).
COMPARATOR DETECTS POWER SUPPLY OVERVOLTAGES, CATCHES GLITCHES.
Electronic Design, Vol. 27, No. 15, July 19, 1979, p. 120.

Power-supply outputs can be monitored for intermittent overvoltage conditions by a comparator circuit that will light LED's and sound a beeper whenever a transient occurs. The circuit can be modified easily to latch the LED and beeper continuously on. This allows the circuit to run without constant monitoring.

16069

COPTING WITH STATIC ELECTRICITY - PART XIII, ARE YOU ALSO A VICTIM OF ESD?

This presentation will identify potential static problem areas within the working environment. The military hardware industry more than the commercial has taken great strides to educate its contractors on electrostatic discharge. The Navy has distributed two proposed documents for review.

16074


248
ELECTROSTATIC DISCHARGE (ESD) LIBRARY LIST.

This document is a library list of ESD articles prepared for the Naval Ship Engineering Center. The article gives library descriptors and separately categorizes articles relating to general information, device sensitivities, and ESD control/elimination.

16074-01
IDENTIFICATION OF SUPPLIERS OF ESD PROTECTIVE MATERIALS AND EQUIPMENT.

Sixty-two manufacturers are identified from various sources as potential suppliers of material and equipment for the protection of sensitive devices for electrostatic discharge. Supplies are categorized as antistatic plastic, conductive plastic, and equipment or tools.

16075
McDermott, J.
ZAP THE ZAPPER BEFORE IT ZAPS YOUR DESIGNS - IMPROVED ICS, PROTECTIVE COMPONENTS HELP.

Electrostatic discharge can destroy ICs at all stages of equipment manufacture, including quality control checks, board stuffing and testing, and even in field maintenance. IC and component manufacturers have developed a variety of products and techniques to deal with this problem.

16076
ELECTROSTATIC DAMAGE TO SEMICONDUCTORS.

The Reliability Analysis Center (RAC) has found it convenient to classify ESD sensitive devices into three groups. These groupings should be considered generalizations, and it is cautioned that damage thresholds within generic classifications can vary widely. When in doubt, individual part types should be tested for sensitivity.

ESD-type overstress can induce latent failure mechanisms in both MOS structures and bipolar junctions which are not necessarily detectable with typical electrical tests. The overstress degrades the device, making it susceptible to failure some time after initial voltage transients in applications where voltage excursions are encountered.

16114
DRIVING INDUCTIVE LOADS?

Most monolithic Darlington have a built in (C-E) diode that is usually ignored. This diode is capable of serving as a surge suppressor for inductive loads. Because the C-E diode is usually ignored its characteristics are seldom given in spec sheets. Measurements compare favorably with several discrete rectifiers.

Fast recovery rectifiers are characterized by low reverse-recovery times. They are not particularly fast on forward recovery. Moreover, when compared to standard or even fast recovery diodes, no major difference in circuit operation can be detected for C-E diodes as a result of variation in reverse-recovery times.

16115
PREDICTING THE STATIC BEHAVIOR OF FIBERS AND TESTING THE EFFECTIVENESS OF ANTISTATIC AGENTS.

The test procedure described here is designed to simulate the mechanism by which fibers become charged in actual mill operations. It is based on the theory that if a textile material cannot be charged with static electricity through friction against itself and certain other materials, static should be no problem.

16116
PHYSICS OF ELECTROSTATIC CHARGE GENERATION IN INDUSTRIAL PROCESSES.

The manufacturing process areas discussed in this paper are conformal coating/potting, hybrid facility, areas using cryogenic coolants, vapor degreasers, ultraviolet light inspection, vacuum pack processing, and Parylene coating process.

The Helmholtz effect-layer theory, Hertz effect and Van der Waals forces are used to explain charge generation. Spraying and dip coating was found not to generate electric charges. Nonoven drying causes a charge of 40 volts due to Van der Waals forces. Assemblies cured in laminar flow ovens are subject to charges when not grounded. Cryogenic cooling will cause charge generation due to the accumulation of moisture on the part with the
effect of Van der Waals forces. Ultraviolet light exposure greater than 30 minutes will cause charge generation because of the Hertz effect. Charges up to 80 kilovolts can be generated when removing a polyethylene sheet from its packaging. Handling processes such as wiping with Kimwipe can cause generation of 500 volts.

16117


The subject of EMP (Electromagnetic Pulse) has been developed into prominence in recent years because of potential nuclear threat. Although gas-filled spark gaps were originally designed to protect telephone apparatus from induced lightning surges they have exhibited fast turn-on characteristics when subjected to the much stronger EMP pulse. Response to laboratory simulated EMP pulses has shown that metal oxide varistors will also clamp fast rise time pulses but undergo reverse degradation upon multiple pulsing. Both devices have been used for large system protection subject to respective limitations of short turn on times and high voltage clamping.

16118


This study of electrical overstress reveals the cause of the failure and explains the appearance of a "zapped" junction. It demonstrates the dependence of long pulse type zap failures on aluminum alloying and migration.

16123


Topical antistats are generally liquids which, when applied, render a material static controlled. They consist basically of two components: 1) a carrier to transport the antistatic mechanism and 2) the mechanism which performs the preventive function.

A new approach to the static problem treats static as a symptom and environmental factors as the cause of it. It follows the thought that static is a natural phenomenon and to prevent it we must counteract the natural elements that create it.

16124


The type of damage which is produced by ESD is a function of the part characteristics, voltage level and polarity energy available and the rise/fall time of the ESD pulse. After the part is soldered to the circuit board, the attached circuitry connectors and arrangement of used interconnections may greatly influence ESD susceptibility.

16142


This report describes a method of organizing and implementing a standardized test method for evaluating ESD susceptibility of CMOS components. Also described are methods for detecting mechanisms of latent failure and other related phenomenon. Procedures for decapsulation and electrical probing of the die are also presented as a method of isolating the cause of failure. As shown by the results, the phenomenon of ESD is controllable and its effects statistically predictable.

16143


Military Specification MIL-B-81705 has been relied on to define static protective materials. Advancing technology has made its methods antiquated. The single most important characteristic of any packaging material is its conductivity. To fully characterize a film as being static protective, all that is needed is a resistivity test. Existing ASTM test procedures can be used.
A proposed electrical overstress (EOS) test method for MIL-STD-883, "Test Methods and Procedures for Microelectronics," was applied as a characterization and screening procedure to a population of gold doped 4002 CMOS devices. To evaluate the possibility of subsequent reliability degradation of devices passing the screen, a high temperature accelerated life test was performed on screened and unscreened devices. For screening, a voltage pulse of sufficient magnitude to fail about 3% of the parts was applied. No significant differences were detected between the failure rates of the screened and unscreened device populations.

Under certain conditions electrostatic discharge (ESD) can cause catastrophic failure in both bipolar and field effect transistor (FET) devices. This paper presents a test technique and describes a testing device that simulates ESD produced by human handling.

Many electrical and electronic devices and components are sensitive to Electrostatic Discharge (ESD). However, ESD controls generally have not been widely implemented by either industry or government. This lack of controls has resulted in increased costs, decreased equipment reliability and increased equipment downtime. To address these problems the Naval Sea Systems Command, under DOD Project Nos. RELI-014 and RELI-012, is developing a military standard and handbook on implementation of ESD control programs. Background, content and status of these documents are presented. Additionally, ESD areas requiring further work are discussed.
Testing has been conducted at The Charles Stark Draper Laboratory, Inc. (CSDL) on several typical or potential bench-top materials. The tests consisted of charging bench-top samples and then discharging them to a ground. All samples exhibited an exponential decay of voltage with time. The only exceptions were vacuum-baked samples of melamine and Benalux-type materials. The author is also certain that pink poly would be an exception if it were vacuum baked. All samples produced a visible static discharge arc when the charged test specimen was grounded.

The differential input pair transistors of an operational amplifier are susceptible to severe damage from EOS/ESD. Typical failure modes of TTL IC's include degradation of the I-V characteristic or short of the input protection diode. EOS/ESD can easily cause degradation of the electrical characteristics or catastrophic damage.

This paper briefly summarizes a study that was initiated to advance knowledge of Personnel Electrostatic Discharge (ESD) by developing descriptions of the "Source" waveforms resulting from the ESD of personnel associated with operation of Electronic Data Processing (EDP) systems. The study was extended to include measurements of the waveforms of ESD from (and through) mobile furnishings and the ESD of personnel through various handheld metallic objects that were intervening in the discharge path. The conceptual direction of this effort was aimed toward eventual development of ESD test simulation equipment and methodology, based on matching the waveforms found during the primary "source" evaluation effort through to the design of the test simulation equipment. From the standpoint of systems susceptibility performance, the conclusions provided by this effort have achieved good correlation in terms of systems operation in active-use situations. Although directed toward systems-susceptibility considerations, the waveform results of this study could easily be applied to equivalent circuit models for purposes of evaluating semiconductor device/component ESD damage.

Rutherford, D.H. (Raytheon Company, Electromagnetic Systems Division, Goleta, CA) and J. Perkins (Hi-Rel Laboratories, Inc., Monrovia, CA).

A large percentage of the microcircuits submitted for failure analysis that are actually defective have been found to be damaged by electrical overstress. It is not unusual to see 60 to 75% of actual failures the result of some sort of overstress conditions. Prior reports of failures of some digital microcircuits gives the impression that certain families of devices have different damage susceptibility levels. This paper describes a series of stress tests performed on several digital microcircuits and the failures that were induced. Procedures used for failure analysis of the damaged microcircuits are discussed.
printed circuit boards and 200 power supply assemblies that contain 10,000 multichip hybrid packages.

16155

Cabayan, H.S., F.J. Deadrick, L.C. Martin, and R.W. Mensing (Lawrence Livermore Laboratory, Livermore, CA).

STATISTICAL FAILURE ANALYSIS OF MILITARY SYSTEMS FOR HIGH-ALTITUDE EMP.


A study of general problems of dealing with uncertainties and their impact on failure analysis in assessment of EMP effects on military systems has suggested a probabilistic approach. Major uncertainties arise in both the interaction and coupling and susceptibility phases of assessment studies. A probabilistic approach, as outlined in this paper, can accommodate all sources of uncertainties. Although propagation of uncertainties by analytical methods is possible for very simple systems, the approach suggested is based on Monte Carlo methods and is possible using available computer programs such as FAST and NET-2. The results of the two simple experiments demonstrate the validity of the tools used and shows the potential usefulness for more complex systems.

16156

Clark, O.M. (General Semiconductor Industries, Inc., Tempe, AZ).

ELECTROSTATIC DISCHARGE PROTECTION USING SILICON TRANSIENT SUPPRESSORS.


The vulnerability of a semiconductor device increases as the slope of the transient voltage wavefront increases. The microstructures characteristic of new semiconductor technology are very fragile and are easily destroyed with the fast rise-time transients originating from electrostatic discharge (ESD). A new silicon transient suppressor structure has been developed specifically for clamping the fast rise-time of ESD and represents more than an order of magnitude improvement over conventional silicon suppressors. Effectiveness of both of these types of suppressors is evaluated and reported in this paper.

16157

Minear, R.L., and G.A. Dodson (Bell Telephone Laboratories, Reading, PA).

THE PHANTOM EMITTER - AN ESD-RESISTANT BIPOLAR TRANSISTOR DESIGN AND ITS APPLICATION TO LINEAR INTEGRATED CIRCUITS.


The immunity of an NPN IC transistor to ESD damage can be markedly improved by simple design changes. The resulting "phantom emitter" transistor used in bipolar op-amp circuits makes their inputs much more damage resistant. The "phantom emitter" diffusion is shorted to the normal base contact by metal and plays no part in normal device operation.

16158


ELECTRICAL OVERSTRESS VERSUS DEVICE GEOMETRY.


Each section of a CMOS quad two-input NOR gate was independently stressed. The resulting failures can be related to device geometry. Review of the test data indicates excessive quiescent leakage (I_{SS}). The failures occurred farthest from the V_{SS} contact. The higher input diode resistance results in a higher voltage drop and increased dissipation. An additional P-well contact was proposed to reduce the voltage drop.

16159

Soden, J.M. (Sandia Laboratories, Albuquerque, NM).

THE DIELECTRIC STRENGTH OF SILICON DIOXIDE IN A CMOS TRANSISTOR STRUCTURE.


It is important to know if the processes required to fabricate the MOS device structure such as oxide etch and regrowth and topographical features such as edges and steps have significant effect upon the SiO_2 gate oxide maximum dielectric strength. Also important to know is how gate oxide defects in the MOS structure affect this maximum dielectric strength. The primary breakdowns occurred at topographical edges at the gate/field oxide interface and the secondary distribution of breakdowns at random locations in the central region of the gate. The maximum dielectric strength in the primary distribution is within about .5MV/cm of that reported for uniform thickness SiO_2 in capacitor studies.

16160

Teng, T., A.R. Hart, and A. McKenna (Hewlett-Packard Co., Corvallis Division, Corvallis, OR).

SUSCEPTIBILITY OF LSI MOS TO ELECTROSTATIC DISCHARGE AT ELEVATED TEMPERATURE.

An investigation of random failures during 125°C burn-in of LSI MOS Memory devices led to a study of the effects of elevated temperature on ESD susceptibility. An experiment was conducted on the ESD susceptibility versus temperature on MOS LSI devices including PMOS, NMOS, and CMOS devices produced by three IC manufacturers. A reduction in ESD failure voltage (Vf) is found at 125°C compared with room temperature levels. An explanation of bulk doped silicon resistivity variation in the input junction protection diode versus temperature combined with processing nonuniformities is offered and supported with a simplified power and current model and physical failure analysis.

This phenomenon affects high temperature testing used for life test, activation energy determination, receiving inspection, outgoing screening, Hi Rel and military specification testing and MOS applications in extreme temperature environments.


The damaging effects of a 20 MHz damped sinusoid on 18 types of powered devices are presented. Failure levels are given in terms of peak currents and voltages. The three most sensitive devices are also modeled in terms of failure energy and failure modes are presented.


This paper describes qualitative results of the work to date and is intended to show only general trends. A quantitative analysis of the junction burnout problem remains to be analyzed, and these results will appear in a later paper. The justification for going to more than a simple one-dimensional analysis is described. The extension of the 1-D to 2 or 3-D analysis is briefly explained and has been restricted to what has been learned from the viewpoint of power dissipation. Folding-in temperature effects serve generally to wash out the basic results that are best illustrated by studying the initial power dissipation.


Second breakdown is generally regarded as one of the principal failure modes of silicon electronic components.

The susceptibility of a particular device to second breakdown depends upon device geometry, spacings, contours, doping levels and heat sinking. The filamentation process involves large currents in a small region of space in short intervals. In modeling the high current pulse effects on P-N junctions, there is an interval when devices are ballasted by the junction voltage; however, when the temperature of the junction becomes high enough the voltage drops precipitously and the filament evolves rapidly.


The heart of an effective ESD control program is commitment to the program by production operators throughout the facility. The unseen nature of electrostatic damage makes it much more difficult to control than the usual quality defects. Consideration of small work group behavior in the design of electrostatic control programs will lead to real acceptance of electrostatic work rules.


Second breakdown in bipolar transistors has been divided into two regimes, forward and reverse. The phenomenon of thermal instability and its relationship to forward bias second breakdown is well understood; the events preceding reverse bias second breakdown are not well understood. Data curves show that the voltage at which second breakdown occurs decreases as the reverse bias increases. This supports the theory that the
focusing of current to the center of the emitter fingers during turnoff is the mechanism that leads to reverse bias second breakdown.


Square and RF pulse overstress data for bipolar UHF transistors are compared. For pulses incident upon the base-emitter terminals the pulses with lowest energy required to cause device failure were reverse polarity square pulses. The comparison indicates that a data format of absorbed pulse energy up to time of failure vs time to failure is well suited for comparing data produced by different types of signals.

With the understanding of second breakdown, one should be able to design devices less susceptible to burnout. The electrothermal computer program has been used to study second breakdown in linearly graded, double- and single-sided abrupt and diffused junction diodes. Tentative design principles are given.


A recently developed platinum-silicon Schottky barrier diode was found to be least sensitive to burnout by electrostatic discharge. Electrostatically burned-out diodes from both natural and circuit simulation techniques exhibited failure points at the periphery of the diode junction similar to that observed for RF burnout depending on junction parameter. A strong correlation exists between electrostatic and RF burnout of Schottky barrier diodes.


The operational amplifier, sample hold amplifier and comparator all share a similar input stage configuration — the bipolar differential input stage. If we apply an ESD pulse to either the inverting or non-inverting input with the other grounded, then there is a conduction path involving both a forward and reverse biased P-N junction.

A second classification of analog circuits is CMOS analog switches and multiplexers. Degradation may occur in three areas: switch cell; address cell; and decode. Switch cell degradation can be both MOS dielectric and P-N junction damage that may result in input-output off state isolation degradation as a result of PN junction damage or solid DC voltages and switching waveforms, depending upon damage location in the MOS dielectric. The address cell is susceptible only to MOS dielectric structure damage destroying the input MOSFET gate. The decode degradation, though an internal circuit structure because of small geometry MOSFETs, can be compromised through the capacitive divider model.


TransZorbsT.M. have been proven to be effective in suppressing fast rise-times, EMP type transients. Small in size, having sub-nanosecond response times and with current handling capabilities at levels of more than 500 amperes, TransZorbs have been found to be suitable in many transient protection applications. This paper describes what TransZorbs are, how they work, and how to employ them for EMP protection. Results of pulse testing are given, along with a description of capacitance effects and means to reduce these effects. Various hybrid schemes in which TransZorbs are used in conjunction with other types of protective devices are also discussed.


Tests on air ionizing grids were conducted to determine which grids would
reduce to less than 100v a static charge of 15kv. The companies that submitted their products to independent testing were Scientific Enterprises, Static Inc., Simco and Westcorp. The laminar flow hood used in the experiment was a vertical down flow type made by Dexon Corp.


Certain commercially available components have been tested to establish test procedures for characterizing terminal protection devices used in electromagnetic-pulse (EMP) applications. The devices tested include spark gaps, filters, avalanche diodes, and various other nonlinear components. Response time and energy leak were recorded for each test. Insertion loss and approximate failure level were measured for each device. Results are presented in tabular form. The devices that appear suitable for terminal protection include spark gaps, some filters, and some semiconductor devices with breakdown voltage less than 50.


The objective of this report was to determine the effects of stressing semiconductor devices with EMP-like transients. The effects of EMP stressing on the devices was assessed by comparing the observed failure rates of the various samples under these accelerated life test conditions.


This report presents user information for the computer code Supersap 2. Supersap 2 is a data storage and retrieval program. It is designed to manipulate data from two large data bases in support of EMP susceptibility threshold analysis. The component data base contains data on approximately 86,000 electronic component types. The system description data base is user defined. Supersap 2 uses a command language to provide user control of a variety of data manipulations.


The need for electrostatic discharge (ESD) awareness on the part of personnel at typical electronic manufacturing facilities is described. Some of the underlying reasons for intuitive disbelief in the static problem are discussed as well as the consequences of nonawareness. The development of an effective training program and proper manner of delivery to the appropriate personnel is presented.


This article indicates that bipolar devices can be damaged by static electricity. The three basic failure characteristics of TTL gates subjected to electrostatic discharge are base-emitter junction shorts, partial oxide passivation layer breakdowns resulting in high leakage currents, and open metallization.


An effective static protection program includes setting up a static protection system, employee education and awareness, and regular monitoring of work areas. This article presents an overview of static generation, dissipation, and protection methods.

Voltage clamping levels for the 1N5629A, 1N5545A, 1N5654A, and 1N5664A TransZorbT silicon transient-suppression devices in a DO-11 package are presented as data in photographs of test waveform. A graph is compiled which illustrates the clamping voltage at a point of 80nsec for each of the devices. The duration of the test pulse was 250nsec with a slope of 4KV per nsec for the rise portion. Clamping levels are nearly constant for test current amplitudes for up to 120A.

This is a list of references compiled by 3M Static Control Systems relating to the theory and experiment of static electricity.

16376
Adair, R.P. (Unitrode Corporation).
TRANSIENT-VOLTAGE SUPPRESSORS SUIT PC-BOARD PROTECTION NEEDS.

When transient voltages occur, system voltages and currents can surge to levels many times greater than their steady state values, permanently damaging semiconductor components. Zener transient-voltage suppressors offer a simple inexpensive method of shunting aside these transients before they reach sensitive components.

16377
Formanek, V.C., and I.M. Mindel (IIT Research Institute, Chicago, IL).
EMP TO ESD VIAP DATA CONVERSION AND CONSIDERATIONS.
1979, 30 pp.

The physical damage mechanisms for ESD and EMP are basically the same. The principal differences are the voltage source and coupling mechanism resulting in different driving voltage waveforms and source impedances. The principal objective of this report is to find common or equating parameters between EOS and ESD.

16378
Myers, S. (Honeywell, Aerospace Division, St. Petersburg, FL).
A TOTAL APPROACH TO ELECTROSTATIC PROTECTION IN THE PRODUCTION ENVIRONMENT.

Static electricity can never be completely eliminated but it can be controlled. Today electronic environment demands that each and every packaging engineer accept his responsibility to see that electrostatic discharge is properly addressed.

This article provides information that will aid him in meeting this responsibility.

16379
SELECTED REFERENCES TO THE THEORY AND EXPERIMENT OF STATIC ELECTRICITY AND ELECTROSTATIC DAMAGE TO ELECTRONIC DEVICES.
November 1979, 16 pp.

Gaspard, K.R. (Honeywell, Inc.).
ELECTROSTATIC DISCHARGE (ESD) STUDY.

This report documents the results of a study to develop an ordnance document which defines: electrostatic discharge sensitive parts; requirements for handling, shipping, storage, and testing of these parts; and methods to assure conformance to these requirements. Included in this report is the completed document written in military standard format along with back-up information discussing electrostatic discharge theory and applications and the categorization of purchased parts into four major electrostatic discharge sensitivity levels.

16475
Sankar, A., and T.S. Lin (TRW Systems Group, Redondo Beach, CA).
GENERALIZED ELECTROMAGNETIC VULNERABILITY PROBLEMS.

This paper has three purposes. The first is to propose a thesis that a system approach is needed to solve any electromagnetic vulnerability (EMV) problem in a comprehensive manner. The second is to present a generalized analysis approach to assist the system designer to optimize system and equipment performance through EMV analysis and control. The third is to enumerate and highlight the basic similarities and differences among the various available and applicable engineering "fixes" and design practices to solve EMV problems.

16476
Madzy, T.M. (IBM Corp., System Products Division, Endicott, NY).
STATIC DISCHARGE MODELING TECHNIQUES FOR EVALUATION OF INTEGRATED (FET) CIRCUIT DESTRUCTION.
Under certain environmental conditions, electrostatic discharge can cause catastrophic failure in both bipolar and FET integrated circuits. This paper presents a technique to test FET devices using a simulated human static discharge and also presents a mathematical model that can predict a catastrophic failure as a function of voltage developed across the FET device and the energy dissipated. Both theoretical and experimental data are presented.

Clark, O.M. (General Semiconductor Industries, Inc., Tempe, AZ).
SUPPRESSION OF FAST RISE-TIME TRANSIENTS.

Highly specialized silicon pn junction devices have been developed for suppressing fast rise-time transients associated with induced lightning and EMP. Methods for low inductance insertion and techniques for effective reduction of capacitance will be both illustrated and discussed in this paper. Hybrid technology using the best qualities and both gas-filled spark gaps and silicon junction devices will be characterized including applications, capabilities and limitations.

Clark, O.M. (General Semiconductor Industries, Inc., Tempe, AZ).
SUPPRESSING TRANSIENT VOLTAGES TO FCC 19528, PART 68.

This application note is intended to provide background information and design criteria for combining TransZorbs and gas surge arresters for protection of Telecommunication equipment against harmful transient voltage effects as described in FCC Docket 19528, Part 68.

Clark, O.M. (General Semiconductor Industries, Inc., Tempe, AZ).
A GUIDE FOR TRANSIENT SUPPRESSION USING TRANSZORB.

This paper discusses the nature of transient voltages; protective measures and their effectiveness, along with some specific applications unique to the TransZorb.
protectors suitable for the protection of low-voltage solid-state components.

16490

Huddleston, G.K., and G.G. Bush (Georgia Institute of Technology, School of Electrical Engineering, Atlanta, GA).
LIGHTNING PROTECTION FOR STATUS AND CONTROL LINES OF THE MARK III INSTRUMENT LANDING SYSTEM.

Solid-state circuits connected to buried control cables are susceptible to damage from surges induced on the cable conductors by lightning and electromagnetic pulse. The lightning protection requirements for solid-state circuits of the Mark III Instrument Landing System which are connected to buried control cables are presented in this paper.

16491

Vance, E.F. (Stanford Research Institute, Menlo Park, CA).
EMP-INDUCED TRANSIENTS IN LONG CABLES.

Sensitivity of modern components and circuit-design techniques to transient upset or damage is increasing. For this reason it is important that the system designer recognize the potential problems of transients induced on power, communication, and other long interconnecting cables. This paper discusses the currents induced in such cables by high-altitude nuclear EMP and suggests some protective measures that may be used by the circuit designer.

16493

Brundrett, G.W. (Electricity Council Research Centre, Chester, CH16ES, Gt. Britain).
A REVIEW OF THE FACTORS INFLUENCING ELECTROSTATIC SHOCKS IN OFFICES.

This article deals with personal electrical parameters and the effect of electrostatic buildup with the wearing of different clothing. It also covers the capacitance and personal sensitivity to shock difference between men and women, physical generation factors of material and the effect of weather. It also identifies the choice of solutions now available to the designer.

16502

Martin, L.C. (Lawrence Livermore Laboratory, University of California, Livermore, CA).
COMPARATIVE EMP DESIGN PRACTICES.

The nuclear electromagnetic pulse creates potentially severe problems in hardening against electromagnetic effects. Each hardening effort is usually supported through development or application of sets of rules, practices, constraints, etc., which aid in decision-making through the design process. This paper addresses the nature of many such practices and provides specific comparisons for a number of them taken from several relatively independent sources.

16504

EFFECTS OF EMP INDUCED TRANSIENTS ON INTEGRATED CIRCUITS.

This paper presents the results of testing by RCA of fourteen types of integrated circuits to determine their short pulse failure threshold. The primary intent of the tests was to determine for each circuit what would be the lowest amplitude of pulse which would cause permanent damage and prevent the circuit from operating. For these tests it was preferred that the actual devices and the circuits in which they are employed be measured. Pulses used during the tests ranged from 25 ns to 20 us, with emphasis on the range below 1 us.

16505

Latorre, V.R., and L.R. Spogen, Jr. (University of California, Lawrence Livermore Laboratory, Livermore, CA).
INGREDIENTS OF PROTECTION ENGINEERING.

A basic protection engineering concept is developed for the protection of an electronic/electrical system from an electromagnetic environment. The concept is general and therefore applicable to many systems. It consists of five stages. A detailed discussion of all functions performed in each
stage is described, the input data to these functions identified, and, means by which the functional operations are satisfied are summarized.

16506


Presented in this paper are the testing results by RCA of various types of integrated circuits to determine their short pulse failure thresholds. The circuits investigated are interface ICs, which are prone to damage by transient pulses coupled into cables electrically connected to the IC.

16507


ESD controls have not been widely implemented by either industry or government. This lack of control has resulted in increased cost, decreased equipment reliability and increased equipment downtime. The Naval Sea Systems Command has developed MIL-STD 1686 and MIL-HDBK-263 for implementing ESD control programs. This article is abstracted from a background-and-status report on the MIL-STD and MIL-HDBK prepared by E.J. McMahon and T.N. Bhar, Reliability Sciences, Inc., and Toshio Oishi of the Naval Sea Systems Command. ESD areas requiring further work are also discussed.

16555


This report describes the work done to determine the extent to which the reliability of integrated circuits suffers when those integrated circuits contain small cracks (microcracks) in their metallization. It was hypothesized that microcracked devices would undergo metallization at lower current pulses than unmicrocracked devices. The microcracked devices in this study did not suffer metallization burnout (MBO) at a level significantly different from the uncracked devices.

16564


This article consists of Honeywell Defense Systems Division’s results from several studies on ESD control products. It also recommends some solutions to the problems that were encountered and suggests where and when the products should be used.

16565


This specification describes procedures that are to be used when handling and packaging semiconductor devices that have been identified as being susceptible to surge current damage.

16632


A description of the design, development, fabrication and testing of transparent conductive coatings and conductive lattices deposited or formed on high resistivity spacecraft dielectric materials to obtain controlled static charge buildup on spacecraft external surfaces is presented. Through development of sputtering techniques and thin film evaporation methods, FEP Teflon and Kapton have been successfully modified to eliminate discharges on surfaces as a result of being exposed to electron beam energies of 25 keV and a current density of 30 nA/cm². Processing methods have been described for indium oxide and indium oxide/tin oxide coatings on FEP and Kapton, and fabrication techniques for grounding techniques are discussed.


The charging and subsequent discharging of high surface charges which are generated on non-conductive satellite surfaces have been identified as one of the chief causes of spurious performance of Air Force satellites. These discharges can cause upsets in the electronics systems which disrupt the normal functioning and data transmission of the satellite. A description is presented of the development, fabrication and testing of transparent conductive coatings deposited on the spacecraft and modifications to high resistivity transparent spacecraft dielectric materials to obtain control of static charge buildup on the spacecraft external surfaces.

16634

Tompkins, J.E. (Harry Diamond Laboratories, Adelphi, MD).


Estimates are made of the emission and resulting Compton currents, air conductivities, and electric fields produced by high-energy neutrons from a nearby nuclear detonation incident on an iron plate. Results for 14-MeV neutrons indicate that appreciable Compton current and electric field are generated in the immediate vicinity of an iron plate due to the neutrongamma reaction process. The magnitudes of the electric fields are such that the phenomena should be considered when assessing the survivability of armored-vehicle mounted military communications equipment.

16669


The approach taken in the paper is to present cloud physics theory as it is now understood from work carried out in the Chemical System Laboratory over the past 15 years. Experimental data then are presented with appropriate literature references, to show that the agreement between experiment and theory is so good that little room is left for traditional interpretations of certain phenomena.

16683


Many electronic parts are susceptible to damage from electrostatic discharge (ESD). ESD control programs are required to protect these parts during manufacture, assembly, test, repair/rework, maintenance, and other handling operations. Such control programs must be implemented throughout the life cycle of these electronic parts. The intent of this training manual is to complement an ESD Awareness Training Course, which is a key part of any effective ESD control program.

16692

*Rupe, B.I. (U.S. Navy, Naval Avionics Center, Indianapolis, IN).


This paper describes a test adapter designed in accordance with formulas stated in ANSI/ASTM D257 for determining the surface resistivities of materials using the concentric ring contact method. "Fringing" effects are virtually eliminated and calculations are reduced to an X 10 multiplication factor. Problems of electrical contact with slightly uneven hard surfaces are solved by the mechanical properties.

*Presently employed by the Reliability Analysis Center, Griffiss AFB, NY.

16693


**COPING WITH STATIC ELECTRICITY - PART XXIV, AN INEXPENSIVE FIXTURE DESIGN FOR MONITORING SURFACE RESISTIVITY.** Evaluation Engineering, July/August 1981, pp. 28-32.

This paper presents a fixture design that can be used to measure the surface resistivity of static control materials. The fixture is inexpensive to fabricate, utilizes readily available materials and common fabrication techniques, and can monitor the surface resistivity of a variety of material configurations.
Weigl, J.W.
ANTISTATIC FOOTWEAR.

This article consists of a non-confidential disclosure of the technology of antistatic shoes, shoe soles and heels. John W. Weigl's patent for the antistatic footwear is also included.

IMPROVING CMOS INPUT PROTECTION.
20 pp.

This report presents the results of an investigation which was launched to determine how much energy could be capacitively discharged into CMOS input protection circuitry before device failure occurred. An analysis was made to determine what mechanism had degraded which component of the input network. Several layout designs were considered, and simplified equivalent circuit models were drawn and characterized. The resultant information was then used to propose design guidelines and methods of improving input ruggedness and reliability. A topological layout was derived for recommended use in future CMOS integrated circuits.

THE MYTHS AND REALITIES OF ELECTROSTATIC DISCHARGE.

This article discusses misconceptions about electrostatic discharge that are cause for alarm. It is hoped that this article has taken a step towards convincing the reader that ESD is real and will surely continue to become a more significant problem unless the necessary precautions are taken.

Whalen, J.J., M.L. Thorn, E. Rastefano (State University of NY at Buffalo, Amherst, NY) and M.C. Calactera (Air Force Avionics Laboratory, Wright Patterson AFB, Dayton, OH).
MICROWAVE NANosecond PULse BURNOUT PROPERTIES OF ONE MICRON MESFETs.

Two dominant failure modes in overstressed MESFET's have been observed. One is the gate-to-source low resistance path (5 to 25 ohms) which frequently is correlated with metal migration (mainly gold) from the source metallization to the gate metallization. This failure mode was dominant when MESFET's failed at lower power levels as at 1.5 nsec. The other dominant failure mode is either a reduction in IDSS or a drain-to-source short which is correlated with massive damage in the channel region between source and gate metallizations. This failure mode was dominant when MESFETs failed at this power levels as at 1.5 nsec.

Ochoa, A., and P.V. Dressendorfer (Sandia National Laboratories, Albuquerque, NM).
A DISCUSSION OF THE ROLE OF DISTRIBUTED EFFECTS IN LATCH-UP.

Latch-up in monolithic integrated circuits is caused by the activation of four-layer SCR paths in certain technologies. A lumped element cross-coupled bipolar model has been widely used to discuss this parasitic SCR action with reasonable success. In the push toward VLSI structures, latch-up modeling and prediction based upon the simple model has proven inadequate. The deviations can be explained by an extension of the model into a network that couples parallel paths and by ensuring that measured parameters for the model reflect those of the latch-up situation. This paper discusses these points to allow the continued use of the lumped model in latch-up studies.

Anon.
ESD-CONTROL STILL IN INFANCY - BUT GROWING.

Electronic device manufacturers are still unaware as to how serious ESD damage can be, and many who are aware are unwilling to spend what it costs to develop adequate ESD-control programs. This is the opinion of almost five dozen companies across the country involved in...

262
manufacturing ESD-control products or providing ESD-related services.

16949


A computer-aided procedure for performing integrated circuit latch-up analyzer is presented. The procedure is the result of merging a computerized integrated circuit design rule checking system with latch-up preventative design rules. The procedure was applied to an IC which was previously analyzed by hand. The results were exactly the same, except that it only took 4 hours with the computer-aided approach and 80 hours with the manual procedure. Also discussed are plans for additional improvements to the system.

16950


Four-layer latch-up is a phenomenon which can occur in integrated circuits because of the presence of parasitic nppn paths which if properly biased may be triggered "on" by ionizing radiation. This can prevent the operation of the circuit until the power supply bias is reduced to a value low enough to break the latch.

This paper presents a latch-up analysis procedure for four-layer (pnpn) latch-up and applies it to specific bipolar LSI devices which represent several current bipolar LSI technologies. The results of the analysis were verified by radiation tests.

16951


Four-layer parasitic SCR paths exist in bulk CMOS integrated circuits which can be activated by transient ionizing radiation, by overvoltage stress, and by other means causing latch-up. These parasitic SCRs often have characteristics which are not explained by simple SCR theory. This paper analyzes a cross-coupled transistor model to explain how these characteristics can occur in parasitic four-layer paths.

16955


The need to control static in electronic assemblies is gaining recognition in the industry. Yet many test engineers are not aware that electrostatic discharge (ESD) can wreak havoc during testing a multilayer bare board. This article describes an experience which demonstrates that ESD problems can occur in the unlikeliest places. It also gives corrective actions that may be taken to control ESD problems in those places.

16961


The objective of this study is to recommend hardware marking guidelines to be incorporated into DOD-HDBK-263 (excluding Electrically Initiated Explosive Devices), dated 2 May 1980. The present issue of DOD-HDBK-263 provides limited guidance in marking hardware.

17013


This document establishes common procedures and precautionary measures for the protection of ESD sensitive devices and components. Work station, clothing, protective packaging, and design documentation are covered in detail.

17016

Transient overvoltages occurring in low-voltage ac power circuits can be the cause of misoperation and product failure for residential as well as industrial systems. This guideline describes what is known and what is not known about the environment, with recommendations on how to cope with the situation.

The origin of transient overvoltages -- lightning and load switching -- are discussed in the context of ac circuits of less than 600V. Available data on frequency of occurrence as a function of voltage levels are presented. Waveshape of 'representative' transients are discussed and a proposal made for a simple test wave. Energy and source impedance of the transients are discussed with reference to the energy-handling capability of available transient suppressors. Power system size and energy of transients are compared.


MODELING THE EFFECTS OF LIGHTNING ON ELECTRICAL EQUIPMENT.

A model was developed for computing the safety and reliability of electrical equipment in a lightning environment. The model specifies the parameters of lightning that are pertinent in causing damage to equipment. This report indicates how the model is to be used for testing equipment to determine failure levels. Using these failure levels, it also shows how to compute the actual safety and reliability to be expected in field use, where lightning is a threat.


FAA LIGHTNING PROTECTION STUDY: RELIABILITY LIFE OF LIGHTNING PROTECTION DEVICES UNDER SIMULATED LIGHTNING CONDITIONS.

This report deals with the experimental design of reliability life testing program, with its implementation, and with the analysis of failure data generated. Four different types of lightning protection devices were tested under simulated lightning conditions. Nineteen MOV failures and twenty-four TransZorb failures were observed out of a total testing sample of 50 and 55, respectively, when subjected to approximately 150 surges of simulated lightning energy.


POWER SUPPLY VOLTAGE TRANSIENT ANALYSIS AND PROTECTION.

A voltage transient is an unexpected change in voltage caused by an unpredictable occurrence. Voltage transients and power surges differ by their causes, magnitude, destructive capabilities, and energy. The technology for suppressing the two are often quite different too. Transients are characterized by high-voltage departures which are less than 8.4 milliseconds in duration. Power surges are characterized by low voltage excursions, lasting greater than 8.4 milliseconds. This paper separates transients into four categories: lightning, EMP, static discharge and inductive switching. It deals primarily with the transients associated with inductive switching; however, with proper component selection and design consideration, the transient suppressor can protect a system from all transient sources. Lightning, EMP, and static are each a study into themselves, but are briefly discussed in this paper.

Sabaroff, S. (Hughes Aircraft Company, El Segundo, CA).

STATIC ELECTRICITY CASE HISTORIES.

The major sources of static charge are on or near the earth. The list could include fuel handling, plastics, rocket engine charging, precipitation, friction, lightning, booster separation and many others. Static charge buildup on spacecraft and humans has been investigated throughout the industry. Transistor and SCR failures have also been related to static effects.

Rogers, P.R. (General Electric Company, Philadelphia, PA).

TRANSIENT COMPATIBILITY MEASUREMENTS IN SPACECRAFT.

The capability of measuring broadband and narrowband frequency domain voltages has existed for many years; in many given systems the fundamental and most spurious frequencies are known. The source of interfering
transients is usually the operation of relays, tuning components, and other high current level changes mostly on main power buses.

**17077**

Whittlesey, A.C. (Jet Propulsion Laboratory, Pasadena, CA).

SPACECRAFT INTERFACE CIRCUITRY SENSITIVITY ANALYSIS. 


The study presented concerns Mariner/Mars Spacecraft. This study was done after the spacecraft was conceived, designed and launched into space. It was limited to intersubsystem problems because of the way the JPL builds.

**17078**

Schenker, B. (Lockheed Missiles & Space Co., Sunnyvale, CA).


Two methods of transient voltage measurement at selected critical points in an aerospace vehicle are described in this paper. These measurements are for the purpose of injecting 6dB higher voltages into aerospace vehicles to demonstrate compliance with specification MIL-E-6051C. Both methods have given positive results in attaining the required objective, but the memory voltmeter/oscillograph combination is preferred because of its simplicity. This latter method is planned to be used in future EMI system compatibility tests.

**17079**


CONTROL OF ELECTROSTATIC INTERFERENCE IN SPACECRAFT.


A study of various electrostatic phenomena will show that both an insulating material and a charging mechanism are always involved. The charging mechanism involves motions of particles, liquids, gases, or in some instances the insulating material itself. There is one factor that can be controlled to some degree: the resistivity of the materials exposed to these charging mechanisms. If conductive materials were always used no electrostatic charge could be developed, and a situation that could be called electrostatic compatibility (ESC) would exist.

**17080**

Hoffart, H.M. (General Electric Co., Valley Forge Space Technology Laboratories, King of Prussia, PA).

THE CONCEPT OF SINGLE-POINT GROUNDING.


Grounding concepts must be designed on a system level rather than on an individual equipment basis because of interface requirements. Effective grounding is not difficult to achieve if properly approached within the discipline of electromagnetic compatibility. The single-point grounding concept is shown to exhibit advantages if effectively implemented. The use of litzwire due to the interweaving of insulated strands will display a low impedance characteristic up to the low MHz area of the frequency spectrum. At the subsystem end, litzwire is used to separately reference the signal and static grounds.

**17082**


REDUCING CONDUCTED EMI WITH A NEW ULTRA-LOW-CAPACITANCE SWITCHING TRANSISTOR CONFIGURATION.


A brief review of the various sources of EMI in the switching power supply is presented. Capacitive coupling of the transistor collector (case) to ground is shown to be a major cause of conducted EMI.

Conventional solutions (e.g., "screened heatsinks") are examined and shown to be much less than optimal. The isolated TO-3 is presented as an effective solution to this problem. Electrical, thermal, and mechanical properties are compared to "standard" configurations. Data showing the comparative reduction in conducted EMI (obtained by an independent testing facility) is provided.

**17151**

Hyatt, H., H. Calvin, and H. Mellberg (Experimental Physics Corp., Hayward, CA).

A CLOSER LOOK AT THE HUMAN ESD EVENT.


This paper presents some of the electronic industry’s tests and procedures for simulating human ESD and how observed ESD events relate to these industry-designed tests. Risetime and leading edge structure of an ESD event is determined by several independent elements in the discharge path:
specifically, the corona losses prior to and during spark formation, electronic structure of the complete discharge circuit, spark formation processes, and the circumstances immediately prior to discharge. Industry test procedures are not consistent and span a greater range of transients than is typical for an ESD event. Limitations on the previously mentioned independent elements in the discharge path must be considered when simulation standards are specified. These constraints lead to a new model for the human ESD circuit.

17152
QUANTITATIVE EFFECTS OF RELATIVE AND ABSOLUTE HUMIDITY ON ESD GENERATION/SUPPRESSION.

The importance of ESD control is widely recognized, but effective and efficient control techniques are still being developed. Grounding through use of conductive floor tile, bench tops, packaging, and wrist straps have been effectively used. Widespread control of ESD has been achieved by environmentally limiting charge build-up using slightly ionized air or maintaining plant and laboratory humidity at a suitably high level.

17153
ANALYSIS OF ELECTROSTATIC DISCHARGE FAILURES.

Identification of ESD problems can be difficult without the use of sound failure analysis procedures. This paper highlights some of the techniques that have proven the most beneficial in identifying the cause and corrective action for static failures. Some key steps that are frequently valuable in ESD analysis are circumstantial evidence of static accumulation, failure duplication tests, chemical etching, liquid crystals and scanning electron microscopy.

17154
THE PERFECT "10" - CAN YOU REALLY HAVE ONE?

The Douglas Aircraft Company, after researching numerous papers and investigations in the area of reliability failure analysis and semiconductor physics, concluded that only a relatively small amount of ESD damage resulted in hard or reported failures. Douglas realized that regardless of the quality of their own ESD protection program, their ESD program would never be a perfect "10" unless everyone from manufacturer, system assembly houses, their customers, the military, and commercial airlines had comparable programs. In this effort to achieve the "10" goals, Douglas embarked upon an informative program.

17155
THE ECONOMIC BENEFITS OF AN EFFECTIVE ELECTROSTATIC DISCHARGE AWARENESS AND CONTROL PROGRAM - AN EMPIRICAL ANALYSIS.

An increasing awareness of IC failures at the device, circuit pack, and PBX system levels prompted an investigation of possible electrostatic discharge damage to semiconductor devices when handled either individually or in circuit packs. Discussions were held with engineers who studied and solved the same types of problems on a smaller scale at other Western Electric plants. Several suppliers of static control equipment were also consulted. This was followed by a Denver Works In-House study that revealed the need for implementing the ESD Awareness and Control Program described.

17156
Head, G.O. (Lear Siegler, Inc., Instrument Division, Grand Rapids, MI).
A LOW-COST PROGRAM FOR EVALUATION OF ESD PROTECTIVE MATERIALS AND EQUIPMENT.

An excess of new electrostatic discharge protective material and equipment has been marketed over the past few years. Many vendors have produced similar products. These materials and equipment range in quality from very useful to potentially damaging. Materials and equipment seemingly very similar may differ in the actual ESD protection they offer. Surface resistance is probably the single most important characteristic in ESD protective material. A few easy, low-cost tests, explained in this paper, can help determine these products' ESD protection capabilities. This paper also includes methods used to identify serious problems in widely used blowers and high voltage relays.
AN ANALYSIS OF ANTISTATIC CUSHIONING MATERIALS.


A large number of antistatic cushion wrap materials are available on the market today. Each of the manufacturers of the products made claims as to their cushioning and electrostatic discharge protection capabilities. At present there are seven manufacturers of antistatic cushion wrap material. Six samples of each material were collected at random by Hewlett-Packard Data Terminals Division. Tests were performed in accordance with existing federal or industrial standards. Significant differences in ESD and cushioning characteristics were found among the products tested.

CHO-TRAP, A NOVEL VOLTAGE TRANSIENT PROTECTION PACKAGING MATERIAL.


Cho-Trap is a trade name for a new transient protection composite material with non-linear current voltage characteristics. The material acts like an insulator at circuit voltages and becomes a conductor when the voltage increases. These properties can be utilized to provide protection against transient electrical overstress. Cho-Trap can be custom-formulated as an elastomer for optimum packaging and protection.

EVALUATION OF INTEGRATED CIRCUIT SHIPPING TUBES.


It has been reported that device failure can occur from the discharge of triboelectrically charged IC pins. Since most devices are shipped in tubes, an obvious place to look for the generation of charge on a device is during the transport, loading or unloading of devices. This paper presents data on the triboelectric charging characteristics of devices resulting from sliding and vibrating in tubes made from metal and various plastic materials. The data show the variation of charge generated on plastic and hermetic packages with various lead frames, epoxy and silicon.
This paper examines the increased susceptibility of MOS VLSI circuits to electrical overstress/electrostatic discharge (EOS/ESD) conditions due to scaling of feature sizes such as metal widths, junction depths and gate oxide thickness of Ibm technology. Failure modes such as thermal overstress, metallization failure, electromigration, silicon resistor failure, gate oxide breakdown, latch-up and packaging-related failure modes are described.

This paper summarizes a study that was initiated to improve the on-chip protection of high density NMOS devices. The capability of approximately 100 different input protection schemes were examined. This was done by producing a test vehicle in a high density NMOS process. The input protection networks studied are combinations of seven basic structures. The ability of each structure to successfully protect the internal circuitry is presented. Guidelines for design and layout of future protection circuits are also presented.

This paper attempts to demonstrate how the application of established theoretical principles to the conceptual design and layout of input protection systems can provide such an increase in effectiveness in a manner compatible with high-volume, high-density processing techniques.

Many silicon planar transistors are scrapped after lot processing or reliability testing due to HFE degradation caused by excessive reverse current applied to the emitter-base junction. The objective of this paper is to identify specific symptoms that are unique to these types of degraded devices and which will enable the failure analyst to isolate the cause of failure.

During failure analysis activities, a large number of ICs were detected which definitely failed due to electrostatic overstress (EOS). In order to quantify the risk of ESD susceptibility of modern ICs, a step-stress test procedure was developed. The results of ESD step-stress tests clearly indicate that the susceptibility of all presently available integrated circuits to electrostatic damage during handling, transport and production is critical. From a user's point of view, the specification of min values according to a standardized ESD test method for ICs is urgently needed to quantify the risk and to make evaluation results comparable.
output, and power supply terminals. Failure was induced by increasing the amplitude of the overstress pulse until observable damage occurred. The device under test was examined for changes in terminal electrical parameters and functional operation after each pulse. The results of the failure threshold investigation are reported as average failure power as a function of pulse width.

17168


The purpose of this paper is to provide a comprehensive review of the effects of various types of EOS on semiconductor devices and to foster an awareness of the similarities between these effects. The information is based on a thorough evaluation of past and ongoing programs in the ESD and EMP communities and provides a comprehensive review of the technical tools and data that are currently available.

17169


A computer code has been written which describes in two dimensions the transient thermal behavior of silicon junctions as the result of excessive power dissipation. The code essentially merges a transient thermal analysis program with an instantaneous power dissipation program. This code must be verified experimentally, and this has not yet been done. The results obtained are consistent both in function and magnitude with existing EOS and EMP data, and no violations of EOS have been suggested by the code.

17170


Rectangular pulse testing can be used to predict semiconductor device failure under sinusoidal stress by defining equivalent rec-
tangular pulses. Four different pulse equivalence criteria are analyzed to determine the bounds on frequency conversion factors. This data can be used to estimate error bounds on the failure power resulting from waveform effects. The analysis suggests that waveform effects are not a major source of uncertainty in EMP vulnerability assessments.

17171


As printed wiring boards with two or more conductor lines between IC pads become increasingly common, fabricators are faced with the need for greater environmental control. Clean rooms have been the solution in semiconductor processing, and many printed wiring board producers have gone the same route. This paper discusses the necessity of clean rooms for printing wiring boards, the required levels of cleanliness, at what cost the levels are achieved, the temperature and humidity controls, and the existing alternatives.

17172


A composite failure threshold probability distribution has been developed to predict emitter-base electrical overstress junction failure of NPN transistors. This composite distribution provides a better probabilistic representation than the lognormal and Weibull distributions that are currently employed in survivability/vulnerability analyses of electronic circuits subjected to electrical overstress. The Component Statistical Characterization (CSC) data base was used in this analysis. In the CSC program, the lognormal was the most rejected of the five distributions tested for prediction of emitter-base transistor failure. The Weibull distribution is an excellent predictor for emitter-base nominal device failure. However, it is inadequate for predicting "maverick" devices and devices which are weaker than nominal.

17173

EOS/ESD FAILURE THRESHOLD ANALYSIS ERRORS, THEIR SOURCE, SIZE, AND CONTROL

Circuit EOS/ESD failure thresholds define the minimum overstress level required to damage a semiconductor. The thresholds are calculated using conventional circuit analysis and semiconductor device damage models, which are synthesized from experimental data, and are based on the principles of semiconductor device physics. This paper examines the accuracy of calculated failure thresholds, identifies the source and magnitude of analysis errors, and suggests techniques for improving analysis accuracy.

Wunsch, D.C. (The BDM Corp.).
AN OVERVIEW OF EOS EFFECTS ON PASSIVE COMPONENTS.

A great deal of electrical overstress testing and analysis on semiconductor devices has been performed and is presented in this paper. Passive components are generally not as vulnerable to EOS as semiconductor components and, therefore, are not usually the primary component of concern for EOS circuit failure. The emphasis on semiconductor devices has been because of the very low energy or voltage necessary to cause failure for many device types. However, there are a number of cases in which passive components are the limiting element in failures from EOS.

PULSE POWER RESPONSE AND DAMAGE CHARACTERISTICS OF CAPACITORS.

This paper presents the results of extensive experimental and theoretical investigations performed to develop quantitative response and damage models for a wide range of capacitor types under pulse electrical overstress environments. These models, with statistical variations and comparisons to manufacturers' ratings, were developed for electrostatic and electrolytic capacitors. When capacitors are subjected to high-level electrical pulse stress, their vulnerability is determined by the pulse response and damage characteristics which are peculiar to the materials and construction details of each particular capacitor type.

BEHAVIOR OF THICK-FILM POWER RESISTORS SUBJECTED TO LARGE MOMENTARY OVERLOADS.

This paper describes work done on the design of thick-film power resistors intended for battery-feed service in telephone exchanges and for other applications involving large momentary overloads. REA requirements governing resistance to momentary overloads must be compiled within the design of these resistors. Two major catastrophic failure modes were identified early in the work and are traced to voltage break and power density. Attention was focused on the problem of designing resistors which would spread the heat out sufficiently to minimize hot spots and the associated thermal gradients, since voltage breakdown effects are easy to control.

EOS THRESHOLD DETERMINATION OF ELECTROEXPLOSIVE DEVICES.

The threshold determination was performed to provide data in the assessment of the Minuteman Missile for Electromagnetic Pulse (EMP) studies. Four basic devices and two subassemblies were subjected to square wave and damped sine waves. Though multiple pulsing was not to be of primary interest, significant changes in breakdown characteristics were observed from the stress.

270
A procedure has been developed to determine probabilistically whether a semiconductor device failure has been caused by prescribed or anomalous EOS/ESD testing. An example is provided where a device that has received catastrophic damage during testing is analyzed by microscopic examination and detailed modeling techniques.

Honeywell experienced an inadvertent firing of an explosive primer at their Honeywell Ordnance Proving Ground (HOPG) Facility. Experimental testing was conducted to determine whether a semi-conductor device failure has been caused by EOS/ESD testing. An example is provided where a device that has received catastrophic damage during testing is analyzed by microscopic examination and detailed modeling techniques.

Electro-statically damaged operational amplifiers exhibit abnormalities and time-dependent shifts in common mode rejection.

A model has been developed to predict the electrical overstress threshold failure current in silicon solar cells as a function of pulse width. The essential features of the model are that initial failure will occur in the silicon junction under the longest finger near where the finger intersects the bus. This failure is due to heat generated in the finger being conducted into the silicon, thereby raising the silicon temperature to the instability point where the silicon resistance starts decreasing with temperature.
A study of ESD damage to 16k EPROMs manufactured both in the United States and Japan has been made. EPROMs have been evaluated using two models for ESD with both positive and negative discharges. The two models for ESD were the "Human Body Model" and the "Charged Device Model." It has been shown that EPROMS show a characteristic signature at the input protection network for either discharge model. Some EPROMS were found to be more susceptible to damage or failure from the charged device model testing than from the human body model testing. Results of experiments on some EPROMS show the three-state input/output data lines to be particularly sensitive to ESDs.

17185


It is well known that the Wunsch-Bell semiconductor junction thermal failure description is based on a constant thermal conductivity-heat conduction model. It is equally well known that the semiconductor material thermal conductivity is a strong function of the material temperature and so is not constant. This tends to cause some apprehension with regard to the range of validity of the Wunsch-Bell model. There have been a number of studies made of damage and thermal failure mechanisms in semiconductors due to coupled electromagnetic pulses (EMP) which produce heat within the semiconductor material. This work addresses the thermal failure of the semiconductor junction due to the ultrapid generation of heat caused by the deposition of incident pulse energy.

17186


This paper outlines a study conducted over a one-year period of electrostatic discharge (ESD) in the manufacturing environment. All data presented was generated from assembly line production. ESD problems are divided into three main categories for analysis: internal humidity control, assembly techniques, and operator awareness. All work done in humidity control was based on obtaining a minimum of 50% relative humidity plant-wide. The data presented on assembly techniques includes an analysis of ESD control in the use of machinery, work surfaces, storage containers and operator grouping. An ESD program is presented to achieve active participation from assembly line personnel.

17279


The antistatic liquid Staticide is tested to determine its effects on the quality of printed circuit boards. Solderability, corrosion rates, and printed circuit damage were checked.

17280


Understanding and being able to measure the operating junction temperature of semiconductor devices is crucial to building reliable systems. This paper describes a method for electrical thermal testing of GaAs FET junctions.

17281


This article gives various ESD problems encountered by companies and how these problems were solved. Special attention is given to rugs and carpeting as being static generators.

17285


This article is a summary of the third EOS/ESD Symposium held September 21-24 at Las Vegas' Aladdin Hotel. Thirty-five papers were presented and thirty-three exhibitors displayed their products and explained their services. Professor A.D. Moore made the luncheon speech on Henry A. Rowland, the forgotten
SECTION 9
STANDARDS
Handbooks, Specifications and Standards Specifying Test Methods and Controls for Protection of Electrical and Electronic Parts, Assemblies and Equipment Against Electrostatic Discharge:

U.S. GOVERNMENT DOCUMENTS

<table>
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<tr>
<td>DOD-HDBK-263</td>
<td>Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment Requirement for the Electrostatic Discharge Protection of Electronic Components and Assemblies</td>
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<tr>
<td>DOD-STD-1686</td>
<td>Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment</td>
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<td>NAVORD OD 46363</td>
<td>Requirements for the Electrostatic Discharge Protection of Electronic Components and Assemblies (completely contained in DOD-HDBK-263 and DOD-STD-1686)</td>
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<td>Packing Procedures for Submarine Repair Parts</td>
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<td>Test Methods and Procedures for Microelectronics; Test Method 3015 Electrostatic Discharge Sensitivity</td>
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<td>MIL-M-38510</td>
<td>Microcircuits, General Specification for</td>
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<td>MIL-M-55565A</td>
<td>Microcircuits, Packaging of</td>
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<td>MIL-B-81705B</td>
<td>Barrier Materials, Flexible, Electrostatic-Free, Heat Sealable</td>
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<tr>
<td>MIL-P-81997A</td>
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U.S. GOVERNMENT DOCUMENTS (Cont'd)

PPP-C-1842
Cushioning Material, Plastic, Open Cell (For Packaging Application)

NAVSUP/SPEC STD Form 36, Contract Requirement G-64
Packaging Instructions for Electromagnetic and Electrostatic Protection

FOREIGN GOVERNMENT DOCUMENTS

Defense STD-59-98 (U.K.)
Handling Procedures for Static Sensitive Devices

INDUSTRY DOCUMENTS

AATCC
134-1975
Test Method for the Electrostatic Propensity of Carpets

ANSI
47 (Secretariat) 707-Draft
Test Method for Electronic Devices Sensitive to Electrostatic Discharge

Z41.3
Conductive Safety-Toe Footwear: Section 5, Conductivity

ASTM
D257-78
D-C Resistance of Conductive or Insulating Materials

D991-75
Test Method for Rubber Property-Volume Resistivity of Electrically Conductive and Antistatic Material

D2679-78
Test Method for Electrostatic Charge

D3509-76
Test Method for Electrostatic Field Strength Due to Surface Charges

EIA (JEDEC)
RS-471
Attention Symbol and Label for Electrostatic Devices

NAS
NAS-853
Field Force, Protection for
INDUSTRY DOCUMENTS (Cont'd)

NFPA

No. 56A  Inhalation Anesthetics: Section 46  Reduction in Electrostatic Hazard

No. 77  Static Electricity

UL

217  Single and Multiple Station Smoke Detectors: Section 36 Static Discharge Test

U.S. GOVERNMENT DOCUMENTS

Specification Sales (3FRSBS)
Bldg. 107, Washington Navy Yard
General Services Administration
Washington, DC 20407

FED-STD-101B
PPP-C-1842

Commanding Officer
Naval Publications and Form Center
5801 Tabor Avenue
Philadelphia, PA 19120

DOD-HDBK-263  MIL-B-117
NAVORD OD-46363  MIL-S-19491
DOD-STD-1686  MIL-M-55565A
MIL-STD-129H  MIL-B-81705B
MIL-STD-758B  MIL-P-81997A
MIL-STD-883B  NAVSUP/SPEC STD Form 36
MS-90363G  Contract Requirement G-64

DOD-HDBK-263: Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment

This handbook provides guidelines for the establishment of an Electrostatic Discharge (ESD) Control Program in accordance with DOD-STD-1686. This document is applicable to the protection of electrical and electronic parts from damage due to ESD.

DOD-STD-1686: Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment

This standard provides direction for the establishment and implementation of an Electrostatic Discharge (ESD) Control Program for any activity that designs, tests, inspects, services, manufactures, processes, assembles, installs, packages, labels, stores or stows or otherwise handles electrical or electronic parts susceptible to damage caused by static electricity.
NAVORD OD 46363: Requirements for the Electrostatic Discharge Protection of Electronic Components and Assemblies

This ordinance document covers the general and detail requirements for the electrostatic discharge protection of electronic components and assemblies. This document has been incorporated in its entirety into DOD-HDBK-263 and DOD-STD-1686.


The test method in this standard describes the procedures to use for testing the electrostatic properties of various materials.

MIL-STD-129H: Marking for Shipment and Storage

Paragraph 5.4.38 of this standard specifies the marking requirements of unit, intermediate and exterior packs of sensitive electronic (ESDS) items.

MIL-STD-758B: Packing Procedures for Submarine Repair Parts

Appendix C of this standard covers protection for sensitive electronic items such as, but not limited to, diodes, transistors, integrated circuits, and equipments incorporating such items which are susceptible to damage from electrostatic, electromagnetic, or both field forces.


This test method establishes the means for determining the electrostatic discharge sensitivity classification for all microcircuits, and is used to determine the handling, marking, and packaging for shipment requirements for each device type.

MS-90363G: Box, Fiberboard, with Cushioning for Special, Minimum Cube Storage and Limited Reuse Applications

Dash Nos. 6, 7, and 8 of this standard specify the packaging and marking requirements of electrostatic sensitive devices.

MIL-B-117: Bags, Sleeves and Tubing, Interior Packing

This specification covers bags, sleeves and tubing, and interior packing for the preservation-packaging, field force protection (shielding), packing and container marking of electrical and electronic devices.
MIL-S-19491: Semiconductor Devices, Packaging of

This specification covers the requirements for the preservation-packaging, field force protection (shielding), packing and container marking of all types of discrete semiconductor devices (such as diodes and transistors).

MIL-M-38510: Microcircuits, General Specification For

This specification (revision E) requires all those devices covered by the specification to be tested for ESD sensitivity during initial qualification and any subsequent product redesign in accordance with MIL-STD-883 Method 3015.1 or the applicable detail (slash sheet) specification. Those devices determined to be sensitive to ESD (category A 2000 volts or less) or untested devices shall be marked accordingly either a) with the MIL-STD-129 symbol, b) an equilateral triangle, or c) utilizing a bright orange marking ink.

Slash sheets covered under this specification contain VZAP requirements for CMOS and MOS integrated circuits.

MIL-M-55565A: Microcircuits, Packaging Of

This specification covers the requirements for the preservation-packaging, field force protection (shielding), packing and container marking of all types of microcircuits.

MIL-B-81705B: Barrier Materials, Flexible, Electrostatic-Free, Heat Sealable

This specification covers opaque and transparent heat sealable, electrostatic-free, flexible, barrier materials for the packaging of missiles, explosive powered and electro-sensitive devices, microcircuits, semiconductors and thin film resistors.

MIL-P-81997A: Pouches, Cushioned, Flexible, Electrostatic-Free, Reclosable, Transparent

This specification covers the requirements for flexible electrostatic-free reclosable transparent pouches designed for shielding, packaging and storage of static-sensitive electronic devices.

PPP-C-1842: Cushioning Material, Plastic, Open Cell (For Packaging Applications)

This specification covers the requirements for Plastic Open Cell Cushioning Material designed for shielding, packaging and storage of static-sensitive devices.

NAVSUP/SPCC Form 36, Contract Requirement G-64: Packaging Instructions For Electromagnetic and Electrostatic Protection

This contract clause specifies the packaging instructions for the protection of field forces sensitive items.
Defense Standard 59-98; Handling Procedures for Static Sensitive Devices

This standard provides guidance relating to the handling, identification and packaging of static sensitive devices.

BS5783: 1979; Code of Practice for Handling of Electrostatic Sensitive Devices

This code of practice recommends the precautions for the storage, transportation, handling and testing of all kinds of electrostatic sensitive devices (ESDS), circuits, and assemblies.
AATCC Test Method 134-1975: Electrostatic Propensity of Carpets

This test method is designed to assess the static propensity of carpets by controlled laboratory simulation of conditions which may be met in practice, and more particularly, with respect to those conditions which are known from experience to be strongly contributory to excessive accumulation of static charges.

ANSI Test Method 47 (Secretariat) 707 (Proposed): Electronic Devices Sensitive to Electrostatic Discharges

This test method is designed to determine which electronic devices are sensitive to electrostatic discharge to the degree that they require special handling precautions.

ANSI Standard 241.3-1976; Conductive Safety-Toe Footwear

This standard provides the requirements for the design of conductive safety-toe footwear which protect against the hazards of the buildup of static electricity.

ASTM Test Method D257-78: D-C Resistance or Conductance of Insulating Materials

This test method covers direct-current procedures for the determination of d-c insulation resistance, volume resistance, volume resistivity, surface resistance and surface resistivity of electrical insulating materials or the corresponding conductances or conductivities.

ASTM Test Method D991-75: Rubber Property-Volume Resistivity of Electrically Conductive and Antistatic Products

This test method covers the determination of volume resistivity of rubbers used in electrically conductive and antistatic products.

ASTM Test Method D2679-78: Electrostatic Charge

This test method covers the determination of the amount of electrostatic charge present on or in a specimen or of the electrostatic charge transferred between two material objects upon contact.
ASTM Test Method D3509-76: Electrostatic Strength Due to Surface Charges

This test method covers the determination of the value of electrical field strength at and near a variety of objects such as metal surfaces at high voltages and insulating bodies with electrostatic charge.

Electronic Industries Association
2001 Eye Street
N.W. Washington, DC 20006

EIA Standard RS-471: Attention Symbol and Label for Electrostatic Sensitive Devices

This standard provides a distinctive caution symbol and label to be used to identify those electronic devices that require special handling to prevent damage due to electrostatic discharge.

National Standards Association
1321 Fourteenth Street N.W.
Washington, DC 20005

NAS 853: Field Force, Protection For

This standard provides for the protection of items, components and assemblies which may be damaged by field forces (electrostatic, electromagnetic, magnetic or radioactive) encountered in nonoperating environment.

National Fire Protection Association
470 Atlantic Ave
Boston, MA 02210

NFPA Standard 56A: Inhalation Anesthetics; Section 46: Reduction in Electrostatic Hazard

Section 46 of this standard provides the requirements to reduce the possibility of electrostatic spark discharges, with consequent ignition of flammable gases in anesthetizing locations.

NFPA Standard 77: Static Electricity

This standard provides recommended practices that assist in reducing the fire hazard of static electricity by presenting a discussion of the nature and origin of static charges, the general methods of mitigation and recommendations in certain specific operations for its dissipation.

Underwriter's Laboratory
383 Pfingsten Road
Northbrook, IL 60062

UL Code 217: Single and Multiple Station Smoke Detectors; Section 36: Static Discharge Test

Section 36 of this code provides a test to determine if smoke detector units are sensitive to electrostatic discharges.
APPENDIX

ADDITIONAL RAC SERVICES
ADDITIONAL RAC SERVICES

Search Services

Retrospective Searches are conducted at a flat fee of $125 per search. If no references are identified, a $50 service charge will be made in lieu of the above. For best results, please call or write for assistance in formulating your search question. An extra charge, based on engineering time and costs, will be made for evaluating, extracting or summarizing information from the cited references.

Consulting Services

Consulting Service fees are determined by the costs incurred in the conduct of the designed work, including staff time and overhead, materials and other expenses. Work will be initiated upon receipt of a signed purchase order. We will be pleased to prepare firm cost proposals.

Full Service Participating Plans

Two plans are offered to both government and industry

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Services provided to a Participant in either plan are:

- Automatic receipt of one (1) copy of each RAC microcircuit and semiconductor device databook issued over twelve months at a savings of $70.
- Availability of additional copies of each of the above databooks at 20% off list price.
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In addition, the Participating Member may access RAC resources as needed without issuing purchase orders. Up to 50 man-hours of professional consultation are authorized.

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The Blanket Purchase Order option enables you to write a single Purchase Order for a stipulated maximum dollar amount (depending on your needs) and active time duration (a one-year period is suggested), but you pay only for services rendered or documents purchased.

Military Agencies: Blanket Purchase Agreement, DD Form 1155, may be useful for ordering RAC reports and/or services. Please stipulate maximum dollar amount authorized and cutoff date on your order. Also specify services (e.g., publications, search services, etc.) to be provided. Identify vendor as IIT Research Institute (Reliability Analysis Center).

Ordering Information

Place orders or obtain additional information directly from the Reliability Analysis Center. Clearly specify the publications and services desired. Except for blanket purchase orders, prepayment is required. All foreign orders must be accompanied by a check drawn on a U.S. bank. Please make checks payable to IITRI/RAC.
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<th>Component Reliability Databooks</th>
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