NONLINEAR SYSTEM IDENTIFICATION STUDY
Implementation Feasibility Study

General Electric Company

Dr. E. J. Ewen

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**Nonlinear System Identification Study, Part I**

**Implementation Feasibility Study**

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**Abstract:**
The implementation feasibility of a nonlinear system identification technique is evaluated in this report. The identification technique uses a "black box" approach requiring measurements only at system input and output terminals and is applicable to weakly nonlinear systems whose behavior is adequately characterized by a finite Volterra series.

Three hardware implementations of the identification technique are postulated.
and their respective performances are evaluated. The impact of A/D converter quantization error, non-ideal amplifiers, multipliers and integrators on performance of the identification process is assessed. Performance requirements for each component of the three implementations are derived via simulation and analysis. The feasibility of implementing the technique using commercially available state of the art components and measurement equipment in each implementation is assessed.

RADC-TR-79-199, Part II, A computational complexity study of the identification technique processing to determine the class of nonlinear systems to which the technique can be practically applied will be published at a later date.
A. STUDY OBJECTIVES

The basic objective of this study effort is to evaluate the practical feasibility of a nonlinear system identification technique. The identification procedure studied is a black box technique where only input and output terminal measurements of the nonlinear system are used. The identification technique is applicable to a broad class of weakly nonlinear systems whose response can be characterized by a finite Volterra series. The identification procedure involves processing the input and output responses of a nonlinear system to obtain a set of linearly independent equations which uniquely define the parameters of a functional form of the second-order impulse response. Theoretically, the proposed identification technique represents a significant improvement over existing identification techniques because of its black box formulation. The intent of the study is to determine if this identification technique can be practically implemented and maintain an advantage over existing techniques.

The study effort is divided into two parts:

Part I An implementation feasibility study to determine practical methods of implementing the measurement scheme - both digital and analog - and to evaluate the requirements for the components of the measurement scheme.

Part II A computational complexity study of the identification technique processing to determine the class of nonlinear systems to which the technique can be practically applied.

This technical report summary covers the results of Part I of the study effort - the implementation feasibility study.

B. SUMMARY OF RESULTS AND CONCLUSIONS

Three basic implementations of the identification technique were evaluated and the requirements for the critical parameters of each element of the measurement scheme were evaluated. The
results of these performance evaluations and significant con-
clusions are summarized below for the three configurations.

1. Digital Implementation (Final Report Section III.B)

The digital implementation of the identification tech-
nique functions as follows. A signal generator excites the
nonlinear system with the appropriate signal. This input signal
and the resultant nonlinear system output are amplified and
converted into digital form via A/D converters. The resultant
samples are stored in memory for future nonreal-time identifica-
tion processing on a general purpose digital computer.

The performance evaluation of the digital implementa-
tion of the identification technique showed that the critical
components of the digital implementation are the A/D converter
and the pre-A/D converter amplifier. The signal generator and
data storage requirements are not technology limited in terms of
enabling implementation of the identification technique. The
important conclusions impacting parameter specification of these
devices are summarized below.

a. A/D Converter

(1) The A/D converter must have 14 to 16 bits of
resolution for adequate performance on a two-
pole system. This increases to 20 to 24 bits
as the number of poles increases to four.
Since the highest resolution commercially
available A/D converter has 16 bits of resolu-
tion at this point in time, any experimental
validation of this implementation should be re-
stricted to systems with two poles or less.

(2) The sampling rate requirements for the A/D
converter are driven by the accuracy re-
quirements of the processing technique. For a
two pole system, the sampling rate should be 4
to 10 times slower than the highest break
frequency of the system under test. Current
16-bit A/D converter technology implies that
the system under test be limited to an upper
break frequency of approximately 10 to 30 kHz.

b. Amplifier

(1) The pre-A/D converter amplifier is necessary
to adjust the output of the system under test
to the full-scale input voltage level of the
A/D converter.
(2) The bandwidth requirements of the amplifier are a function of the processing approach used for identification. In general, one approach requires an amplifier with a bandwidth 1000 times the bandwidth of the system under test while the other approach requires the amplifier bandwidth to be approximately equal to the bandwidth of the system under test.

The above conclusions support the subsequent conclusion that the digital implementation of the identification technique can feasibly be constructed and used in an experimental test setup under the various constraints presented above.

2. Hybrid Implementation (Final Report Section III.C)

A hybrid implementation of the identification technique was evaluated. This implementation differs from the digital implementation in that the input and output of the system under test are integrated a number of times using analog integrators prior to sampling via A/D converters. These samples are stored for future nonreal-time processing on a digital computer.

The analyses of the performance of this implementation led to the following conclusions:

(1) The resolution requirements for the hybrid implementation are significantly greater than for the digital implementation. The hybrid implementation requires 24 bits which is beyond the current state of the art in A/D converter technology. The conversion speed requirements are essentially the same as those required for the digital implementation.

(2) For systems with two poles or less, the hybrid implementation offers no advantages over the digital implementation. For systems with more than two poles, the hybrid implementation offers potential performance improvement over the digital approach for an A/D converter with 24 bits. This improvement however increases the measurement implementation complexity and cost.

It was concluded that it is not feasible to consider implementation of this approach for an experimental validation at this time because of the A/D converter requirements. However, future improvements in A/D converter technology may permit implementation of this approach at that time.
3. Analog Implementation (Final Report Section III.D)

An analog implementation of the identification technique was also evaluated.

The analog implementation derives the necessary processing (inner product) quantities using analog components. The inner product device outputs are sampled and stored for further nonreal-time processing on a digital computer.

The performance evaluation has shown that the critical components in the analog implementation are the inner product device and the A/D converter; this has led to the following conclusions.

(1) A minimum of 18 bits of A/D converter resolution is required to achieve minimum identification performance. Conversion speed is not important since only one sample per inner product device output is required.

(2) The maximum tolerable error in the inner product output is on the order of $10^{-3}$ percent to achieve a minimum level of identification performance for A/D converters with 18 or more bits of resolution.

(3) Performance improvement requires less inner product error ($10^{-4}$ to $10^{-6}$ percent) and increased A/D converter resolution (20 to 24 bits). However, the performance of the analog implementation is below that demonstrated for the digital implementation.

(4) Currently available analog multipliers have an output error on the order of 0.05 percent, which is approximately 50 times greater than the maximum tolerable error of 0.001 percent required for minimum performance of the identification technique.

The analog multiplier and the A/D converter requirements for the analog implementation imply that it is not feasible to consider this implementation for an experimental test setup in the present time frame. Significant technological developments for analog multipliers and A/D converters are necessary before this implementation can prove feasible.
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EVALUATION

The objective of this effort was to develop, quantify, and evaluate the practical constraints for the implementation of a time domain methodology for weakly nonlinear system identification. This time domain methodology permits the functional characterization (as opposed to numerical) of the second and third order Volterra kernels from input/output measurements (and subsequent analysis) on an otherwise, nonlinear black box with memory.

The process of system identification consists of postulating a valid analytical model for the system under consideration and performing tests on the system to completely specify or "identify" the parameters which describe the system analytical model. For example, a linear system is completely characterized by its impulse response, h(t). The system identification process for this linear system analytical model consists of any procedure that completely determines h(t). The present consideration in the area of nonlinear system identification is the derivation of a valid analytical model for the nonlinear system under consideration.

The identification procedure successfully studied is a black box technique where only input and output terminal measurements of the nonlinear system are used. The identification technique is applicable to a broad class of weakly nonlinear systems whose response can be characterized by a finite Volterra series. The identification procedure involves processing the input and output responses of a nonlinear system to obtain a set of linearly independent equations which uniquely define the parameters of a functional form of the second-order impulse response. Theoretically, the proposed identification technique represents a significant improvement over existing identification techniques because of its black box formulation. The intent of the study was to determine where this identification technique
can be practically implemented and maintain an advantage over existing techniques. To these ends, the practical implementation constraints have been developed, quantified and assessed for these candidate measurement configurations. The robustness of the technique to nonlinear circuits with many and/or repeated poles is the subject of Part II of this final report.

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SECTION I
INTRODUCTION

A. STUDY OBJECTIVES

The basic objective of this study effort is to evaluate the practical feasibility of a nonlinear system identification technique. The identification procedure studied is a black box technique where only input and output terminal measurements of the nonlinear system are used. The identification technique is applicable to a broad class of weakly nonlinear systems whose response can be characterized by a finite Volterra series. The identification procedure involves processing the input and output responses of a nonlinear system to obtain a set of linearly independent equations which uniquely define the parameters of a functional form of the second-order impulse response. Theoretically, the proposed identification technique represents a significant improvement over existing identification techniques because of its black box formulation. The intent of the study to determine if this identification technique can be practically implemented and maintain an advantage over existing techniques.

The study effort is divided into two parts:

Part I An implementation feasibility study to determine practical methods of implementing the measurement scheme - both digital and analog - and to evaluate the requirements for the components of the measurement scheme.

Part II A computational complexity study of the identification technique processing to determine the class of nonlinear systems to which the technique can be practically applied.

This final report represents the results of Part I of the study effort - the implementation feasibility study. The computational complexity study results will be presented in Part II of this final report.

B. SUMMARY OF RESULTS AND CONCLUSIONS

Three basic implementations of the identification technique were evaluated and the requirements for the critical parameters of each element of the measurement scheme were evaluated. The
results of these performance evaluations and significant conclusions are summarized below for the three configurations.

1. Digital Implementation

The block diagram of the digital implementation of the identification technique is shown in Figure 1. A signal generator excites the nonlinear system with the appropriate sum of decaying exponential functions. This input and the resultant nonlinear system output are amplified and converted into digital form via A/D converters. The resultant samples are stored in memory for future nonreal-time processing on a general-purpose digital computer.

The performance evaluation of the digital implementation of the identification technique showed that the critical components of the digital implementation are the A/D converter and the pre-A/D converter amplifier. The important conclusions impacting parameter specification of these devices are summarized below.

a. A/D Converter

(1) The A/D converter must have 14 to 16 bits of resolution for adequate performance with a two-pole system. This increases to 20 to 24 bits as the number of poles increases to four. Since the highest resolution commercially available A/D converter has 16 bits of resolution at this point in time, any experimental validation of this implementation should be restricted to systems with two poles or less.

(2) The sampling rate requirements for the A/D converter are driven by the accuracy requirements of the processing technique. For a two pole system, the sampling rate should be 4 to 10 times slower than the highest break frequency of the system under test. The fastest 16-bit A/D converter currently available is limited to a sampling rate of 125 kHz. This implies that the system under test be limited to an upper break frequency of approximately 10 to 30 kHz.

b. Amplifier

(1) The pre-A/D converter amplifier is necessary to adjust the output of the system under test to the full-scale input voltage level of the A/D converter.
Figure 1. Digital Implementation of Identification Technique
(2) The bandwidth requirements of the amplifier are a function of the processing approach used for identification. In general, one approach requires an amplifier with a bandwidth 1000 times the bandwidth of the system under test while the other approach requires the amplifier bandwidth to be approximately equal to the bandwidth of the system under test.

(3) Operational amplifiers with gain-bandwidth products of up to 1000 MHz are presently commercially available. These are compatible with either processing approach described in (2) above.

c. Remaining Components

The remaining components of the digital implementation are not technology limited in terms of enabling implementation of the identification technique. The important conclusions are given below:

(1) No commercially available waveform generator has an exponential function capability. The appropriate inputs will be generated by using operational amplifiers as low-pass filters and appropriately clamping the short pulse response to obtain the exponential function.

(2) Data storage will be accomplished using static random access memory (RAM) chips and a programmable interface to transmit the data to the digital computer for nonreal-time processing.

The above conclusions support the subsequent conclusion that the digital implementation of the identification technique can feasibly be constructed and used in an experimental test setup under the various constraints presented above.

2. Hybrid Implementation

A hybrid implementation of the identification technique is shown in Figure 2 for a test system with two poles.

This implementation differs from the digital implementation in that the input and output of the system under test are integrated twice using analog integrators prior to sampling via A/D converters. These samples are stored for future nonreal-time processing on a digital computer.
Figure 2. Hybrid Implementation
The analyses of the performance of this implementation led to the following conclusions:

(1) The resolution requirements for the hybrid implementation are significantly greater than for the digital implementation. The hybrid implementation requires 24 bits which is beyond the current state of the art in A/D converter technology. The conversion speed requirements are essentially the same as those required for the digital implementation.

(2) For systems with two poles or less, the hybrid implementation offers no advantages over the digital implementation. For systems with more than two poles, the hybrid implementation offers potential performance improvement over the digital approach for an A/D converter with 24 bits. This improvement however increases the measurement implementation complexity and cost.

(3) The amplifier and signal generator requirements are the same as those derived for the digital implementation.

(4) The amount of data to be stored is \([N + (1/2)]\) times greater for the hybrid implementation than for the digital implementation (N is the number of poles in the linear portion of the system under test).

It is not feasible to consider implementation of this approach for an experimental validation at this time because of the A/D converter requirements.

However, future improvements in A/D converter technology may permit implementation of this approach at that time.

3. Analog Implementation

An analog implementation of the identification technique is shown in Figure 3.

The analog implementation derives the necessary inner product quantities using analog components. The inner product device outputs are sampled and stored for further nonreal-time processing on a digital computer.

The performance evaluation has shown that the critical components in the analog implementation are the inner product.
Figure 3. Analog Implementation
device and the A/D converter; this has led to the following conclusions.

(1) A minimum of 18 bits of A/D converter resolution is required to achieve minimum identification performance. Conversion speed is not important since only one sample per inner product device output is required.

(2) The maximum tolerable error in the inner product output is on the order of $10^{-3}$ percent to achieve a minimum level of identification performance for A/D converters with 18 or more bits of resolution.

(3) Performance improvement requires less inner product error ($10^{-4}$ to $10^{-6}$ percent) and increased A/D converter resolution (20 to 24 bits). However, the performance of the analog implementation is below that demonstrated for the digital implementation.

(4) Currently available analog multipliers have an output error on the order of 0.05 percent, which is approximately 50 times greater than the maximum tolerable error of 0.001 percent required for minimum performance of the identification technique.

(5) Amplifier and signal generator requirements are essentially the same as those derived for the digital implementation.

(6) Data storage requirements are significantly reduced for the analog implementation. Only $(4N + 1)$ data words need to be stored ($N$ is the number of poles in linear portions of systems under test).

The analog multiplier and the A/D converter requirements for the analog implementation imply that it is not feasible to consider this implementation for an experimental test setup in the present time frame. Significant technological developments for analog multipliers and A/D converters are necessary before this implementation can prove feasible.
SECTION II
IDENTIFICATION TECHNIQUE

A. IDENTIFICATION TECHNIQUE DEVELOPMENT

1. Background

The basic objective of this study (Part I) is to investigate the implementation feasibility of an identification technique for nonlinear systems. The identification technique is described in detail in this section and is based on the analysis presented in Reference 1. This technique is a "black box" procedure in that only measurements at the system input and output terminals are required. The feasibility of implementing a test setup to make the required data measurements of the input and output is the primary focus of this study (Part I). The identification technique is applicable to a class of weakly nonlinear systems whose behavior is adequately characterized in terms of a finite Volterra functional series given by

\[ y(t) = \sum_{n=1}^{\bar{N}} y_n(t) = \sum_{n=1}^{\bar{N}} \int h_n(\tau_1, ..., \tau_n) \prod_{p=1}^{n} x(t - \tau_p) d\tau_p, \quad (1) \]

where

- \( y_n(t) \) is the n-th order portion of the response
- \( \int \) denotes an n-fold integration from \(-\infty\) to \(\infty\)
- \( \prod \) denotes an n-fold product
- \( \bar{N} \) is the finite sum

The n-th-order Volterra kernel \( h_n(\tau_1, ..., \tau_n) \) can be referred to as the nth-order nonlinear impulse response (Reference 2). In actuality, the nonlinear impulse responses may not be identically zero above order \( \bar{N} \). However, the finite sum of
equation (1) implies that higher-order terms contribute negligibly to the output.

As is the case with linear systems, there is a corresponding representation in the Laplace transform domain. The $n\text{th}$-order nonlinear transfer function, which is defined to be the $n$-dimensional Laplace transform of $h_n(t_1, \ldots, t_n)$, is given by

$$H_n(s_1, \ldots, s_n) = \int h_n(t_1, \ldots, t_n) \prod_{p=1}^{n} e^{-s_p t_p} dt_p. \quad (2)$$

Closely related to $y_n(t)$ is the multidimensional time function

$$y_n(t_1, \ldots, t_n) = \int h_n(t_1, \ldots, t_n) \prod_{p=1}^{n} x(t_p - \tau_p) d\tau_p. \quad (3)$$

It is observed that $y_n(t_1, \ldots, t_n) = y_n(t)$ when $t_1 = \ldots = t_n = t$. If the $n$-dimensional Laplace transform of $y_n(t_1, \ldots, t_n)$ is denoted by $Y_n(s_1, \ldots, s_n)$, it follows from equation (3) that

$$Y_n(s_1, \ldots, s_n) = H_n(s_1, \ldots, s_n) \prod_{p=1}^{n} X(s_p) \quad (4)$$

where $X(s)$ is the conventional one-dimensional Laplace transform of $x(t)$. $Y_n(s_1, \ldots, s_n)$ is reduced to $Y_n(s)$, the Laplace transform of $y_n(t)$, by applying the "association of variables" technique introduced by George (Reference 3). This approach implies that the nonlinear system is completely characterized by
the nonlinear impulse responses or, equivalently, the nonlinear transfer functions. Once either of these is known, the system response can be determined for arbitrary inputs. The problem of identifying a weakly nonlinear system therefore, consists of identifying the nonlinear impulse responses, by \( h_n (t_1, t_2, ..., t_n), n = 1, 2, ..., \bar{N}. \)

The identification technique developed in Reference 1 is designed to identify the parameters of closed-form expressions for the nonlinear impulse responses, \( h_n (t_1, t_2, ..., t_n), n = 1, 2, ..., \bar{N}. \) The analysis presented in Reference 1 demonstrates how the technique identifies the parameters of \( h_1(t), h_2(t_1, t_2) \) and \( h_3(t_1, t_2, t_3). \) On the basis of this analysis, it is believed that the technique is extendable to identification of higher order nonlinear impulse responses (\( \bar{N} \geq 4 \)). This study (Part I) is concerned with the feasibility of implementing the identification of only the linear and second-order nonlinear impulse responses, \( h_1(t) \) and \( h_2(t_1, t_2). \)

A functional form for \( h_2(t_1, t_2) \) for a broad class of nonlinear systems is presented below.

2. Functional Form for \( h_2(t_1, t_2) \)

In Volterra analysis, \( h_1(t) \) is the impulse response usually associated with the linear incremental model of a nonlinear system. When this model consists of linear resistors, capacitors, inductors, and controlled sources, the linear impulse response is described by

\[
h_1(t) = \begin{cases} 
\sum_{i=1}^{N} \Re \lambda_i e^{R_i t}, & t > 0 \\
0, & t < 0 
\end{cases}
\]

(5)

where \( \Re \{ \lambda_i \} \leq 0 \) and it is assumed that the \( \lambda_i \) are distinct.

In general, a weakly nonlinear system contains several nonlinearities. If the nonlinearities can be modeled by nonlinear resistors, capacitors, inductors, and controlled sources whose current-voltage relationships can be expanded into power series as shown in Table 1 and if \( h_1(t) \) is given by equation (5), the second-order nonlinear impulse response can be expressed in the symmetrical form (Reference 1):
TABLE 1.  CURRENT-VOLTAGE RELATIONSHIPS OF POSSIBLE NONLINEARITIES

1) Zero Memory, Independent Nonlinearity

\[ i = K(v) = \sum_{j=1}^{\infty} K_j v^j \]

2) Zero Memory, Dependent Nonlinearity

\[ i = G(u,v) = \sum_{j=0}^{\infty} \sum_{k=0}^{\infty} g_{jk} u^j v^k \]

3) Capacitive, Independent Nonlinearity

\[ i = \frac{d}{dt} Q(v) = \frac{d}{dt} \sum_{j=1}^{\infty} \gamma_j v^j \]

4) Inductive, Independent Nonlinearity

\[ i = \sum_{j=1}^{\infty} \psi_j \left[ \int_{-\infty}^{t} v(z) \, dz \right]^j \]

where

- \( v \) = incremental voltage across the element
- \( i \) = incremental current through the element
- \( u \) = incremental voltage elsewhere in the circuit.
\[ h_2(t_1,t_2) = \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} a_{k_1k_2} t_1^{a_{k_1} t_1} a_{k_2} t_2^{a_{k_2} t_2} U(t_2 - t_1) \]

\[ + \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} a_{k_1k_2} t_1^{a_{k_1} t_1} a_{k_2} t_2^{a_{k_2} t_2} U(t_1 - t_2) \]

where

\[ M = N^2 + 1. \]

\[ U(t) = \begin{cases} 
1 & , t > 0 \\
0 & , t < 0 
\end{cases} \]

and where the natural frequencies in equation (6) are related to those in equation (5) according to:

\[ a_1 = \lambda_1, a_2 = \lambda_2, \ldots, a_N = \lambda_N, \]
\[ a_{N+1} = \lambda_1 - \lambda_1 = 0, a_{N+2} = \lambda_1 - \lambda_2, \ldots, a_{2N} = \lambda_1 - \lambda_N \]
\[ a_{2N+1} = \lambda_2 - \lambda_1, a_{2N+2} = \lambda_2 - \lambda_3, \ldots, a_{3N-1} = \lambda_2 - \lambda_N \]
\[ a_{N^2-N+3} = \lambda_N - \lambda_1, a_{N^2-N+4} = \lambda_N - \lambda_2, \ldots, \]
\[ a_{N^2+1} = \lambda_N - \lambda_{N-1}. \]

The ordering of the \( a_{k_1} \) terms in equation (6) assumes all the factors \( \lambda_i - \lambda_j \) to be distinct, such that \( \lambda_i - \lambda_j \neq \lambda_k \) for any \( i,j,k = 1, \ldots, N \). Also, the zero entry that results from \( \lambda_i - \lambda_j \) when \( i = j \) is included only once as the entry \( a_{N+1} \). In addition, it is readily shown that (Reference 1)

\[ A_{k_1k_2} = A_{k_2k_1} \quad \text{for} \quad k_1, k_2 \leq N \]

and that the coefficients of terms in equation (8) having the form
\[(\lambda_i - \lambda_j)t_1 + \lambda_i t_2 \quad , \quad i \neq j\]

are identically zero.

The identification technique will identify the parameters of \(h_2(t_1, t_2)\) as represented in equation (6).

3. Identification Technique Description

The functional form for \(h_2(t_1, t_2)\) established in equation (6) implies that the identification of \(h_2(t_1, t_2)\) reduces to identification of the parameters \(a_{k1}, a_{k2}, A_{k1}k_2\) and \(N\). However, equations (5) and (9) show that \(a_{k1}, a_{k2}\) and \(N\) can be determined once the linear impulse response is known. Therefore, the task of identifying these parameters reduces to the task of identifying \(h_1(t)\). The problem of identifying the coefficients \(A_{k1}k_2\) still remains.

The identification process separates into two distinct steps: (1) identification of \(h_1(t)\); and (2) identification of the \(A_{k1}k_2\) quantities of \(h_2(t_1, t_2)\). These two steps are considered below.

a. Identification of the Linear Impulse Response, \(h_1(t)\)

The first step in the identification of \(h_1(t)\), the linear impulse response of a nonlinear system, is to excite the system with an input amplitude such that the output is linear. The amplitude of this signal can be determined by exciting the system with a sinusoidal signal of amplitude \(A\) and performing a spectral analysis of the resultant response. Amplitude \(A\) is then adjusted until the amplitude level of the harmonic frequencies of the output becomes sufficiently small compared to the level of the fundamental component. The following analysis assumes that the output of the nonlinear system represents the linear response of the systems described by

\[
h_1(t) = \begin{cases} 0, & t < 0 \\ \sum_{i=1}^{N} R_i e^{\lambda_i t}, & t > 0 \end{cases}
\]

\[(11)\]
where Re \( \{\lambda_i\} \) < 0 and the \( \lambda_i \) are distinct. The \( \lambda_i \) and \( R_i \) will be identified using the pencil-of-functions approach (Reference 4).

The pencil-of-functions approach operates on the system as shown in Figure 4, where the input to the linear system and resulting output are integrated \( N \) times over the real-time interval \( (0,T) \). The following notation is used in Figure 4.

\[
x_{i+1}(t) = \begin{cases} 
  \int_0^t x_i(\tau) \, d\tau & 0 \leq t \leq T \\
  0 & \text{elsewhere}
\end{cases} \quad i = 1, \ldots, N \\
\]

\[
\bar{y}_{i+1}(t) = \begin{cases} 
  \int_0^t \bar{y}_i(\tau) \, d\tau & 0 \leq t \leq T \\
  0 & \text{elsewhere}
\end{cases} \quad i = 1, \ldots, N \\
\]

\[
X_1(s) = \mathbb{L} \{ x_1(t) \} = \int_0^T x(t) \, e^{-st} \, dt \quad (14)
\]

\[
X_{i+1}(s) = \frac{X_i(s)}{s} \quad i = 1, \ldots, N \\
(15)
\]

\[
\bar{Y}_1(s) = \mathbb{L} \{ \bar{y}_1(t) \} = \int_0^T y(t) \, e^{-st} \, dt \quad (16)
\]

\[
\bar{Y}_{i+1}(s) = \frac{\bar{Y}_i(s)}{s} \quad i = 1, \ldots, N \\
(17)
\]
Figure 4. Identification Technique Configuration with N Integrators
It has been shown (Reference 4) that poles of the linear system satisfy the polynomial equation

\[ \sum_{i=0}^{N} \lambda^{N-1} \left( G_{2N+1} \begin{bmatrix} i+1, i+1 \end{bmatrix} \right)^{1/2} = 0 \]  

(18)

where \( G_{2N+1} \) is the Gram determinant shown in equation (19) below:

\[
G_{2N+1} = \begin{vmatrix}
\langle \bar{y}_1, \bar{y}_1 \rangle & \langle \bar{y}_1, \bar{y}_2 \rangle & \cdots & \langle \bar{y}_1, \bar{y}_{N+1} \rangle & \langle \bar{y}_1, x_2 \rangle & \cdots & \langle \bar{y}_1, x_{N+1} \rangle \\
\langle \bar{y}_2, \bar{y}_1 \rangle & \langle \bar{y}_2, \bar{y}_2 \rangle & \cdots & \langle \bar{y}_2, \bar{y}_{N+1} \rangle & \langle \bar{y}_2, x_2 \rangle & \cdots & \langle \bar{y}_2, x_{N+1} \rangle \\
\vdots & \vdots & \ddots & \vdots & \vdots & \cdots & \vdots \\
\langle \bar{y}_N, \bar{y}_1 \rangle & \langle \bar{y}_N, \bar{y}_2 \rangle & \cdots & \langle \bar{y}_N, \bar{y}_{N+1} \rangle & \langle \bar{y}_N, x_2 \rangle & \cdots & \langle \bar{y}_N, x_{N+1} \rangle \\
\langle x_2, \bar{y}_1 \rangle & \langle x_2, \bar{y}_2 \rangle & \cdots & \langle x_2, \bar{y}_{N+1} \rangle & \langle x_2, x_2 \rangle & \cdots & \langle x_2, x_{N+1} \rangle \\
\vdots & \vdots & \ddots & \vdots & \vdots & \cdots & \vdots \\
\langle x_{N+1}, \bar{y}_1 \rangle & \langle x_{N+1}, \bar{y}_2 \rangle & \cdots & \langle x_{N+1}, \bar{y}_{N+1} \rangle & \langle x_{N+1}, x_2 \rangle & \cdots & \langle x_{N+1}, x_{N+1} \rangle \\
\end{vmatrix}
\]

(19)

Further, the residues \( R_i \) of the poles \( \lambda_i \) satisfy the equation

\[ R = C^{-1} Y \]

(20)

where

\[
R = \text{residue matrix} = \begin{bmatrix} R_1 \\ R_2 \\ \vdots \\ R_N \end{bmatrix}
\]

(21)
\[ Y = \text{output matrix} = \begin{bmatrix}
\bar{y}_2(T) \\
\bar{y}_3(T) \\
\bar{y}_4(T) \\
\vdots \\
\bar{y}_{N+1}(T)
\end{bmatrix} \] (22)

\[ C = N \times N \text{ matrix whose } i,j\text{th element is defined by} \]

\[ C_{ij} = \frac{P_j(T)}{\lambda_j^i} - \sum_{m=1}^{i} \frac{x_{m+1}(T)}{(\lambda_j)^i+m} \] (23)

where

\[ P_j(T) = \int_0^T e^{\lambda_j(T-\tau)} x(\tau) \, d\tau \] (24)

Equations (18), (20), (23), and (24) show how \( R_i \) and \( \lambda_i \) are obtained once \( N \) is known. The pencil of functions technique also permits determination of \( N \), the number of poles of the linear system. This can be accomplished as follows:

Using the system shown in Figure 4:

1. Assume \( N = 1 \)
2. Measure \( \bar{y}_i(t), i=1,\ldots,N+1, \) and \( x_i(t), i=2,\ldots,N+1 \)
3. Form the Gram determinant \( G_{2N+1} \) as given by equation (19)
4. Check singularity of \( G_{2N+1} \)
(5) If $G_{2N+1}$ is nonsingular, increase $N$ by 1 and repeat from step (2)

(6) If $G_{2N+1}$ is singular, then the number of poles is $N - 1$

Therefore, the pencil-of-functions system identification technique completely specifies $h_1(t)$ as given in equation (11).

b. Identification of the Second Order Impulse Response, $h_2(t_1, t_2)$

The second step of the identification procedure is to identify the unknown parameters of $h_2(t_1, t_2)$. With $h_2(t_1, t_2)$ given by:

$$h_2(t_1, t_2) = \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} a_{k_1} t_1 + a_{k_2} t_2 e^{k_1 k_2} U(t_2 - t_1)$$

$$+ \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} a_{k_1} t_2 + a_{k_2} t_1 e^{k_1 k_2} U(t_1 - t_2)$$

the only unknown parameters are the $A_{k_1 k_2}$ quantities since $M, N, A_k$ and $A_k$ are known from identification of $h_1(t)$. A procedure for determining the $A_{k_1 k_2}$ using the pencil-of-functions method is described in this section.

The identification procedure utilizes the response of the weakly nonlinear system to a sum of $L$ decaying exponentials as described by:

$$x(t) = \begin{cases} 
L \sum_{i=1}^{L} e^{-a_i t} & , \quad t \geq 0 \\
0 & , \quad t < 0 
\end{cases}$$

where $\text{Re} \{a_i\} > 0$. The second-order portion of the response to $x(t)$ is given by the two-dimensional transform

$$Y_2(s_1, s_2) = H_2(s_1, s_2) X(s_1) X(s_2)$$

(27)
Taking the one-dimensional Laplace transform of \( x(t) \) and the two-dimensional Laplace transform of \( h_2(t_1, t_2) \) and substituting into equation (27) results in

\[
Y_2(s_1, s_2) = \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} \sum_{i=1}^{L} \sum_{j=1}^{L} A_{k_1 k_2}
\]

\[
\cdot \left( \frac{s_1 + s_2 - a_{k_2}}{(s_1 + s_2 - a_{k_1} - a_{k_2})(s_1 - a_{k_2})(s_2 - a_{k_2})} \right) \left( \frac{1}{s_1 + a_{i}} \right) \left( \frac{1}{s_2 + a_{j}} \right).
\]

(28)

Applying George's "association of variables" technique (Reference 3), \( Y_2(s) \) becomes

\[
Y_2(s) = \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} \sum_{i=1}^{L} \sum_{j=1}^{L} A_{k_1 k_2}
\]

\[
\cdot \left[ \frac{\alpha_i + \alpha_j + 2a_{k_1}}{(\alpha_j + a_{k_1})(\alpha_i + a_{k_1})(\alpha_i + a_j + a_{k_1} + a_{k_2})} \right] \left( \frac{1}{s - (a_{k_1} + a_{k_2})} \right)
\]

\[- \left( \frac{1}{(\alpha_j + a_{k_1})(\alpha_i + a_{k_1})} \right) \left( \frac{1}{s + (\alpha_j - a_{k_2})} \right) \]

\[- \left( \frac{1}{(\alpha_i + a_{k_1})(\alpha_j + a_{k_2})} \right) \left( \frac{1}{s + (\alpha_i - a_{k_2})} \right) \]

\[+ \left( \frac{\alpha_i + \alpha_j + 2a_{k_2}}{(\alpha_j + a_{k_2})(\alpha_i + a_{k_2})(\alpha_i + a_j + a_{k_1} + a_{k_2})} \right) \left( \frac{1}{s + a_{i} + a_{j}} \right) \]

(29)
where

$$\alpha_j \neq a_{k_1}$$ for \( j = 1, \ldots, L; k_1 = 1, \ldots, M $$

$$\alpha_1 + \alpha_j + a_{k_1} + a_{k_2} \neq 0 \text{ for } i, j = 1, \ldots, L; k_1 = 1, \ldots, M; k_1 = 1, \ldots, N $$

$$a_{k_1} \neq a_{k_2}$$ for \( k_2 = 1, \ldots, N; k_1 = N + 1, \ldots, M. $$

The expression in equation (29) is the Laplace transform of a sum of exponential time functions. This sum can be interpreted as the impulse response of an equivalent linear system as indicated in Figure 5. In other words, the second-order response \( y_2(t) \) can be visualized as though it were generated by an equivalent linear system. However, the equivalence is valid only if the equivalent linear system is considered to be excited by an impulse. It follows that the problem of identifying \( h_2(t_1, t_2) \) has been reduced to the simpler problem of identifying a linear system and the pencil-of-functions technique can be used again.

Figure 5. Equivalent Linear System with Transfer Function \( Y_2(s) \)
The system is excited by an input amplitude such that the output is described by linear and second-order terms, \(y_1(t)\) and \(y_2(t)\). The identification process will operate the signal \(y_2(t)\). For this purpose, the second-order portion of the response, \(y_2(t)\) is isolated from the total response. \(y_2(t)\) is obtained by subtracting from the total response the corresponding linear response \(y_1(t)\), which is known because \(h_1(t)\) has been identified. It is shown in Reference 1 that the second-order response \(y_2(t)\) need not be isolated from the total response for the identification procedure to work. (This will be investigated in detail in Part II of the study.) However, isolation of \(y_2(t)\) from the total response eases the mathematical presentation and will be assumed necessary at this point, to identify implementation constraints.

Once \(y_2(t)\) is isolated from the total response, the coefficients \(A_{k_1k_2}\) are then evaluated by applying the pencil-of-functions method to \(y_2(t)\), treating it as though it were the impulse response of a linear system. This latter step is now discussed in detail.

From equation (29), the poles of \(Y_2(s)\) are given by

\[
\begin{align*}
  s &= a_{k_1} + a_{k_2}, \quad k_1 = 1, \ldots, M; k_2 = 1, \ldots, N \\
  s &= -a_i + a_{k_2}, \quad i = 1, \ldots, L; k_2 = 1, \ldots, N \\
  s &= -a_i - a_j, \quad i, j = 1, \ldots, L.
\end{align*}
\]

(31)

First, consider poles of the form \(s = a_{k_1} + a_{k_2} = 2 \lambda_\ell \), \(\ell = 1, \ldots, N\). The terms in \(Y_2(s)\) corresponding to the pole at \(2 \lambda_\ell\) are given by

\[
Y_{2\ell \ell}(s) = \sum_{i=1}^{L} \sum_{j=1}^{L} A_{i \ell \ell} \frac{1}{(a_j + \lambda_\ell)(a_i + \lambda_\ell)} \frac{1}{s - 2 \lambda_\ell}.
\]

(32)
If the residue of the pole at \(2\lambda_k\), as evaluated using the pencil-of-functions method, is \(\beta_{k\ell}\), it follows that

\[
A_{k\ell} = \beta_{k\ell} \sum_{i=1}^{L} \sum_{j=1}^{L} \frac{1}{(\alpha_j + \lambda_k)(\alpha_i + \lambda_k)} \quad \ell = 1, \ldots, N. \tag{33}
\]

This procedure results in identification of \(N\) of the coefficients.

Consider next poles of the form \(s = a_k + \lambda_k + \lambda_m\) where \(k \neq m\) and \(k, m = 1, \ldots, N\). Since \(A_{km} = A_{mk}\) for \(k, m \leq N\), the terms in \(Y_2(s)\) corresponding to the pole at \(\lambda_k + \lambda_m\) are given by

\[
Y_{2km}(s) = \sum_{i=1}^{L} \sum_{j=1}^{L} A_{km}^{i} \left[ \frac{\alpha_i + \alpha_j + 2\lambda_k}{(\alpha_j + \lambda_k)(\alpha_i + \lambda_k)(\alpha_i + \alpha_j + \lambda_k + \lambda_m)} \right. \\
+ \left. \frac{\alpha_i + \alpha_j + 2\lambda_m}{(\alpha_j + \lambda_m)(\alpha_i + \lambda_m)(\alpha_i + \alpha_j + \lambda_k + \lambda_m)} \frac{1}{s - \lambda_k - \lambda_m} \right]. \tag{34}
\]

If the residue of the pole at \(\lambda_k + \lambda_m\), as evaluated using the pencil-of-functions method, is \(\beta_{km}\), it follows that

\[
A_{km} = \beta_{km} \left\{ \sum_{i=1}^{L} \sum_{j=1}^{L} \left[ \frac{\alpha_i + \alpha_j + 2\lambda_k}{(\alpha_j + \lambda_k)(\alpha_i + \lambda_k)(\alpha_i + \alpha_j + \lambda_k + \lambda_m)} \right. \right. \\
+ \left. \left. \frac{\alpha_i + \alpha_j + 2\lambda_m}{(\alpha_j + \lambda_m)(\alpha_i + \lambda_m)(\alpha_i + \alpha_j + \lambda_k + \lambda_m)} \right] \right\}^{-1} \quad k, m = 1, \ldots, N \quad k \neq m, k < m. \tag{35}
\]
This procedure results in identification of \( N(X - 1) \) coefficients.

The remaining unknown \( N \) coefficients cannot be evaluated directly, as was done in equation (5.0) and (5.0), because the residues of the other poles, \( Y_p(x) \) involve linear combinations of more than one unknown coefficient. However, if the number of exponential input signals, \( I \), is set equal to \( N \), \( N \) linearly independent equations, involving the \( N \) unknown \( A_k(k) \) coefficients, can be obtained by considering the poles of \( Y_p(x) \) of the form: \( a_1 A_1 + 1 \), ..., \( a_N A_N \), in a manner similar to the above analysis. Thus fact is proven in Reference 1. Solution of the \( N \) equations completes the identification process.

E. IDENTIFICATION TECHNIQUE PROCESSING

The required identification technique processing is done on a nonreal-time basis using a general-purpose digital computer. The processing uses the input and output measurements of the system under test, which are obtained in real time. The computer program used to perform the identification technique processing is described in this section.

The computer program listing is presented in Appendix A. The inputs to the program include:

1. Number of output samples, \( M \)
2. Sampling interval
3. System order, \( 3N \)
4. Analytical description of input and output

This study assumes that the order of the system under test is known. In general, this information may or may not be known. A technique was discussed in paragraph 4.1.3 that resulted in determination of system order using the pencil of functions approach. This technique may be limited by the numerical accuracy of the digital computer and is an issue that merits further attention. In general, determining system order is a key problem in system identification and an in-depth analysis of this problem is beyond the scope of the current study.

An important aspect of the identification technique processing is the determination of the inner product entries of the Gram matrix equation (2.10). These entries are the result of several integrations of the input and output data. When analytical or analog integration is not used, numerical integration techniques are implemented.
The input and output functions are integrated using Simpson's rule of integration (Reference 5), given by

\[
\int_{a}^{b} y(t) \, dt = \frac{(b - a)}{6n} \left[ y(0) + 4y(\Delta T) + 2y(2\Delta T) + 4y(3\Delta T) \\
+ \ldots + 2y((2n - 2)\Delta T) + 4y((2n - 1)\Delta T) \\
+ y(2n\Delta T) \right]
\]

where

\[\Delta T = \frac{b - a}{2n} = \text{time between samples}\]

\[2n = \text{number of subintervals between data points.}\]

The effect of numerical integration techniques on the performance of the identification technique will be addressed in Part II of this study.

The remaining processing involves matrix manipulations which are accomplished using standard FORTRAN computer subroutines, as listed in Appendix A.

C. PERFORMANCE INDICES FOR THE IDENTIFICATION TECHNIQUE

A first step in assessing the performance of given implementation of the identification technique is to establish a set of performance indices which adequately reflects that performance. This is not a simple task, as performance indices are very numerous and in many cases require subjective interpretation. The intent in this study has been to establish a set of performance indices that is used consistently for all implementations and that reflects, at least for comparison purposes, the performance of the identification technique.

Two primary performance indices were used during the study:

1. Percentage error between the predicted system poles and residues and the actual system poles and residues
2. Normalized mean-squared error between predicted system output response and actual system response.
The percentage error index of performance indicates how well the technique identifies each pole and residue of the test system. The percentage error is given by

\[
E_{\text{pole}} = \frac{(\text{Predicted System Pole}) - (\text{Actual System Pole})}{\text{Actual System Pole}} \times 100
\]

\[
E_{\text{residue}} = \frac{(\text{Predicted System Residue}) - (\text{Actual System Residue})}{\text{Actual System Residue}} \times 100
\]

The normalized mean squared error is defined by the equation

\[
\text{NMSE} = \frac{\frac{1}{T} \int_{0}^{T} (y_p - y_a)^2 \, dt}{\frac{1}{T} \int_{0}^{T} y_a^2 \, dt}
\]

(39)

where

- \(y_p(t)\) is the predicted system output to input \(x(t)\)
- \(y_a(t)\) is the actual system output to input \(x(t)\)
- \(T\) is the period of integration

The normalized mean squared error performance index indicates how well the predicted system response approximates the actual response to the same input. It is possible to construct this performance index in this study because the actual system response is analytically known for the systems considered. This index of performance is better than the percentage error in the sense that it evaluates the influence of errors in the poles and residues on predicting system responses. It is possible that a very large error in a pole or residue (>100 percent) will have only a minor impact on normalized mean squared error since the pole and residue contribute negligibly to the total system output.
This study considers systems whose outputs generally consist of sums of exponential functions. In these cases, the predicted system output and actual system output are represented as:

\[ y_p(t) = \sum_{i=1}^{N} R_p e^{-\lambda_p t} \quad t > 0 \]  
\[ y_a(t) = \sum_{i=1}^{N} R_a e^{-\lambda_a t} \quad t > 0 \]  

The normalized mean squared error is given by

\[ \text{NMSE} = \frac{F}{D} \]  

where

\[ F = \sum_{i=1}^{N} \sum_{j=1}^{N} \left[ \frac{R_p e^{(\lambda_p + \lambda_p) T}}{(\lambda_p + \lambda_p)^2} - 1 \right] \]  
\[ D = \sum_{i=1}^{N} \sum_{j=1}^{N} \left[ \frac{(\lambda_a + \lambda_a) T}{(\lambda_a + \lambda_a)^2} - 1 \right] \]
One remaining issue in the area of performance indices is the interpretation of the results. The question is "How accurate must the identification technique be to achieve a satisfactory level of performance?" The absolute accuracy requirements depend on the application of the technique. If a precise description of the system under test is required, then percentage errors of 0.05 to 0.1 might be necessary. On the other hand, prediction of the poles of a system to within 10 to 20 percent may be more than adequate in some cases.

Similarly, the interpretation of the normalized mean square error (NMSE) also causes this dilemma. For this study, an arbitrary level of minimum performance has been established which corresponds to that level of NMSE induced by a 10-percent error in each pole and residue. This NMSE performance level is a function of the system under test and is established quantitatively for the test systems considered later in the report.

It should be noted that significantly better performance of the identification technique will generally be desired, but this level of minimum performance will permit determination of a set of minimum system requirements for each implementation of the technique.
SECTION III
IMPLEMENTATION FEASIBILITY STUDY

A. IMPLEMENTATION APPROACHES

The basic objective of this study phase is to establish requirements for implementation of the identification technique described in Section II. Three basic implementations were considered:

(1) Digital - the input and output of the system under test are sampled using analog-to-digital (A/D) converters and all subsequent processing is done on a general-purpose (GP) computer in nonreal time.

(2) Hybrid - the input and output of the system under test are integrated N times by analog integrators and the outputs of each integrator are sampled for further processing on a GP computer.

(3) Analog - the pencil-of-functions processing is implemented using analog components and only the inner products for the Gram matrix are sampled using A/D converters. These samples are then used in a GP computer for solution of the appropriate equations.

These implementations are discussed in paragraphs B, C, and D below and the results of the implementation feasibility study are reported.

B. DIGITAL IMPLEMENTATION

The digital implementation of the identification technique is shown in Figure 6. A signal generator excites the nonlinear system with the appropriate sum of decaying exponential functions. This input and the resultant nonlinear system output are amplified and converted into digital form via A/D converters. The resultant samples are stored in memory for future nonreal-time processing on a general-purpose digital computer using the program described in Section II.A. These input and output samples are then numerically integrated to form the appropriate inner product entries of the Gram matrix for the pencil-of-functions method of system identification.
Figure 6. Digital Implementation of Identification Technique
The requirements for each element of the digital implementation of Figure 6 are discussed in detail below.

1. A/D Converter
   a. Requirements

   A key element of the digital implementation of Figure 6 is the A/D converter used to obtain the input and output data samples for identification processing. The study determined the required performance specifications for the A/D converter to achieve satisfactory identification technique performance and also assessed the state of the art in commercially available A/D converters to determine if the required specifications can be met. Performance specifications for A/D converters are numerous but the major parameters impacting technique performance are resolution and conversion time. The requirements for these parameters were established during the study.

   The identification processing computer simulation was modified to include an A/D converter model which is described in detail below.

   b. Simulation Model

   The A/D converter simulation model is illustrated in Figure 7.

   ![Figure 7. A/D Converter Simulation Model](image)

   The simulation inputs for the A/D converter are: (1) the most significant bit magnitude (MSB) and (2) the number of bits of resolution of the A/D converter (NBITS). The simulation converts the input to the A/D converter to a digital representation according to the input-output representation of Figure 8.

   The level L in Figure 8 corresponds to the magnitude of the least significant bit. The least significant bit is related to the most significant bit by the relation...
Figure 8. Digital Output Voltages vs. Input Voltage
This assumes that one bit is used to indicate the sign (positive or negative) of the input signal.

The output of an A/D converter is a string of digital 1's and 0's that represent the input voltage level. The simulation model of the A/D converter produces a decimal number that is the equivalent of these 1's and 0's. The output of the A/D converter is given by

\[
W' = \text{SIGN} \cdot \sum_{i=1}^{\text{NBITS}-1} \alpha_i \cdot \frac{(\text{MSB})}{2^{i-1}}
\]

for \( \alpha_i \in \{0, 1\} \)

where \( \text{SIGN} = \pm \) depending on polarity of input voltage \( W \).

From Figure 8, if

\[
2\text{MSB} - L < W < 2\text{MSB} - L
\]

then the input voltage \( W \) is not hard limited by the A/D converter. This level determines the value of MSB to be used in the simulation to obtain greatest resolution for a given converter size.

The A/D converter simulation model is given in its FORTRAN representation in Figure 9.

Most commercially available A/D converters have a fixed full-scale input signal level (typically \( \pm 5 \) or \( \pm 10 \) volts). This input signal level determines the magnitude of the most significant bit at the A/D converter output. This implies that an input to the A/D converter will need to be amplified to the full scale input voltage level in order to obtain maximum resolution out of the A/D. This presents little problem to the identification technique if the amplifier is ideal (infinite bandwidth, linear) since its effect can be removed in the nonreal-time processing of the GP computer. Consequently, the simulation...
SUBROUTINE ATOD(W,XMSB,NBITS)
IF(NBITS.LE.0) GO TO 80
U2=0.0
SIGN=-1.
IF(W.GE.0.0) SIGN=1.
XW=W
D=2.0*XMSB
XW=XW*SIGN
20 DELTA2=XMSB
DO 30 I=1,NBITS-1
30 DELTA2=DELTA2/2.
WOUT=2.*XMSB-DELTA2
DO 5 I=1,NBITS
D=D/2.0
Y=ABS(XW-U2)
IF(Y.LE.DELTA2) WOUT=U2
X=U2-D
IF(XW.GE.(2.*XMSB-D/2.)) PRINT."A/D HARD LIMITED SAMPLE"
5 U2=X
IF(XW.LT.DELTA2) WOUT=0.0
IF(XW.GE.(2.*XMSB-D/2.)) PRINT."A/D HARD LIMITED SAMPLE"
70 W=WOUT*SIGN
80 RETURN
END

Figure 9. Listing of FORTRAN Subroutines for A/D Converter
assumes, at this point of the study, that an ideal amplifier is used and the most significant bit of the A/D converter is set according to the level of the function input to it. The effects of a non-ideal amplifier are evaluated in paragraph B.9. below.

c. Performance Evaluation

Two representative systems were used to evaluate the performance of the identification technique and assess requirements for the components of the digital implementation. The first is a two-pole system whose linear and second-order impulse responses were determined in Reference 1. The second is a four-pole system introduced to evaluate the effects of system complexity (number of poles, N, in linear model) on technique performance. The details of these systems and the performance results are presented below.

(1) Two-Pole System Analysis and Results

The initial system selected for investigation was a two-pole linear system with an impulse response given by

\[ h(t) = 2.8069192 \times 10^5 e^{-0.011550998 (2\pi \times 10^6)t} \]
\[-2.7368441 \times 10^8 e^{-10.616986 (2\pi \times 10^6)t} \] (48)

This is a linear representation of the amplifier shown in Figure 10. The poles of the system are at 11.550998 KHz and 10.616986 MHz.

The input to the system was selected to be

\[ x(t) = (1 \times 10^{-3}) e^{-10^7t} u(t) \] (49)
Figure 10. Common Emitter Amplifier Circuit
where \( u(t) \) is a unit step function. This corresponds to the input level required to excite the circuit in Figure 10 in linear operation. The resultant output is given by

\[
y(t) = \left( 2.82744 \times 10^{-1} e^{-0.01550998 (2 \pi \times 10^6)t} \right. \\
+ 4.82616765 \times 10^{-2} e^{-10.616986 (2 \pi \times 10^6)t} \\
- 4.85444205 \times 10^{-2} e^{-10^7t} \right), \quad t \geq 0
\]  
(50)

These representations of \( y(t) \) and \( x(t) \) were used in the computer program as the inputs to the A/D converter of Figure 6. To establish a baseline for performance comparison, the initial simulation run was made without an A/D converter. The accuracy of the samples was equivalent to the GP computer machine accuracy. This result is presented in Table 2 for an integration time of \( 9.6 \times 10^{-6} \) second. Variation of the integration time and sampling interval indicated that the 9.6 \( \mu \)s integration time resulted in best performance. Results for other integration times/sampling intervals are shown later in this section. The results of Table 2 indicate that excellent performance is achieved using the identification technique. The percentage error on all poles and residues is less than 0.05 while the normalized mean squared error is \( 0.41 \times 10^{-8} \). As noted earlier, the minimum level of acceptable performance was set to the normalized mean squared error corresponding to a 10-percent error in each residue and pole. For the system described by equation (48), a 10-percent error in each pole and residue corresponds to a normalized mean square error of

\[
\text{NMSE}_{(10\%)} = 0.63 \times 10^{-3}.
\]  
(51)

The simulation was exercised for various levels of A/D resolution from 8 to 24 bits and the results are presented in Table 3. Figure 11 is a plot of normalized mean squared error as a function of A/D converter resolution. Figure 11 and Table 3 results indicate that little performance improvement is gained for A/D converters in excess of 16 bits resolution. The minimum performance level is exceeded for A/D converters with 10 bits or more resolution.
**TABLE 2. IDENTIFICATION RESULTS FOR PERFECT A/D CONVERTER (MACHINE ACCURACY), DIGITAL IMPLEMENTATION (9.6 µs INTEGRATION TIME)**

<table>
<thead>
<tr>
<th>System Poles (MHz)</th>
<th>System Residues</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Actual</td>
<td>Predicted</td>
<td>Percentage Error</td>
<td>Actual</td>
<td>Predicted</td>
<td>Percentage Error</td>
</tr>
<tr>
<td>0.01550998</td>
<td>0.01545154</td>
<td>-0.05</td>
<td>2.8069192 x 10^5</td>
<td>2.8063116 x 10^5</td>
<td>-0.02</td>
</tr>
<tr>
<td>10.615986</td>
<td>10.615088</td>
<td>-0.0187</td>
<td>-2.7368441 x 10^8</td>
<td>-2.7362615 x 10^8</td>
<td>-0.021</td>
</tr>
</tbody>
</table>
### Table 3. Results for Levels of A/D Converter Resolution from 8 to 24 Bits

| Number of A/D Bits | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Mean Squared Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 100 MHz |
|--------------------|-------------------------------|------------------|----------------------------|------------------|-------------------|-----------------------------------------------|
| No A/D Converter   | 0.011545154                   | -0.05            | 2.8063166E5                | -0.02            | 0.411 x 10^-8     | 0.011                                         |
|                    | 10.615088                     | -0.01787         | -2.7362615E8               | -0.021           |                   |                                               |
| 24                 | 0.011550163                   | -0.0072          | 2.8068418E5                | -0.00275         | 0.983 x 10^-8     | 0.044                                         |
|                    | 10.612980                     | -0.0377          | -2.7357912E8               | -0.0385          |                   |                                               |
| 16                 | 0.011537262                   | -0.119           | 2.8059592E5                | -0.0342          | 0.147 x 10^-7     | 0.029                                         |
|                    | 10.621939                     | 0.0466           | -2.7381345E8               | 0.047            |                   |                                               |
| 14                 | 0.01157308                    | 0.191            | 2.8108237E5                | 0.139            | 0.174 x 10^-5     | 0.042                                         |
|                    | 10.560624                     | -0.5308          | -2.7233161E8               | -0.494           |                   |                                               |
| 12                 | 0.011565797                   | 0.128            | 2.8179798E5                | 0.394            | 0.185 x 10^-5     | 0.059                                         |
|                    | 10.575364                     | -0.392           | -2.7294636E8               | -0.27            |                   |                                               |
| 10                 | 0.010017392                   | -13.2            | 2.7057878E5                | -3.6             | 0.49 x 10^-4      | -1.06                                         |
|                    | 10.355187                     | -2.46            | -2.678456E8                | -2.13            |                   |                                               |
| 8                  | 0.0048517152                  | -58.             | -2.9278812E4               | -204.3           | 0.367             | Not Calculated                                |
|                    | 10.942193                     | 3.06             | -1.1073848E8               | -59.5            |                   |                                               |
Figure 11. Normalized Mean Square Error vs. A/D Converter Resolution for Two-Pole System (Integration Time = 9.6 μs; Sampling Time = 4 ns)
Another performance measure is indicated in Table 4 which corresponds to the maximum error in the magnitude squared of the transfer function, \(|H(s)|^2\), over the frequency range of 1 kHz to 100 MHz. This error is less than 0.06 dB for A/D converters with more than 12 bits resolution.

These simulation runs were repeated for different integration time periods and sampling intervals. These results are tabulated in Tables 4 to 6 and are summarized in Figure 12. These results indicate that no significant difference in performance is noted for integration times of 4.8 \(\mu\)s or greater.

(2) Four-Pole System Analysis and Results

The two-pole system identification example presented above leads to the conclusion that it is feasible to consider an experimental implementation of the identification technique (as far as A/D converter resolution requirements are concerned). It is necessary to consider systems with more than two poles because, as the system complexity (number of poles) increases, the computational load increases and it is expected that the impact of error in the input and output samples will be greater. Therefore, a four-pole system was investigated to determine the effect of system complexity on implementation requirements and performance.

The four-pole system considered had an impulse response given by

\[
h(t) = 2.8069192 \times 10^5 e^{-0.011550998 (2 \pi \times 10^6)t} - 1.20 \times 10^7 e^{-0.510 (2 \pi \times 10^6)t} + 1.51 \times 10^7 e^{-0.82 (2 \pi \times 10^6)t} - 1.61 \times 10^8 e^{-6.50 (2 \pi \times 10^6)t}
\] (52)

Several trial runs led to the selection of a 4.8 \(\mu\)s integration time and a 1.5 ns sampling interval. The initial set of results was run for a perfect A/D converter. These results are presented in Table 7. The results for this example indicate acceptable performance of the identification technique; however, the performance is not as good as was achieved for the two-pole example. There are several potential reasons for this lower level of performance. The first explanation is the increased
| Number of A/D Bits | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Mean Squared Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 1 MHz |
|--------------------|-----------------------------|------------------|---------------------------|------------------|-------------------|----------------------------------|
| No A/D Converter   | 0.011565417                | 0.125            | 2.8081012E5              | 0.04             | 0.387 x 10^-7     | -0.08                           |
|                    | 10.608509                  | -0.08            | -2.7347864E8             | -0.075           |                   |                                  |
| 16                 | 0.011541588                | -0.08            | 2.8067905E5              | -0.0046          | 0.351 x 10^-8     | 0.025                           |
|                    | 10.615394                  | -0.015           | -2.7365799E8             | 0.009            |                   |                                  |
| 14                 | 0.011528914                | -0.191           | 2.8075629E5              | -0.0229          | 0.734 x 10^-7     | 0.067                           |
|                    | 10.611083                  | -0.055           | -2.7360498E8             | -0.029           |                   |                                  |
| 12                 | 0.011562609                | 0.100            | 2.8222309E5              | 0.545            | 0.222 x 10^-5     | 0.118                           |
|                    | 10.600426                  | -0.156           | -2.7367906E8             | -0.00195         |                   |                                  |
| 10                 | 0.011648442                | 0.843            | 2.8312792E5              | 0.868            | 0.132 x 10^-3     | -0.43                           |
|                    | 10.228063                  | 3.66             | -2.6608803E8             | -2.77            |                   |                                  |
| 8                  | 0.0053343822               | -53.8            | -1.1663478E4             | -104.0           | 0.18              | Not Calculated                   |
|                    | 10.863888                  | 2.32             | -1.6087431E8             | -41.2            |                   |                                  |
TABLE 5. RESULTS FOR LEVELS OF A/D CONVERTER RESOLUTION,  
INTEGRATION TIME = 4.8 µs, SAMPLING INTERVAL = 2 ns

| Number of A/D Bits | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Mean Squared Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 100 MHz |
|--------------------|-----------------------------|------------------|---------------------------|------------------|-------------------|---------------------------------|
| No A/D Converter   | 0.011620899                 | 0.605            | 2.8107143E5               | 0.135            | 0.154 x 10^{-7}   | -0.177                          |
|                    | 10.612452                   | -0.0427          | -2.7359561E8              | -0.032           |                   |                                 |
| 16                 | 0.011003596                 | -4.744           | 2.7786488E5               | -1.0             | 0.622 x 10^{-6}   | 0.968                           |
|                    | 10.644432                   | 0.2383           | -2.7420457E8              | 0.19             |                   |                                 |
| 14                 | 0.011016497                 | -4.63            | 2.7853243E5               | -0.77            | 0.404 x 10^{-6}   | 0.985                           |
|                    | 10.642807                   | 0.2438           | -2.7432920E8              | 0.236            |                   |                                 |
| 12                 | 0.011173394                 | -3.27            | 2.8101151E5               | 0.114            | 0.249 x 10^{-5}   | 0.938                           |
|                    | 10.633183                   | 0.1524           | -2.7447830E8              | 0.29             |                   |                                 |
| 10                 | 0.0044293814                | -61.63           | 2.9211082E5               | 4.07             | 0.196 x 10^{-2}   | 23.2                            |
|                    | 10.813444                   | 3.851            | -2.9038197E8              | 6.1              |                   |                                 |
| 8                  | 0.0027540105                | -76.2            | -2.4200426E4              | -108.6           | 0.266             | Not Calculated                  |
| Number of A/D Bits | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Mean Squared Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 1 MHz |
|-------------------|-----------------------------|------------------|--------------------------|-----------------|-------------------|-----------------------------------------------|
| No A/D Converter  | 0.012876359                 | 11.47            | 2.8427807E5              | 1.27            | 0.204 x 10^-6     | 3.96                                          |
|                   | 10.613347                   | -0.034           | -2.7372492E8             | 0.0148          |                   |                                               |
| 16                | 0.018471276                 | 59.9             | 3.0007228E5              | 6.9             | 0.608 x 10^-5     | 11.2                                          |
|                   | 10.595075                   | -0.206           | -2.738586E8              | 0.0636          |                   |                                               |
| 14                | 0.013670863                 | 18.35            | 2.8783611E5              | 2.54            | 0.206 x 10^-5     | 5.65                                          |
|                   | 10.615823                   | -0.011           | -2.7407198E8             | 0.1416          |                   |                                               |
| 12                | 0.0083855822                | -27.4            | 2.8361473E5              | 1.04            | 0.239 x 10^-4     | 10.0                                          |
|                   | 10.630804                   | 0.13             | -2.752973E8              | 0.589           |                   |                                               |
| 10                | 0.015998973                 | 38.5             | 2.9614702E5              | 5.5             | 0.12 x 10^-3      | -9.2                                          |
|                   | 10.728059                   | 1.046            | -2.793664E8              | 2.076           |                   |                                               |
| 8                 | 0.013912348                 | 20.4             | 4.1746044E5              | 48.7            | 0.526 x 10^-2     | -1.26                                         |
|                   | 10.757434                   | 1.32             | -2.9730088E8             | 8.63            |                   |                                               |
Figure 12. Results of A/D Converter Resolution Simulation Runs for Two-Pole System
<table>
<thead>
<tr>
<th>System Poles (MHz)</th>
<th>System Residues</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual</td>
</tr>
<tr>
<td>0.011550998</td>
<td>0.011279618</td>
</tr>
<tr>
<td>0.510</td>
<td>0.4988702</td>
</tr>
<tr>
<td>0.82</td>
<td>0.8540037</td>
</tr>
<tr>
<td>6.5</td>
<td>6.453757</td>
</tr>
</tbody>
</table>

TABLE 7. FOUR-POLE SYSTEM, PERFECT A/D CONVERSION
computational load required to form the inner products for the Gram matrix. Each integration of input and output using the Simpson's rule integration technique results in a reduction of the number of samples that can be used for the next integration. This is illustrated below.

Consider the output samples $y_1(0)$, $y_1(T)$, $y_1(2T), \ldots, y_1(2nT)$, where $nT$ is the $n$th sample and $T$ is the sampling interval. The integral of $y_1(t)$, $y_2(t)$, as obtained using Simpson's rule, is given by the samples $y_2(0)$, $y_2(2T)$, $y_2(4T), \ldots, y_2(2nT)$.

It is noted that there are only $nT$ samples of $y_2(t)$ whereas there were $2nT$ samples of $y_1(t)$. As this output is successively integrated, the time distance between samples increases and the numerical accuracy of the integration technique is expected to decrease. This will have an adverse effect on the performance of the identification technique and is a contributor to the difference in performance achieved for a two-pole system and four-pole system.

A second potential reason for the performance degradation of the identification technique is the wide-band nature of the selected system. Previous studies (Reference 6) have demonstrated that the technique should not be applied directly to wide-band systems. For these systems, the frequency range is divided into low, medium, and high ranges and the technique is applied to each range of the frequencies. The resultant transfer functions are then appropriately merged to form the total system transfer function. These are two explanations of the performance degradation experienced as system complexity increases. Part II of this study will consider this phenomenon in more detail.

The performance results of Table 7 were based on a perfect A/D conversion capability. The effect of A/D converter resolution on technique performance was investigated and the results are presented in Table 8.

The results of Table 8 indicate that satisfactory performance of the identification technique is achieved for an A/D converter with 20 bits or greater resolution. The results indicate that the identification technique predicts system poles with acceptable accuracy for a A/D converter of 12-14 bits resolution. However, the predicted residues are significantly in error for A/D conversion with less than 20 bits of resolution.
<table>
<thead>
<tr>
<th>Number of A/D Bits</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>No A/D Converter</td>
<td>0.011279618</td>
<td>-2.35</td>
<td>2.789548 x 10^5</td>
<td>-0.619</td>
<td>0.103 x 10^-4</td>
</tr>
<tr>
<td></td>
<td>0.4968702</td>
<td>-2.18</td>
<td>-1.048074 x 10^7</td>
<td>-12.66</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8540037</td>
<td>4.14</td>
<td>1.3534398 x 10^7</td>
<td>-10.36</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.453757</td>
<td>-0.711</td>
<td>-1.594465 x 10^8</td>
<td>-0.964</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>0.011284216</td>
<td>-2.3</td>
<td>2.791535 x 10^5</td>
<td>-0.548</td>
<td>0.108 x 10^-5</td>
</tr>
<tr>
<td></td>
<td>0.49891</td>
<td>-2.17</td>
<td>-1.062 x 10^7</td>
<td>-11.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.853884</td>
<td>4.13</td>
<td>1.39232 x 10^7</td>
<td>-7.79</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.454</td>
<td>-0.707</td>
<td>-1.6059077 x 10^8</td>
<td>-0.254</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>0.011199456</td>
<td>-3.04</td>
<td>2.8101495 x 10^5</td>
<td>0.115</td>
<td>0.2 x 10^-2</td>
</tr>
<tr>
<td></td>
<td>0.498283</td>
<td>-2.297</td>
<td>-1.2463 x 10^7</td>
<td>3.86</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.855755</td>
<td>4.36</td>
<td>1.921179 x 10^7</td>
<td>27.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.4495</td>
<td>-0.776</td>
<td>-1.764755 x 10^8</td>
<td>9.6</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>0.01050104</td>
<td>-9.1</td>
<td>3.337596 x 10^5</td>
<td>18.9</td>
<td>0.131 x 10^1</td>
</tr>
<tr>
<td></td>
<td>0.492189</td>
<td>-3.49</td>
<td>-5.46427 x 10^7</td>
<td>355.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.877295</td>
<td>6.99</td>
<td>1.48004 x 10^8</td>
<td>880.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.40103</td>
<td>-1.52</td>
<td>-5.695889 x 10^8</td>
<td>253.0</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>0.01269649</td>
<td>5.35</td>
<td>4.7975 x 10^5</td>
<td>70.9</td>
<td>0.13 x 10^2</td>
</tr>
<tr>
<td></td>
<td>0.4992365</td>
<td>-2.11</td>
<td>-1.634088 x 10^8</td>
<td>1261.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.86406</td>
<td>5.37</td>
<td>4.474 x 10^8</td>
<td>2862.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.455498</td>
<td>0.684</td>
<td>-1.4533 x 10^9</td>
<td>802.0</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>0.01381562</td>
<td>19.6</td>
<td>1.6083188 x 10^7</td>
<td>5629.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.519115</td>
<td>1.78</td>
<td>-1.480015 x 10^10</td>
<td>1.23 x 10^5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8355322</td>
<td>1.89</td>
<td>3.653195 x 10^10</td>
<td>2.41 x 10^5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.473508</td>
<td>-0.407</td>
<td>-1.0109 x 10^11</td>
<td>6.27 x 10^4</td>
<td></td>
</tr>
</tbody>
</table>
This reflects the impact of errors that result when the system output is numerically integrated four times.

These results suggest difficulty in achieving identification of systems with four or more poles because the maximum resolution of commercially available A/D converters is 16 bits.

d. A/D Conversion Time Requirements

In addition to resolution, another important A/D converter performance parameter is conversion time. The conversion time is defined as the time required for a complete measurement by an analog-to-digital converter. The conversion time defines the rate at which the input to the A/D converter can be sampled.

The sampling interval impacts the performance of the identification technique since numerical integration techniques are used to form the Gram matrix inner products. In order to determine the sampling interval required for satisfactory performance of the identification technique, the sampling rate was varied using the computer simulation. A summary of results is presented in Tables 9 through 13. Table 9 presents the results for a perfect A/D converter and Tables 10 to 13 present results for 16, 14, 12, and 10 bit A/D converters, respectively. These results are plotted in Figure 13.

These results indicate that the sampling interval should be on the order of 8 nanoseconds for the system output with an upper break frequency of 10.62 MHz. It is also observed that this interval can be increased to 24 nanoseconds with a slight degradation in performance. This implies that the sampling rate is between 41.6 and 125 MHz for a 10.6 MHz signal. If the Nyquist rate is defined as being twice the highest break frequency of the output function, or 21.2 MHz, the recommended sampling interval for the two-pole system investigated is approximately 2 to 6 times the Nyquist rate.

These conclusions could change as more complex (N > 2) systems are taken into consideration. This is due to the "shrinking number of samples" characteristic of the Simpson's rule of integration. It is necessary to sample the output of the system under test at a rate sufficient to generate enough samples for the final integration.

It is clear from these results that the sampling rate required is driven by the need for accuracy of numerical integration and not by Nyquist sampling constraints.
| Sampling Interval (ns) | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 100 MHz | Mean Squared Error |
|-----------------------|-----------------------------|------------------|---------------------------|------------------|---------------------------------|--------------------|
| 4                     | 0.011545154 | 0.01787 | 2.8063116E5 | 0.021 | 0.011 | 0.411 x 10^-8 |
| 6                     | 0.011548873 | 0.26   | 2.8067558E5 | 0.26  | 0.022 | 0.467 x 10^-6 |
| 8                     | 0.011522691 | 0.335  | 2.8040241E5 | 0.355 | 0.0577 | 0.88 x 10^-6 |
| 12                    | 0.011501365 | 0.429  | 2.8019682E5 | 0.176 | 0.1136 | 0.91 x 10^-5 |
| 16                    | 0.011498709 | 0.452  | 2.8017916E5 | 0.182 | 0.138 | 0.19 x 10^-4 |
| 24                    | 0.011620742 | 0.604  | 2.8142850E5 | 0.262 | 0.124 | 0.285 x 10^-4 |
### TABLE 10. SAMPLING INTERVAL RESULTS FOR 16-BIT A/D CONVERTER, INTEGRATION TIME = 9.6 µS

| Sampling Interval (ns) | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 100 MHz | Mean Squared Error |
|------------------------|-------------------------------|------------------|---------------------------|------------------|---------------------------------|-------------------|
| 4                      | 0.011537262 10.621939         | -0.119 0.0466    | 2.8059592E5 -2.7381345E8 | -0.0342 0.04715 | 0.029                           | 0.147 x 10^-7     |
| 6                      | 0.011537338 10.600888         | -0.1182 -0.1516  | 2.8056244E5 -2.7325026E8 | -0.04613 0.1586 | 0.0279                           | 0.172 x 10^-6     |
| 8                      | 0.011503870 10.593911         | -0.408 -0.217    | 2.8028340E5 -2.7304170E8 | -0.1455 -0.2348 | 0.0978                           | 0.399 x 10^-6     |
| 12                     | 0.011507740 10.493012         | -0.3744 -1.167   | 2.8026737E5 -2.7034192E8 | -0.1512 -1.221 | 0.105                           | 0.103 x 10^-9     |
| 16                     | 0.011502428 10.447852         | -0.42 -1.593     | 2.8027978E5 -2.6900207E8 | -0.1468 -1.71  | 0.154                           | 0.211 x 10^-4     |
| 24                     | 0.011622867 10.535917         | 0.622 -0.763     | 2.8145425E5 -2.7037742E8 | 0.2715 -1.208  | 0.1199                          | 0.289 x 10^-4     |
| Sampling Interval (ns) | Predicted System Poles (MHz) | Predicted System Residues | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 100 MHz | Mean Squared Error |
|----------------------|-----------------------------|---------------------------|----------------------------------|-------------------|
| 4                    | 0.0115573082 10.560624      | 2.8108237E5 -2.7233161E8  | 0.0426                           | 0.173 x 10^-5    |
| 6                    | 0.011551605 10.566747       | 2.8087744E5 -2.7246056E8  | 0.0385                           | 0.139 x 10^-5    |
| 8                    | 0.011522615 10.547927       | 2.8066333E5 -2.7195890E8  | 0.0767                           | 0.269 x 10^-5    |
| 12                   | 0.011490437 10.488631       | 2.8030790E5 -2.7030774E8  | 0.1477                           | 0.103 x 10^-4    |
| 16                   | 0.011485884 10.466335       | 2.8021712E5 -2.6949992E8  | 0.1922                           | 0.169 x 10^-4    |
| 24                   | 0.011609131 10.527826       | 2.8166121E5 -2.7029216E8  | 0.1726                           | 0.258 x 10^-4    |
### TABLE 12. SAMPLING INTERVAL RESULTS FOR 12-BIT A/D CONVERTER, INTEGRATION TIME = 9.6 µs

| Sampling Interval (ns) | Predicted System Poles (MHz) | Percentage Error | Predicted System Residues | Percentage Error | Maximum Error in $|H(s)|^2$ (dB) for 1 kHz to 100 MHz | Mean Squared Error |
|------------------------|------------------------------|------------------|---------------------------|------------------|-----------------------------------|-------------------|
| 4                      | 0.01156579 10.575364         | 0.128 -0.392     | 2.8179798E5 -2.7294636E8 | 0.394 -0.2697    | 0.059                             | 0.185 x 10^{-5}   |
| 6                      | 0.011525954 10.587743        | -0.2168 -0.2754  | 2.8187778E5 -2.7342334E8 | 0.422 -0.095     | 0.1679                            | 0.311 x 10^{-5}   |
| 8                      | 0.011539311 10.574969        | -0.1011 -0.3957  | 2.8081213E5 -2.7259698E8 | 0.0428 -0.397    | 0.057                             | 0.105 x 10^{-5}   |
| 12                     | 0.011529217 10.515567        | -0.1885 -0.955   | 2.8103355E5 -2.7106579E8 | 0.1217 -0.9568   | 0.123                             | 0.611 x 10^{-5}   |
| 16                     | 0.011496888 10.440006        | -0.468 -1.667    | 2.8060646E5 -2.6884574E8 | -0.0304 -1.768   | 0.211                             | 0.22 x 10^{-4}    |
| 24                     | 0.011619679 10.490084        | 0.594 -1.195     | 2.8208909E5 -2.6939983E8 | 0.4977 -1.565    | 0.19                              | 0.3 x 10^{-4}     |
TABLE 13. SAMPLING INTERVAL RESULTS FOR 10-BIT A/D CONVERTER,
INTEGRATION TIME = 9.6 μs

<table>
<thead>
<tr>
<th>Sampling Interval (ns)</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Maximum Error in</th>
<th>Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$</td>
<td>H(s)</td>
</tr>
<tr>
<td>4</td>
<td>0.010017392</td>
<td>-13.27</td>
<td>2.7057878E5</td>
<td>-3.6</td>
<td>-1.06</td>
<td>0.49 x 10^{-4}</td>
</tr>
<tr>
<td></td>
<td>10.355187</td>
<td>-2.46</td>
<td>-2.678456E8</td>
<td>-2.13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0.01001557</td>
<td>-13.29</td>
<td>2.7150760E5</td>
<td>-3.27</td>
<td>-1.09</td>
<td>0.7 x 10^{-4}</td>
</tr>
<tr>
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<td>10.316076</td>
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<td>-2.6727096E8</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.01000578</td>
<td>-13.37</td>
<td>2.7116091E5</td>
<td>-3.39</td>
<td>-1.09</td>
<td>0.754 x 10^{-4}</td>
</tr>
<tr>
<td></td>
<td>10.287152</td>
<td>-3.1</td>
<td>-2.6632976E8</td>
<td>-2.69</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>0.0099222242</td>
<td>-14.1</td>
<td>2.7140996E5</td>
<td>-3.30</td>
<td>-1.21</td>
<td>0.11 x 10^{-3}</td>
</tr>
<tr>
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<td>10.219084</td>
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<td>-2.6491260E8</td>
<td>-3.20</td>
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<td></td>
</tr>
<tr>
<td>16</td>
<td>0.0099410072</td>
<td>-13.94</td>
<td>2.7199783E5</td>
<td>-3.097</td>
<td>-1.19</td>
<td>0.133 x 10^{-3}</td>
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<tr>
<td></td>
<td>10.164943</td>
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<td>-2.6339261E8</td>
<td>-3.76</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>0.010148000</td>
<td>-12.15</td>
<td>2.7214522E5</td>
<td>-3.045</td>
<td>-0.915</td>
<td>0.89 x 10^{-4}</td>
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<tr>
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<td>10.252004</td>
<td>-3.438</td>
<td>-2.6415126E8</td>
<td>-3.48</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 13. Results of Sampling Interval Rate Simulation for All A/D Converters
e. Second-Order Impulse Response Identification

The primary goal of the identification technique is to identify the second-order impulse response of a nonlinear system. It has been shown (Reference 1) that the functional form of the second-order impulse response, $h_2(t_1, t_2)$ is given by equation (25).

The second-order response of a nonlinear system to an input given by

$$x(t) = \sum_{i=1}^{L} e^{\alpha_i t} u(t)$$

has also been shown to be (Reference 1) given by

$$y_2(s) = \sum_{k_1=1}^{M} \sum_{k_2=1}^{N} \sum_{l=1}^{L} A_{k_1 k_2}$$

$$\frac{\alpha_i + \alpha_j + 2a_{k_1}}{(\alpha_j + a_{k_1})(\alpha_i + a_{k_1})(\alpha_j + a_{k_1} + a_{k_2})} \frac{1}{s - (a_{k_1} + a_{k_2})}$$

$$- \frac{1}{(\alpha_j + a_{k_1})(\alpha_i + a_{k_2})} \frac{1}{s + (\alpha_j - a_{k_2})}$$

$$- \frac{1}{(\alpha_i + a_{k_1})(\alpha_j + a_{k_2})} \frac{1}{s + (\alpha_i - a_{k_2})}$$

$$+ \frac{\alpha_i + \alpha_j + 2a_{k_2}}{(\alpha_j + a_{k_2})(\alpha_i + a_{k_2})(\alpha_i + \alpha_j + a_{k_1} + a_{k_2})} \frac{1}{s + \alpha_i + \alpha_j}$$

where

$$\alpha_j \neq a_{k_1}$$

for $j = 1, \ldots, L; \ k_1 = 1, \ldots, M$

$$a_1 + \alpha_j + a_{k_1} + a_{k_2} \neq 0$$

for $i, j = 1, \ldots, L; \ k_1 = 1, \ldots, M;$

$$a_{k_1} \neq a_{k_2}$$

for $k_2 = 1, \ldots, N; \ k_1 = N + 1 \ldots, M.$

(55)
The quantities $a_{k_1}$, $a_{k_2}$, $M$ and $N$ were shown in Section II to be known from identification of the linear impulse response, $h_1(t)$. The remaining unknown quantities, $A_k$, are identifiable from the residues of the second-order response. These residues are given by the equation

$$R = C^{-1}Y$$

(56)

where

$$R = \text{residue matrix} = \begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ \vdots \\ R_N \end{bmatrix}$$

(57)

$$Y = \text{output matrix} = \begin{bmatrix} \bar{Y}_2(T) \\ \bar{Y}_3(T) \\ \bar{Y}_4(T) \\ \vdots \\ \bar{Y}_{N+1}(T) \end{bmatrix}$$

(58)

where

$$\bar{y}_i = (i - 1)\text{th integral of } y(t)$$

$$C = N \times N \text{ matrix whose } ij \text{th element is defined by}$$

$$C_{ij} = \frac{p_{j}(T)}{\lambda_j} - \frac{i}{\Sigma m=1} \frac{x_{m+1}(T)}{(\lambda_j)^{i+1-m}}$$

(59)

where

$$p_{j}(T) = \int_0^T e^{\lambda_j (T-\tau)} x(\tau) \, d\tau$$

(60)
\[ x_i(T) = i^{\text{th}} \text{ integration of input } x(t) \text{ from } t = 0 \text{ to } t = T \]

\[ x_i(t) = \delta(t), \text{ unit impulse} \]

The key impact of identifying the residues of \( Y_2(s) \) on the implementation requirements is the need to accurately measure \( y_2(T), y_3(T), ..., y_N(T) \), which are the integrated outputs of the nonlinear system. This is explained in detail below.

The system is excited by a input consisting of a sum of decaying exponential functions. The amplitude is selected to excite the linear and second-order responses of the system under test. The system output is \( y_1(t) + y_2(t) \) where \( y_1(t) \) is the linear response and \( y_2(t) \) is the second-order response. The identification technique operates on \( y_2(t) \) so there is a need to isolate \( y_2(t) \) from the total response \( y_1(t) + y_2(t) \). However, since the linear impulse response of the system under test will have been identified previously, the function \( y_1(t) \) is known. Therefore \( y_2(t) \) can be isolated from \( y_1(t) + y_2(t) \). A potential problem arises because \( y_2(t) \) is typically small in magnitude compared to \( y_1(t) \). The implementation equipment will measure \( y_1(t) + y_2(t) \) to the prescribed resolution of the A/D converter but the resolution of \( y_2(t) \) will be lower because the most significant bit of the A/D will be assigned on the basis of the peak magnitude of the input \( y_1(t) + y_2(t) \).

The purpose of this part of the investigation is to determine the A/D converter resolution characteristics required to accurately identify the residues of \( Y_2(s) \) and subsequently the \( A_{k_1k_2} \). The second-order response of the nonlinear system to be used in this study is given by

\[
y_2(t) = \left( 2.575137 \times 10^{-3} e^{-0.11550998 (2 \pi x 10^6) t} - 1.5725176 \times 10^4 e^{-10.616986 (2 \pi x 10^6) t} + 2.3537485 e^{-0.023101996 (2 \pi x 10^6) t} - 3.223955 \times 10^3 e^{-21.233972 (2 \pi x 10^6) t} - 1.3645 e^{-1.603100 (2 \pi x 10^6) t} + 1.2645 \times 10^4 e^{-12.208535 (2 \pi x 10^6) t} - 2.051956 \times 10^2 e^{-3.1830988 (2 \pi x 10^6) t} \right) u(t)
\]
where the input is
\[ x(t) = 10^{-2} e^{-10^7 t} u(t). \]  \hspace{1cm} (62)

This corresponds to an approximate representation of the second-order response of an amplifier circuit whose linear impulse response is given by (Reference 1)

\[ h_1(t) = \begin{pmatrix} 2.8069192 \times 10^5 e^{-0.011550998 (2 \pi x 10^6)t} \\ -2.7368441 \times 10^8 e^{-10.616986 (2 \pi x 10^6)t} \end{pmatrix} u(t) \]  \hspace{1cm} (63)

This is the two-pole system being considered in detail during the study. The expression for the second-order response \( y_2(t) \) is approximate because the actual response would have natural frequencies at

\[ s_1 = -10.616986 (2 \pi x 10^6) \]
\[ s_2 = -10.628537 (2 \pi x 10^6) \]  \hspace{1cm} (64)

These poles arise from the two poles of the linear impulse response \((s_1 = 0.011550998(2 \pi x 10^6)\) and \(s_2 = 10.616986 (2 \pi x 10^6)\)\) according to the relation

\[ s_1 = \lambda_2 \]
\[ s_2 = \lambda_1 + \lambda_2 \]  \hspace{1cm} (65)

Previous analyses (Reference 1) have shown that these poles will cause computational problems in evaluating the residues due to matrix inversion. In order to avoid this problem at this point of the study, \( y_2(t) \) was assumed to have a single pole at \( s_1 = \lambda_2 \) with a residue given by the sum of the residues of \( \lambda_1 \) and \( \lambda_1 + \lambda_2 \) given in Reference 1. The problem of poles of the form \( \lambda_2 + \lambda_1 = \lambda_2 \) will be addressed in Part II of this study.

This second-order response was used in the computer simulation of the identification technique. The results are shown in Table 14. The most significant bit of the
<table>
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<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
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<td>Predicted System Residues</td>
<td>Percentage Error</td>
<td>Normalized Mean Squared Error</td>
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</table>
A/D converter was set by the peak level of the system total response, \( y_1(t) + y_2(t) \). A plot of normalized mean squared error as A/D converter resolution is given in Figure 14.

These results indicate that 14 to 16 bits of resolution is required to achieve a reasonable level of performance.

Another set of simulation runs was made assuming that \( y_2(t) \) could be isolated from the total response \( y_1(t) + y_2(t) \) prior to A/D conversion. This makes it possible to set the most significant bit of the A/D converter based on the peak magnitude of \( y_2(t) \). These results are presented in Table 15. A plot of normalized mean squared error versus A/D converter resolution is provided in Figure 15.

These results indicate that 10 to 12 bits of resolution are sufficient if \( y_1(t) \) can be removed from the total response \( y_1(t) + y_2(t) \) before A/D conversion. This will be, at best, difficult to achieve. This issue of separation of responses will be addressed in more detail in Part II of this study.

f. Additional A/D Converter Requirements

Previous paragraphs have concentrated on the A/D converter parameters of resolution and conversion time. (Cost considerations are provided in paragraph g. below). Conversion time and resolution are the key parameters because they place the most restrictions on the systems to which the identification technique can be applied. However, numerous other A/D converter characteristics must be taken into account when specifying an A/D converter. These include maximum rate of change of input, and absolute accuracy, among others.

The slew rate is an indication of the maximum rate of change of the input that the A/D converter can tolerate and still respond to individually important samples of the input. It is given by (Reference 7).

\[
\frac{dV}{dt}\bigg|_{\text{max}} = 2^{-N} \frac{V_{\text{FS}}}{T_{\text{convert}}} \tag{66}
\]

where \( N \) is the number of A/D converter bits

\( V_{\text{FS}} \) is the full scale input voltage
Figure 14. Second-Order System Response, Integration Time = 3.2 μs, Sampling Interval = 1 ns, MSB Set for $y_1(t) = y_2(t)$
TABLE 15. SECOND-ORDER RESPONSE RESULTS FOR A/D CONVERTERS, INTEGRATION
TIME = 3.2 ms, SAMPLING INTERVAL = 1 ns, MSB SET FOR $y_2(t)$

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<th>Number of A/D Bits</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
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<td>1.60156682</td>
<td>-0.095</td>
<td>-8.938179 x 10^2</td>
<td>6.54 x 10^4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10.365204</td>
<td>-2.1</td>
<td>2.1137867 x 10^4</td>
<td>6.999</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.1830988</td>
<td>0</td>
<td>-1.2048383 x 10^2</td>
<td>-0.00867</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.0048517152</td>
<td>-58.</td>
<td>-0.002157</td>
<td>-16.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10.942193</td>
<td>3.06</td>
<td>-1.5334967 x 10^4</td>
<td>-2.48</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.00970342</td>
<td>-58.</td>
<td>1.9260158</td>
<td>-18.17</td>
<td></td>
</tr>
<tr>
<td></td>
<td>21.884386</td>
<td>3.06</td>
<td>-3.1433888 x 10^3</td>
<td>-5.43</td>
<td>0.118 x 10^-3</td>
</tr>
<tr>
<td></td>
<td>1.59640114</td>
<td>-0.418</td>
<td>1.0950628 x 10^1</td>
<td>-902.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12.533742</td>
<td>2.66</td>
<td>1.9252994 x 10^4</td>
<td>-2.54</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.1830996</td>
<td>0</td>
<td>-9.5911069 x 10^2</td>
<td>5.95</td>
<td></td>
</tr>
</tbody>
</table>
Figure 15. Second-Order System Response, Integration Time = 3.2 μs, Sampling Period = 1 ns. MSB Set for $y_2(t)$
$T_{\text{convert}}$ is the conversion time

If the input signal changes at a rate faster than this maximum, 1 LSB changes in the input cannot be resolved within the sampling period. This problem can be alleviated somewhat by using a sample and hold circuit at the input to the A/D converter. Between conversions, the sample and hold acquires the input signal, and, just before conversion takes place, the signal is placed in hold, where it remains throughout the conversion.

If a sample and hold is used, the rate of change of the input is limited by

$$\left. \frac{dV}{dt} \right|_{\text{max}} = 2^{-N} \frac{V_{\text{FS}}}{t_{\text{apu}}}$$

(67)

where $t_{\text{apu}}$ is the aperture time of the sample and hold. The aperture time of a typical sample and hold is on the order of 2 to 3 ns. This eases the problem described above. The signal conditioning using the sample and hold also tends to improve overall accuracy of the A/D conversion process.

The absolute accuracy error of an A/D converter is the difference between the analog input theoretically required to produce a given digital output code and the analog input actually required to produce that same code (Reference 7). Absolute accuracy error can be caused by several different sources of error. A good A/D converter will have an absolute accuracy of $\pm 1/2$ LSB. This implies that the performance of a 16 bit converter will lie somewhere between the performance predicted for a 16-bit converter and a 15-bit A/D converter.

Other A/D converter parameters, such as input full scale voltage and output code, are not as important as those discussed above. In general they need to be addressed for the particular system under consideration.

### g. Survey of Currently Available A/D Converters

The objective of this phase of the study was to survey the characteristics of commercially available A/D converters to determine if the requirements of paragraphs B.2.c and d above can be met. The key characteristics of interest for this survey were the number of bits of resolution, the conversion time, and the cost. Many companies manufacture commercially available A/D converters, and, of course, these converters vary in performance and cost over a very broad range.
It is not warranted to present a detailed listing of all available A/D converters in this report. Therefore only the general characteristics of these converters will be listed and a selected few will be reviewed in detail. Data for this survey was obtained from A/D converter specification sheets obtained from the following manufacturers (listed in alphabetical order):

- Analog Devices, Inc.
- Analogic Corp.
- Beckman Instruments, Inc.
- Burr-Brown Research Corp.
- Computer Labs, Inc.
- Datel Systems, Inc.
- DDC - ILC Data Device Corp.
- Fairchild Semiconductor
- Ferranti Electric
- Hybrid Systems Inc.
- Intech
- Intersil, Inc.
- Micro Networks Corp.
- National Semiconductor
- Precision Monolithics, Inc.
- Teledyne Semiconductor
- Texas Instruments, Inc.
- TRW LSI Products
- Zeltex, Inc.

The range of available A/D converters is illustrated in Figure 16, which is a plot of A/D converter resolution bits vs conversion time, for converters with less than 1 ms conversion time. Each X represents a device corresponding to a given resolution and conversion time manufactured by one of the companies listed above.

Figure 17 is a plot of minimum conversion speed for each level of resolution. The conversion time is converted to maximum input frequency in Figure 18. Figure 18 indicates that A/D converters of high resolution (14 to 16 bits) cannot accurately convert signals of frequency greater than 100 to 125 kHz. This imposes a significant restriction on the applicability of the identification technique since the results indicate that 14 to 16 bits of A/D converter resolution is generally needed for satisfactory performance. This frequency restriction is even more constrained (20 kHz) when sampling requirements are taken into account.

The general trend of Figure 17 is that the conversion time increases as the resolution increases. The current development trend seems to be directed toward the 8 to 12 bit resolution A/D converter. The 16-bit A/D converters are significantly more costly than a lower resolution converter.
Figure 16. Available A/D Converter Characteristics
Figure 17. Current A/D Converter Conversion Speed Characteristics
(8-12 bits) and not too many devices have appeared on the market. Commercially available 16-bit A/D converters are listed in Table 16.

### TABLE 16. COMMERCIALY AVAILABLE A/D CONVERTERS

<table>
<thead>
<tr>
<th>Conversion Time (ns)</th>
<th>Manufacturer</th>
<th>Cost (dollars)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>Intech</td>
<td>1500.</td>
</tr>
<tr>
<td>10</td>
<td>Zeltex</td>
<td>750.</td>
</tr>
<tr>
<td>20</td>
<td>Zeltex</td>
<td>750.</td>
</tr>
<tr>
<td>25</td>
<td>Analogic</td>
<td>1395.</td>
</tr>
<tr>
<td>30</td>
<td>Analogic</td>
<td>895.</td>
</tr>
<tr>
<td>32</td>
<td>Zeltex</td>
<td>750.</td>
</tr>
<tr>
<td>40</td>
<td>Intech</td>
<td>460.</td>
</tr>
<tr>
<td>100</td>
<td>Micro Networks</td>
<td>220.</td>
</tr>
<tr>
<td>5,000</td>
<td>Analog Devices</td>
<td>1720.</td>
</tr>
<tr>
<td>100,000</td>
<td>Analogic</td>
<td>210.</td>
</tr>
<tr>
<td>200,000</td>
<td>Burr Brown</td>
<td>270.</td>
</tr>
<tr>
<td>250,000</td>
<td>Intersil</td>
<td>---</td>
</tr>
</tbody>
</table>

2. Amplifier Requirements

The digital implementation of the identification technique shown in Figure 6 indicates a pre-A/D converter amplifier. The purpose of this amplifier is to adjust the output of the system under test to the full-scale input level of the A/D converter. Most commercially available A/D converters have a normalized analog input signal level of ±5 or ±10 volts. In order to make complete use of the resolution capability of the A/D converter, it is necessary to adjust the level of the output of the system under test to this input level. For example, consider the two-pole system discussed in paragraph III.B.1.c.(2). This is a representation of the linear portion of an amplifier (Reference 1) and is valid only for low level input voltages (on the order of 1 millivolt). The peak system response to a 1
millivolt input is also on the order of millivolts. If a standard 16-bit A/D converter with a full-scale input voltage level of 10 volts were used in the digital implementation of the identification technique, the samples of the system response would be accurate to only about 5 bits of resolution.

This need for a pre-A/D converter amplifier complicates the identification process. This complication arises because the A/D converter samples the output of the cascaded nonlinear system and the amplifier. The identification technique processes these samples and will attempt to identify the total system, which consists of the system under test in series with the amplifier. This is illustrated in Figure 19.

The identification technique attempts to identify the transfer function

$$H_T(s) = H_1(s) H_A(s)$$

(68)

where $H_1(s)$ is the transfer function of the system under test and $H_A(s)$ is the transfer function of the amplifier. The primary complication introduced by the amplifier is one of dimensionality. If $H_1(s)$ has two poles and $H_A(s)$ has two poles, the identification process will attempt to identify a four-pole system. Since $H_A(s)$ will be known, there is no difficulty in obtaining $H_1(s)$ from $H_T(s)$. It will be necessary to maintain the frequency extent of $H_A(s)$ approximately equal to that of $H_1(s)$ to avoid the wide-band problem discussed in paragraph III.B.1.c. However, the difference in the performance of the
identification technique for a two-pole system and a four-pole system was amply demonstrated in paragraph III.B.1.c.(2). These results suggest that the amplifier may unduly degrade the performance of the technique. It would therefore be advantageous to devise an approach to alleviate the complication introduced by the amplifier. Two approaches were considered during the study and these are discussed below. The first approach to solving the amplifier problem was to use an amplifier that is very wide-band compared to the system under test. This approach is based on the concept that the amplifier frequency response will not significantly affect the frequency response of interest. This is illustrated in Figure 20.

![Figure 20](image)

**Figure 20.** Frequency Extent Comparison for Test System and Amplifier

If $\omega_1 << \omega_a$ and $\omega_2 >> \omega_b$, then

$$H_1(s) H_A(s) \approx H_1(s)$$  (69)

Previous work on the pencil-of-functions technique (Reference 6) has demonstrated that a system can be excited such that only a limited region of its frequency extent significantly affects the output. In order to determine the bandwidth requirements of this amplifier, a set of simulation cases was run. The first amplifier considered has a transfer function given by
The Bode diagram of this transfer function is shown in Figure 21.

\[
H_{A_1}(s) = \frac{100}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \quad \omega_2 > \omega_1 \tag{70}
\]

Figure 21. Bode Diagram of Amplifier with Transfer Function \(H_{A_1}(s)\)

This amplifier model was added to the computer simulation. The system to be identified was the two-pole system described in paragraph III.B.1.c.(1), whose transfer function is given by

\[
H_1(s) = \frac{2.8069192 \times 10^5}{s + 0.011550998 (2\pi) (10^6)} - \frac{2.7368441 \times 10^8}{s + 10.616986 (2\pi) (10^6)} \tag{71}
\]
The break frequencies of the amplifier, \( \omega_1 \) and \( \omega_2 \), were varied and performance of the technique was evaluated. Since \( \omega_1 \) determines the 3-dB bandwidth of the amplifier, it is the key parameter to be evaluated. The number of poles of the system to be identified was set to two in the simulation. Therefore, the identification process operates on the samples of the cascaded system (system under test and amplifier) and attempts to identify only two poles. The results of the simulation are shown in Table 17 for different values of \( \omega_1 \) and \( \omega_2 \). The normalized mean squared error is plotted as a function of \( \omega_1 \) in Figure 22.

![Figure 22. Normalized Mean Squared Error as a Function of \( \omega_1 \)](image)

Figure 22 indicates that an upper break frequency of at least approximately 1000 times the upper break frequency of the system under test is necessary to minimize the effect of the amplifier on identification performance.
TABLE 17. IDENTIFICATION TECHNIQUE PERFORMANCE FOR DIFFERENT AMPLIFIER CONFIGURATIONS, PERFECT A/D CONVERSION, INTEGRATION TIME = 9.6 μs, SAMPLING INTERVAL = 4 ns

AMPLIFIER TRANSFER FUNCTION = \( \frac{1}{(1+\frac{S}{\omega_1})(1+\frac{S}{\omega_2})} \)

<table>
<thead>
<tr>
<th>Filter Poles (MHz)</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.011666102</td>
<td>1.25</td>
<td>2.6233227 ( \times 10^5 )</td>
<td>0.584</td>
<td>0.57 ( \times 10^{-2} )</td>
</tr>
<tr>
<td>100</td>
<td>8.0143939</td>
<td>-24.51</td>
<td>-2.0681498 ( \times 10^6 )</td>
<td>-24.43</td>
<td>0.155 ( \times 10^{-2} )</td>
</tr>
<tr>
<td>100</td>
<td>0.011612318</td>
<td>0.53</td>
<td>2.8139416 ( \times 10^5 )</td>
<td>0.25</td>
<td>0.389 ( \times 10^{-3} )</td>
</tr>
<tr>
<td>200</td>
<td>9.1377518</td>
<td>-13.93</td>
<td>-2.3570199 ( \times 10^8 )</td>
<td>-13.88</td>
<td>0.96 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>200</td>
<td>0.011576915</td>
<td>0.224</td>
<td>2.8099455 ( \times 10^5 )</td>
<td>0.108</td>
<td>0.35 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>400</td>
<td>9.8365571</td>
<td>-7.35</td>
<td>-2.537214 ( \times 10^8 )</td>
<td>-7.29</td>
<td>0.167 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>400</td>
<td>0.011563444</td>
<td>0.1077</td>
<td>2.808394 ( \times 10^5 )</td>
<td>0.0525</td>
<td>0.96 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>800</td>
<td>10.217587</td>
<td>-3.76</td>
<td>-2.6351515 ( \times 10^8 )</td>
<td>-3.72</td>
<td>0.35 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>800</td>
<td>0.011561855</td>
<td>0.0939</td>
<td>2.808174 ( \times 10^5 )</td>
<td>0.0447</td>
<td>0.167 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>1000</td>
<td>10.30997</td>
<td>-2.31</td>
<td>-2.6743464 ( \times 10^8 )</td>
<td>-2.28</td>
<td>0.167 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>1000</td>
<td>0.011560029</td>
<td>0.0782</td>
<td>2.807956 ( \times 10^5 )</td>
<td>0.0369</td>
<td>0.96 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>2000</td>
<td>10.447546</td>
<td>-1.596</td>
<td>-2.6938381 ( \times 10^8 )</td>
<td>-1.57</td>
<td>0.167 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>2000</td>
<td>0.01155798</td>
<td>0.06</td>
<td>2.8077123 ( \times 10^5 )</td>
<td>0.0282</td>
<td>0.49 ( \times 10^{-4} )</td>
</tr>
<tr>
<td>4000</td>
<td>10.524276</td>
<td>-0.873</td>
<td>-2.7133375 ( \times 10^8 )</td>
<td>-0.859</td>
<td>0.11 ( \times 10^{-5} )</td>
</tr>
<tr>
<td>4000</td>
<td>0.011550391</td>
<td>-0.0052</td>
<td>2.8068824 ( \times 10^6 )</td>
<td>-0.0013</td>
<td>0.11 ( \times 10^{-5} )</td>
</tr>
<tr>
<td>8000</td>
<td>10.572337</td>
<td>-0.42</td>
<td>-2.7254702 ( \times 10^8 )</td>
<td>-0.415</td>
<td>0.11 ( \times 10^{-5} )</td>
</tr>
<tr>
<td>8000</td>
<td>0.011554565</td>
<td>0.0145</td>
<td>2.8073282 ( \times 10^5 )</td>
<td>0.031</td>
<td>0.708 ( \times 10^{-6} )</td>
</tr>
<tr>
<td>10000</td>
<td>10.581781</td>
<td>-0.33</td>
<td>-2.7279100 ( \times 10^6 )</td>
<td>-0.33</td>
<td>0.708 ( \times 10^{-6} )</td>
</tr>
<tr>
<td>10000</td>
<td>0.011548797</td>
<td>-0.019</td>
<td>2.8067059 ( \times 10^5 )</td>
<td>-0.0076</td>
<td>0.256 ( \times 10^{-6} )</td>
</tr>
<tr>
<td>20000</td>
<td>10.596042</td>
<td>-0.197</td>
<td>-2.7314685 ( \times 10^6 )</td>
<td>-0.196</td>
<td>0.136 ( \times 10^{-6} )</td>
</tr>
<tr>
<td>20000</td>
<td>0.011554792</td>
<td>-0.033</td>
<td>2.8073499 ( \times 10^5 )</td>
<td>0.0153</td>
<td>0.136 ( \times 10^{-6} )</td>
</tr>
<tr>
<td>20000</td>
<td>0.011554154</td>
<td>-0.145</td>
<td>-2.7329259 ( \times 10^8 )</td>
<td>-0.143</td>
<td>0.136 ( \times 10^{-6} )</td>
</tr>
<tr>
<td>200000</td>
<td>0.01155088</td>
<td>-0.0187</td>
<td>-2.7362615 ( \times 10^8 )</td>
<td>-0.021</td>
<td>0.411 ( \times 10^{-8} )</td>
</tr>
</tbody>
</table>
The low frequency characteristics required of the amplifier were investigated using an amplifier with a transfer function of the form

$$H_{A2}(s) = \frac{K\left(1 + \frac{s}{\omega_1}\right)}{(1 + \frac{s}{\omega_2})(1 + \frac{s}{\omega_3})}$$

(72)

$$\omega_1 < \omega_2 < \omega_3$$

The Bode diagram of this transfer function is shown in Figure 23.

Figure 23. Bode Diagram of Amplifier with Transfer Function $H_{A2}(s)$
The break frequencies of the amplifier were varied and the performance of the identification technique evaluated.

These results are summarized in Table 18. A plot of normalized mean squared error versus $\omega_2$ for $\omega_1 = \omega_2/10$ and selected values of $\omega_3$ is presented in Figure 24. These results indicate that the lower break frequency of the amplifier, $\omega_2$, should be, at least, approximately $1/4 \omega_0$ of the lowest break frequency of the system under test to minimize the impact of the amplifier on the results.

$$H_A(s) = \frac{k_1(s+\omega_1)}{(s+\omega_2)(s+\omega_3)}$$

Figure 24. Identification Technique Performance as a Function of Amplifier Characteristic
### Table 18. Identification Technique Performance for Different Amplifier Configurations, Perfect A/D Conversion, Integration Time = 9.6 μs, Sampling Interval = 4 ns

Amplifier Transfer Function = \( \frac{K[s]}{1 + \left( \frac{S}{\omega_1} \right) \left( 1 + \frac{S}{\omega_2} \right) \left( 1 + \frac{S}{\omega_3} \right)} \)

<table>
<thead>
<tr>
<th>Filter Frequencies (MHz)</th>
<th>Predicted System Poles</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_1 = 0.0001 )</td>
<td>0.011597292</td>
<td>0.4</td>
<td>3.0406266 x 10^5</td>
<td>8.33</td>
<td>0.78 x 10^{-4}</td>
</tr>
<tr>
<td>( \omega_2 = 0.001 )</td>
<td>10.340356</td>
<td>-2.6</td>
<td>-2.6666951 x 10^8</td>
<td>-2.56</td>
<td></td>
</tr>
<tr>
<td>( \omega_3 = 400 )</td>
<td>0.011554641</td>
<td>0.03</td>
<td>2.831267 x 10^5</td>
<td>0.867</td>
<td></td>
</tr>
<tr>
<td>( \omega_1 = 0.00001 )</td>
<td>10.344142</td>
<td>-2.57</td>
<td>-2.667433 x 10^8</td>
<td>-2.54</td>
<td></td>
</tr>
<tr>
<td>( \omega_2 = 0.0001 )</td>
<td>0.011561775</td>
<td>0.093</td>
<td>2.8105734 x 10^5</td>
<td>0.13</td>
<td></td>
</tr>
<tr>
<td>( \omega_3 = 400 )</td>
<td>10.341452</td>
<td>-2.59</td>
<td>-2.6667401 x 10^8</td>
<td>-2.56</td>
<td></td>
</tr>
<tr>
<td>( \omega_1 = 0.000001 )</td>
<td>0.011558284</td>
<td>0.063</td>
<td>2.8080413 x 10^5</td>
<td>0.04</td>
<td>0.436 x 10^{-4}</td>
</tr>
<tr>
<td>( \omega_2 = 0.0001 )</td>
<td>10.345566</td>
<td>-2.56</td>
<td>-2.6677372 x 10^8</td>
<td>-2.52</td>
<td></td>
</tr>
<tr>
<td>( \omega_3 = 400 )</td>
<td>0.011589247</td>
<td>0.33</td>
<td>3.0396171 x 10^5</td>
<td>8.29</td>
<td></td>
</tr>
<tr>
<td>( \omega_1 = 0.00001 )</td>
<td>10.554968</td>
<td>-0.584</td>
<td>-2.7213314 x 10^8</td>
<td>-0.567</td>
<td>0.38 x 10^{-4}</td>
</tr>
<tr>
<td>( \omega_2 = 0.0001 )</td>
<td>0.011548494</td>
<td>-0.0217</td>
<td>2.8305334 x 10^5</td>
<td>0.841</td>
<td>0.26 x 10^{-5}</td>
</tr>
<tr>
<td>( \omega_3 = 2000 )</td>
<td>10.553439</td>
<td>-0.598</td>
<td>-2.7207385 x 10^8</td>
<td>-0.588</td>
<td></td>
</tr>
<tr>
<td>( \omega_1 = 0.00001 )</td>
<td>0.011555324</td>
<td>0.0375</td>
<td>2.8098128 x 10^5</td>
<td>0.103</td>
<td>0.234 x 10^{-5}</td>
</tr>
<tr>
<td>( \omega_2 = 0.0001 )</td>
<td>10.55293</td>
<td>-0.603</td>
<td>-2.7206022 x 10^8</td>
<td>-0.593</td>
<td></td>
</tr>
<tr>
<td>( \omega_3 = 2000 )</td>
<td>0.011555295</td>
<td>0.0138</td>
<td>2.8073657 x 10^5</td>
<td>0.0159</td>
<td>0.215 x 10^{-5}</td>
</tr>
<tr>
<td>( \omega_1 = 0.00001 )</td>
<td>10.5555751</td>
<td>-0.577</td>
<td>-2.7212768 x 10^8</td>
<td>-0.569</td>
<td></td>
</tr>
<tr>
<td>( \omega_2 = 0.0001 )</td>
<td>0.011591676</td>
<td>0.352</td>
<td>3.0398925 x 10^5</td>
<td>8.3</td>
<td></td>
</tr>
<tr>
<td>( \omega_3 = 10000 )</td>
<td>10.589241</td>
<td>-0.261</td>
<td>-2.7300537 x 10^8</td>
<td>0.248</td>
<td>0.372 x 10^{-4}</td>
</tr>
<tr>
<td>( \omega_1 = 0.00001 )</td>
<td>0.011548645</td>
<td>0.02</td>
<td>2.8305346 x 10^5</td>
<td>0.841</td>
<td>0.659 x 10^{-6}</td>
</tr>
<tr>
<td>( \omega_2 = 0.0001 )</td>
<td>10.59398</td>
<td>-0.217</td>
<td>-2.7310357 x 10^8</td>
<td>0.21</td>
<td></td>
</tr>
<tr>
<td>( \omega_3 = 10000 )</td>
<td>0.011555811</td>
<td>0.065</td>
<td>2.8101477 x 10^5</td>
<td>0.115</td>
<td></td>
</tr>
<tr>
<td>( \omega_1 = 0.00001 )</td>
<td>10.587531</td>
<td>-0.277</td>
<td>-2.7294168 x 10^8</td>
<td>-0.271</td>
<td>0.49 x 10^{-6}</td>
</tr>
<tr>
<td>( \omega_2 = 0.00001 )</td>
<td>0.011553427</td>
<td>0.021</td>
<td>2.8074415 x 10^5</td>
<td>0.0186</td>
<td>0.266 x 10^{-6}</td>
</tr>
<tr>
<td>( \omega_3 = 10000 )</td>
<td>10.595411</td>
<td>-0.2</td>
<td>-2.7313569 x 10^8</td>
<td>-0.2</td>
<td></td>
</tr>
<tr>
<td>( \omega_1 = 0 )</td>
<td>0.011545154</td>
<td>0.05</td>
<td>2.8063116 x 10^5</td>
<td>0.02</td>
<td></td>
</tr>
<tr>
<td>( \omega_2 = 0 )</td>
<td>0.011505088</td>
<td>-0.0187</td>
<td>-2.7362615 x 10^7</td>
<td>-0.021</td>
<td>0.411 x 10^{-8}</td>
</tr>
</tbody>
</table>

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This approach requires that the amplifier have a bandwidth approximately 1000 times that of the system under test. This is reasonable for test systems with bandwidths on the order of 10 to 50 kHz. However, this places severe bandwidth requirements on the amplifier for test systems with 1 MHz bandwidth or greater.

In view of these performance requirements for the amplifier, another approach was investigated.

The second approach to alleviating the amplifier problem employed linear system analysis techniques. Consider once again the digital implementation of Figure 6. The input to the A/D converter, in the Laplace domain, is given by

\[ Y_0(s) = H_1(s)H_A(s)U(s) \]  

(73)

From a linear system point of view, this is equivalent to a system with a transfer function, \( H_1(s) \), being excited with an input of \( H_A(s)U(s) \) or as shown in Figure 25.

![Figure 25. Linear System Equivalence Concept](image)

This implies an equivalent technique implementation (for processing only) given by that configuration shown in Figure 26.
This technique implementation was simulated for an amplifier whose transfer function was of the form

\[ H_A(s) = \frac{K}{\left[1 + \left(\frac{s}{\omega_1}\right)\right]\left[1 + \frac{s}{\omega_2}\right]} \]  

(74)

The results of the performance simulation are presented in Tables 19 and 20. Graphs of normalized mean squared error for these results are shown in Figures 27 and 28. These results suggest that best performance of the identification technique is obtained when the upper break frequency of the amplifier is approximately one to two times the upper break frequency of the system under test. The reason for this behavior is that, for the integration period needed to identify the low frequency break point of the system under test, the high frequency components of the system output generated by the high frequency components of the input \([H_A(s)U(s)]\) have a negligible effect on the inner products generated for the Gram determinant. Therefore, the amplifier must have a frequency response essentially matched in bandwidth to the system under test for this approach to yield satisfactory performance.

The results indicate that similar performance is obtained using either approach. Therefore, the approach used in an actual test setup will depend on the characteristics of the system under test.

The above analysis concentrated on the frequency response characteristics of the pre-A/D converter amplifier. These characteristics will have, as shown, a profound effect on the performance of the identification technique. There are, however, many other parameters that must be considered before selecting an amplifier. These include gain, slew rate, input impedance, common mode rejection ratio, and output voltage swing, among others. The specification of these parameters depends on the particular system under test and must be evaluated accordingly.
### Table 19. Identification Technique Performance for Different Amplifier Configurations, Perfect A/D Conversion, Integration Time = 9.6 μs, Sampling Interval = 4 ns

<table>
<thead>
<tr>
<th>Filter Poles (MHz) w1, w2</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>0.011555324</td>
<td>0.0375</td>
<td>2.8024309 x 10^5</td>
<td>-0.16</td>
<td>0.134 x 10^-5</td>
</tr>
<tr>
<td>50</td>
<td>10.592746</td>
<td>-0.23</td>
<td>-2.7282039 x 10^8</td>
<td>-0.316</td>
<td>0.196 x 10^-4</td>
</tr>
<tr>
<td>100</td>
<td>0.011536579</td>
<td>-0.12</td>
<td>2.7832421 x 10^5</td>
<td>-0.84</td>
<td>0.47 x 10^-4</td>
</tr>
<tr>
<td>100</td>
<td>10.561845</td>
<td>-0.519</td>
<td>-2.7120376 x 10^8</td>
<td>-0.906</td>
<td>0.47 x 10^-4</td>
</tr>
<tr>
<td>200</td>
<td>0.011554257</td>
<td>0.028</td>
<td>2.7741538 x 10^5</td>
<td>-1.16</td>
<td>0.909 x 10^-4</td>
</tr>
<tr>
<td>200</td>
<td>10.497776</td>
<td>-1.12</td>
<td>-2.6912371 x 10^8</td>
<td>-1.66</td>
<td>0.909 x 10^-4</td>
</tr>
<tr>
<td>200</td>
<td>0.011551949</td>
<td>-0.164</td>
<td>2.8450411 x 10^5</td>
<td>1.36</td>
<td>0.909 x 10^-4</td>
</tr>
<tr>
<td>400</td>
<td>10.814967</td>
<td>1.86</td>
<td>-2.8077018 x 10^8</td>
<td>2.59</td>
<td>0.909 x 10^-4</td>
</tr>
<tr>
<td>400</td>
<td>0.011543181</td>
<td>-0.0677</td>
<td>2.9494878 x 10^5</td>
<td>5.08</td>
<td>0.962 x 10^-3</td>
</tr>
<tr>
<td>800</td>
<td>11.190547</td>
<td>5.4</td>
<td>-2.9555270 x 10^8</td>
<td>7.99</td>
<td>0.962 x 10^-3</td>
</tr>
<tr>
<td>800</td>
<td>0.011498102</td>
<td>-0.457</td>
<td>2.9802372 x 10^5</td>
<td>6.17</td>
<td>0.153 x 10^-2</td>
</tr>
<tr>
<td>700</td>
<td>11.395104</td>
<td>7.33</td>
<td>-3.0261627 x 10^8</td>
<td>10.6</td>
<td>0.153 x 10^-2</td>
</tr>
<tr>
<td>2000</td>
<td>0.011502276</td>
<td>-0.42</td>
<td>3.0687918 x 10^5</td>
<td>9.32</td>
<td>0.322 x 10^-2</td>
</tr>
<tr>
<td>4000</td>
<td>11.708577</td>
<td>10.28</td>
<td>-3.1528646 x 10^8</td>
<td>15.2</td>
<td>0.322 x 10^-2</td>
</tr>
<tr>
<td>No Filter</td>
<td>0.011545154</td>
<td>-0.05</td>
<td>2.8063116 x 10^5</td>
<td>-0.02</td>
<td>0.411 x 10^-8</td>
</tr>
<tr>
<td>10.615068</td>
<td>-0.0187</td>
<td>-2.7362615 x 10^8</td>
<td>-0.021</td>
<td>0.411 x 10^-8</td>
<td></td>
</tr>
</tbody>
</table>
**TABLE 20. IDENTIFICATION TECHNIQUE PERFORMANCE FOR DIFFERENT AMPLIFIER CONFIGURATIONS, PERFECT A/D CONVERSION, INTEGRATION**

**TIME = 9.6 μs, SAMPLING INTERVAL = 4 ns**

<table>
<thead>
<tr>
<th>Filter Poles (MHz) $\omega_1, \omega_2$</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.011528838</td>
<td>-0.1918</td>
<td>2.8048702 x 10^5</td>
<td>-0.0908</td>
<td>0.597 x 10^-6</td>
</tr>
<tr>
<td>11</td>
<td>10.650187</td>
<td>0.3127</td>
<td>-2.7449821 x 10^8</td>
<td>0.297</td>
<td>0.389 x 10^-6</td>
</tr>
<tr>
<td>11</td>
<td>0.011566252</td>
<td>0.132</td>
<td>2.8083652 x 10^5</td>
<td>0.0515</td>
<td>0.148 x 10^-7</td>
</tr>
<tr>
<td>12</td>
<td>10.590722</td>
<td>-0.247</td>
<td>-2.7302155 x 10^8</td>
<td>-0.242</td>
<td>0.147 x 10^-6</td>
</tr>
<tr>
<td>12</td>
<td>0.011539614</td>
<td>-0.098</td>
<td>2.8054255 x 10^5</td>
<td>-0.0532</td>
<td>0.148 x 10^-7</td>
</tr>
<tr>
<td>13</td>
<td>10.633535</td>
<td>1.559</td>
<td>-2.7407930 x 10^8</td>
<td>0.144</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>0.011560636</td>
<td>0.0834</td>
<td>2.8076305 x 10^5</td>
<td>0.025</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>10.601234</td>
<td>-0.148</td>
<td>-2.7327608 x 10^8</td>
<td>-0.199</td>
<td>0.17 x 10^-5</td>
</tr>
<tr>
<td>14</td>
<td>0.011588840</td>
<td>0.326</td>
<td>2.8015747 x 10^5</td>
<td>0.13</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>10.561955</td>
<td>-0.518</td>
<td>-2.7230306 x 10^8</td>
<td>-0.505</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>0.011540601</td>
<td>-0.09</td>
<td>2.805308 x 10^5</td>
<td>-0.057</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>10.629864</td>
<td>0.119</td>
<td>-2.7397023 x 10^8</td>
<td>0.104</td>
<td>0.91 x 10^-7</td>
</tr>
<tr>
<td>16</td>
<td>0.011559574</td>
<td>0.074</td>
<td>2.8072548 x 10^5</td>
<td>0.0119</td>
<td>0.12 x 10^-6</td>
</tr>
<tr>
<td>17</td>
<td>10.603475</td>
<td>-0.127</td>
<td>-2.7331924 x 10^8</td>
<td>-0.133</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>0.011514039</td>
<td>-0.3199</td>
<td>2.8022400 x 10^5</td>
<td>-0.166</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>10.666838</td>
<td>0.469</td>
<td>-2.7487678 x 10^8</td>
<td>0.435</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>0.011555627</td>
<td>0.04</td>
<td>2.8066038 x 10^5</td>
<td>-0.0112</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>10.606738</td>
<td>-0.965</td>
<td>-2.7338636 x 10^8</td>
<td>-0.1089</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>0.011542878</td>
<td>-0.0703</td>
<td>2.8051016 x 10^5</td>
<td>-0.0647</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>10.621596</td>
<td>0.0434</td>
<td>-2.7374330 x 10^8</td>
<td>0.0215</td>
<td>0.467 x 10^-7</td>
</tr>
<tr>
<td>20</td>
<td>0.011528307</td>
<td>-0.196</td>
<td>2.8033879 x 10^5</td>
<td>-0.126</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>10.640706</td>
<td>0.223</td>
<td>-2.7420633 x 10^8</td>
<td>0.191</td>
<td>0.33 x 10^-6</td>
</tr>
</tbody>
</table>
Figure 27. Identification Technique Performance as a Function of Amplifier Characteristics
Figure 28. Identification as a Function of Amplifier Characteristics
The required gain of the amplifier is a function of the peak output voltage of the nonlinear system under test and the full-scale input voltage of the A/D converter. This gain can be achieved, if necessary, by cascading multiple amplifiers with similar frequency responses. Common mode rejection needs to be considered because of the small signals that will most likely be generated by the nonlinear system under test. Noise will be a critical factor in implementing a viable experimental measurement setup for the technique and the amplifier common mode rejection capability is a measure of how well noise can be eliminated from the amplifier output. The remaining parameters (slew rate, output voltage swing, etc.) must be specified to be compatible with the other devices of the measurement implementation and with the output of the system under test.

A survey of available amplifier characteristics reveals again a multitude of devices and manufacturers. The wide-band operational amplifiers have a gain-bandwidth product which typically lies in the range of 10 to 200 MHz. (Teledyne Philbrick and Burr Brown make operational amplifiers with a gain bandwidth product of 1000 MHz. This was the maximum gain-bandwidth product determined during the survey.) These devices typically have a frequency response which is flat from dc to BW/10, where BW = 3 dB bandwidth.

Several of these devices are recommended by the manufacturer for use as pre-A/D converter amplifiers in an implementation considered here.

The available amplifiers appear to be compatible with the existing A/D converters for application to the identification technique implementation for either of the two approaches described above. The fastest high resolution A/D converter (14 to 16 bits) was on the order of 125 kHz sampling rate. In one approach described above, the required amplifier bandwidth would be 1000 times the upper break frequency of the system under test. This upper break frequency would be less than 125 kHz due to sampling considerations but an amplifier bandwidth of 1000 (125 kHz) = 125 MHz would provide the required frequency response. This bandwidth is achievable with a gain of 8 using the 1000 MHz gain bandwidth product device described above. Cascading several of these devices will provide the required gain. If the sampling requirements are taken into account, the system under test would be limited to 20 kHz which would necessitate a 20-MHz amplifier bandwidth which is achievable with the above device having a gain of 50.

The implementation feasibility of the digital configuration of the identification technique does not appear to be limited by amplifier technology at this point in time. The A/D converter remains the critical component in the digital
implementation and its characteristics will determine the overall feasibility of implementing the identification technique.

The amplifier survey was based on amplifier specification data supplied by the following manufacturers:

- Plessey Semiconductors
- Analog Devices
- Harris Semiconductor Products Division
- Fairchild Semiconductor
- National Semiconductor
- Amplifier Research
- M.S. Kennedy Corp.
- Teledyne Philbrick
- RCA
- Precision Monolithics
- Datel Systems, Inc.
- Burr Brown Research Corp.

3. Signal Generator Requirements

The identification technique requires that an input function of the form

\[ x(t) = \sum_{i=1}^{N} e^{-at} u(t) \]  \hspace{1cm} (75)

be used to excite the system for identification of \( h_2(t_1, t_2) \). The identification of \( h_1(t) \) may use an arbitrary waveform (Reference 4) but it would be convenient if the same waveform generator could be used for identification of \( h_1(t) \) and \( h_2(t_1, t_2) \).

The input, which consists of a sum of decaying exponentials or even a single decaying exponential, is not a convenient waveform in terms of commercially available signal generators. The vast majority of waveform/signal generators provide the square wave, sine wave and triangular waveforms with pulse and frequency modulation options. No commercially available waveform generator with a specific exponential function output was found during the survey of waveform generator manufacturing companies.
The only potential signal generator candidate for use in the identification technique was a system manufactured by WAVETEK. This system was the WAVETEK Model 175 Arbitrary Waveform Generator. This device is a programmable waveform generator which permits the user to store waveforms as digital points on a 256 x 255 grid. The data points are stored in four random access memories (RAM) and are entered via a panel keyboard interface.

This signal generator is a very capable device but has some limitations that will affect its use in the identification technique. The output of the signal generator is piece-wise continuous linear between sample points which results in a distorted exponential input. The dynamic range of the device is 20 volts to 2 millivolts. This corresponds to a limitation imposed by a 13 bit A/D converter operating on an analog waveform generator. The output amplitude resolution is 1/256 which restricts the time period over which the exponential input can be used for the identification technique.

For the two-pole example of interest, the input $x(t) = 10^{-3}e^{-10^3t}u(t)$ would be resolved only to a minimum amplitude of $3.9 \times 10^{-6}$ which corresponds to a integration period of approximately $5.5 \times 10^{-7}$ second. Beyond this time period, the input function would be zero.

Although the arbitrary waveform generator provides a level of capability beyond the typical commercially available waveform generator, it does not appear to meet the accuracy requirements of the identification technique.

The conclusion of the survey of commercially available signal/waveform generators is that no signal generator on the present market can generate a sum of decaying exponential functions. This requires that a circuit be designed to provide this input.

There are several options available at this point. The first option is to use the system shown in Figure 29.

![Figure 29. RC Networks](image-url)
The output voltage of this system is

\[ E_0(s) = \frac{1}{s + \frac{1}{RC}} \]  

(76)

or, in the time domain

\[ e_0(t) = e^{-\frac{1}{RC}t} u(t) \]  

(77)

This is the function required -- a decaying exponential. The circuit is driven by a unit step input which is easily generated using standard equipment.

A sum of decaying exponentials can be generated using several of these passive networks in parallel with their outputs summed using an operational amplifier as a summary amplifier. The time constants (1/RC) of each network are set by appropriate selection of R and C. One requirement is that the input impedance of the summing amplifier not load down the passive network and effectively change the time constant.

Another implementation of the signal generator is to use an operational amplifier as shown in Figure 30.

![Figure 30. Operational Amplifier Network for Signal Generator](image-url)
The closed loop transfer function of this amplifier circuit is

\[
G_c(s) = \frac{R_0 + R_1}{R_1} \frac{1}{1 + \frac{2\pi}{f_0 A_0} \left( \frac{R_0 + R_1}{R_1} \right)} = \frac{K}{1 + \frac{s}{\omega'}}
\]

where

\[
K = \frac{(R_0 + R_1)}{R_1}, \quad \omega' = 2\pi f_0 A_0/K
\]

and \( f_0 \) is the high frequency cutoff of the operational amplifier.

The impulse response of this network is

\[
e_0(t) = K \omega' e^{-\omega' t} = 2\pi f_0 A_0 e^{-\omega' t}
\]

A practical impulse is actually a short pulse of width \( \delta \). For this practical impulse, the output of the circuit is

\[
e_0(t) = (K - Ke^{-\omega' t}) u(t) \quad 0 \leq t < \delta
\]

\[
e_0(t) = K (e^{-\omega' t} - 1) e^{-\omega' t} \quad t \geq \delta
\]

This output is shown in Figure 31.
Figure 31. Short Pulse Response of Operational Amplifier Network of Figure 30

The portion of the output of the operational amplifier that represents the exponential input is for \( t > 0 \). Therefore it is necessary to use an analog switch to clamp the operational amplifier from time \( t = 0 \) to \( t = \tau \).

The amplitude of the exponential function generated by the operational amplifier will be controlled by an attenuator connected in series with the operational amplifier circuit. The unattenuated amplitude of the decaying exponential is

\[
K(1 - e^{-\delta \omega t})
\]

\[
K(e^{\delta \omega t}(1-e^{-\omega t}))
\]

\[
K(0.5(1 - e^{-\delta \omega t}))
\]

\[
K(1 - e^{-\omega t})
\]

The time constant is a function of the open-loop gain \( A_0 \) of the operational amplifier, the open-loop 3-dB bandwidth \( f_0 \), and the resistors \( R_1 \) and \( R_0 \). The open loop gain and bandwidth are functions of the operational amplifier selected for use while \( R_1 \) and \( R_0 \) are selectable at the discretion of the user.

A sum of decaying exponential functions can be generated by exciting a parallel set of these operational amplifier networks with the same input pulse and using a summing operational amplifier configuration to add the functions. The analog switch is then used to clamp the output until time \( t = \delta \). A sample configuration for \( N = 2 \) is shown in Figure 32.

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The output is the negative sum of the input exponential functions. This can be reinverted using another inverting operational amplifier. Proper selection of $R_A$, $R_B$, and $R_C$ will serve to properly attenuate the amplitude of each exponential function prior to summing. The output of this system is

$$c_0(t) = -\left( \frac{R_c}{R_A} \left( \frac{R_{01} + R_{11}}{R_0} \right) \right) \frac{\delta \omega_{01}' t}{e^{\omega_{01}' t} - 1} e^{-\omega_{01}' t}$$

$$+ \left( \frac{R_c}{R_B} \frac{R_{02} + R_{12}}{R_{02}} \right) \frac{\delta \omega_{02}' t}{e^{\omega_{02}' t} - 1} e^{-\omega_{02}' t}$$

where

$$\omega_{0i}' = \frac{2\pi f_0 A_{0i}}{\left( \frac{R_{0i}}{R_{0i}} + \frac{R_{1i}}{R_{0i}} \right)}, \quad i = 1, 2.$$
4. Data Storage Requirements

The data storage requirements for the digital implementation are a function of the number of A/D converter bits and the number of samples required for the input and output. The number of digital bits requiring storage for the digital implementation is given by

\[ \text{Data Bits} = 2 \left( \frac{T}{T_s} \right) \cdot M \]  \hspace{1cm} (83)

where

- \( T \) is the integration period
- \( T_s \) is the sampling interval
- \( M \) is the number of A/D converter bits

The integration period and sampling interval are a function of the system under test and it is difficult to establish a fixed number for these values. For the example systems, the maximum number of samples used was 3200. This was limited by the memory capacity of the GP computer used for the simulation. For this case the number of data bits to be stored for a 16 bit A/D converter is

\[ \text{Data Bits} = 2(3200)(16) = 102,400 \text{ bits} \]

An upper limit of 8000 samples seems to be reasonable for systems to which the technique can be applied with existing components. This requires a storage capacity of

\[ \text{Data Bits} = 2(8000)(16) = 256,000 \text{ bits} \]

The data bits can be stored using static RAM. RAM's with a 2048 word x 8 bits organization are currently available. Two of these are required to store 2048 words of 16 bit length. To store 16,000 words of 16 bit length requires 16 of these RAM chips. These devices have a typical access time of 200 ns, which is an indication of the time required to write an 8-bit word into memory. This is easily compatible with the fastest 16-bit A/D converter presently available (conversion time = 8 \( \mu s \)).

Although establishing a maximum level of data storage required is difficult, it appears that memory devices are available to handle the data storage for any practical implementation of the identification technique. As the number of samples increases and as data storage requirements increase,
it will, of course, be necessary to build a larger memory by adding chips and any necessary interface circuitry at additional cost. However, the capability is available if needed, and the data storage requirements do not appear to be technology limited at this time. The only limitation of these devices could be in the area of the access time. However, these devices are one to two orders of magnitude faster than the currently available A/D converters. This trend will probably be maintained as both memory technology and A/D converter technology advance.

Once the data is stored in the static RAM, it is necessary to transmit this data to the appropriate storage device for future non-real time processing using the GP computer. This storage device may be a time sharing data file, magnetic tape, paper tape, or punched data cards. Data transmission is most easily accomplished using a device such as a USART (Universal Synchronous/Asynchronous Receiver/Transmitter, Intel 8251A). This device is a programmable communication interface capable of transmitting the data from the RAM to the permanent storage device.

5. Digital Implementation - Conclusions

The performance evaluation of the digital implementation of the identification technique suggests that the critical components of the digital implementation are the A/D converter and the pre-A/D converter amplifier. The important conclusions impacting parameter specification of these devices are summarized below.

a. A/D Converter

(1) The A/D converter must have 14-16 bits of resolution for adequate performance with a two-pole system. This increases to 20 to 24 bits as the number of poles increases to four. Since the highest resolution commercially available A/D has 16 bits of resolution at this point in time, any experimental validation of this implementation should be restricted to systems with two poles or fewer.

(2) The sampling rate requirements for the A/D converter are driven by the accuracy requirements of the processing technique. For a two-pole system, the sampling rate should be 4 to 10 times slower than the highest break frequency of the system under test. The fastest 16 bit A/D converter currently available is limited to a sampling
rate of 125 kHz. This implies that the system under test must be limited to an upper break frequency of approximately 10 to 30 kHz.

b. Amplifier

(1) Three approaches to the identification problem are designed to handle the complication of using a pre-A/D converter amplifier. The first approach is to use the identification technique directly and identify a transfer function that is the product of the transfer functions of the system under test and the amplifier. This increases the dimension of the identification problem, which will probably degrade performance of the identification technique. This approach requires an amplifier that is approximately equal in frequency extent to the system under test.

The second approach is to use a very wide-band (compared to system under test) amplifier. The lower 3-dB break frequency of the amplifier should be 1/1000 of the lower break frequency of the test system. The upper 3-dB break frequency of the amplifier should be 1000 times the upper break frequency of the test system.

The final approach is to use linear system theory to modify the required identification processing. This requires that the amplifier be approximately matched in frequency extent to the system under test.

(2) Operational amplifiers with gain-bandwidth products up to 1000 MHz are presently commercially available. These will work well with all the processing approaches described in (1) above.

(3) The amplifier gain requirement is determined by the peak output voltage of the system under test and the full-scale input voltage of the A/D converter.
c. Remaining Components

The remaining components of the digital implementation did not appear to be technology limited in terms of enabling implementation of the identification technique. The important conclusions are given below.

(1) There is no commercially available waveform generator with an exponential function capability. The appropriate inputs will be generated by using operational amplifiers as low-pass filters and appropriately damping the short pulse response to obtain the exponential function.

(2) Data storage is accomplished using static random access memory (RAM) chips and a programmable interface to transmit the data to the digital computer for nonreal-time processing.

d. Summary

The analysis of the digital implementation supports the following important conclusion. The pencil-of-functions technique requires high accuracy to perform identification satisfactorily. This accuracy is impacted by the choice of the numerical integration technique used in the processing. Simpson's rule of numerical integration results in increased error as the number of system poles increases. There is a need to determine the best integration technique for the identification processing. This issue will be dealt with in more detail during Part II of the study.

Given the constraints presented above, the digital implementation of the identification technique can feasibly be constructed and used in an experimental test setup.

A remaining issue is the problem of noise in the implementation. A 16-bit A/D converter with a 10 volt full-scale input can resolve a signal of 152 microvolts. These low level signals require careful handling to reduce the impact of noise on the performance of the technique. The devices used in the implementation must be extremely low noise components and advantage must be taken of any common mode rejection capability available in the measurement configuration.

C. HYBRID IMPLEMENTATION

During the investigation of the digital implementation, it became apparent that the numerical integration of the A/D con-
verted samples was a primary source of performance degradation. A hybrid implementation of the identification technique was pos-
tuted to possibly alleviate this performance degradation. This implementation is shown in Figure 33. The input and output
of the test system are integrated N times using analog inte-
grators. The integrator outputs are appropriately amplified and
sampled by a set of A/D converters. These samples are then
stored for further nonreal-time pencil-of-functions processing
on the GP computer.

The potential advantages of this configuration are that it
will minimize the error in the integrated outputs by eliminating
the need for numerical integration of the outputs. (The inner
products will still be formed using numerical integration of the
products of the A/D converted samples.) In addition, this imple-
mentation eliminates the "shrinking number of samples" problem
encountered using Simpson's rule as discussed in Section II.B. However, this implementation has several disadvantages when com-
pared to the digital implementation of paragraph III.B. These
are apparent from Figure 33 where it is observed that 2N + 1 A/D
converters are required for implementation as well as 2N + 1
analog integrators and 2N + 1 amplifiers. The digital implemen-
tation required only two A/D converters and two amplifiers. For
a complex system (N large), this implementation could become
complex and costly compared to the digital system. Another
disadvantage lies in the fact that N must be known before the
final implementation configuration is established. This
complicates the procedure of evaluating N since the measurement
setup must be changed for each iteration of the procedure to
evaluate system order. It is recommended that the system order
be established using the digital approach if possible and that
the hybrid implementation be used only for pole and residue
determination if its performance warrants its use. The
performance of the implementation is addressed in the following
sections.

1. Simulation of Hybrid Implementation

The simulation of the identification technique was
modified to represent the hybrid implementation. The numerical
integration process was deleted and the analytical expressions
for the integrated outputs and inputs were inserted into the
program. A listing of the simulation for this implementation is
provided in Appendix B.

The general form of the output of the system under test
is

$$y(t) = \sum_{i=1}^{N} c_i e^{\lambda_i t}$$

(84)
Figure 33. Hybrid Implementation
The resulting integrations yield

\[
\bar{y}_2(t) = \int_0^t y(\tau) \, d\tau = \frac{N}{\lambda_1} \sum_{i=1}^N \frac{C_i}{\lambda_1} (e^{\lambda_1 \tau} - 1)
\]

(85)

\[
\bar{y}_3(t) = \int_0^t \bar{y}_2(\tau) \, d\tau = \frac{N}{\lambda_1} \sum_{i=1}^N \frac{C_i}{\lambda_1} (e^{\lambda_1 \tau} - 1) - \frac{C_i}{\lambda_1} t
\]

(86)

\[
\bar{y}_4(t) = \int_0^t \bar{y}_3(\tau) \, d\tau = \frac{N}{\lambda_1^2} \sum_{i=1}^N \frac{C_i}{\lambda_1^2} (e^{\lambda_1 \tau} - 1) - \frac{C_i}{\lambda_1^2} t - \frac{C_i}{2\lambda_1} t^2
\]

(87)

\[
\bar{y}_5(t) = \int_0^t \bar{y}_4(\tau) \, d\tau = \frac{N}{\lambda_1^3} \sum_{i=1}^N \frac{C_i}{\lambda_1^3} (e^{\lambda_1 \tau} - 1) - \frac{C_i}{\lambda_1^3} t - \frac{C_i}{\lambda_1^2} \frac{t^2}{2} - \frac{C_i}{6\lambda_1} t^3
\]

(88)

The general form of the input is

\[x(t) = A_1 e^{A_1 t}\]

(89)

and the resultant integrations are similar in form to those for \(y(t)\) (setting \(N = 1\)).

2. Two-Pole System Analysis and Results

The two pole system investigated in paragraph III.B was used to evaluate the performance of the hybrid implementation. The performance results for this implementation are shown in Table 21 for different A/D converter resolutions. Figure 34 is a plot of normalized mean squared error vs A/D converter resolution. These results indicate that this approach does not
<table>
<thead>
<tr>
<th>Number of A/D Bits</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Square Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>No A/D Converter</td>
<td>0.011554792</td>
<td>0.0328</td>
<td>2.8073336 x 10^5</td>
<td>0.0147</td>
<td>0.356 x 10^-7</td>
</tr>
<tr>
<td></td>
<td>10.60926</td>
<td>-0.0727</td>
<td>-2.7349133 x 10^8</td>
<td>-0.705</td>
<td>0.436 x 10^-4</td>
</tr>
<tr>
<td></td>
<td>0.011620211</td>
<td>0.599</td>
<td>2.8009951 x 10^5</td>
<td>-0.211</td>
<td>0.809 x 10^-3</td>
</tr>
<tr>
<td></td>
<td>10.34654</td>
<td>-2.54</td>
<td>-2.667889 x 10^8</td>
<td>-2.52</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>0.0126683786</td>
<td>9.807</td>
<td>2.8531059 x 10^5</td>
<td>1.64</td>
<td>0.589 x 10^-1</td>
</tr>
<tr>
<td></td>
<td>9.5219201</td>
<td>-10.31</td>
<td>-2.4551532 x 10^8</td>
<td>-10.29</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>0.023587263</td>
<td>104.2</td>
<td>3.9067486 x 10^5</td>
<td>39.18</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4.4864759</td>
<td>-57.7</td>
<td>-1.210728 x 10^8</td>
<td>-55.76</td>
<td></td>
</tr>
</tbody>
</table>

TABLE 21. SIMULATION RESULTS FOR HYBRID IMPLEMENTATION FOR DIFFERENT LEVELS OF A/D CONVERTER RESOLUTION, INTEGRATION TIME = 9.6 µs, SAMPLING INTERVAL = 4 ns
Figure 34. Hybrid Implementation Identification Performance as a Function of A/D Converter Resolution
perform as well as the digital implementation (see Table 3). Acceptable performance is obtained for A/D converters of 14 bits or greater resolution whereas, for the digital implementation, acceptable performance is obtained for A/D converters with resolution of 10 bits or greater.

The apparent reason for the poorer performance of this implementation compared to the digital implementation is that the implementation accuracy of the integrator outputs is greater for the latter than for hybrid implementation. Every sample of the integrated output and input is converted to an N-bit digital representation in the hybrid implementation. In the digital implementation, the integrated output and input are formed by numerically integrating the N-bit samples of the system input and output. The numerical integration is accomplished using the full capability of the GP computer machine accuracy. The samples are accumulated and not rounded to 16 bits as is the case for the hybrid implementation. Therefore, the digital implementation is actually more accurate than the hybrid implementation.

3. Four-Pole System Analysis and Results

Although the performance of the hybrid implementation was not as good as the digital implementation for the two-pole system, its performance for the four-pole system of paragraph III.B.1.c.(2) was investigated. The results of the investigation are presented in Table 22. The performance of the hybrid implementation is significantly better than the digital implementation for a 24-bit A/D converter and an ideal A/D converter. The performance of the hybrid implementation is slightly better than the digital implementation for a 20-bit A/D converter but its performance deteriorates significantly for a 16-bit A/D converter. With 16-bit resolution, the hybrid implementation identifies a pair of complex conjugate poles instead of poles at 0.51 and 0.82 MHz.

The results of Table 22 are useful in another respect. The performance of the hybrid implementation with an ideal A/D converter (machine accuracy) is significantly better than that of the digital implementation. This is highlighted in Table 23. These results indicate the effect of numerical integration on the performance of the pencil-of-functions approach. For systems with \( N > 2 \), the numerical integration using Simpson's rule appears to be a serious limitation to the performance of the technique.
### Table 22. Simulation Results for Hybrid Implementation for Different Levels of A/D Converter Resolution, Four-Pole System, Integration Time = 4.8 μs, Sampling Interval = 1.5 ns

<table>
<thead>
<tr>
<th>Number of A/D Bits</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>No A/D Converter</td>
<td>0.011550994</td>
<td>-0.3 x 10^-4</td>
<td>2.8069668 x 10^5</td>
<td>0.0017</td>
<td>0.775 x 10^-8</td>
</tr>
<tr>
<td></td>
<td>0.5099998</td>
<td>-0.34 x 10^-4</td>
<td>-1.200447 x 10^7</td>
<td>0.037</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8200003</td>
<td>0.53 x 10^-4</td>
<td>1.5111038 x 10^7</td>
<td>0.073</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.49999</td>
<td>0.8 x 10^-5</td>
<td>-1.61031116 x 10^8</td>
<td>0.0193</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.011550716</td>
<td>0.00244</td>
<td>2.8068844 x 10^5</td>
<td>-0.00123</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.5100335</td>
<td>0.00657</td>
<td>-1.200283 x 10^7</td>
<td>0.0236</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8199492</td>
<td></td>
<td>1.510175 x 10^7</td>
<td>0.0116</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.49999</td>
<td></td>
<td>-1.6099426 x 10^8</td>
<td>0.0035</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>0.0116280268</td>
<td>0.006189</td>
<td>2.82697507 x 10^5</td>
<td>0.714</td>
<td>0.245 x 10^-9</td>
</tr>
<tr>
<td></td>
<td>0.511678239</td>
<td>0.329</td>
<td>-1.3764095 x 10^7</td>
<td>14.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.815207</td>
<td></td>
<td>1.900147 x 10^7</td>
<td>25.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.508094</td>
<td>0.140</td>
<td>-1.7141638 x 10^8</td>
<td>6.47</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>0.38824 ±0.28327</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.0226615</td>
<td>36%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7.617245</td>
<td>17.2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 23. Comparison of Hybrid and Digital Implementation Performance for Four-Pole System, Integration Time = 4.8 μs, Sampling Interval = 1.5 ns

<table>
<thead>
<tr>
<th>Implementation</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid</td>
<td>0.011550994</td>
<td>-0.3 x 10^-4</td>
<td>2.8069668 x 10^5</td>
<td>0.0017</td>
<td>0.775 x 10^-8</td>
</tr>
<tr>
<td></td>
<td>0.5099998</td>
<td>-0.34 x 10^-4</td>
<td>-1.200447 x 10^7</td>
<td>0.037</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8200003</td>
<td>0.53 x 10^-4</td>
<td>1.5111038 x 10^7</td>
<td>0.073</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.499999</td>
<td>0.8 x 10^-5</td>
<td>-1.61031116 x 10^8</td>
<td>0.0193</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.011278618</td>
<td>-2.35</td>
<td>2.789548 x 10^5</td>
<td>-0.619</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.4988702</td>
<td>-2.18</td>
<td>-1.048074 x 10^7</td>
<td>-12.66</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8540037</td>
<td>4.14</td>
<td>1.3593498 x 10^7</td>
<td>10.36</td>
<td>0.103 x 10^-4</td>
</tr>
<tr>
<td></td>
<td>6.463757</td>
<td>-0.711</td>
<td>-1.594465 x 10^8</td>
<td>-0.984</td>
<td></td>
</tr>
</tbody>
</table>
4. Amplifier, Signal Generator, and Data Storage Requirements

The signal generator and amplifier requirements for the hybrid implementation are essentially the same as those detailed for the digital implementation. The amplifiers in the hybrid implementation will have different gains to match the integrator outputs to the appropriate A/D converter full-scale input voltage but the frequency characteristics required are the same as those required for the digital implementation.

The data storage requirements are more complicated for the hybrid implementation because there are $2N + 1$ data streams to be recorded and stored in memory. This implies that a larger number of memory chips is required; however, there is no inherent technology limitation in meeting the data storage requirements. The cost of the data storage system will be approximately $(N + 1)/2$ times that required for the digital implementation.

5. Conclusions - Hybrid Implementation

The resolution requirements for the hybrid implementation are significantly greater than for the digital implementation. Since the hybrid implementation require A/D converters of approximately 24 bits, this implementation is beyond the current state of the art (16 bits). For systems with two poles or fewer, the hybrid implementation offers no advantages over the digital implementation. For systems with more than two poles, the hybrid implementation offers potential performance improvement over the digital approach for an A/D converter with 24 bits. This improvement, however, increases the measurement implementation complexity and cost.

It is not feasible to consider implementation of this approach for an experimental validation at this time because of the A/D converter requirement.

Future improvements in A/D converter technology may permit implementation of this approach at that time. Therefore, the approach cannot be dropped from total consideration at this time but should be relegated to a low priority position until the A/D converters become available.

D. ANALOG IMPLEMENTATION

The analog implementation for the identification technique is shown in Figure 35 for $N = 2$. 

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Figure 35. Analog Implementation

The block labeled "inner product" in Figure 35 performs the operation shown in Figure 36.

\[ g(t) = \langle a(t), b(t) \rangle = \int_0^1 a(\tau) b(\tau) d\tau \]

Figure 36. Inner Product Device Model

The analog implementation forms the inner products for the Gram matrix of the pencil-of-functions approach using analog devices. Analog integrators are used to obtain the integrated input and output functions, and inner product devices that multiply the two inputs and integrate the product are used to form the Gram matrix entries. The output of each inner product
device is sampled using A/D converters and stored for further processing on a general purpose computer.

1. Digital Simulation – Analog Implementation

The simulation of the identification technique was modified to represent the analog implementation. The numerical integration for the inner products was removed and replaced by the analytical functions for the inner products. The various integrated inputs, outputs, and inner products for \( N = 2 \) are listed in the FORTRAN computer program listing in Appendix C.

2. A/D Converter Requirements

The A/D converter requirements for the analog implementation are considered in this paragraph. Only one sample of the output of each inner product device is necessary for pencil-of-functions processing. Therefore, the conversion time requirements for the A/D converters in this implementation are considerably different from those of the digital implementation. If the output of each inner product device is sampled and held at the end of the integration period, then the A/D converters can take as long as necessary to convert the input. This is significant because, as was observed in paragraph III.B.1.g, generally the higher the resolution of the A/D converter, the slower the conversion time. Also, because only a single sample per inner product device is required, it is feasible to think of using a single A/D converter to convert all inner product outputs via multiplexing circuitry.

The resolution requirements for the A/D converters are discussed in the following section.

a. Two-Pole System Analysis and Results

The performance of the analog implementation was evaluated for the two-pole system of paragraph III.B.1.c.(1). The assumed impulse response of the system is

\[
\begin{align*}
  h(t) &= 2.8069192 \times 10^5 e^{-0.011550998 \cdot (2 \pi \times 10^6)t} \\
  &\quad - 2.7368441 \times 10^8 e^{-10.616986 \cdot (2 \pi \times 10^6)t}, \quad t > 0
\end{align*}
\]

For the initial performance evaluation, the analog integrators and inner product devices were assumed perfect. The inner
product device outputs were sampled with A/D converters whose most significant bit magnitude was established on the basis of the peak value of each inner product device. The performance results for different levels of A/D converter resolution are presented in Table 24. These results indicate that 18-20 bit resolution is required for satisfactory performance. This is beyond the current state of the art in A/D converters and restricts the feasibility of this implementation in the present time frame. In general, the performance of the analog implementation is significantly less than that of the digital implementation. Once again, the reason for this appears to be the fact that the digital implementation forms the inner products by accumulating products of N-bit numbers using full machine accuracy. Consequently, the resolution of the inner product is greater than that obtained using the analog implementation which uses a N-bit representation of the final inner product value.

b. Integrator and Inner Product Device Requirements

The A/D converter requirements were determined in section a. above, assuming perfect integrator and inner product devices. This is impossible to achieve in a practical system. This paragraph evaluates accuracy requirements for the integrators and inner product devices.

Each entry of the Gram matrix will be in error prior to A/D conversion. These error will arise from the imperfections of the integrator and the inner product device, and these will be a function of the devices and the inputs to the devices. In order to evaluate the tolerable magnitude of these errors using the computer simulation, they were assumed to be uniformly distributed between ±K percent where K is an input to the simulation. Each inner product is evaluated using the exact expression in the simulation and is then multiplied by \((1 + 100 \cdot X)\) where X is uniformly distributed between ±K percent and is selected independently for each inner product.

The performance results using this error model are provided in Table 25. These results assume a perfect A/D converter (machine accuracy). The results of Table 25 indicate that an inner product total error of less than \(10^{-3}\) percent must be maintained to achieve satisfactory performance.

The performance of the analog implementation was also evaluated taking into account the effects of the A/D converter resolution. These results are provided in Tables 26 through 29 for A/D converters of 24, 20, 18 and 16 bits, respectively. Figure 37 is a plot of normalized mean squared error as a function of inner product error. These results support the conclusion that the total inner product error must
<table>
<thead>
<tr>
<th>No. of A/D Converters</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>No A/D Converter</td>
<td>0.01155099799</td>
<td>-0.71 x 10^-7</td>
<td>2.80691908 x 10^5</td>
<td>2.87 x 10^-5</td>
<td>0.545 x 10^-18</td>
</tr>
<tr>
<td>10</td>
<td>0.01154828177</td>
<td>-0.023</td>
<td>-2.7368410828 x 10^8</td>
<td>3.03 x 10^-5</td>
<td>0.154 x 10^-7</td>
</tr>
<tr>
<td>24</td>
<td>0.01153782195</td>
<td>0.0361</td>
<td>2.80271658 x 10^5</td>
<td>-0.025</td>
<td>0.37 x 10^-6</td>
</tr>
<tr>
<td>22</td>
<td>0.01149365755</td>
<td>-0.114</td>
<td>-2.7403180907 x 10^8</td>
<td>-0.149</td>
<td>0.705 x 10^-5</td>
</tr>
<tr>
<td>20</td>
<td>0.01149365755</td>
<td>-0.496</td>
<td>2.788648036 x 10^5</td>
<td>-0.651</td>
<td>0.117 x 10^-3</td>
</tr>
<tr>
<td>18</td>
<td>0.011319341</td>
<td>-2.0</td>
<td>2.73339299 x 10^5</td>
<td>-2.62</td>
<td>0.217 x 10^-2</td>
</tr>
<tr>
<td>16</td>
<td>0.010570331</td>
<td>3.33</td>
<td>2.50092183 x 10^5</td>
<td>-1.9</td>
<td>0.92 x 10^-1</td>
</tr>
<tr>
<td>14</td>
<td>12.3080966</td>
<td>-8.49</td>
<td>-3.045420229 x 10^8</td>
<td>11.27</td>
<td>0.10003</td>
</tr>
<tr>
<td>12</td>
<td>5.8839899</td>
<td>-44.6</td>
<td>-2.017712 x 10^8</td>
<td>-26.2</td>
<td>0.001</td>
</tr>
</tbody>
</table>
TABLE 25. SIMULATION RESULTS FOR ANALOG IMPLEMENTATION FOR DIFFERENT LEVELS OF INNER PRODUCT ERROR, INTEGRATION TIME = 9.6 μS, PERFECT A/D CONVERTER

<table>
<thead>
<tr>
<th>Inner Product Error (%)</th>
<th>Predicted System Poles (MHz)</th>
<th>Percentage Error</th>
<th>Predicted System Residues</th>
<th>Percentage Error</th>
<th>Normalized Mean Squared Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.01550998, 10.61698603</td>
<td>-7.1 x 10^{-6}</td>
<td>2.806919208 x 10^5</td>
<td>2.8 x 10^{-5}</td>
<td>0.545 x 10^{-18}</td>
</tr>
<tr>
<td>10^{-5}</td>
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<tr>
<td>Inner Product Error (%)</td>
<td>Predicted System Pole (MHz)</td>
<td>Predicted System Residue</td>
<td>Percentage Error</td>
<td>Normalized Mean Squared Error</td>
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</tr>
<tr>
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<tr>
<td>Inner Product Error (%)</td>
<td>Predicted System Poles (MHz)</td>
<td>Percentage Error</td>
<td>Predicted System Residues</td>
<td>Percentage Error</td>
<td>Normalized Mean Squared Error</td>
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<tr>
<td>Inner Product Error (%)</td>
<td>Predicted System Poles (MHz)</td>
<td>Percentage Error</td>
<td>Predicted System Residues</td>
<td>Percentage Error</td>
<td>Normalized Mean Squared Error</td>
</tr>
<tr>
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<tr>
<td>Inner Product Error (%)</td>
<td>Predicted System Poles (MHz)</td>
<td>Percentage Error</td>
<td>Predicted System Residues</td>
<td>Percentage Error</td>
<td>Normalized Mean Squared Error</td>
</tr>
<tr>
<td>-------------------------</td>
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<td>------------------</td>
<td>----------------------------</td>
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<td>-----------------------------</td>
</tr>
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<td>-72.8</td>
<td>-8.98437394 x 10^8</td>
<td>-67.2</td>
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</tr>
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</table>
Figure 37. Identification Technique Performance as a Function of Inner Product Error—Analog Implementation
be less than $10^{-3}$ percent to achieve satisfactory performance for A/D converters of 18 bits or greater resolution. The analog implementation does not achieve satisfactory performance with less than an 18 bit A/D converter.

The problem now is to assess the sources of error in the analog implementation and determine the requirements for each device to meet the total system error requirement. The sources of error in the analog implementation are: (1) the integrator and (2) the inner product device.

The integrator affects the total error in two ways. First, the inputs to some of the inner product devices are the outputs of integrators. Second, the inner product device integrates the product of the two functions input to it. The error introduced by the integrator is examined below.

(1) Integrator Error

The transfer function of a true integrator ($H_{TI}(s)$) is given by

$$H_{TI}(s) = \frac{1}{s}$$  \hspace{1cm} (91)

A practical integrator has a transfer function of the form

$$H_{PI}(s) \approx \frac{1}{s + \gamma}$$  \hspace{1cm} (92)

A practical way of implementing an integrator is to use an operational amplifier as shown in Figure 38.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{practical_integrator.pdf}
\caption{Practical Integrator}
\end{figure}

The transfer function of this implementation is given by (Reference 8)
\[ H_0(s) = A_v \frac{(2\pi f_1)}{RC} \frac{1}{|s + \left(\frac{1}{RCA_v}\right)| \left| s + A_v (2\pi f_1) \right|} \]  

(93)

where

- \( f_1 \) is the high frequency pole of the operational amplifier
- \( A_v \) is the low frequency gain of the operational amplifier

Typically, \( f_1 \) is very high (50 to 100 MHz) and \( A_v \) is 10^4 to 10^8. Therefore the pole at \( S = -2\pi f_1 A_v \) is on the order of 5 \times 10^{11} \text{ Hz}. This means that, for systems in the range of 10 to 50 MHz, this pole can effectively be ignored. Then

\[ H_0(s) = H_{pl}(s) = \frac{K}{s + \frac{1}{RC A_v}} \]  

(94)

where

\[ \gamma = \frac{1}{RC A_v} \]

and

\[ K = \frac{2\pi f_1 A_v}{RC} \]

Now we examine the difference in performance between an ideal and practical integrator. The output of an ideal integrator is given by

\[ y_0(t) = \int_0^t x(\tau) \, d\tau = x(t) * u(t) \]  

(95)

where \( x(t) \) is the input function and \( u(t) \) is the unit step function. The output of the ideal integrator is the convolution
of the input and a unit step function. Similarly, the double integral of $x(t)$ is given by

$$\int_0^t \int_0^t x(\beta) \, d\tau \, d\beta = x(t) \ast (t \, u(t)) \quad (96)$$

or the input convolved with a ramp function.

The outputs of a practical integrator are listed below

- **Single Integration**
  - $x(t) \ast e^{-\gamma T} u(t)$

- **Double Integration**
  - $x(t) \ast te^{-\gamma T} u(t)$

For a single integration, the error in the integration is a function of the value of $e^{-\gamma T}$, where $T$ is the integration period. This is a measure of the "droop" of the integrator over the integration period. This concept of "droop" also extends to the double integration. The key to reducing the error of a practical integrator is to maintain the product $\gamma T$ as close to zero as possible. For $\gamma T = 1 \times 10^{-13}$, the maximum difference between the true integrator impulse response and that of a practical integrator is given in Table 30 for $T = 9.6 \mu s$.

**TABLE 30. PRACTICAL INTEGRATOR ERROR**

<table>
<thead>
<tr>
<th>Integration</th>
<th>Maximum Error Magnitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>$0.6 \times 10^{-11}$</td>
</tr>
<tr>
<td>Double</td>
<td>$0.58 \times 10^{-10}$</td>
</tr>
</tbody>
</table>

For the two-pole system of interest, the integrator output levels are of the magnitudes listed in Table 31.

**TABLE 31. INTEGRATED OUTPUT PEAK VALUES - TWO-POLE SYSTEM**

<table>
<thead>
<tr>
<th>Integrator Output</th>
<th>Peak Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>$0.13 \times 10^{-2}$</td>
</tr>
<tr>
<td>Double</td>
<td>$0.4 \times 10^{-2}$</td>
</tr>
</tbody>
</table>
The errors introduced in the integrator outputs are almost negligible, and are on the order of $10^{-15}$ for a single integration and $2 \times 10^{-13}$ for a double integration. The magnitude of these errors will be compared with those of the inner product device to determine which device is the primary contributor to the total system error.

For $\gamma T = 1 \times 10^{-13}$, it is necessary that

$$\gamma = \frac{1 \times 10^{-13}}{9.6 \times 10^{-6}} = 1.04 \times 10^{-8}$$

where

$$\gamma = \frac{1}{RC A V_0}$$

(97)

For a typical operational amplifier in use today, $A V_0$ varies from $10^4$ to $10^{10}$. This requires that $RC$ be in the range of $9.6 \times 10^{-3}$ to $9.6 \times 10^3$. A typical $RC$ selection is $R = 1$ megohm and $C = 1 \mu F$ or $RC = 1$. Achieving $RC = 9600$ requires larger capacitors and larger resistors than are desired. Therefore, an operational amplifier with an $A V_0$ of $10^8$ to $10^{10}$ or higher is recommended for use with $RC$ chosen accordingly.

(2) Inner Product Device

The remaining critical component in the analog implementation is the inner product device. One approach to implementing the inner product device is shown in Figure 39.

![Figure 39. Inner Produce Device](image)

As detailed above, the integrator should not contribute significantly to the error in the inner product. This means that the critical item in the inner product device is the analog multiplier.
The analog multiplier operates conceptually as shown in Figure 40.

\[ E_q = \frac{V_x V_y}{V_o} \]

**Figure 40. Analog Multiplier Model**

\( V_o \) is a dimensional constant of a practical multiplier and is typically equal to 10 volts. There are several sources of error in a typical multiplier, some of which can be reduced or eventually eliminated by using external trimming techniques. A detailed discussion of these reducible errors is not provided in this report. However, the irreducible error in an analog multiplier is generally limited by the nonlinearity of the analog multiplier. The nonlinearity specification represents the peak difference between the multiplier output and the theoretical output. The typical range of nonlinearity errors for analog multipliers is in the range of 0.05 to 2 percent. These are specified in terms of full-scale output, i.e., a multiplier with a 0.1 percent nonlinearity error and a 10 volt full-scale maximum output has a maximum nonlinear error of 0.1 volt. The nonlinearity for each input is usually given in multiplier specifications and the nonlinearity error can be conservatively predicted from (Reference 9):

\[ f(x,y) = |V_x|_x^4|V_y|_y \tag{98} \]

where

- \( f(x,y) \) is the nonlinearity error
- \( |V_x|_x \) is the fractional nonlinearity coefficient for \( x \) input
- \( |V_y|_y \) is the fractional nonlinearity coefficient for \( y \) input
- \( V_x \) is the \( x \) input voltage
- \( V_y \) is the \( y \) input voltage
If $V_x$ and $V_y$ are assumed to have a maximum value of 0.1 volt, the expected product would have a maximum output of $0.1(0.1)/10 = 0.001$ volt.

If the nonlinearity error is to be maintained at less than 0.001 percent, then it is necessary that

$$f(x,y) \leq 0.00001 (V_x V_y) = 0.001 (\varepsilon_x + \varepsilon_y) \leq 10^{-8} \quad (99)$$

or

$$(\varepsilon_x + \varepsilon_y) \leq 10^{-5} \quad (100)$$

For $\varepsilon_x = \varepsilon_y$,

$$\varepsilon_x \leq 0.5 \times 10^{-3} \% \quad (101)$$

A survey of commercially available multiplier devices indicates that the best multiplier accuracy that can be achieved is on the order of 0.05 percent. This device does not have sufficient accuracy to meet the requirements above. If the inputs to the multiplier are amplified to a peak of 10 volts, the product maximum will be 10 volts. The nonlinearity error is to be maintained to

$$f(x,y) \leq 10^{-5} \quad (10) = 10^{-4} \quad (102)$$

This requires that

$$(\varepsilon_x + \varepsilon_y) \leq \frac{10^{-4}}{10} = 10^{-5} \quad (103)$$

so that no advantage is gained by amplifying the signals.

These results imply that the analog implementation is not feasible in the present time frame because of the inaccuracy of the analog multiplier. Multiplier specifications are for the maximum nonlinearity error of the output voltage. They are obtained by setting one input to a constant dc voltage. The other input is varied over the maximum input range and the output voltage measured and compared with the theoretical output. The maximum deviation is then recorded as the nonlinearity error. This complicates the error analysis undertaken in this section because the nonlinearity error specification is a worst case value. In reality, the range of voltages over which the system under test will operate may lie
in a region where the multiplier nonlinearity is much less than the worst case value. This cannot be determined from a multiplier specification sheet; indeed, it is a function of the actual devices to be used in the implementation. A significant amount of device testing would be required before the analog implementation could be considered feasible. The present indications, however, are that the multiplier errors are on the order of 0.05 percent as a minimum. This does not meet the accuracy requirements defined earlier for the inner product.

Another potential drawback for the analog multiplier is the bandwidth limitation. The analog multiplier with the 0.05 percent nonlinearity error is the Analog Devices Model #435K, which has a 3-dB bandwidth of 250 kHz. Wider bandwidth multipliers (1 to 10 MHz) are available at the price of increased nonlinearity error (minimum 0.1 to 0.5 percent).

On the basis of the extrapolation of the amplifier results of I11.c, the upper 3-dB break frequency of the multiplier should be 1000 times the upper break frequency of the system under test. This implies that the system under test will be limited to 250 Hz for the 0.05 percent amplifier described above and to 1 to 10 kHz for the less accurate multipliers.

The analog implementation will also require careful consideration of the propagation time delays incurred in the circuitry. The inputs to the various inner product devices will, in many instances, have been processed by a different number of integrators. Any appreciable propagation delay will result in an error being introduced in the product of the two functions input to the analog multiplier. The results of this section clearly indicate that the error in the inner product calculation must be very small in order to obtain satisfactory performance from the identification technique. Therefore, the time delays must be compensated for as much as possible to reduce the overall inner product error. This may require a significant amount of testing prior to using the identification technique to appropriately synchronize the inputs to each inner product device.

A survey of available analog components did not reveal any analog correlator devices capable of forming the required inner product. This implies that the preferred implementation of the inner product device is the analog multiplier-integrator configuration of Figure 39.

These results support the conclusion that the analog implementation is not a feasible implementation for the identification technique at this time. Technology advancements in analog multiplier devices in the areas of increased accuracy...
and bandwidth are necessary before the identification technique can be implemented using analog devices.

3. Amplifier, Signal Generator and Data Storage Requirements

The analog implementation requires $2N + 1$ amplifiers to adjust the output of the inner product devices to the full-scale input voltage of the A/D converters. The performance requirements for the amplifier are similar to those determined for the digital implementation. The gain of each amplifier must be set dependent on the inner product peak amplitude of the inner product device output and the A/D converter input characteristics.

The signal generator requirements are the same as those determined for the digital implementation.

The data storage requirements are significantly reduced for the analog implementation. The stored data consists of $4N + 1$ numerical values representing the inner product device outputs. This will permit use of smaller and fewer memory chips than are required for the digital implementation. This data storage requirement does not limit the feasibility or applicability of the identification technique as was discussed in detail in paragraph III.B.4.

4. Conclusions - Analog Implementation

The critical components in the analog implementation are the inner product device and the A/D converter. The analysis of the analog implementation has led to the following conclusions.

(1) A minimum of 18 bits of A/D converter resolution is required to achieve minimum identification performance.

(2) The maximum tolerable error in the inner product output is on the order of $10^{-3}$ percent to achieve a minimum level of identification performance for A/D converters with 18 or more bits of resolution.

(3) Performance improvement requires less inner product error (10^{-4} to 10^{-5} percent) and increased A/D converter resolution (20 to 24 bits). However, the performance of the analog implementation is below that demonstrated for the digital implementation.
Currently available analog multipliers have an output error on the order of 0.05 percent which is approximately 50 times greater than the maximum tolerable error of 0.001 percent required for minimum performance of the identification technique.

The analog multiplier and the A/D converter requirements for the analog implementation imply that it is not feasible to consider this implementation for an experimental test setup in the present time frame. Significant technological developments for analog multipliers and A/D converters are necessary before this implementation can prove feasible.
SECTION IV
REFERENCES


APPENDIX A

COMPUTER PROGRAM LISTING FOR THE DIGITAL IMPLEMENTATION OF THE IDENTIFICATION TECHNIQUE

A listing of the computer program for the digital implementation is provided below for the two-pole system of Section III.B.
100 DIMENSION Y1(1,2401)
110 DIMENSION A(4),CP(4),CI(4),AP(4)
120 DIMENSION G(10,10),Y(3,2401),U(3,2401),A(20,10),C(25,25)
130 DIMENSION ISN(10),XLX(10),COEF(10),XLAMR(10),XLAMC(10)
140 DIMENSION RR(10),CR(10),B(25),CRR(10,10),CI(10,10)
150 DIMENSION LIMITI(10),LABEL(25),S(25,1),R(25,1)
160 INTEGER SN,STEP1,STEP2
170C INITIALIZATION AND INPUT PARAMETERS
180 P12=2.*3.14159
190 ERMS=0.
200 W3=10.
210 A(3)=-1.E6*W3
220 AP(3)=A(3)
230 DELT=4.E-3
240 SN=2
250 PRINT:"ORDER OF LINEAR SYSTEM IS",SN
260 PRINT:""
270 SN2=2*SN
280 SK=1.
290 M=2400
300 MORIG=M
310 LIMITI(1)=M+1
320 STEP=SN+1
330 T=DELT*M
340 LL=0
350 XMSBI=1.E-3
360 XMSBO=1.5E-3
370 NBITS=0
380 PRINT:"NUMBER OF BITS IN A/D=" ,NBITS
390 PRINT:""
400 PRINT:"NUMBER OF WAVEFORM SAMPLES=" ,M
410 PRINT:""
420 PRINT:"INTEGRATION TIME IN MICROSECONDS=" ,T
430 PRINT:""
440 PRINT:"INTEGRATION INTERVAL IN MICROSECONDS=" ,DELT
450 PRINT:""
460 R3=1.E-3
470 CP(3)=R3
480 FORMAT(19X,F14.5)
490C EVALUATE INPUT AND OUTPUT FUNCTIONS
500 R1=2.8069192E5
510 R2=-2.7368441E8
520 W1=P12*.011550998
530 A(1)=-1.E6*W1
540 W2=P12*10.616986
550 A(2)=-1.E6*W2
560 CA=R1*R3/((W3-W1)*1.E6)
570 C2=R2*R3/((W3-W2)*1.E6)
C3 = H2*R3/((W2-W3)*1.E6)
C3 = C3 + R3/((W1-W3)*1.E6)
C1(1) = -CA
C1(2) = -C2
C1(3) = -C3
IF(JK = 1, JK = M + 1)

XJK = JK
U(I, JK) = 0.
XT3A = -W3*(XJK-1)*DELT
IF(XT3A.LT.-80.) GO TO 166
U(I, JK) = EXP(-W3*(XJK-1)*DELT)
CONTINUE

U(I, JK) = 1.E-3*SK*U(I, JK)
CALL AT01(U(I, JK),XMSRI,NBITS)
XT1 = CA*EXP(-W1*(XJK-1)*DELT)
XT2 = 0.
XT3 = 0.
XT2A = -W2*(XJK-1)*DELT
XT3A = -W3*(XJK-1)*DELT
IF(XT3A.GT.-H0.) XT3 = C3*EXP(XT3A)
IF(XT2A.GT.-810., XT2 = C2*EXP(XT2A)
Y(I, JK) = XT1 + XT2 + XT3

PRINT:"ACTUAL SYSTEM POLES ARE":,W1/PI2,W2/PI2
PRINT:""
1070  120  LIMIT=M-1
1080      JAT=0
1090  1 LIMIT(JK)=M/2+1
1100  CONST=T/(3.*M)
1110   140  J=0
1120  1 Y(JK,1)=0.
1130   1 LIMIT+2
1140   DO  13  I=3,LIMIT,2
1150      J=J+1
1160   KK=I-J
1170   TERM52=Y(JK-1,I-2)+4.*Y(JK-1,I-1)+Y(JK-1,I)
1180   Y(JK,KK)=Y(JK,KK-1)+CONST*TERM52
1190  13  CONTINUE
1200  1 M=M/2
1210  38  CONTINUE
1220  101  CONTINUE
1230C  EVALUATE INNER PRODUCTS FOR GRAM DETERMINANT
1240  M=M/2
1250  STEPL=SN+1
1260  STEP=2*SN+1
1270   DO  100  K=1,STEP1
1280      LJ=1
1290      M=1
1300   MSL,J=1
1310  220  LIMIT=M-2
1320      JAT=0
1330  CONST=T/(3.*M)
1340  240  CONTINUE
1350C  EVALUATE G(K,K) FOR K=1,SN
1360   (X) 7  I=1,LIMIT(K)-2,2
1370      XI=I
1380   TERM1=2**FLOAT(K-1)*CONST
1390   TERM2=Y(K,I)**2+4.*Y(K,I+1)**2+Y(K,I+2)**2
1400   TERM3=TERM1*TERM12
1410   G(K,K)=G(K,K)*TERM13
1420  7  CONTINUE
1430C  EVALUATE G(K,KM) FOR J .GT. K TO J=SN+1
1440   DO  3  J=2,STEP1
1450      MSL,J=1
1460  IF(K-J) 435,437,436
1470  435  DO  6  I=1,LIMIT(J)-2,2
1480      XTER2=2**FLOAT(J-1)*CONST
1490   TERM22=Y(K,MSL,J)*U(J,I)
1500   HSL,J=MSL,J+2**FLOAT(J-K)
1510   TERM23=4.*Y(K,HSL,J)*U(J,I+1)
1520   KSL,J=MSL,J+2**FLOAT(J-K+1)
1530   TERM24=Y(K,KSL,J)*U(J,I+2)
1540   TERM2=XTER2*(TERM22+TERM23+TERM24)
1550   KM=J+SN
1560   G(K,KM)=G(K,KM)+TERM2
1570   MSL,J=KSL,J
1580 6 CONTINUE
1590 GO TO 3
1600C EVALUATE G(K,KM) FOR K .GT. J TO K=SN+1
1610 436 DO 176 I=1,LIMITI(K)-2,2
1620 XTER2=2**FLOAT(K-1)*CONST
1630 TERM22=Y(K,I)*U(J,MSLJ)
1640 HSLJ=MSLJ+2**FLOAT(K-J)
1650 TERM23=4.*Y(K,I+1)*U(J,HSLJ)
1660 KSLJ=MSLJ+2**FLOAT(K-J+1)
1670 TERM24=Y(K,I+2)*U(J,KSLJ)
1680 TERM2=XTER2*(TERM22+TERM23+TERM24)
1690 KM=J+SN
1700 G(K,KM)=G(K,KM)+TERM2
1710 MSLJ=KSLJ
1720 176 CONTINUE
1730 GO TO 3
1740C EVALUATE G(K,KM) FOR K=J
1750 437 DO 276 I=1,LIMITI(K)-2,2
1760 TERM22=Y(K,I)*U(J,I)
1770 TERM23=4.*Y(K,I+1)*U(J,I+1)
1780 TERM24=Y(K,I+2)*U(J,I+2)
1790 XTER2=2**FLOAT(K-1)*CONST
1800 TERM2=XTER2*(TERM22+TERM23+TERM24)
1810 KM=J+SN
1820 G(K,KM)=G(K,KM)+TERM2
1830 276 CONTINUE
1840 3 CONTINUE
1850 IF(K-STEP1) 236,100,100
1860 100 CONTINUE
1870C EVALUATE G(K,K) FOR K=SN+1 TO 2*SN+1
1880 DO 8 K=SN+2,SN2+1
1890 DO 9 I=1,LIMITI(K-SN)-2,2
1900 DER1=2**FLOAT(K-SN-1)*T/(3*M)
1910 DER2=UJ(K-SN,I)**2+4.*UJ(K-SN,I+1)**2+U(K-SN,I+2)**2
1920 DER3=DER1+DER2
1930 G(K,K)=G(K,K)+DER3
1940 9 CONTINUE
1950 8 CONTINUE
1960 GO TO 425
1970 236 IF(K-SN) 237,237,100
1980C EVALUATE G(K,LK) FOR K .LT. SN, LK=K+1,SN+1
1990 237 DO 401 LK=K+1,SN+1
2000 MMW=LIMITI(LK)-2
2010 LJ=1
2020 DO 402 LI=1,MMW,2
2030 TERM31=Y(K,LJ)*Y(LK,LI)
2040 KH1=LJ+2**FLOAT(LK-K)
2050 TERM32=Y(K,KH1)*Y(LK,LI+1)
2060 KH2=LJ+2**FLOAT(LK-K+1)
2070 TERM33=Y(K,KH2)*Y(LK,LI+2)
2080 TERM34=TERM1*2**FLOAT(K-K)

130
2090   LJ=LJ+2**FLOAT(LK-K+1)
2100   TERM3=TERM34*(TERM31+4.*TERM32+TERM33)
2110   G(K,LK)=G(K,LK)+TERM3
2120   402 CONTINUE
2130   401 CONTINUE
2140   238 IF(K-I) 57,57,58
2150C   EVALUATE G(K+SN,LK+SN) FOR K=2,SN+1, LK=3,SN+1
2160   58 DO 601 LK=K+1,SN+1
2170   MMW=LIMIT1(LK)-2
2180   LJ=1
2190   DO 602 LI=1,MMW,2
2200   TEX1=U(K,LJ)*U(LK,LI)
2210   KLI=LJ+2**FLOAT(LK-K)
2220   TEX2=U(K,KLI)*U(LK,LI+1)
2230   KLI=LJ+2**FLOAT(LK-K+1)
2240   TEX3=U(K,KLI)*U(LK,LI+2)
2250   TEX4=TERM2*2**FLOAT(LK-K)
2260   LJ=LJ+2**FLOAT(LK-K+1)
2270   TEX5=TEX4*(TEX1+4.*TEX2+TEX3)
2280   G(K+SN,LK+SN)=G(K+SN,LK+SN)+TEX5
2290   602 CONTINUE
2300   601 CONTINUE
2310   57 CONTINUE
2320   GO TO 100
2330   425 CONTINUE
2340   PRINT:"UNSCALED ENTRIES IN GRAM DETERMINANT ARE"
2350   PRINT":"  ROW  COLUMN INNER PRODUCT"
2360   PRINT:""  I  J  G(I,J)"
2370   PRINT:""  I  J  G(I,J)"
2380   STEP1=STEP1+SN
2390   DO 942 JIK=I,STEP1
2400   DO 943 KLI=I,STEP1
2410   G(KLI,JIK)=G(JIK,KLI)
2420   PRINT:JIK,KLI,G(JIK,KLI)
2430   943 CONTINUE
2440   942 CONTINUE
2450   MORM=M
2460   N=SN2
2470C   SCALE SCALAR PRODUCTS BY 1.6E FOR COMPUTATION FACILITY
2480   DO 1011 I=1,SN2+1
2490   DO 1021 J=1,SN2+1
2500   G(I,J)=1.66*G(I,J)
2510   1021 CONTINUE
2520   1011 CONTINUE
2530C   EVALUATE DIAGONAL COFACTORS COEF(I)
2540   PRINT:"DIAGONAL COFACTORS ARE AS FOLLOWS"
2550   DO 300 J=1,SN2
2560   DO 310 I=1,SN2
2570   A(J,I)=G(J+1,I+1)
2580   A(I,J)=A(J,I)
2590   310 CONTINUE
2590   300 CONTINUE
2600 300 CONTINUE
2610  ID=I
2620  COEF(I)=DETE(A,N,20)
2630  PRINT:ID,COEF(I)
2640  DO 500  KJ=1,SN
2650  DO 400  J=1,KJ
2660  DO 410  I=1,KJ
2670  A(J,I)=G(J,I)
2680  A(I,J)=G(I,J)
2690  410 CONTINUE
2700  400 CONTINUE
2710  DO 510  J=1,KJ
2720  DO 520  I=KJ+1,SN2
2730  A(J,I)=G(J,I+1)
2740  A(I,J)=A(I,J)
2750  520 CONTINUE
2760  510 CONTINUE
2770  DO 600  J=1,KJ+1,SN2
2780  DO 610  I=KJ+1,SN2
2790  A(J,I)=G(J+1,I+1)
2800  A(I,J)=A(J,I)
2810  610 CONTINUE
2820  600 CONTINUE
2830  COEF(KJ+1)=DETE(A,N,20)
2840  PRINT:KJ+1,COEF(KJ+1)
2850  LNY=KJ+1
2860  500 CONTINUE
2870  PRINT:"EIGENVALUE EQUATION COEFFICIENTS ARE"
2880  N=SN
2890  PRINT:"NUMBER REAL(MHZ) IMAG(MHZ)"
2900  CALL DOWH(R,N,RR,CR)
2910  DO 650  J=1,SN
2920  XIAMR(J)=RR(J)/PI2
2930  XIAMC(J)=CR(J)/PI2
2940  AP(J)=RR(J)*1.E6
2950  PRINT:J,XIAMR(J),XIAMC(J)
2960  XIAMR(J)=RR(J)
2970  650 CONTINUE
2980  640 CONTINUE
2990  630 CONTINUE
3000  CALL DOWH(R,N,RR,CR)
3010  DO 660  K=1,SN+1
3020  IF(XIAMC(J)) 670,660,670
3030  660 CONTINUE
3040  650 CONTINUE
3050  640 CONTINUE
3060  630 CONTINUE
3070  CALL DOWH(R,N,RR,CR)
3080  IF(XIAMC(J)) 670,660,670
3090  660 CONTINUE
3100  650 CONTINUE
3110 IF(FLAG) 680,680,690
3120 690 DO 700 I=1,SN
3130 DO 710 J=1,SN
3140 700 TEMP=1
3150 DO 711 I=1,1
3160 TEMP=TEMP*XLMR(J)
3170 711 CONTINUE
3180 EWE1=0.
3190 EWE2=0.
3200 EWE=1./(TEMP*(XLMR(J)+W3))
3210 EWE1A=XLMR(J)*T
3220 EWE2A=-W3*T
3230 IF(EWE2A.GT.-BO.) EWE2=EXP(EWE2A)
3240 IF(EWE1A.GT.-BO.) EWE1=EXP(EWE1A)
3250 C(I,J)=EWE*(EWE1-EWE2)
3260 C(I,J)=1.E-3*SK*C(I,J)
3270 TEMP=0.
3280 DO 720 K=1,1
3290 TEMP2=1.
3300 DO 721 KK=1,1+1-K
3310 TEMP2=TEMP2*XLMR(J)
3320 721 CONTINUE
3330 TEMP=TEMP+U(K+1,LIMIT(K+1))/TEMP2
3340 720 CONTINUE
3350 C(I,J)=C(I,J)-TEMP
3360 710 CONTINUE
3370 700 CONTINUE
3380 CALL MTINV(C,N,N,25,LABEL)
3390 DO 740 I=2,SN+1
3400 SS(I-1,1)=Y(I,LIMIT(I))
3410 740 CONTINUE
3420 CALL MTMPY(0,C,S,R,SN,SN,1)
3430 PRINT*"RESIDUES OF SYSTEM POLES ARE GIVEN BELOW"
3440 DO 751 I=1,SN
3450 PRINT1,'X(I,1)*1.E6
3460 751 CONTINUE
3470 GO TO 1000
3480 680 CONTINUE
3490 1000 CONTINUE
3491 XI=100.*(R(I,1)*1.E6-R1)/R1
3492 X2=100.*(R(2,1)*1.E6-R2)/R2
3493 PRINT"
3494 PRINT"PERCENTAGE ERROR-RESIDUES",XI,X2
3495 PRINT"
3496 XI=100.*(AP(I)-A1(1))/A1(1)
3497 X2=100.*(AP(2)-A1(2))/A1(2)
3498 PRINT"PERCENTAGE ERROR-POLES",XI,X2
3499 PRINT"
3500 PRINT"
3510 PRINT" JK ACTUAL PREDICTED DIFFERENCE"
3520 SUM=0.
**DETERMINANT EVALUATION**

1. **COMPUTE** the determinant of a matrix using the following algorithm:
   
   ```
   C = (C(i, j) * R(i, j) / R(i, j) * R(i, j) * W1)
   ```
   
   2. **DO** 24 times:
   
   ```
   J = 1, M + 1
   X(J) = J
   X(J) = C(J) * EXP(X(J) * (X(J) - 1)) * DET
   ```
   
   3. **PRINT** X(J), Y(J), DET, DEL, DET
   
   **STOP** 24 times:
   
   ```
   DET = DET / X(J + 1)
   ```
   
   4. **GO** to 1

**END**

---

**NOTE:** The code snippet provided is a segment of a program designed to compute the determinant of a matrix. It involves iterative computations and exponential functions. The specific details of the computation and the context in which this code is used are not provided here.
3930 FUNCTION DETE(A,NARG,IDIM)
3940 DIMENSION A(IDIM,NARG)
3950 I N=NARG
3960 SIGN=1.0
3970 NMNI=N-1
3980 IF(NMINI.EQ.0) GO TO 401
3990 DO 391 J1 = I,NMINI
4000* ***************FIND REMAINING ROW CONTAINING LARGEST***********
4010* ***************ABSOLUTE VALUE IN PIVOTAL COLUMN***************
4020 DO 101 TEMP=0.0
4030 DO 121 J2=J1,N
4040 IF(ABS(A(J2,J1)) .LT. TEMP) GO TO 121
4050 TEMP=ABS(A(J2,J1))
4060 IBIG=J2
4070 121 CONTINUE
4080 IF(TEMP.NE.0.0) GO TO 201
4090* **************PIVOTAL COLUMN CONTAINS ALL ZEROES***********
4100 DETE=0.0
4110 GO TO 5001
4120 201 IF(J1.EQ.IBIG) GO TO 301
4130* ***************INTERCHANGE ROWS AND CHANGE SIGN*************
4140 DO 221 J2=J1,N
4150 TEMP=A(J1,J2)
4160 A(J1,J2)=A(IBIG,J2)
4170 221 A(IBIG,J2)=TEMP
4180* ***************SIGN=-SIGN**********
4190 DO 301 Ni=J1+1
4200* ***************COMPUTE NEW COEFFICIENTS BELOW PIVOTAL ROW*************
4210 301 Ni=J1+1
4220 DO 321 J2=N1,N
4230 TEMP=A(J2,J1)/A(J1,J1)
4240 DO 321 J3=N1,N
4250 321 A(J2,J3)=A(J2,J3)-A(J1,J3)*TEMP
4260 391 CONTINUE
4270* **************ELEMENTS TIMES (-1) ** NO. OF ROW INTERCHANGED***********
4280 401 DETE=1.0
4290 DO 421 J1=1,N
4300 421 DETE=DETE*A(J1,J1)
4310 DETE=DETE*SIGN
4320 5001 RETURN
4330 END
4340* ZORP2
4350* ROUTINES FOR SOLVING POLYNOMIALS
4360 SUBROUTINE POLY(N,A,R,C,PR,PC,RHO,PHI)
4370 DIMENSION A(0000)
4380 IF(RHO)10,5,10
4390 5 R=A(1)
4400 C=0.
4410 PR=A(2)
4420 PC=0.
4430 RETURN
135
4440 10 V1=1.
4450  V2=0.
4460  R=A(I)
4470  C=0.
4480  PR=0.
4490  PC=0.
4500  W1=RHO*COS(Phi)
4510  W2=RHO*SIN(Phi)
4520  NN=N+1
4530  DO 20 I=2,NN
4540  TI=W1*V1-W2*V2
4550  V2=W2*V1+W1*V2
4560  V1=TI
4570  R=R+A(I)*V1
4580  C=C+A(I)*V2
4590  PR=PR+A(I)*(I-1)*V1
4600  20 PC=PC+A(I)*(I-1)*V2
4610  PH=PR/RHO
4620  PC=PC/RHO
4630  RETURN
4640  END

4650  SUBROUTINE ARCTA(X,Y,ANGLE)
4660  PI=3.14159265
4670  IF(X)10,30,20
4680  10 ANGLE=ATAN(Y/X)+PI*SIGN(I,Y)
4690  RETURN
4700  20 ANGLE=ATAN(Y/X)
4710  RETURN
4720  30 IF(Y)40,60,50
4730  40 ANGLE=-PI/2.
4740  RETURN
4750  50 ANGLE=0.
4760  RETURN
4770  60 ANGLE=0.
4780  RETURN
4790  END

4800  SUBROUTINE DmWNI(A,NAR,RR,CR)
4810  DIMENSION A(9999),RR(9999),CR(9999),Q(101),B(3)
4820  CALL EOPT(67,1,1,0)
4830  J=0
4840  N=NAR
4850  NPl=N+1
4860  ANPP=A(NPl)
4870  DO 102 I=1,NPl
4880  IF(A(I))103,102,103
4890  102 CONTINUE
4900  103 C=ABS(A(I)/A(NPl))
4910  10 Ll=120
4920  10 LL=-120
4930  100 IF(C-2,**LL)100,100,101
4940  100 IF(C-2,**LL)101,105,105

136
4950 101 NAR=-NAR
4960  GO TO 5001
4970 105 II=(LJ+LI)/2
4980 109 IF(C-2.*II)110,111,109
4990 109 LL=II
5000  GO TO 111
5010 110 LJ=II
5020 111 IF(JL-LL-1)5001,112,105
5030 112 IB=II/N
5040 114 DO 115 I=1,NPL1
5050 114 II=I-1
5060 115 A(I)=A(I)*2.*II(IR)
5070 120 DO 121 J,I=1,NPL1
5080 121 A(JI)=A(JI)/A(NPL1)
5090 201 IF(N)2001,2001,206
5100 206 IF(A(I))301,211,301
5110 211 J=J+1
5120 211 RH(J)=0.
5130 211 CH(J)=0.
5140 221 J=J+1,N
5150 221 A(JI)=A(JI+1)
5160 230 N=N-1
5170  GO TO 201
5180 201 IF(N-2)601,501,401
5190 401 CALL GRAD(A,N,X,Y)
5200 401 IF(ABS(Y)-ABS(X*1,E-4))431,431,441
5210 431 Y=0.
5220 431 J=J+1
5230 441 RH(J)=X
5240 441 CH(J)=Y
5250 461 IF(Y)461,1021,461
5260 461 J=J+1
5270 461 RH(J)=X
5280 461 CH(J)=-Y
5290  GO TO 1011
5300 1011 DISC=A(2)**2-4.*A(I)
5310 501 DISC=A(2)**2-4.*A(I)
5320 521 Y=SQR(-DISC)/2.
5330 521 X=-A(I)/2.
5340  GO TO 421
5350 421 J=J+1
5360 421 RH(J)=(-A(I)+SQR(DISC))/2.
5370 421 CH(J)=0.
5380  GO TO 1021
5390 1021 J=J+1
5400 601 RH(J)=-A(I)
5410 601 CH(J)=-A(I)
5420  GO TO 2001
5430 1011 RH(J)=-A(I)
5440 1011 RH(J)=-A(I)
5450 1011 RH(J)=-A(I)
B(3)=1.
NB=2
GO TO 1041
1021 B(1)=-RR(J)
B(2)=1.
1041 CALL DIV(A,B,N,NB,Q)
1061 DO 1061 J1=1,N
1061 IF(CR(J1))1081,1071,1081
1071 N=N-1
1081 N=N-2
1090 GO TO 201
2002 DO 2000 I=1,NAR
2000 RR(I)=RR(I)*((2.**IB))
2005 CR(I)=CR(I)*((2.**IB))
2010 DO 2011 I=2,NP1
2011 DO 2021 I=I,NAR
2021 A(I)=Q(I)
2021 IF(NA-NAR)2021,3001,3001
3001 DO 3011 J2=I,IPAR
3011 A(J2)=A(J2)*ANPP
5001 RETURN
END

SUBROUTINE GRAD(A,N,NZ,YZ)
DIMENSION A(9999),X(3),Y(3),RP(3),CP(3),R90(3),PHI(3)
DIMENSION ABS(3),PR(3),PC(3)
PI=3.14159265
MTST=1
101 NZ=0,0
101 YZ=1,0
DZ=2.
RHOZ=1.
PHIZ=PI/2.

CALL POLY(N,A,RZ,CZ,PRZ,PCZ,RHOZ,PHIZ)

SU=SQRT(PRZ**2+PCZ**2)

ABSPZ=SQRT(RZ**2+PCZ**2)

U=2.*ABSPZ*SU

PSI=ATAN(tJ)

TOP=RZ*PCZ-CZ*PRZ

BOT=-(RZ*PRZ+CZ*PCZ)

CALL ARCTA(BOT, TOP, THETA)

COSI=COS(THETA+PHIZ)

SINE=SIN(THETA+PHIZ)

IF(ABSPZ)300,5001,300

IF(SU)301,501,301

IF(RHOZ)321,401,321

IF(ABSPZ/(lIOZ*Si)-1.E-7)5001,5001.701

IF(ABSPZ/(UfHo7*SlJ)-10.**(-MTST))801,R01,40

DZ=DZ/8.0

IM=0

DO 431 I=1,3

DZ=2.*DZ

X(I)=XZ+DZ*COSI

Y(I)=YZ+DZ*SINE

RHO(I)=SQRT(X(I)**2+Y(I)**2)

CALL ARCTA(X(I), Y(I), PHI(I))

CALL POLY(N,A,RP(I),CP(I),PR(I), PC(I),RHO(I),PHI(I))

ABSP(I)=SQRT(RP(I)**2+CP(I)**2)

IF(ABSPZ-ABSP(I)) 431.431,421

IF(ABSPZ-ABSP(I)) 431.431,421

ABSPZ=ABSP(I)

IM=I

CONTINUE

IF(IM) 441,441,461

DZ=DZ/8.

IF(RHOZ)443,445,443

IF(DZ/RHOZ-1.E-7)451,451,401

IF(DZ-1.E-7)451,451,401

IF(SU-ABSPZ) 501,501,5001

DZ=(2.**((IM-2)))*DZ

XZ=X(IM)

YZ=Y(IM)

PHIZ=PHI(IM)

PRZ=PR(IM)

PCZ=PC(IM)

RHOZ=RHO(IM)

RZ=RP(IM)

CZ=CP(IM)

GO TO 221

DZ=1.0

DTHETA=PI/10.

THETA=0.0

139
DO 561 I=1,20
THETA=THETA+DTHETA
XS=XZ+DZ*COS(PHIZ+THETA)
YS=YZ+DZ*SIN(PHIZ+THETA)
RHOS=SQRT(XS**2+YS**2)
CALL ARCTA(XS,YS,PHIS)
CALL POLY(N,A,RS,CS,PRS,PCS,RHOS,PHIS)
ABSP(I)=SQRT(RS**2+CS**2)
IF(ABSPZ-ABSP(I))561,561,601
CONTINUE
DZ=DZ/2.
IF(RHOS)563,565,563
IF(DZ/RHOS-1.E-7)5001,5001,521
IF(DZ-1.E-7)5001,5001,521
XZ=XS
YZ=YS
PHIZ=PHIS
RHOZ=RHOZ
ABSPZ=ABSP(I)
PRZ=PRS
PCZ=PCS
RZ=RS
CZ=CS
GO TO 221
IF(PHI(I)-1.E-6)711,711,351
IF(SU-ABSPZ)501,501,351
RHOZ=RHOZ+B0/SU**2
IF(RH0Z(I))901,901,816
PHI(I)=PHIZ+TOP/(RHOZ*SU**2)
CALL POLY(N,A,RS,CS,PRS,PCS,RH0Z(I),PHI(I))
ABSP(I)=SQRT(RZ**2+CZ**2)
IF(ABSP(I)-ABSPZ)851,881,881
XZ=RHOZ*COS(PHIZ)
YZ=RHOZ*SIN(PHIZ)
GO TO 5001
RHOZ=RHOZ
ABSPZ=ABSP(I)
PHIZ=PHIZ(I)
TOP=RZ*PCZ-CZ*PHIZ
BOT=-(RZ*PRZ+CZ*PCZ)
SU=SQRT(PRZ**2+PCZ**2)
IF(SU)855,501,855
U2=ABS2*SU
PSI=ATAN(U)
IF(ABSPZ/(RHOZ*SU)-10.***(-MTST))861,861,901
IF(ABSPZ/(RHOZ*SU)-1.E-7)841,841,871
IF(PHI(I)-1.E-6)881,881,801
DZ=ABSPZ/SU
XZ=RHOZ*COS(PHIZ)
YZ=RHOZ*SIN(PHIZ)
SUBROUTINE MTAL0D(AARG, NA, !AR, NB, C)

DIMENSION AARG(9999),!ARG(9999),C(9999),A(101),B(IO1)

I NAPLI=NA+1

DO 1 JI=1, NAPLI
A(JI)=AARG(JI)
1 CONTINUE

NBPl.

DO 41 JI=1, NB+1
f3(JI)=BARG(JI)
41 CONTINUE

NCPLI=NAPLI+NBPLI-1

I NTMP=O.

IF(J2-NAPLI) 61, 61, 81
N2=JII-J2+I
IF(N2-NPPLI) 71, 71, 81
TEMP=TEMP+A(J2)*B(N2)
81 CONTINUE

C(JI)=TEMP

CONTINUE

RETURN

END

S[Jf3RoIj'INE

DIMENSION A(9999),B(9999),C(9999)

II=NA-NB+1

DO 61 JI=1,II
(Q(JI)=O.
61 CONTINUE

QKI=NA-N9+1

DO 391 KK=1, QkmAX
K=KK-1
TEMP=O.

IF(K-1) 301, 211, 211
11=NA-K+J
TEMP=TEMP*B(I1)*O(I2+1)
1 CONTINUE

I=NA-NH-K
2 CONTINUE

RETURN

END

** **********MATR INVERSION************* **

SUBROUTINE MTINV(A, NA, NRARG, NCARG, IDIM, LABEL)
7500 DIMENSION A(IDIM,NCARG),LABEL(NRARG)
7510 1 NR=NRARG
7520 NC=NCARG
7530 DO 21 J1=1,NR
7540 21 LABEL(J1)=J1
7550 DO 291 J1=1,NR
7560* ***************FIND REMAINING ROW CONTAINING LARGEST***
7570* ***************ABSOLUTE VALUE IN PIVOTAL COLUMN***********
7580 DO 101 TEMP=0.0
7590 DO 121 J2=J1,NR
7600 IF(ABS(A(J2,J1)).LT TEMP) GO TO 121
7610 TEMP=ABS(A(J2,J1))
7620 IBIG=J2
7630 121 CONTINUE
7640 IF(IBIG.EQ.J1)GO TO 201
7650* ***************REARRANGE ROWS TO PLACE LARGEST ABSOLUTE
7660* ***************VALUE IN PIVOT POSITION***************
7670 DO 141 J2=1,NC
7680 TEMP=A(J1,J2)
7690 A(J1,J2)=A(IBIG,J2)
7700 141 A(IBIG,J2)=TEMP
7710 J=LABEL(J1)
7720 LABEL(J1)=LABEL(IBIG)
7730 LABEL(IBIG)=J
7740* *********COMPUTE COEFFICIENTS IN PIVOTAL ROW******
7750 201 TEMP=A(J1,J1)
7760 A(J1,J1)=1.0
7770 DO 221 J2=1,NC
7780 221 A(J1,J2)=A(J1,J2)/TEMP
7790* **********COMPUTE COEFFICIENTS IN OTHER ROWS******
7800 DO 281 J2=1,NR
7810 IF(J2.EQ.J1) GO TO 281
7820 TEMP=A(J2,J1)
7830 A(J2,J1)=0.0
7840 DO 241 J3=1,NC
7850 241 A(J2,J3)=A(J2,J3)-TEMP*A(J1,J3)
7860 281 CONTINUE
7870 291 CONTINUE
7880* ***************INTERCHANGE COLUMNS ACCORDING TO*******
7890* ***************INTERCHANGES OF ROWS OF ORIGINAL MATRIX*
7900 DO 301 NI=NR-1
7910 DO 391 J1=1,NI
7920 DO 321 J2=J1,NR
7930 IF(LABEL(J2).NE.J1) GO TO 321
7940 IF(J2.EQ.J1) GO TO 391
7950 GO TO 341
7960 321 CONTINUE
7970 341 DO 361 J3=1,NR
7980 TEMP=A(J3,J1)
7990 A(J3,J1)=A(J3,J2)
8000 361 A(J3,J2)=TEMP
8010 LABEL(J2)=LABEL(J1)
8020 391 CONTINUE
8030 5001 RETURN
8040 END

8050C  MTMPY — REV. APRIL 1971
8060*  HONEYWELL TIME SHARING APPLICATIONS
8070*  ************************************MATRIX MULTIPLICATION**************************
8080 SUBROUTINE MTMPY(IND, A, B, C, LARG, MARG, N)
8090 DIMENSION A(25,999), B(25,999), C(25,999)
8100   L=IABS(LARG)
8110   M=IABS(MARG)
8120   I=IND+1
8130 GO TO (101,201,301,401),1
8140   101 DO 121 J1=1,L
8150   121 DO 121 J2=1,n
8160   C(JI,J2)=0.0
8170   102 IF(LARG)103,5001,110
8180   103 IF(MARG)105,5001,103
8190   104 TEMP=A(J3,J1)*B(J3,J2)
8200   105 TEMP=A(J1,J3)*B(J3,J2)
8210   106 TEMP=A(J1,J3)*B(J3,J2)
8220   110 IF(MARG)111,5001,115
8230   111 TEMP=A(J1,J3)*B(J3,J2)
8240   115 TEMP=A(J1,J3)*B(J3,J2)
8250   121 C(JI,J2)=C(JI,J2)+TEMP
8260   121 C(JI,J2)=C(JI,J2)+TEMP
8270   121 C(JI,J2)=C(JI,J2)+TEMP
8280   121 C(JI,J2)=C(JI,J2)+TEMP
8290   100 GO TO 5001
8300   201 DO 221 J1=1,L
8310   221 C(JI,J1)=A(JI,J1)*B(J1,1)
8320   221 C(JI,J1)=A(JI,J1)*B(J1,1)
8330   221 C(JI,J1)=A(JI,J1)*B(J1,1)
8340   221 C(JI,J1)=A(JI,J1)*B(J1,1)
8350   201 DO 321 J2=1,M
8360   321 C(J1,J2)=C(J1,J2)*M
8370   321 C(J1,J2)=C(J1,J2)*M
8380   321 C(J1,J2)=C(J1,J2)*M
8390   321 C(J1,J2)=C(J1,J2)*M
8400   310 IF(MARG)311,5001,315
8410   310 IF(MARG)311,5001,315
8420   315 TEMP=A(J1,J1)*B(J1,1)
8430   315 TEMP=A(J1,J1)*B(J1,1)
8440   315 TEMP=A(J1,J1)*B(J1,1)
8450   315 TEMP=A(J1,J1)*B(J1,1)
8460   321 C(J1,J2)=TEMP
8470   321 C(J1,J2)=TEMP
8480   321 C(J1,J2)=TEMP
8490   321 C(J1,J2)=TEMP
8500   401 DO 421 J1=1,L
8510   421 C(J1,J2)=C(J1,J2)*L
8520   421 C(J1,J2)=C(J1,J2)*L
8530   421 C(J1,J2)=C(J1,J2)*L
8540   421 C(J1,J2)=C(J1,J2)*L
8550   410 IF(MARG)411,5001,415
8560   410 IF(MARG)411,5001,415
8570   415 TEMP=A(J1,J1)*B(J1,1)
8580   415 TEMP=A(J1,J1)*B(J1,1)
8590   415 TEMP=A(J1,J1)*B(J1,1)
8510   415 TEMP=A(J1,J1)*B(J1,1)
8520 410 TEMP=A(J2,J1)*B(J2,1)
8530 GO TO 421
8540* **************MATRIX X DIAGONAL A(I,M)*B(M,1)=C(****
8550 415 TEMP=A(J1,J2)*B(J2,1)
8560 421 C(J1,J2)=TEMP
8570 5001 RETURN
8580 END
8590 SUBROUTINE ATOD(N,XMSR,NBITS)
8600 IF(NBITS.LE.0) GO TO 80
8610 U2=0.0
8620 SIGN=-1.
8630 IF(XGE.0.0) SIGN=1.
8640 XW=W
8650 D=2.0*XMSR
8660 XW=XW*SIGN
8670 20 DELTA2=XMSR
8680 30 I=1,NBITS-1
8690 30 DELTA2=DELTA2/2.
8700 WOUT=2.*(XMSR-DELTA2)
8710 50 I=1,NBITS
8720 D=N/2.0
8730 Y=ABS(XW-U2)
8740 IF(YLE.DELTA2) WOUT=U2
8750 X=U2-D
8760 IF(XW.GE.(2.*XMSB-D/2.)) PRINT91"A/D HARD LIMITED SAMPLE"
8770 50 U2=X
8780 IF(XW.LT.DELTA2) WOUT=0.0
8790 IF(XXGE.(2.*XMSR-0/2.)) PRINT,"A/D HARD LIMITED SAMPLE"
8800 70 W=W.OUT
8810 80 RETURN
8820 END
8830 SUBROUTINE HMAG(R1A,R2A,XL1A,XL2A,R1,R2,X11,XL2)
8840 DIMENSION LIM(5),SK(5)
8850 PI2=2.*3.14159
8860 PRINT","
8870 PRINT,"CALCULATION OF ERROR IN H(S)**2"
8880 PRINT","
8890 J=1
8900 PRINT","SYSTEM POLES ARE"X11/PI2,XL2/PI2"
8910 PRINT","
8920 PRINT","SYSTEM RESIDUES ARE"R1*1.E6,R2*1.E6"
8930 PRINT","
8940 PRINT","FREQUENCY MAGNITUDE PHASE DIFFERENCE"
8950 PI2=2.43.14159
8960 XL1A=XL1A*1.E6
8970 XL2A=XL2A*1.E6
8980 R1=R1*1.E6
8990 R2=R2*1.E6
9000 LIM(1)=40
9010 LIM(2)=10
9020 LIM(3)=0

144
9030 LIM(4)=10
9040 LIM(5)=15
9050 SK(1)=1.E3
9060 SK(2)=5.E4
9070 SK(3)=1.E6
9080 SK(4)=1.E7
9090 SK(5)=5.E7
9100 CONTINUE
9110 DO 100 I=1,LIM(J)
9120 XI=I
9130 XI=XI*SK(J)
9140 W=PI2*XI
9150 AHMAG=W**((R1A+R2A)**2)+(R1A*XL2A+R2A*XL1A)**2
9160 AHMAG1=(W**W+XL1A*XL1A)**2*(W**W+XL2A*XL2A)
9170 AHMAGT=AHMAG/AHMAG1
9180 HMAG2=W**((R1+R2)**2)+(R1*XL2+R2*XL1)**2
9190 HMAG1=(W**W+XL1*XL1)**2*(W**W+XL2*XL2)
9200 HMAGT=HMAG2/HMAG1
9210 Y1=W*(R1+R2)
9220 Y2=R1*XL2+R2*XL1
9230 PHASE=-ATAN2(W,XL1)-ATAN2(W,XL2)+ATAN2(Y1,Y2)
9240 PHASE=PHASE*360./PI2
9250 IF(PHASE.LT.0.) PHASE=PHASE+360.
9260 DRDIFF=10.*(ALOG(HMAGT)/ALOG(10.))-(ALOG(HMAGT)/ALOG(10.))
9270 PRINT,XI,HMAGT,PHASE,DRDIFF
9280 CONTINUE
9290 J=J+1
9300 IF(J.LE.4) GO TO 200
9310 RETURN
9320 END
APPENDIX B

COMPUTER PROGRAM LISTING FOR THE HYBRID IMPLEMENTATION OF THE IDENTIFICATION TECHNIQUE

This is the listing of the computer program for the hybrid implementation. Note that the subroutines are identical to those listed in Appendix A and are not duplicated here.
HYBRID2P

DIMENSION XTA(10), XT(10), XX(10), R1(10), W(10)

DIMENSION A1(10), AP(10), CP(10), CI(10), CA(10)

DIMENSION G(10,10), Y(3,2420), U(3,2420), A(20,10), C(25,25)

DIMENSION ILSN(10), XLX(10), COEF(10), XLAMR(10), XLAMC(10)

DIMENSION RR(10), CH(10), B(25), CRR(10,10), CI(10,10)

DIMENSION LIMIT1(10), LABEL(25), S(25,1), R(25,1)

DIMENSION E1(25,25), E(25,25), CS(25,25)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION RN=10) , CI(10, 10), 3(25) , CRR(10, 10), CI(10, 10)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)

DIMENSION LIMIT1(I0), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(10), XMSB0(10)

DIMENSION LIMIT1(10), L.ABEL(25), S(25,1). R(25,1)

DIMENSION XMSH1(25,25), E(25,25), CS(25,25)
490 PRINT,   "  
500 FORMAT(18X,E14.5)  
510C EVALUATE INPUT AND OUTPUT FUNCTIONS  
520 RI(1)=2.806912E5  
530 RI(2)=-2.7368441E8  
540 RI(3)=1.E-3  
550 RI(4)=1.51F7  
560 RI(5)=1.E-3  
570 W(1)=.011550998*PI2  
580 W(2)=10.616986*PI2  
590 W(3)=10.  
600 W(4)=8.2*E-1*PI2  
610 W(5)=.350*PI2  
620 L=STEP  
630 AI(SN+1)=-W(SN+1)  
640 DO 991 IK=1,SN  
650 AI(K)=W(IK)  
660 CA(I)=CA(I)+RI(IK)*RI(I)/((W(IK)-3(I))*1.E6)  
670 CA(IK)=RI(IK)*RI(I)/((W(I)-W(IK))*1.E6)  
680 CI(IK)=-CA(IK)  
690 CONTINUE  
700 CI(I)=-CA(I)  
710 DO 999 JK=1,M+1  
720 XJK=JK  
730 U(1,JK)=0.  
740 XT3A=-W(STEP)*(XJK-1)*DELT  
750 IF(XT3A.LT.-80.) GO TO 166  
760 U(1,JK)=EXP(XT3A)  
770 CONTINUE  
780 U(1,JK)=1.E-3*SK*K*(1,JK)  
790 CALL ATOD(U(1,JK),XMSR(I),NRTS)  
800 DO 999 LJ=1,STEP  
810 XT(I)=0.  
820 XT(A(I))=-W(I)*X(JK-1)*DELT  
830 IF(XT(A(I)).LT.-80.) XT(I)=CA(I)*EXP(XT(A(I)))  
840 Y(1,JK)=Y(1,JK)*XT(IJ)  
850 Y(I,JK)=SK*Y(1,JK)  
860 CALL ATOD(Y(1,JK),XMSRO(I),NRTS)  
870 CONTINUE  
880 PRINT,   "  
890 PRINT,   " ACTUAL SYSTEM POLES AND RESIDUES"  
900 PRINT,   "  
910 PRINT,   " NUMBER POLE RESIDUE"  
920 DO 440 KL=1,SN  
930 PRINT,KL,K(KL)/PI2,RI(KL)  
940 440 PRINT,   "  
950 PRINT,   "  
960 M=M  
970 PRINT,"INPUT MSG="XMSGI  
980 PRINT, "  
990 CONTINUE
990 PRINT "OUTPUT MSB=",XMSR0
1000 PRINT """
1002 JN=SN+1
1005 DO 137 II=1,M+1
1010 XCV=-W(SN+1) *(II-1)*DELT
1012 IF(XCV.LT.-80.) GO TO 1480
1020 U(2,II)=R1(JN)/AI(JN)*(EXP(XCV))
1025 U(3,II)=R1(JN)/(AI(JN)**2)*(EXP(XCV))
1030 1480 U(3,II)=U(3,II)-R1(JN)/AI(JN)*II-1)*DELT
1034 U(2,II)=U(2,II)-R1(JN)/AI(JN)
1036 U(3,II)=U(3,II)-R1(JN)/(AI(JN)**2)
1040 137 CONTINUE
1050 M2=M2/2
1060 138 CONTINUE
1070 DO 10 JK=1,SN+1
1080 LIMIT(JK)=M+1
1090 DO 117 IL=1,SN+1
1100 XCV=-W(IL) *(KK-1) *DELT
1110 IF(XCV.LT.-80.) GO TO 1485
1120 Y(2,II)=Y(2,II) +CA(IL)/AI(IL)*(EXP(XCV))
1130 Y(3,II)=Y(3,II)+CA(IL)/(AI(IL)**2)*(EXP(XCV))
1140 1485 CONTINUE
1150 Y(2,II)=Y(2,II) -CA(IL)/AI(IL)
1160 Y(3,II)=Y(3,II)-CA(IL)/(AI(IL)**2)
1170 117 CONTINUE
1175 DO 39 IJK=2,SN+1
1180 CALL ATD(U(IJK,KK),XMSRI(IJK),NBITS)
1190 CALL ATD(Y(IJK,KK),XMSB0(IJK),NBITS)
1200 39 CONTINUE
1210 38 CONTINUE
1220 M=MORIG
1230 STEP1=SN+1
1240 STEP=2*SN+1
1250 DO 100 K=1,STEP1
1260 LJ=1
1270 M1=M
1280 MSL=1
1290 220 LIMIT=M-2
1300 JAT=0
1310 CONST=T/(3.*M)
1320 240 CONTINUE
1330 Evaluate inner products for Gram determinant
1340 M=MORIG
1350 STEP1=SN+1
1360 STEP=2*SN+1
1370 DO 100 K=1,STEP1
1380 LJ=1
1390 M1=M
1400 MSL=1
1410 220 LIMIT=M-2
1420 JAT=0
1430 CONST=T/(3.*M)
1440 240 CONTINUE
1450 Evaluate G(K,K) for K=1,SN

149
I = CONST
TERM1 = Y(K,I)**2 + 4.*Y(K,I+1)**2 + Y(K,I+2)**2
TERM3 = TERM1*TERM12
G(K,K) = G(K,K) + TERM3
STOP

CONTINUE
EVALUATE G(K,KM) FOR K = J+SN+1 TO K = SN+I
DO 3 J = 2, STEP 1
MSLJ = 1
IF(K-J) 435, 437, 436
DO 6 I = 1, M-1, 2
XTER2 = CONST
TEI2M22 = Y(K,MSLJ)*U(J,I)
HSLJ = MSLJ+1
TERM23 = 4.*Y(K,HSLJ)*U(J,I+1)
KSLJ = HSLJ+2
TERM24 = Y(K,KSLJ)*U(J,I+2)
TERM2 = XTER2*(TERM22+TERM23+TERM24)
KM = J+SN
G(K,KM) = G(K,KM) + TERM2
MSLJ = KSLJ
6 CONTINUE
GO TO 3
EVALUATE G(K,KM) FOR K = J TO K = SN+I
DO 176 I = 1, M-1, 2
XTER2 = CONST
TERM22 = Y(K,I)*U(J,MSLJ)
HSLJ = MSLJ+1
TERM23 = 4.*Y(K,HSLJ)*U(J,HSLJ)
KSLJ = HSLJ+2
TERM24 = Y(K,KSLJ)*U(J,KSLJ)
TERM2 = XTER2*(TERM22+TERM23+TERM24)
KM = J+SN
G(K,KM) = G(K,KM) + TERM2
MSLJ = KSLJ
176 CONTINUE
GO TO 3
EVALUATE G(K,KM) FOR K = J
DO 276 I = 1, M-1, 2
TERM22 = Y(K,I)*U(J,I)
TERM23 = 4.*Y(K,I+1)*U(J,I+1)
TERM24 = Y(K,I+2)*U(J,I+2)
XTER2 = CONST
TERM2 = XTER2*(TERM22+TERM23+TERM24)
KM = J+SN
G(K,KM) = G(K,KM) + TERM2
276 CONTINUE
3 CONTINUE
IF(K-STEP1) 236, 100, 100
100 CONTINUE
EVALUATE G(K,K) FOR K = SN+1 TO 2*SN+1
DO 8 K=SN+2,SN2+1
1970 DO 9 I=1,M-1,2
1980 DER1=V3(3,3)
1990 DER2=U(K-SN,I)**2+4.*U(K-SN,I+1)**2+U(K-SN,I+2)**2
2000 DER3=DER1*DER2
2010 G(K,K)=G(K,K)+DER3
2020 CONTINUE
2030 CONTINUE
2040 GO TO 425
2050 IF(K-SN)237,237,100
2060 IF(EVALUATE G(K,LK) FOR K .LT. SN, LK=K+1,SN+1
2070 DO 401 LK=K+1,SN+1
2080 MMW=LIMIT1(LK)-2
2090 LJ=1
2100 DO 402 LI=1,M-1,2
2110 TERM31=Y(K,LI)*Y(LK,LI)
2120 KHI=LI+1
2130 TERM32=Y(K,KHI)*Y(LK,LI+1)
2140 KH2=LI+2
2150 TERM33=Y(K,KHI)*Y(LK,LI+1)
2160 TERM34=TERM1
2170 LJ=LJ+2**FLOAT(1K-K+1)
2180 TERM2=TERM34*(TERM31+4.*TERM32+TERM33)
2190 G(K,LK)=G(K,LK)+TERM3
2200 CONTINUE
2210 CONTINUE
2220 IF(K-I)57,57,58
2230 IF(EVALUATE G(K+SN,LK+SN) FOR K=2,SN+1, LK=3,SN+1
2240 DO 601 LK=K+1,SN+1
2250 MMW=LIMIT1(LK)-2
2260 LJ=1
2270 DO 602 LI=1,M-1,2
2280 TEX1=U(K,LI)*U(LK,LI)
2290 KLI=LI+1
2300 TEX2=U(K,KLI)*U(LK,LI+1)
2310 KL2=LI+2
2320 TEX3=U(K,KLI)*U(LK,LI+2)
2330 TEX4=TERM1
2340 LJ=LJ+2**FLOAT(1K-K+1)
2350 TEX5=TEX4*(TEX1+4.*TEX2+TEX3)
2360 G(K+SN,LK+SN)=G(K+SN,LK+SN)+TEX5
2370 CONTINUE
2380 CONTINUE
2390 CONTINUE
2400 GO TO 100
2410 CONTINUE
2420 PRINT,"UNSCALED ENTRIES IN GRAM DETERMINANT ARE";
2430 PRINT,"";
2440 PRINT,"";
2450 PRINT,"";
2460 STEP1=STEP1+SN
2470 DO 942 JIK=1,STEP1
2480 DO 943 KLI=1,STEP1
2490 G(KLI,JIK)=G(JIK,KLI)
2500 PRINT, JIK, KLI, G(JIK,KLI)
2510 943 CONTINUE
2520 942 CONTINUE
2530 MM=MM+1
2540 N=SN2
2550 SCALE SCALAR PRODUCTS BY 1.E6 FOR COMPUTATION FACILITY
2560 DO 1011 I=1,SN2+1
2570 DO 1021 J=1,SN2+1
2580 G(I,J)=1.E6*G(I,J)
2590 1021 CONTINUE
2600 1011 CONTINUE
2610 EVALUATE DIAGONAL COFACTORS COEF(I)
2620 PRINT,"DIAGONAL COFACTORS ARE AS FOLLOWS"
2630 DO 300 J=1,SN2
2640 DO 310 I=1,SN2
2650 A(J,I)=G(J+I,I+1)
2660 A(I,J)=A(J,I)
2670 310 CONTINUE
2680 300 CONTINUE
2690 ID=1
2700 COEF(I)=DETE(A,N,20)
2710 PRINT, I, COEF(I)
2720 DO 500 LKJ=1,SN
2730 DO 400 J=1,LKJ
2740 DO 410 I=1,LKJ
2750 A(J,I)=G(J+I,I+1)
2760 A(I,J)=A(J,I)
2770 410 CONTINUE
2780 400 CONTINUE
2790 500 CONTINUE
2800 DO 510 J=1,LKJ
2810 DO 600 I=1,SN2
2820 A(J,I)=G(J+I,I+1)
2830 A(I,J)=A(J,I)
2840 600 CONTINUE
2850 510 CONTINUE
2860 500 CONTINUE
2870 COEF(LKJ+1)=DETE(A,N,20)
2880 PRINT, LKJ+1, COEF(LKJ+1)
2890 LKJ=LKJ+1
2900 640 CONTINUE
2910 PRINT,"EIGENVALUE EQUATION COEFFICIENTS ARE"
2920 EVALUATE EIGENVALUE EQUATION COEFFICIENTS R(I)
2930 DO 640 I=1,SN+1
2980 B(I)=SQRT(ABS(COEF(SN+2-I)))
2990 PRINT,I,B(I)
3000 640 CONTINUE
3010C EVALUATE SYSTEM POLES
3020 N=SN
3030 PRINT,"POLES OF SYSTEM ARE GIVEN BELOW"
3040 PRINT,"NUMBER REAL(MHZ) IMAG(MHZ)"
3050 CALL DOWNH(N,RR,CR)
3060 DO 650 J=1,SN
3070 XLAMR(J)=RR(J)/PI2
3080 XLAMC(J)=CR(J)/PI2
3090 AP(J)=RR(J)*1.E6
3100 AI(J)=1.E6*AI(J)
3110 PRINT,J,XLAMR(J),XLAMC(J)
3120 650 CONTINUE
3130 RR(SN+1)=-W(SN+1)
3140 A1(SN+1)=1.E6*A1(SN+1)
3150C EVALUATE SYSTEM RESIDUES
3160 FLAG=1
3170 DO 660 K=1,SN+1
3180 IF(XLAMC(J)FL 670,660,670
3190 670 FLAG=0
3200 660 CONTINUE
3210 IF(FLAG) 680,680,690
3220 680 IF(XLAMC(J)) 670,660,670
3230 690 FLAG=0
3240 DO 700 I=1,SN
3250 DO 710 J=1,SN
3260 TEMPI=1
3270 711 CONTINUE
3280 EWE1=0.
3290 EWE2=0.
3300 EWE1=1./TEMPI*(XLAMR(J)+W(SN+1))
3310 EWE1A=XLAMR(J)T
3320 EWE2A=-W(SN+1)T
3330 IF(EWE2A.GT.-RO.) EWE2=EXP(EWE2A)
3340 IF(EWE1A.GT.-BO.) EWE1=EXP(EWE1A)
3350 C(I,J)=EWE*(EWE1-EWE2)
3360 C(I,J)=1.E-3*SK*C(I,J)
3370 TEMP=0.
3380 DO 720 K=1,SN
3390 TEMP2=1.
3400 DO 721 KK=1,1+I-K
3410 TEMP2=TEMP2*XLAMR(J)
3420 721 CONTINUE
3430 TEMP=TEMP+U(K+1,LIMIT(K+1))/TEMP2
3440 720 CONTINUE
3450 C(I,J)=C(I,J)-TEMP
3455 CS(I,J)=C(I,J)
3460 710 CONTINUE

153
3470 700 CONTINUE
3480 CALL MTHINV(C,N,N,25,LABEL)
3490 ICOUNT=1
3500 EPS=1.E-3
3510 CALL MTMPY(O,CS,C,E,N,N)
3520 DO 763 I=1,SN
3530 DO 763 J=I,SN
3540 E(I,J)=EID(I,J)+E(I,J)
3550 763 CONTINUE
3560 TEMPO=0.E0
3570 DO 764 I=1,SN
3580 XNOR=0.E0
3590 DO 765 J=I,SN
3600 XNOR=XNOR+ABS(E(I,J))
3610 765 CONTINUE
3620 IF(XNOR.GT.TEMPO) TEMPO=XNOR
3630 764 CONTINUE
3640 IF(TEMPO.GT.1.0) GO TO 997
3650 IF(TEMPO.LE.EPS) GO TO 998
3660 DO 766 I=1,SN
3670 DO 766 J=I,SN
3680 766 CONTINUE
3690 CALL MTHPY(C,E,G,N,N)
3700 C(I,J)=G(I,J)
3710 DO 740 I=2,SN+1
3720 S(I-1,1)=Y(I,1,LIMIT(I))
3730 740 CONTINUE
3740 CALL MTMPY(O,C,S,R,SN,SN,1)
3750 PRINT*,"RESIDUES OF SYSTEM POLES ARE GIVEN BELOW"
3760 DO 751 I=1,SN
3770 PRINT,I,R(I,I)*1.E6
3780 751 CONTINUE
3790 998 CONTINUE
3800 DO 740 I=2,SN+1
3810 S(I-1,1)=Y(I,1,LIMIT(I))
3820 740 CONTINUE
3830 CALL MTMPY(O,C,S,R,SN,SN,1)
3840 PRINT*,"PERCENTAGE ERROR"
3850 DO 346 I=1,SN
3860 XX(I)=100.*(R(I,I)*1.E6-R1(I,J))/R1(I,J)
3870 346 CONTINUE
3880 PERCENTAGE ERROR
3890 PRINT,*" NUMBER POLE RESIDUE"
3900 PRINT,**
3910 DO 346 II=1,SN
3920 XX(II)=100.*(AP(II)-AL(II))/AL(II)
393) 346 PRINT, J,J,X(J), Y(J)
399)  PRINT, "JK ACTUAL PREDICTED DIFFERENCE"
400)  PRINT, "SUM=0.
4025  SUM=0.
4030  J=SN+1
4040  DO 341 J=1,SN
4050  CP(J)=R(J,1)*R(J)/(-N(J)-R(J,1))
4050  CP(J)=CP(J)+R(J,1)*R(J)/(-N(J)+R(J,1))
4070  341 CONTINUE
4072  IJK=0
4080  DO 247 J=1,SN+1
4090  K=JK
4100  YOUT=0
4110  DO 343 J=1,SN+1
4120  XT(I,J)=.0
4130  XI(A(I,J))*R(J)*DEL T
4140  IF(XA(I,J)<.0) YT(I,J)=CP(I,J)*EXP(XTA(I,J))
4150  YOUT=YOUT+5*XT(I,J)
4160  343 CONTINUE
4170  DEUT=DEUT-Y(I,J)
4180  IJK=IJK+1
4190  IF(IJK=SN+2) GO TO 248
4200  GO TO 249
4210  248 IJK=0
4220  PRINT, J,J,X(J),Y(J),DEUT,DEOUT
4230  249 CONTINUE
4240  247 CONTINUE
4250  T=1*1.E-5
4260  DO 242 J=1,SN+1
4270  I=242 I+1,SN+1
4280  SUM=SUM+CP(X)*CP(J)/(AP(I)+AP(J))
4290  IF((AP(I)+AP(J))<.0) GO TO 243
4300  SUM=SUM+CP(X)*CP(J)/(AP(I)+AP(J))+(EXP((AP(I)+AP(J))*T))
4310  SUM=SUM+CP(X)*CP(J)/(AP(I)+AP(J))+(EXP((AP(I)+AP(J))*T))
4320  SUM=SUM+CP(X)*CP(J)/(AP(I)+AP(J))+(EXP((AP(I)+AP(J))*T))
4330  SUM=SUM+CP(X)*CP(J)/(AP(I)+AP(J))+(EXP((AP(I)+AP(J))*T))
4340  242 CONTINUE
4350  TSM=SUM/T
4360  SUM=SUM/T
4370  PRINT,"SUM=",SUM
4380  PRINT,"TSM=",TSM
4390  PRINT,"TSN=",TSN
4400  PRINT,"TSO=",TSO
4410  PRINT,"MEAN SQUARED ERROR=",TSM
4420  PRINT,"TSN=",TSN
4430  PRINT,"TSM=",TSM
4440  STOP
APPENDIX C

COMPUTER PROGRAM LISTING FOR THE ANALOG IMPLEMENTATION OF THE IDENTIFICATION TECHNIQUE

This is the listing of the computer program for the analog implementation. Note that the subroutines are identical to those listed in Appendix A and are not duplicated here.
560 PRINT, ""
570 PRINT, "INTEGRATION TIME IN MICROSECONDS=".T
580 PRINT, ""
590 PRINT, "INTEGRATION INTERVAL IN MICROSECONDS=".DELT
600 PRINT, ""
610 900 FORMAT(18X,E14.5)
620C EVALUATE INPUT AND OUTPUT FUNCTIONS
630 RI(1)=2.8069192D5
640 RI(2)=-2.7368441D8
650 RI(3)=1.D-3
660 RI(4)=1.51D7
670 RI(5)=1.D-3
680 W(1)=1.1550998D-2*PI2
690 W(2)=1.061986D1*PI2
700 W(3)=10.
710 W(4)=8.20D-1*PI2
720 W(5)=.35*PI2
730 L=STEP
740 AI(SN+1)=-W(SN+1)-GAMMA
750 DO 901 IK=1,SN
760 AI(IK)=-W(IK)-GAMMA
770 CA(L)=CA(L)+RI(IK)*RI(L)/(W(IK)-W(L))*1.E6
780 CA(IK)=RI(IK)*RI(L)/(W(L)-W(IK))*1.E6
790 CI(IK)=CA(IK)
800 901 CONTINUE
810 CI(L)=CA(L)
820 XJK=JK
830 U(1,JK)=0.
840 XT3A=-W(STEP)*(XJK-1)*DELT
850 IF(XT3A.LT.-80.) GO TO 166
860 U(1,JK)=DEXP(XT3A)
870 166 CONTINUE
880 U(1,JK)=1.D-3*SK*U(1,JK)
900 DO 902 IJ=1,STEP
910 XT(IJ)=0.
920 XTA(IJ)=-W(IJ)*(XJK-1)*DELT
930 IF(XTA(IJ).GT.-80.) XT(IJ)=CA(IJ)*DEXP(XTA(IJ))
940 902 Y(I,JK)=Y(I,JK)+XT(IJ)
950 Y(I,JK)=SK*Y(I,JK)
970 999 CONTINUE
980 PRINT, "" ACTUAL SYSTEM POLES AND RESIDUES
990 PRINT, ""
1000 PRINT, "" NUMBER POLE RESIDUE"
1010 PRINT, ""
1020 PRINT, ""
1030 DO 446 KL=1,SN
1040 PRINT,KL,W(KL)/PI2,RI(KL)
1050 446 PRINT, ""
1060 PRINT, ""
1070 M2=M
1090 PRINT, ""
ANALOG IMPLEMENTATION———TWO POLES——

IMPERFECT INTEGRATOR——

VERSION 2——

IMPLICIT DOUBLE PRECISION(A-H,O-Z)

DIMENSION FA(10)

DIMENSION XTA(10),XT(10),XX(10),R1(10),W(10)

DIMENSION A1(10),AP(10),CP(10),CI(10),CA(10)

DIMENSION G(10,10),Y(5,1),U(5,1),A(20,10),C(25,25)

DIMENSION ISN(10),XLX(10),COEF(10),XLMR(10),XLMC(10)

DIMENSION RR(10),CR(10),R(25),CRR(10,10),CI(10,10)

DIMENSION LIMITI(10),LABEL(25),S(25,1),R(25,1)

DIMENSION EID(25,25),E(25,25),CS(25,25)

DIMENSION ISN,STEP1,STEP2

INTEGER SN,STEP1,STEP2

INITIALIZE AND INPUT PARAMETERS

PI2=2.*3.14159

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1100 PRINT, "INTEGRATOR LOW FREQ CUTOFF (HERTZ)", GAMMA/(PI2*1.0-6)
1110 PRINT, "MULTIPLIER ERROR(x)=" SG*100.
1120 JN=SN+1
1125 SC=GAMMA*T
1130 II=1
1140 XCV=-M(5*I+1)*M*DELT
1150 IF(XCV_LT.-.30.,) G0 1480
1160 U(2,II)=R(JN)/A(JN)**(EXP(XCV))
1170 U(3,II)=R(JN)/A(JN)**2*(EXP(XCV))
1180 U(4,II)=R(JN)/A(JN)**3*(EXP(XCV))
1190 U(5,II)=R(JN)/A(JN)**4*(EXP(XCV))
1200 IF(XCV.LT.-.90.) (3)
1210 U(2,II)=U(2,II)-R(JN)*EXP(SC)/A(JN)**2*(T1-T)*DELT
1220 U(4,II)=U(4,II)-R(JN)*EXP(SC)/A(JN)**2*(T1-T)*DELT
1230 U(5,II)=U(5,II)-R(JN)*EXP(SC)/A(JN)**2*(T1-T)*DELT
1240 U(3,II)=U(3,II)-R(JN)*EXP(SC)/A(JN)**2*(T1-T)*DELT
1250 U(4,II)=U(4,II)-R(JN)*EXP(SC)/A(JN)**3*(T1-T)*DELT
1260 U(5,II)=U(5,II)-R(JN)*EXP(SC)/A(JN)**3*(T1-T)*DELT
1270 U(3,II)=U(3,II)-R(JN)*EXP(SC)/A(JN)**3*(T1-T)*DELT
1280 U(4,II)=U(4,II)-R(JN)*EXP(SC)/A(JN)**3*(T1-T)*DELT
1290 U(5,II)=U(5,II)-R(JN)*EXP(SC)/A(JN)**3*(T1-T)*DELT
1300 CONTINUE
1310 U3=U3/2
1320 CONTINUE
1340 X0=10 JK=1,SN+1
1350 LIMIT(JK)=1
1360 CONTINUE
1370 XJ=1,SN=1
1380 CONTINUE
1390 U0=117 IL=1,SN+1
1400 XCV=-M(IL)**M*DELT
1410 IF(XCV_LT.-.90.) G0 1485
1420 Y(2,KK)=Y(2,KK)+CA(IL)/A(IL)**(EXP(XCV))
1430 Y(3,KK)=Y(3,KK)+CA(IL)/A(IL)**2*(EXP(XCV))
1440 Y(4,KK)=Y(4,KK)+CA(IL)/A(IL)**3*(EXP(XCV))
1450 Y(5,KK)=Y(5,KK)+CA(IL)/A(IL)**4*(EXP(XCV))
1460 CONTINUE
1470 Y(2,KK)=Y(2,KK)-CA(IL)*EXP(SC)/A(IL)**2
1480 Y(3,KK)=Y(3,KK)-CA(IL)*EXP(SC)/A(IL)**2*(K1-T)*DELT
1490 Y(4,KK)=Y(4,KK)-CA(IL)*EXP(SC)/A(IL)**2*(K1-T)*DELT
1500 Y(5,KK)=Y(5,KK)-CA(IL)*EXP(SC)/A(IL)**2*(K1-T)*DELT
1510 Y(3,KK)=Y(3,KK)-CA(IL)*EXP(SC)/A(IL)**3*(K1-T)*DELT
1520 Y(4,KK)=Y(4,KK)-CA(IL)*EXP(SC)/A(IL)**3*(K1-T)*DELT
1530 Y(5,KK)=Y(5,KK)-CA(IL)*EXP(SC)/A(IL)**3*(K1-T)*DELT
Y(5,KK) = Y(5,KK) - CA(I) * EXP(SC) / (2. * A1(I) ** 2) * ((KK-1) ** 2)
Y(5,KK) = Y(5,KK) - CA(I) * EXP(SC) / (A1(I) ** 4)

CONTINUE

1580 13 CONTINUE
1590 C EVALUATE INNER PRODUCTS FOR SINH DETERMINANT
1600 M = MORT G
1610 STEP = SN + 1
1620 STEP = 2 * SN + 1
1630 SUM = 0.
1640 IF (K, I = 1, STEP)
1650 IX = J = 1, SN + 1
1660 SUM = SUM + C1(I) * C1(J) / (A1(I) + A1(J))
1670 S3 = (A1(I) + GAMMA * A1(J) + GAMMA * T)
1680 IF (S3, LT, -90.) GO TO 1
1690 SUM = SUM + C1(I) * C1(J) / (A1(I) + A1(J)) * EXP(S3)
1700 1 CONTINUE
1710 G(1,1) = SUM
1715 G(1,1) = (I, * SG * UNIFM2(10., 0., 2.)) * G(1,1)
1720 SUM = 0.
1730 IF (DO 2 I = 1, STEP)
1740 SUM = SUM + C1(I) * C1(I) / (2. * A1(I) ** 2)
1750 X1 = X1 = C1(I) / A1(I)
1760 S3 = 2. * (A1(I) * GAMMA) * T
1770 IF (S3, LT, -90.) GO TO 2
1780 SUM = SUM + C1(I) * C1(I) / (2. * A1(I) ** 2) * EXP(S3)
1790 2 CONTINUE
1800 IF (DO 3 I = 1, SN + 1)
1810 S3 = A1(I) * T
1820 IF (S3, GT, -90.) SUM = SUM - X1 * C1(I) / A1(I) * EXP(S3)
1830 DO 3 J = 1, STEP
1840 IF (J, LE, I) GO TO 3
1850 SUM = SUM + C1(I) * C1(J) / (A1(I) + A1(J))
1860 S3 = (A1(I) + GAMMA * A1(J) + GAMMA) * T
1870 IF (S3, LT, -90.) GO TO 3
1880 SUM = SUM + C1(I) * C1(J) / (A1(I) + A1(J)) * EXP(S3)
1890 3 CONTINUE
1900 G(1,2) = SUM
1905 G(1,2) = (1. * SG * UNIFM2(10., 0., 2.)) * G(1,2)
1910 SUM = 0.
1920 DO 4 I = 1, STEP
1930 DO 4 J = 1, STEP
1940 S1 = A1(I) * A1(J)
1950 S2 = A1(I) * A1(J)
1960 SUM = SUM + C1(I) * C1(J) / S2 * (1. / A1(I) + 1. / A1(J) + T - 1. / S1)
1970 S3 = (A1(I) + GAMMA * A1(J) + GAMMA) * T
1980 IF (S3, LT, -90.) GO TO 41
1990 SUM = SUM + C1(I) * C1(J) / (A1(I) + A1(J)) * S3 / A1(I) * EXP(S3)
2000 41 SUM = SUM + C1(I) * C1(J) / (A1(I) + A1(J)) * S3 / A1(I) * EXP(S3)
203)  $S3 = A1(J) \times T$

204)  IF(S3.LT.-90.) G0 TO 4

2050)  $SUM = SUM - CI(1) \times CI(J) / S2 \times DEXP(S3) / A1(J)$

2060)  4 CONTINUE

2070)

2270)  $G(2,2) = SUM$

2275)  $G(2,2) = (1. \times 5 \times U \times V \times M \times Z(10.,0.,2.,.) \times G(2,2))$

2280)  $SUM = 0.$

2290)  $F = CI(1) / AI(1) + CI(2) / AI(2) + CI(3) / AI(3)$

2300)  $FA(1) = CI(1) / AI(1) \times (CI(2) / AI(2) + CI(3) / AI(3))$

2310)  $FA(1) = FA(1) - CI(1) / AI(1) \times (CI(2) / AI(2) + \times CI(3) / AI(3))$

2320)  $FA(2) = CI(2) / AI(2) \times (CI(1) / AI(1) + CI(3) / AI(3))$

2330)  $FA(2) = FA(2) - CI(2) / AI(2) \times (CI(1) / AI(1) + CI(3) / AI(3))$

2340)  $FA(3) = CI(3) / AI(3) \times (CI(1) / AI(1) + CI(2) / AI(2))$

2350)  $FA(3) = FA(3) - CI(3) / AI(3) \times (CI(1) / AI(1) + CI(2) / AI(2))$

2360)  $FA(2) = FA(2) - CI(3) / AI(3) \times (CI(1) / AI(1) + CI(2) / AI(2))$

2370)  $FA(3) = FA(3) - CI(3) / AI(3) \times (CI(1) / AI(1) + CI(2) / AI(2))$

2380)  $F(1) = CI(1) / AI(1) \times (CI(2) / AI(2) + CI(3) / AI(3))$

2390)  $F(2) = CI(2) / AI(2) \times (CI(1) / AI(1) + CI(3) / AI(3))$

2400)  $F(3) = CI(3) / AI(3) \times (CI(1) / AI(1) + CI(2) / AI(2))$

2410)  IF(S3.LT.-90.) G0 TO 9

2420)  $SUM = SUM + FA(I) \times DEXP(S3)$

2430)  9 CONTINUE

2440)  IF(S3.LT.-90.) G0 TO 10

2450)  $SUM = SUM + CI(1) \times CI(I) / (2. \times AI(I) \times **3) \times DEXP(S3)$

2460)  10 SUM = SUM + CI(1) \times CI(I) / (2. \times AI(I) \times **3)

2470)  9 CONTINUE

2480)  $SUM = SUM + CI(1) \times CI(I) / (2. \times AI(I) \times **3)$

2490)  9 CONTINUE

2500)  $SUM = SUM + CI(1) \times CI(I) / (2. \times AI(I) \times **3)$

2510)  9 CONTINUE

2520)  $SUM = SUM + CI(1) \times CI(I) / (2. \times AI(I) \times **3)$

2530)  9 CONTINUE

2540)  $SUM = SUM + CI(1) \times CI(I) / (2. \times AI(I) \times **3)$

2550)  9 CONTINUE

2560)  $SUM = SUM \times CI \times DEXP(S3)$

2570)  9 CONTINUE

2580)  $G(1,3) = SUM$

2590)  $G(1,3) = (1. \times 5 \times U \times V \times M \times Z(10.,0.,2.,.) \times G(1,3))$

2600)  $X = CI(1) / AI(1)$

2610)  $Y = CI(2) / AI(2)$

2620)  $Z = CI(3) / AI(3)$

2630)  $T = X \times Y / 2$

2640)  $F1 = X \times X + 2. \times X \times Y / 2 + X \times Z + Y \times A + 2. \times Y \times A + 2. \times Z \times Z$

2650)  $F2 = X \times X / A1(1) + 2. \times X \times Y / A1(3) + 2. \times Y \times Y / A1(2) + 2. \times Z \times Z / A1(3) + 2. \times X \times X + 2. \times X \times Y + 2. \times Y \times Z + 2. \times Z \times Z$

2660)  $F3 = X \times Y / A1(1) \times **2 + 2. \times X \times Y / A1(1) \times **2 + 2. \times Y \times Y / A1(1) \times **2 + 2. \times Z \times Z / A1(1) \times **2$

2670)  $F4 = X \times X \times Y \times Y / A1(2) \times A1(3) \times A1(3)$

2680)  $F5 = X \times Y / A1(1)$

2690)  $F_5 = 2. \times A1(1)$

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320) \[ D1 = X**2/A1(1) + X*YA/A1(2) + X*Z/A1(3) + YA**2/A1(2) + YA*Z/A1(3) \]
321) \[ D1 = D1 + Z*Z/A1(3) \]
322) \[ D1 = D1 + X*YA/A1(1) + X*Z/A1(1) + Y*Z/A1(2) \]
323) \[ SUM = SUM + D1*T \]
324) \[ B1 = X**2*2.*X*YA + X*Z*2.*Y*Z + YA**2/2. \]
325) \[ SUM = SUM + B1*T*T/2. \]
326) \[ SUM = SUM + G1/A1(1) - G2/A1(2) - G3/A1(3) \]
327) \[ S3 = A1(1)*T \]
328) \[ IF(S3, LT, -90.) G0 TO 40 \]
329) \[ SUM = SUM + G1/A1(1)*D*EXP(S3) \]
330) \[ 40 S3 = A1(2)*T \]
331) \[ IF(S3, LT, -90.) G0 TO 14 \]
332) \[ SUM = SUM + G2/A1(2)*D*EXP(S3) \]
333) \[ 14 S3 = A1(3)*T \]
334) \[ IF(S3, LT, -90.) G0 TO 15 \]
335) \[ SUM = SUM + G3/A1(3)*D*EXP(S3) \]
336) \[ 15 CONTINUE \]
337) \[ DO 16 I = 1, SN+1 \]
338) \[ SUM = SUM + Cl(I)*Cl(I)/(2.*A1(I)**4) \]
339) \[ S3 = 2.*A1(I) + GAMMA*A*T \]
340) \[ IF(S3, LT, -90.) G0 TO 61 \]
341) \[ SUM = SUM + Cl(I)*Cl(I)/(2.*A1(I)**4)*D*EXP(S3) \]
342) \[ 16 CONTINUE \]
343) \[ S3 = (A1(I) + GAMMA*A1(I) + GAMMA)*T \]
344) \[ IF(S3, LT, -90.) G0 TO 61 \]
345) \[ SUM = SUM + X*YA*(1./A1(2) + 1./A1(1))*D*EXP(S3) \]
346) \[ 61 S3 = (A1(I) + GAMMA*A + GAMMA)/A1(3)*D*EXP(S3) \]
347) \[ IF(S3, LT, -90.) G0 TO 62 \]
348) \[ SUM = SUM + X*Z*(1./A1(3) + 1./A1(1))*D*EXP(S3) \]
349) \[ 62 S3 = (A1(2) + GAMMA*A + GAMMA)/A1(3)*D*EXP(S3) \]
350) \[ IF(S3, LT, -90.) G0 TO 63 \]
351) \[ SUM = SUM + YA*Z*(1./A1(3) + 1./A1(2))*D*EXP(S3) \]
352) \[ 63 CONTINUE \]
353) \[ SUM = SUM + X*YA*(1./A1(2) + 1./A1(1))/(A1(I) + A1(2)) \]
354) \[ SUM = SUM + X*Z*(1./A1(3) + 1./A1(1))/(A1(I) + A1(3)) \]
355) \[ SUM = SUM + YA*Z*(1./A1(3) + 1./A1(2))/(A1(I) + A1(3)) \]
356) \[ G(2, 3) = SUM \]
357) \[ G(2, 3) = (1.*G1*UNIFM2(10., 0., 2.)*G(2, 3)) \]
358) \[ SUM = 0. \]
359) \[ KN = SN+1 \]
360) \[ X = R1(KN)/A1(KN) \]
361) \[ DO 28 I = 1, SN+1 \]
362) \[ SUM = SUM + X*(Cl(I) + A1(I) - A1(KN))/A1(KN) \]
363) \[ S3 = (A1(I) + GAMMA*A + GAMMA)/A1(KN)*D*EXP(S3) \]
364) \[ IF(S3, LT, -90.) G0 TO 29 \]
365) \[ SUM = SUM + X*Cl(I)/A1(I)*D*EXP(S3) \]
366) \[ 29 S3 = A1(I)*T \]
367) \[ IF(S3, LT, -90.) G0 TO 28 \]
368) \[ SUM = SUM - X*Cl(I)/A1(I)*D*EXP(S3) \]
369) \[ 28 CONTINUE \]
370) \[ G(1, 4) = SUM \]
G(1,4) = (1. + SG*UNIFORM2(10.,0.,2.))*G(1,4)
SUM=G(1,4)/AI(KN)
DO 30 I=1,KN
SUM=SUM-X*C(I)/(AI(I)**2)
S=AI(I)*T
IF(S3.LT.-90.) GO TO 30
SUM=SUM-X*C(I)*(T/AIN(I)-1./AI(I)**2))**DEXP(S3)
CONTINUE

S1=G(1,5)
S1=SUM
DO 30 1=1,KN
X=RI(KN)/AI(KN)
SUM=SUM+X*C(1)/AI(I)*(1./AI(I)-1./AI(I)**2)
S3=AI(I)*T
IF(S3.LT.-90.) GO TO 33
S3=(AI(I)-GAMMA*AI(KN)+GAMMA)**T
IF(S3.LT.-90.) GO TO 51
SUM=SUM+RI(KN)*C(I)*(AI(I)**2/((AI(I)-1.)/(AI(I)-1.)*AI(I))**2))**DEXP(S3)
51 S3=AI(KN)**T
IF(S3.LT.-90.) GO TO 45
SUM=SUM-RI(KN)/AI(KN)*C(I)/(AI(I)-1.)*DEXP(S3)
CONTINUE

S1=G(2,4)=SUM
S1=G(2,4)/AI(KN)
DO 34 I=1,KN
SUM=SUM+T**2/2.*RI(KN)*C(I)/(AI(I)*AI(KN))
SUM=SUM-RI(KN)*C(I)/(AI(I)-1.)*AI(KN)**2)
S3=AI(I)*T
IF(S3.LT.-90.) GO TO 34
SUM=SUM-RI(KN)/AI(KN)*C(I)/(AI(I)**2/((AI(I)-1.)/(AI(I)-1.)*AI(I))**2))**DEXP(S3)
CONTINUE

S1=G(2,5)=SUM
S1=G(2,5)/AI(KN)
SUM=0.
X=RI(KN)/AI(KN)
DO 40 I=1,SN+1
SUM=SUM+X*C(I)/(AI(I)**2/((AI(I)-1.)/(AI(I)-1.)*AI(I))**2))**DEXP(S3)
CONTINUE

S1=G(2,4)=SUM
S1=G(2,4)/AI(KN)
SUM=0.
X=RI(KN)/AI(KN)
DO 40 I=1,SN+1
SUM=SUM+X*C(I)/(AI(I)**2/((AI(I)-1.)/(AI(I)-1.)*AI(I))**2))**DEXP(S3)
CONTINUE

T=1./(AI(KN)**2)-T/AIN(KN)-1./AI(I)**2)

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4120  SUM=SUM+X*CI(I)/AI(I)*TER*DEXP(S3)
4130  53  S=AI(I)*T
4140  IF(S3.LT.-90.) GO To 35
4150  SUM=SUM-X*CI(I)/(AI(I)**3)*DEXP(S3)
4160  35  CONTINUE
4170  G(3,4)=SUM
4175  G(3,4)=1.+SG*UNIFORM(10.,0.,2.)*G(3,4)  
4180  SUM=G(3,4)/AI(KN)
4190  DO 36  I=1,KN
4200  X=RI(KN)/AI(KN)*CI(I)/AI(I)
4210  YA=X
4220  SUM=SUM-X/((AI(I)**3)+YA*(T*T/(2.*AI(I))+(T**3)/3.))
4230  36  S3=AI(I)*T
4240  IF(S3.LT.-90.) GO To 37
4250  SUM=SUM-X*(T/(AI(I)**2)-1./((AI(I)**3))*DEXP(S3)
4260  37  CONTINUE
4270  G(3,5)=SUM
4275  G(3,5)=1.+SG*UNIFORM(10.,0.,2.)*G(3,5)
4280  SUM=0.
4290  X=RI(KN)/AI(KN)
4300  SUM=X*X*(T+AI(KN)-1.)/(2.*AI(KN)))
4310  S3=AI(KN)*T
4320  IF(S3.LT.-90.) GO To 38
4330  SUM=SUM-X*X**2./AI(KN)*DEXP(S3)
4340  38  S3=2.*AI(KN)*GAMMA*T
4350  IF(S3.LT.-90.) GO To 44
4360  SUM=SUM+X*X/(2.*AI(KN))*DEXP(S3)
4370  44  CONTINUE
4380  G(4,4)=SUM
4385  G(4,4)=1.+SG*UNIFORM(10.,0.,2.)*G(4,4)
4390  SUM=G(4,4)/AI(KN)
4395  SUM=SUM-X*X*(1./((AI(KN)**2)-T*T/2.))
4400  S3=AI(KN)*T
4410  IF(S3.LT.-90.) GO To 38
4420  SUM=SUM-X*X*(T/AI(KN)-1./((AI(KN)**2)))*DEXP(S3)
4430  38  CONTINUE
4450  G(4,5)=SUM
4455  G(4,5)=1.+SG*UNIFORM(10.,0.,2.)*G(4,5)
4460  SUM=G(4,5)/AI(KN)**2
4465  SUM=SUM*X**3/(T**3)/3.
4470  S3=AI(KN)*T
4475  IF(S3.LT.-90.) GO To 38
4480  SUM=SUM+X*X*(T/AI(KN)-1./((AI(KN)**2)))*DEXP(S3)
4490  38  CONTINUE
4500  G(5,5)=SUM
4505  G(5,5)=1.+SG*UNIFORM(10.,0.,2.)*G(5,5)
4510  PRINT,*"UNSCALED ENTRIES IN GRAM DETERMINANT ARE"
4515  PRINT,"I   J   G(I,J)"
4520  PRINT,"ROW   COLUMN   INNER PRODUCT"
4580  STEPI=STEPI+SN
4590  DO 942 JIK=1,STEPI
4600  DO 943 KLI=1,STEPI
4601
4602  XMSGI=DABS(G(JIK,KLI))*(I.+1./((2.*NBITS))
4605  CALL ATOD(G(JIK,KLI),XMSGI,NBITS)
4610  G(KLI,JIK)=G(JIK,KLI)
4620  PRINT,JIK,KLI,G(JIK,KLI)
4630  943 CONTINUE
4640  942 CONTINUE
4650  MD=IG=M
4660  N=SN2
4670  SCALE SCALAR PRODUCTS BY 1.E6 FOR COMPUTATION FACILITY
4680  DO 1011 I=1,SN2+1
4690  DO 1021 J=ISN2+1
4700  (G(I,J))=FQ*G(I,J)
4710  1021 CONTINUE
4720  1011 CONTINUE
4730  EVALUATE DIAGONAL COFACTORS COEFA(I)
4740  PRINT,"DIAGONAL COFACTORS ARE AS FOLLOWS"
4750  DO 300 J=1,SN2
4760  DO 310 I=1,SN2
4770  A(J,I)=G(J+1,I+1)
4780  A(I,J)=A(J,I)
4790  310 CONTINUE
4800  300 CONTINUE
4810  ID=1
4820  COEF(1)=DETE(A,N,20)
4830  PRINT, "DIAGONAL COFACTORS ARE AS FOLLOWS"
4840  DO 500 LKJ=1,SN
4850  DO 510 J=1,LKJ
4860  DO 520 I=1,LKJ
4870  A(J,I)=G(J,I)
4880  A(I,J)=G(I,J)
4890  520 CONTINUE
4900  510 CONTINUE
4910  DO 600 J=1,LKJ
4920  DO 610 I=1,LKJ
4930  A(J,I)=G(J+1,I+1)
4940  A(I,J)=A(J,I)
4950  610 CONTINUE
4960  600 CONTINUE
4970  COEF(I+1)=DETE(A,N,20)
4980  PRINT, LKJ+1, COEF(LKJ+1)
4990  LNKJ+1, COEF(LKJ+1)
5050 500 CONTINUE
5060 PRINT, "EIGENVALUE EQUATION COEFFICIENTS ARE"
5060 PRINT, "EVALUATE EIGENVALUE EQUATION COEFFICIENTS B(I)
5070 DO 640 I=1,SN+1
5080 B(I)=DOSA(T(DABS(COEF(SN+2-I))))
5090 PRINT, I, B(I)
5100 CONTINUE
5110 640 CONTINUE
5120 640 CONTINUE
5130 PRINT, "POLES OF SYSTEM ARE GIVEN BELOW"
5140 PRINT, "NUMBER REAL(MHZ) IMAG(MHZ)"
5150 DO 650 J=1,SN
5160 XLMR(J)=RR(J)*PI2
5170 XLMC(J)=CR(J)*PI2
5180 AP(J)=RR(J)*1.E6
5190 A1(J)=-1.06*W(J)
5200 PRINT, J,XLMR(J),XLMC(J)
5210 XLMR(J)=RR(J)
5220 CONTINUE
5230 PRINT, "POLES OF SYSTEM ARE GIVEN BELOW"
5240 DO 650 J=1,SN
5250 RR(SN+1)=RR(J)*1.E6
5260 A1(SN+1)=-1.06*W(SN+1)
5270 AP(SN+1)=RR(SN+1)*1.E6
5280 PRINT, "POLES OF SYSTEM ARE GIVEN BELOW"
5290 C(1,J)=F1*(W1-EQM2)
5300 CONTINUE
5310 IF(XLMR(J)) 670, 660, 670
5320 IF(XLMC(J)) 670, 660, 670
5330 670 FLAG=0
5340 660 CONTINUE
5350 IF(FLAG) 680, 680, 690
5360 690 DO 700 I=1,SN
5370 700 J=1,SN
5380 IF(TEMP) 711, 1
5390 711 TEMP=TEMP1*XLMR(J)
5400 711 CONTINUE
5410 IF(W1-EQM2) 5420, 5430
5420 W1=0.
5430 W2=0.
5440 W1=E1/(TEMP1*XLMR(J)+A(SN+1)))
5450 W2=W1*XLMR(J)*T
5460 TEMP2=A(W(SN+1))
5470 IF(W1GT80.) EWE2=EXP(EWM2)
5480 IF(W1GT80.) EWE1=EXP(EWM1)
5490 C(1,J)=E1*(EWE1-EWE2)
5500 TEMP=0.
5510 720 X=1,1
5520 721 KK=1,1+1-K
5530 721 CONTINUE
5540 TEMP=TEMP+U(K+1,LIMIT1(K+1))/TEMP2

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CONTINUE
C(I,J) = C(I,J) - TEMP
CS(I,J) = C(I,J)
CONTINUE
CALL MTEPV0,C,N,N,35,LABEL)
ICOUNT = 1
EPS = 1.0
DO 763 I = 1,SN
DO 763 J = 1,SN
E(I,J) = FID(I,J) - F(I,J)
CONTINUE
IF XNOR,XT,TEMPO TEMPO=XNOR
DO 764 I = 1,SN
XNOR = 0.0
DO 765 J = 1,SN
XNOR = XNOR + DABS(E(I,J))
CONTINUE
IF (XNOR,XT,TEMPO) GO TO 997
CONTINUE
IF (TEMPO, GT, 1.0) GO TO 997
IF (TEMPO, LT, EPS) GO TO 998
DO 766 I = 1,SN
DO 767 J = 1,SN
E(I,J) = FID(I,J) + E(I,J)
CONTINUE
CALL MTEPV0,C,E,G,N,N,N
DO 768 I = 1,SN
DO 769 J = 1,SN
C(I,J) = G(I,J)
CONTINUE
IF (ICOUNT, GT, 5) GO TO 998
ICOUNT = ICOUNT + 1
GO TO 997
997 PRINT, "NORM TOO LARGE", TEMPO
998 CONTINUE
DO 740 I = 2,SN+1
S(I-1,1) = Y(I,LIMIT(I))
740 CONTINUE
CALL MTEPV0,C,E,S,SN,SN,1
PRINT, "RESIDUES OF SYSTEM POLES ARE GIVEN BELOW"
DO 751 I = 1,SN
DO 751 I = I*1.ES
CONTINUE
DO 751 I = 1,SN
DO 751 I = 1.000
DO 751 1000 CONTINUE
CONTINUE
PRINT," PERCENTAGE ERROR"
6080  PRINT, "NUMBER POLE RESIDUE"
6090  PRINT,""
6100  DO 346 11=1,SN
6110  XAX(II)=100.*R(I1,1)*E6-R1(II))/R1(II)
6120  XX(II)=100.*((AP(II)-AI(II))/A1(II))
6130  346  PRINT,I!,XAX(II),XX(II)
6140  PRINT,""
6150  PRINT,""
6170  SUM=0.
6180  SUM1=0.
6190  J=SN+1
6200  DO 341 1J=1,SN
6210  CI(JI)=CI(JI)
6220  CP(JI)=R(JI,1)*R1(JI)/W(JI)+RR(Jl)
6230  CONTINUE
6230  341  CONTINUE
6240  CI(J)=CI(J)
6249  M0RIG=1
6250  DO 247  JK=1,M0RIG+1
6260  XJK=JK
6270  YOUT=0.0
6280  DO 343  IJ=1,SN+1
6290  XT(IJ)=0.0
6300  XT(IJ)=R(IJ,1)*R1(IJ)/W(IJ)+RR(IJ)
6310  IF(XTA(IJ).GT.-80.) XT(IJ)=CP(IJ)*DEXP(XTA(IJ))
6320  YOUT=YOUT+S1*XT(IJ)
6330  343  CONTINUE
6340  DELOUT=YOUT-Y(1,JK)
6350  IJK=IJK+1
6360  IF(IJK.GE.100) GO TO 248
6370  GO TO 249
6380  248  IJK=0
6390  249  CONTINUE
6400  247  CONTINUE
6410  T=T*1.E-6
6420  DO 242  IX=1,SN+1
6430  DO 242  IJ=1,SN+1
6440  SUM=0.0
6450  SUM=SUM+CP(IX)*CP(JX)/(AP(IX)+AP(JX))
6460  IF((AP(IX)+AP(JX))<0.) GO TO 243
6470  SUM=SUM+CP(IX)*CP(JX)/(AP(IX)+AP(JX))+(AP(IX)+AP(JX))/T
6480  243  SUM=SUM+2.*CP(IX)*CI(JX)/(AP(IX)+A1(JX))
6490  IF((AP(IX)+A1(JX))<0.) GO TO 244
6500  SUM=SUM-2.*CP(IX)*CI(JX)/(AP(IX)+A1(JX))+(AP(IX)+A1(JX))/T
6510  244  SUM=SUM-CP(IX)*CI(JX)/(A1(IX)+A1(JX))
6520  SUM=SUM+CI(IX)*CI(JX)/(A1(IX)+A1(JX))
6530  IF((A1(IX)+A1(JX))<0.) GO TO 242
6540  SUM=SUM+CI(IX)*CI(JX)/(A1(IX)+A1(JX))+(A1(IX)+A1(JX))/T
6550  242  CONTINUE
6560  TSUM=SUM/T
6570  SUM=SUM/T
6580  SUM=SUM/T
6590  SUM=SUM/T
6590 PRINT,"NORM="SUMNOR
6600 PRINT,
6610 TNorm=TSum/SUMNOR
6620 PRINT,
6630 PRINT,"MEAN SQUARED ERROR="TSum
6640 PRINT,
6650 PRINT,"NORMALIZED MSE="TNorm
6660 STOP
6670 END
MISSION

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