TECHNICAL NOTE

LOADING ANALYSIS OF
CONTROL GROUP CMOS ICs IN
TORPEDO MK 46 MOD 5 (NEARTIP)

December 1977

Prepared for
NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152
Under Contract N00123-76-C-0797

Publication W77-1640-TN03

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LOADING ANALYSIS OF CONTROL GROUP CMOS ICs IN TORPEDO MK 46 MOD 5 (NEARTIE)

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UNCLASSIFIED/UNLIMITED
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SUMMARY

A loading analysis of CMOS integrated circuits in the Control Group of Torpedo Mk 46 Mod 5 (NEARTIP) was performed for the Naval Ocean Systems Center. The analysis, which included documenting loads and calculating rise times for about 1400 CMOS outputs, revealed no problems related to CMOS fanout or rise time.
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INTRODUCTION

As a task under Contract N00123-76-C-0797, ARINC Research Corporation conducted a loading analysis of CMOS integrated circuits in the Control Group of Torpedo Mk 46 Mod 5 (NEARTIP). The purpose of the investigation was to help ensure that the torpedo system will not be degraded because of CMOS loading problems.

This report documents all CMOS fanout numbers and related application factors in the NEARTIP Control Group circuits. Input information to the study included Control Group schematics, change authorizations (CAs) related to revisions of the schematics, direct inputs from Naval Ocean Systems Center personnel, and ARINC Research and Honeywell technical reports.

In this report, applicable documents are listed in Section 2; data compilation and documentation are described in Section 3; the determination of IC output rise time is discussed in Section 4; results of the loading analysis are presented in Section 5; and conclusions and recommendations are given in Section 6.
Source documents for the loading analysis of CMOS ICs in the NEARTIP Control Group are listed below.

a. Control Group Schematics

<table>
<thead>
<tr>
<th>NEARTIP Schematic</th>
<th>Revision Letter</th>
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<td>D</td>
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<td>3235523</td>
<td>E</td>
</tr>
<tr>
<td>3235524</td>
<td>D</td>
</tr>
</tbody>
</table>


e. ARINC Research Corporation, Design Analysis Reports (DARs), prepared under Contract N00123-76-C-0797.

f. NAVSEA 0967-LP-597-1010, Table VII.
DATA COMPILATION AND DOCUMENTATION

For the CMOS IC loading analysis, data from about 475 ICs having about 1425 individual outputs and 5000 loads were recorded. This section describes how the data were compiled and documented.

3.1 CMOS INTERCONNECT DATA

CMOS IC interconnections were identified for every IC output in the 19 schematics of the NEARTIP Control Group. The data include reference designator, section number, pin number, and associated loads for each IC output. The loads include CMOS ICs, resistors, and capacitors. For the identified loads, the reference designator, section number, and pin number are also recorded. These data are presented in Appendix B and illustrated in Table 1 for a portion of the data from Control Group schematic no. 3235514.

3.2 CMOS LOADING DATA

Recorded for every IC output on each of the 19 Control Group schematics were the IC number, output pin number, loads, number of CMOS loads, and rise time (at 70°C) where thought to be significant. These data are presented in Appendix A and illustrated in Table 2 for a portion of Control Group schematic no. 3235514.
### TABLE 1. EXAMPLE OF INTERCONNECT DATA FROM APPENDIX B

<table>
<thead>
<tr>
<th>A5A2</th>
<th>A5B4</th>
<th>A5C6</th>
<th>A5D10</th>
<th>A5E12</th>
<th>A5F15</th>
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<tr>
<td>A6D13</td>
<td>D7A5</td>
<td>D6B9</td>
<td>G7B10</td>
<td>B6D12</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C8A2</td>
<td>C8B4</td>
<td>C8C6</td>
<td>C8D10</td>
<td>C8E12</td>
<td>C8F15</td>
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<td>D8C13</td>
<td>A7B5</td>
<td>B6D13</td>
<td>B5A3</td>
<td>24</td>
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<tr>
<td>D7B9</td>
<td>A7A2</td>
<td>B6B5</td>
<td>D7A2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G7B11</td>
<td>B6C9</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Schematic No. 3235514)

(1) Referring to IC C8D10 (block-enclosed for illustrative purposes), "C8" is the IC's reference designator, "D" is the IC section, and "10" is the IC's output pin number. Below the line are five CMOS loads connected to output pin 10.

(2) For CMOS IC A5F15, the value 49 is shown encircled. The 49 is a pin number on the board connector, and the circle indicates that the reference load is physically located on a different NEARTIP board. The total load is documented in Appendix A.
### TABLE 2. EXAMPLE OF LOADING DATA FROM APPENDIX A

<table>
<thead>
<tr>
<th>Reference IC Number</th>
<th>Pin Number</th>
<th>Total Load</th>
<th>Number of CMOS Loads</th>
<th>Rise Time, $10^{-6}$ sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8</td>
<td>2</td>
<td>4013</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>4023, 12, 13</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>4023</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>4011, 23, 11, 12, 11</td>
<td>5</td>
<td></td>
</tr>
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<td></td>
<td>12</td>
<td>4027, 23</td>
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<td></td>
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<tr>
<td></td>
<td>15</td>
<td>(4049, 23, 23)</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

(1) On C8D10 (note enclosed entry in Table 1, which is pin 10 in Table 2), the five CMOS loads are 4011, 4023, 4011, 4012, 4011. If the rise time was significant it would be listed in the last column. Had part of the load been resistive or capacitive, that would be listed in the Total Load column.

(2) Pin 15 has its total load shown in parenthesis, which indicates that the load is on a different NEARTIP board.
DETERMINATION OF IC OUTPUT RISE TIME

For calculation of the rise time of IC outputs, much of the input data was provided by the Honeywell letter report, "CD4000 Series Input Capacitance Study", dated 2 December 1976. That report, reproduced herein as Appendix C, provided data on CMOS output transition time, input capacitance, and dynamic impedance.

Rise times of ICs in the NEARTIP system were calculated from the external IC load and the internal dynamic impedance of the IC output. The equation is:

\[ T_{R(NT)} = 2.2(Z_{o(int)} + R_{ex})(C_{ex}) \]  

where:

- \( T_{R(NT)} \) = Rise time (NEARTIP) from 10% to 90% of the output wave shape
- \( Z_{o(int)} \) = IC internal dynamic impedance
- \( R_{ex} \) = Any resistance external to IC
- \( C_{ex} \) = Any capacitance external to IC.

\( Z_{o(int)} \) is calculated as follows:

a. The transition time (\( T_t \)) of the chip into a 50 pf load is given in Table 2 of Appendix C.

b. Then, from equation 1,

\[ T_t = 2.2 Z_{o(int)} C_{ex} \]

from which

\[ Z_{o(int)} = \frac{T_t}{2.2 \times 50 \, \text{pf}} \]  

(2)
With $Z_{\text{o(int)}}$ now known and $R_{\text{ex}}$ and $C_{\text{ex}}$ known from the loading analysis, $T_{\text{R(NT)}}$ can be calculated from equation 1.

As an example, consider the NEA RTIP CMOS device S/N 4001. From Table 2 of Appendix C, its transition time is 80 nanoseconds with a 50 pf load at 25°C. The transition time increases $0.3^\circ/{ }^{\circ}$C since from equation 2, $T_t$ is directly proportional to $Z_{\text{o(int)}}$, values for which appear in Appendix C, page C-4. At 70°C the transition time is:

$$T_t = (80 \times 10^{-9} \text{ sec}) \left[ (1 + \frac{0.3}{50}) (70^\circ - 25^\circ) \right]$$

$$= 90.8 \times 10^{-9} \text{ sec}$$

or an increase of 10.8 nanoseconds from its value at 25°C. Then, from equation 2,

$$Z_{\text{o(int)}} = \frac{90.8 \times 10^{-9} \text{ sec}}{2.2 (50 \times 10^{-12} \text{ f})} = 825 \Omega$$

Assume an external load of 80 pf on the output of the example device. The rise time, from equation 1, is

$$T_{\text{R(NT)}} = 2.2(825 + 0)(80 \times 10^{-12} \text{ F}) = 0.145 \times 10^{-6} \text{ sec}.$$
RESULTS OF LOADING ANALYSIS

Results of the loading analysis of CMOS ICs in the NEARTIP Control Group are summarized in this section. Complete data are presented in Appendix A.

5.1 LOADING AND RISE TIME CHART

For CMOS IC outputs having more than nine loads, Table 3 shows the number of loads and the associated rise time. NOSC designated a fanout of nine for CMOS ICs as a design goal for NEARTIP.

TABLE 3. CMOS OUTPUTS WITH MORE THAN NINE LOADS

<table>
<thead>
<tr>
<th>Drawing No.</th>
<th>IC Number</th>
<th>Number of CMOS Loads</th>
<th>Rise Time, $10^{-6}$ sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>3235513</td>
<td>B7 Pin 1</td>
<td>12</td>
<td>0.156</td>
</tr>
<tr>
<td>3235513</td>
<td>B7 Pin 13</td>
<td>16</td>
<td>0.22</td>
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<tr>
<td>3235514</td>
<td>C7 Pin 6</td>
<td>17</td>
<td>0.36</td>
</tr>
<tr>
<td>3235515</td>
<td>C8 Pin 12</td>
<td>11</td>
<td>0.145</td>
</tr>
<tr>
<td>3235519</td>
<td>A7 Pin 11</td>
<td>12</td>
<td>0.2</td>
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<td>3235519</td>
<td>C8 Pin 12</td>
<td>32</td>
<td>0.6</td>
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<tr>
<td>3235519</td>
<td>F5 Pin 15</td>
<td>13</td>
<td>0.3</td>
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<tr>
<td>3235521</td>
<td>B6 Pin 1</td>
<td>36</td>
<td>1.15</td>
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<td>3235521</td>
<td>C8 Pin 2</td>
<td>13</td>
<td>0.36</td>
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<td>3235521</td>
<td>D6 Pin 10</td>
<td>20</td>
<td>0.37</td>
</tr>
<tr>
<td>3235522</td>
<td>D4 Pin 10</td>
<td>16</td>
<td>0.32</td>
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<td>3235522</td>
<td>E7 Pin 2</td>
<td>10</td>
<td>0.301</td>
</tr>
<tr>
<td>3235523</td>
<td>D9 Pin 12</td>
<td>10</td>
<td>0.135</td>
</tr>
</tbody>
</table>

Since none of the ICs analyzed have resistive loads that stress their output current capability (most devices are operating at less than 20% of their maximum current rating at 25°C), resistive loads are not included in Table 3.
5.2 RISE TIME ANALYSIS

Clock rates within the NEARTIP Control Group will generally determine what rise time between the IC output and input will be adequate. To ensure proper operation of some ICs, the individual IC may have a specified rise time required at the input. Both of these points will now be addressed.

Excluding the SAC board (Assy No. 3235508), the fastest clock time in the Control Group is 5 kHz. The period for a 5 kHz cycle is 0.20 milliseconds. Using a translation factor of 6, from ref. d of Section 2 (as low as 3 would be acceptable), the minimum rise time for a chip input is \((0.20 \times 10^{-3})/6\) or 0.033 millisecond. Since no rise time greater than 4 microseconds was found in the Control Group, there are no potential clocking problems. In fact, a safety factor of \((0.33 \times 10^{-3})/(4 \times 10^{-6}) = 8\) exists with respect to a possible clocking problem.

The Honeywell report (Appendix C) states that the slowest rise time in the NEARTIP system should be 1.5 microseconds. This calculation was derived from worst-case conditions for all components that affect rise time.

The four ICs with a calculated rise time greater than 1.5 microseconds were examined. The CMOS loads of each were checked to determine if a slow rise time could affect their operation. Table 4 identifies these ICs and their rise times.

**TABLE 4. ICs WITH RISE TIMES GREATER THAN 1.5 MICROSECONDS**

<table>
<thead>
<tr>
<th>Dwg. No.</th>
<th>Chip No.</th>
<th>Output Pin No.</th>
<th>CMOS Output Rise Time, (\mu)sec</th>
<th>CMOS Loads</th>
</tr>
</thead>
<tbody>
<tr>
<td>3235505</td>
<td>1E</td>
<td>12</td>
<td>3.27</td>
<td>4023</td>
</tr>
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<td>3235505</td>
<td>2A</td>
<td>2</td>
<td>3.30</td>
<td>4011, 12</td>
</tr>
<tr>
<td>3235702</td>
<td>C10</td>
<td>1</td>
<td>1.85</td>
<td>4013, 13</td>
</tr>
<tr>
<td>3235520</td>
<td>G4</td>
<td>1</td>
<td>3.45</td>
<td>4012</td>
</tr>
</tbody>
</table>

In discussions with an ARINC Research representative, application engineers of RCA and National Semiconductor agree that CMOS devices 4023, 4011, and 4012 are not sensitive to slow input rise times. Factory specification sheets and NEARTIP SIDs do not specify these three CMOS input rise times.

The 4013 chip requires a minimum rise time of 3 microseconds for its clock input. Inputs to the 4013s listed in Table 4 go to the set and reset pins. These inputs do not
require a specific rise time. If the input is present 20 nanoseconds before the clock signal arrives, as is the case in NEARTIP, the chip will operate properly.

The SAC board has an internal oscillator with a resonant frequency of about 240 kHz. Where rise time is important on the SAC board, the chips are interconnected directly to ensure operation at the higher frequency. The highest approximate frequency to enter and leave the SAC board is 5 kHz, which is well within the operating frequency of the board.

The analytical concepts used in the Honeywell report (Appendix C) and in this report are the same. However, ARINC used specific cases in its calculations where Honeywell used an absolute worst case in its calculations. If a worst case had actually occurred, ARINC would have noted and documented it in this report.

In summary, the rise time of CMOS ICs in the control group do not appear to represent a problem.

5.3 CMOS FANOUT ANALYSIS

Table 3 shows that certain CMOS loads in the NEARTIP Control Group range from 10 to 36. The question arises as to how many loads a CMOS IC should have in the NEARTIP system. The Honeywell report (Appendix C) recommends only nine because of rise time constraints. However, it has been shown (Section 4.2) that rise time is not a problem, even on the IC with a fanout of 36. If rise time is the only limitation, then none of the CMOS ICs in the Control Group are fanout-limited.

NAVSEA 0967-LP-597-1010, Table VIII, recommends that a fanout on digital microcircuits be limited to 70 percent of manufacturer rating. If rise time is not a constraint, device manufacturers generally state that a fanout of 100 is acceptable. Since 70% of that value is 70, the worst case fanout of 36 from Table 3 would still have a safety margin of approximately 2-to-1.

From a mission completion point of view, it may be preferential to spread the risk of not completing a mission among different outputs instead of having as many as 36 outputs coming from the same IC. If this is a concern, then a separate study should be implemented to investigate the costs and effectiveness tradeoffs associated with applications of redundant signal paths.
In summary, overloaded outputs on CMOS devices in the NEARTIP Control Group do not appear to represent a problem.
CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSIONS

The overall conclusions drawn from this study are the following:

a. Of the 1,425 CMOS circuits analyzed, 13 ICs had a fanout of greater than nine, and four had an output rise time of greater than 1.5 microseconds.

b. A fanout of nine and a rise time no greater than 1.5 microseconds, considered as limiting values by Honeywell (see Appendix C), are not applicable to the CMOS circuits in the NEARTIP Control Group.

c. The design goal for fanout of CMOS devices in the NEARTIP Control Group, also nine, is extremely conservative.

d. All factors considered, there are no problems relating to fanout or rise time in CMOS devices in the NEARTIP Control Group.

6.2 RECOMMENDATION

ARINC Research recommends that no action be taken at this time to reduce the loading effects of CMOS IC outputs in the NEARTIP Control Group.
## APPENDIX A

CMOS IC OUTPUT LOADING DATA

<table>
<thead>
<tr>
<th>Control Group Schematic Number</th>
<th>Page</th>
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*The symbol "||" denotes "in parallel with".*
<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>TOTAL LOAD</th>
<th>CMOS LOADS</th>
<th>RISE TIME 10⁻⁶ SEC</th>
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</thead>
<tbody>
<tr>
<td>IC #</td>
<td>PIN #</td>
<td>LOAD</td>
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</tr>
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<td>(4001,49)</td>
<td>2</td>
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APPENDIX C
HONEYWELL CD 400 SERIES
INPUT CAPACITANCE STUDY

(Reproduction of Honeywell letter report of
2 December 1976)
S1MMARY

This study was undertaken to determine the input capacitances for CD4000 series CMOS devices used in NEUTIP. Vendor data sheets, MIL-M-38510, and visits to National and Motorola were utilized to compile a listing of input capacitance values. These values, together with device output impedance specifications, were used to compute worst-case pulse rise and fall time values. From this it was found that the gate loading design guideline being used by NEC has a 3:1 safety factor, and there should not be any problems related to capacitive loading of CMOS gates in NEUTIP hardware.

DISCUSSION

The study was begun by compiling a list of vendor data obtained from catalog data sheets. There was a wide disparity of values resulting from this study: for example, on the CD4006 a ratio of 5:1 exists in the CLOCK input capacitance values. Therefore, visits were made to National and Motorola CMOS facilities in order to obtain actual input capacitance data and to obtain first-hand information on the nature and character of CMOS input capacitance.

The data obtained from National and Motorola, plus catalog and MIL-M-38510 data is shown in Table 1. Note that both National and Motorola supplied data for relatively few devices; however, they consider these values typical of a broad spectrum of product. For example the Motorola 4002 and 4012 data is typical of all gate inputs. In addition to actual data both Motorola and National supplied "estimates" of typical input capacitance for the device types. Motorola was more specific in this, although the value for the 4012 does not correlate with actual data given. National supplied a less specific listing, specifying most devices as 4-5.5 pf, and no data for those devices which would tend to run higher.

National furnished the best treatise on the makeup of input capacitance: a discussion by John Jorgensen, CMOS Design Manager. Input capacitance is composed of the sum of the capacitances associated with the:

- Package (0.8 to 1.7 pf)
- Input protection diode to VGSS (1 to 2 pf)
- Inverter stage (1 to 2 pf)
In addition to the above, there are gate-drain and gate-source capacitances associated with the P and N channel transistors of the input inverter stage. The gain of this stage is 10-20, and this results in a capacitance multiplication factor as the device switches through threshold. Figure 1 illustrates this for a 4601 B (CM001) device switched from a "0" input to "1" input at \( V_{pp} = 15 \) V. Integrating under the curve results in \( C_1 = 3.1 \) \( \mu F \) compared to \( 3.04 \) \( \mu F \) measured on a steady-state basis. This characteristic becomes even more pronounced at \( V_{pp} = 5 \) V (see appendix A data sheet).

Both National and Motorola were asked the following questions, with both furnishing essentially the same answers:

1. Is \( C_1 \) affected by \( V_{pp} \)? Ans. Not significantly.
2. Is \( C_1 \) affected by temperature? Ans. Not significantly.
3. What is the typical output impedance of the devices? Ans. No one has ever asked about this - consult data sheets for rise/fall times and output voltage vs. current sinking capability.
4. What is the effect of \( V_{pp} \) on output impedance? Ans. Referring to output rise and fall times, if these are given at \( V_{pp} = 5 \) V then use \( t_r \) and \( t_f \) values divided by 4 to obtain 15 V values. If \( V_{pp} \) is given as 10 V, then divide by 1.25.
5. What is the effect of temperature on output impedance? Ans. +0.5\%/°C. (Represents +13.8\% at +71°C.)
6. What are the typical clock rise time or pulse input rise times on the devices which have such requirements? Ans. Consult data sheets. Data shown represent at least a 2:1 safety factor, when operating voltage is factored in as shown in question 4.
7. What is your MIL-STD-883 Level B capability? Ans. Answers to this question differed greatly. National has all product available to 883 Level B. Motorola does not have any product available. They have just acquired the necessary test equipment (term chambers, dynamic test gear, etc.) and plan to have some product available first quarter 1977. Other product will follow throughout 1977.
8. What is the future availability of types not now produced? (Motorola question only: National produces all, if the 4070 can be substituted for the 4030.) Ans. Motorola does not plan to produce the missing devices. (4019, 4029, 4047, and 4048).
9. Do you have any application notes regarding AC operation of CMOS? Ans. Neither had any specific notes or suggestions to offer, referring instead to previously published notes by RCA and Harris, and to magazine articles.
National and Motorola personnel contacts are listed in Appendix A, along with data sheets furnished by each.

Table 2 illustrates the Motorola, National and RCA catalog data maximum transition times of each CMOS type. These are all specified for a 50 pf load and 15 V operation, except as noted. Therefore, an estimate of output impedance can be derived, and thereby a calculation of the maximum allowable capacitance (or gate loads) for a given rise time requirement can be made. Data for the CD4019 and CD4029 was obtained from Fairchild CMOS data sheets.

Following is a calculation of a worst-case capacitance load:

- Maximum transition time in Table II: 150 nsec (4013, 4027, 4042)
  Increase for 71°C: (71°C - 25°C times 0.3%/°C) = 1.138 X 150 = 147.94 = 148 nsec.
- Compute number of RC time constants for 10% to 90% pulse amplitude:
  10% = .105 RC; 90% = 2.3 RC; therefore, 10% to 90% rise time is 2.2 RC.
- Compute maximum output impedance: 148 X 10^-9 = 2.2 X R X 50 X 10^-2
  \[ R = \frac{1345 \text{ ohms}}{2.2} \]
- Maximum rise time allowed on CMOS prints is 3 microseconds; applying a 2:1 safety factor this becomes 1.5 microseconds. Compute the maximum capacitive load the 1345 ohm output impedance can drive without degrading the rise time above 1.5 microseconds:
  \[ 2.2 \times 1345 \times C = 1.5 \times 10^{-6} \]
  \[ C = \frac{507 \text{ pF}}{2.2} \]
- Maximum gate load in Table I: 20 pf (4049) (Motorola estimates this at 17-19 pf, they are changing their data sheet to specify 20 pf, maximum.) Calculate number of CM049 inputs a CD4013, 4027 or 4042 could drive:
  \[ N_g = \frac{507}{20} = 25 \]

The next worst case load in Table I is the 12 pf maximum specified by MIL-M-38510. On this basis 42 loads could be driven. For a typical gate input such as the National CD4020, and rounding 4.7 pf to 5 pf, over 100 loads could be driven.

Therefore the 9 loads specified by MAC as a design goal is very conservative, representing at worst a 3:1 safety factor.
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4. A = ANY INPUT
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APPENDIX A  NATIONAL AND MOTOROLA PERSONNEL CONTACTS AND CMOS DATA SHEETS.

National (Santa Clara, Ca.)

Sharon (San) O’Connell - Military/Aerospace Marketing Manager, 408-737-5880
Bob Bennett - CMOS Product Marketing Manager 408-732-5000
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Rick Goeld - Production Manager, 512-928-2600
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Mike Hadley - CMOS Applications Engineer, 512-928-2600