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RADIO CORPORATION OF AMERICA
RCA LABORATORIES

EVAPORATED THIN FILM DEVICES

BY

P. K. WEIMER
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V. E. HENRICH
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NOVEMBER 30, 1962

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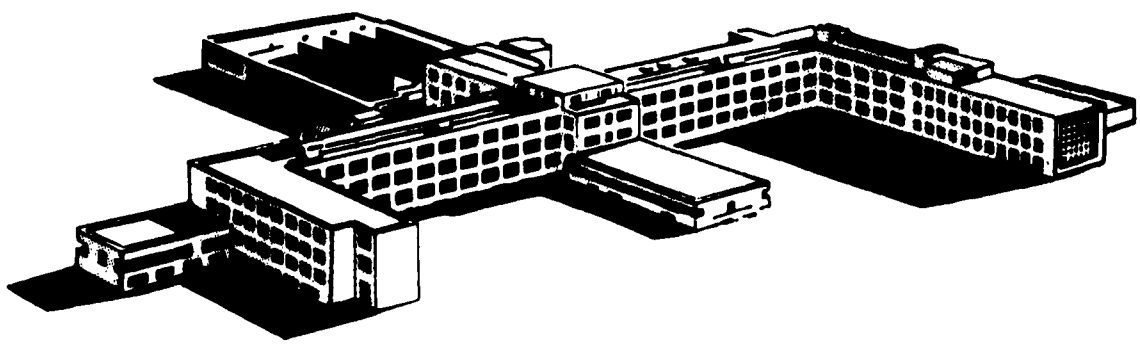
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
OFFICE OF AEROSPACE RESEACH
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS



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ABSTRACT

Additional evidence is presented to show that the dominant current control mechanism in the insulated-gate cadmium sulfide thin film transistor (TFT) is conductivity modulation in the semiconductor by field effect action of the gate. Good agreement has been found between the observed drain characteristics and those predicted by a field-effect analysis. The characteristics of the coplanar-electrode TFT having overlying "ohmic" contacts were demonstrated to be equivalent to the earlier staggered-electrode structure having underlying gold contacts. Experimental tests on cadmium sulfide TFT structures incorporating Hall electrodes showed systematic differences between the measured Hall mobility and the measured drift mobility. The measured drift mobility as calculated from the ratio of transconductance to input capacitance may be either higher or lower than the measured Hall mobility depending upon the method of preparation of the semiconductor film. An increase in the Hall mobility as a function of positive gate bias was found, contrary to predictions based upon the effect of scattering at the surface of a homogeneous semiconductor. To explain these two anomalies a nonhomogeneous film structure was postulated, consisting of relatively conducting crystallites of cadmium sulfide surrounded by insulating barriers. Measurements on input capacitance, switching speeds, and the temperature dependence of drain characteristics and Hall mobilities were made. Tests on various processing procedures and electrode contacts were carried out for cadmium sulfide and other materials potentially useful for TFT fabrication.

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I. INTRODUCTION

The insulated-gate thin-film transistor (TFT), which has been developed at RCA Laboratories during the past several years[1-4], continues to present challenging problems. Although the basic operation of the "standard" TFT is now largely understood, many subtle aspects of the performance characteristics remain to be clarified. In Section II of this report recent experiments on various types of evaporated TFT structures provide new evidence on the current-control mechanisms involved.

A persistent anomaly in the performance of the TFT utilizing polycrystalline cadmium sulfide has been that the measured ratio of transconductance to input capacitance has often appeared to exceed that expected from the measured Hall mobilities in the film. In Section III measurements upon TFT structures incorporating Hall electrodes are described. The existence of an insulating barrier between conducting crystallites of the CdS is proposed to account for the observed increase of Hall mobility with gate voltage and the lack of agreement with the measured Hall mobility and the effective drift mobility.

In Section IV a field-effect analysis of the insulated-gate TFT structure for drain voltages up to the point of saturation is presented. The calculated characteristics are found to agree closely with the measured characteristics of the TFT.

Section V reports test results on experimental TFT's at room temperature and over a range of temperatures. Drain characteristics, switching speeds, and input capacitance as a function of gate bias have been measured.

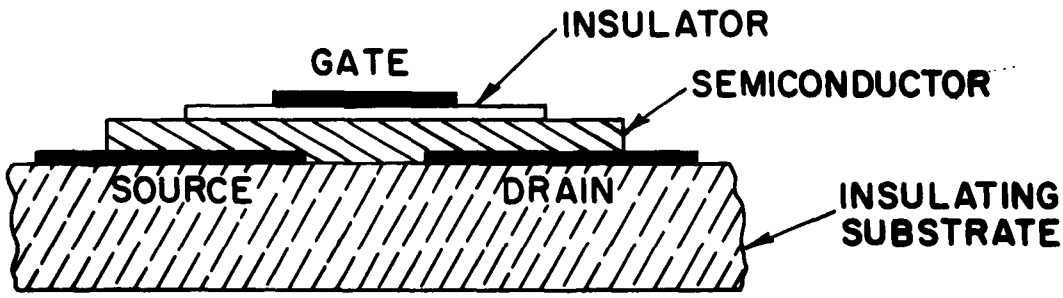
A continued objective of the present research program is to attain the performance with evaporated TFT's which can be reached in single crystal devices. In Section VI an outline of current studies on thin-film materials, electrode contacts and processing procedures is given.

II. CURRENT-CONTROL MECHANISMS IN THE INSULATED-GATE TFT

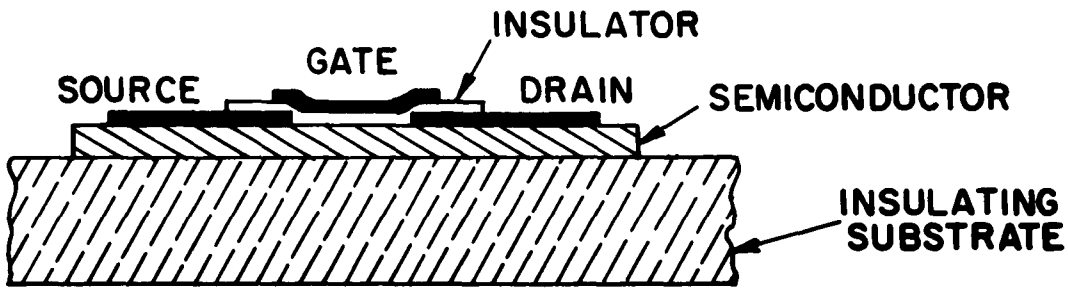
In the basic paper[3] on the thin-film transistor it was proposed that the dominant current-control mechanism for a high-performance TFT having saturated pentode-like characteristics was the modulation by field effect of the carrier density in the cadmium sulfide surface near the insulator interface. Since that paper was written, additional experience at RCA Laboratories has been overwhelmingly in support of this viewpoint[4]. Recently, a paper[5] from another laboratory has rejected this view in favor of the control of injection efficiency at the source as being the dominant mechanism. In the present section these alternative mechanisms will be discussed and additional evidence will be presented in support of conductivity modulation as being the primary control mechanism in the "standard" TFT structures. At the same time alternative conditions will be described wherein other mechanisms may play a role.

Two insulated-gate TFT structures whose cross-sections are shown in Fig. 1 will be considered. In Fig. 1a the source and drain are on opposite sides of the semiconductor from the gate, while in Fig. 1b all electrodes are on the same side. The performance of the two structures is substantially identical; each can be designed for operation in either the enhancement or the depletion mode. Figures 2a and 2b show typical enhancement-type characteristics for the staggered and planar geometries, respectively, and Figs. 3a and 3b show depletion-type characteristics. Each "depletion-type" unit will also operate in the enhancement mode, the transition from depletion to enhancement operation in either structure occurring very smoothly as the gate potential is changed from negative to positive bias. The so-called "enhancement-type" units will not operate well in the depletion mode since drain current is essentially zero at zero gate bias.

There is no doubt that the depletion-type units are field-effect devices operating by the modulation of conductivity in the conduction channel between source and drain much the same as in a conventional field-effect transistor. The depletion-type TFT's differ from the enhancement-type units only in that a conducting skin or accumulation layer is already present on the surface of

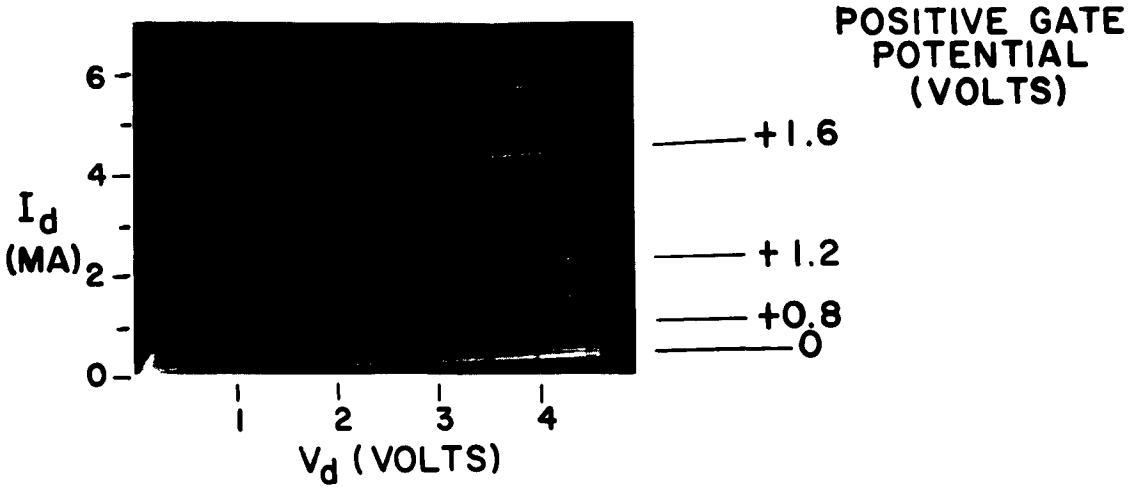


(a) TFT with Staggered Electrode Structure

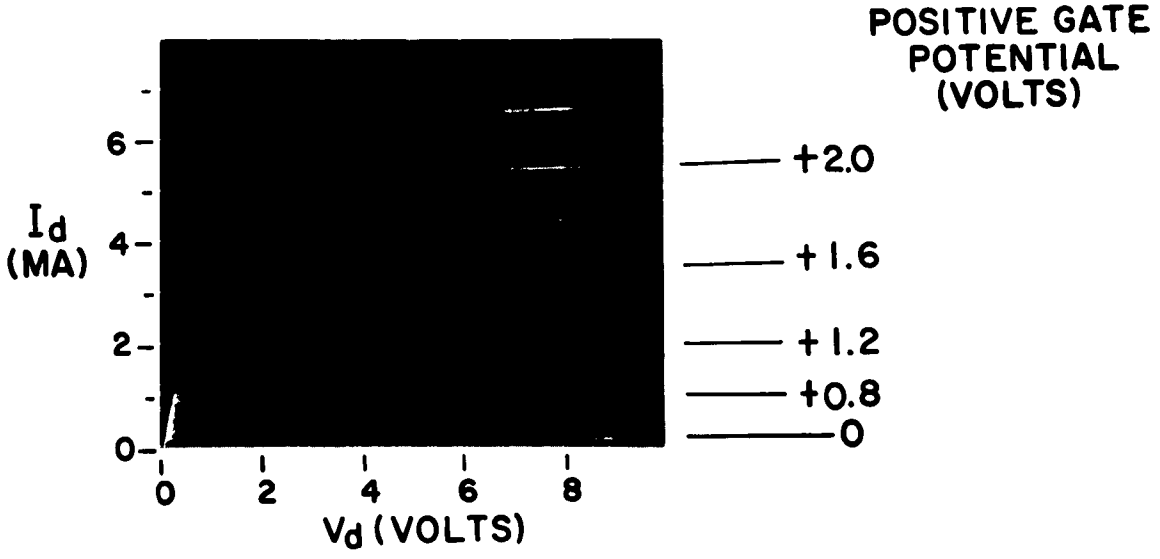


(b) TFT with Coplanar Electrode Structure

Fig. 1 Cross-Section of Two Insulated-Gate TFT Structures

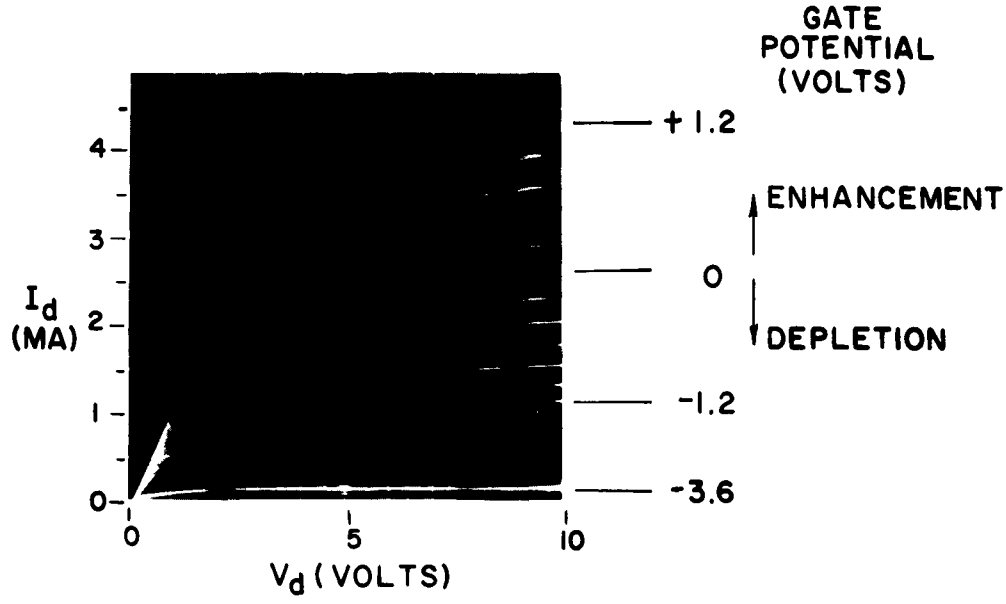


(a) Staggered Electrode TFT (Underlying Gold Source and Drain)

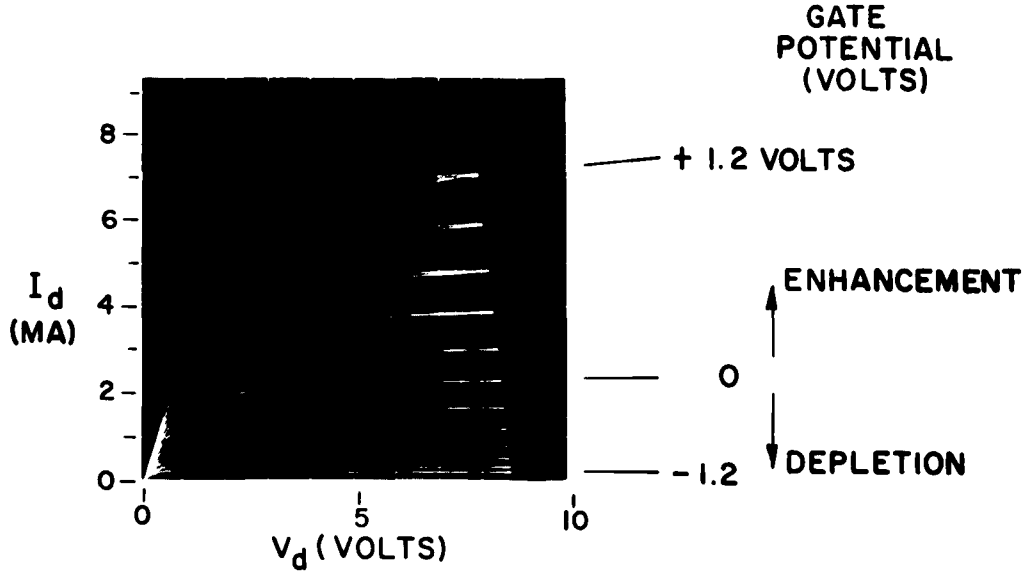


(b) Coplanar Electrode TFT (Overlying Indium Source-Drain Contacts)

Fig. 2 Enhancement-Type TFT's



(a) Staggered Electrode TFT (Underlying Gold Source-Drain)



(b) Planar Electrode TFT (Overlying Electrodes)

Fig. 3 Depletion-Type TFT's

the CdS at zero gate bias. By adjusting the gate potential either positively or negatively with respect to the source, the carrier density in this conducting channel can be increased or decreased. The saturation of drain current at high drain voltage arises from the pinch-off of current in the neighborhood of the drain just as in the usual field-effect transistors. The pentode-like characteristics of the conventional field-effect transistor has been discussed many years ago by Shockley[6], and a partial analysis of the effect is given in Section IV of this report.

In an enhancement-type unit the CdS surface is initially more insulating, the drain current at zero gate bias being only a few microamperes. In a good unit the drain current can be increased by a factor of 10^3 or more when the gate is biased several volts positive with respect to the source. This increase may be explained as follows in terms of conductivity modulation. Let us assume for the moment that the source electrode makes a low-impedance contact with the cadmium sulfide whose resistivity is relatively high, say 10^4 ohm-cm. Although an ample supply of electrons exists at the source, these electrons do not continue to pour into the CdS when the gate is at zero bias because of space charge repulsion. Now if the gate voltage is increased to some positive value V_g, the total number of carriers drawn in from the source is

$$n = \frac{C_g V_g}{e} \tag{1}$$

where C_g is the total gate capacitance and e is the electronic charge. A conducting channel is formed electronically as an accumulation layer on the surface of the CdS. The lateral flow of current in this channel provides the conduction path between source and drain at positive gate biases. The induced channel produced by the positive gate is subject to the same pinch-off condition in the neighborhood of the drain as that which gave rise to saturation in the depletion-type units. Thus pentode-like characteristics will be found for the enhancement mode just as for the depletion mode, and a smooth transition from depletion to enhancement operation is to be expected.

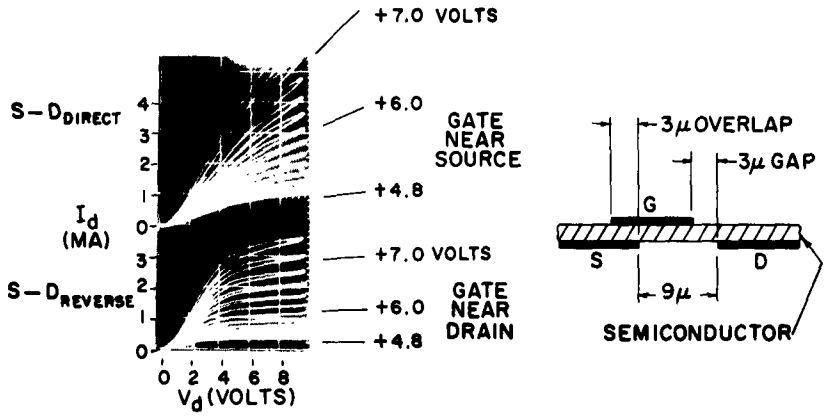
The complete similarity of performance of the coplanar TFT's having "ohmic" contacts (indium at the source-drain interfaces) and the staggered TFT having the underlying "quasi-ohmic" gold contacts[12] provides strong evidence that the primary current control mechanism is not the modulation of injection efficiency from the source as suggested in reference 5. In the coplanar structure the field from the gate cannot reach a significant distance along the underside of the source (because of the small thickness of the CdS), leading to the expectation that emission modulation should be even less significant in the coplanar structure than in the staggered structure. The basis for the suggestion that emission modulation was required in the TFT probably stems from the knowledge that a gold source electrode in contact with cadmium sulfide may not be completely ohmic but is often somewhat blocking. This fact was recognized in the original design of the staggered electrode structure of Fig. 1a, where it was found somewhat advantageous to allow the gate electrode to overlap the source. The result of the overlap was to extend the induced channel out over the source, thus increasing the effective area of the source contact. Numerous tests, however, in which the degree of overlap of gate and source were varied showed only a moderate increase in maximum transconductance with gate overlap (often less than a factor of two).

Figure 4a shows the characteristics of an enhancement-type staggered unit whose gate overlaps one gold electrode but fails to reach the other gold electrode. This unit can be tested with the overlapped electrode acting either as the source or as the drain. The g_m is only slightly higher when the source is overlapped, and the saturation is much poorer owing to the gap at the drain end. This test shows that the source contact need not be completely ohmic provided the contact impedance is already low compared to the channel impedance. It shows further that the modulation of emitter efficiency which should be greatly increased when the gate is closer to the source (if this were the primary mechanism) is a relatively small effect compared to the conductivity enhancement factor of at least two orders of magnitude by which the positive gate can increase the current between source and drain. The

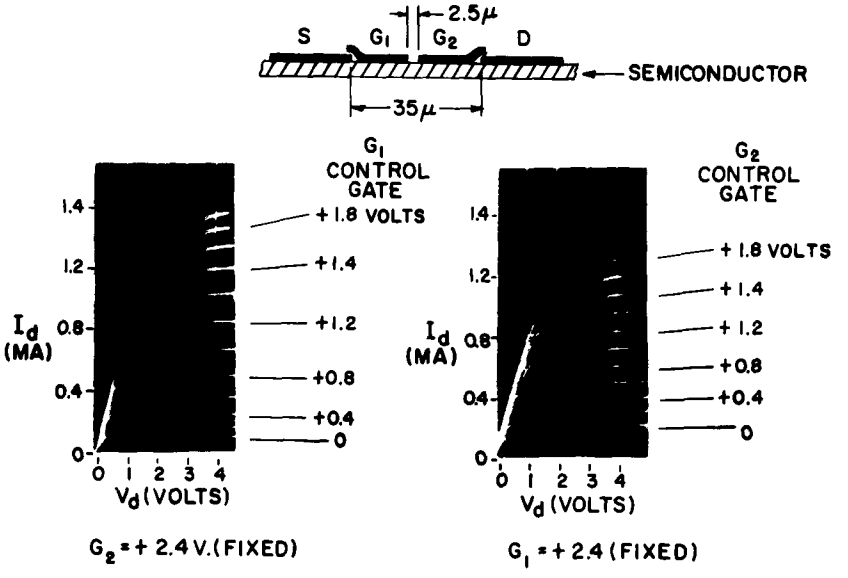
poorer saturation observed in Fig. 4a when the gate does not reach the drain would be expected on the basis of the field-effect explanation for saturation. If one denies the existence of the conductivity-modulation effect in the TFT in favor of an emission modulation at the source, he will be forced to provide a new saturation mechanism to explain its pentode-like characteristics.

Figure 4b shows the characteristics of a two-gate coplanar-type TFT operating in the enhancement mode under two conditions of gate drive. In the picture on the left the gate G_1 (nearest the source) is modulated with voltage steps ranging from zero to 2.0 volts while the gate G_2 (nearest the drain) is held at a fixed positive potential of 2.4 volts. In the picture at the right G_1 is held at a fixed positive potential while G_2 is modulated. The similarity of the two curves provides additional evidence that conductivity modulation in the region between source and drain represents the major control mechanism in the TFT.

The suggestion has frequently been made that one is dealing entirely with space-charge-limited currents in the enhancement-type TFT. This could be true only if the source and drain were spaced sufficiently close together (or the drain voltage were sufficiently high) so that the field from the drain could reach under the gate all the way to the source. Under these conditions the induced channel would not be formed at the interface and one would expect to obtain unsaturated triode-like characteristics instead of the pentode characteristics. Such triode-like characteristics have been assumed by Atalla[7] in a recent patent describing a silicon space-charge-limited insulated gate triode. In the usual pentode-like TFT's, however, the current flow in the induced channel under the gate is ohmic, although the current flow in the narrow high-field region next to the drain may be regarded as "emission-limited" in the same sense that the electron flow between the screen grid and the plate of a vacuum pentode is emission-limited. The failure to observe saturation in a TFT cannot, of course, be interpreted as proof of the existence of a space-charge-limited triode since many other spurious factors may prevent saturation[3].



(a) Off-Center Gate Operated with Gate Overlapping Source (direct connection) or Gate Overlapping Drain (reverse connection)



(b) Double Gate TFT Operated with Control Gate Close to Source (left) or Control Gate Close to Drain (right)

Fig. 4 Operating Characteristics of Experimental TFT's

III. MOBILITY STUDIES IN THIN-FILM MATERIALS

A. EXPERIMENTAL MEASUREMENTS (First Quarter)

The performance of an enhancement-type insulated-gate TFT as measured by the ratio of its transconductance to input capacitance would be expected to depend upon the carrier drift mobility in its semiconductor layer according to the following relation[1]:

$$\frac{g_m}{C_g} = \frac{\mu_D V_d}{L^2} \tag{2}$$

where g_m is the transconductance

C_g is the gate capacitance

μ_D is the drift mobility in the semiconductor

V_d is the drain voltage

L is the source-drain spacing, also equal to gate "length".

Equation (2), which is based upon the approximate field-effect analysis of reference (1), is valid only in the unsaturated part of the characteristic where $V_d < V_g$. Equation (2) can be used to calculate an effective value of the drift mobility μ_D since all other terms in the expression can be measured independently. When such calculations have been made, however, the value of μ_D obtained has been inconsistent with the Hall mobility μ_H measured on other CdS films prepared in a similar manner. While a value of μ_D less than μ_H could readily result from trapping effects, it was surprising to obtain values of μ_D as much as ten times larger than μ_H.

To shed light upon the above discrepancy, Hall electrodes were incorporated into some experimental TFT structures permitting both μ_D and μ_H to be measured upon the same film sample. This was the first time to our knowledge that Hall mobility measurements have been made directly upon an accumulation layer formed by an external field electrode. It was expected that at positive gate biases the measured Hall mobility should actually <u>decrease</u> as the electron flow was

crowded into a thin channel near the surface where surface scattering would play a larger role*. In fact, precisely the opposite effect was found, a result which has led to a broadened understanding of the possible nature of the thin films with which we are dealing.

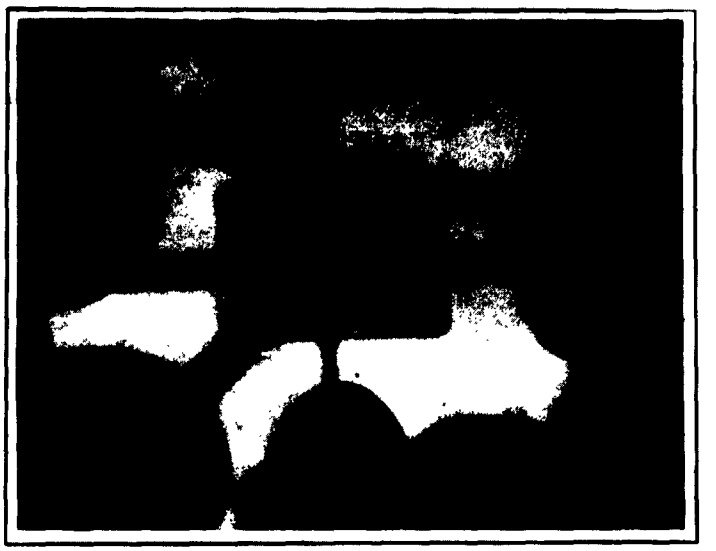
Figure 5 shows a diagram and photomicrograph of the TFT-Hall structure which was built. Since the initial tests were exploratory in nature, a four-electrode Hall configuration was simpler to build than the usual six-electrode structure. These four electrodes, oriented in the form of a square 0.010 inch on a side, made contact to the underside of the CdS film, while the insulator and gate structure were deposited on top of the film. A floating voltage supply was used in series with the electrometer to buck out the small residual voltage appearing across the Hall probes in the absence of a magnetic field. Owing to the small Hall voltages which were generated, relative to possible contact noise, it was found advantageous to use a recorder on the electrometer output for greater accuracy. Since the electrometer input impedance was very high ($>10^{12}$ ohms) any leakage through the gate insulator had to be kept very small to avoid additional spurious noise due to this cause.

It can be readily shown that the Hall mobility is related to the Hall voltage V_H by the following expression

$$\mu_H = \frac{10^8}{B} \frac{V_H}{V_d} \frac{L}{W} \tag{3}$$

---

* Since the discovery of field-effect conductivity modulation[8], there has been a great deal of work done, both theoretical and experimental, on surface space charge layers and channels. The problem of mobilities in such layers has been discussed by Schrieffer[9] and others, and later numerous experiments were carried out on conductivity and mobility in layers produced by controlling the ambient gases in contact with the semiconductor surface[10]. Measurements of mobility in gas-controlled channels gave values which, in general, agreed with Schrieffer's predictions of reduced mobility in the channel. Even where agreement was not exact, the general decrease in mobility was noted. These measurements were made on single crystals.



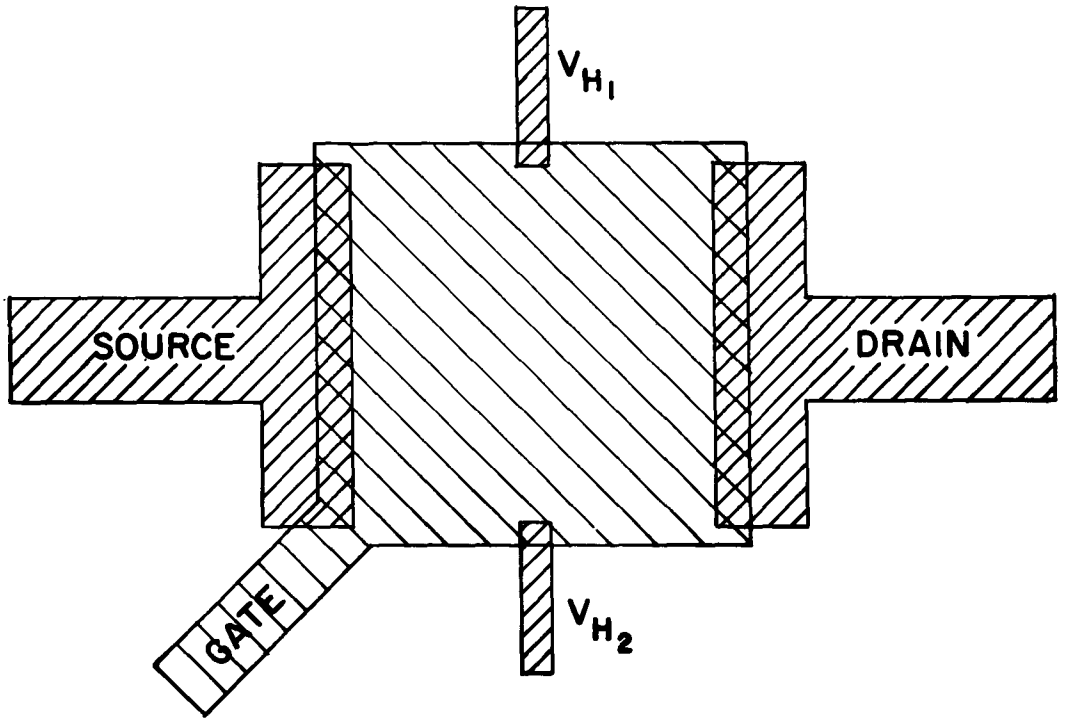


Fig. 5 Electrode Layout and Photomicrograph of TFT-Hall Test Structure

where V_H is the true Hall voltage

V_d is the source-drain voltage

L is the source-drain spacing

W is the distance between the Hall electrodes

Due to the shorting effect of the electrodes the measured value of the Hall voltage V_{HM} is less than the true Hall voltage V_H by a factor F, where $V_{HM} = F\ V_H$.

In the structures tested, $\frac{L}{W} = 1$ and $F = 2/3$. Hence the relation used to calculate μ_H was:

$$\mu_H = \frac{10^8}{B} \frac{V_{HM}}{V_d} \ 3/2 \qquad (4)$$

where V_{HM} and V_d are measured values in volts,

B is in gauss,

μ_H is in cm^2/volt-sec.

In using Eq. (4) the actual voltage drop in the sample may be less than the applied voltage V_D if an appreciable voltage drop exists in a barrier at either the source or drain. If this were true the value of μ_H given by Eq. (4) will be too small. It shall be assumed that the barrier drop is negligible, but for greater accuracy the 6-electrode structure would be preferable.

It is noted that the thickness of the conducting medium does not enter into Eq. (4). However, if a positive gate potential causes an enhanced current to be concentrated into a narrow surface channel, it is reasonable to assume that the mobility calculated from Eq. (4) would apply largely to the channel. Petritz[11] has studied the effects of layered structures in samples used for Hall mobility measurements.

Figures 6-8 show Hall mobility for three units as computed from the above formula versus gate voltage. The drain characteristic curves are included beside each plot. Units 616-2 and 620-4 are enhancement-type units,

while 623-2 is a depletion type. In each type an increase in μ_H by a factor of 2 to 3 times is noted with an increase in gate bias. Although this increase in μ_H is sizeable and entirely contrary to expectations, the increase is quite small compared to the increase in μ_D with gate bias found in a good enhancement-type unit having a high trap density.

The values of μ_D for several samples conputed from performance data at points where V_G is much greater than V_D are compared with μ_H in the chart of Table I. It is noted that even though the tests are made on the same semiconductor layer, the discrepancy between μ_D and μ_H still exists in an amount

TABLE I

Fig. No.	Unit Number	Type	Substrate Temperature °C	μ_H cm^2/volt-sec	μ_D cm^2/volt-sec
	615-3	ENHANCE.	170	6	19
	616-4	ENHANCE.	170	6	33
6	616-2	ENHANCE.	170	7	40
7	620-4	ENHANCE.	100	23	10
	620-5	ENHANCE.	100	27	10
8	623-2	DEPLET.	100	22	15

which exceeds the probable experimental error. Even more striking is the fact that in the units in which the CdS is deposited on a 170°C substrate the drift mobility is consistently higher than the Hall mobility, while in the units deposited at 100°C substrate the drift mobility is lower than the Hall mobility. While the total number of units tested is somewhat limited, it is interesting to note that two such different classes exist and that the observation correlates with a difference in preparation of the films. Since

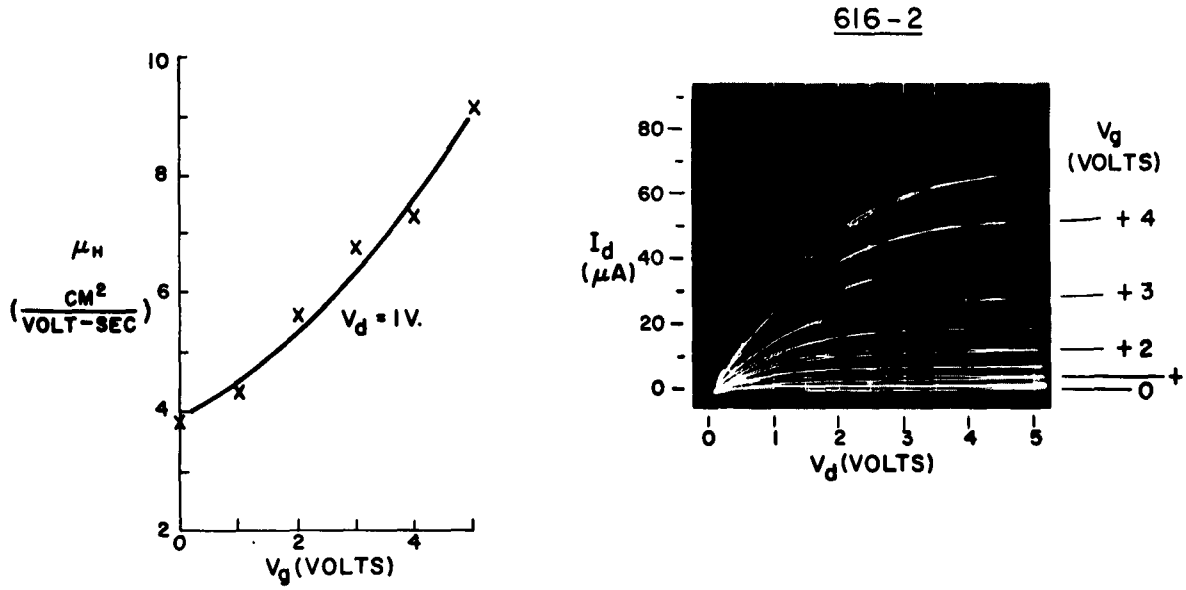


Fig. 6 Hall Mobility as a Function of Gate Bias for an Enhancement-Type TFT Having CdS Deposited upon a Substrate at 170°C (616-2)

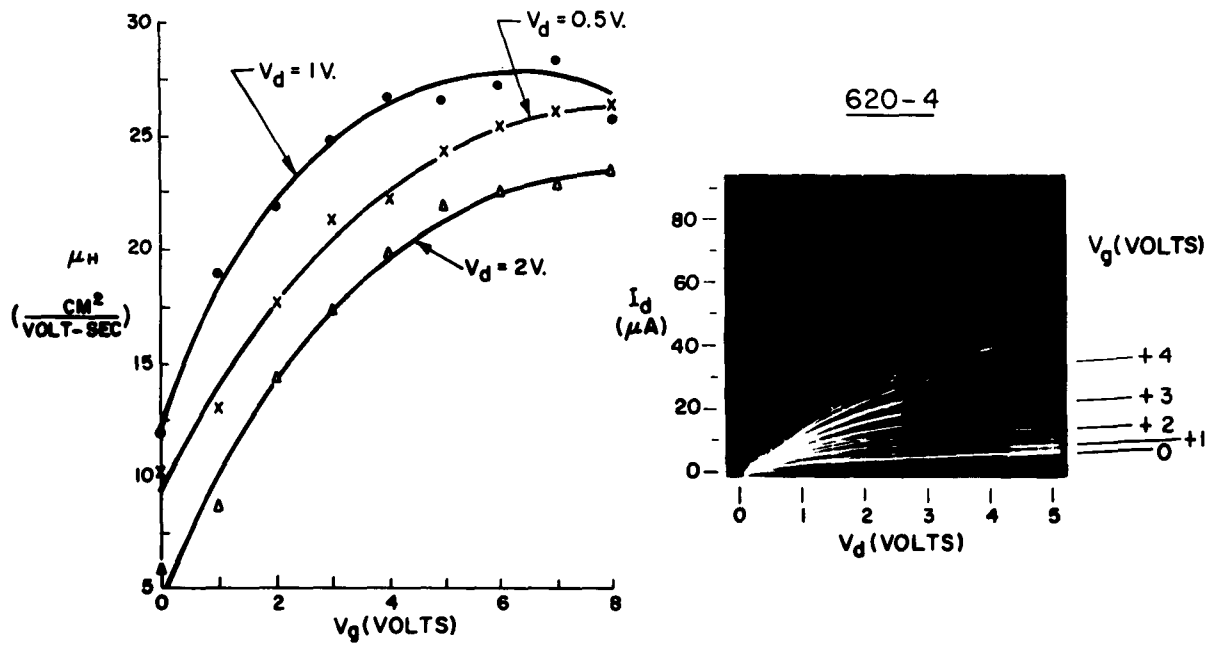


Fig. 7 Hall Mobility as a Function of Gate Bias for a Unit Whose CdS Was Evaporated on a 100°C Substrate (620-4)

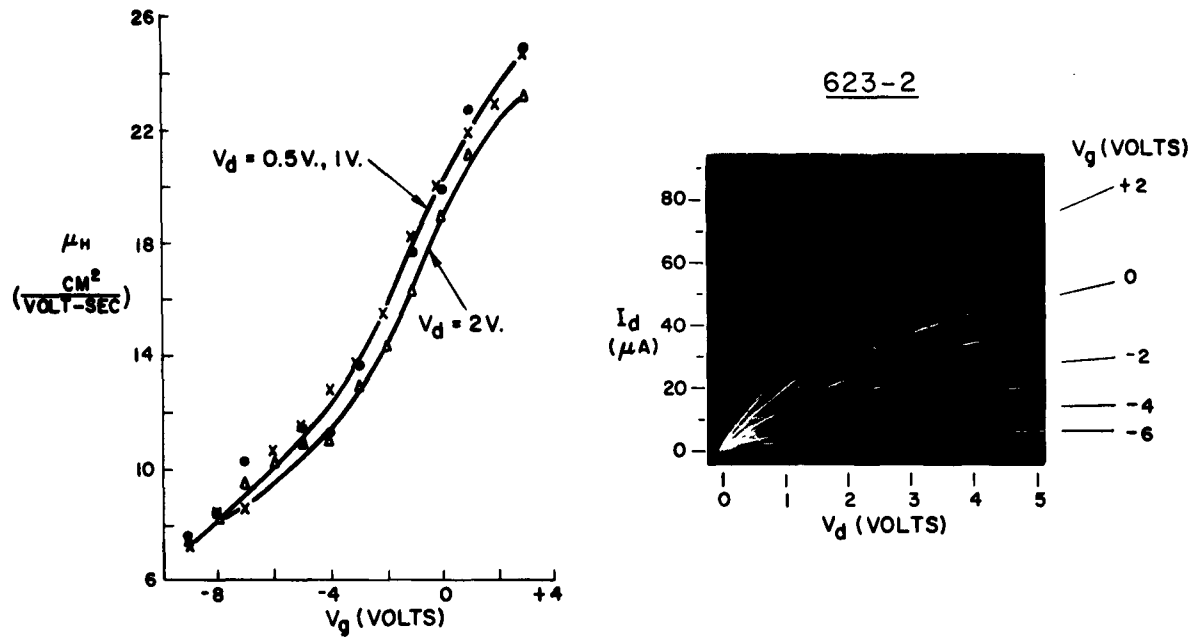


Fig. 8 Hall Mobility as a Function of Gate Bias for a Depletion-Type Unit Whose CdS Was Evaporated on a 100°C Substrate (623-2)

it is well known that the degree of crystallinity of an evaporated film is a strong function of the substrate temperature[12] the above results are compatible with the suggestion of nonhomogeneous layers postulated in the next section.

B. A PROPOSED INTERPRETATION OF THE MOBILITY MEASUREMENTS

Reconciliation of the above data solely in terms of field-effect action on the surface of a homogeneous semiconductor is extremely difficult. Consider the disparity between values of μ_H and μ_D. Regardless of the scattering processes assumed, μ_D must be less than or equal to μ_H. And if one considers trapping, μ_D can easily be as little as 10^{-5} times μ_H, since traps do not affect Hall mobility. While it is possible for most of the traps to be filled at high gate voltages, thereby increasing the effective drift

mobility, μ_D should still never be greater than μ_H. Looking again at the formula used in computing μ_H, one sees that although contact voltage drops would give a smaller computed μ_H than actually exists, such contact drops would also tend to give a smaller computed value of μ_D.

The rise in Hall mobility with increasing gate voltage is also an effect that seems to go in the wrong direction. As was mentioned before, Schrieffer's theory predicts a decrease in mobility in an accumulation layer and numerous experiments have confirmed this. Both theory and experiment in this area had been carried out on single crystal rather than polycrystalline films.

Although the evaporated CdS layers were known to consist of a large number of very small crystallites, it had been implicitly assumed that the net electrical effect was that of a homogeneous medium. We now propose that we are in truth dealing with many small crystallites, separated by insulating barriers. These barriers could be oxides or salts of Cd or S, amorphous CdS, excesses of S, etc. The results of Hall measurements on such media were considered by Volger[13], who showed that, to the first approximation, the measured Hall coefficient will be the same as the Hall coefficient of the conducting crystallites. Later Petritz[14] dealt more thoroughly with this problem in connection with lead salts. If the situation is essentially the same in a CdS film, such a picture should also be valid here.

One can think of the film as consisting of many small, relatively conducting crystals of CdS imbedded in an insulating matrix of the type described above. For simplicity, one can think in terms of a one-dimensional chain of crystallites of individual length ℓ_c separated by barriers of length ℓ_b. When a potential is applied along such a chain, the field will be much greater across the barriers than across the crystallites, given roughly by

$$\frac{E_b}{E_c} = \frac{G_c}{G_b}$$

where G_b and G_c refer to the conductivity in the insulating barriers and in the conducting crystallites, respectively.

The operation of the TFT would then be due to modulation by field effect of the conductivity in these barrier layers, while the crystallites can be considered as conducting islands between successive barriers. If this is the case, then the effective source-drain spacing will be much smaller than the geometrical spacing of the electrodes. Assuming that the barrier conductivity is small compared to the crystallite conductivity even under positive gate bias conditions, calculations show that L, the geometrical source-drain spacing in Eq. (2), should be replaced by

$$L_{eff} = L \cdot L_b^{1/2}$$

where $L_b = \Sigma \ell_b$ = the total distance between source and drain occupied by barriers. Thus Eq. (2) becomes

$$\frac{g_m}{C_g} = \frac{\mu_D V_d}{L \cdot L_b} \tag{5}$$

where μ_D is the effective drift mobility in the barrier. Since L_b is always less than L, the effective g_m/C_g is increased for a given value of μ_D. Conversely if Eq. (5) were used to calculate μ_D, a smaller value of μ_D would result, depending upon the relative sizes of crystallites and insulating barriers. Although the actual barrier thicknesses are still speculative this hypothesis could readily bring the maximum calculated values of μ_D and μ_H into closer agreement.

If such barriers do exist in the CdS the question arises as to just what meaning is to be ascribed to the Hall mobility measurements. It has been proposed in the past[15] that the effective mobility of charge carriers in polycrystalline photoconductors may vary with illumination if the conductivity is limited by intercrystalline barriers and if the height of these barriers is modulated by light. Thus the effective mobility would increase with light up to the point where the barrier is completely depressed and the mobility is observed experimentally in sintered CdSe layers[15]. It appears quite reasonable

that a similar mechanism could be acting in the CdS layers if the intercrystalline barrier were lowered by the field effect of the gate.

While the barrier hypothesis is not uniquely required in accounting for the increase in μ_H with gate voltage it does fit the observations and provides justification for the fact that the drift mobility in polycrystalline films can exceed the measured Hall mobility under the operating conditions of the TFT. Although, in general, one would still expect larger values of Hall mobility to yield higher performance in the TFT, this conclusion does not necessarily hold in all polycrystalline films as noted in Table I. In single crystal films a more direct correlation between performance and μ_H should follow provided one is sure that the measured value of μ_H applies to the surface layer of the CdS where the induced channel will be formed.

It will be noted that the polycrystalline barrier hypothesis is not inconsistent with the saturation mechanism and the field effect analysis which has been derived in Section III for a homogeneous semiconductor. Although the barrier picture replaces on a microscopic scale the single TFT by a row of elemental TFT's in series controlled by a single gate, an effective conducting channel is still formed on the surface of the film just as in a homogeneous layer. As before when the gate is made more positive additional electrons are drawn in from the source electrode contributing to increased conductivity of the barriers nearest the insulator interface. Although the elemental TFT's in the series would not individually exhibit a saturated pentode-like characteristic, the group as a whole does show saturation since those elemental TFT's nearest the drain would be operating near pinch-off. It can be demonstrated that a group of enhancement-type TFT's connected in series with a common gate will show saturation at a total applied voltage too low for any one of the group to saturate.

C. ADDITIONAL MOBILITY MEASUREMENTS (Second Quarter)

To examine the conductivity mechanism in TFT structures and to attempt

to explain the observed Hall and drift mobility in these devices, measurements of conductivity and Hall mobility are being made on operating units as a function of temperature. A detailed study of the temperature effects should provide information on the nature of electrode-semiconductor barriers, intercrystalline barriers, trap depths and impurity levels, and on the nature of scattering centers in the semiconductor films.

The previously described Hall apparatus has been modified to permit operation over a moderate range of temperatures in such a way that is readily adaptable to use with present TFT Hall structures. By use of suitable thermal insulation, samples can be maintained at temperatures between about +120 and -120°C; heating or cooling of the sample is done by passing hot or cold nitrogen gas over the sample. Gas temperature is controlled by use of a cooling coil in liquid nitrogen in series with a heated coil. Temperature uniformity is achieved by the use of a relatively large thermal mass in the sample holder and by means of the very small TFT area.

The temperature dependence of Hall mobility for sample 620-4 is shown in Fig. 9. Figure 10 shows the drain current temperature dependence for the same sample on a 1/T plot. This sample was a standard Hall-TFT structure with CdS deposited on a 100°C substrate and given a subsequent air bake. The data are shown for a drain voltage of 1 volt and gate voltage between 0 and 3 volts. In this temperature range Hall mobility and conductance increase with temperature. The drain current shows an approximately exponential dependence on 1/T, indicating an activation energy in the range of 0.1 to 0.2 e.v., in agreement with results on standard TFT units. Additional samples are being studied, and the evidence suggests a maximum in mobility somewhat above room temperature. A more detailed analysis of the temperature dependence results will be made as further data become available.

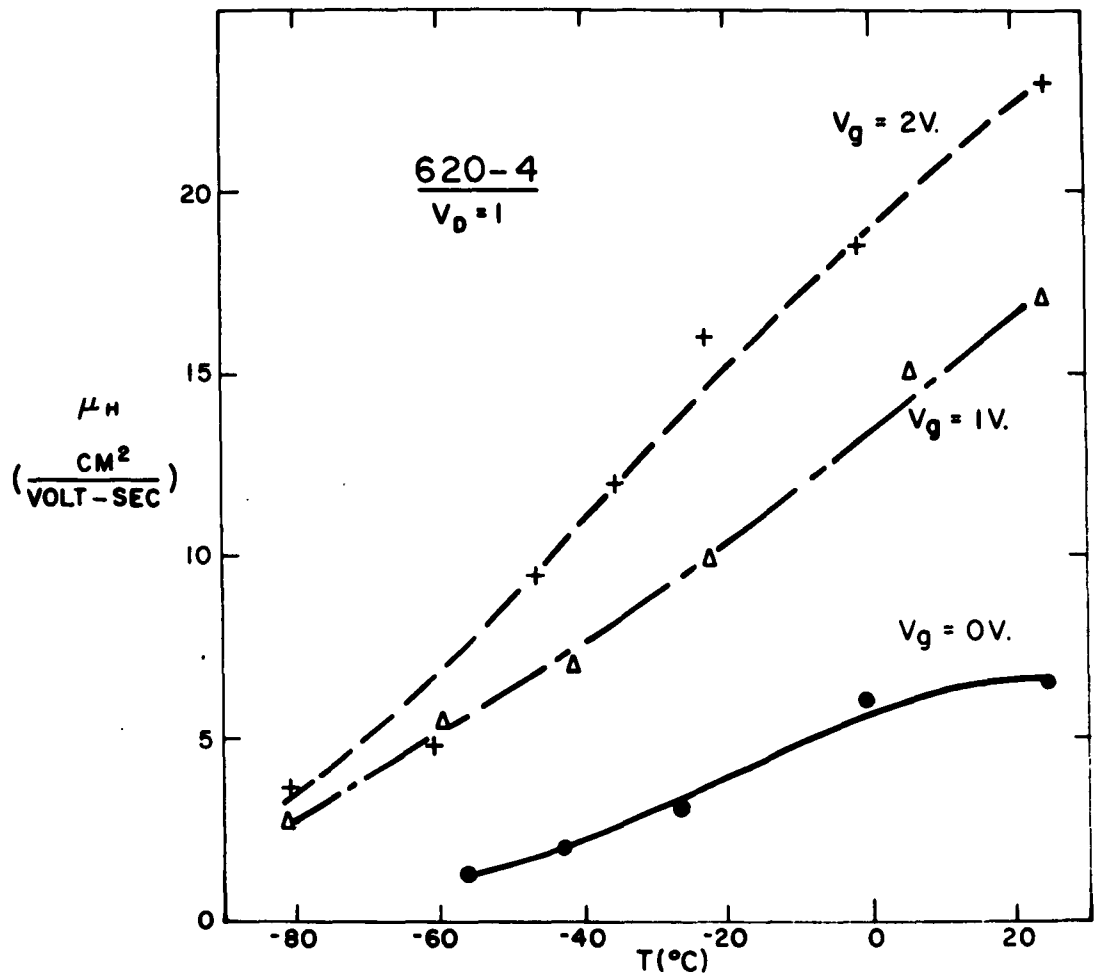


Fig. 9 Hall Mobility vs. Temperature for Sample (620-4)

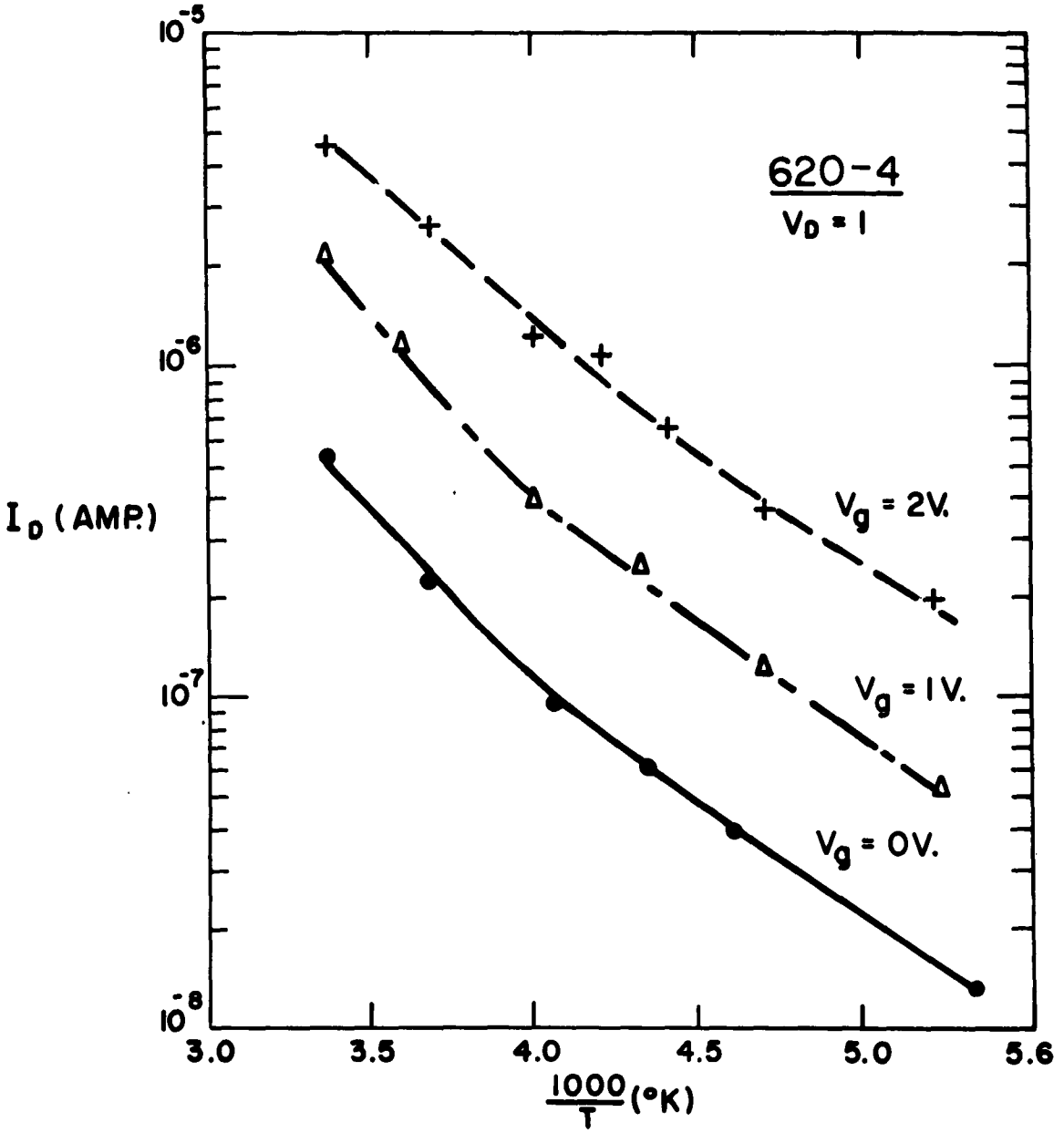


Fig. 10 Drain Current vs. 1/T for Sample (620-4)

IV. FIELD EFFECT ANALYSIS OF THE INSULATED-GATE TFT

The following analysis* predicts the drain characteristic of a TFT structure entirely from the point of view of a field-effect mechanism. It assumes a homogeneous layer of semiconductor that is free of traps and forms ohmic contacts with the source and drain electrodes. Only majority carriers are considered to exist in the semiconductor. A somewhat similar analysis applicable to the unipolar field-effect transistor was presented by W. Shockley[6] in 1952.

As is shown in Fig. 11, the semiconductor is a film having thickness, h; length of gap between source and drain electrode, L; and width, w. The gate electrode is spaced from the semiconductor by an insulating layer with a capacitance, C per unit area, existing between the gate and the semiconductor. In this analysis C is assumed constant even though measurements indicate that C does vary with the operating voltages. The potential of the semiconductor at an arbitrary point x measured from the source electrode, is given as V(x); the fixed potential of the gate, V_g; and that of the drain, V_d, all measured with respect to the source. Assuming that ΔN charges per unit area of q coulombs per charge are impressed onto the gate, an equal charge is induced on the semiconductor. The change in charge per unit area may be written as,

$$q \cdot \Delta N = C \left[V_g - V(x) \right] \tag{6}$$

The mean current density, $\bar{J}$, in the semiconductor is expressed as

$$\bar{J} = \bar{n}\, q\, \mu\, E_x = q\, \mu \left(n_o + \frac{\Delta N}{h} \right) \frac{dV(x)}{dx} \tag{7}$$

where μ is the mobility in cm^2/volt-sec

E_x is the electric field in volts/cm

$\bar{n}$ is the mean number of charges per unit volume

n_o is the initial number of charges per unit volume.

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* Unpublished work by A. Many, RCA Laboratories, Princeton, New Jersey.

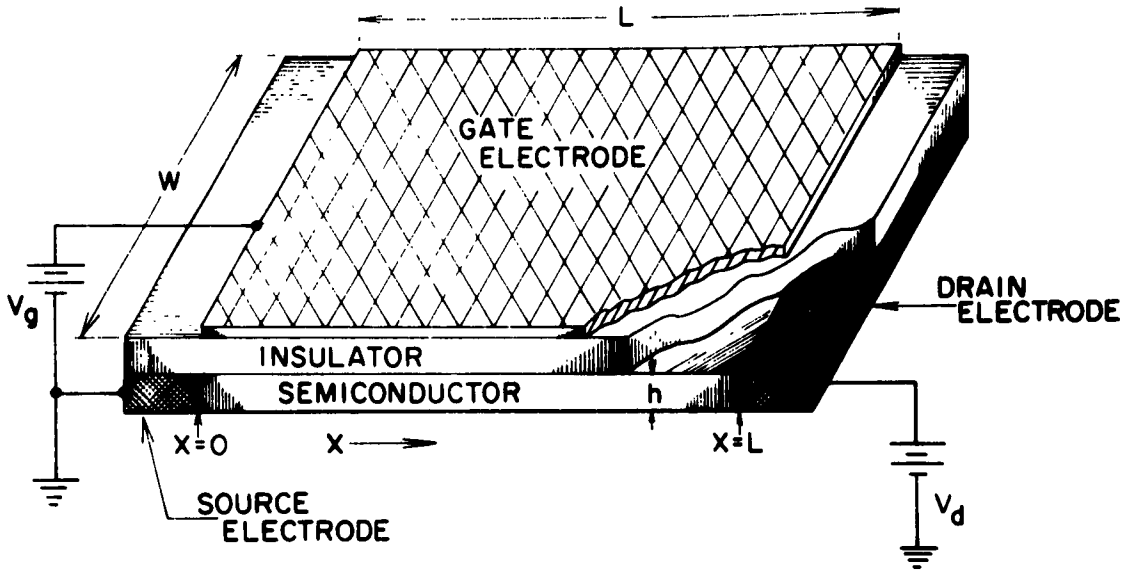


Fig. 11 TFT Structure Used for Analysis

The expression for the drain current,

$$I_d = hw\bar{J} = hwq\mu \left\{ n_o + \frac{C\left[V_g - V(x)\right]}{qh} \right\} \frac{dV(x)}{dx} \tag{8}$$

$$\frac{I_d}{w\mu C} \int_0^L dx = \int_0^{V_d} \left[\frac{n_o hq}{C} + V_g - V(x)\right] dV(x) \tag{9}$$

yields,

$$\frac{I_d L}{w\mu C} = \left[\frac{n_o hq}{C} + V_g\right] V_d - \frac{V_d^2}{2} \tag{10}$$

For a specified geometry and materials, the following may be regarded as constants:

$$n_o hq = Q_o = CV_o \ , \tag{11}$$

and

$$\frac{L}{w\mu C} \equiv m \tag{12}$$

V_o is the voltage required to deplete the carriers in the semiconductor. Substituting (11) and (12) in Eq. (10),

$$I_d = \frac{V_o + V_g}{m} V_d - \frac{V_d^2}{2m} \tag{13}$$

This expression (13) relates the drain current to both the drain and gate voltages. The expression is valid only up to the point where the slope is zero corresponding to the knee of the characteristic. From there on it may be shown that the drain current should be independent of the drain voltage.

The following characteristics are derived from Eq. (13): The resistance of the curves at the origin is,

$$r_d = \left.\frac{\partial V_d}{\partial I_d}\right|_{V_d = 0} = \frac{m}{V_g + V_o} \tag{14}$$

which shows that the conductivity is linear with gate voltage.

The location of knees of the curves is determined from the condition of zero slope of the drain characteristics. It is found that the drain voltage at the knee,

$$V_{d\ knee} = V_g + V_o \tag{15}$$

A similar expression corresponding to the locus of points below the maximum drain current by a factor y, $(y < 1)$ may be shown to be,

$$V_{d\ knee}' = \left[1 - \sqrt{1-y}\right] (V_g + V_o) \tag{16}$$

The maximum drain current at the knee is given as,

$$I_{d\ max} = \frac{(V_g + V_o)^2}{2m} \tag{17}$$

from which the transconductance of the device in the saturated drain current region is derived as,

$$g_m = \left.\frac{\partial I_{d\ max}}{\partial V_g}\right|_{V_d = V_{d\ knee}} = \frac{V_g + V_o}{m} = \sqrt{\frac{2\ I_{d\ max}}{m}} \tag{18}$$

The results of this analysis predict the following TFT characteristics from solely a field-effect mechanism: (1) at low drain voltage the output resistance is inversely proportional to the gate-voltage-plus-a-constant, (2) the drain voltage at the knee is linear with gate voltage, and (3) the transconductance in the saturated portion of the curves is proportional to the square root of the drain current. All of these characteristics have been consistently observed in experimental TFT's and are reported in Section V. The close correlation between the analysis and experimental data gives strong evidence that the operating mechanism depends upon the electric field which is produced by the gate potential and which modulates the conductivity of the semiconductor.

V. MEASUREMENTS OF OPERATING CHARACTERISTICS OF THE TFT

A typical drain characteristic of an enhancement-type TFT (staggered structure) is shown in Fig. 12. The drain current is plotted as a function of drain voltage with the gate voltage as a parameter. All voltages indicated are positive with respect to the source. Note that the device exhibits pentode-like characteristics. Since a 0.2 volt change on the gate produces a 2 milliampere change in drain current, the transconductance, or g_m of this unit is about 10,000 micromhos. The dynamic output resistance determined by the reciprocal of the slope of the curves in the saturation region is about 8,000 ohms. The voltage amplification factor calculated from the product of the transconductance and output resistance is 80.

The evidence indicates that the saturated characteristics result from the pinch-off of the induced conduction channel in the region of the drain. The rising potential along the channel from source-to-drain relative to the gate potential causes a gradation from an accumulation layer near the source to a depletion layer near the drain. The saturation mechanism is thus a gate control phenomenon quite analogous to that observed in the conventional field-effect transistor.

A figure of merit which characterizes the high-frequency performance of any three-terminal active device is its gain-bandwidth product. For the TFT it can be shown that the gain-bandwidth product,

$$G \cdot BW \approx \frac{g_m}{2\pi C_g} \tag{19}$$

where C_g is the total gate capacitance. Typical experimental units have demonstrated gain-bandwidth products of about 15 megacycles.

Insulated gate TFT's have also been produced which operate in the "depletion" mode. (See Fig. 3) Such units exhibit saturated characteristics with 1 or 2 milliamperes drain current flowing when the gate is at the same potential

as the source. This drain current may be depleted by applying negative gate voltage or enhanced by positive gate voltage. The drain characteristic is similar to the enhancement-type units except for the gate voltage scale.

Enhancement units are of interest for integrated-circuit applications because the positive gate bias permits direct coupling of successive stages. The depletion units are useful for input, detector and other applications where zero bias is desirable.

Figure 13 shows the behavior of drain characteristics that are typical of both enhancement and depletion type TFT's. The drain characteristics illustrated have been separated into two regions by the dashed line. In region (1) at low drain voltage below the onset of current saturation, the output resistance is inversely proportional to the gate-voltage-plus-a-constant. The dashed line (2) represents the locus of the knees of the curves. It has been found that the voltage at the knee is linear with the gate voltage. Region (3) is

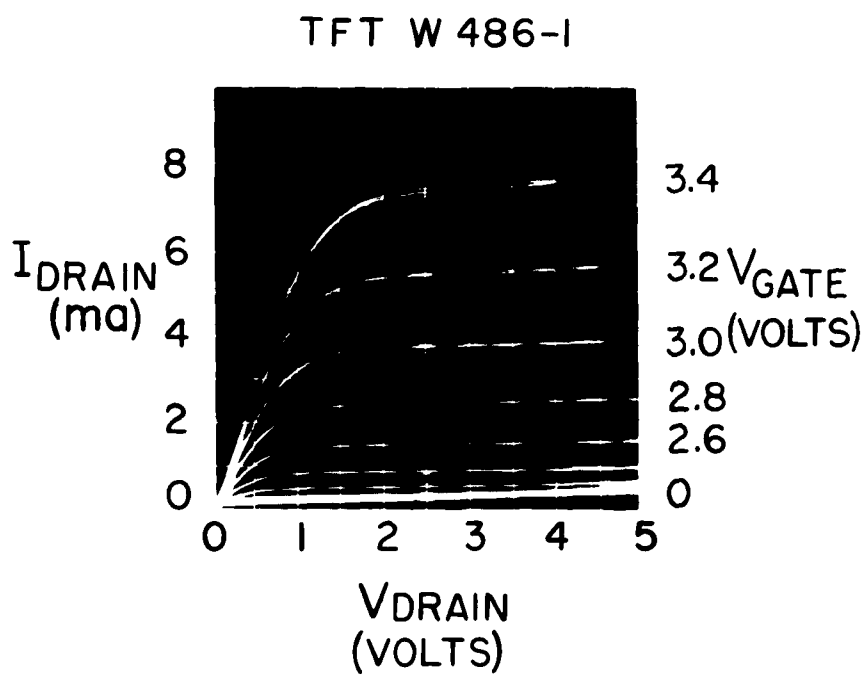
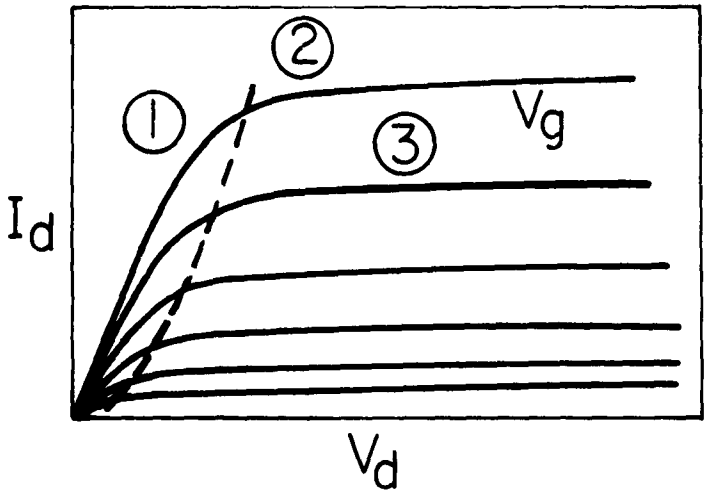


Fig. 12 Drain Characteristic of an Experimental Enhancement-type CdS TFT. The Maximum Transconductance is 10,000 μmhos while the Output Impedance is about 8,000 Ohms



① $r_d \propto \frac{1}{V_g + k_1}$

② $V_{d\ knee} \propto V_g + k_2$

③ $I_d \propto (V_g + k_3)^2$

$\therefore g_m \propto \sqrt{I_d}$

Fig. 13 Typical Drain Characteristic and Experimentally Determined Relationships Which Describe It

the high drain voltage, current saturation area. Here the drain current is proportional to the quantity: gate-voltage-plus-a-constant squared. A consequence of this last characteristic is that the transconductance is proportional to the square root of the drain current. These experimental observations are consistent with theoretically predicted characteristics of the insulated-gate field-effect structure shown in Section IV.

The small-signal equivalent circuit of a TFT may be represented as shown in Fig. 14. The gate, drain and source electrodes are represented as the nodal points marked G, D and S. The impedances between gate-and-source and gate-and-drain electrodes are represented by parallel RC circuits. As will be shown, the magnitudes of these impedances are dependent upon the d-c operating point and also upon the frequency. The output circuit consists of the dynamic output resistance, r_d, driven by a constant current generator, $g_m e_{gs}$. Drain-source capacitance is small and has been neglected.

The impedances between the elements in a TFT have been measured by several different techniques. Figure 15 shows the total gate capacitance, C_g, measured between the gate and both the source and drain electrodes. C_g is plotted as a function of gate-to-source voltage with drain-to-source voltage as a parameter. As is shown in the transfer characteristic below, the unit illustrated is of the depletion type. Approximately 1 milliampere drain current flows at zero bias condition. The data presented were taken at 100 kilocycles using a Boonton Electronics capacitance bridge. Other measurements taken at frequencies between 2 kc and 200 kc have shown similar results except that the measured capacitance decreases slightly at the higher frequencies. Note that with zero drain volts applied, the capacitance increases and tends to level off as the gate potential increases in the positive direction. This behavior is expected because the width of the space-charge region in the semiconductor adjacent to the insulator is being reduced as the gate voltage is increased. Therefore, the asymptotic value of capacitance approaches the geometrical capacitance across the insulator layer. However, at higher drain voltages it is found that the capacitance increases, reaches a maximum, and then decreases with gate voltage. This behavior has been observed repeatedly in both enhancement and depletion TFT's, the peak in capacitance being shifted toward positive gate biases for the enhancement units. The maximum in capacitance always seems to occur at a gate voltage which produces a drain current of about 5-10% of its maximum stable value. Since the fall-off of capacitance at high drain voltage is observed over a wide range of frequencies, and the shunt resistance is large (as will be discussed shortly), the effect is due to a change in capacitance within the TFT. However, from the applications point of view, it does not matter whether the cause is due to a capacitance or a resistance change, since the input signal will see the capacitance and shunt resistance as measured in these tests.

Three-terminal capacitance measurements are used to determine the isolated capacitances and shunt resistances which exist between two of the three terminals of the TFT. The results of such measurements are shown in Fig. 16. The solid-line curves correspond to zero drain voltage, while the dashed curves are for

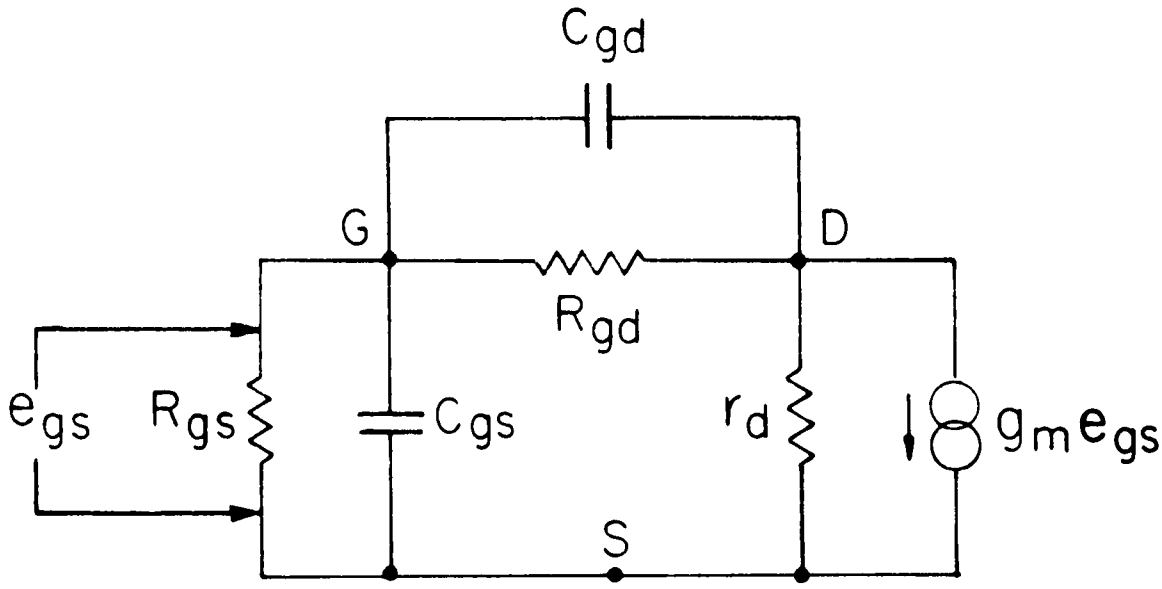


Fig. 14 Equivalent Circuit of a TFT

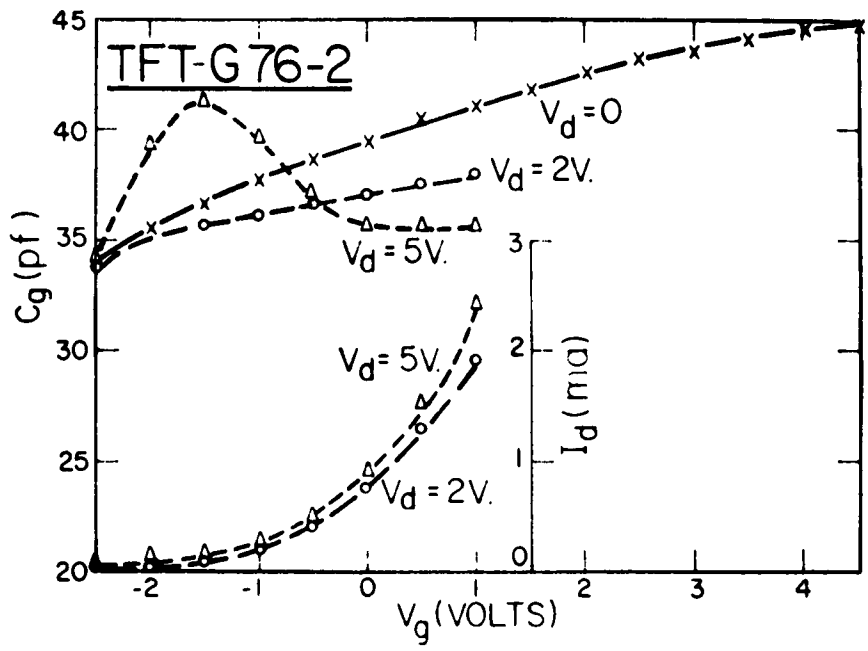


Fig. 15 Total Gate Capacitance (measured at 100 kc) and Transfer Characteristic of an Experimental Depletion-Type TFT

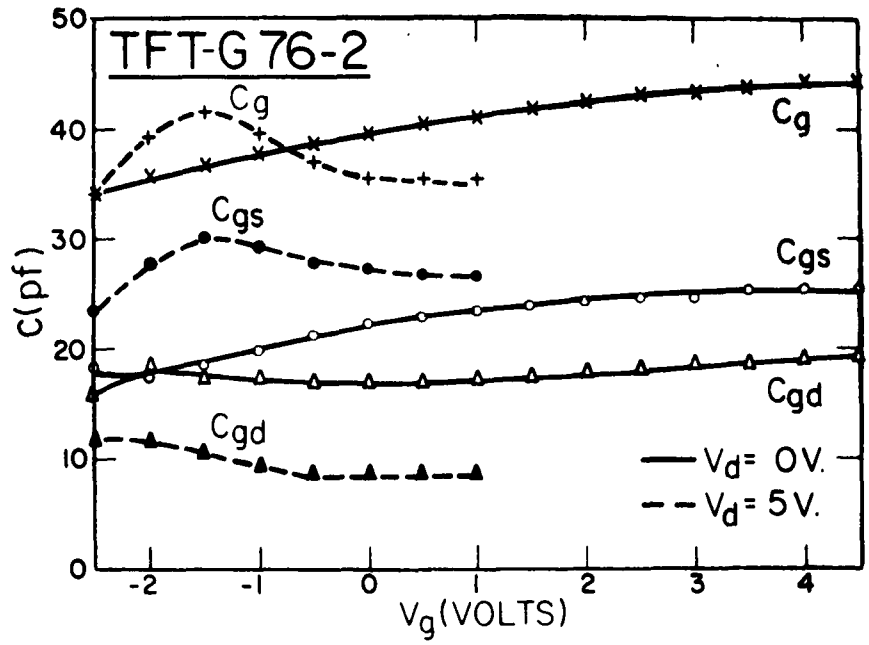


Fig. 16 Distribution of Gate Capacitance Between Source and Drain Electrodes. Characteristics for Drain Voltages of Zero and 5 volts Are Shown. All Curves Were Measured Independently.

5 volts applied to the drain. The total gate capacitance, C_g, is separated into two components: C_{gs}, the capacitance between gate and source and C_{gd}, the capacitance between gate and drain. Note that with both source and drain electrodes grounded, the total gate capacitance divides about equally between the gate-source and gate-drain regions. However, at higher drain voltage (in the saturation region) the major portion of gate capacitance, including the peaked characteristic, exists in the gate-source circuit and only a relatively small amount in the gate-drain circuit. This situation is desirable because in TFT amplifier applications, it is the gate-drain capacitance which is magnified by feedback. The distribution of shunt resistance from the gate to the source and drain electrodes also varies with operating voltages. At zero drain volts the gate-drain and gate-source resistances are about equal and do not vary greatly with gate voltage. But the gate-drain resistance increases and the gate-source resistance decreases as the drain voltage is increased.

It has been found that these shunt resistances, measured at 100 kilocycles are greater than about one megohm for the TFT being described. The observed fall-off in capacitance with the onset of drain current in the saturation region can be explained by the repulsion of the induced channel away from the gate in the neighborhood of the drain. This is consistent with the explanation for saturation given previously.

The TFT is of interest for switching applications since negligible power is consumed in the "off" state and only moderate power (~1 milliwatt) in the "on" state. Figure 17 shows the switching waveforms observed on a TFT. Two cases are illustrated, both producing a change of 2 milliamperes in drain current. Note that the drain current increases in the direction of the arrow. In the upper oscilloscope photo, trace "A" is a low-to-intermediate current transition while trace "B" is the reverse, an intermediate-to-low transition. The lower photo trace "C" is an intermediate-to-high and trace "D" is a high-to-intermediate current transition. The opposite-polarity transient is direct feed-through of a signal via the gate-drain capacitance. The effect is greater in the transitions between low and intermediate drain current because the input pulse is larger. Note that the switching transitions occur in about 30 nano-seconds. However, the transients produce apparent delay and storage times which account for about one-half of the total switching time. These results were obtained using a pulse source impedance of 50 ohms.

The temperature dependence of an experimental TFT is shown in Fig. 18. The drain current is plotted as a function of the reciprocal of the absolute temperature for a constant drain potential of 4 volts. The gate voltage is the parameter. The drain current decreases by 2 or 3 orders of magnitude when the temperature is decreased from 120°C to -120°C. The slopes of the curves on a log current vs. 1/T plot yield activation energies. These are listed at the extremities of the curves. Note that the energies vary from 0.09 to 0.2 electron-volts, suggesting that a distribution of levels is involved. Further tests are required to identify the kind of energy levels that may be responsible for the observed temperature variations.

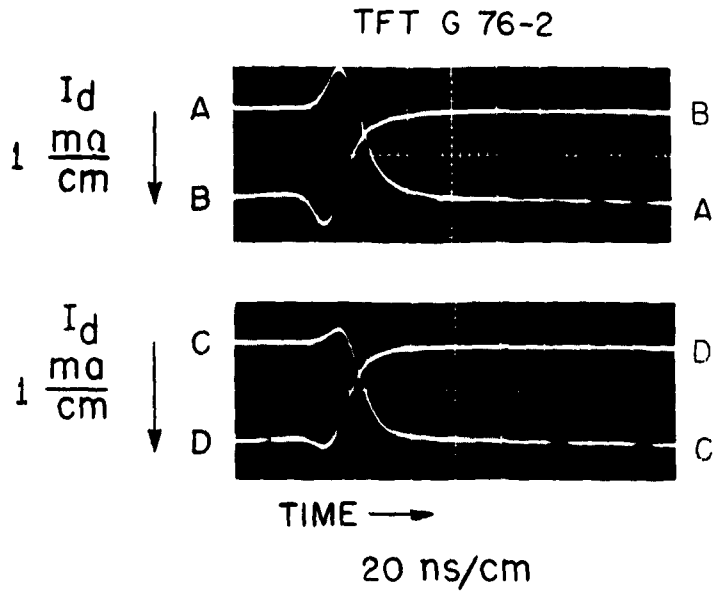


Fig. 17 TFT Drain Current Transitions: A - low to intermediate, B - intermediate to low, C - intermediate to high, and D - high to intermediate

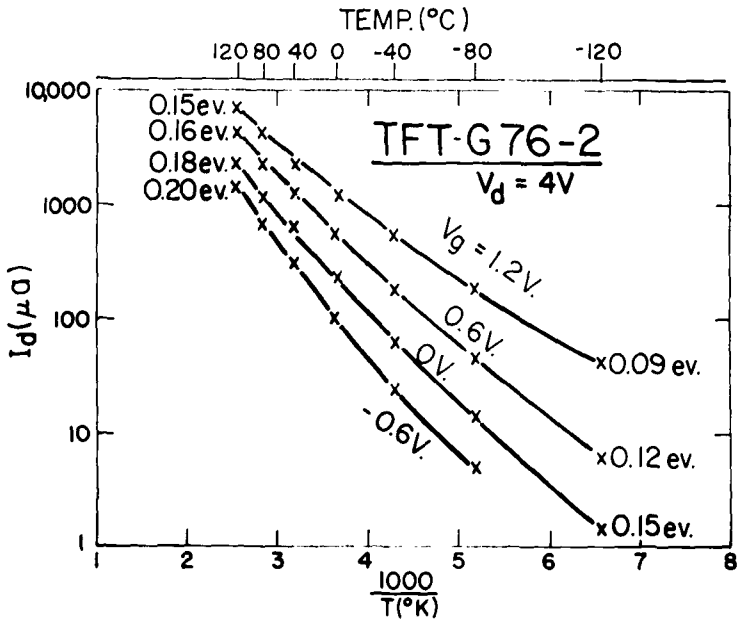


Fig. 18 TFT Drain Current vs. Temperature Dependence

VI. THIN FILM MATERIALS STUDIES

The general approach to improved materials for TFT's has included an evaluation of processing modifications to yield higher performance CdS films and an investigation of other semiconductors suitable for TFT operation. A subsidiary problem has been a study of contacts to the semiconductors, from the standpoint of both electrical properties and mechanical compatibility with sample processing. A major part of the materials problem has involved attempts to fabricate semiconductor layers having high Hall mobilities, both with CdS and other materials, since the TFT transconductance should be proportional to drift mobility and thus dependent on Hall mobility.

Work on CdS layers has been primarily directed toward a study of post-evaporation processing designed to improve device performance. It had been shown prior to the start of the contract that heating of CdS films in contact with CdS:Cu powder substantially increased both crystallinity and Hall mobility of the films. During the contract period evaluation of TFT's treated in this manner and by similar treatment in CdS:Cu,Cl powder in the temperature range 300°C to 500°C for several hours has been carried out. In general, such layers tend to be relatively photosensitive and to yield Hall mobilities on the order of 30 cm^2/v-sec in TFT Hall samples without illumination. TFT performance in such layers appears to be particularly sensitive to electrode configuration and contact problems. For example, gold electrode contacts appear to be inferior to indium or aluminum, readily forming high resistance contacts to this type of layer. The processing appears to yield somewhat nonuniform layers and, in general, contacts above the film yield different results from contacts below the films due both to mechanical instability of the electrodes and film inhomogeneity. Control of film resistivity is critical in processed layers, and can be controlled by optimum combinations of substrate temperature, copper to chloride ratio, and baking temperature. Usually, CdS resistivity on the order of 10^3 ohm-cm is desired. Increasing substrate temperature and copper concentration increases

resistivity. The bake cycle is relatively complicated due to effects of Cd, Cu, and Cl diffusion, but resistivity generally increases with baking temperature. Under optimum conditions CdS films given post evaporation treatment of this type have yielded TFT's having performance superior to unprocessed units.

Treatment of CdS films in other environments after deposition is also advantageous. Bakes in air, hydrogen, or various inert atmospheres have been investigated and have indicated both general advantages attributable to annealing and grain growth and, more specific, advantages based on control of film composition.

Work is now under way to evaluate in more detail the dependence of CdS film properties upon evaporator temperature and evaporant composition.

Parallel work is being carried out on CdS diodes to permit study of contact behavior and conduction mechanism in the CdS films. Preliminary results on Au-CdS-Au sandwich diodes indicate a significant rectification with the exposed top gold electrode blocking; based on $1/C^2$ plots, the upper gold contact has about a 0.9 ev barrier height.

The other semiconductors under evaluation for use in TFT's include group IV elements, and II-VI, IV-VI and III-V compounds. Recently, much of the work has been concerned with indium antimonide, indium arsenide, and gallium arsenide. Preliminary work, including some Hall measurements, has been done on silicon lead sulfide and cadmium telluride. Operating TFT's have been built with indium antimonide deposited onto substrates between 100 and 200°C, using a continuously fed evaporator to minimize fractionation. These units yielded a maximum transconductance of 500 μmho's but did not show significant saturation. Attempts to prepare suitable indium arsenide and gallium arsenide samples for TFT use are in progress.

VII. GENERAL FACTUAL DATA

A. PERSONNEL

Individuals who contributed to the contract activity during this report period were:

H. Borkan

V. E. Henrich

F. V. Shallcross

P. K. Weimer

Fabrication of experimental units was carried out by V. Frantz, W. S. Homa, and H. Lambert.

B. VISITORS, CONFERENCES, AND TRAVEL

Visitors

Mr. Rainer Zuleeg of Hughes Semiconductor Division, Newport Beach, California, visited RCA Laboratories, Princeton, N. J.

Conferences

P. K. Weimer and H. Borkan attended the IRE-AIEE Device Research Conference at the University of New Hampshire, Durham, New Hampshire, on July 9, 10, 11, 1962.

F. V. Shallcross attended the National Vacuum Symposium, Los Angeles, California, on October 31, November 1, 2, 1962.

P. K. Weimer and H. Borkan attended the NEREM Conference at Boston, Massachusetts, on November 6, 7, 1962.

Travel

H. Borkan and P. K. Weimer visited AFCRL at Bedford, Massachusetts, on November 6, 1962.

C. PUBLICATIONS

H. Borkan and P. K. Weimer, "Characteristics of the Insulated-Gate Thin-Film Transistor", a paper presented at the NEREM Conference at Boston, Massachusetts, November, 1962 and published in NEREM Record 1962, page 158.

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2. Semiconducting films
3. Semiconductors
4. Cadmium sulfide films

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II. Contract AF19(628)-1617
III. Radio Corporation of America, RCA Laboratories, Princeton, N.J.
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