UNCLASSIFIED

AD 295 097

Reproduced
by the

ARMED SERVICES TECHNICAL INFORMATION AGENCY
ARLINGTON HALL STATION
ARLINGTON 12, VIRGINIA

UNCLASSIFIED

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

65-2-3

CATALOGED BY ASTIA
AS AD No. 295 097

AIR FORCE INSTITUTE OF TECHNOLOGY

AIR UNIVERSITY
UNITED STATES AIR FORCE

295 097

SCHOOL OF ENGINEERING

WRIGHT-PATTERSON AIR FORCE BASE, OHIO

AF-WP-O-MAY 65 3,500

THESIS

Presented to the Faculty of the School of Engineering

The Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the

Master of Science Degree

in Electrical Engineering

LOGIC DESIGN FOR TRISTABLE DEVICES

by

Joseph A. Krupinski, B.S. E.E., P.E.

Captain, USAF

GE/EE/62-13

Graduate Electronics

December 1962

Forward

This report has been written under the assumption that an electronic device having three distinct stable states will become available in the near future. I have attempted to predict what such a device will make possible in the fields of computer technology and data processing. The logical use of this device will be in the ternary number system. With this in mind, I have attempted to present a comprehensive discussion of ternary logic and some circuitry which will work in a ternary computation system.

The bibliography which follows the text is divided into primary, secondary, and tertiary groupings. The primary set of references contain those books and articles which have a direct bearing on the material presented in this work. The secondary set of references include that material which is pertinent to this thesis but not specifically referenced in the text. The tertiary set of references comprise the remainder of the material which was researched in the course of this work.

I wish to acknowledge the valuable assistance of the personnel of the Molecular Electronics Laboratory of the Aeronautical Systems Division (AFSC) who have sacrificed of their time and facilities to help me in this endeavor. In particular, I would like to thank Mr. Steenbergen and Mr. Conklin for permitting me free access to their respective

branches. The assistance of my Faculty Thesis Advisor, Prof. T. Regulinski, cannot be neglected. I thank him for the advice and assistance he has rendered in maintaining the task and the available time in balance. I would also like to express my gratitude to the personnel of the AFIT library, ASTIA, and the Foreign Technology Division Library for their assistance in my research effort.

Contents

	Page
Foreword	ii
List of Figures	v
List of Tables	vi
Abstract	vii
I. Introduction	1
II. The Preferability of Ternary Logic	6
III. Characteristics of a Tristable Device	12
IV. The Ternary Number System	23
V. The Trinary in Ternary Computing Systems	33
VI. The Trinary in Current Systems	45
VII. Summary and Conclusions	47
Bibliography	51
Appendix A: Addition in the Ternary Adder	54
Appendix B: Tabulated Data for Curve of Figure 5	57
Vita	59

List of Figures

Figure		Page
1	Analog-to-Digital Converter	2
2	Tristable Circuits of Kumagai and Kawamoto . . .	4
3	Volt-Ampere Characteristic of a Tristable Device	12
4	Symmetrical Characteristic Curve	15
5	Characteristic Curve from Equation 40	22
6	Binary AND Circuit	33
7	Ternary Coincidence Circuit	35
8	Ternary OR Circuit	36
9	Ternary Counter Circuit	37
10	Ternary Serial Feed Adder	39
11	Ternary Circuits	41
12	Ternary Amplitude Half Adder	43
13	Tristable Multivibrator	44
14	Binary-Ternary Converter	46

List of Tables

Table		Page
I	Calculations	18
II	Rules of Ternary Addition	26
III	Rules of Ternary Subtraction	27
IV	Ternary Multiplication Table	28
V	Ternary Addition and Multiplication	31

Abstract

The development of a semiconductor device which exhibits three stable states of operation has prompted this thesis on ternary logic and its applications. A characteristic curve for the tristable device, called a TRINARY, is hypothesised and an equation determined which approximates the expected curve. The merits of the ternary system over binary are enumerated. The mathematics of a ternary number system is discussed and a method of converting between radix 3 and other number systems is presented. Some basic circuits of a ternary computer are presented and examples are given of a number of ternary circuits developed by others.

I. Introduction

A new approach is being considered in the effort to increase the capacity and speed of information processing equipment. Most of the computers and data processing machines in use today utilize the binary number system although this is not the best system (see Chapter 2). The sole exception known to the author is the SETUN computer built and operated by the University of Moscow, USSR, which uses ternary logic (Ref 11:72-120).

The purpose of this thesis is to investigate the use of ternary logic based on a device which has three stable states of operation. A tristable device, henceforth referred to as a TRINARY, is within the state of the art as evidenced by a patent issued to G. L. Pearson on 9 May 1961. The device is described as an integrated tristable device utilizing two tunnel junctions on an intrinsic wafer (Ref 7).

During the infancy of computers the logical functions were performed by relays. As bigger and more complex computers were made, the relay was replaced by the diode. The continued growth of computers and the need to process more data faster forced the industry to look to microelectronics. The amount of data continues to increase while the storage elements have been reduced in size to their practical limit. Throughout this entire growth the binary system persisted,

not because it was best, but because there were no devices comparable to the diode to permit the use of another number system.

A paper by B. Rabinovici and J. Klapper discusses the use of tunnel diodes connected in series to obtain a multistable functional network. The primary objective of their work was to analyze multiple diode circuits. They showed that it is possible to design integrated circuits that will operate at other than binary levels. One application mentioned is an Analog-to-Digital Converter in which a given voltage may be translated into any numbering system desired. Figure 1 shows the circuit that was used (Ref 8:46-48).

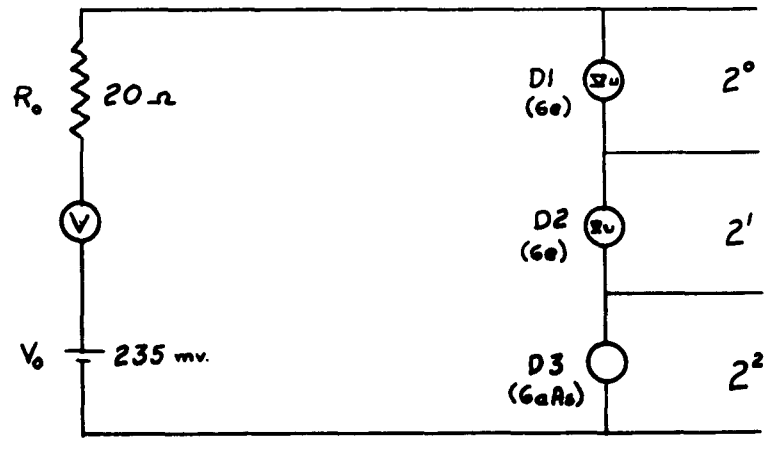


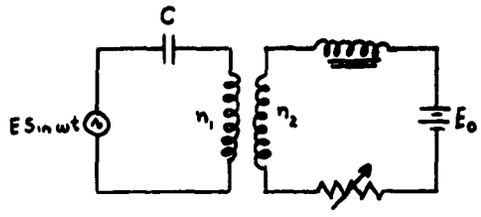
Figure 1

Analog-to-Digital Converter

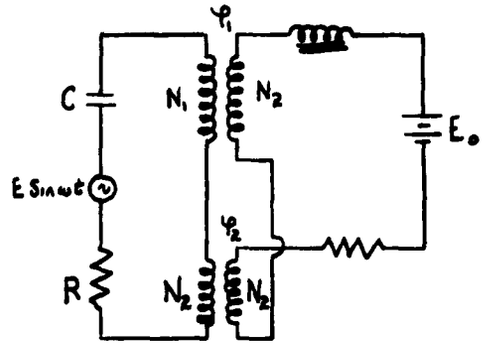
(From Ref 8:47)

Molecular electronics has now made it possible to build a device which will provide more data handling capacity by adding a third state in the same volume as is presently achievable through the use of binary devices. Initial investigations indicate that switching time, the accepted measure of speed, is in the nanosecond range. The TRINARY is the next step in the continuing struggle to process information at a rate comparable to the rate at which this information is being produced.

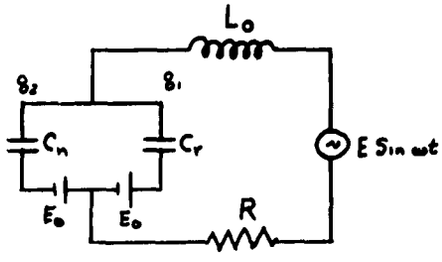
Numerous other individuals over the years have investigated ways of obtaining circuits which will provide tristable operation. R. S. MacKay and R. MacIntyre built a ternary counter from standard Flip-Flop Multivibrators which were modified to obtain an intermediate state between the usual binary output levels (Ref 6:144-149). Another approach using non-linear reactance circuits was tried by S. Kumagai and S. Kawamoto (Ref 5:432). By varying one or more of the reactance elements in their circuits they were able to obtain a transfer characteristic with three stable states as illustrated in Figure 2. A third approach, using tunnel diodes, has been used by W. F. Kosonocky to obtain a tristable circuit. The logic circuit consists of two series connected tunnel diodes and a resistor network. The three stable operating points are achieved by changing the diode characteristics (Ref 4).



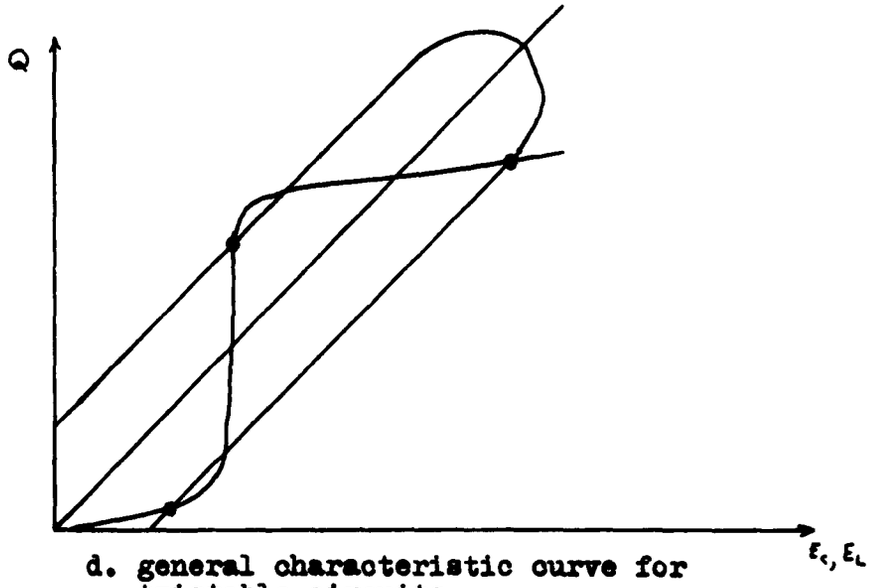
a. one element tristable circuit



c. two nonlinear inductances for a tristable circuit



b. two nonlinear capacitors in a tristable circuit



d. general characteristic curve for tristable circuits

Figure 2

Tristable Circuits of Kumagai and Kawamoto

(From Ref 5:438)

The TRINARY will be analyzed and consideration given to its possible applications. The first requirement is to present the reasons why a ternary system of logic should be considered. Following this is an analysis of the TRINARY, which is envisioned as the basic element of a ternary computation system. Although the characteristic equations obtained are without supporting experimental data, it is felt that they are general enough to permit their application to the TRINARY when it becomes available. The next chapter is an analysis of the ternary number system. This serves to provide a foundation for the remaining chapters which delve into a few of the areas where the ternary device may find wide applications. The final chapter summarizes the work accomplished in this thesis and identifies a number of topics which require further investigation.

II. The Preferability of Ternary Logic

D. R. Hartree, in his book "Calculating Instruments and Machines," states:

> "It is rash to make guesses about future progress- or anyway, to proclaim them; but my own guess is that the use of the binary system in the machine is a passing phase, characteristic of the present stage of developement (Ref 3:61)."

Justification of Hartree's statement can be made on the following basis: 1) Binary logic is based on the GO-NO GO logic of relay technology; 2) The binary system does not make the fullest use of machine components; 3) The information "explosion" requires more data handling capability per unit time than is available in a binary system; 4) A savings of 58% in storage space can be gained in going from a binary to a ternary number system (Ref 1:420).

There are two ways to process data faster. The first is by increasing the speed of operation. To achieve shorter computation times it is necessary to perform each discrete operation faster. Experiments are presently in progress to test a computer that operates at a clock rate of 500 KMc. With the advent of the maser and laser it is conceivable that operating times approaching the speed of light will be obtainable. The time required for each step in the computation process will still be finite. The second way of obtaining shorter computation times is to process more data per unit time. More data per unit time implies a more com-

plex way of representing the data than that which is available in a binary system. The decimal system of numbers would satisfy this criterion since it would be able to use less digits than are required in the binary system to represent the same quantity. For example, the number 19 in decimal requires only two digits whereas the same quantity in binary, 10011, requires five digits. Why stop at a base 10 number system if increasing the base will provide more information per digit? If that were the only consideration, the scientific community would long since have made use of this approach. Two restraints, technology and economics, must be applied to considerations of a base, or radix, other than 2. Technology, in the sense of being able to distinguish between symbols; and economics, in that the cost of a system must be considered.

The technological factors which affect the amount of significance of each digit of information are sensitivity, reliability, and noise. Electronic computers and data processing equipment depend on voltage levels to represent information. In binary systems, for example, the "1" state is associated with +10 volts and the "0" state with -30 volts. The difference of 40 volts was chosen to insure that the "0" and "1" states will be distinguishable even under the most unfavorable conditions. Under this criterion, the signals may degenerate as much as 10 volts (0, -20 volts) before the various circuits will be affected.

As more information, in the form of voltage levels, is crowded into a data unit, it becomes more difficult for the circuitry to distinguish between levels. Considering the decimal number system again, ten distinct voltage levels are required to represent one digit of decimal information. To retain a 40 volt seperation between levels would require a 400 volt range of operation. The cost of circuits which could operate over this range of voltages would make such a computer economically infeasible. In additiOn, the circuits would require more space and cooling equipment than comparable binary circuits in order to dissipate the heat generated in the circuit elements due to the high voltages present. Should the need for a 40 volt seperation be waived, it would be necessary to use far more expensive equipment to insure that the ten voltage levels be distinct. In a computer environment, in order to insure that the voltage levels remain constant, it is necessary to provide a regulated power supply for each voltage level as well as insuring that every point in the computer will have the same voltage level to work with. Because this work is not intended to describe the problems attendant on the construction of a computer let it suffice to say that the fewer the number of regulated voltages required the less complications ame expected.

In a ternary computer system three distinct voltage levels are required. However, in the ternary system the digits are represented by +1, 0, -1. Thus, all that is

required is a positive voltage, a zero voltage, and a negative voltage respectively. For those concerned with dependable signals, the virtue of this system is obvious. A good ground system and sensitivity to positive and negative signals is basically all that is required. A positive voltage, regardless of magnitude, will represent the +1 state; similarly, a negative voltage, regardless of magnitude, will represent the -1 state. The major restriction that must be placed on these voltage levels is that they be large enough to overcome spurious undesirable signals or noise.

The economic restraint on the choice of a radix is concerned with the amount of equipment required. It may be shown mathematically that the most economical number is one whose radix is e = 2.71828... .

The staff of Engineering Research Associates has demonstrated that the number of tubes required in a system of n digits in radix r is given by the following equation (Ref 1:84). The numberof tubes required is equal to the radix multiplied by the number of digits desired.

$$N = rn \tag{1}$$

The largest number that may be expressed in this system is

$$M = r^n \tag{2}$$

The economic objective is to minimize N for a fixed value of M. To do this, it is necessary first to express n in

terms of M thus:

$$\ln M = n \ln r = M'$$

and

$$n = \frac{M'}{\ln r} \tag{3}$$

Substituting N = rn in this equation gives

$$N = \frac{M'r}{\ln r} \tag{4}$$

To minimize N the derivative of N with respect to r must be zero.

$$\frac{dN}{dr} = M' \frac{\ln r - 1}{\ln^2 r} = 0 \tag{5}$$

If $M'/\ln^2 r$ is not zero, then

$$\ln r - 1 = 0 \tag{6}$$

$$r = e = 2.71828... \tag{7}$$

The nearest integer to this is 3, thus showing that a ternary system is the most desirable. Although the above derivation was performed considering tubes, it is equally valid for transistors, tunnel diodes, ternary devices, or any other multistable circuit element.

The staff of the Computation Laboratory of Harvard University has supported the use of the ternary system in preference to binary as early as 1951 (Ref 9:145). Interest in the ternary number system is growing steadily as evidenced

by recent published articles by Kumagai and Kawamoto (Ref 5), Hallworth and Heath (Ref 2), and Vacca (Ref 10). The economic and technological desirability of a radix 3 system, as discussed above, coupled with the need to process more data faster makes the ternary number system and tristable devices very important areas for investigation. An integrated tristable device has not been reported in the literature although the patent issued to Pearson suggests that industry is interested in obtaining a TRINARY. In the next chapter an analysis is made of the hypothesised volt-ampere characteristic curve of a TRINARY.

III. Characteristics of a Tristable Device

One of the principle requirements for incorporation of a device into a logical network is the knowledge of the transfer function of the device. The transfer function of an electronic device is normally represented by its volt-ampere characteristic and the equation which satisfies this characteristic curve. It is anticipated that the volt-ampere characteristic of a TRINARY will have the form shown in Figure 3. This curve may be represented by a power series expansion of the form

$$i = a_5v^5 + a_4v^4 + a_3v^3 + a_2v^2 + a_1v + a_0 \tag{8}$$

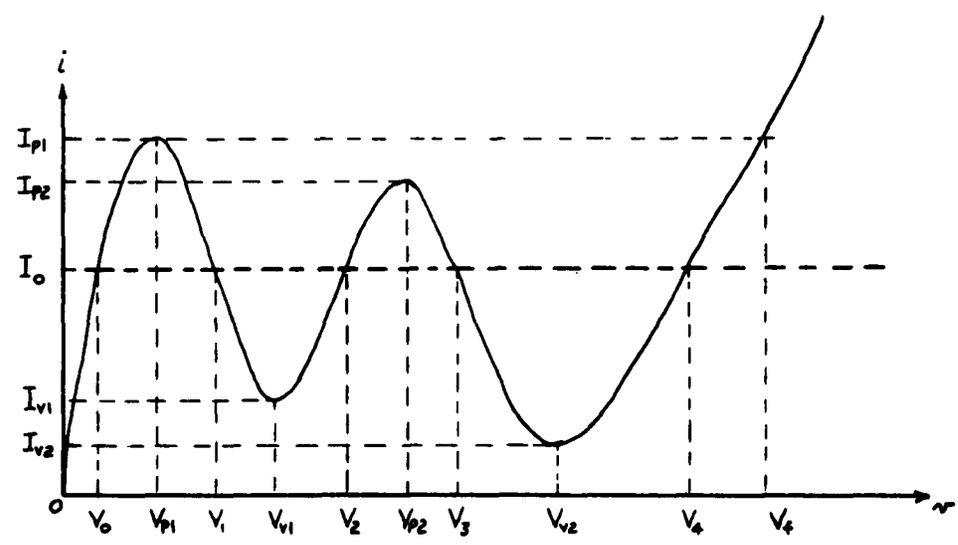


Figure 3

Volt-Ampere Characteristic of a Tristable Device

where i and v are the instantaneous current and voltage respectively, and the a's are arbitrary constants which identify the particular curve. The evaluation of the coefficients of the voltage terms as functions of the device parameters is the major problem to be solved.

The significant points are indicated in the figure. They are the peak and valley points, the voltages which correspond to the bias current I_0, and the final voltage denoted V_f. In order to solve for the coefficients of the characteristic equation the method of least squares as outlined in Wylie will be used (Ref 13:175-183). The set of equations to be used are given below in matrix form.

$$\begin{vmatrix} I_0 \\ I_0 \\ I_0 \\ I_0 \\ I_0 \\ I_{p1} \\ I_{v1} \\ I_{p2} \\ I_{v2} \end{vmatrix} = \begin{vmatrix} V_0^5 & V_0^4 & V_0^3 & V_0^2 & V_0 \\ V_1^5 & V_1^4 & V_1^3 & V_1^2 & V_1 \\ V_2^5 & V_2^4 & V_2^3 & V_2^2 & V_2 \\ V_3^5 & V_3^4 & V_3^3 & V_3^2 & V_3 \\ V_4^5 & V_4^4 & V_4^3 & V_4^2 & V_4 \\ V_{p1}^5 & V_{p1}^4 & V_{p1}^3 & V_{p1}^2 & V_{p1} \\ V_{v1}^5 & V_{v1}^4 & V_{v1}^3 & V_{v1}^2 & V_{v1} \\ V_{p2}^5 & V_{p2}^4 & V_{p2}^3 & V_{p2}^2 & V_{p2} \\ V_{v2}^5 & V_{v2}^4 & V_{v2}^3 & V_{v2}^2 & V_{v2} \end{vmatrix} \begin{vmatrix} a_5 \\ a_4 \\ a_3 \\ a_2 \\ a_1 \end{vmatrix} \qquad (9)$$

The normal equations yield:

$$I_0(V_0^5 + V_1^5 + V_2^5 + V_3^5 + V_4^5) + I_{p1}V_{p1}^5 + I_{v1}V_{v1}^5 + I_{p2}V_{p2}^5 + I_{v2}V_{v2}^5 =$$
$$a_5\sum_{n=0}^{v2} V_n^{10} + a_4\sum_{n=0}^{v2} V_n^9 + a_3\sum_{n=0}^{v2} V_n^8 + a_2\sum_{n=0}^{v2} V_n^7 + a_1\sum_{n=0}^{v2} V_n^6 \qquad (10)$$

$$I_0(V_0^4 + V_1^4 + V_2^4 + V_3^4 + V_4^4) + I_{p1}V_{p1}^4 + I_{v1}V_{v1}^4 + I_{p2}V_{p2}^4 + I_{v2}V_{v2}^4 =$$
$$a_5\sum_{n=0}^{v2} V_n^9 + a_4\sum_{n=0}^{v2} V_n^8 + a_3\sum_{n=0}^{v2} V_n^7 + a_2\sum_{n=0}^{v2} V_n^6 + a_1\sum_{n=0}^{v2} V_n^5 \qquad (11)$$

$$I_0(V_0^3 + V_1^3 + V_2^3 + V_3^3 + V_4^3) + I_{p1}V_{p1}^3 + I_{v1}V_{v1}^3 + I_{p2}V_{p2}^3 + I_{v2}V_{v2}^3 =$$
$$a_5\sum_{n=0}^{v2} V_n^8 + a_4\sum_{n=0}^{v2} V_n^7 + a_3\sum_{n=0}^{v2} V_n^6 + a_2\sum_{n=0}^{v2} V_n^5 + a_1\sum_{n=0}^{v2} V_n^4 \qquad (12)$$

$$I_0(V_0^2 + V_1^2 + V_2^2 + V_3^2 + V_4^2) + I_{p1}V_{p1}^2 + I_{v1}V_{v1}^2 + I_{p2}V_{p2}^2 + I_{v2}V_{v2}^2 =$$
$$a_5\sum_{n=0}^{v2} V_n^7 + a_4\sum_{n=0}^{v2} V_n^6 + a_3\sum_{n=0}^{v2} V_n^5 + a_2\sum_{n=0}^{v2} V_n^4 + a_1\sum_{n=0}^{v2} V_n^3 \qquad (13)$$

$$I_0(V_0 + V_1 + V_2 + V_3 + V_4) + I_{p1}V_{p1} + I_{v1}V_{v1} + I_{p2}V_{p2} + I_{v2}V_{v2} =$$
$$a_5\sum_{n=0}^{v2} V_n^6 + a_4\sum_{n=0}^{v2} V_n^5 + a_3\sum_{n=0}^{v2} V_n^4 + a_2\sum_{n=0}^{v2} V_n^3 + a_1\sum_{n=0}^{v2} V_n^2 \qquad (14)$$

where n takes on the values 0,1,2,3,4,p1,v1,p2,v2.

Rewriting the normal equations in matrix form and replacing everything on the left of the equal sign by R_s, where s corresponds to the power of the voltage terms, gives:

$$\begin{vmatrix} R_5 \\ R_4 \\ R_3 \\ R_2 \\ R_1 \end{vmatrix} = \begin{vmatrix} \Sigma V_n^{10} & \Sigma V_n^{9} & \Sigma V_n^{8} & \Sigma V_n^{7} & \Sigma V_n^{6} \\ \Sigma V_n^{9} & \Sigma V_n^{8} & \Sigma V_n^{7} & \Sigma V_n^{6} & \Sigma V_n^{5} \\ \Sigma V_n^{8} & \Sigma V_n^{7} & \Sigma V_n^{6} & \Sigma V_n^{5} & \Sigma V_n^{4} \\ \Sigma V_n^{7} & \Sigma V_n^{6} & \Sigma V_n^{5} & \Sigma V_n^{4} & \Sigma V_n^{3} \\ \Sigma V_n^{6} & \Sigma V_n^{5} & \Sigma V_n^{4} & \Sigma V_n^{3} & \Sigma V_n^{2} \end{vmatrix} \begin{vmatrix} a_5 \\ a_4 \\ a_3 \\ a_2 \\ a_1 \end{vmatrix} \quad (15)$$

Without the particular values of the voltages and currents this is the equation which must be solved to obtain the coefficients of the terms in the power series representation of the characteristic curve.

In order to obtain a less involved equation a symmetrical characteristic curve, as shown in Figure 4, is assumed.

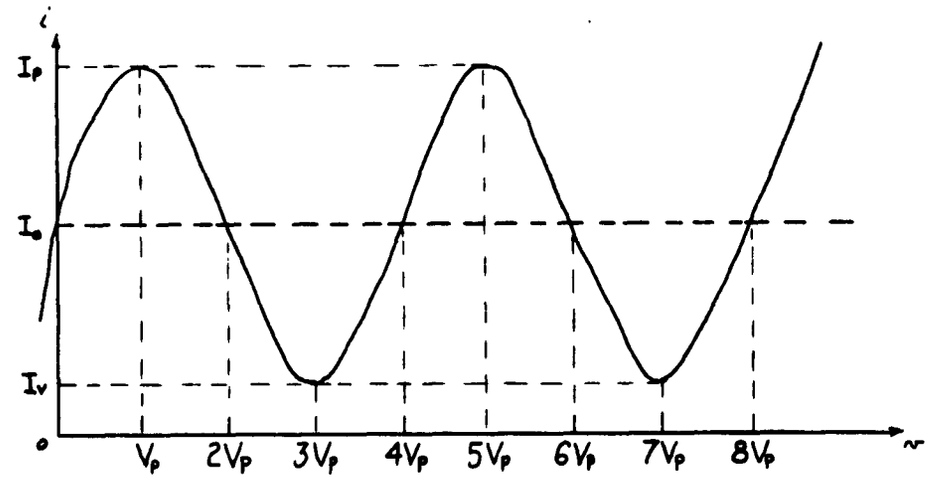


Figure 4

Symmetrical Characteristic Curve

Although generality has been sacrificed, the resulting solution gives a reasonable approximation to the expected characteristic curve shown in Figure 3.

The equal increments in the voltages of the significant points on the curve permits the use of orthogonal polynomials in the least squares solution. The procedure described on pages 179-183 of Wylie will be used.

The first step is to introduce the auxiliary variable $x = V/V_{pl}$ which will take on the values 0,1,2,3,4,5,6,7,8, when V takes on the values 0, V_{pl}, $2V_{pl}$, $3V_{pl}$, $4V_{pl}$, $5V_{pl}$, $6V_{pl}$, $7V_{pl}$, and $8V_{pl}$ respectively. Next the orthogonal polynomials must be computed from the formula

$$P_{nm}(x) = \sum_{i=0}^{m} (-1)^i \binom{m}{i} \binom{m+i}{i} \frac{(x)^i}{(n)^i} \tag{16}$$

where m = 0,1,2,3,4,5 and n = 8 for this problem.

The polynomials are:

$$P_{80}(x) = 1 \tag{17}$$

$$P_{81}(x) = 1 - \frac{x}{4} \tag{18}$$

$$P_{82}(x) = 1 - \frac{3}{4}x + \frac{6}{56}x(x-1) \tag{19}$$

$$P_{83}(x) = 1 - \frac{3}{2}x + \frac{30}{56}x(x-1) - \frac{20}{336}x(x-1)(x-2) \tag{20}$$

$$P_{84}(x) = 1 - \frac{20}{8}x + \frac{90}{56}x(x-1) - \frac{140}{336}x(x-1)(x-2) + \frac{70}{1680}x(x-1)(x-2)(x-3) \tag{21}$$

$$P_{85}(x) = 1 - \frac{30}{8}x + \frac{210}{56}x(x-1) - \frac{560}{336}x(x-1)(x-2)$$
$$+ \frac{630}{1680}x(x-1)(x-2)(x-3)$$
$$- \frac{252}{6720}x(x-1)(x-2)(x-3)(x-4) \tag{22}$$

The solutions for values of $x = 0,1,2,3,4,5,6,7$, and 8 are given in Table 1.

The coefficients of the 5th order equation are determined by the formula

$$a_i = \frac{\sum_{x=0}^{n} I(x)P_{ni}(x)}{\sum_{x=0}^{n} P_{ni}^{2}(x)} \tag{23}$$

where $i = 0,1,2,3,4,5$. The quantity $\sum_{x=0}^{n} P_{ni}^{2}(x)$ is obtainable from the general formula

$$\sum_{x=0}^{n} P_{ni}^{2}(x) = \frac{(n+i+1)^{(i+1)}}{(2i+n)(n)^{(i)}} \tag{24}$$

where $i = 0,1,2,3,4,5$. The particular equations are:

$$\sum_{x=0}^{n} P_{n0}^{2} = n+1 \tag{25}$$

$$\sum_{x=0}^{n} P_{n1}^{2} = \frac{(n+1)(n+2)}{3n} \tag{26}$$

$$\sum_{x=0}^{n} P_{n2}^{2} = \frac{(n+1)(n+2)(n+3)}{5n(n-1)} \tag{27}$$

$$\sum_{x=0}^{n} P_{n3}^{2} = \frac{(n+1)(n+2)(n+3)(n+4)}{7n(n-1)(n-2)} \tag{28}$$

Table I

Calculations

x	I	P_{80}	P_{81}	P_{82}	P_{83}	P_{84}	P_{85}
0	I_0	1.0	1.000	1.00000	1.00000	1.00000	1.000
1	I_p	1.0	0.750	0.25000	-0.50000	-1.50000	-2.750
2	I_0	1.0	0.500	-0.28571	-0.92858	-0.78572	1.000
3	I_v	1.0	0.250	-0.60715	-0.64286	0.64285	2.250
4	I_0	1.0	0.000	-0.71429	0.00000	1.28571	0.000
5	I_p	1.0	-0.250	-0.60715	0.64286	0.64285	-2.250
6	I_0	1.0	-0.500	-0.28572	0.92857	-0.78532	-1.000
7	I_v	1.0	-0.750	0.25000	0.50000	-1.50000	2.750
8	I_0	1.0	-1.000	1.00000	-1.00000	1.00000	-1.000

$$\sum_{x=0}^{8} P_{80}^{2}(x) = 9.00000$$

$$\sum_{x=0}^{8} P_{81}^{2}(x) = 3.75000$$

$$\sum_{x=0}^{8} P_{82}^{2}(x) = 3.53571$$

$$\sum_{x=0}^{8} P_{83}^{2}(x) = 5.05102$$

$$\sum_{x=0}^{8} P_{84}^{2}(x) = 10.21428$$

$$\sum_{x=0}^{8} P_{85}^{2}(x) = 29.25000$$

$$\sum_{x=0}^{n} P_{n4}{}^{2} = \frac{(n+1)(n+2)(n+3)(n+4)(n+5)}{9n(n-1)(n-2)(n-3)} \tag{29}$$

$$\sum_{x=0}^{n} P_{n5}{}^{2} = \frac{(n+1)(n+2)(n+3)(n+4)(n+5)(n+6)}{11n(n-1)(n-2)(n-3)(n-4)} \tag{30}$$

For n = 8, these values are given in Table I. The coefficients are then found to be as follows:

$$a_0 = 0.55555\ I_0 + 0.22222\ I_p + 0.22222\ I_v \tag{31}$$

$$a_1 = 0 + 0.13333\ I_p - 0.13333\ I_v \tag{32}$$

$$a_2 = 0.20201\ I_0 - 0.10101\ I_p - 0.10101\ I_v \tag{33}$$

$$a_3 = 0 + 0.02828\ I_p - 0.02828\ I_v \tag{34}$$

$$a_4 = 0.16786\ I_0 - 0.08391\ I_p - 0.08391\ I_v \tag{35}$$

$$a_5 = 0 - 0.17094\ I_p + 0.17094\ I_v \tag{36}$$

In terms of x the equation of the curve is given by

$$v = a_0P_{80}(x) + a_1P_{81}(x) + \ldots + a_5P_{85}(x) \tag{37}$$

Substituting for $P_{8i}(x)$ and combining terms this may be written as:

$$i = a_0 + a_1 + a_2 + a_3 + a_4 + a_5$$
$$-x(0.25000a_1 + 0.85714a_2 + 2.15475a_3 + 5.19047a_4$$
$$+ 13.98333a_5)$$

$$+x^2(0.10714a_2 + 0.71428a_3 + 3.31547a_4 + 14.75000a_5)$$

$$-x^3(0.05952a_3 + 0.66666a_4 + 5.22916a_5)$$

$$+x^4(0.04166a_4 + 0.75000a_5)$$

$$-x^5(0.03750a_5) \tag{38}$$

Substituting for a_i and x and combining terms gives the final equation:

$$\begin{aligned} i = \quad & 0.92542\ I_0 + 0.02796\ I_p + 0.04663\ I_v \\ & - \frac{V}{V_p}\ (1.04443\ I_0 - 2.81816\ I_p + 1.77393\ I_v) \\ & + \frac{V}{V_p}^{2}(0.57818\ I_0 - 2.79019\ I_p + 2.21214\ I_v) \\ & - \frac{V}{V_p}^{3}(0.11191\ I_0 - 0.94813\ I_p + 0.83625\ I_v) \\ & + \frac{V}{V_p}^{4}(0.00699\ I_0 - 0.13170\ I_p + 0.12471\ I_v) \\ & + \frac{V}{V_p}^{5}(\quad 0 \quad + 0.00641\ I_p - 0.00641\ I_v) \end{aligned} \tag{39}$$

It is reasonable to assume that I_v will be negligible with respect to I_0 if not actually zero. Under this condition I_0 will be 0.5 I_p. With these considerations the equation becomes, with i normalized to I_p:

$$\begin{aligned} i = \ & 0.49067 + 2.29594\ \frac{V}{V_p} - 2.50110\left(\frac{V}{V_p}\right)^2 \\ & + 0.89218\left(\frac{V}{V_p}\right)^3 - 0.12820\left(\frac{V}{V_p}\right)^4 + 0.00641\left(\frac{V}{V_p}\right)^5 \end{aligned} \tag{40}$$

The curve which satisfies this equation is shown in Figure 5. The data for this curve is tabulated in Appendix B. Although this curve does not exactly match the symmetrical curve from which the approximation was made, there is a definite similarity to the characteristic curve that is expected to describe the TRINARY. Unfortunately, the verification of this effort will have to await the availability of an actual tristable device.

The TRINARY, whose characteristic equation has been determined, will be used in circuitry which functions in the ternary number system. The mathematics of this system must be considered before circuits can be developed. The next chapter discusses ternary mathematics as well as the conversion between various number systems.

Cycle 1
Cycle 2
Cycle 3
Cycle 4
Cycle 5
Cycle 6
Cycle 7
Cycle 8
Cycle 9
Cycle 10
Cycle 11
Cycle 12
Cycle 13
Cycle 14
Cycle 15
Cycle 16
Cycle 17
Cycle 18
Cycle 19
Cycle 20
Cycle 21
Cycle 22
Cycle 23
Cycle 24
Cycle 25
Cycle 26
Cycle 27
Cycle 28
Cycle 29
Cycle 30
Cycle 31
Cycle 32
Cycle 33
Cycle 34
Cycle 35
Cycle 36
Cycle 37
Cycle 38
Cycle 39
Cycle 40
Cycle 41
Cycle 42
Cycle 43
Cycle 44
Cycle 45
Cycle 46
Cycle 47
Cycle 48
Cycle 49
Cycle 50
Cycle 51
Cycle 52
Cycle 53
Cycle 54
Cycle 55
Cycle 56
Cycle 57
Cycle 58
Cycle 59
Cycle 60
Cycle 61
Cycle 62
Cycle 63
Cycle 64
Cycle 65
Cycle 66
Cycle 67
Cycle 68
Cycle 69
Cycle 70
Cycle 71
Cycle 72
Cycle 73
Cycle 74
Cycle 75
Cycle 76
Cycle 77
Cycle 78
Cycle 79
Cycle 80
Cycle 81
Cycle 82
Cycle 83
Cycle 84
Cycle 85
Cycle 86
Cycle 87
Cycle 88
Cycle 89
Cycle 90
Cycle 91
Cycle 92
Cycle 93
Cycle 94
Cycle 95
Cycle 96
Cycle 97
Cycle 98
Cycle 99
Cycle 100
Cycle 101
Cycle 102
Cycle 103
Cycle 104
Cycle 105
Cycle 106
Cycle 107
Cycle 108
Cycle 109
Cycle 110
Cycle 111
Cycle 112
Cycle 113
Cycle 114
Cycle 115
Cycle 116
Cycle 117
Cycle 118
Cycle 119
Cycle 120
Cycle 121
Cycle 122
Cycle 123
Cycle 124
Cycle 125
Cycle 126
Cycle 127
Cycle 128
Cycle 129
Cycle 130
Cycle 131
Cycle 132
Cycle 133
Cycle 134
Cycle 135
Cycle 136
Cycle 137
Cycle 138
Cycle 139
Cycle 140
Cycle 141
Cycle 142
Cycle 143
Cycle 144
Cycle 145
Cycle 146
Cycle 147
Cycle 148
Cycle 149
Cycle 150
Cycle 151
Cycle 152
Cycle 153
Cycle 154
Cycle 155
Cycle 156
Cycle 157
Cycle 158
Cycle 159
Cycle 160
Cycle 161
Cycle 162
Cycle 163
Cycle 164
Cycle 165
Cycle 166
Cycle 167
Cycle 168
Cycle 169
Cycle 170
Cycle 171
Cycle 172
Cycle 173
Cycle 174
Cycle 175
Cycle 176
Cycle 177
Cycle 178
Cycle 179
Cycle 180
Cycle 181
Cycle 182
Cycle 183
Cycle 184
Cycle 185
Cycle 186
Cycle 187
Cycle 188
Cycle 189
Cycle 190
Cycle 191
Cycle 192
Cycle 193
Cycle 194
Cycle 195
Cycle 196
Cycle 197
Cycle 198
Cycle 199
Cycle 200
Cycle 201
Cycle 202
Cycle 203
Cycle 204
Cycle 205
Cycle 206
Cycle 207
Cycle 208
Cycle 209
Cycle 210
Cycle 211
Cycle 212
Cycle 213
Cycle 214
Cycle 215
Cycle 216
Cycle 217
Cycle 218
Cycle 219
Cycle 220
Cycle 221
Cycle 222
Cycle 223
Cycle 224
Cycle 225
Cycle 226
Cycle 227
Cycle 228
Cycle 229
Cycle 230
Cycle 231
Cycle 232
Cycle 233
Cycle 234
Cycle 235
Cycle 236
Cycle 237
Cycle 238
Cycle 239
Cycle 240
Cycle 241
Cycle 242
Cycle 243
Cycle 244
Cycle 245
Cycle 246
Cycle 247
Cycle 248
Cycle 249
Cycle 250
Cycle 251
Cycle 252
Cycle 253
Cycle 254
Cycle 255
Cycle 256
Cycle 257
Cycle 258
Cycle 259
Cycle 260
Cycle 261
Cycle 262
Cycle 263
Cycle 264
Cycle 265
Cycle 266
Cycle 267
Cycle 268
Cycle 269
Cycle 270
Cycle 271
Cycle 272
Cycle 273
Cycle 274
Cycle 275
Cycle 276
Cycle 277
Cycle 278
Cycle 279
Cycle 280
Cycle 281
Cycle 282
Cycle 283
Cycle 284
Cycle 285
Cycle 286
Cycle 287
Cycle 288
Cycle 289
Cycle 290
Cycle 291
Cycle 292
Cycle 293
Cycle 294
Cycle 295
Cycle 296
Cycle 297
Cycle 298
Cycle 299
Cycle 300
Cycle 301
Cycle 302
Cycle 303
Cycle 304
Cycle 305
Cycle 306
Cycle 307
Cycle 308
Cycle 309
Cycle 310
Cycle 311
Cycle 312
Cycle 313
Cycle 314
Cycle 315
Cycle 316
Cycle 317
Cycle 318
Cycle 319
Cycle 320
Cycle 321
Cycle 322
Cycle 323
Cycle 324
Cycle 325
Cycle 326
Cycle 327
Cycle 328
Cycle 329
Cycle 330
Cycle 331
Cycle 332
Cycle 333
Cycle 334
Cycle 335
Cycle 336
Cycle 337
Cycle 338
Cycle 339
Cycle 340
Cycle 341
Cycle 342
Cycle 343
Cycle 344
Cycle 345
Cycle 346
Cycle 347
Cycle 348
Cycle 349
Cycle 350
Cycle 351
Cycle 352
Cycle 353
Cycle 354
Cycle 355
Cycle 356
Cycle 357
Cycle 358
Cycle 359
Cycle 360
Cycle 361
Cycle 362
Cycle 363
Cycle 364
Cycle 365
Cycle 366
Cycle 367
Cycle 368
Cycle 369
Cycle 370
Cycle 371
Cycle 372
Cycle 373
Cycle 374
Cycle 375
Cycle 376
Cycle 377
Cycle 378
Cycle 379
Cycle 380
Cycle 381
Cycle 382
Cycle 383
Cycle 384
Cycle 385
Cycle 386
Cycle 387
Cycle 388
Cycle 389
Cycle 390
Cycle 391
Cycle 392
Cycle 393
Cycle 394
Cycle 395
Cycle 396
Cycle 397
Cycle 398
Cycle 399
Cycle 400
Cycle 401
Cycle 402
Cycle 403
Cycle 404
Cycle 405
Cycle 406
Cycle 407
Cycle 408
Cycle 409
Cycle 410
Cycle 411
Cycle 412
Cycle 413
Cycle 414
Cycle 415
Cycle 416
Cycle 417
Cycle 418
Cycle 419
Cycle 420
Cycle 421
Cycle 422
Cycle 423
Cycle 424
Cycle 425
Cycle 426
Cycle 427
Cycle 428
Cycle 429
Cycle 430
Cycle 431
Cycle 432
Cycle 433
Cycle 434
Cycle 435
Cycle 436
Cycle 437
Cycle 438
Cycle 439
Cycle 440
Cycle 441
Cycle 442
Cycle 443
Cycle 444
Cycle 445
Cycle 446
Cycle 447
Cycle 448
Cycle 449
Cycle 450
Cycle 451
Cycle 452
Cycle 453
Cycle 454
Cycle 455
Cycle 456
Cycle 457
Cycle 458
Cycle 459
Cycle 460
Cycle 461
Cycle 462
Cycle 463
Cycle 464
Cycle 465
Cycle 466
Cycle 467
Cycle 468
Cycle 469
Cycle 470
Cycle 471
Cycle 472
Cycle 473
Cycle 474
Cycle 475
Cycle 476
Cycle 477
Cycle 478
Cycle 479
Cycle 480
Cycle 481
Cycle 482
Cycle 483
Cycle 484
Cycle 485
Cycle 486
Cycle 487
Cycle 488
Cycle 489
Cycle 490
Cycle 491
Cycle 492
Cycle 493
Cycle 494
Cycle 495
Cycle 496
Cycle 497
Cycle 498
Cycle 499
Cycle 500
Cycle 501
Cycle 502
Cycle 503
Cycle 504
Cycle 505
Cycle 506
Cycle 507
Cycle 508
Cycle 509
Cycle 510
Cycle 511
Cycle 512
Cycle 513
Cycle 514
Cycle 515
Cycle 516
Cycle 517
Cycle 518
Cycle 519
Cycle 520
Cycle 521
Cycle 522
Cycle 523
Cycle 524
Cycle 525
Cycle 526
Cycle 527
Cycle 528
Cycle 529
Cycle 530
Cycle 531
Cycle 532
Cycle 533
Cycle 534
Cycle 535
Cycle 536
Cycle 537
Cycle 538
Cycle 539
Cycle 540
Cycle 541
Cycle 542
Cycle 543
Cycle 544
Cycle 545
Cycle 546
Cycle 547
Cycle 548
Cycle 549
Cycle 550
Cycle 551
Cycle 552
Cycle 553
Cycle 554
Cycle 555
Cycle 556
Cycle 557
Cycle 558
Cycle 559
Cycle 560
Cycle 561
Cycle 562
Cycle 563
Cycle 564
Cycle 565
Cycle 566
Cycle 567
Cycle 568
Cycle 569
Cycle 570
Cycle 571
Cycle 572
Cycle 573
Cycle 574
Cycle 575
Cycle 576
Cycle 577
Cycle 578
Cycle 579
Cycle 580
Cycle 581
Cycle 582
Cycle 583
Cycle 584
Cycle 585
Cycle 586
Cycle 587
Cycle 588
Cycle 589
Cycle 590
Cycle 591
Cycle 592
Cycle 593
Cycle 594
Cycle 595
Cycle 596
Cycle 597
Cycle 598
Cycle 599
Cycle 600
Cycle 601
Cycle 602
Cycle 603
Cycle 604
Cycle 605
Cycle 606
Cycle 607
Cycle 608
Cycle 609
Cycle 610
Cycle 611
Cycle 612
Cycle 613
Cycle 614
Cycle 615
Cycle 616
Cycle 617
Cycle 618
Cycle 619
Cycle 620
Cycle 621
Cycle 622
Cycle 623
Cycle 624
Cycle 625
Cycle 626
Cycle 627
Cycle 628
Cycle 629
Cycle 630
Cycle 631
Cycle 632
Cycle 633
Cycle 634
Cycle 635
Cycle 636
Cycle 637
Cycle 638
Cycle 639
Cycle 640
Cycle 641
Cycle 642
Cycle 643
Cycle 644
Cycle 645
Cycle 646
Cycle 647
Cycle 648
Cycle 649
Cycle 650
Cycle 651
Cycle 652
Cycle 653
Cycle 654
Cycle 655
Cycle 656
Cycle 657
Cycle 658
Cycle 659
Cycle 660
Cycle 661
Cycle 662
Cycle 663
Cycle 664
Cycle 665
Cycle 666
Cycle 667
Cycle 668
Cycle 669
Cycle 670
Cycle 671
Cycle 672
Cycle 673
Cycle 674
Cycle 675
Cycle 676
Cycle 677
Cycle 678
Cycle 679
Cycle 680
Cycle 681
Cycle 682
Cycle 683
Cycle 684
Cycle 685
Cycle 686
Cycle 687
Cycle 688
Cycle 689
Cycle 690
Cycle 691
Cycle 692
Cycle 693
Cycle 694
Cycle 695
Cycle 696
Cycle 697
Cycle 698
Cycle 699
Cycle 700
Cycle 701
Cycle 702
Cycle 703
Cycle 704
Cycle 705
Cycle 706
Cycle 707
Cycle 708
Cycle 709
Cycle 710
Cycle 711
Cycle 712
Cycle 713
Cycle 714
Cycle 715
Cycle 716
Cycle 717
Cycle 718
Cycle 719
Cycle 720
Cycle 721
Cycle 722
Cycle 723
Cycle 724
Cycle 725
Cycle 726
Cycle 727
Cycle 728
Cycle 729
Cycle 730
Cycle 731
Cycle 732
Cycle 733
Cycle 734
Cycle 735
Cycle 736
Cycle 737
Cycle 738
Cycle 739
Cycle 740
Cycle 741
Cycle 742
Cycle 743
Cycle 744
Cycle 745
Cycle 746
Cycle 747
Cycle 748
Cycle 749
Cycle 750
Cycle 751
Cycle 752
Cycle 753
Cycle 754
Cycle 755
Cycle 756
Cycle 757
Cycle 758
Cycle 759
Cycle 760
Cycle 761
Cycle 762
Cycle 763
Cycle 764
Cycle 765
Cycle 766
Cycle 767
Cycle 768
Cycle 769
Cycle 770
Cycle 771
Cycle 772
Cycle 773
Cycle 774
Cycle 775
Cycle 776
Cycle 777
Cycle 778
Cycle 779
Cycle 780
Cycle 781
Cycle 782
Cycle 783
Cycle 784
Cycle 785
Cycle 786
Cycle 787
Cycle 788
Cycle 789
Cycle 790
Cycle 791
Cycle 792
Cycle 793
Cycle 794
Cycle 795
Cycle 796
Cycle 797
Cycle 798
Cycle 799
Cycle 800
Cycle 801
Cycle 802
Cycle 803
Cycle 804
Cycle 805
Cycle 806
Cycle 807
Cycle 808
Cycle 809
Cycle 810
Cycle 811
Cycle 812
Cycle 813
Cycle 814
Cycle 815
Cycle 816
Cycle 817
Cycle 818
Cycle 819
Cycle 820
Cycle 821
Cycle 822
Cycle 823
Cycle 824
Cycle 825
Cycle 826
Cycle 827
Cycle 828
Cycle 829
Cycle 830
Cycle 831
Cycle 832
Cycle 833
Cycle 834
Cycle 835
Cycle 836
Cycle 837
Cycle 838
Cycle 839
Cycle 840
Cycle 841
Cycle 842
Cycle 843
Cycle 844
Cycle 845
Cycle 846
Cycle 847
Cycle 848
Cycle 849
Cycle 850
Cycle 851
Cycle 852
Cycle 853
Cycle 854
Cycle 855
Cycle 856
Cycle 857
Cycle 858
Cycle 859
Cycle 860
Cycle 861
Cycle 862
Cycle 863
Cycle 864
Cycle 865
Cycle 866
Cycle 867
Cycle 868
Cycle 869
Cycle 870
Cycle 871
Cycle 872
Cycle 873
Cycle 874
Cycle 875
Cycle 876
Cycle 877
Cycle 878
Cycle 879
Cycle 880
Cycle 881
Cycle 882
Cycle 883
Cycle 884
Cycle 885
Cycle 886
Cycle 887
Cycle 888
Cycle 889
Cycle 890
Cycle 891
Cycle 892
Cycle 893
Cycle 894
Cycle 895
Cycle 896
Cycle 897
Cycle 898
Cycle 899
Cycle 900
Cycle 901
Cycle 902
Cycle 903
Cycle 904
Cycle 905
Cycle 906
Cycle 907
Cycle 908
Cycle 909
Cycle 910
Cycle 911
Cycle 912
Cycle 913
Cycle 914
Cycle 915
Cycle 916
Cycle 917
Cycle 918
Cycle 919
Cycle 920
Cycle 921
Cycle 922
Cycle 923
Cycle 924
Cycle 925
Cycle 926
Cycle 927
Cycle 928
Cycle 929
Cycle 930
Cycle 931
Cycle 932
Cycle 933
Cycle 934
Cycle 935
Cycle 936
Cycle 937
Cycle 938
Cycle 939
Cycle 940
Cycle 941
Cycle 942
Cycle 943
Cycle 944
Cycle 945
Cycle 946
Cycle 947
Cycle 948
Cycle 949
Cycle 950
Cycle 951
Cycle 952
Cycle 953
Cycle 954
Cycle 955
Cycle 956
Cycle 957
Cycle 958
Cycle 959
Cycle 960
Cycle 961
Cycle 962
Cycle 963
Cycle 964
Cycle 965
Cycle 966
Cycle 967
Cycle 968
Cycle 969
Cycle 970
Cycle 971
Cycle 972
Cycle 973
Cycle 974
Cycle 975
Cycle 976
Cycle 977
Cycle 978
Cycle 979
Cycle 980
Cycle 981
Cycle 982
Cycle 983
Cycle 984
Cycle 985
Cycle 986
Cycle 987
Cycle 988
Cycle 989
Cycle 990
Cycle 991
Cycle 992
Cycle 993
Cycle 994
Cycle 995
Cycle 996
Cycle 997
Cycle 998
Cycle 999
Cycle 1000

IV. The Ternary Number System

A number in any number system can be written in the form

$$N = S_0R^0 + S_1R^1 + \dots + S_nR^n \tag{41}$$

where N is the number to be represented, S is the symbol of the system, and R is the radix of the system. In practice it is usual to write only the system symbols, one after the other, omitting the radix. The symbols are written in the opposite order to that shown above such that:

$$N = S_nS_{n-1}\dots S_1S_0 \tag{42}$$

In the ternary system the radix is three (R = 3) and the symbols are normally expressed as zero, one, and two. The general form of a number expressed in the ternary system is

$$N = S_03^0 + S_13^1 + \dots + S_n3^n \tag{43}$$

or

$$N = S_o + 3S_1 + 9S_2 + \dots + 3^nS_n \tag{44}$$

As a specific example, the number 67 is expressed as

$$\begin{aligned} 67 &= (1)3^0 + (1)3^1 + (1)3^2 + (2)3^3 \\ &= 1 + 3 + 9 + 54 \end{aligned}$$

This is written as 2111 in ternary.

Any decimal number may be converted into the corresponding ternary number by finding each of the coefficients of the

radix term seperately. The procedure is to divide the number by the radix, 3, and note the remainder. The quotient of this division is then divided by 3 and the remainder noted. This operation is continued until the dividend is less than the divisor. The remainder from each division corresponds to the symbols S_0, S_1, S_2, ... S_n respectively. This may be formulated as follows:

$$\frac{N}{3} = N' + S_0; \quad \frac{N'}{3} = N'' + S_1; \quad \frac{N''}{3} = N''' + S_2; \text{ etc.} \tag{45}$$

Using the decimal number 67 to illustrate this method gives

$$\frac{67}{3} = 22 + 1 \qquad S_0 = 1$$

$$\frac{22}{3} = 7 + 1 \qquad S_1 = 1$$

$$\frac{7}{3} = 2 + 1 \qquad S_2 = 1$$

$$\frac{2}{3} = 0 + 2 \qquad S_3 = 2$$

The ternary number is 2111.

Since most computers are in the binary form, the conversion between binary and ternary is of special importance. This conversion is performed in the same manner as was done with the decimal number. However, since binary is a radix less than three the divisor 3 is expressed as the binary 11. The remainders formed after each division are in the binary system and must be converted to ternary by the following rule:

If the remainder is 0 then S = 0.

If the remainder is 1 then S = 1.

If the remainder is 10 then S = 2.

The following example illustrates the conversion of the binary number 1000011 into ternary.

$$\frac{N}{3} = \frac{1000011}{11} = 10110 \qquad \text{Remainder 1,} \quad S_0 = 1$$

$$\frac{N'}{3} = \frac{10110}{11} = 111 \qquad \text{Remainder 1,} \quad S_1 = 1$$

$$\frac{N''}{3} = \frac{111}{11} = 10 \qquad \text{Remainder 1,} \quad S_2 = 1$$

$$\frac{N'''}{3} = \frac{10}{11} = 0 \qquad \text{Remainder 10,} \quad S_3 = 2$$

The ternary number is 2111.

In the conversion from ternary to binary, a higher to lower radix, the division operation is performed and the remainders give the symbols directly in binary.

The conversion operation from one number system to another may be summarized in the following manner. The number in the system which is being converted is divided by the radix number of the other system expressed in terms of the system being converted. If the new radix is smaller than the radix of the old system then the remainders are in terms of the new system. If the new radix is larger than the radix of the system being converted the remainders must be converted into the new system through the appropriate numeric relations. The remainders from the successive divisions are the symbols of the new system in ascending order.

The mathematical operations performed on ternary numbers are similar to those performed on decimal numbers. When the numbers are added in the decimal system a carry to the next higher order of ten is effected, e.g. 6 + 5 = 11. The same operation is performed in the ternary system except that three digits are used instead of ten. Ternary addition is illustrated in the example showing the result of successive addition of 1 to a decimal and a ternary number. Table II gives the basic rules of ternary addition.

Table II
Rules of Ternary Addition

	0	1	2
0	0	1	2
1	1	2	10
2	2	10	11

Decimal	Ternary
0	000
1	1
2	2
3	10
4	11
5	12
6	20
7	21
8	22
9	100

Subtraction takes the same form as with decimal numbers. If the minuend is less than the subtrahend, a digit is borrowed from the next higher order of the minuend number. The subtraction of ternary numbers is shown in Table III and the accompanying example.

Table III
Rules of Ternary Subtraction

	Subtrahend		
Minuend	0	1	2
10	10	2	1
11	11	10	2
12	12	11	10

The following are examples of ternary subtraction.

A	- B	= Difference	Borrow	Decimal	Ternary
0	0	0	0	10	101
				9	100
0	1	2	1	8	22
				7	21
0	2	1	1	6	20
				5	12
1	0	1	0	4	11
				3	10
1	1	0	0	2	2
				1	1
1	2	2	1	0	0
2	0	2	0		
2	1	1	0		
2	2	0	0		

Multiplication of any two numbers is performed by adding the multiplicand to itself as many times as the multiplier designates, e.g. 4 x 5 = 4 + 4 + 4 + 4 + 4. Rather than perform this repeated addition it is customary to use a table which defines all the primary multiplications as shown in Table IV.

Table IV
Ternary Multiplication Table

	0	1	2
0	0	0	0
1	0	1	2
2	0	2	11

When ternary numbers greater than those shown in the table are to be multiplied, the same procedure is followed as in the decimal system. The multiplicand is multiplied seperately by each number of the multiplier and all the partial products are added together. This is illustrated by the following example.

```
     2102
    x1201
    -----
     2102
    0000
   11211
   2102
  -------
  11002202
```

Division of ternary numbers is performed in the same manner as in decimal division except that the rules of ternary addition and subtraction are adhered to. This is illustrated by the following example.

```
              2102
1201 √11002202
       10102
         2002
         1201
          10102
          10102
```

To complete the coverage of the ternary number system it is necessary to include fractional numbers. Fractional numbers are expressed as the sum of negative powers of the radix as:

$$N = D_1R^{-1} + D_2R^{-2} + \ldots + D_mR^{-m} \tag{46}$$

or

$$N = \frac{D_1}{3} + \frac{D_2}{9} + \frac{D_3}{27} + \ldots + \frac{D_m}{3^m} \tag{47}$$

A number which includes fractions may be expressed as:

$$N = S_n \ldots S_2S_1S_0 . D_1D_2 \ldots D_m \tag{48}$$

The conversion between number systems of fractional numbers is effected by a multiplication process instead of by division. To convert a decimal fraction to ternary it is necessary to multiply the decimal fraction by 3. The whole number which results is the coefficient D_1. The fractional part of the product is then multiplied by 3 and the whole number in the product is D_2. This process is continued until the fractional part of the product is zero. If the process is halted before the operation terminates, the last digit is rounded off. The conversion of the decimal 0.4 to ternary will illustrate this procedure.

$0.4 \times 3 = 1.2$	$D_1 = 1$
$0.2 \times 3 = 0.6$	$D_2 = 0$
$0.6 \times 3 = 1.8$	$D_3 = 1$
$0.8 \times 3 = 2.4$	$D_4 = 2$

$$0.4 \times 3 = 1.2 \qquad D_5 = 1$$

$$0.2 \times 3 = 0.6 \qquad D_6 = 0$$

The ternary number is 0.10121012... . This process can be continued with the same pattern repeating indefinitely. Converting from ternary to decimal is performed by dividing each ternary symbol D_m by the corresponding power of 3 and adding the results.

In general, to convert from one system to another the fractional number of the first system is multiplied by the radix number of the second system. The whole number part of the product is the symbol in the new system. The fractional part of the product is then multiplied by the new radix and the next significant digit of the new number is the whole number part of this product. The process is continued until the fractional part of the product becomes zero or the desired degree of accuracy is reached. The conditions relating to the relative size of the radices mentioned earlier under whole number conversion applies equally well to the fractional numbers.

Computer operation in the ternary number system will utilize the negative, zero, and positive voltage levels instead of the symbols 0, 1, and 2. The relationship between the two sets of symbols are:

$$0 = 0$$

$$1 = +$$

$$2 = +-$$

The rules of ternary mathematics using the -, 0, + symbols are shown in Table V.

Table V
Ternary Addition and Multiplication

Addition

	-	0	+
-	-+	-	0
0	-	0	+
+	0	+	+-

Multiplication

	-	0	+
-	+	0	-
0	0	0	0
+	-	0	+

An interesting and useful feature of this system is that both positive and negative numbers can be represented directly without the need of a sign bit or complement circuit. The symbols +, 0, - represent respectively the presence of a power of three, the absence of a power of three, and the presence of a power of three in the negative sense. The decimal number +67 is expressed in ternary as:

$$+67 = +++-+ = +1 + 3 + 9 - 27 + 81$$

The decimal number -67 is expressed in ternary as:

$$-67 = ---+- = -1 - 3 - 9 + 27 - 81$$

It will be noted that a negative number is represented by the opposite, or inverse, of the symbols which represent a positive number of the same magnitude.

The ternary number 2121 is taken as an illustration of

this system. The number is converted into -, 0, + symbolism as follows:

$$\begin{array}{rcr} 2000 & = & +-000 \\ 100 & = & +00 \\ 20 & = & +-0 \\ 1 & = & + \\ \hline 2121 & = & +0--+ \end{array}$$

Converting each of these numbers into decimal will verify that they represent the same quantity.

$$2121 = (1)3^0 + (2)3^1 + (1)3^2 + (2)3^3 = 70$$

$$+0--+ = (+)3^0 + (-)3^1 + (-)3^2 + (0)3^3 + (+)3^4 = 70$$

The mathematics discussed in detail for the 0, 1, 2 symbols will apply to the 0, +, - symbols as well. The conversion from other number systems to ternary will have to be done in terms of the numeric symbols and then converted into the 0, +, - symbols which correspond to the voltage levels in the computer. In the next chapter a number of ternary computer circuits are presented which use the 0, +, - system in their operation.

V. The Trinary in Ternary Computing Systems

Any digital computer contains the following basic components; 1) counters, 2) adders, 3) coincidence circuits, 4) mixer circuits, 5) inverters, and 6) storage elements. There are many variations in the detailed circuitry from one computer to another although the logic is basically the same.

A ternary computer requires that the circuits be responsive to three voltage levels rather than the two required in a binary computer. Binary circuits in general cannot be used directly in a ternary system although the principles of operation can be very usefully employed. This is apparent when the AND circuit is considered. The logic of an AND circuit is simply that there will be an output only when all the inputs are present. The binary circuit which performs this function is shown in Figure 6. The output voltage follows the lowest input voltage. With only two voltage levels to consider, the output will not go positive (no output) unless all of the inputs are positive. Considering ternary inputs to this same circuit presents a much more complex logic function. Each of the in-

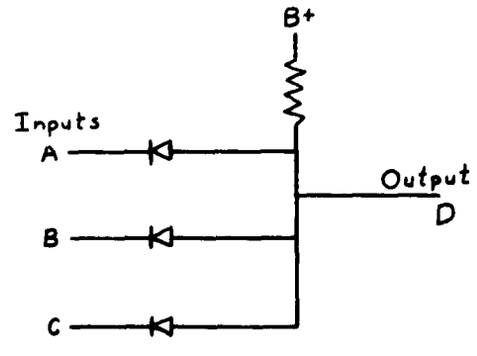


Figure 6

Binary AND Circuit

put lines have a positive (+), zero (0), or negative (-) voltage. The truth table for this ternary circuit is:

Inputs			Output	Inputs			Output
A	B	C	D	A	B	C	D
-	-	-	-	0	0	-	-
-	-	0	-	+	+	+	+
-	-	+	-	+	+	0	0
0	0	0	0	+	+	-	-
0	0	+	0	+	-	0	-

It is evident from this truth table that coincidence of the same signal on all of the input lines will give the proper output signal. However, when the inputs are not identical the output will follow the lowest input signal which may be - or 0. The simplest way to insure that the output will be zero (no information) except when there is coincidence at the inputs is to limit the excursion of the output voltage. By adding a diode to ground at the output the excursion will be restricted to 0 or +. Although extravagant, it is possible to obtain negative coincidence by using the same circuit with an inverter placed on each of the input lines and on the output. To complete the coincidence circuit, the outputs of these two circuits are combined in a resistance bridge which feeds an amplifier. When both inputs to the resistors are zero, a zero signal is applied to the amplifier. When positive coincidence occurs, the voltage applied to the amplifier

is positive and half the input amplitude. When negative coincidence occurs, the voltage applied to the amplifier is negative and half the input amplitude. The complete ternary coincidence circuit is shown in Figure 7.

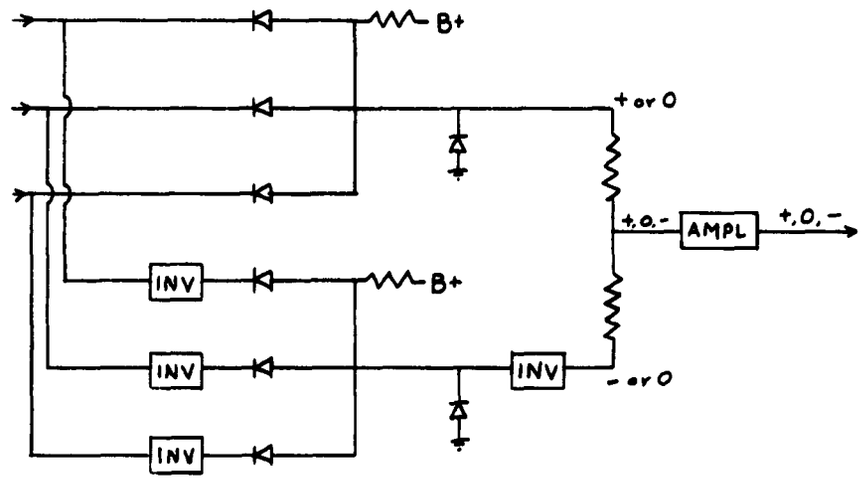


Figure 7

Ternary Coincidence Circuit

The OR circuit used in binary computers may be used in a ternary computer system if the only requirement of the circuit is that the output follow the highest input signal. A variation of the OR logic permits the use of the circuit shown in Figure 8, which shall be called a Ternary OR. The one restriction placed on this circuit is that only one input line may have a signal during a particular time interval. The output of this circuit will be the same as the non-zero input.

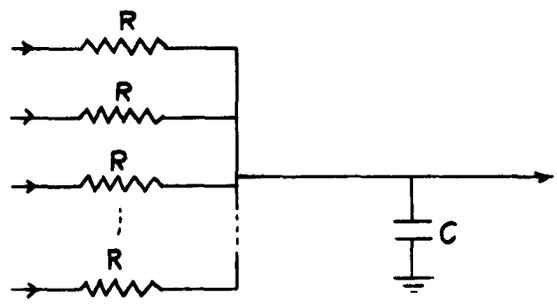


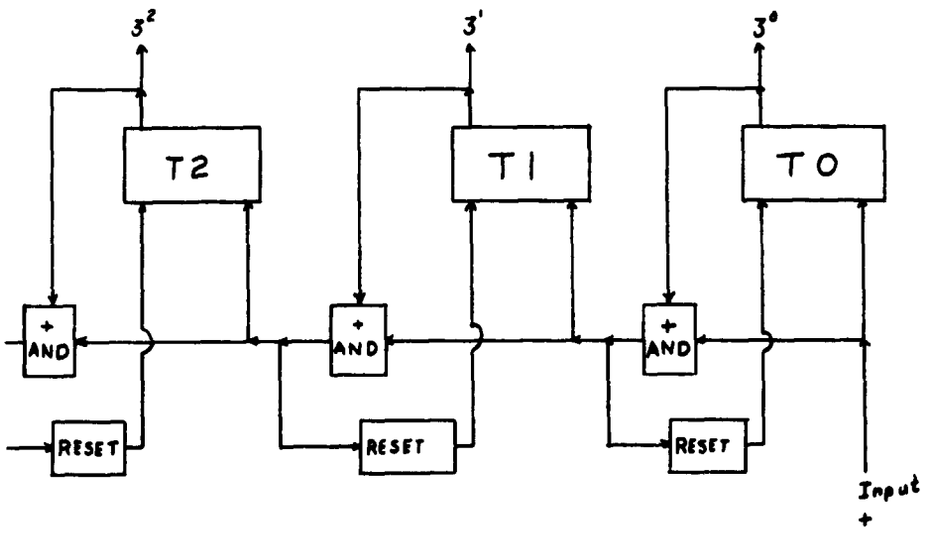
Figure 8

Ternary OR Circuit

The inverter mentioned earlier is basically an amplifier which is responsive to positive and negative voltage excursions. In those instances where signal amplification is not required, the inversion may be accomplished by any device which will transform a positive signal to a negative signal of the same magnitude and vice versa.

A counter circuit which may be used in a ternary computer is shown in Figure 9. The circuit utilizes the TRINARY as the storage element. The reset circuit consists of an amplifier which produces a negative output signal for a positive signal input. The output must be of sufficient magnitude and duration to drive the TRINARY from the + state to the - state. Before each counting operation all of the TRINARY elements are reset to the 0 state. The carry function is performed in the following manner. When a TRINARY has been advanced to the + state, its output energizes the + AND (positive coincidence) circuit associated with it. The next input

pulse (+) has no effect on the TRINARY but is passed through the + AND to the next higher order TRINARY which is advanced by one unit. The output of the + AND also activates the reset circuit which applies a double negative signal to the TRINARY thus reseting it to the - state. The counting sequence for a train of input pulses is shown in Figure 9.



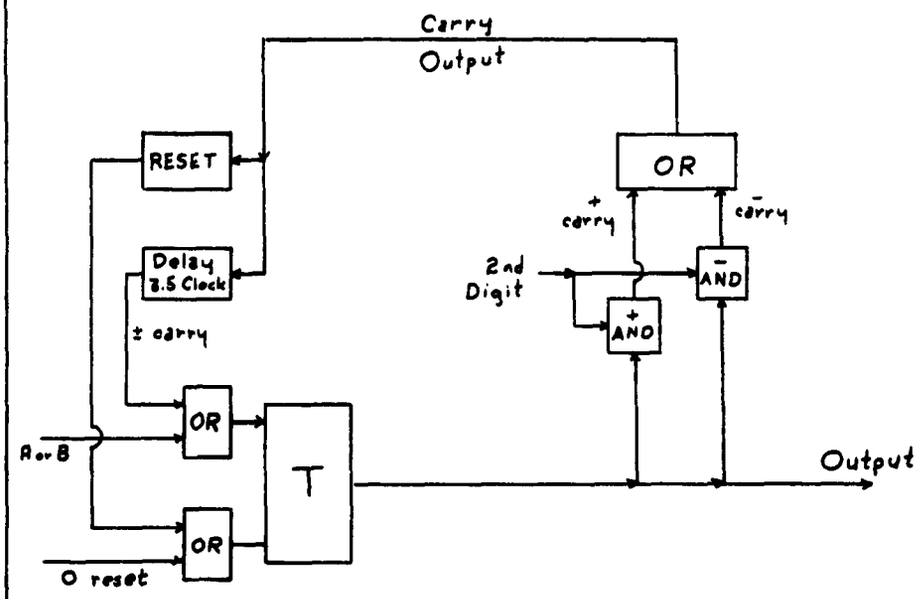
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
T0	+	-	0	+	-	0	+	-	0	+	-	0	+	-
T1	0	+	+	+	-	-	-	0	0	0	+	+	+	-
T2	0	0	0	0	+	+	+	+	+	+	+	+	+	-

Figure 9

Ternary Counter Circuit

The next circuit to be considered is the ternary adder shown in Figure 10. This is a serial feed adder which performs the addition of two numbers utilizing a TRINARY. The operating sequence is shown in the figure. The TRINARY is in the 0 state at the beginning of each addition. The first digit of word A sets the TRINARY to correspond with it. The TRINARY output is fed to a coincidence circuit to permit a carry. The first digit of word B is then applied to the adder. This bit will change the state of the TRINARY if it can. If not, it will activate a + or - carry signal from the coincidence circuit. Following this, the output of the TRINARY is sensed and the voltage level transferred out. The TRINARY is reset to 0 and is ready to add the next set of digits. Before the second digit of word A is added, the carry signal, if any, is added to the TRINARY. An example of the addition of two ternary words is shown by steps in Appendix A.

The circuits described above have been designed for use with the TRINARY. Actual values and characteristics of the individual circuit elements will have to be determined for the particular TRINARY used. There have been ternary circuits designed which utilize presently available equipment. The most recent article published is the one by Hallworth and Heath (Ref 2:219-225). Their circuits utilize transistors, diodes, and resistors. Thru the use of the techniques of Molecular Electronics, the circuits they propose could be built today with a significant increase in data capacity per



Sequence of Operation

Clock Time	Operation
1	Add A, initiate carry, carry reset
2	Add B, initiate carry, carry reset
3	Read out A+B+carry from previous digits
4	Reset T to 0
4.5	Add carry from 1
5.5	Add carry from 2
1	Add next digit of A

Figure 10

Ternary Serial Feed Adder

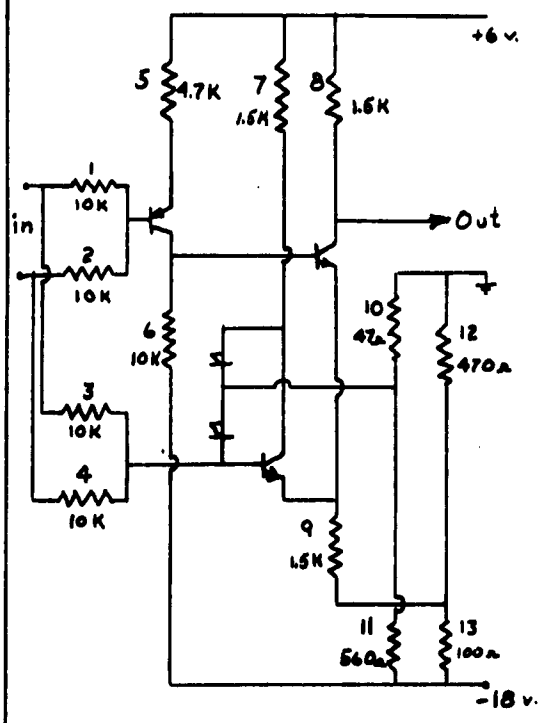
equipment volume. Two circuits which illustrate their design technique are shown in Figure 11. The convention that is used in their circuits is that the ternary symbols 0, 1, 2 are represented as +2, 0, and -2 volts respectively. Ternary addition is performed in the circuit shown in Figure 11a. R1 and R2 have an output of half the analog sum of the two inputs. T1 and T2 are a complementary-pair amplifier with the output in phase with the input and twice as large. Thus, with T3 and its circuit, the ternary sums with no carry are:

$$0 + 0 = 0$$
$$0 + 1 = 1 + 0 = 1$$
$$0 + 2 = 2 + 0 = 2$$
$$1 + 1 = 2$$

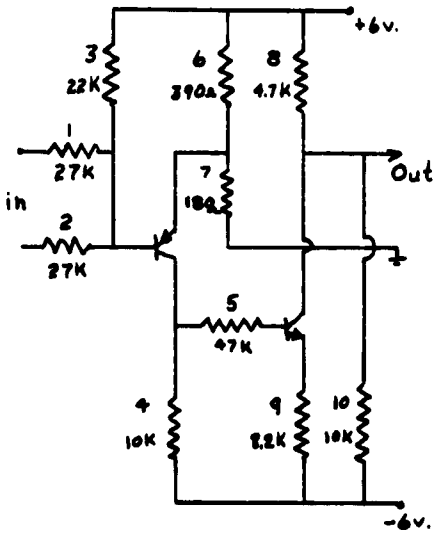
If the inputs are such that a carry is required, T3 is biased so that the signal thru R3 and R4 switches the current thru R11 from D1 to R8, and increases the output current of T2 by 3 units. This effect from T3 provides the three other sums:

$$1 + 2 = 2 + 1 = 0 \quad \text{(3 - 3 in analog)}$$
$$2 + 2 = 1 \quad \text{(4 - 3 in analog)}$$

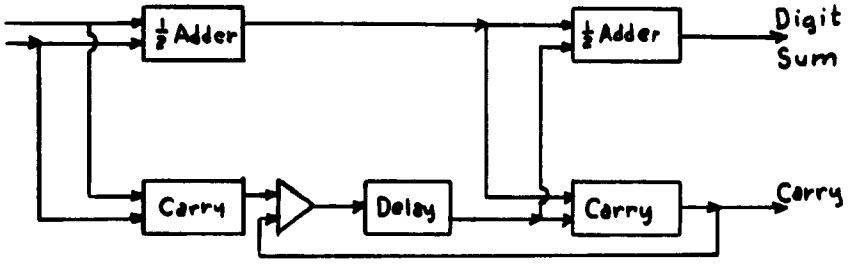
The carry circuit, Figure 11b, is essentially a resistance analog adder with an inverter. The adder is designed so that T1 is switched on when the sum of the input voltages is greater than '2' (voltage at base of T1 less than 2 volts)



a. modulo 3 half-sum circuit



b. carry circuit



c. ternary addition circuit

Figure 11

Ternary Circuits

(From Ref 2:222)

and T2 is switched on. A voltage divider chain provides the output, and T2 shunts R8 thus changing the output from 0 to 1. This carry circuit was designed on the assumption that the ternary addition would be performed with the circuit shown in Figure 11c.

A ternary adder circuit proposed by the Staff of Engineering Research Associates, Inc. using vacuum tubes is shown in Figure 12 (Ref 1:288).

MacKay and MacIntyre, as stated earlier, used a modified Flip-Flop Multivibrator to build a ternary counter. The tristable circuit, its characteristic curve, and the output waveform are shown in Figure 13. The three stable states are identified as follows:

0 state: V_B cutoff, V_A on and drawing grid current
1 state: V_A and V_B on and drawing grid current
2 state: V_A cutoff, V_B on and drawing grid current

The 0 and 2 states are similar to the two stable states of the binary type of circuit.

The storage of information in the ternary computer may be acheived thru the use of magnetic devices such as cores, tapes, or drums. The basic philosophy is to use two magnetic elements to represent one ternary digit. The three stable states corresponding to -, 0, + respectively would be: both elements negative; one negative and one positive thus cancelling each other; and both positive. The preferred approach would be to have a tristable magnetic element.

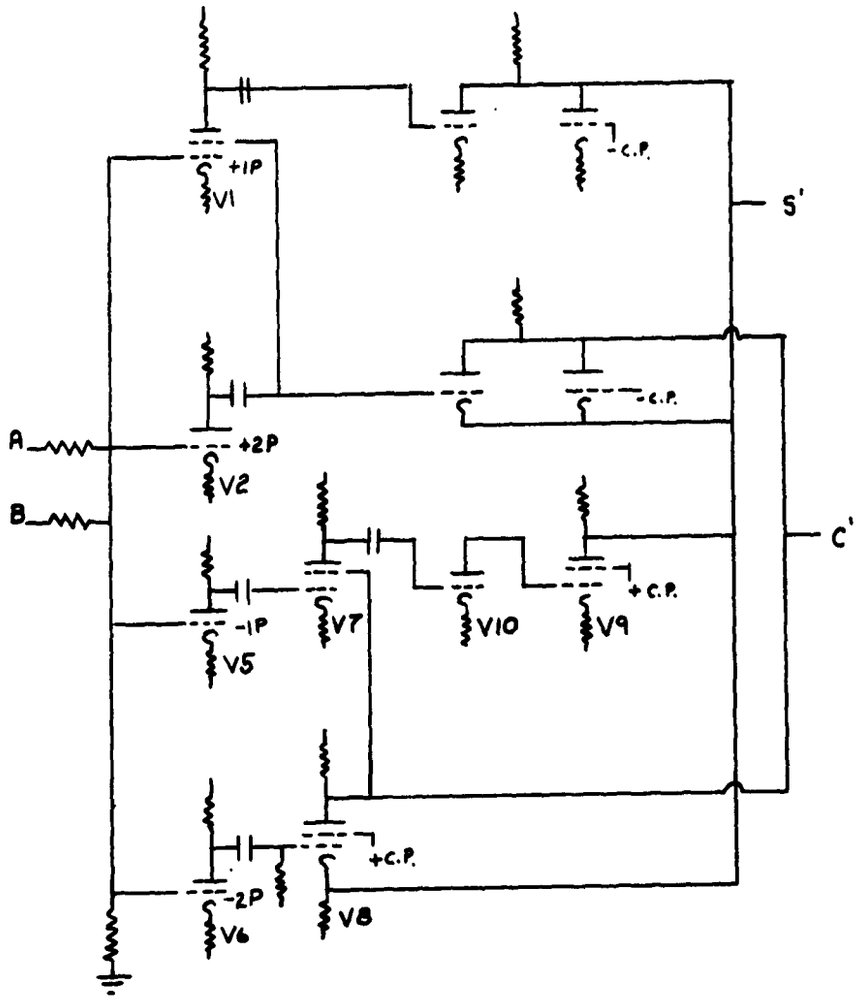
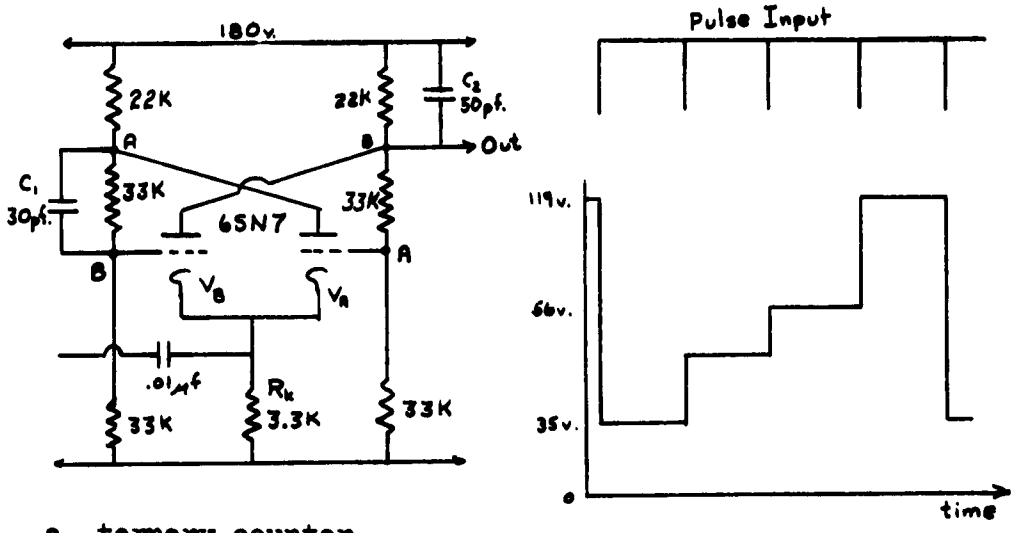


Figure 12

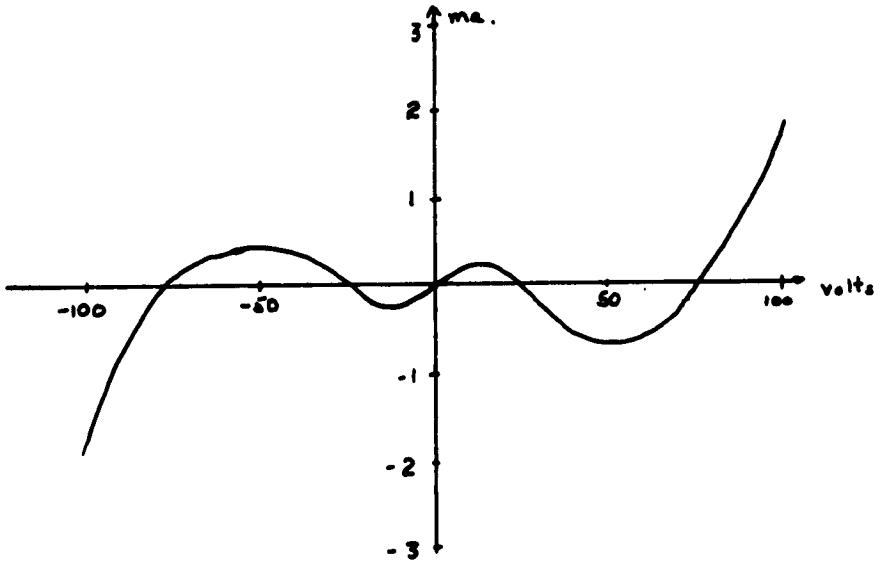
Ternary Amplitude Half Adder

(From Ref 1:288)



a. ternary counter circuit

b. plate A waveform



c. double negative resistance characteristic

Figure 13

Tristable Multivibrator

(From Ref 6:145)

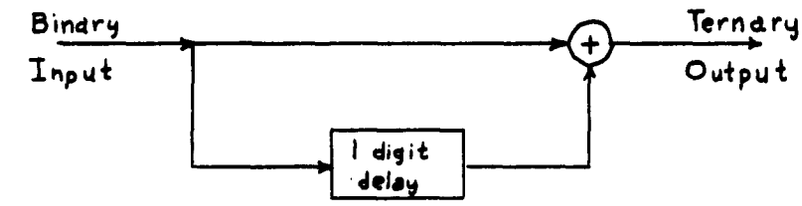
VI. The Trinary in Current Systems

The most likely area in which the TRINARY may be used is in servo-motor control systems. The -, 0, + output of the ternary device is of the form which is required to adjust the position of the control element. The amount of adjustment or angular rotation of a motor can be determined by the duration of the output of the TRINARY.

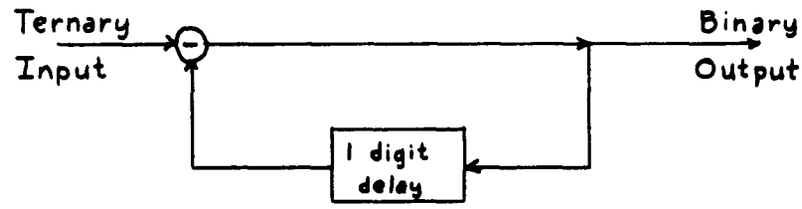
Another aspect of the relation between the ternary and binary number systems is the increased data handling capability of the ternary system. Through the use of a binary-ternary converter it would be possible to process the data with available binary equipment, convert the data into a ternary code, and transmit the data by radio or other means in the ternary number system. This will permit the transmission of 50% more information per unit time than is possible in the binary system. With the same conversion between number systems it would be possible to store data in the ternary system, again at a savings of 50% in the amount of storage space required for the same amount of information. A binary to ternary converter has been developed by Wolf and Richard (Ref 12). A block diagram of their circuit is shown in Figure 14.

A review of the current electronic computing and data processing equipment did not uncover any circuits in which the TRINARY could be readily incorporated. This was expected since it is felt that the most valuable use that can be made

of the TRINARY is in systems that use ternary logic in their entirety.



a. binary to ternary



b. ternary to binary

Figure 14

Binary-Ternary Converter

(From Ref 12)

VII. Summary and Conclusions

The need for increasing the amount of data that can be processed by an electronic computer has prompted studies in many diverse areas. This work has been concerned with one feasible solution to the problem through the use of a ternary, radix 3, system. The one factor which makes this system more attractive today than it has been in the past is the realizability of a monolithic semiconductor device which has three stable states. Although this device, which is referred to in this work as a TRINARY, has not been produced in quantity there are reasons to believe that our present technology is capable of doing so. Demand, the driving force of all manufacturing, has yet to be fully realized. In an effort to stimulate this demand, a study has been made of the advantages of the ternary system over the currently popular binary system. Two of the major advantages are the savings in the number of parts required, and the ability to process three bits of data in the same time interval that is required to process two bits of data in the binary system.

The ternary number system has been discussed in terms of two sets of symbols; the mathematical system symbols 0, 1, 2, and the computer system symbols -, 0, +. The conversion from one system of numbers to another was shown to be a division process wherein the number to be converted is divided by the radix number, expressed in the system to be converted, of the

new system. The remainder after each division corresponds to the coefficient of the powers of the new radix in ascending order. In the conversion process the Arabic numerals 0, 1, 2 are used to represent the ternary system. The arithmetic operations have been identified for both the 0, 1, 2 symbols and the -, 0, + symbols. An interesting and very useful feature of the -, 0, + system is that both positive and negative numbers can be formed without recourse to a seperate sign bit. The negative number is the inverse of the positive number of the same magnitude.

An equation has been presented which will approximate the characteristic curve of the TRINARY. Unfortunately, a physical device is not available with which to compare the theory to an actual characteristic curve. The approaches to three-stable state devices that have been propounded in the literature are not suitable for comparison with the hypothesised TRINARY characteristic curve. When an actual device is made available, the method of curve fitting discussed in this work will provide the basis for a more accurate characteristic equation.

A ternary computer incorporates networks which will perform functions similar to the basic circuits of binary computers. It has been shown that the binary AND circuit with minor modification can be used as a ternary coincidence circuit. A serial feed adder circuit has been proposed which will add two ternary numbers at the rate of 5 clock pulses

per digit. In addition, a counter, an inverter, two types of OR circuits, and a magnetic storage element have been discussed.

The use of a TRINARY in present systems has been briefly discussed. Aside from its use in control and servo systems, the TRINARY is not likely to be used extensively as a substitute for binary circuits. The most beneficial use that can be made of the TRINARY in conjunction with current systems is the transmission of data. Since a ternary digit contains 50% more information than a binary digit, it is possible to transmit a block of data faster with ternary than is possible with binary. A device is mentioned which has been developed to transform binary information into a ternary code and back.

There is much that will have to be accomplished before the full capability of the ternary system can be exploited. A few of the tasks that need to be undertaken are:

1. Determination of the characteristic equations which accurately describe actual tristable devices that become available.

2. Development of other ternary circuits to be used with those presented. Some circuits that should be considered are; shift registers, comparators, memory, and the associated input-output equipment.

3. Physical construction of the ternary circuits to determine component values and evaluate the optimum operating conditions.

4. Improvement of these circuits, particularly the adder, to obtain faster operating times.

5. Investigation of the use of the ternary system in data processing equipment to facilitate the use of EDPM in conjunction with ternary computers. In this connection, the development of a card or tape punch system using ternary coding would be very desirable.

Bibliography

Primary

1. ERA Staff. High Speed Computing Devices. New York: McGraw-Hill Book Co., Inc., 1950.

2. Hallworth, R. P., and F. G. Heath. "Semiconductor Circuits for Ternary Logic." Proceedings of the Institution of Electrical Engineers, 109C:219-225 (March 1962).

3. Hartree, D. R. Calculating Instruments and Machines. Urbana, Illinois: University of Illinois Press, 1949.

4. Kosonocky, W. F. Three State Circuit. U. S. Patent 3,027,464 issued March 27, 1962.

5. Kumagai, S., and S. Kawamoto. "Multistable Circuits Using Nonlinear Reactances." Transactions of the Institute of Radio Engineers, CT-7:432-440 (December 1960).

6. MacKay, R. S., and R. MacIntyre. "Ternary Counters." Transactions of the Institute of Radio Engineers, EC-4:144-149 (December 1955).

7. Pearson, G. L. Semiconductor Device. U. S. Patent 2,983,854 issued May 9, 1961.

8. Rabinovici, B., and J. Klapper. "Designing Tunnel-Diode Circuits Using Composite Characteristics." Electronics, 35:46-48 (February 16, 1962).

9. Staff of Computation Laboratory. "Synthesis of Electronic Computing and Control Circuits." Annals of the Harvard Computation Laboratory, 27:145 (1951).

10. Vacca, R. A 3-Valued System of Logic and its Application to Base 3 Digital Circuits. UNESCO/NS/ICIP/G. 2.14. New York: United Nations, n.d.

11. Ware, W. H., et al. "Soviet Computer Technology-1959." Transactions of the Institute of Radio Engineers, EC-9:72-120 (March 1960).

12. Wolf, J. K. , and W. R. Richard. Binary to Ternary Conversion by Linear Filtering. RADC-TDR-62-230. Rome, New York: U. S. A. F., May 1962.

13. Wylie, C. R. Jr. Advanced Engineering Mathematics. (Second Edition). New York: McGraw-Hill Book Co., Inc., 1960.

Secondary

14. Culbertson, J. T. Mathematics and Logic for Digital Devices. New York: D. Van Nostrand Co., Inc., 1958.

15. Kious, G. A. "Digital Communications System Design." Electronic Industries, 81:108-113 (March 1962).

16. Morris, D. J., and W. Alexander. "An Introduction to the Ternary Code Number System." Electronic Engineering, 32:554-557 (September 1960).

17. Phister, J. K. Logical Design of Digital Computers. New York: John Wiley and Sons, Inc., 1958.

18. Richards, R. K. Digital Computer Components and Circuits. New York: D. Van Nostrand Co., Inc., 1957.

Tertiary

19. Alford, C. H. "Analysis and Design of the Twin-Tunnel-Diode Logic Circuit." WESCON Convention Record, Part 2:94-101 (1960).

20. Auger, E. P. "A Practical Tunnel Diode NOR Circuit." Electronic Design, 10:72-77 (March 15, 1962).

21. Brody, T. P., and R. H. Boyer. "The Evaluation of 'ESAKI INTEGRALS' and an Approximate Expression for the Tunnel-Diode Characteristics." Solid State Electronics, 2:209-215 (May 1961).

22. Bunch, V. L. "Volt-Ampere Characteristics of a Tunnel Diode." Radio Engineering and Electronic Physics, 6:1828-1841 (December 1961).

23. Cheney, P. W. "Analog-to-Digital Conversion with Threshold Detectors." Transactions of the Institute of Radio Engineers, EC-10:100 (March 1961).

24. Chow, W. F. "Tunnel Diode Digital Circuitry." Transactions of the Institute of Radio Engineers, EC-9:295-301 (September 1960).

25. Esaki, L. "New Phenomenon in Narrow Germanium p-n Junctions." Physical Review, 109:603 (1958).

26. Hall, R. N. "Tunnel Diodes." Transactions of the Institute of Radio Engineers, ED-7:1-9 (January 1960).

27. Hamann, D. T. "A Matched Amplifier Using 2 Cascaded Esaki Diodes." Proceedings of the Institute of Radio Engineers, 49:904-906 (May 1961).

28. Kaenel, R. A. "High Speed Analog-to-Digital Converters Utilizing Tunnel Diodes." Transactions of the Institute of Radio Engineers, EC-10:273-284 (June 1961).

29. Mitchell, F. H. Jr. "Deriving the Tunnel Diode Curve." Electronic Industries, 20:96-97 (October 1961).

30. Przybylski, J., and G. N. Roberts. "The Design and Construction of Tunnel Diodes." Journal of the British Institution of Radio Engineers, 22:497-505 (December 1961).

31. Rowley, G. C. "Transistor Circuits for a Digital Differential Analyser." Proceedings of the Institution of Electrical Engineers, 106B-16:685-687,698-701 (1959).

32. Tarnay, K. "Approximation of Tunnel Diode Characteristics." Proceedings of the Institute of Radio Engineers, 50:202-203 (February 1962).

33. Winterbottom, N., and J. S. B. Walters. "A High-Speed Analog to Digital Converter." Electronic Engineering, 33:144-149 (March 1961).

Appendix A

Addition in the Ternary Adder

The operation of the ternary adder follows the sequence given in Figure 10. Before the addition begins the TRINARY is in the 0 state. For the purpose of illustration, each addition cycle is identified by a Roman numeral. The two words to be added are:

A = 102201 = 0++0-0+

B = 210120 = +-++--0

Cycle	Clock Time	Operation	TRINARY Output	Carry Output
I	1	Add A_1 = +	+	0
	2	Add B_1 = 0	+	0
	3	Read out	+	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	0	0
	5.5	Add carry from 2	0	0
II	1	Add A_2 = 0	0	0
	2	Add B_2 = -	-	0
	3	Read out	-	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	0	0
	5.5	Add carry from 2	0	0

Cycle	Clock Time	Operation	TRINARY Output	Carry Output
III	1	Add A_3 = -	-	0
	2	Add B_3 = -	-	-
	2+	Carry reset	+	0
	3	Read out	+	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	0	0
	5.5	Add carry from 2	-	0
IV	1	Add A_4 = 0	-	0
	2	Add B_4 = +	0	0
	3	Read out	0	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	0	0
	5.5	Add carry from 2	0	0
V	1	Add A_5 = +	+	0
	2	Add B_5 = +	+	+
	2+	Carry reset	-	0
	3	Read out	-	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	0	0
	5.5	Add carry from 2	+	0

Cycle	Clock Time	Operation	TRINARY Output	Carry Output
VI	1	Add A_6 = +	+	+
	1+	Carry reset	-	0
	2	Add B_6 = -	-	-
	2+	Carry reset	+	0
	3	Read out	+	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	+	0
	5.5	Add carry from 2	0	0
VII	1	Add A_7 = 0	0	0
	2	Add B_7 = +	+	0
	3	Read out	+	0
	4	Reset to 0	0	0
	4.5	Add carry from 1	0	0
	5.5	Add carry from 2	0	0

The output is A + B = ++-0+-+. This is verified by adding the inputs:

$$A = 0 + + 0 - 0 +$$
$$\underline{B} = \underline{+ - + + - - 0}$$
$$A + B = + + - 0 + - +$$

Appendix B

Tabulated Data for Curve of Figure 5

$\frac{V}{V_p}$	i	$\frac{i}{I_p}$
0.00	$0.92542\ I_0 + 0.02796\ I_p$	0.49067
0.25	$0.69873\ I_0 + 0.57242\ I_p$	0.92178
0.50	$0.53420\ I_0 + 0.85008\ I_p$	1.11718
0.75	$0.42232\ I_0 + 0.93193\ I_p$	1.14309
1.00	$0.35426\ I_0 + 0.87876\ I_p$	1.05589
1.25	$0.32180\ I_0 + 0.74113\ I_p$	0.90203
1.50	$0.31741\ I_0 + 0.55915\ I_p$	0.71785
1.75	$0.33420\ I_0 + 0.36780\ I_p$	0.55490
2.00	$0.36593\ I_0 + 0.18645\ I_p$	0.36942
2.25	$0.40705\ I_0 - 0.00167\ I_p$	0.20185
2.50	$0.45261\ I_0 - 0.06938\ I_p$	0.15692
2.75	$0.49839\ I_0 - 0.12878\ I_p$	0.12041
3.00	$0.51073\ I_0 - 0.13987\ I_p$	0.11549
3.25	$0.57640\ I_0 - 0.10664\ I_p$	0.18156
3.50	$0.60556\ I_0 - 0.03387\ I_p$	0.26891
3.75	$0.62108\ I_0 + 0.06232\ I_p$	0.37286
4.00	$0.62684\ I_0 + 0.18645\ I_p$	0.49987
4.25	$0.62053\ I_0 + 0.31141\ I_p$	0.62167
4.50	$0.60381\ I_0 + 0.42967\ I_p$	0.73157
4.75	$0.56086\ I_0 + 0.52918\ I_p$	0.80961
5.00	$0.54024\ I_0 + 0.59905\ I_p$	0.86917

$\frac{V}{V_p}$	i	$\frac{i}{I_p}$
5.25	$0.49767\ I_0 + 0.63032\ I_p$	0.87915
5.50	$0.45172\ I_0 + 0.61669\ I_p$	0.84255
5.75	$0.40597\ I_0 + 0.55532\ I_p$	0.75830
6.00	$0.36463\ I_0 + 0.44751\ I_p$	0.63012
6.25	$0.33265\ I_0 + 0.29955\ I_p$	0.46587
6.50	$0.31558\ I_0 + 0.12334\ I_p$	0.28113
6.75	$0.31964\ I_0 - 0.06275\ I_p$	0.09707
7.00	$0.35179\ I_0 - 0.23317\ I_p$	-0.05728
7.25	$0.41947\ I_0 - 0.35443\ I_p$	-0.14470
7.50	$0.53093\ I_0 - 0.38435\ I_p$	-0.11889
7.75	$0.69597\ I_0 - 0.27133\ I_p$	0.07665
8.00	$0.95175\ I_0 + 0.04644\ I_p$	0.52231
8.25	$1.21959\ I_0 + 0.64169\ I_p$	1.25148

Vita

Joseph Alexander Krupinski was born on 25 February 1933 in Dickson City, Pennsylvania, the son of Alexander John Krupinski and Helen Sosnowski Krupinski. He moved with his family to Newark, New Jersey in 1942. He was graduated from East Side High School, Newark, New Jersey in 1950 and enrolled in Newark College of Engineering that same year. In June 1954 he was graduated with the degree of Bachelor of Science in Electrical Engineering and received his commission as a Second Lieutenant in the USAF Reserve. Upon graduation he entered the employ of the International Business Machines Corporation at Poughkeepsie and Kingston, New York. He entered the Air Force on active duty in August 1955. His military assignments prior to his coming to the Air Force Institute of Technology were in the Air Material Command, now the Air Force Logistics Command, as a Ground Electronics Officer. His most recent assignment was with the Ground Electronics Engineering Installation Agency Headquarters at Griffiss Air Force Base, New York.

Permanent address: 110 Woodside Road
Maplewood, New Jersey

This thesis was typed by Mrs. Rose McHenry.