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REVIEW ARTICLE OPEN

Building logical qubits in a superconducting quantum computing system

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The technological world is in the midst of a quantum computing and quantum information revolution. Since Richard Feynman's famous 'plenty of room at the bottom' lecture (Feynman, *Engineering and Science* **23**, 22 (1960)), hinting at the notion of novel devices employing quantum mechanics, the quantum information community has taken gigantic strides in understanding the potential applications of a quantum computer and laid the foundational requirements for building one. We believe that the next significant step will be to demonstrate a quantum memory, in which a system of interacting qubits stores an encoded logical qubit state longer than the incorporated parts. Here, we describe the important route towards a logical memory with superconducting qubits, employing a rotated version of the surface code. The current status of technology with regards to interconnected superconducting-qubit networks will be described and near-term areas of focus to improve devices will be identified. Overall, the progress in this exciting field has been astounding, but we are at an important turning point, where it will be critical to incorporate engineering solutions with quantum architectural considerations, laying the foundation towards scalable fault-tolerant quantum computers in the near future.

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INTRODUCTION

Quantum computing holds the promise of solving some computation problems, that are untenable on conventional computers.[1–3] Loosely speaking, quantum computing targets problems that can exploit entanglement to explore correlations in computations, then selects the correct answer through constructive interference. For example, Shor's algorithm addresses the computational challenge of factoring by exploiting quantum interference to measure the periodicity of arithmetic objects.[1]

However, there is a pernicious flaw to this increase in computational power. In a quantum computer, the information is encoded in quantum bits, or qubits, which need to interact strongly with one another, external inputs for control, and outputs for detection, but nothing else. This leads to the quantum conflict: balancing just enough control and coupling, while preserving quantum coherence. This conflict represents a fundamental impediment to reducing the physical qubit error rate low enough to perform long/difficult/large-scale/practical quantum computations with them directly.

Fortunately, it has been shown that with quantum error correction (QEC) it is possible to perform fault-tolerant quantum computing.[4,5] The essential idea in QEC is to encode information in subsystems of a larger physical space that are immune to noise. QEC can be used to define fault-tolerant logical qubits, through employing a subtle redundancy in superpositions of entangled states and non-local measurements to extract entropy from the system without learning the state of the individual physical qubits. The particular architecture for implementing a fault-tolerant operating scheme has bearing on the requirements necessary for the underlying physical qubits.

While there are many approaches to achieving quantum fault-tolerance, one of the most promising is the two-dimensional (2D) surface code.[6–9] This code has a high tolerance to errors, or threshold (approximately 6.7×10^{-3}), requires only nearest-neighbor qubit interactions, has simple error syndrome extraction circuits,[10] and a suite of fault-tolerant logic based on transversal gates,[7] code deformation,[8,11] or lattice surgery.[12]

All together, this suggests that to build a quantum computer we require:

- a physical qubit that is well isolated from the environment and is capable of being addressed and coupled to more than one extra qubit in a controllable manner,
- a fault-tolerant architecture supporting reliable logical qubits, and
- universal gates, initialization, and measurement of logical qubits

A physical quantum computer satisfying all three of these requirements is still an outstanding challenge. However, in recent work, physical qubits in trapped-ion and superconducting systems have reached the point where errors are at or below the threshold,[13–16] and networks of 4–9 superconducting qubits with individual control and readout have been used to show concepts of error correction.[17–19] Over the next few years, the field will be in a stage of building interesting quantum devices with a complexity that could never be emulated in full generality on a classical computer (~50 or more qubits). These devices will allow us to understand nature in a regime that has never been explored before, offering new insight into analog simulations of quantum systems. Nonetheless, near-term progress towards the monumental task of fully fault-tolerant universal quantum computing will hinge upon using QEC for demonstrating a quantum memory:

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a logical qubit that is sufficiently stable against local errors and ultimately allows essentially error-free storage.

In this review, we present a view of what a medium-sized quantum computing system will comprise, as well as a discussion on the current state of coheren control and readout of superconducting qubits. We also detail some of the main challenges that the community will face in building a device of O(100) qubits so as to further the state-of-the-art of QEC and approach a useful fault-tolerant quantum memory.

THE QUANTUM COMPUTING SYSTEM AND FAULT-TOLERANT ARCHITECTURE

A full fault-tolerant quantum computing system can be envisioned within a layered structure as shown in Fig. 1. The system is comprised of two primary layers, a physical qubit layer and a logical qubit layer. The lower physical layer contains physical qubits controlled via a QEC processor, which is in essence a classical processor that uses measurement outcomes of the physical qubits to realize a QEC code. This classical processor keeps track of the physical errors that arise, and implements the appropriate feedback on the controls of the physical qubits. The upper layer of Fig. 1 is called a logical layer and functions through control of the physical layer. Here, logical qubits are encoded within the fully error-corrected system of physical qubits, and logical controls and readouts are governed through a processor that determines how to implement difficult quantum algorithms, e.g. Shor's, Grover's, and quantum simulation.[1–3]

Residing at the very bottom of the physical qubit layer are imperfect physical qubits, which have been explored in a variety of different experimental systems: superconducting qubits,[17–20] trapped-ion,[15,16,21] solid-state spin,[22,23] nuclear spin,[24,25] non-linear photonic,[26] and neutral atom[27] qubits, which are just a few examples of more mature qubit systems demonstrating multi-qubit operations. Coherence times in these systems are relatively varied. However, for the purposes of quantum computing, it is important to normalize coherence to the gate (control) lengths possible for the system. Especially for superconducting qubits, with coherence times in the ~100 µs range and gate lengths ~10–100 ns, the number of operations per coherence time becomes a very promising number (currently approaching 10^4 operations).

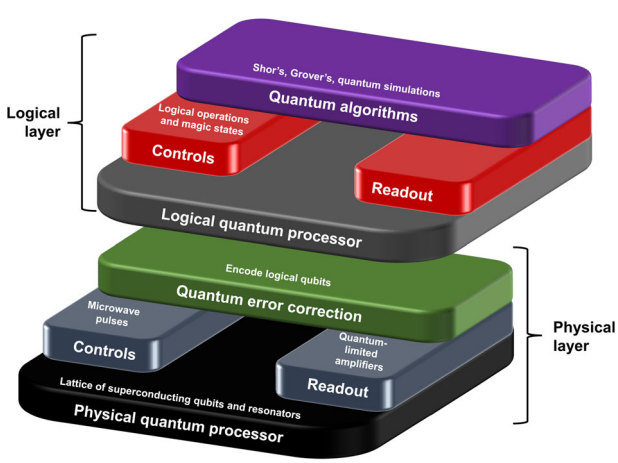

Fig. 1 A systems view of a quantum information processor. It consists of a physical and logical layer. The physical layer provides the error correction and consists of a physical quantum processor that has both input and output lines that are controlled by the QEC processor. This processor is in turn controlled by the logical layer, where the encoded qubits are defined and the logical operations are performed for the desired quantum algorithm

Inputs and outputs to the layer of physical qubits are controls and readouts, respectively. For superconducting qubits, controls can involve a full suite of microwave electronics and pulse-shaping, to realize specific qubit rotations and two-qubit controlled operations. The noise on these controls is filtered and attenuated so that the noise at the qubit is negligible. It is also important for readout of superconducting qubits to be boosted through stages of amplification, the first of which is quantum-limited.[28–30] Analog readout signals are then digitally processed either on classical computers or in customized field-programmable gate arrays (FPGAs) for fast processing.[31,32] A schematic of the physical layer for superconducting qubits is shown in Fig. 2. Although currently the quantum error correcting process sits at room temperature, it is possible in the future that some of this operation might be performed at lower temperatures stages within the dilution refrigerator.[34]

The particular arrangement of physical qubits is governed by selection of a fault-tolerant error correction architecture. With high error thresholds and simple physical lattice arrangement, the rotated surface code (RSC)[35] is one of the most promising schemes for QEC. The RSC code uses less qubits than the standard surface code, and Fig. 3a shows a conceptualized version of it consisting of d^2 data qubits (the *black dots* at the vertices of the graph) arranged in a *square lattice*, where d is the distance of the code (shown for a $d = 5$ code). These qubits are in a simultaneous eigenstate of both the (d^2–1) Z-parity (*blue faces*) and X-parity (*red faces*) stabilizers and the logical qubit is the one remaining with unconstrained degree of freedom. The $Z(X)$-parity stabilizers are the multi-qubit operators represented by the product of single qubit $Z(X)$ operator on the data qubits located at the vertices of the face. A logical $\overline{X}$ (Pauli X bit-flip logical gate) is represented by

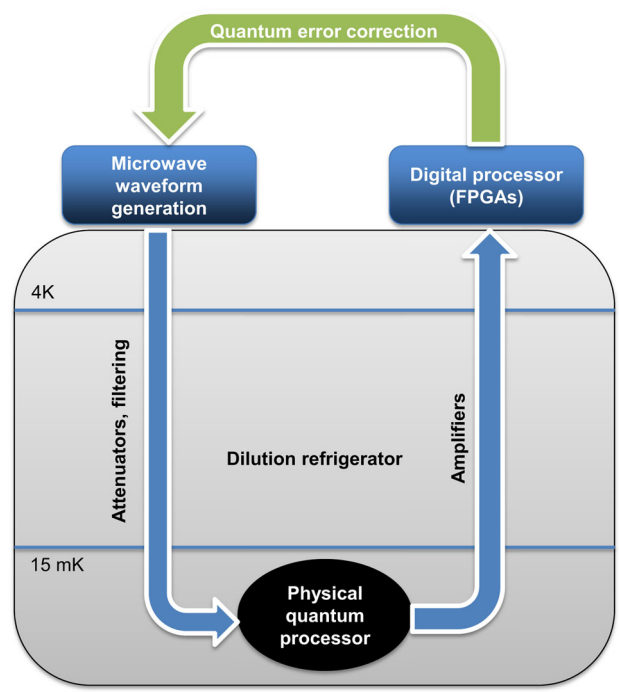

Fig. 2 The physical qubit processor is located at the bottom (15 mK) plate of a dilution refrigerator. Microwave pulses are generated at room temperature using synthesizers, arbitrary waveform generators, and mixers. These pulses are filtered and attenuated to assure negligible noise at the qubit. High-fidelity readout of the qubit state requires quantum-limited and other cryogenic amplification to overcome thermal noise for digitization and weighted homodyne measurement.[33] The QEC processor sits above and orchestrates the physical control and readout functions, to perform the error correction protocol

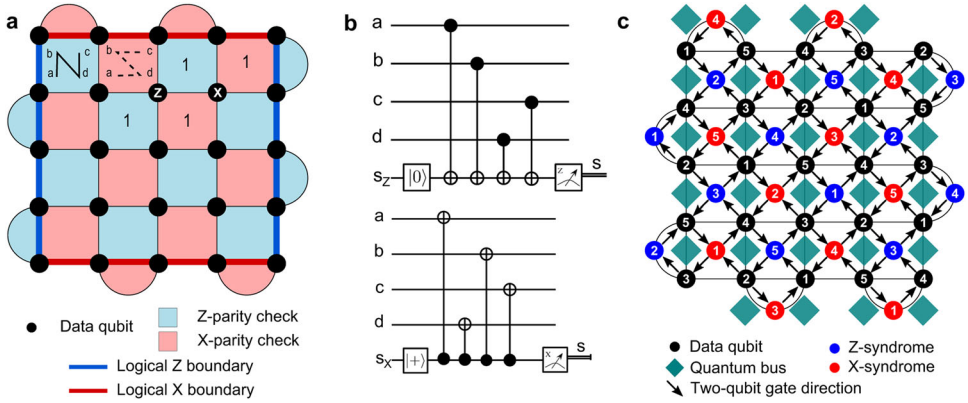

Fig. 3 **a** The RSC with d^2 data qubits (*black circles*) and the (d^2–1) *X*- (*red*) and *Z*-parity (*blue*) checks, shown for $d = 5$. Examples of errors are shown (*white* lettering inside *black* data qubit *circles*) along with the corresponding measured syndromes for surrounding parity checks. Logical operation boundaries are shown for *X* and *Z* Pauli operations as *red* and *blue lines*, respectively. **b** The quantum circuits used to perform the *Z*-parity and *X*-parity checks. The order of these checks ensures that no hook errors[10] can be incorrectly assigned as single-qubit errors. **c** A physical realization of the RSC superconducting qubits with quantum buses for mediating interactions. Here, quantum buses are used to connect data qubits to syndrome bits for *Z* and *X* parity detection. Furthermore, a proposed arrangement of five distinct qubit frequencies (numbering within the qubits) is shown to minimize crosstalk and addressability errors.[36]

a chain of *X* operations that connect the two *X*-boundaries (*red lines*) and a logical $\bar{Z}$ (Pauli *Z* phase-flip logical gate) is represented by a chain of *Z* operations that connect the two *Z*-boundaries (*blue lines*).

The QEC processor (*green* slab in Fig. 1) sits above the physical controls and readouts and functions to keep the lattice in a simultaneous eigenstate of the *Z*-parity and *X*-parity stabilizers implemented by the circuits shown in Fig. 3b. The order of the controlled-NOT (cNOT) gates is important for fault-tolerant operation to ensure that all error syndrome bits correctly identify single error faults anywhere in the extraction process. In each cycle, d^2–1 syndrome bits are extracted, and, in the absence of errors, the syndrome bit will have the same value every cycle. Each time the syndrome bit changes value, an endpoint of a chain of errors is identified. From these chains, Edmonds' minimum weight perfect matching algorithm can be used to find the set of corrective operations.[37] Corrections are applied to the classical data associated with the measurement results rather than to the actual physical qubits. This ensures that no corrective operations need to be applied to the qubits (no additional errors) and no complicated feedback is necessary.

To realize this code, we induce coupling between the data qubits and the syndromes by using a quantum bus.[38,39] The arrangement of the bus is shown in Fig. 3c as the *green squares*, where each bus couples to four data qubits and each qubit couples to two buses allowing a tiling that achieves the connectivity required for the RSC.[40] Using this tiling and provided the gate is directional (e.g. CR [41] and tunable-frequency activated gates[42]) a minimum of five frequencies are required to allow selective two-qubit gates.[36] At IBM we are using coplanar waveguide microwave resonators for the bus, and examples of connected multi-qubit experimental devices employing this sub-lattice are shown in Fig. 4.

With an error-corrected sea of physical qubits, it becomes possible to enter the logical layer of Fig. 1. In the RSC only the logical Hadamard can be implemented transversally (i.e. the logical gate is represented by the product of operations on the single qubits) up to a rotation of the code. The version of the cNOT that we find attractive because of its lower overhead is provided by lattice surgery.[12] Optimal implementations of the remaining logical gates, $S = \sqrt{Z}$, $T = \sqrt{S}$ are still open questions. It is known that RSC or any 2D stabilizer code cannot implement all universal gates transversally[43] and methods such as distillation and injection are needed.[44] The distillation process for the *T* gate is the most expensive in terms of number of physical qubits and the community is working hard to reduced this overhead.[45,46] With these logical operations all quantum gates can be implemented efficiently using the Solovay-Kitaev algorithm[47] or more recent optimizations.[48,49] At the top of this layer sits the proposed applications of quantum computing, including the possibility to perform quantum algorithms such as Shor's factoring,[1] Grover's search,[2] or digital quantum simulations of real world chemical molecules and dynamics.[3]

For the rest of this article, we focus primarily on the lower section of the diagram, giving some detail about the current state of such a quantum computing system with respect to superconducting qubit technology implementing the RSC approach for QEC. We will discuss some of the challenges that lie ahead for the superconducting qubit community in the march towards implementing a fully-error corrected surface of physical qubits.

COHERENCE OF SUPERCONDUCTING QUBITS

Josephson junction (JJ) based superconducting qubits have emerged as one of the contenders to build a practical quantum computer. Detailed descriptions of superconducting qubits have been discussed previously[20,50] and here we only provide a brief historical overview and concise description of current state-of-the-art implementations.

Superconducting qubits are constructed out of one or more inductors, capacitors and JJs. By virtue of employing superconducting materials, losses in these systems can be greatly reduced, which is a necessary requirement. The JJ consists of a superconducting electrode, a thin insulator and another superconducting electrode allowing Cooper pairs to tunnel across the insulating barrier, and behaves effectively as a non-linear inductor. This circuit element is necessary because its non-linearity leads to quantum mechanical energy levels that are not equally spaced. The deviation from a harmonic oscillator (or anharmonicity) permits the isolation of two energy levels to provide the computational basis states $|0\rangle$ and $|1\rangle$ for a qubit. Typically, the qubit transition energies (between $|0\rangle$ and $|1\rangle$ are in the microwave frequency regime, ~4–6 GHz, and the difference between this transition and one that involves going out of the qubit manifold $|0\rangle$, $|1\rangle$ is 5% for weakly anharmonic qubits like the transmon qubits.[51]

Important metrics for the qubits are the coherence times, T_1 and T_2 (energy relaxation and dephasing times, respectively). Energy

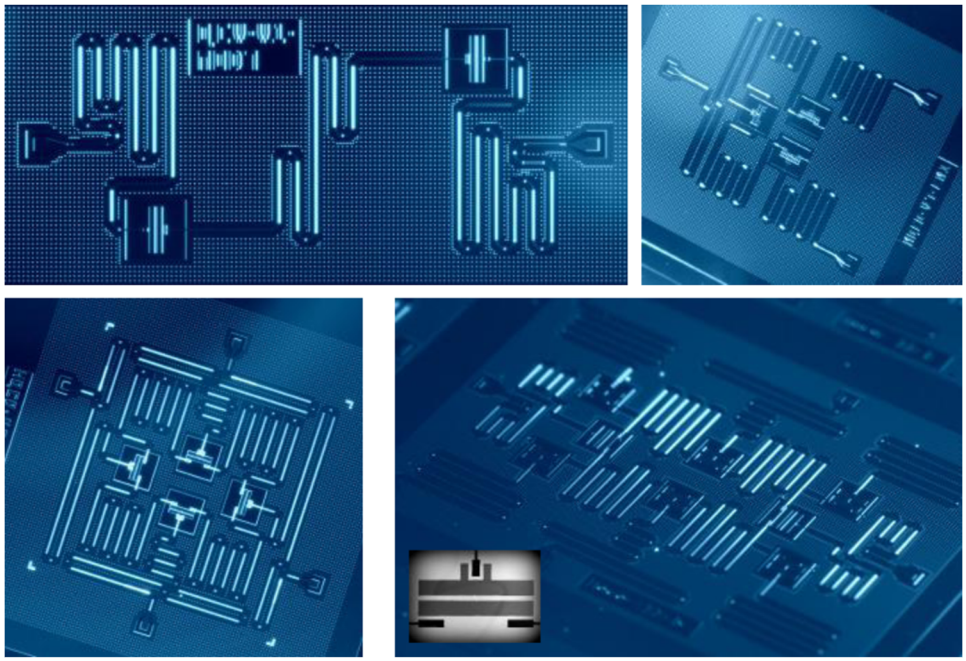

Fig. 4 Images of four recent devices fabricated at IBM. The device in the top left corner contains 2Q(qubits)/1B(us)/2R(eadout resonators) and is currently being used to study optimal two-qubit gates. The top right corner shows a device with 3Q/2B/3R which was used to demonstrate a parity measurement.[40] In the lower left corner is a device with 4Q/4B/4R for demonstrating the [[2,0,2]] code[17] and the lower right corner shows a device of 8Q/4B/8R for studying both *Z* and *X* parity checks. Inset shows an optical micrograph of an individual transmon qubit

relaxation quantifies the time it takes for a qubit to decay from its excited state $|1\rangle$ to the ground state $|0\rangle$ (a bit-flip error) while dephasing times correspond to the time it takes for a quantum superposition state $|+\rangle=(|0\rangle+|1\rangle)/\sqrt{2}$ to lose its phase relationship between $|0\rangle$ and $|1\rangle$ (i.e. a phase-flip error). Both quantities play an important role as shorter times will reduce the accuracy of quantum operations.

The first experimental demonstration of a superconducting qubit[52] is attributed to the group at NEC in 1999, albeit with T_2~1 ns. Since this seminal result, many groups around the world conceived and implemented a variety of superconducting qubits by varying with the superconducting circuits, for example, by adding loops interrupted by one or more JJs or by adding capacitors. Research involving all these variants helped the community shed light on what limits coherence times. By now, it is known that the charge noise, flux noise, the microwave environment, and materials play crucial roles.

Any electromagnetic mode with finite quality factor that couples to the qubit will impact the T_1. T_1 limitations from various external couplings can now be analytically calculated, by analyzing the real part of the admittance as seen by the qubit.[53] As such, over the years many results have shown how to reduce or eliminate residual coupling to electromagnetic modes that are present, intentional or not.[54–56] At the same time, it is also necessary to minimize stray radiation especially at high frequency which may be capable of generating quasi-particles.[57,58]

Dielectric loss plays a crucial role and appears to be limiting T_1 for many superconducting qubits. It is believed to be due to two-level systems (TLSs) at the microscopic level [59] that couple to the qubit's electric field.[60–62] This dielectric loss manifests itself in two different ways. First, bulk insulating material with a non-zero loss tangent that is involved in any of the qubit's total capacitance can limit T_1 times. A continuum of TLSs residing in this bulk material lead to the standard exponential decay. However, when there are only few TLS present, the dielectric loss manifests itself differently. Individual TLSs at some specific frequencies can couple to the qubit and give rise to avoid level crossings among other undesirable effects.[59]

For the transmon qubits that we design,[63] we typically aim for a transition frequency of 5–5.4 GHz, with an anharmonicity of ~-346 MHz so that the charge dispersion is less than 30 kHz. With numerical simulations combined with static field simulations of the qubit design, we aim to achieve a qubit capacitance of C_q~65 fF, paired with a JJ critical current of about I_0~27 nA. The junction is made quite small (100–200 × 100–200 μm), which avoids TLS defects residing in the tunnel junction. The shunting capacitor is formed by metal pads spaced apart as much as 70 μm so as to minimize dielectric loss from any of the substrate surfaces.[61,62] This style of qubit currently provides some of the highest and reliable coherence times for transmon devices, T_1,T_2~100 μs, almost 5 orders of magnitude improved over the initial demonstration of superconducting qubits and enough to demonstrate concepts of error correction.

CONTROL OF SUPERCONDUCTING QUBITS

To universally control a quantum system, it is sufficient to be able to perform arbitrary single-qubit gates and a two-qubit gate.[64] For superconducting qubits most researchers have converged on using microwave drives to perform arbitrary single-qubit rotations in the *x*–*y* plane through control of the amplitude and the phase of the drives. However, for transmon qubits, due to the weak anharmonicity, it is necessary to perform corrections due to the effects of the higher levels. The standard is to use Derivative Removal Adiabatic Gate shaping.[65] This approach has improved single-qubit gate fidelity to $5(2)\times10^{-4}$ as demonstrated by benchmarking.[66] Interestingly, coherence times predict that these gates should still be much better, and it is still an open question as to what is the limitation.[66]

There have been many variants of entangling two-qubit gates for superconducting qubits, each with their own set of pros and cons. We find it convenient to split the gates into two classes. One class of gates contains all of those which rely on the dynamical

flux-tunability of either the underlying qubits or some separate sub-circuit. This includes the direct-resonant iSWAP,[67,68] and the higher-level resonance-induced dynamical c-Phase (DP).[14,42] The second class of gates contains all those in which the qubits have fixed frequencies and microwave sources are used to activate the interaction. The gates in this class include the resonator sideband-induced iSWAP,[69] the cross-resonance (CR) gate,[13] the Bell-Rabi,[70] the mircowave activated phase gate,[71] and the driven resonator-induced c-Phase (RIP).[72]

The primary advantage of the dynamically tunable class of gates is the ability to operate the qubits in very different regimes: one in which the qubits are independent with negligible interaction, and one where the two-qubit interaction is maximized. In the first regime, single-qubit gates can be applied trivially without the need for specialized decoupling schemes as the qubits will not experience significant crosstalk errors. In the second regime, the qubits can be tuned to optimize the two-qubit interaction so as to enable the shortest possible gate times. This allows simple single-qubit gates, the possibility of strong two-qubit interactions, and low crosstalk errors. The main disadvantages of such gates are the reliance on flux-tunable qubits, which can have reduced coherence times due to flux-noise,[73] the risk of interacting with other energy levels in the system during tuning, and additional circuit and control complexity due to on-chip tunable flux controls or couplers which support dynamical tunability.

For the case of the microwave two-qubit gates, the qubits are fixed in frequency, and thereby can be parked at 'sweet-spots' of coherence or made to be untunable. Furthermore, the addressing hardware and shaped-microwave controls become analogous to those of single-qubit gates. There is additional circuit complexity for some of the schemes, specifically CR gates require local microwave addressability for each qubit. The most significant disadvantages for the fixed-frequency gates are tradeoffs to either coherence or single-qubit control in order to have stronger two-qubit interactions. For example, in the CR gate the qubit-qubit detunings which would give the strongest two-qubit interaction, also happen to result in reduced single-qubit addressability. This potentially could be overcome by optimal control.

Fast high-fidelity two-qubit gates is still an open area of research, although great progress has been made with the DP gate[14] achieving 6×10^{-3} and we have achieved $9(2) \times 10^{-3}$ with the CR gate[74] and 2×10^{-2} with RIP.[75] Moving forward, these gates need to be made better and a good goal for the field is to achieve errors below 10^{-4}, ~100 times less than the RSC threshold so that the overhead is not too large. As these fidelities continue to improve, important questions emerge in verification and validation. It becomes critical to bound the errors for different characterization methods: for example, although randomized benchmarking[76,77] has become a standard for the field, it is also known that this method fails to pick out particular types of errors.[78]

READOUT OF SUPERCONDUCTING QUBITS

To discern the state of a superconducting qubit, it has become standard to use a dispersive interaction with a resonator.[79–81] This interaction results in a dispersive shift that causes the frequency of the resonator to change depending on the state of the qubit.[81] The resonator frequency is interrogated with a microwave pulse, typically at a frequency near the midpoint of the resonant frequencies corresponding to the ground and excited states, and the phase and amplitude of the reflected signal are used to distinguish the state of the qubit. The appropriate discrimination techniques (including machine learning[33]) and optimal control protocols for depopulation and resetting of the cavity states[82] are areas of important exploration for realizing repetitive error correction protocols required for syndrome detection.

However, a large part of the focus for improving readout is dealing with the circuitry after the resonator, including elements such as filters and amplifiers. Purcell filters[54–56] are commonly used to reduce the probability of the qubit to undergo spontaneous emission (and hence excited state relaxation) by changing the coupled external environment at the frequency of the qubit. Although original incarnations[83] had a very small frequency bandwidth of protection, since then better designs have allowed for larger bandwidth versions[55,56] which should allow for T_1 to be in principle well over 10 ms, while still having enough signal for high-fidelity readout.

Quantum limited amplifiers are used to further boost the readout resonator signals, and a number of parametrically-driven options are now widely available. These includes Josephson parametric amplifiers, which incorporate a microwave resonator with an inherent non-linearity, parametrically driven so as to activate a four-wave-mixing effect.[28] Other amplifiers also incorporate three-wave mixing via a Josephson-ring modulator, with the added benefits of frequency conversion[84,85] or non-reciprocity.[86] Besides these amplifiers which add the minimal half-photon of quantum noise, near quantum-limited amplification with demonstrated directionality are also being investigated using traveling-wave effects and SQUIDs.[30,87,88] In total, the level of sophistication for qubit-readout amplifiers has matured significantly such that high-fidelity single-shot readout is a well-known experimental technique.

TECHNICAL CHALLENGES AHEAD

The technical advances over the last 15 years for superconducting qubits have been astounding. However, it is important to ask what is now necessary for a demonstration of quantum computing on a modest-sized system and what such a demonstration might look like. With current experiments scaling into a double-digit number of qubits, a lattice of O(100) physical qubits which can perform QEC experiments is well within possibility in the near term. Such a system would serve as an invaluable learning tool not just for testing the feasibility of QEC, but also for enabling insight into how to scale a system to the next level of 10^4–10^8 physical qubits. With such numbers of physical qubits, some of the canonical quantum algorithms could possibly be tested in a universal fault-tolerant system. Getting to this important intermediary stage of O (100) qubits would represent a major stepping stone towards bringing the next level of quantum computing to reality.

There are still a number of important technological challenges to address to successfully demonstrate an O(100) qubit system. Aside from advances in coherence times, optimal control and calibration routines for high-fidelity quantum gates, the following list represents other critical areas for exploration and advancement:

Breaking the plane

Arrangements of multi-qubit devices to date have been limited to a single physical plane. This has serious limitations for systems beyond an $n \times 2$ *square* lattice. In such a scenario, qubits on the interior of the grid require a path in and out for addressability. There are many options for breaking this 'third dimension' ,which include standard silicon-based lithographic techniques such as thru-silicon-vias, a flip-chip multi layer stack, or employing waveguide package resonance modes.[89] Ultimately, the solution must also be cryogenically compatible, preserve coherence times and gate fidelities, while not also introducing any new loss mechanisms.

Substrate modes

The device substrate size will need to increase in order to accommodate a larger number of qubits. Due to the boundary

conditions of the substrate die, it will host electromagnetic modes that decrease in frequency for increasing sizes. These modes can facilitate both cross-talk between pairs of qubits in the plane and a reduction in coherence times. While at the moment this problem can be circumvented by clever design, this challenge in the long term is an outstanding question. Metallic vias are a potential route, although these must be cryogenically compatible and the additional fabrication processing and materials must also not negatively impact coherence times.

On-chip microwave integrity

As the complexity of the network grows, it becomes more difficult to insure that broken ground planes in the designed network are still properly tied together at relevant microwave frequencies. Improper grounding can result in undesired slot-line modes and other spurious microwave resonances, which again will lead to cross-talk and reduced coherence. Air-bridge cross-overs,[90] vias, and flip-chip lids[91] are all potential paths towards improved microwave integrity.

Josephson-junction reproducibility and accuracy

In a large network of qubits, variations in the qubit frequency will lead to undesired frequency collisions of the fundamental and higher levels. Such collisions can lead to strong correlated interactions, leakage effects, and addressability errors. Currently, numerical simulations of qubit device designs have allowed an accurate prediction of the qubit capacitance and the couplings. However, fluctuations in the critical current of the JJ are currently on the order of 10%, which result in an ~280 MHz variation in our designed qubits. This is a substantial spread, which will only be improved through more reliable JJ fabrication. Another aspect is the long-term critical current variability of fabricated JJs, and investigating what might influence perturbations on successive experimental cooldowns.

Extensible control and readout hardware

With current qubit network devices, the usage of commercial-off-the-shelf (COTS) equipment for control and readout is not yet cost prohibitive. However, moving towards O(100) networks would require a substantial lowering of the cost per qubit. This can be achieved by shifting from COTS towards customized and targeted electronics solutions. Nonetheless, another important caveat to consider is the overall noise performance for different hardware (e.g. phase, amplitude noise), and ensuring that these would not limit ever-decreasing gate and readout error rates. The extensibility of readout hardware for the application towards QEC also hinges upon having low latency, and the ability to perform a full qubit state discrimination, meter and qubit reset, at a fast desired measurement rate. This could potentially involve customized design for fast-feedback on FPGAs, which are also amenable to programming new concepts for discrimination.[33]

Cryogenic system integrity

Larger devices also mean more signal-carrying wires and ancillary microwave equipment, which all sit inside of a dilution refrigerator. The cryogenic load will need to be handled with care, especially in the proper appropriation of filtering, attenuation, isolation, and amplification so as to not degrade any coherence times, while providing the ability to perform fast and high-fidelity operations. The exact engineering of the cryogenic system environment (e.g. thermalization, impedance matching, infrared radiation shielding[57,58,92]) and paths towards reduction of component size and mass for isolators, amplifiers, circulators, etc., are important topics of open study.

System calibration

State-of-the-art high-fidelity gate experiments[66,93] have already shown that the accuracy of gates can crucially depend on the ability to calibrate all necessary microwave pulse parameters. How, then, will the complexity of the calibration set grow with system size? With more connected qubits, the possibility of correlated errors increases, and new sequences need to be developed to ensure that these play no significant effect on the performance of the independent controls. Determining how to make robust and extensible system calibrations will be critical for high-performance experiments.

Verification & validation

Tools currently exist to measure the accuracy of one-qubit or two-qubit gates in a relatively straightforward manner. These can in principle be extended to larger systems but typically scale exponentially with increasing number of qubits[94] or give only partial information.[76,77,95] Moving forward, tools that determine how accurate quantum gates operate on a subset of a larger fabric of qubits will have relevance for QEC. One current technique, simultaneous benchmarking,[96] is a starting point, but it is not yet clear how sensitive it can be towards adverse errors. Overall, verification and validation methods will likely grow from boot-strapping techniques on smaller subsystems, extended upwards towards larger lattices.

New QEC codes

Even though the surface code and its variants are very attractive for guiding current experiments, there is still a significantly large overhead associated with proper functioning, especially when going towards logical qubit operations. The community is actively working towards reducing this overhead through either finding new codes with inherent universal transversal operations[45,46] or reducing the requirements for magic state distillation.[97,98]

Software

In the end, when an O(100) system is built, how would such a system be operated? It still remains to be seen what will be the assembly language of such a quantum network, to take simple instruction sets in a user-defined program, to be translated into sequences of microwave and/or flux signals that are applied to the qubits directly. Moving forward, a standardized software and compiler code-base will need to be developed.

CONCLUSION

In conclusion, the road towards a full-scale universal quantum computer with fault-tolerant error correction will be long, dark, but filled with exciting challenges. However, in the near future, systems of O(100) qubits are within reach and already beyond what can be emulated in full generality on a classical computer. This will usher in a new era in quantum information science, with explicit hardware to match broad ideas in theory, and culminate in the demonstration of a useful logical memory. A very promising route forward is the RSC, offering simplicity in the network, implemented with superconducting qubits, which has shown tremendous and rapid progress in coherence times, controls, and readout. The challenges that we outlined in this review, while difficult, are not insurmountable and with clever engineering and new insights we believe the road ahead is lit.

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COMPETING INTERESTS

The authors declare that they have no competing interests.

REFERENCES

1. Shor, P. W. *SIAM J. Comput.* **26**, 1484 (1997).
2. Grover, L. K. *Phys. Rev. Lett.* **79**, 325 (1997).
3. Yung, M. H., Whitfield, J. D., Boixo, S., Tempel, D. G., and Aspuru-Guzik, A. in *Advances in Chemical Physics*, Vol. 154 (ed. Kais, S.) (Wiley, 2014).
4. Aharonov, D. & Ben-Or, M. in *Proceedings of the Twenty-Ninth Annual ACM Symposium on Theory of Computing*, STOC 97 176–188 (ACM, 1997).
5. Preskill, J. Fault-tolerant quantum computation. Preprint at arXiv:quant-ph/9712048v1 (1997).
6. Kitaev, A. *Ann. Phys.* **303**, 2 (2003).
7. Bravyi, S. B. & Kitaev, A. Y. Quantum codes on a lattice with boundary. Preprint at arXiv:quant-ph/9811052v1 (1998).
8. Raussendorf, R. & Harrington, J. *Phys. Rev. Lett.* **98**, 190504 (2007).
9. Fowler, A. G., Mariantoni, M., Martinis, J. M. & Cleland, A. N. *Phys. Rev. A* **86**, 032324 (2012).
10. Dennis, E., Kitaev, A., Landahl, A & Preskill, J. *J. Math. Phys.* **43**, 4452 (2002).
11. Raussendorf, R., Harrington, J. & Goyal, K. *New J. Phys* **9**, 199 (2007).
12. Horsman, C., Fowler, A., Devitt, S., & Meter, R. V. *New J. Phys.* **14**, 123011 (2012).
13. Chow, J. M. *et al. Phys. Rev. Lett.* **109**, 060501 (2012).
14. Barends, R. *et al. Nature* **508**, 500 (2014).
15. Harty, T. P. *et al. Phys. Rev. Lett.* **113**, 220501 (2014).
16. Nigg, D. *et al. Science* **345**, 302 (2014).
17. Corcoles, A. D. *et al. Nat. Commun.* **6**, 6979 (2015).
18. Riste, D. *et al. Nat. Commun.* **6**, 6983 (2015).
19. Kelly, J. *et al. Nature* **519**, 66 (2015).
20. Devoret, M. H. & Schoelkopf, R. J. *Scisence* **339**, 1169 (2013).
21. Ospelkaus, C. *et al. Nature* **476**, 181 (2011).
22. Shulman, M. D. *et al. Science* **336**, 202 (2012).
23. Zwanenburg, F. A. *et al. Rev. Mod. Phys.* **85**, 961 (2013).
24. Gumann, P. *et al. Phys. Rev. Lett.* **113**, 267604 (2014).
25. Lu D. *et al. Phys. Rev. Lett.* **114**, 140505 (2015).
26. Martin-Lopez, E. *et al. Nat Photon* **6**, 773 (2012).
27. Maller, K. M. *et al. Phys. Rev.* A **92**, 022336 (2015).
28. Hatridge, M., Vijay, R., Slichter, D. H., Clarke, J. & Siddiqi, I. *Phys. Rev. B* **83**, 134501 (2011).
29. Abdo, B., Schackert, F., Hatridge, M., Rigetti, C. & Devoret, M. *Appl. Phys. Lett.* **99**, 162506 (2011).
30. Hover, D. *et al. Appl. Phys. Lett.* **104**, 152601 (2014).
31. Riste, D., Bultink, C. C., Lehnert, K. W. & DiCarlo, L. *Phys. Rev. Lett.* **109**, 240502 (2012).
32. Vijay, R. *et al. Nature* **490**, 77 (2012).
33. Magesan, E., Gambetta, J. M, Corcoles, A. D. & Chow, J. M. *Phys. Rev. Lett.* **114**, 200501 (2015).
34. Hornibrook, J. M. *et al. Appl. Phys. Rev.* **3**, 024010 (2015).
35. Bombin, H. & Martin-Delgado, M. A. *Phys. Rev. A* **76**, 012305 (2007).
36. Gambetta, J. & Smolin, J. Frequency arrangement for surface code on a superconducting lattic US Patent 9,111,230 (2015).
37. Edmonds, J. *Canad, J. Math.* **17**, 449–467 (1965).
38. Majer, J. *et al. Nature (London)* **449**, 443 (2007).
39. Sillanpaa, M. A., Park, J. I. & Simmonds, R. W. *Nature (London)* **449**, 438 (2007).
40. Chow, J. M. *et al. Nat Commun* **5**, 4015 (2014).
41. Chow, J. M. *et al. Phys. Rev. Lett.* **107**, 080502 (2011).
42. DiCarlo, L. *et al. Nature* **460**, 240 (2009).
43. Bravyi, S. & Konig, R. *Phys. Rev. Lett.* **110**, 170503 (2013).
44. Bravyi, S. & Kitaev, A. *Phys. Rev. A* **71**, 022316 (2005).
45. Bravyi, S. & Cross, A. Doubled color codes.Preprint at arXiv:1509.03239 (2015).
46. Jochym-O'Connor, T. & Bartlett, S. D. *Phys. Rev. A* **93**, 022323 (2016).
47. Dawson, C. M. & Nielsen, M. A. The solovay-kitaev algorithm. Preprint at arXiv: quant-ph/0505030 (2005).
48. Kliuchnikov, V., Maslov, D. & Mosca, M. *Quantum Info. Comput.* **13**, 607 (2013).
49. Selinger, P. *Quantum Info. Comput.* **15**, 159 (2015).
50. Clarke, J. & Wilhelm, F. K. *Nature* **453**, 1031 (2008).
51. Koch, J. *et al. Phys. Rev. A* **76**, 042319 (2007).
52. Nakamura, Y., Pashkin, Y. A. & Tsai, J. S. *Nature* **398**, 786 (1999).
53. Houck, A. *et al. Phys. Rev. Lett.* **101**, 080502 (2008).
54. Reed, M. D. *et al. Appl. Phys. Lett.* **96**, 203110 (2010).
55. Jeffrey, E. *et al. Phys. Rev. Lett.* **112**, 190504 (2014).
56. Bronn, N. T. *et al. Applied Physics Letters* **107**, 172601 (2015).
57. Barends, R. *et al. Appl. Phys. Lett.* **99**, 113507 (2011).
58. Corcóles, A. D. *et al. Appl. Phys. Lett.* **99**, 181906 (2011).
59. Martinis, J. M. *et al. Phys. Rev. Lett.* **95**, 210503 (2005).
60. Wenner, J. *et al. Appl. Phy. Lett.* **99**, 113513 (2011).
61. Wang, C. *et al. Appl. Phys. Lett.* **107**, 162601 (2015).
62. Dial, O. *et al. Superconductor Science and Technology*, **29**, 044001 (2016).
63. Chow, J. M. *et al.* in Proc. SPIE 9500, Quantum Information and Computation XIII, 95001G (2015).
64. Barenco, A. *et al. Phys. Rev. A* **52**, 3457 (1995).
65. Motzoi, F., Gambetta, J. M., Rebentrost, P. & Wilhelm, F. K. *Phys. Rev. Lett.* **103**, 110501 (2009).
66. Sheldon, S. *et al. Phys. Rev. A* **93**, 012301 (2016).
67. Bialczak, R. C. *et al. Nat Phys* **6**, 409 (2010).
68. Dewes, A. *et al. Phys. Rev. Lett.* **108**, 057002 (2012).
69. Leek, P. J. *et al. Phys. Rev. B* **79**, 180511 (2009).
70. Poletto, S. *et al. Phys. Rev. Lett.* **109**, 240505 (2012).
71. Chow, J. M. *et al. New J. Phys.* **15**, 115012 (2013).
72. Cross, A. W. & Gambetta, J. M. *Phys. Rev. A* **91**, 032325 (2015).
73. Yoshihara, F., Harrabi, K., Niskanen, A. O., Nakamura, Y. & Tsai, J. S. *Phys. Rev. Lett.* **97**, 167001 (2006).
74. Sheldon, S., Magesan, E., Chow, J. M. & Gam-betta, J. M. *Phys. Rev. A* **93**, 060302 (2016).
75. Paik, H. *et al. Phys. Rev. Lett.* **117**, 250502 (2016).
76. Knill, E. *et al. Phys. Rev. A* **77**, 012307 (2008).
77. Magesan, E., Gambetta, J. M. & Emerson, J. *Phys. Rev. Lett.* **106**, 180504 (2011).
78. Epstein, J. M., Cross, A. W., Magesan, E. & Gambetta, J. M. *Phys. Rev. A* **89**, 062321 (2014).
79. Blais, A., Huang, R.-S., Wallraff, A., Girvin, S. M. & Schoelkopf, R. J. *Phys. Rev. A* **69**, 062320 (2004).
80. Wallraff, D. I. *et al. Nature (London)* **431**, 162 (2004).
81. Gambetta, J. *et al. Phys. Rev. A* **77**, 012112 (2008).
82. McClure, D. T. *et al. Phys. Rev. Applied* **5**, 011001 (2016).
83. Reed, M. D. *et al. Appl. Phys. Lett.* **96**, 203110 (2010).
84. Bergeal, N. *et al. Nat Phys* **6**, 296 (2010).
85. Abdo, B., Kamal, A. & Devoret, M. *Phys. Rev. B* **87**, 014508 (2013).
86. Abdo, K. *et al. Phys. Rev. Letters* **112**, 167701 (2014).
87. Ho Eom, B., Day, P. K., LeDuc, H. G., & Zmuidzinas, J. *Nat Phys* **8**, 623 (2012).
88. O'Brien, K., Macklin, C., Siddiqi, I. & Zhang, X. *Phys. Rev. Lett.* **113**, 157001 (2014).
89. Minev, Z. *et al. Phys. Rev. Applied* **5**, 044021 (2016).
90. Chen, Z. *et al. Appl. Phys. Lett.* **104**, 052602 (2014).
91. Abraham, W. *et al.* Removal of spurious microwave modes via flip-chip crossover. US Patent Application No. 20,140,264,287 (2014).
92. Rigetti, C. *et al. Phys. Rev. B* **86**, 100506 (2012).
93. Kelly, J. *et al. Phys. Rev. Lett.* **112**, 240504 (2014).
94. Chuang, L. & Nielsen, M. A. *J. Mod. Opt.* **44**, 2455 (1997).
95. Magesan, J. M. *et al. Phys. Rev. Lett.* **109**, 080505 (2012).
96. Gambetta, M. *et al. Phys. Rev. Lett.* **109**, 240504 (2012).
97. Bravyi, S. & Haah, J. *Phys. Rev. A* **86**, 052329 (2012).
98. Jones, C. *Phys. Rev. A* **87**, 042305 (2013).

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